# TRAVELING WAVES-BASED FAULT DETECTION AND LOCATION IN MULTI-TERMINAL HIGH VOLTAGE DC SYSTEMS

by

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# ABSTRACT

BHASKAR MITRA. Traveling Waves-Based Fault Detection and Location in Multi-Terminal High Voltage dc Systems. (Under the direction of DR. BADRUL CHOWDHURY)

An advanced electricity infrastructure for efficient and reliable delivery of offshore renewable energy to onshore grids calls for High Voltage direct current (HVdc) transmission networks. With the advancement of power electronics, HVdc networks have evolved from point-to-point two terminals to Multi-Terminal direct current (MTdc) networks. For efficient operation of MTdc networks, fast and accurate methods of fault detection and isolation is a necessity. Traditional ac breakers fail to protect the system from dc faults due to their slow operational speed. The dc faults if not detected and removed can cause catastrophic damages to the network. This dissertation analyses the several stages of a dc fault and their impacts. Several specially designed dc breaker studies have been performed and evaluated. Hybrid dc circuit breaker (dcCB) has been found to be a viable choice for dc fault interruption owing to its fast operation and lower conduction losses. The major contributions of this dissertation are: (1) Spectral analysis of traveling waves using wavelet transform to detect faults; (2) Development of an efficient and robust non-communication-based algorithm for detection of fault; and finally (3) A non-intrusive method of fault location by analyzing the natural decay of line current after proper fault detection and isolation.

Due to the absence of reactance in dc transmission lines and cables the rate of rise of fault current is high. Thus, the window of fault detection is very short for dc systems. Fault detection in dc systems is challenging due to the presence of common terminals and is affected by sensitivity and reliability issue with existing algorithms. This dissertation analyses the effects of faults on HVdc transmission systems and proposes two methods based on traveling wave detection through application of wavelet

transform and also by the direction of arrival of current and voltage transients for efficient fault detection. Traveling wave are generated at the onset of faults. These fault transients are highly informative and help to provide us with the idea of time and location of the faults. With the application of wavelet transform, these transient signals are analyzed to detect and isolate the faults using hybrid dc breakers.

Present communication technologies do not work faster than the speed of fault propagation. Most of the suggested fault detection methods require communication for efficient operation. Post-fault voltage and current are comprised of a transient portion from the generated traveling waves on the pre-fault voltage and current. By isolating the current and voltage transients and analyzing their direction of arrival at the hybrid dcCB's, a faulted section of the network can be determined. All the connected dc breakers are operated individually, and the proposed methodology helps to prevent any misoperation of the breakers even on ac side faults.

Finally, MTdc networks are installed in remote locations. Proper location of fault is a challenge. The natural dissipation of the circuit parameters is considered for fault location. A relationship between the natural frequency of oscillation of the fault current and fault location has been established. The hybrid dcCB interrupts the fault current and the line current attenuates under the absence of any driving voltage source. The line capacitance discharges into the fault at a damping frequency and a rate of attenuation. Utilizing these information's, the fault location in a MTdc network is achieved.

With the current advancements in MTdc network installations for off-shore renewable energy integration, the proposed fault detection and location techniques can be utilized to develop resilient and robust networks. All the proposed methods were justified theoretically and their performances were evaluated through simulation studies.

# DEDICATION

*To,*

My father (Mr. Sujoy Mitra), mother (Mrs. Anjana Mitra), my wife (Mrs. Mukulika Bose), my in-laws (Adv. Somenath Bose and Mrs. Kantasree Basu), my late grandparents (Joydeb Mitra, Biju Rani Mitra, Ajit Kumar Bose and Chanda Bose), my sister (Mrs. Sayantanee Basu), my brother-in-law (Mr. Rubel Ghosh) and last but not the least Mrs. Stephanie LaClair Brilliante.

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I would like to thank my advisor Dr. Badrul Chowdhury for providing me with the opportunity to perform research and his support. His guidance and direction made an indelible impact for my vision towards research. I would also like to thank the members of my dissertation committee members Dr. Madhav Manjrekar, Dr. Tiefu Zhao, Dr. Andrew Willis and Dr. Wesley Williams, they have been ever present with useful tips and helpful insights. Dr. Andrew Willis has been an amazing mentor, endless hours of discussion with him have been always fruitful. Teachings from Dr. Robert Cox is something I would like to take with me and hopefully become an amazing professor like him one day.

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I would like to end with a quote from late Dr. A.P.J. Abdul Kalam, the former President of India, "Dream is not that which you see while sleeping it is something that does not let you sleep".

TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# LIST OF ABBREVIATIONS

ac alternating current

ACSB Active Short Circuit Breaker

ADC Analog-to-Digital Converter

ADS Accessory Discharge Switch

AI Artificial Intelligence

ASCB Active Short Circuit Breaker

CSC Current Source Converter

CWT Continuous Wavelet Transform

DAE Differential Algebraic Equation

dc direct current

dcCB direct current Circuit Breaker

DFT Discrete Fourier Transform

DSP Digital Signal Processing

DWT Discrete Wavelet Transform

EMTDC Electro Magnetic Transients including Direct Current

FFT Fast Fourier Transform

FIR Finite Impulse Response

GPS Global Positioning System

HHT Hilbert Huang Transform

HVac High Voltage alternating current

HVdc High Voltage direct current

IGBT Insulated Gate Bipolar Transistor

KVL Kirchhoff's Voltage Law

LCC Line Commutated Converter

LCS Load Commutation Switch

LR Linear Regression

LVdc Low Voltage direct current

MB Main Breaker

MMC Modular Multilevel Converter

MOV Metal Oxide Varistor

MRA Multi-Resolution Analysis

MTdc Multi-Terminal direct current

PMU Phasor Measurement Unit

PPU Power Probe Unit

PSCAD Power System Computer Aided Design

PWM Pulse Width Modulation

ROCOV Ratio of Change of Reactor Voltage

SM Sub Module

SNR Signal Noise Ratio

STFT Short Time Fourier Transform

SVM Support Vector Machine

UFD Ultra-Fast Disconnect

VSC Voltage Source Converter

# CHAPTER 1: INTRODUCTION

The push for integrating offshore renewable energy with the existing grid infrastructure is transforming the modern electrical grid. Onshore energy consumption increases the distance between offshore renewable energy generation and site of consumption, thereby, increasing the cost of transmission [1].

For high power transmissions over long distances, initially High Voltage alternating current (HVac) systems were utilized. High transmission losses proved to be a barrier for using HVac transmission. The resistance of dc cables are lower than that of ac cables, that leads to lower losses [2]. With the first HVdc transmission systems being established in the 1950s, there has been a considerable growth in its implementation over the years across the world. The inherent advantages offered by HVdc over HVac made it a popular and economically viable option for power transmission over long distances. Current and proposed projects related to HVdc networks are shown in Figure 1.1 [3]. Table 1.1 shows the vast network of HVdc systems currently in use and proposed for future installations [3].

HVdc converter stations were initially modeled as Current Source Converter (CSC) stations, simple two-terminal point-to-point networks [4]. With the advancement of power electronics and development of Voltage Source Converter (VSC) HVdc stations, there has been a rise in the installation of MTdc systems. The CSC stations are also referred as Line Commutated Converter (LCC) stations, designed using thyristor valves utilizing the frequency of the ac grid. Due to their nature of low switching frequency, the LCC stations resulted in lower switching losses and could sustain the dc-side faults, preventing the ac grid to feed into the dc faults. VSC HVdc stations are modelled using Insulated Gate Bi-polar Transistor (IGBT) switches controlled by

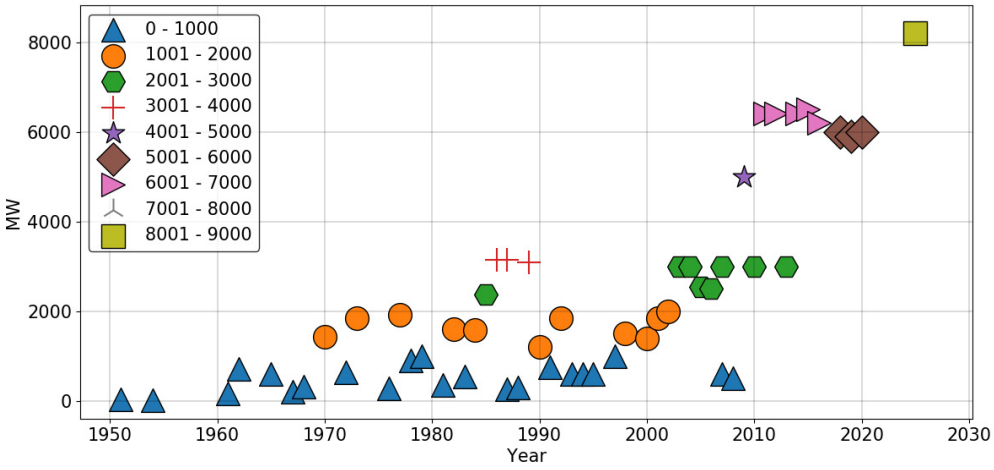


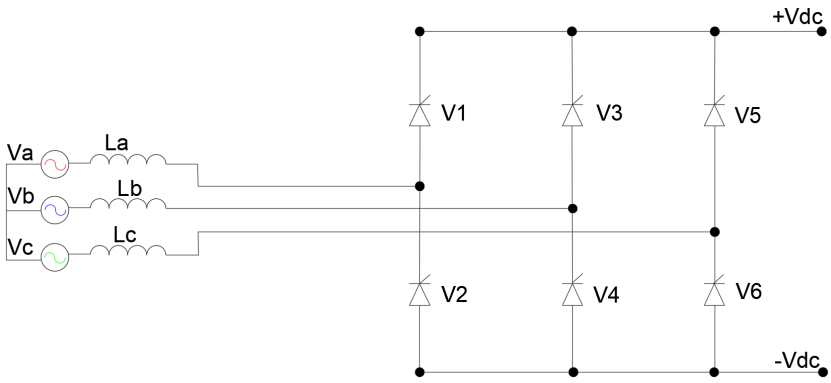

Figure 1.1: HVdc projects over the years

Table 1.1: List of some HVdc projects

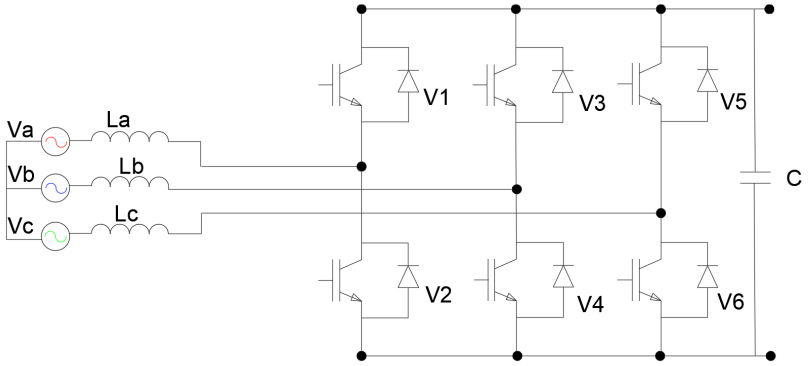
| **Continent** | **Project** |
|---|---|
| North America | Pacific dc Intertie |
| | Trans Bay Cable |
| | Eastern Alberta Transmission Link |
| South America | Belo Monte HVdc |
| | Melo B2B |
| | Rio Madeira |
| Africa and Middle East | Cahora Bassa |
| | Inga Shaba |
| | Ethiopia - Kenya (Under Construction) |
| Indian Subcontinent | Northeast Agra |
| | Rihand-Delhi |
| | Chandrapur B2B |
| Europe | Borwin 1,2 & 3 |
| | Dolwin 1,2 & 3 |
| | NorNed |
| China, Japan and South East Asia | Jinping-Suan |
| | Three Gorges - Guangdong |
| | Qinhai - Tibet |

Pulse Width Modulation (PWM) controllers. The fully controllable IGBT switches provide the advantage of bi-directional power flow and self-active and reactive power control. The ability to control dc and ac voltages provides the advantage of connecting with weak ac grids.

Despite the advantages, VSC HVdc systems suffer from the limitation of protection from high dc fault currents. VSC HVdc designs are vulnerable to fault currents, the anti-parallel diodes of the IGBT switches provide a path for the current to be free-wheeled and the fault current continues to be fed from the source [5]. LCC based systems on the other hand are self-commutating as the thyristor pairs are reverse biased, thus preventing the increase of the dc fault current [6]. These vulnerabilities of the VSC HVdc have motivated research studies to find more efficient and fast methods for fault detection. The schematic representation of CSC and VSC HVdc stations are shown in Figure 1.2(a) and 1.2(b) respectively.




(a) Current source converter




(b) Voltage source converter

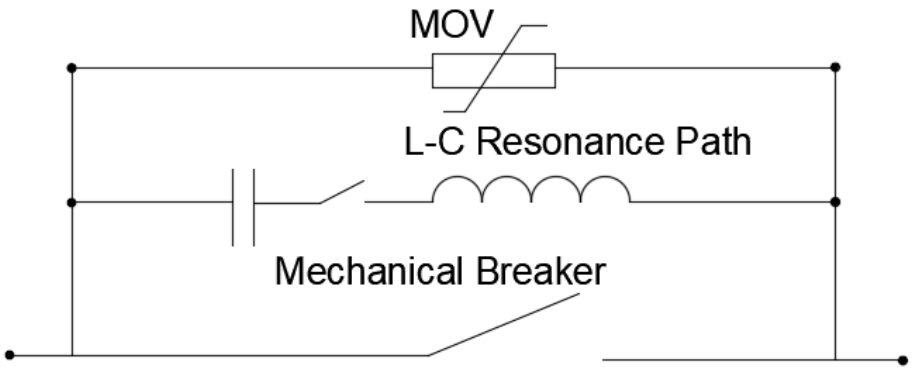
Figure 1.2: Types of HVdc converter stations

Use of traditional ac breakers to interrupt the fault current is not a viable option, since dc currents do not have a natural zero crossing for current interruption. The rate of rise of fault current is faster in dc systems compared to ac systems due to the lack of reactance in the dc cables [7]. The traditional ac breakers require about 5 to 6 cycles to interrupt the fault current [8]. A faster interruption time is necessary for the dc fault current to protect the converter stations and other equipment from damage.

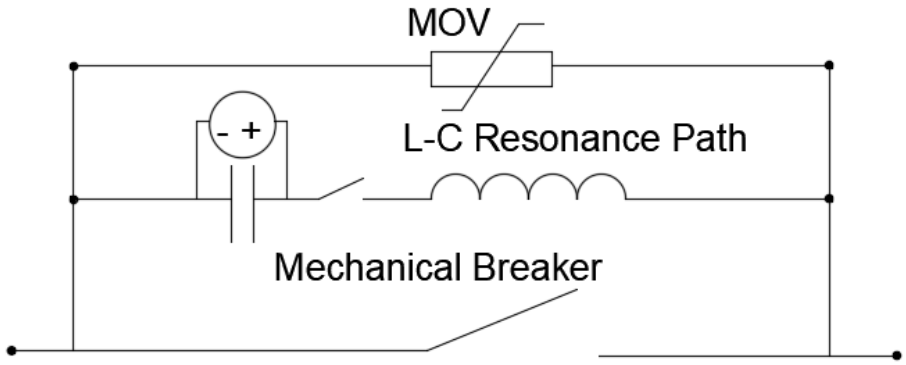
## 1.1 DC Breakers

Passive resonant topology based dc breakers have been prototyped and ha used over the years [9]. The interruption time for those breakers are typically between

30-100ms. During this time period the dc fault current would rise 20 times of its rated value [10]. Active resonant type breakers offer a higher interruption of the fault current but suffer from the same problem of long interruption time. Schematic diagrams of active and passive resonant breakers are shown in Figure 1.3(a) and (b) respectively.




(a) Passive resonant dc breaker




(b) Active resonant dc breaker

Figure 1.3: Types of resonant dc breakers

Semi-conductor based dc breakers have been used to reduce the interruption time. They have a rapid turn-off capability (using IGBT switches) to interrupt the fault current. A pair of such devices are connected anti-parallel to each other to implement bi-directional flow of current. The solid-state breakers are capable of interrupting the fault current at 0.2ms. The switches are turned off in the event of a fault. However, the major disadvantage is the significant power loss experienced by the

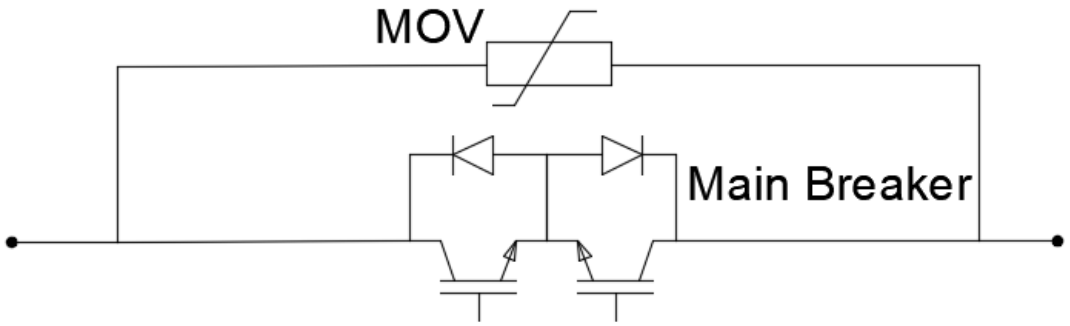



Figure 1.4: Solid state dc breaker.

breaker under normal operating conditions that are significantly higher, due to the on-state conduction loss of the semi-conductor switches. A schematic of the solid-state breaker is shown in Figure 1.4. It has only one path for conduction and interruption, and the Metal Oxide Varistor (MOV) dissipates any excess energy after interruption.

The hybrid dc circuit breaker (dcCB) design, proposed in [11], is similar to that of the solid-state dc breaker, but it has two parallel paths namely auxiliary path and main breaker path. The auxiliary path consists of fewer number of semiconductor devices known as Load Commutation Switch (LCS), and thus reduces the loss during normal operating conditions. A mechanical Ultra-Fast Disconnect (UFD) switch, connected in series with the LCS, helps to transfer the fault current into the main breaker and acts as a protective unit for the LCS during re-connection. A Metal Oxide Varistor (MOV) is in parallel with each section of the main breaker limits the rapid increase of voltage after the main breaker is switched off.

The power losses that incur in a hybrid dcCB are significantly less due to the presence of lower number of IGBT switches in the main conduction path. The fault current transfer in the path of the main breaker is also achieved quicker due to the presence of lower number of semi-conductor switches. Several such devices are connected in series, acting as backup protection units if one of the units fails. A schematic representation of the hybrid dcCB is shown in Figure 1.5. The IGBT

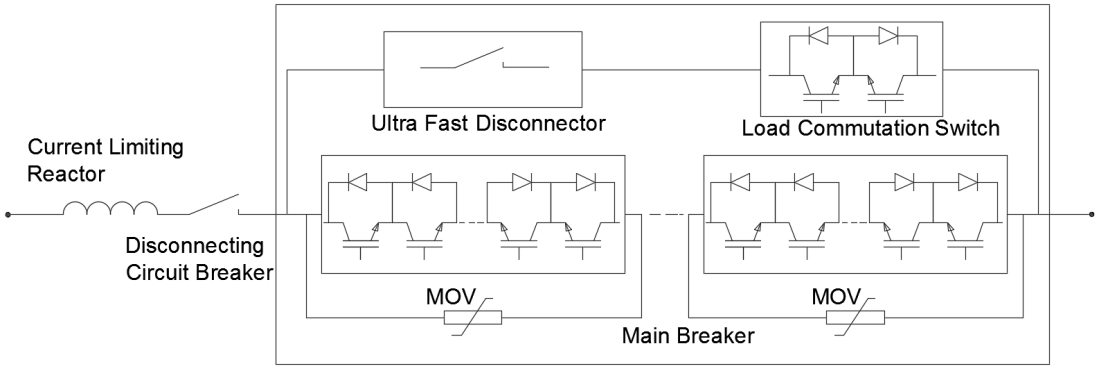



Figure 1.5: Hybrid dc breaker

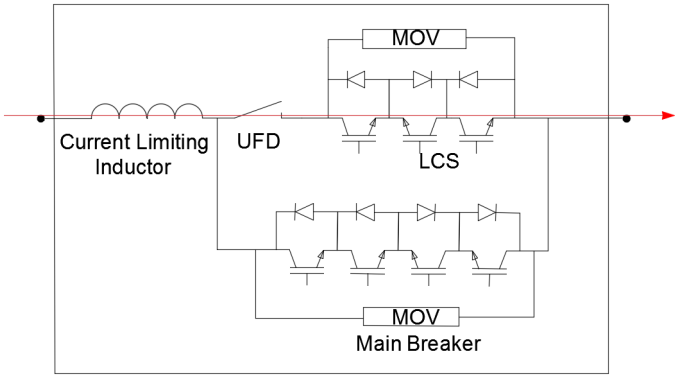
units are placed anti-parallel to each other providing the capability of bi-directional interruption.

For the work on fault detection hybrid dcCB have been utilized and from here on the term breaker will be referred to as the hybrid dcCB unless otherwise mentioned.

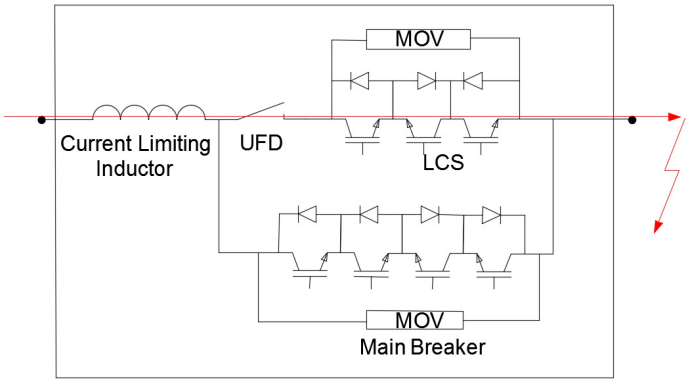
## 1.2 Modes of Breaker Operation

The fault interruption in a breaker is a multi-step process occurring in a sequential manner. This section emphasizes on the physical operation of the dc breaker to isolate a fault.

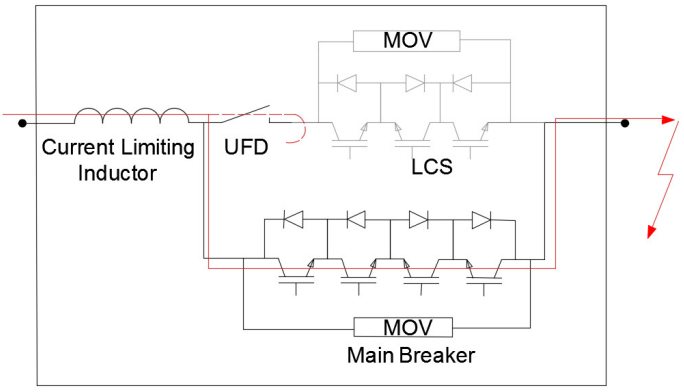
Under normal operating conditions current flows through the UFD and LCS branch, since it is the path of least resistance. Once a fault has been detected, the LCS switches are turned off after a certain duration, and the fault current begins to transfer into the path of the main breaker. When a complete fault current transfer takes place, the UFD is opened under zero current to avoid any arcing. The fault current is finally interrupted at the main breaker (MB) by turning the IGBT switches off, after a certain current threshold is reached. Finally, any excess energy is dissipated at the MOV connected in parallel to the main breakers. The sequential stages of operation are shown in Figure 1.6.




(a) Normal Operating Condition

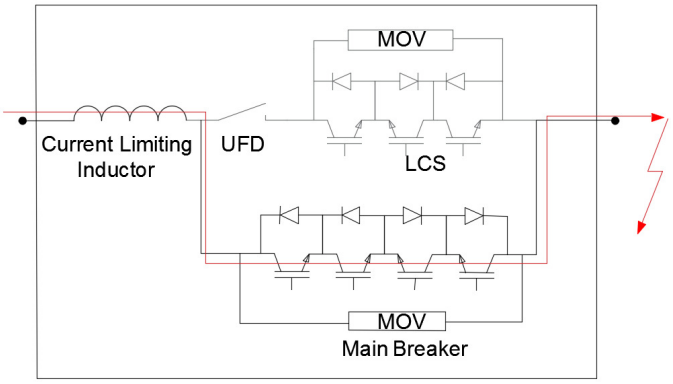



(b) Fault

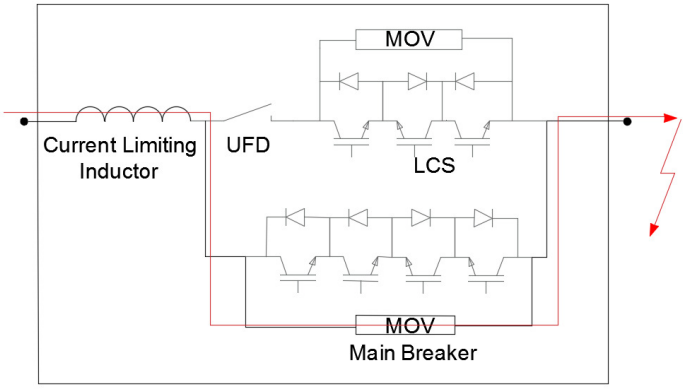



(c) LCS turned off

Figure 1.6: Hybrid dcCB operation




(d) UFD turned off




(e) MB turned off

Figure 1.6: Hybrid dcCB operation (Continued)

## 1.3 Analysis of Hybrid dc Breaker

The stages of operation of the hybrid dcCB has been described in Section 1.2. For a fault occurring at time $t$, a certain amount of time is taken before the fault is detected at time $t_1$. The LCS is commanded to be turned off at $t_1$, and then the fault current begins to transfer to the main breaker. When the fault current has completely transferred to the main breaker branch, the UFD starts to open at $t_2$. Finally, the main breaker is turned off to interrupt the fault current at $t_3$. The rest of the energy from the fault is dissipated by the MOVs and the fault current drops to zero at $t_4$. The operational characteristics of a hybrid dcCB are shown in Figure 1.7.

For efficient design of the dcCB units the peak current interruption periods are taken into consideration. For analysis, the VSC HVdc can be a constant voltage source with inductance $L$. After a fault at time $t$, the fault current flowing through the dcCB is expressed as (1.1);

$$i_{fault} = I + \frac{V_1}{L_{lim} + L_{CLR}}(t - t_1) \tag{1.1}$$

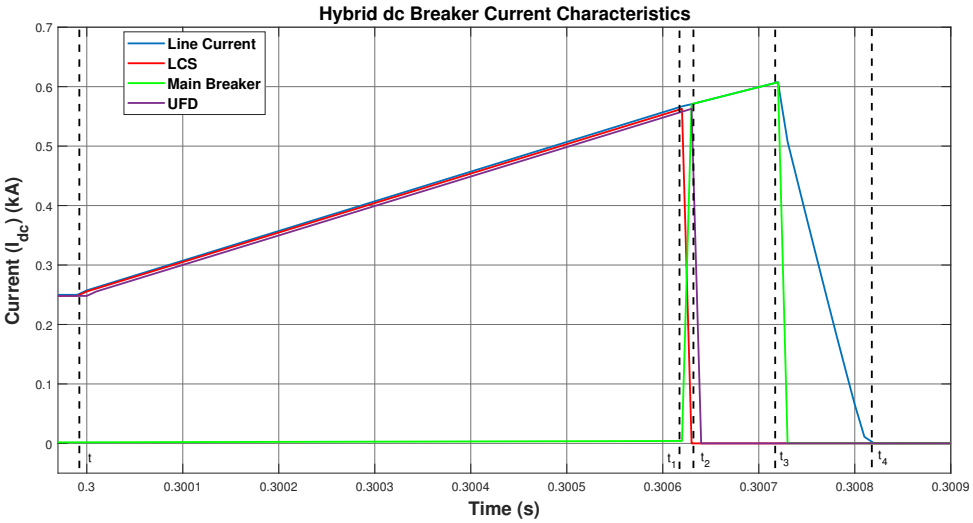
where $V_1$ is the dc voltage of the VSC, $I$ is the cable current, $L_{lim}$ is the current limiting reactor, $L_{CLR}$ is the equivalent arm inductance.

Similarly, the peak currents of LCS and main breaker is given as (1.2) and (1.3) respectively,

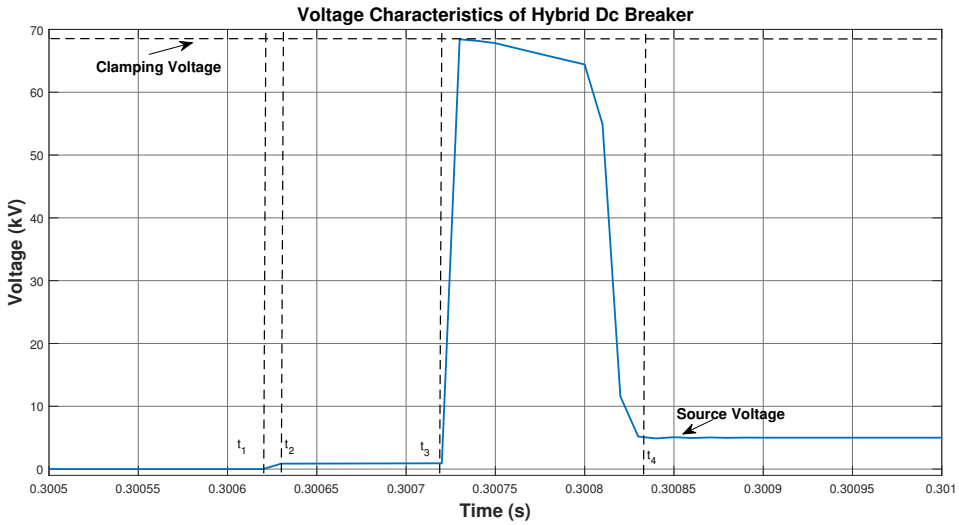
$$i_{LCS} = I + \frac{V_1}{L_{lim} + L_{CLR}}(t_2 - t_1) \tag{1.2}$$

$$i_{MB} = I + \frac{V_1}{L_{lim} + L_{CLR}}(t_3 - t_1) \tag{1.3}$$

As shown in Figure 1.6, the maximum energy dissipated by the MOV happens after the main breaker interruption between $t_3$ and $t_4$. The energy dissipated by each cell




(a) Current characteristics during interruption




(b) Voltage characteristics during interruption

Figure 1.7: Hybrid dcCB operation characteristics

of the MOV is given as (1.4);

$$E_{MOV} = \left[ I + \frac{V_1}{L_{lim} + L_{CLR}} (t_3 - t_1) \right] V_{cell} \left( \frac{t_4 - t_3}{2} \right) \tag{1.4}$$

where $V_{cell}$ is the voltage rating of the main breaker.

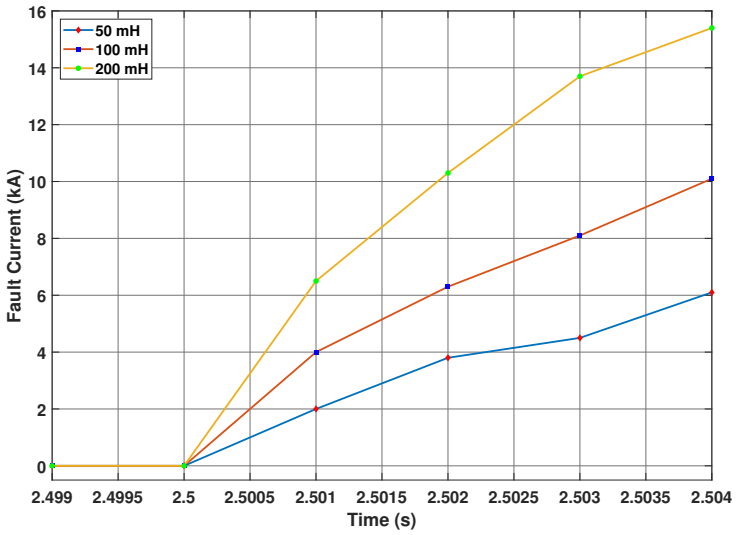



Figure 1.8: Variation in current threshold due to change in inductance

## 1.4 Problem Statement

From the analysis performed in Section 1.3, it can be seen that $t_1$ i.e. the time of fault detection is directly proportional to the peak current ratings of the LCS and Main Breaker (MB) as given by (1.2) and (1.3) respectively. The delay in fault detection results in a higher fault current and thus the ratings of the LCS and MB increase proportionately. Similarly, a larger amount of energy needs to be dissipated by the MOV. Methods using threshold for fault current to trigger the dc breaker has been found to be inefficient. Variations in the current limiting inductance has an impact on the rate of rise of fault current as shown in Figure 1.8. Thus it is difficult to justify a threshold for the fault current.

Similarly, the ratio of change of reactor voltage (ROCOV) method has been suggested, comparing the variation of voltage change across the inductor to detect faults. A variation of change of voltage can be seen with the change of the limiting inductance as shown in Figure 1.9. MTdc networks having common terminals as shown later in Figure 4.2, have similar $di/dt$ and $dv/dt$ making it difficult to isolate faults based on rate of change of voltage or current, as shown in Figure 1.10. The drawbacks

of some other methods are discussed in later Chapters.

This dissertation aims to address the following: in Chapter 2, the vulnerabilities associated with dc side faults and the impact that it can have if the faults are not isolated within a short time. In Chapter 3, methods involving traveling waves, that are independent of the system architecture and other parameters, are suggested. A time-frequency based analysis is also suggested that helps identify the time of fault and initiate the hybrid dc breakers. In Chapter 4, direction of arrival of the current and voltage transients from the traveling waves are utilized to locate the faulted section of the network to avoid any misoperation of the dc breakers that can lead to a shutdown. In Chapter 5, the challenges associated with locating faults in remote MTdc networks are addressed. A novel method for fault location on a transmission line using the natural decay of transmission line current after successful fault detection and isolation is utilized. Finally, in Chapter 6, the dissertation concludes with its major findings and future implications.

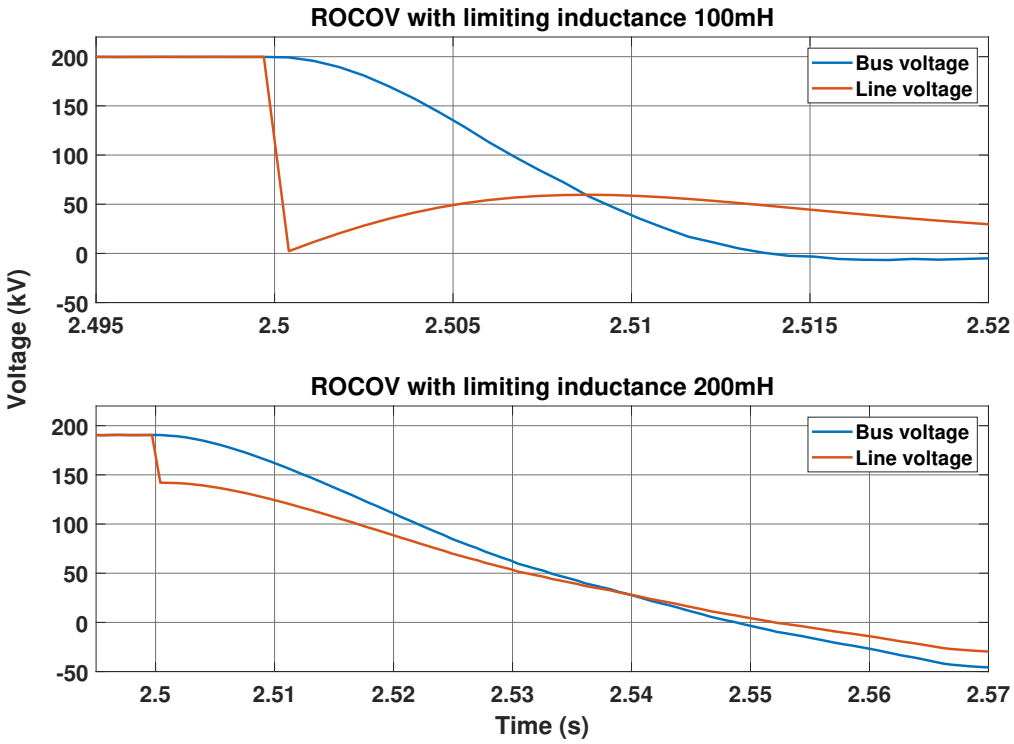



Figure 1.9: ROCOV affected with change of limiting inductance

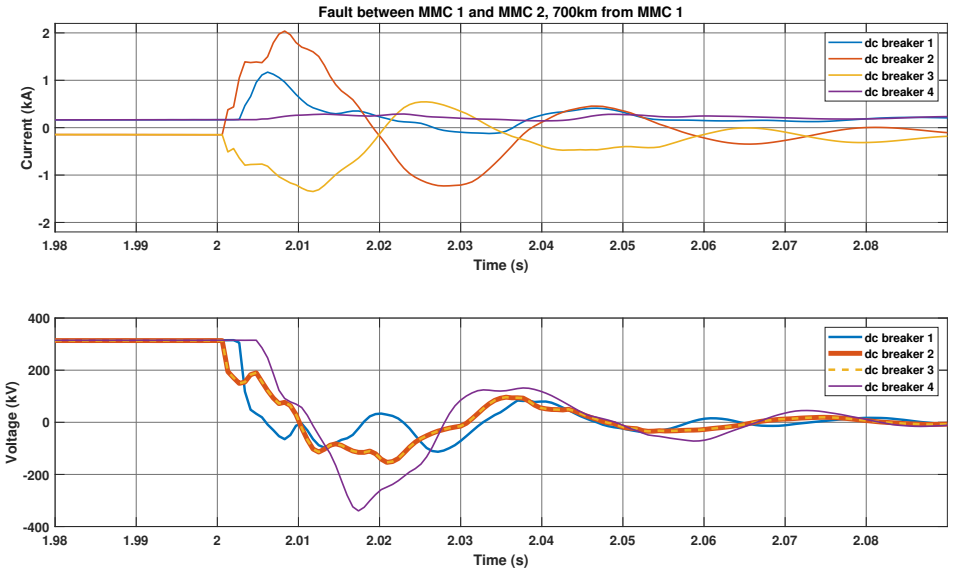



Figure 1.10: Comparison $dv/dt$ and $di/dt$

# CHAPTER 2: DC FAULTS AND THEIR ANALYSIS

A variety of conditions can give rise to dc faults. Insulation deterioration or breakdown has been seen to be one of the most common reasons [12]. Although, multiple other associated factors can cause a fault, such as physical damage, aging, electrical stress etc. Faults in dc systems can be categorized into two major types [5]:

- Line-to-Ground fault;
- Line-to-Line fault.

The line-to-ground fault is most common fault type occurring in dc systems [5],[12],[13]. The following Section 2.1 discusses the stages of the fault and the system response under fault conditions initially for a VSC, and then for a Modular Multi-level Converter (MMC).

## 2.1 Line-to-Ground Fault

The grounding scheme of the dc system determines the loop that will be formed between the fault and the rest of the system. In case of mono-polar HVdc links, the grounding can be achieved through the ground or using a metallic return. For this analysis a positive line-to-ground fault has been considered. The change observed for a negative line-to-ground fault is the direction of current. Figure 2.1, shows a positive line-to-ground fault. Although the IGBTs are blocked under a fault, the converter acts as an uncontrolled rectifier and the anti-parallel diodes continue to freewheel the fault current. For analysis the dc cable up to the fault point is modelled as a single pi-section. The cable resistance up to the fault point is given as $\frac{R_c}{2}$ and inductance $\frac{L_c}{2}$. The equivalent capacitance $C$ has been assumed to be the capacitance equivalent of the cable pi-section.

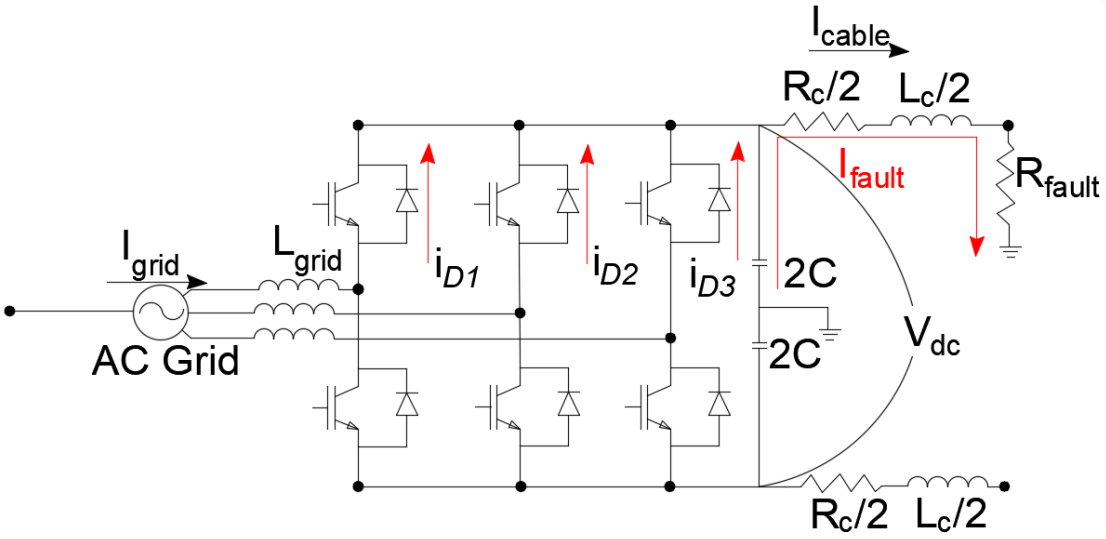



Figure 2.1: Line-to-ground fault

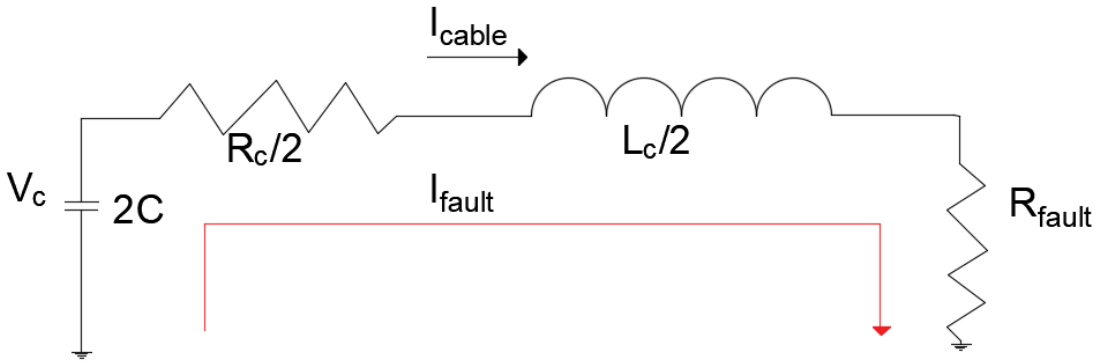



Figure 2.2: Equivalent circuit representing capacitor discharge phase

A fault on the dc side is a superposition of two responses in the system, the natural response and the forced response. The response of the stages are summarized below.

1. *Natural Response (Capacitor Discharge):* The faulted ground forms a loop with the mid-point grounding of the dc link. During this stage the capacitor voltage is discharged into the fault. The system can be represented as a *RLC* equivalent circuit as shown in Figure 2.2. The fault resistance plays a vital role in the damping of the fault current. Applying Kirchhoff's Voltage Law (KVL) to the *RLC* circuit, the response is given by (2.1);

$$\frac{\mathrm{d}^2 v_c}{\mathrm{d}t^2} + 2\alpha \frac{\mathrm{d}v_c}{\mathrm{d}t} + \omega_0^2 v_c = 0 \tag{2.1}$$

where $\alpha = \frac{R}{2L}$ and $\omega_0 = \sqrt{\frac{1}{2L_c C}}$. The equivalent resistance of the circuit becomes $R = \frac{R_c}{2} + R_{fault}$, $\alpha = \frac{R_c + R_{fault}}{2L_c}$ and $\omega_0 = \sqrt{\frac{1}{2L_c C}}$. The solution of the second order differential equation (2.1), under the condition $R_{fault} + \frac{R_c}{2}\sqrt{\frac{C}{L_c}} > 1$ is given as (2.2), with initial conditions as $V_c(t_0) = V_0$ and $I_{cable}(t_0) = I_0$;

$$V_c(t) = e^{-\alpha t}(B_1 cos\omega_d t + B_2 sin\omega_d t) \tag{2.2}$$

And the cable current is given by (2.3);

$$I_{cable}(t) = 2C\alpha\omega_d e^{-\alpha t}(B_1 sin\omega_d t - B_2 cos\omega_d t) \tag{2.3}$$

where, $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$, $B_1 = V_0$ and $B_2 = -\frac{I_0}{2C\alpha\omega_d}$ at $t = 0$.

2. *Forced Response (Grid Side Current Feeding):* As the capacitor voltage drops below the dc side voltage, the IGBT's are blocked by their internal over-current protection. A significant over current is produced as the anti-parallel diodes begin to free-wheel. The VSC has the potential to be severely damaged under such a condition.

   It is difficult to have an analytical expression for this stage due to the non-linear response of the system. State space equations are used to describe this phase, is given by (2.4);

$$\begin{pmatrix} \frac{\mathrm{d}v_c}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{cable}}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{lim}}{\mathrm{d}t} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{2C} & \frac{1}{2C} \\ \frac{1}{L_c} & -\frac{R_c + R_{fault}}{L_c} & 0 \\ -\frac{1}{L_{grid}} & 0 & 0 \end{pmatrix} \begin{pmatrix} v_c \\ i_{cable} \\ i_c \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ \frac{1}{L_{grid}} \end{pmatrix} v_{G_{a,b,c}} \tag{2.4}$$

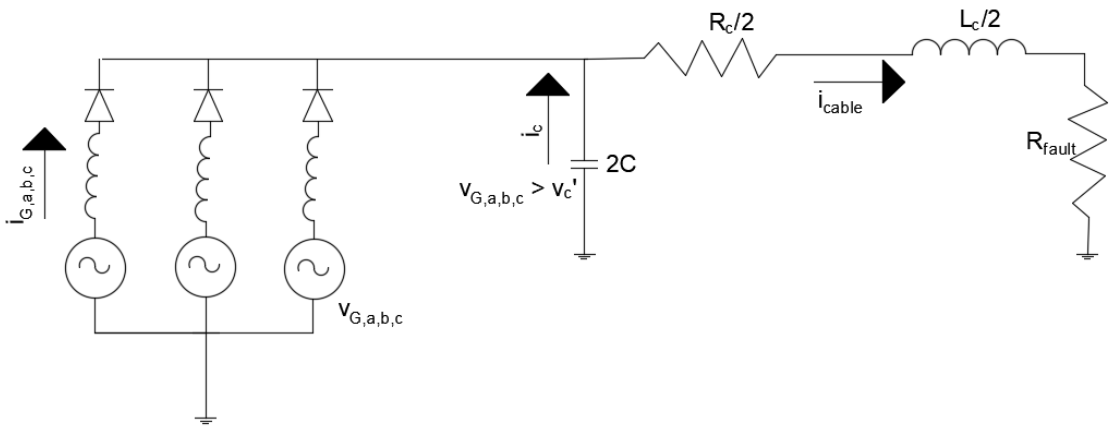



Figure 2.3: Grid side current feeding stage

Figure 2.6, shows the grid side current feeding stage.

3. *Steady State Response:* The steady state response of the equivalent circuit involves the grid continuously feeding the fault, the equivalent impedance can be calculated as (2.5);

$$Z = (R_f + R_c + j_c)||(1/j\omega_s C) + j\omega_s L_{grid} = Z\angle\theta \tag{2.5}$$

where $\omega_s$ is the angular frequency (synchronous) and $L_{grid}$ is the grid side reactance.

The current flowing through the diodes under this condition is given as (2.6);

$$i_{D_1} = i_{ga,(>0)} = \frac{V_g\angle\zeta}{|Z|\angle\theta} = \frac{V_g}{|Z|}\angle\zeta - \theta \tag{2.6}$$

As the diodes are in freewheeling stage the cable current is equivalent to the fault current given by (2.7);

$$i_{fault} = i_{cable} = i_{D1} + i_{D2} + i_{D3} \tag{2.7}$$

where, $i_{D1}, i_{D2}, i_{D3}$ are the diode currents of each converter arm.

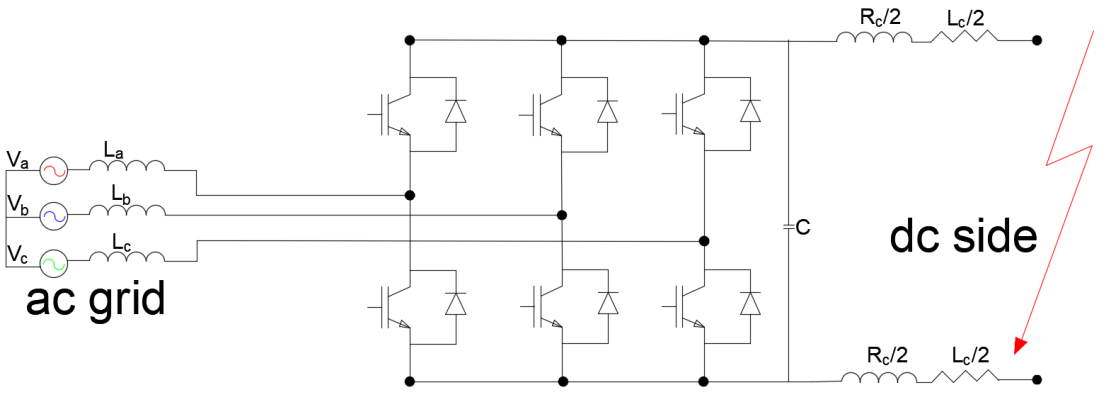



Figure 2.4: Equivalent VSC network under line-to-line fault

## 2.2 Line-to-Line Fault

This type of fault is a rare phenomenon. When the positive and negative poles are in contact with each other a line-to-line fault occurs. Although, the IGBT's are blocked but the anti-parallel diodes continue to circulate the fault current, leaving the VSC exposed to over-current. This type of fault is also characterized by a natural response and a forced response. The natural response is further subdivided into two phases. The response of the stages are summarized below:

1. *Natural Response (Capacitor Discharge):* Similar to the capacitor discharge phase for a line-to-line fault the can be represented as a $RLC$ circuit. The expressions for the cable current and the dc voltage is represented by solving the second order $RLC$ circuit shown in Figure 2.4. Applying KVL to the equivalent circuit it can be represented as (2.8),

$$V_c + R_c C\frac{\mathrm{d}V_c}{\mathrm{d}t} + L_c C\frac{\mathrm{d}^2 V_c}{\mathrm{d}t^2} = 0 \tag{2.8}$$

As the dc link capacitor discharges a second-order natural damping oscillation is observed. The dc link voltage and cable current can be derived similarly to (2.2) and (2.3) respectively.

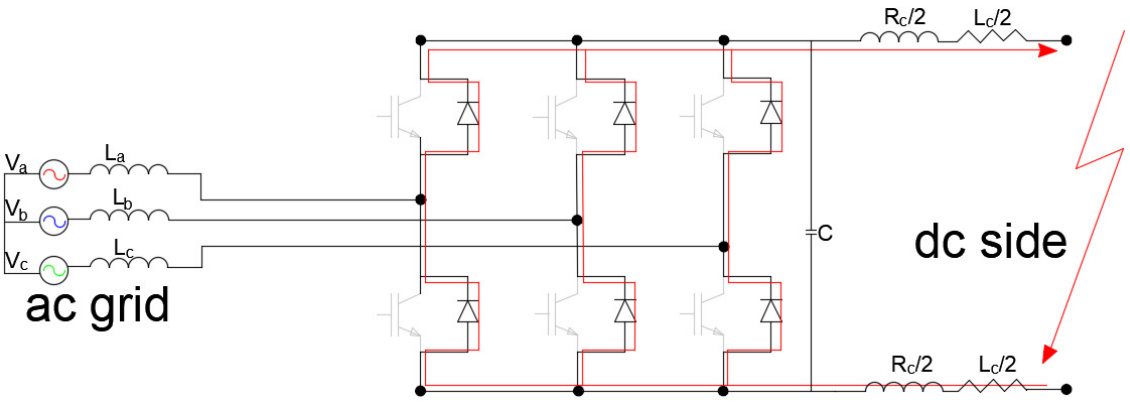



Figure 2.5: Diode freewheeling stage for VSC line-to-line fault

Assuming the fault happens at time $t_0$, the time taken for the capacitor voltage to drop to zero is given as (2.9);

$$t_1 = t_0 + \left(\frac{\pi - \delta}{\omega_0}\right) \tag{2.9}$$

where, $\delta = arctan\left(\frac{(V_0\omega_0 C sin\beta}{V_0\omega_0 C cos\beta - I_0}\right)$. This stage is followed by the diode freewheeling stage.

2. *Natural Response (Diode Freewheeling Stage):* The cable current $I_{cable}$ is transferred to the free wheeling diodes of the VSC, after the voltage of the dc link drops to zero. The anti-parallel diodes discharges the cable inductance into the fault through this path. The cable current is given as (2.13);

$$i_{cable} = I_1 e^{\frac{R_c}{L_c}t} \tag{2.10}$$

The current carried by each diode is equivalent to one-third of the cable current $i_{Di} = i_{cable}/3$, where $i = 1, 2, .., 6$. The VSC is at its worst under this phase with a potential damage. The diode freewheeling stage is schematically represented in Figure 2.5.

3. *Forced Response (Grid Current Feeding Stage):* The last stage of the current

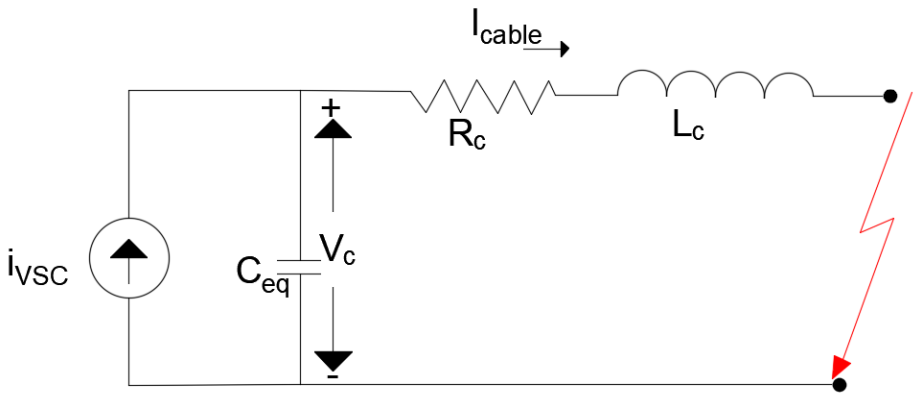



Figure 2.6: Grid side current feeding stage for VSC line-to-line fault

discharge after the converter IGBTs are blocked. The grid behaves as a current source and feeds the fault current. The equivalent circuit under this response is shown in Figure 2.6. Assuming the fault in the dc cable happens at the zero crossing of phase $a$ voltage, the grid voltage per phase is given as (2.11);

$$v_{ga} = V_{grid} sin(\omega_g t + \theta_g) \tag{2.11}$$

where $V_{grid}$ is the phase voltage amplitude, $\theta_g$ is the phase angle and $\omega_g$ is the synchronous angular frequency.

The corresponding grid current amplitude and phase is given as (2.12);

$$i_{ga} = I_g[sin(\omega_g t + \theta_{g0} - \delta) - sin(\theta_{g0} - \delta)e^{-\frac{t}{\tau}}] + I_{a1}e^{-\frac{t}{\tau}} \tag{2.12}$$

where $\delta = tan^{-1}(\omega_g \tau)$, $\tau = \frac{L_c + L_{grid}}{R_c}$, $I_{a1} = i_{ga}(t)$.

The current from the converter under this condition is similar to the positive half-cycle of the grid current as (2.13);

$$I_{dc} = i_{D1}(i_{ga} > 0) + i_{D2}(i_{gb} > 0) + i_{D3}(i_{gc} > 0) \tag{2.13}$$

For simplification, only analysis of phase $a$ response has been analyzed. The responses for phase $b$ and $c$ are super imposed later on. As stated earlier, the worst condition is analyzed when the voltage angle is zero during the initiation of the fault. The cable current and the dc bus voltage is expressed as (2.14) and (2.15) respectively;

$$i_{cable} = Asin(\omega_g t + \gamma) + Be^{-\frac{t}{\tau}} + [C\omega_0 e^{-\delta t} sin(\omega_d + \beta)]/\omega_d + [De^{-\delta t} sin\omega_d t]/\omega_d \tag{2.14}$$

$$v_c = R_c i_{cable} + L_c \frac{\mathrm{d}i_{cable}}{\mathrm{d}t} \tag{2.15}$$

where,

$$A = I_{grid}\left[(1-\omega_s L_c C)^2 + (R_c C\omega_s)^2\right]^{-1/2}$$

$$\gamma = \alpha - \varepsilon - \theta$$

$$\theta = tan^{-1}\left[\frac{R_c C\omega_s}{1-\omega_s^2 L_c C}\right]$$

$$B = I_{gn}\left[\tau^2/\left(\tau^2 - R_c C\tau + L_c C\right)\right]$$

$$C = -\left(Asin\gamma + B\right)$$

$$D = B/\left(\tau - \omega_s Acos\gamma\right)$$

The analysis performed was for a two-level VSC, a similar analysis has been performed for the MMC in the following section.

## 2.3 MMC Fault Analysis

As described previously the dc bus capacitor for a two level VSC is replaced by sub-module (SM) capacitors. Thus, the capacitor discharge stages as discussed previously are avoided. The IGBTâs are blocked due to over current but the anti-parallel

continue to feed the fault current, this action is similar to a two level VSC. As stated earlier the absence of a large dc capacitor bus helps to avoid the capacitor discharge phase. But the ac grid contributes to the fault current. In this section the contribution of the ac sources to the fault current has been analyzed.

The upper-arm and lower-arm currents for a MMC under normal operating conditions for phase $j$ are given as (2.16);

$$\begin{aligned} i_{p,j} &= i_{cir,j} + \tfrac{i_j}{2} \\ i_{n,j} &= i_{cir,j} - \tfrac{i_j}{2} \end{aligned} \tag{2.16}$$

$i_{cir,j}$ is the circulating current for phase-$j$ and $i_j$ is the phase-$j$ ac side current. The circulating current, is given as (2.17);

$$i_{cir,j} = \frac{i_{p,j} + i_{n,j}}{2} \tag{2.17}$$

From the per-phase diagram of the MMC shown in Figure 2.7, the dc side voltages can be given as (2.18);

$$\begin{aligned} \tfrac{V_{dc}}{2} - v_{p,j} &= L_c \tfrac{\mathrm{d}i_{p,j}}{\mathrm{d}t} + R_c i_{p,j} + v_j + v_{cm} \\ \tfrac{V_{dc}}{2} - v_{n,j} &= L_c \tfrac{\mathrm{d}i_{n,j}}{\mathrm{d}t} + R_c i_{n,j} - v_j - v_{cm} \end{aligned} \tag{2.18}$$

where $v_j$ and $v_{cm}$ are described as the fundamental and common mode voltages of the MMC for phase-$j$, $v_{p,j}$ and $v_{n,j}$ are the upper and lower arm voltages of the MMC for phase-$j$ respectively. The equivalent per phase circuit diagram for a MMC is shown in Figure 2.9. Solving (2.18) the phase current can be expressed as (2.19);

$$L_c \frac{\mathrm{d}i_{p,j}}{\mathrm{d}t} + \frac{R_c}{2} i_j = \frac{v_{n,j} - v_{p,j}}{2} - v_j - v_{cm} \tag{2.19}$$

1. *Phase I:* Assuming the fault occurs at time $t_0$ and the SMs are blocked under over current or under voltage at time $t_1$, the MMC is operational and the SM

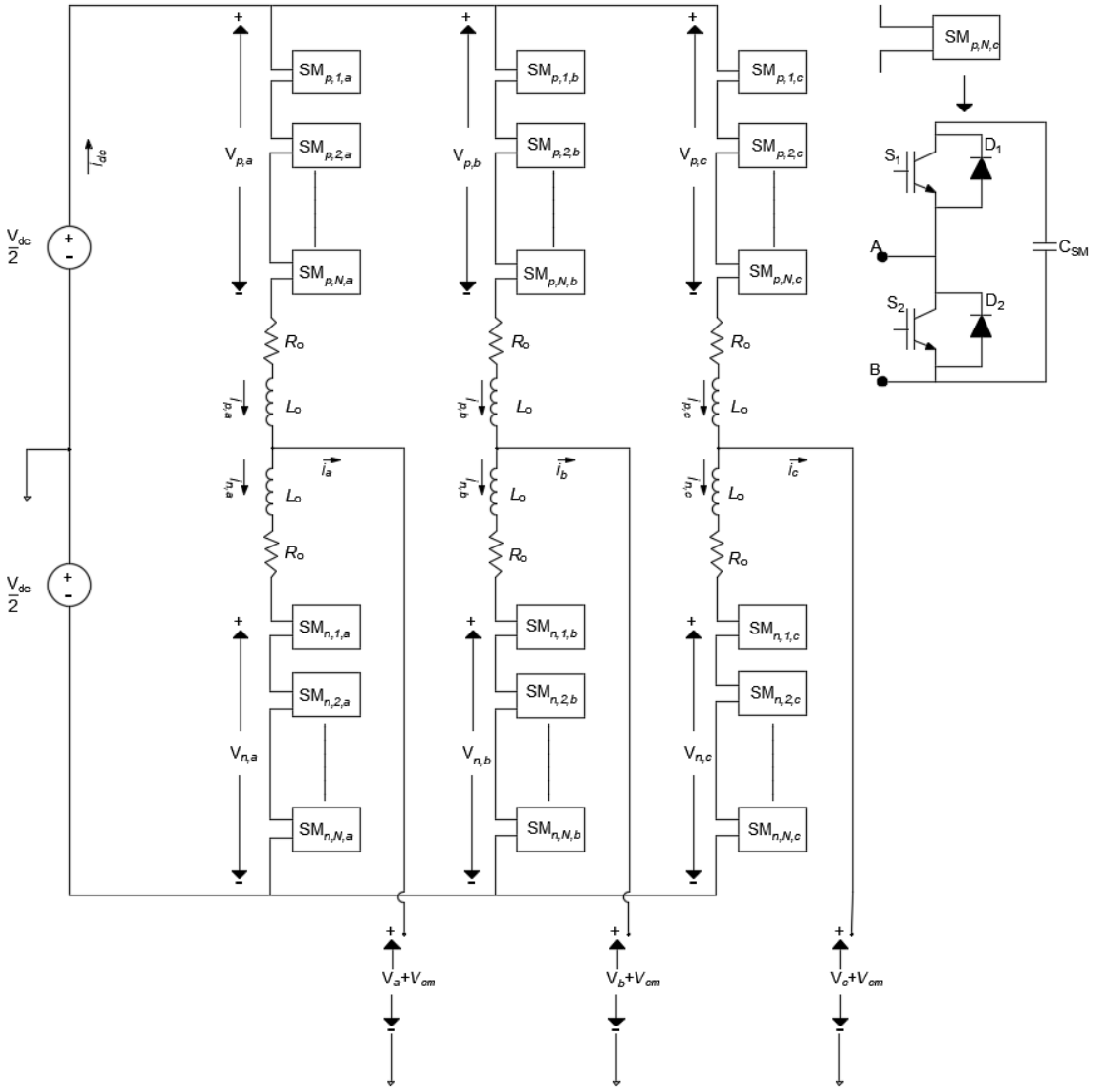



Figure 2.7: Detailed schematic of MMC with HBSM

capacitors discharge into the fault. The equivalent stage response is shown in Figure 2.8(a). The arm currents during those stages are given as (2.20);

$$\begin{aligned} i_{p,j} &= \frac{i_j}{2} + \frac{I_{dc}}{3} + \frac{V_{dc}}{2L_c} \\ i_{n,j} &= -\frac{i_j}{2} + \frac{I_{dc}}{3} + \frac{V_{dc}}{2L_c} \end{aligned} \tag{2.20}$$

2. *Phase II:* After time $t_1$ the SM IGBTs are blocked either by over current protection or under voltage protection. The fault current begins to freewheel through the anti-parallel diodes. The dc link voltage can be approximated as (2.21);

$$V_{dc} = V_{dc_0} e^{-\delta t} sin(\omega_0 t + \beta) \tag{2.21}$$

where $V_{dc_0}$ is the initial dc voltage and $\beta = \frac{R_c}{2L_c}$. The schematic representation is shown in Figure 2.8(b).

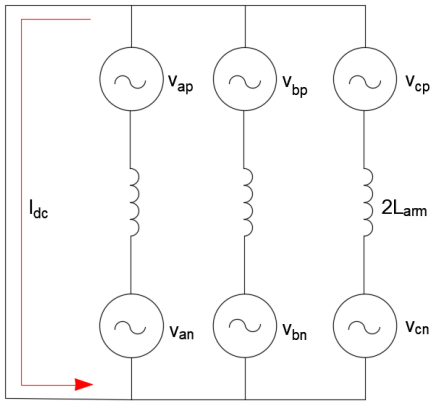
3. *Phase III:* The final phase is when the grid begins to feed the fault similar to the one observed in Section 2.2. Assuming the breakers interrupt the fault current with this period. The fault current begins to decay through the line inductance as an under damped $RLC$ circuit with no driving voltage source. The current decay is given as (2.22);

$$i_{cable} = I^*_{dc} e^{-\alpha t} \tag{2.22}$$

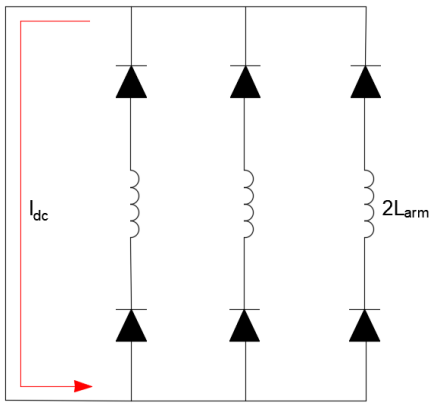
where $\alpha = \sqrt{\omega_0^2 - \omega_d^2}$ is the attenuation constant and $\omega_d$ is the frequency at of current decays and $\omega_0$ is the natural frequency of oscillation. The schematic of this phase is shown in Figure 2.8(c).

## 2.4 Analysis

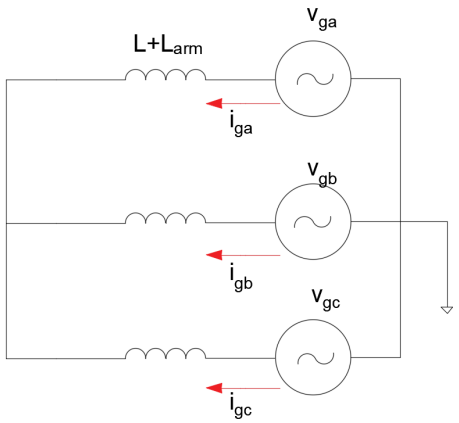
In the above Section 2.3 a detailed analysis of the fault stages for a VSC (two-level and MMC) have been performed, and it can be seen that conventional VSCs are




(a) Phase I




(b) Phase II




(c) Phase III

Figure 2.8: Half-bridge MMC equivalent fault response stages, (a) Phase I before IGBT is blocked, (b) Phase II diode freewheeling stage, and (c) Phase III grid current feeding stage

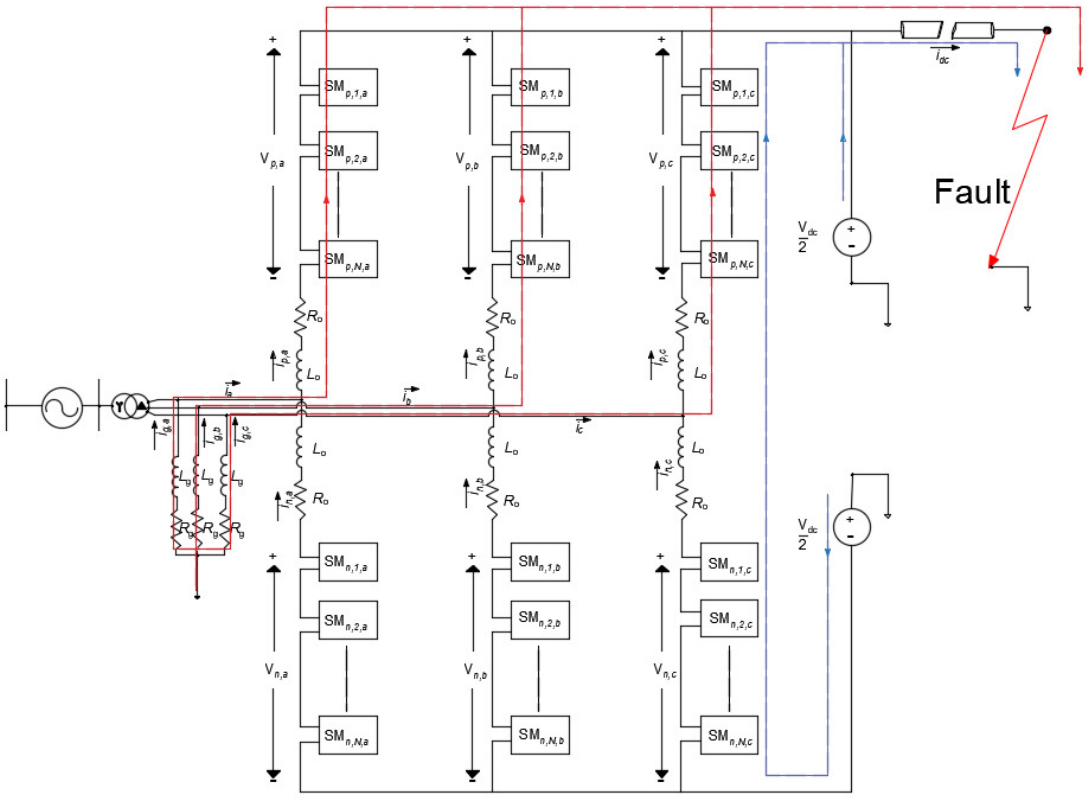



Figure 2.9: MMC fault equivalent circuit

incapable of controlling dc side fault currents due to their inherent design. VSCs are essential is the development of MTdc networks as they offer the flexibility of power flow in either direction. The rate of rise of dc fault currents are also higher due to the lack of reactance of dc cables unlike ac systems. The ac breakers are slow to react and are thus incapable of controlling the fault currents. Specially designed hybrid dcCBs as discussed in Section 1.1 are required to be installed to protect the VSC from any over current conditions to prevent potential damage. Protection methodologies needs to be designed to operate the breakers keeping in mind the following essential parameters:

1. Speed: detect and isolate the fault before any potential damage to the converter stations;

2. Robustness: avoid false triggering of the breakers and able to detect fault under varying conditions i.e. location of the fault, measurement noise etc;

3. Selectivity: detect and isolate only the faulted section of the cable;

4. Operation: the non-faulted section does not get affected by the breaker operations.

The following Chapters discuss various methods that have been implemented for fast and efficient fault detection under various circumstances.

# CHAPTER 3: WAVELET BASED FAULT DETECTION

## 3.1 Overview

The development of MTdc networks are impeded by the vulnerabilities of VSC networks to dc faults [14]. Since it is desired that under fault conditions the converters connected to the healthy sections of the network remains operation [15]. Such actions motivate the need for fast and accurate fault detection techniques and isolate the dc fault using specially designed dc breakers. Challenges in such fault identification involves (1) detection of the faulty section of the network; (2) avoiding false fault detection due to non-fault high frequency transients.

Multiple approaches has been investigated in the past involving fault detections using over-current or under-voltage thresholds [16]. Such approaches suffer from sensitivity to high frequency fault transients leading to approaches for incorrect fault detections. Hence, it is clear the more reliable fault detection methods must discover fault events over small time intervals, rather than an instantaneous current or voltage value. Work in [17], discusses the need for fast decision making, i.e. detection on the order of milliseconds, to safeguard high power HVdc transmission systems from commutation failures due to faults. It is, therefore, essential to have a feature to distinguish between a fault transient and a non-fault transient.

The fault transients are highly informative since they provide the idea of time, location, and type of the fault, in addition to other less important attributes. It is essential to analyze and extract data from the fault signals for fast protection mechanism. Wavelet analysis is able to analyze and synthesize information with the help of fast processing digital signal processing (DSP) tools, useful in analysis of transient signals [18]. Voltage drop in the dc cables do not exist due to the absence

of inductive reactance; thus, the propagation of dc fault in the grid is also faster. During faults, one of the causes for system failure is the extreme rate of current rise. The motivation for this part of the research is to develop a fast and reliable fault detection mechanism for MTdc systems.

Faults in a dc system occur more frequently on the cables compared to other parts of the system. The most common cause is the failure of insulation and breakdown due to electrical and environmental stress. For VSC systems, the converter is defenseless against dc faults, such as a dc-link short-circuit, dc cable short-circuit, and dc cable ground faults. Previous work performed in [19] focuses on the study of faults on the dc rails. A dc-cable short-circuit fault is more common compared to a fault in the dc rails [12]. The potential impact of the dc cable fault on the VSC system is much more significant as compared to a dc rail fault. Although, the chances of a short circuit fault for underground cables is negligible in comparison to overhead lines, it is critical that the system protection be designed considering the worst case scenarios.

Fault detection at remote off-shore locations is challenging due to conflicting requirements to be both fast and reliable. Generally, speed of detection increases considering the signal over smaller time intervals. Conversely, reliability increases considering the signal over larger time intervals. Good fault detection requires the designer to strike a compromise between these conflicting requirements. Under fault conditions, the voltage of the fault point can abruptly reduce to a low value. Such abrupt voltage changes give rise to electromagnetic waves in the form of traveling waves, travelling throughout the network.

The traveling wave theory as a method to model faults on transmission networks has been studied since the 1950's. With the development of signal processing tools contemporary signal processing system can apply these models to implement wave-based fault protection. The duration of the fault transients can vary from a few microseconds to seconds; thus, it is necessary to capture the information using high

speed data acquisition devices. The wavelet transform provides a unique feature for extracting components of traveling waves generated by the fault transients [20]. They also are able to provide a feature that allows a clear distinction between fault and non-fault transients.

### 3.1.1 Related Work

One major challenge in multi-terminal dc network design is their vulnerability to faults. Various techniques for fault detection in HVdc grids have been discussed. Some leading methods from the literature includes ROCOV [21], reactor voltage change rate [22], inverse time over current protection [23], Short Time Fourier Transform (STFT) [24], wavelets [25], rate of change in line impedance [26] , traveling waves [27], Prony analysis [28], machine learning [29], etc.

The dc voltage derivative method introduced in [21] emphasizes the quick isolation from dc faults, but neglects the influence of the arm reactor. In [22], the rate of change of voltage is independent of power flow directions and fault resistance variation, but it is still dependent on the network parameters. A continuous monitoring of voltage thresholds is required, governed by a fault detection time $\Delta t$, whereas the arm inductance also has an important role in the detection time. The application of STFT in [24], demonstrates the use of fixed duration of time intervals for frequency resolution, that is not effective for non-periodic and fast transient responses i.e. faults. In [26], a protection scheme has been designed using thresholds for $dU/dt$ with variations in fault impedances. Studies in [28] have been performed for only 20 kV medium voltage networks, whereas in [29] the decision making depends on the training and available dataset. The algorithm has to be retrained when the operating conditions are changed and a new dataset is available, that requires significant time and effort and is computationally intensive. The methods discussed in [21] - [28], make it difficult to quickly identify the faulted cable and sometimes lead to false triggering of the dc breakers.

The Hilbert-Huang Transform (HHT) [30], [31] has several important analytical benefits it shares with the wavelet transform; most importantly a time-frequency decomposition of the signal. As such, it is possible to apply this transformation for fault detection. One potential shortcoming of this approach is the decision of appropriate parameters to reliably extract a basis and associated collection of transform coefficients that sufficiently isolate the fault phenomenon. This helps to localize characteristically large energy in frequencies around the fault frequency not otherwise observed under non-fault conditions. As such, it is unclear if distinct realizations of grid faults can be detected via a single, i.e., time-invariant, threshold on the associated HHT coefficients. Specifically, it is unclear if manifestations of some faults lead to HHT intrinsic mode functions that do not properly separate energies in the vicinity of the fault frequency from other potentially noisy frequency bands. If this can occur then detection for these fault manifestations may be problematic using a time-invariant, i.e. constant threshold. While the application of the HHT for fault detection remains an open research topic, the proposed work explores a time-invariant method to detect faults using the fixed basis of the wavelet transform.

The choice of the wavelet transform is justified over other transforms due to its unique compromise between time-and-frequency localization and simultaneous freedom for the choice of basis functions [32]. Other options provide either good frequency resolution, e.g., Fourier transform [33], or provide time-and-frequency resolution, e.g., STFT [24], but do not also afford free choice of the basis functions.

Wavelet transform has been used in power systems for data compression, transient analysis, signal analysis, and de-noising. Wavelet analysis has been proposed in literature [34], [35] and [36] as a tool for identification of transients for fault detection and localization. The fault detection approach leverages the wavelet transform to quickly generate a representation of the current signal that captures both its local and semi-global time-and-frequency properties as a compact collection of numbers re-

ferred to as wavelet coefficients [29]. The proposed method aims at looking into more specific wavelet coefficients, the fault signals are more variable and may manifest in the wavelet transform such that these specific coefficients are not excited. It looks at a much broader range of specific sets of frequencies in the wavelet domain, and thus tried to overcome the shortcomings of the previous methods.

## 3.2 Contribution

Lack of fault detection techniques is a major impediment to creation of fault-tolerant MTdc networks and limits widespread adoption of MTdc networks. Specially designed dc breakers operate within 3-5ms; after a proper fault detection. Previously, suggested methods utilizing time-frequency analysis fails to do a good job in identifying a good time-frequency resolution for the signal. Other previously discussed methods are dependent on the system parameters. Thus, a reliable and fast detection underlies all the major operation a hybrid dcCB.

This Chapter proposes a framework and case-example for fault detection based on features derived from the wavelet transform of the grid current. The algorithm is intended to control new high-speed dc breakers to improved fault resilience, e.g., an assembly HVdc breaker. In this Chapter, the measurements are taken locally at each of the converter stations and they are operated independently to avoid any failure. During fault the energy storage components across the network fail to release the stored energy abruptly, and electric and magnetic fields build around the conductor giving rise to high frequency electromagnetic waves that traverse the grid called traveling waves. The incident waves traveling almost at the speed of light reach the sensors located closest to the point of the fault. The arrival of the first peak can be captured using a wavelet transform. Wavelet transforms help us to tailor detection to specific frequency band for faults in the MTdc network. Using Multi-Resolution Analysis (MRA) technique, it helps us in extracting the target fault frequencies in the faulted cable that gets attenuated at the other locations on the network. There is

a change in the energy due to the onset of faults at every decomposition level. This information, extracted from the traveling waves, is utilized in the fault detection. To evaluate the performance of the proposed algorithm a three terminal VSC MTdc was designed using Power Systems Computer Aided Design (PSCAD)/Electromagnetic Transients including dc (EMTDC). The results verify the effectiveness of the algorithm.

## 3.3 HVdc Breakers

Traditional ac breakers are not suitable for the purpose of fault isolation in HVdc circuits due to its slow speed and nature of operation. Active and passive resonant dc breakers have been proposed as alternative solutions. This approach employs a fast mechanical switch in series with semi-conductor switches. The typical fault clearing time is around 60-100ms for a 5kA fault current [11]. Other, faster options include the use of semiconductor switches for current interruption, but the high conduction losses during normal operations result in unacceptable reductions in system efficiency.

Hybrid dc breakers for HVdc applications, as proposed in [9] offer an alternative solution. This approach employs semiconductor switches for current interruption. The hybrid design enables the breaker to have minimum conduction losses during normal operations and higher current interruption specifications. These breakers must be placed in front of each converter station to prevent complete shutdown of the MTdc grid during fault conditions. The main breaker unit employs multiple redundant semiconductor modules, that increases the cost of the device.

This shortcoming can be overcome with the design proposed in [37]. The assembly HVdc breaker, by design, is efficient in removing faults from the system within a specific period of 2-5ms. This design reduces the number of main breakers required [7].

This sub-section discusses recent evolution's of dc breaker design with a focus on the Assembly HVdc circuit breaker, physical mechanisms involved in dc faults, and

the related articles from the literature describing their HVdc breaker operation for fault isolation.

### 3.3.1 Assembly HVdc Circuit Breaker

To overcome this concern, a different design for dc breaker has been proposed in [37]. The assembly HVdc breaker uses a traditional dc-fault detection strategy [37] that thresholds the current to detect faults in the system.

1. Components : The following sections describe the four functional components of an Assembly HVdc circuit breaker:

   **ASCB:** The design and functionality of an Active Short Circuit Breaker (ASCB) is similar to the main breaker unit of a hybrid dc breaker. The design for the ASCB shown in this Chapter has been modified slightly from [37] for implementing it on a symmetric monopole MTdc system, as shown in Figure 3.1(a). The ASCB is designed to withstand a large $di/dt$ change during a fault. It serves as the major current interruption unit. For safety measures, it has back up IGBT switches are installed, so that if some of the units fail to operate, the other back up devices can share the fault current, thereby preventing a complete device failure. The ASCB remains open under normal operating conditions, but closes immediately during the time of fault, thus creating a new short-circuit point. The fault current is shunted by the closing of the ASCB allowing the main breaker to operate at low current conditions.

   **Main Breaker:** The main breaker unit has some features similar to that of the ASCB, but with much lower number of IGBT modules. The voltage rating for this device is very low as compared to the ASCB as it does not interrupt the fault current. This is a bidirectional device to facilitate operation in either direction. As this is designed to withstand low voltages, it has a much lower rating and has very low conduction losses. It remains operational under normal

operating conditions.

**UFD switch:** This is a mechanical switch designed to be opened at zero current. It acts as a mechanical isolator for the circuit and protects the main breaker from over-voltage. The mechanical breaker opens after the main breaker has isolated the faulted cable from the grid at zero current conditions.

**ADS:** The accessory dis-charge switch consists of semiconductor thyristor switches with a resistor connected in series. The ADS closes along with the ASCB once a fault has been detected, creating another short-circuit point on the other end of the main breaker. The main function of the ADS is to reduce the voltage across the main breaker before it opens. Durability is an issue with ADS devices as it needs to withstand high breaking current. The design of an ADS is illustrated in Figure 3.1(b).

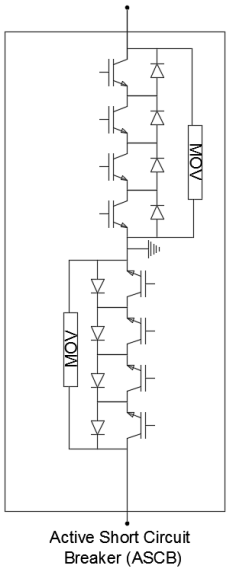
2. Working Principle: The isolation mechanism is a step-wise process as explained below:

   *Step 1:* The ASCB and ADS are turned on immediately after the fault is detected, creating a short circuit on either ends of the main breaker. This action lowers the cable current to almost zero allowing the main breaker to operate under operating voltage conditions.

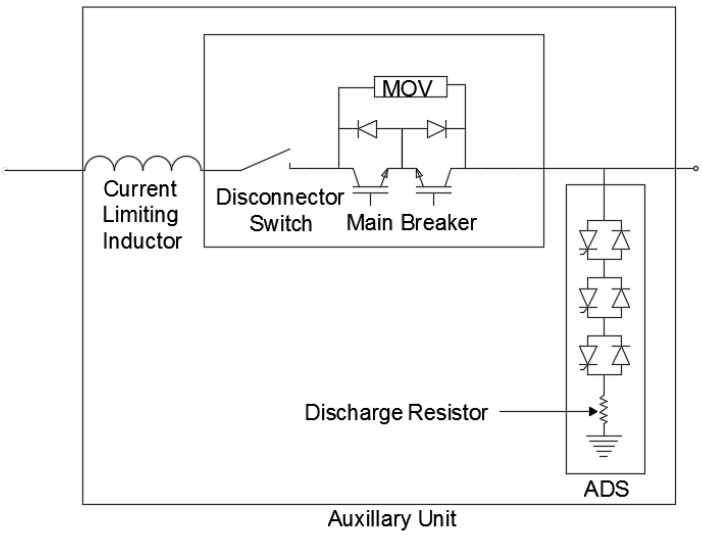
   *Step 2:* The main breaker is turned off, and the mechanical disconnect switch is operated at zero current, thus isolating the faulted cable from the network.

   *Step 3:* Finally, the ASCB is turned off, restoring the dc bus voltage. The current through the ADS commutates to zero, the commutation time being dependent on the discharge resistor connected to it.

A summary of the operational characteristics of different dc breaker designs is shown in Table 3.1.




(a) ASCB




(b) Auxiliary Unit

Figure 3.1: Assembly HVdc breaker sections, (a) ASCB for symmetric monopole, (b) Auxiliary unit consisting of the disconnect switch, main breaker and the ADS

Table 3.1: Performance characteristics of dc breakers

| | **Solid State** | **Resonant** | **Hybrid dc Breaker** | **Assembly HVdc Breaker** |
|---|---|---|---|---|
| Commutation [ms] | switch: 0.1 | breaker:<20; resonance:≤30 | switch: 0.1; breaker: ≤ 20; UFD: 1-4 | main breaker: 0.2; UFD: 2-3; ASCB: 0.3 |
| Interruption time [ms] | <1 | <60 | 3-5 | 3-5 |
| Max. Voltage [kV] | 800 | 550 | 750 | 800 |
| Max. Current [kA] | ≤ 5 | 4 | 15 | 15-20 |
| Loss [%] | 30 -40 | ≤ 0.3 | negligible | negligible |

## 3.4 Spectral Analysis

For better understanding time domain analog signals, it is necessary to evaluate their spectral information in the frequency domain as well. Fourier Transform has been largely used for spectral representation of given signals. Fourier Transform fails to provide the time information for respective representative frequencies. Also, spectrum the time-interval needs to be relatively small for detecting high-frequency spectrum and large for detecting low-frequency spectrum [38].

The choice of window size and absence of time information for the spectral domain was solved using STFT by Gabor in 1946. A localized Fourier transform for a "specified window" size was performed on the signal where the signal was assumed to be stationary. The entire signal was broken into lengths of this small window sizes. The STFT was thus able to resolve a time-domain signal into a time-frequency representation. The major drawback associated with STFT was the constant window size. As stated earlier a small window provides a better high spectral resolution and large window provides a better low spectral resolution, as perceived by Heisenberg's Uncertainty principle [18]. STFT fails to provide a proper time-frequency analysis due to its fixed window size.

Wavelet Transform is a similar tool performing a time-frequency analysis for the given signal. It provides the flexibility to choose a basis function with adjustable time-frequency window. For high frequency observations the window size narrows to provide finer spectral resolution and similarly the window becomes wider for low frequency observations. A comparison of the time-frequency analysis is shown in Figure 3.2. The wavelet transform uses an adaptive window function to perform analysis of a non-stationary signal, whereas the time-frequency window for STFT remains constant.

Wavelet transform has found its application in power systems domain in power quality analysis, signal de-noising, fault detection, fault location, data acquisition etc.

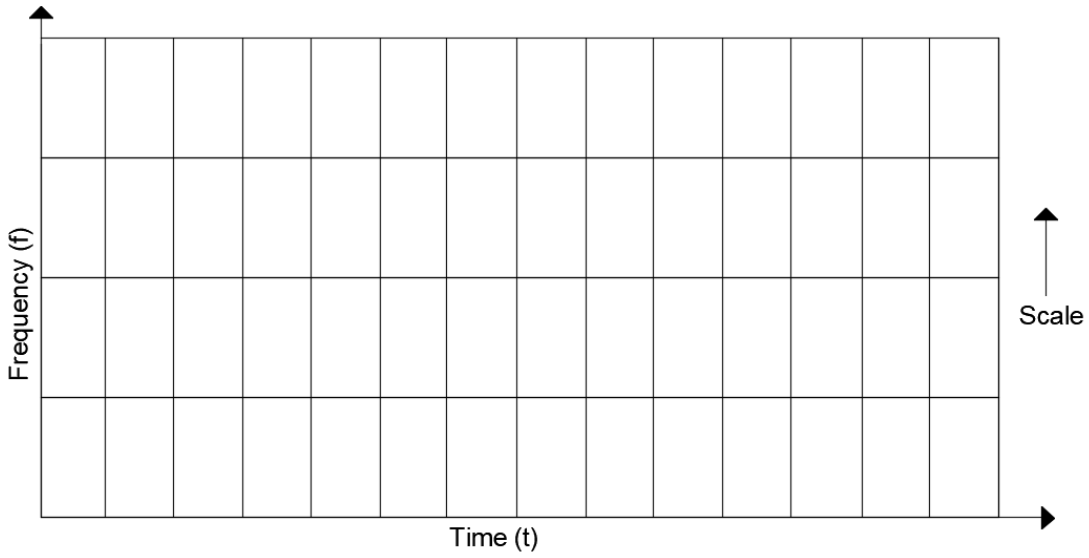
In the following sub-sections the continuous and discrete wavelet transforms and describe the use of this transform for fault detection have been introduced.

### 3.4.1 Continuous Wavelet Transform

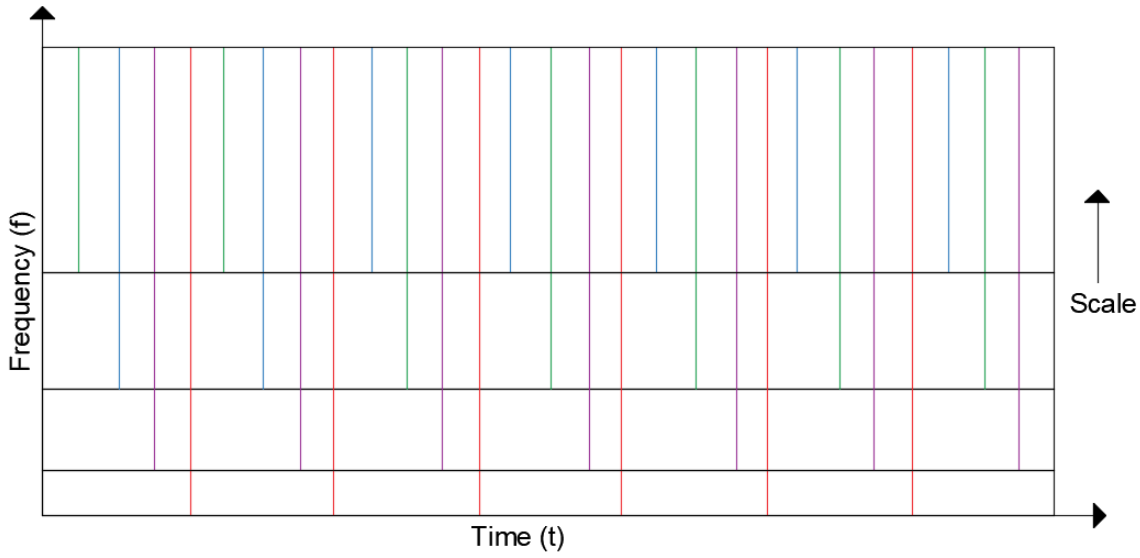
The continuous wavelet transform (CWT) consists of two parts, an analysis component that generates wavelet coefficients *WT(a, b)* from an input function *x(t)* and an synthesis components that reconstructs *x(t)* from a collection of wavelet coefficients. Generated wavelet coefficients depend on the specific form of a "mother wavelet" basis function, $\psi(t)$, and lie a 2-dimensional space *(a, b)*. The continuous wavelet transform of *x(t)* is given in (3.1) [8];

$$WT(a,b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} \phi(t)\psi^*(\frac{t-b}{a})dt \tag{3.1}$$

Where $*$ denotes complex conjugation and the parameter $a$ is referred to as the scale parameter. Typically $a < 1$ and when this occurs the domain of the function $\psi(t)$ expands on the $t$-axis by a factor of $a$. The parameter $b$ shifts the basis function in time, cross-correlating the wavelet basis function with *x(t)*. Typically the wavelet




(a) Short Time Fourier Transform




(b) Wavelet Transform

Figure 3.2: Time frequency analysis

transform is computed as a dyadic decomposition, i.e. power-of-two, sequence. Under these conditions the scale parameter is $a = 2^{-j}$ where $j$ = *1,2,....,J* and the shift parameter $b$ is chosen to be $b = ka = k2^{-j}$. Let's assume that a scale 1 is performed, wavelet transform for a real-valued wavelet, i.e. $\psi(t) = \psi^*(t)$. Then (3.1) takes the form shown in (3.2). By allowing the dyadic scale, $a = 2^{-j}$ to vary, wavelet transform coefficients at distinct scales are generated as given in (3.2);

$$WT(j,k) = \sqrt{2^j} \int_{-\infty}^{\infty} x(t)\psi(2^j t - k)dt \tag{3.2}$$

In implementation, the continuous wavelet transform may be computed by scaling, i.e. dilating, $\psi(t)$ by a factor of $2^j$ and then cross-correlating the resulting signal with the input signal $x(t)$.

### 3.4.2 Discrete Wavelet Transform

Similar to other transforms, the discrete wavelet transform (DWT) is derived by sampling the continuous wavelet transform. For this application, the standard form of the wavelet transform as given by the dyadic decomposition discussed in Section 3.4.1 are of focus. Here, by time-reversing the dilated mother wavelet and compute convolution rather than cross-correlation and rather than dilating the function in continuous time by sub-sampling the input signal by $2^j$ that effectively extends the domain of $\psi(t)$ by $2^j$ as shown in (3.2). The result of these two transformations using (3.2) generates two discrete instances of the mother wavelet referred to as filters, i.e. a low-pass filter *h[n]* and a high-pass filter *g[n]*.

Implementations of the DWT cross-correlate the input signal with these filters and subsequently down-sampling the outputs by two to generate two collections of coefficients. Wavelet coefficients produced are collected into two groups: (1) a collection of approximation coefficients, $A[k] = h[-n] * x[n]$, including the low frequency information of the input signal, and detail coefficients, $D[k] = g[-n] * x[n]$, including the

high frequency information of the input signal. As such low-frequencies and high-frequencies are localized to the sets *A[k]* and *D[k]* respectively and the index of each coefficient localizes the time at that frequency occurs to a specific time interval in the input signal.

The critical free parameter of the discrete wavelet transform, is the specific form of the wavelet basis functions *(h[n],g[n])*. Many options for the basis exist and the general practice is to choose a basis that most compactly characterizes typical realizations of the signal for analysis $x[n]$. For current signals, work in [25] explored a number of options and suggests the Daubechies *'db3'* wavelet as the "best fit" wavelet for fault events for a specific sampling frequency of 15kHz. The wavelet selection was facilitated using Pearson's product coefficient. Fault detection is the mode of detecting abrupt and rapid changes lasting for a short time duration, the compactness of the mother wavelet coefficient plays an important role [39], [40]. As such, this Chapter adopts the wavelet basis provided by the *'db4'* wavelet coefficients. Also the Daubechies *'db4'* performing the wavelet analysis has a larger energy distribution as compared to *'db6'*, *'db7'*. The key benefit afforded here is to reduce the holistic shape of the fault event to a small number of wavelet coefficients. Some representative mother wavelets are shown in Figure 3.3.

### 3.4.3 Multi-Scale Discrete Wavelet Transform

As mentioned previously, to seek a representation of the current signal that captures both its local and semi-global time-and- frequency properties as a compact collection of numbers. As such it is required to consider semi-global information to differentiate rapid signal fluctuations from true fault signals and local information to quickly detect a fault condition. This need for both semi-global and local analysis is provided by applying the multi-scale DWT.

The multi-scale DWT is generated by recursively applying the DWT to the DWT approximation coefficients where by taking the input signal as the initial approxima-

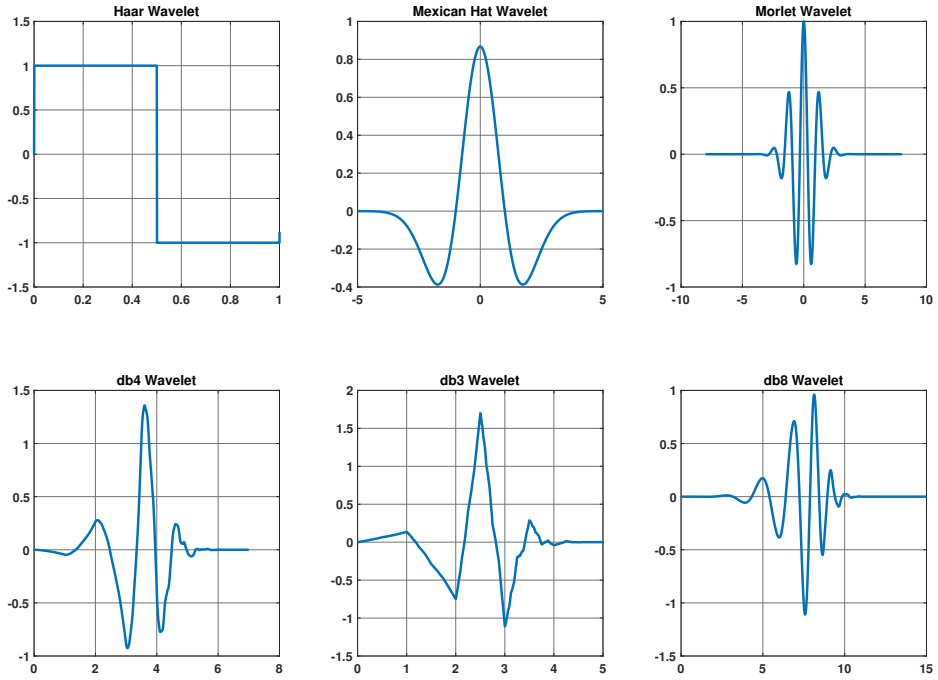



Figure 3.3: Commonly used mother wavelets

tion coefficients. For the multi-resolution analysis, a suitable sampling frequency band is chosen for the signal spectrum matching the signal frequency. Each scale is generated by applying the DWT to the approximation coefficients from the previous level starting with the input signal at the top-most level, e.g, $A_1[k] = h[-2n] * x[n]$ and $A_j[k] = h[-2n] * A_{j-1}[n]$ and $D_1[k] = g[-2n] * x[n]$ and $D_j[k] = g[-2n] * A_{j-1}[n]$.

As scale increases the spatial resolution of the DWT decreases and the frequency resolution of the DWT increases. Hence, spatially-local variations of the signal are best captured in DWT coefficients having small scale values and semi-global spatial variations are best captured in DWT coefficients with large scale values. Conversely, signal frequency content is best captured in DWT coefficients having large scale values and low frequency content are captured in DWT coefficients with small scale values. A three-level decomposition of a signal using MRA is shown in Figure 3.4. The specific time-and-frequency trade-off as the coefficient scale varies can be well understood by

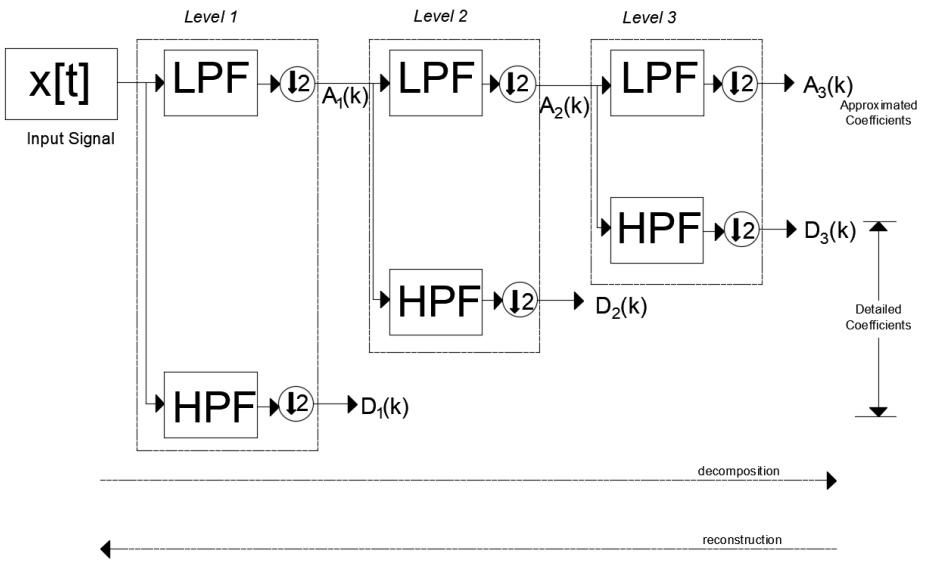



Figure 3.4: A 3-level DWT.

answering the following two questions:

**How local is a coefficient at scale j**

As discussed earlier the parameter $b = ka$ defines the position of the wavelet, while a governs its frequency. As the scale i.e. $j$ increases the frequency resolution increases as, $a = 2^{-j}$ , thus the time resolution decreases. The implementation of wavelet transform in PSCAD/EMTDC [41] is done on an "online" basis, it uses a finite impulse response (FIR). Typically, for processing the FIR filters require a specific length of the input data before processing. Steady state denotes the unique lag index $k = \frac{N-1}{2}$ here the coefficients at all DWT levels rely on input sample data from lag indices $x[n-n_0]$ where $n_0$*=0,1,...,N-1.* The length of the output sample delay with respect to the input is dependent on the type and scale of the wavelet transform. Table 3.2 shows the lag in samples between input samples and the wavelet-transformed output for different types wavelets.

Table 3.2: Output sample delays ($*\triangle$t)

| **Level** | **Haar** | **Db2** | **Db4** | **Db8** |
|---|---|---|---|---|
| 1 | 2 | 4 | 8 | 16 |
| 2 | 4 | 10 | 22 | 46 |
| 3 | 8 | 22 | 50 | 106 |
| 4 | 16 | 46 | 106 | 226 |
| 5 | 32 | 94 | 218 | 466 |

**What frequencies are represented in scale j**

Frequencies are well defined at higher values of $j$. As the scale increases a wider representation of the frequency band is achieved with the expense of a poor resolution in the spatial domain.

Due to the down sampling process, the spatial domain that determines of each coefficient doubles at each scale and the frequency domain of the transform coefficients halve. The signal bands ranges in $D_j[k]$ and $A_j[k]$ obtained upon reconstruction as given in (3.3);

$$\begin{cases} D_j[k] : [\frac{f_s}{2^{(j+1)}}, \frac{f_s}{2^j}] & (j = 1, 2, 3, ..., J) \\ A_j[k] : [0, \frac{f_s}{2^{(j+1)}}] \end{cases} \tag{3.3}$$

Table 3.3 shows the spectral bandwidths of the DWT at sampling frequency $f_s$ = 50kHz. The frequency decomposition using a DWT is shown in Figure 3.5.

Table 3.3: DWT frequency spectrum for $f_s$= 50kHz

| Level | Approximation$[A_j(k)]$(kHz) | Detail$[D_j(k)]$(kHz) |
|---|---|---|
| 1 | $A_1 : [0, 12.5]$ | $D_1 : [12.5, 25]$ |
| 2 | $A_2 : [0, 6.25]$ | $D_2 : [6.25, 12.5]$ |
| 3 | $A_3 : [0, 3.125]$ | $D_3 : [3.125, 6.25]$ |

## 3.5 Methodology

The proposed general approach for fault detection using wavelet transforms consists of the following steps:

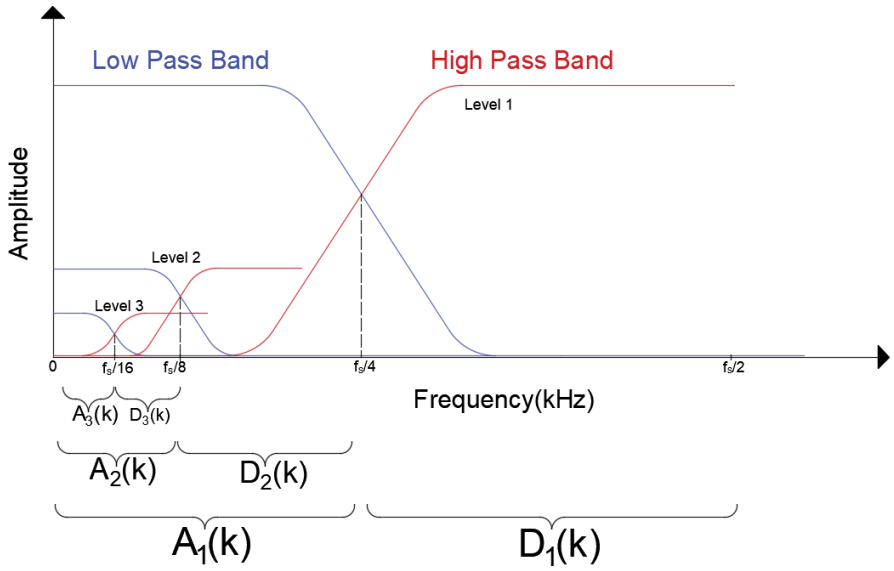



Figure 3.5: A 3-level frequency decomposition using MRA

1. Identify the wavelet transform parameters that map HVdc fault events to specific basis function in a time-and-frequency decomposition;

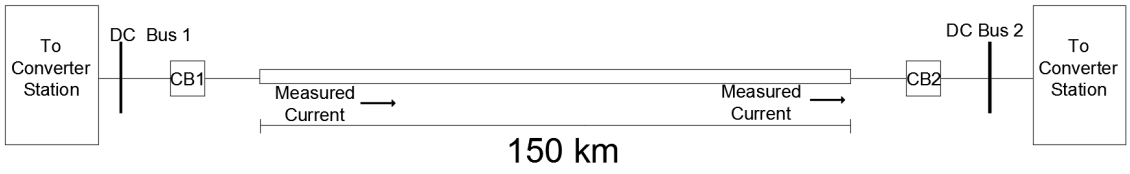
2. Use the energy of these basis function coefficients as a feature for detection.

Additional considerations are taken into account to consider the current direction to improve reliability. The distribution of energy at various levels allows the user to detect the persisting problems. In power system relaying, the use of wavelets to periodically analyze the transient signals leads to efficient performance of the protection system. They also help to identify the location of the fault by capturing the time of arrival of the travelling waves.

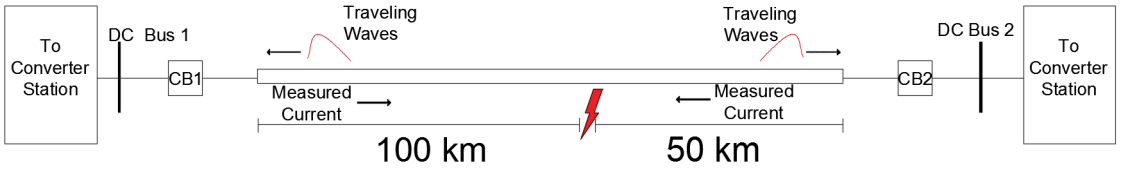
### 3.5.1 Fault Propagation Through the Network

The fault point in a cable is treated as the point of lowest impedance. The fault feeding network consists of dc link capacitors, adjacent connected feeders and also the grid side network that has a free-wheeling action for the fault current. During a ground fault, the system voltage drops rapidly [42]. Due to the high imbalance in impedance it gives rise to voltage surges traveling towards the terminals from the

point of the fault. The voltage surges are reflected back as positive surges due to the capacitive termination of the dc cable [43]. The midpoint of the dc capacitors are usually grounded providing a voltage reference. The grounded capacitor midpoint and the fault point induce the voltage discharge of the capacitors. The current discharge are usually superimposed on the traveling surge waves, thus, providing an indication of the change in current direction. The effect of the distributed capacitance does not impact the current direction under fault. Thus, at the faulted cable, the current directions at either ends of the transmission line are complementary to each other. The other current directions may also reverse depending on the location of the fault, but their current directions change in pairs as shown in, Figure 3.6(a) and 3.6(b).




(a) Normal condition




(b) Under fault

Figure 3.6: Current direction, (a) under normal condition, (b) traveling waves generated and monitored current polarities

### 3.5.2 Detection Strategy for Cable Faults Using the Wavelet Transform

For this application, by applying an "online" discrete wavelet transform to discrete samples from the sampled current signal. In this context each new sample value is taken into a wavelet transform filter and generates a collection of wavelet coefficients. The number of coefficients generated depends upon the number of chosen scales for the wavelet transform.

The proposed detection strategy computes wavelet transform coefficients for the input signal, *x[n]*, as each sample is captured. A 3-scale wavelet transform on the input signal then produces 4 wavelet transform coefficients: $A_3[k], D_1[k], D_2[k], D_3[k]$. A feature, $X[k] = D_1^2[k] + D_2^2[k] + D_3^2[k] + A_3^2[k]$ and uses the energy of the wavelet coefficient as a test statistic to detect the fault condition.

1. *Time Delay Analysis:* The output samples from a 'online' wavelet transform are time-delayed due to the nature of its filter operation. The number of input sample delay is shown in Table 3.2. The time delay between the time of fault and when the wavelet transform captures it depends on the sampling frequency and the type of wavelet selected. The wavelet operation is based on convolution of the input signal with predefined filter as per each wavelet type. Considering *'db4'* as the wavelet signal, the sample delay at scale 1 is 8 samples, and with a sampling frequency of $f_s$ the first output sample will have a delay of 0.16 ms. Some offline tools for wavelet transform such as MATLAB [44], is able to provide accurate results without any sampling delay. Specifically, *X[k]* will only partially capture frequency content from the most recent sample data. When this data is samples in the past, the frequency content of *x[n]* will be strongest (in terms of magnitude) in the feature *X[k]*. As such, *X[k]* lags *x[n]* in terms of its spatial and frequency characterization of *x[n]*. The index when the first output sample is received, with the first sample at index 0 is given by (3.4);

$$r(j) = (2^j - 1) * (m - 1),\ j = 1, 2, ..., J \tag{3.4}$$

where, $J$ is the maximum scale of the wavelet decomposition and $m$ is the length of the wavelet filter. By using orthogonal filters for analysis, both the high pass and low pass filters are of the same length.

2. *Fault Detection and Isolation:* The detection scheme is computed as a result

of two detection processes: (1) detects changes in current shape due to the traveling wave and (2) detects changes in current direction.

### Detecting Traveling Fault Waves

Data discussed in the results Section 3.7, demonstrates that typical power faults exhibit characteristic frequency signatures. Analysis of these signatures provide motivations for the proposed detection approach. This approach focuses on specific frequencies uniquely excited under fault circumstances. The wavelet transform provides a fast detection technique allowing faults to be detected and isolated more quickly than existing approaches.

Table 3.3 shows the frequency distribution of a 3-level wavelet transform and with a 50kHz sampling frequency, $D_3$ contains the fault frequencies of interest, i.e. 3kHz - 6kHz, from the power signal. The detection scheme computes a feature from this frequency band similar to the power spectral density of the signal within this frequency band.

As a loss less transform, the total energy of the signal is conserved in the wavelet coefficients as is confirmed for all lossless transforms via Parseval's theorem [45]. For wavelet analysis Parseval's theorem takes the form shown in (3.5);

$$\frac{1}{N}\sum_{n} x[n]^2 = \frac{1}{N}\sum_{j=1}^{J}(\sum_{k} A_{j,k}^2 + \sum_{k} D_{j,k}^2) \tag{3.5}$$

where, $N$ is the number of samples from the input $x[n]$ transformed. In (3.5) states that the average power of the signal is equal to the average power of the wavelet coefficients. Faults introduce high frequency content to the signal that changes the distribution of energy within the wavelet transform coefficients. Experimental work has shown that detail coefficients within $D_3$ capture frequencies indicative of faults. For fault detection, the total energy of the wavelet

coefficients in this band are calculated as described by (3.6). The corresponding energy change on the onset of a fault can be normalized as given as (3.7);

$$H_3 = \frac{1}{N_3}\sum_k D_{3,k}^2 = \frac{\|D_3\|^2}{N_3} \tag{3.6}$$

$$N_{3,energy} = \frac{H_3}{\sum_{i=1}^{p} H_{3,i}} \tag{3.7}$$

where, $\|D_3\|^2$ represents the average power spectral density of the detail coefficients and the norm of the expansions of the coefficients of $|D_3|$ at level *3*. $N_{3,energy}$ corresponds to the normalized energy change observed at $H_3$ and $i$ represents the number of cables in the system. The net energy distribution of the function remains unaffected due to the disturbance present in the system. If the sum of the normalized value of the energy coefficients exceeds the threshold (i.e. 1) a fault is detected in that zone. Due to the scale and complexity of a MTdc system, additional measures are taken into consideration to ensure a correct detection.

The traveling wave detection method helps to identify the frequencies that are most excited under a dc fault. The values of $D_3$ correspond to the fault frequencies as shown in Table 3.3.

Environmental conditions and power grid topology may change the spectral content of a fault signal. While this may alter the analysis as provided results, the approach remains valid if the fault signal's spectral content is distinct from a standard, i.e. non-fault power signal that are assumed to be true. Changes would require targeting the new frequency band(s) that uniquely correspond to fault signals.

### Detecting Current Direction Change

The background provided in Section 3.4.2 discusses the principle of using directional relays for fault sensing. The directional relays are preset for a particular current

direction [46]. However, during fault, the current direction from one of the converter ends change as it begins to feed the fault. The directional relay senses this change and updates its decision making as discussed previously. This feature demonstrates the importance of current direction for fault detection. incorpotating this attribute into the detector regarding the decision making process in order to trigger a breaker response.

The decision regarding the fault and the breakers to operate are made by simultaneously checking for the wavelet energy coefficient change and also the directional change of current. If two conditions decide 'yes' (i.e. 1) a fault is detected and a trip command is sent to the breaker, using (3.8);

$$Trip_{decision} = A_{Wavelet}.B_{Direction} \tag{3.8}$$

### 3.5.3 Algorithm

In Algorithm 2, the detectors present at each converter station monitor the current signals on a real-time basis, and the corresponding wavelet energy coefficients are computed. Upon the onset of a fault in a section of a cable travelling waves are generated as discussed previously, and they reach the detectors at different time intervals due to the asymmetrical location of the fault. The detectors computing wavelet transform in real-time are able to capture the arrival of the first peaks of the travelling waves. When this occurs $H_3$ changes. If $H_3$ exceeds the threshold and a change of current direction in the cable is observed, then a fault is detected. When a fault is detected the breaker connected to that cable is operated to isolate the faulted cable.

## 3.6 Modeling

To evaluate the approach, a three terminal HVdc system as shown in Figure 3.7, was designed in the PSCAD/EMTDC simulation platform. The system consists of

**Algorithm 1:** Fault Detection

**while** *DC line current* $I_{dc} > 0$ **do**
  Compute *3*-level wavelet transform *(db4)*; $Eq.(1)$;
  Compute Wavelet energy for each line current; $Eq.(6)$;
  Normalization of energy coefficients $N_{j,energy}$; $Eq.(7)$;
**end**
$Flag_{dir} = 0$;
$Flag_{energy} = 0$;
Check:
$I_{dir}$ =current direction at opposite cable terminals;
**if** $I_{dir} < 0$ **then**
  $Flag_{dir} = 1$;
**else**
  $Flag_{dir} = 0$;
**end**
**if** $N_{j,energy} > Threshold$ **then**
  $Flag_{energy} = 1$;
**else**
  $Flag_{energy} = 0$;
**end**
**if** $Flag_{energy}$ && $Flag_{dir} == True$; $Eq.(8)$ **then**
  **Fault Detected**; Trip command send to respective breakers;
**else**
  **goto** line 1;
**end**

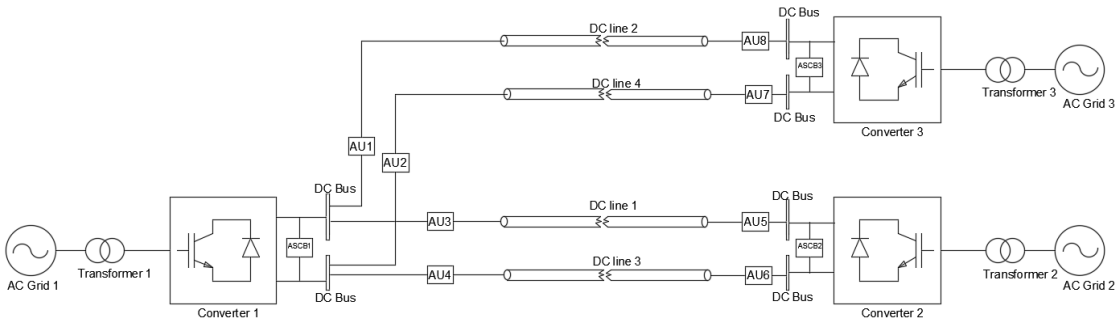



Figure 3.7: Three terminal VSC HVdc network

two ac utility grids connected through a HVdc link. The ac grid 3 is assumed to be 200 MW in the dc link that is operated at ±500 kV, shown in Figure. 3.8. The power is delivered to converter stations 1 and 2, connected to on-shore utility grids. Converter 1 is designed to supply for the losses in the system and also any additional requirement of power into the dc link, when there is a change of output voltage at converter station 1. The dc cables are modeled using a detailed frequency dependent cable model [47] in PSCAD/EMTDC. A detailed system description is given in Table 3.4. The cross-sectional diagram from the cable is shown in Appendix A. Converter 1 is used to control the voltage ($V_{dc}$ control) of the dc link and converter station 2 is operated under P-Q control.

## 3.7 Simulation Results

To verify the efficacy of the proposed algorithm, various simulation conditions were evaluated to ensure proper detection of the faulted cable. At time t = 2.8s, the power delivered by converter station 3 changes from 200 MW to 178 MW, converter station 1 supplements for the change in power transfer. The change in power of the converter stations is shown in Figure 3.9.

The change in load does not give a false trigger to the breakers to turn-on since traveling waves are not generated due to load changes in the cables.

At time t = 4.3s, a low impedance line-to-ground fault, occurs at dc cable 1, as shown in Figure 3.6(b), 50 km from converter station 2. The fault generates traveling

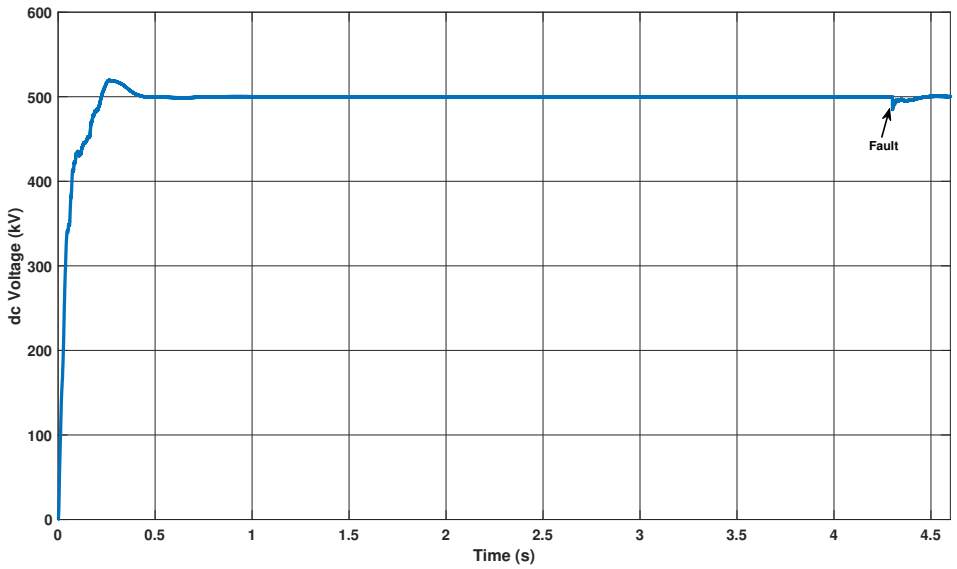



Figure 3.8: Voltage of the dc bus operating at 500kV

Table 3.4: Test system description

| | **Items** | **Values** |
|---|---|---|
| dc Side | dc bus Voltage | ±500 kV |
| | Length of Cable 1 | 150 km |
| | Length of Cable 2 | 150 km |
| | Length of Cable 3 | 200 km |
| | Length of Cable 4 | 200 km |
| ac Side | System Frequency | 60 Hz |
| | Active Power Converter 1 | 45 MW |
| | Active Power Converter 2 | -200 MW |
| | Active Power Converter 3 | 200 MW |
| | ac System Voltage (L-L) | ±230 KV |
| | Source Inductance | 7 mH |
| | Transformer Rating | 1500 MVA |
| | Transformer Leakage Reactance | 0.1 p.u. |
| Transmission Line | Series Impedance | 0.0002252 Ω/m |
| | Shunt Admittance | $10e^{-10}$/m |

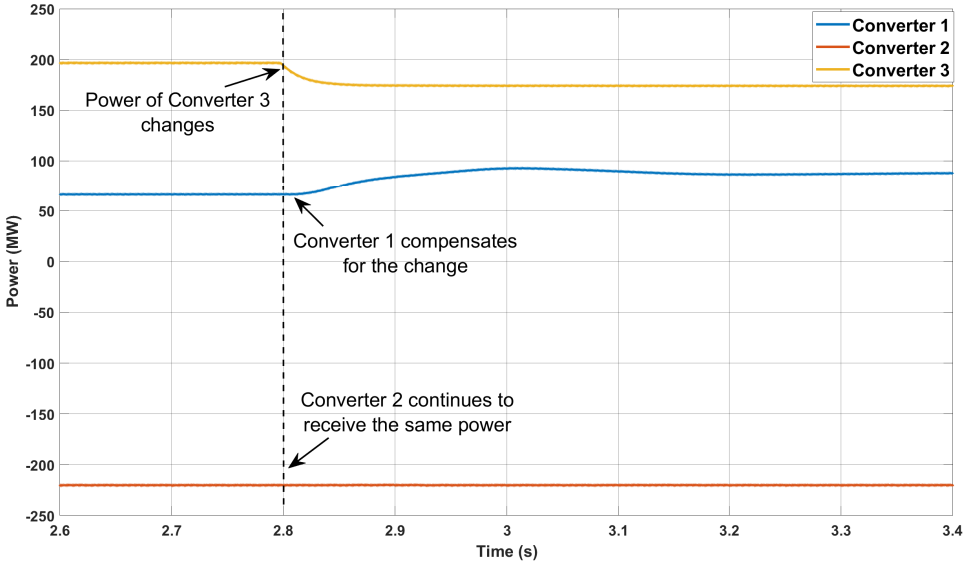



Figure 3.9: MTdc power sharing

waves in the cable, due to the sudden change in voltage at the fault point, whose energy is captured by the wavelet transform.

The cable current is sampled at $f_s = 50$ kHz (a very common sampling frequency for power applications). Modern digital relays are able to operate with higher sampling frequencies [48].

Quantization of the current signal due to analog to digital converter (ADC) introduces high-frequency noise at all frequencies, include the frequencies of $H_3$. As such, by over-sampling to signal the noise in the sensitive frequency range of the detector is diminished. For commonly used Sigma-Delta ADCs noise shaping can contribute to further reduction of noise in the frequencies used for detection. Certain amount of noise and distortion starts appearing on the signal from the use of real-field measurements. If a signal is over-sampled by a factor $k$, there is a significant drop in the noise energy spreading over a wider frequency range.

The change in direction of the current in the faulted dc cable helps to confirm the faulted cable. Since the fault is closer to converter station 2, the waves arrive at the

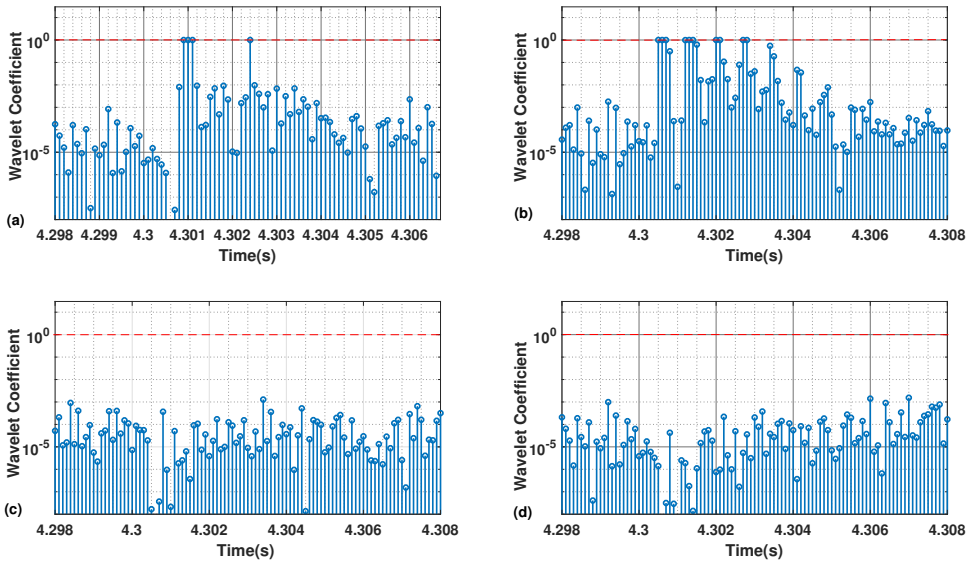



Figure 3.10: DWT energy coefficients, (a) Measurement at cable 1 near converter station 1, (b) Measurement at converter station 2 at cable 1, (c) and (d) measurements at converter stations 1 and 3 respectively for cable 3.

location earlier as recorded by the wavelet coefficients.

During the same time, the wavelet coefficient for the other cables exhibit changes as the travelling wave generated at the fault point would traverse through the entire network, the frequencies at those locations are attenuated and thus do not reach the threshold, thereby preventing false trigger. The initiation of the assembly HVdc breaker results in the removal of cable 1 from operation of the HVdc grid; however, the other lines remain operational.

Using (3.6), the energy change associated in the faulted cable. The energy change is normalized over time using (3.7). The contributions of the wavelet energy coefficients in comparison to an unfaulted cable is shown in Figure 3.10.

As discussed previously that the high frequency components of the fault signal provide us with more information at detailed level 3 rather than at lower levels. The contribution from $D_3$ coefficients are compared with $D_1$ under fault conditions in Figure 3.11.

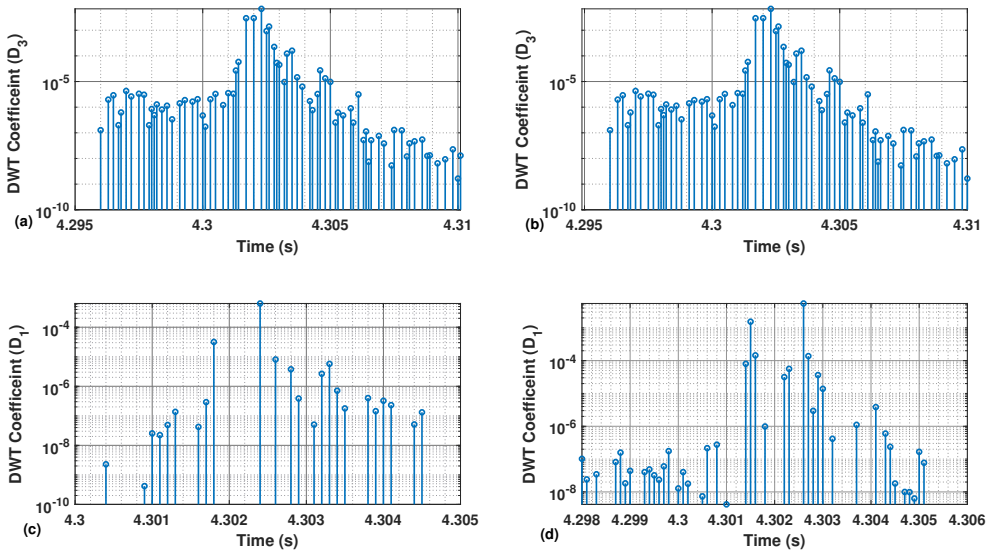



Figure 3.11: Contribution of detail coefficients during fault; (a) and (b) show the contribution of $H_3$, (c) and (d) show the contribution of $H_1$

The operation of the assembly HVdc breaker is completed within 3-4ms and the ASCB opens, thereby restoring the dc bus voltage after t = 0.35s of the fault inception, as shown in Figure. 3.13. The ASCB and auxiliary sischarge switch (ADS) do not carry the load current under normal operating conditions. After the fault identification is made, the ASCB and ADS are turned on and the currents begins to rise, the main breaker is turned off after an interval of 250$\mu$s. Thus, the disconnect switch can be operated at zero current. It can be seen that the main breaker and the disconnect switch operate under low fault current, and can be designed to carry only up to two times the rated current. The effort for breaking the fault current is done with the help of the ASCB, that can be designed with higher capacity. The current in the ADS branch goes to zero through the dissipating resistor that is connected in series.

The fault detection and isolation is achieved within the desired time frame. This high operational speed prevents the system from catastrophic failure, and also prevents false trigger of the breaker in the other lines as shown in Figure 3.12.

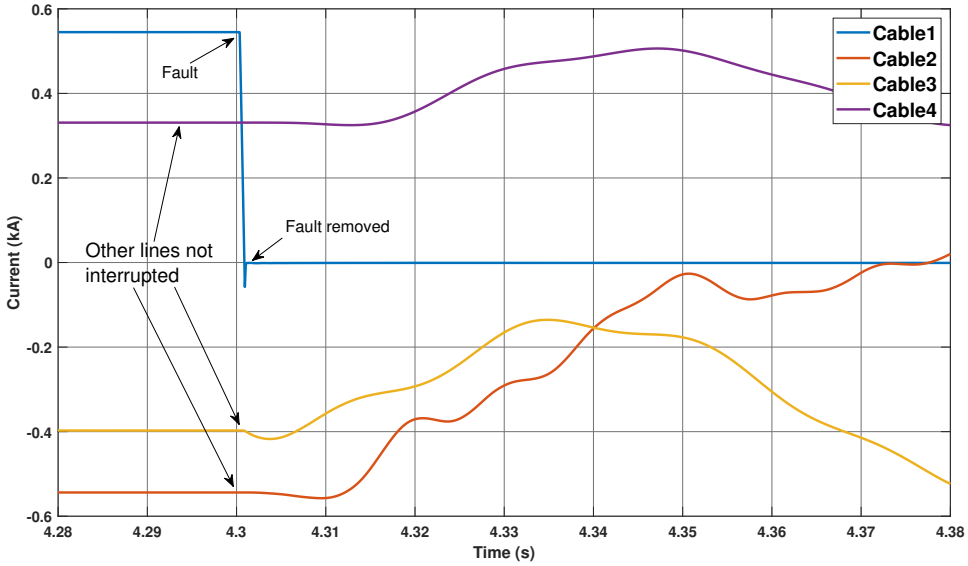



Figure 3.12: Cable current

The operation of the assembly HVdc breaker is completed within 3-4ms and the ASCB opens, thereby restoring the dc bus voltage after t = 0.35s of the fault inception. Once the ASCB is turned on it creates a temporary short circuit at the dc bus, but the voltage levels are not affected by this temporary short-circuit condition. The fault is isolated and the dc bus voltage is restored as shown in Figure 3.13.

The current distribution in the assembly HVdc breaker under fault condition is shown in Figure 3.14. Since the ASCB creates a temporary short circuit at the dc bus, it lowers the fault current in the auxiliary branch, making it possible to design it with a lower rating.

### 3.7.1 Breaker Co-ordination and Operation

The breakers connected to the sections of the line are controlled individually, through a central decision making system. The breaker connected in cable 2 is not affected by a fault in cable 1 and vice-versa. As discussed in Section 3.3.1, the ASCB and ADS remains turned off (grey), under normal operating condition as shown in Figure 3.15. On the onset of fault in cable 1, the fault detection picks up travelling

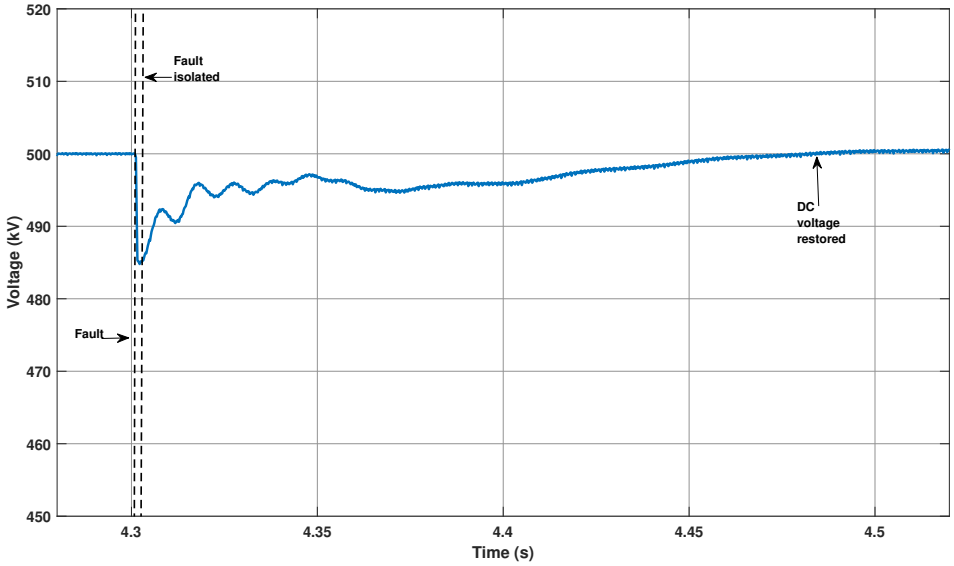



Figure 3.13: Voltage restoration after fault is removed

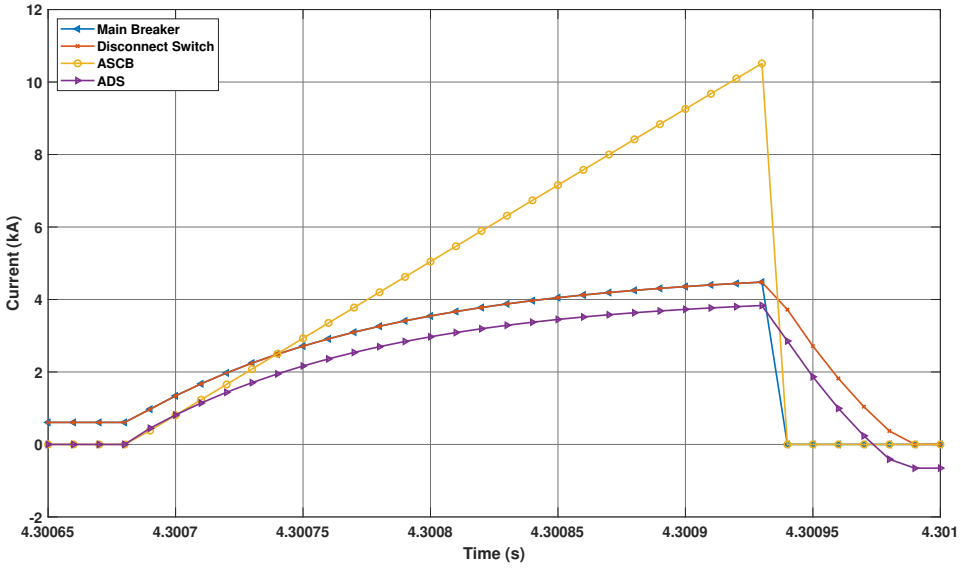



Figure 3.14: Assembly HVdc breaker current characteristics

waves. Algorithm 2 computes the change in energy content of the signal using wavelet transform and co-ordinates the breakers connected to the concerned cable to operate in a sequential operation as shown in Figure. 3.16. After the fault has been isolated the ASCB and ADS return to their original off state, shown in Figure 3.16(b), thereby

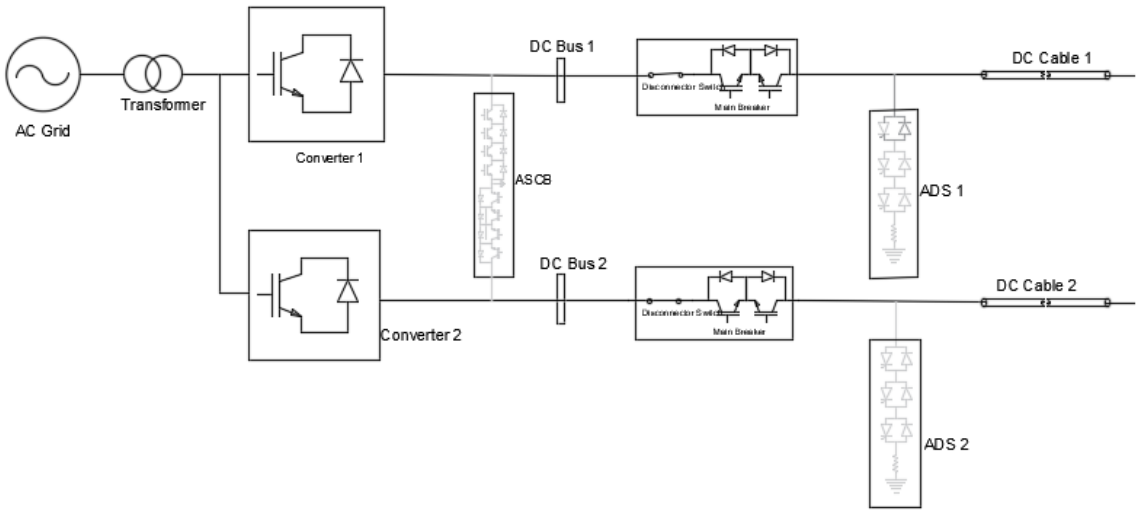
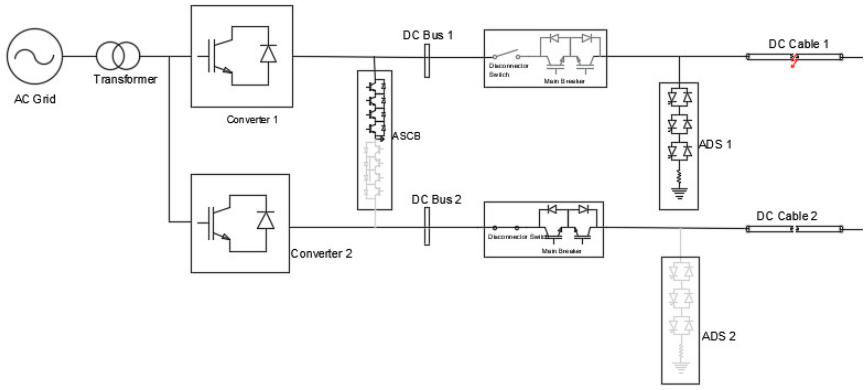


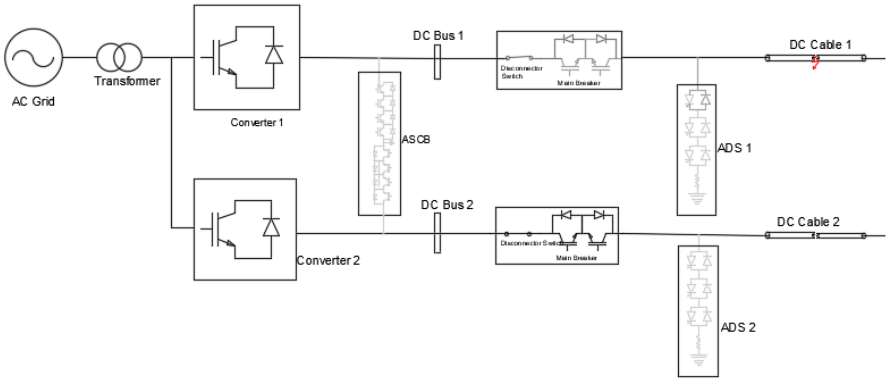

Figure 3.15: ASCB under normal operating conditions

completely isolating the faulted cable. Cable 2 adjacent to cable 1 is not affected by the fault conditions. The breaker operations are shown in Figure 3.17(a) and 3.17(b).

The disconnector switch modelled in PSCAD is defined as closed when the signal state is 0 and open when the state is 1, whereas it is just the opposite for other semi-conductor modelled switches.

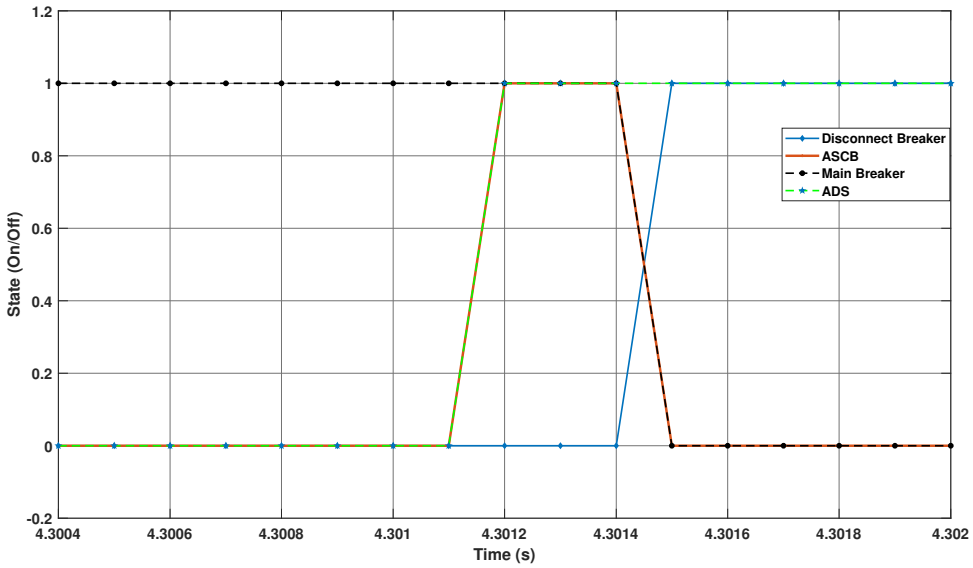



(a) ASCB and ADS turns on; main breaker is turned off

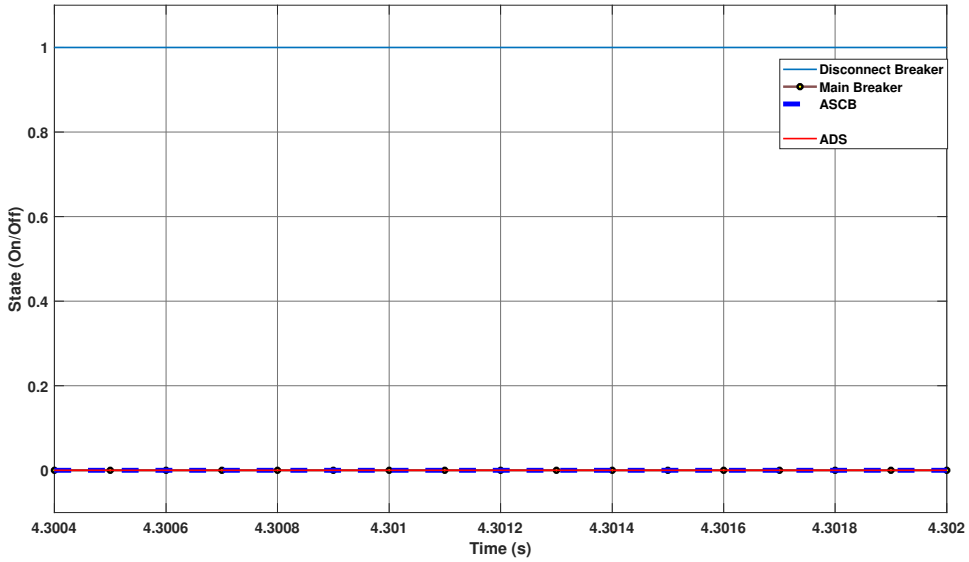



(b) Fault isolation complete

Figure 3.16: Assembly HVdc breaker operation




(a) Operational diagram of breaker connected to cable 1




(b) Operational diagram of breaker connected to cable 2

Figure 3.17: Assembly HVdc breaker operational states

## 3.8 Conclusion

This work presents dc fault detection and clearing capability of assembly HVdc breakers using a traveling wave protection scheme for a three-terminal VSC based

HVdc system designed in PSCAD/EMTDC. With conventional fault locating strategies, dc breakers have to be coordinated separately for each system. However, sudden load changes can result in false triggering of the dc breakers, resulting in a complete shutdown of the system.

In order to overcome the shortcomings of the traditional strategies, a coordinated protection strategy for assembly HVdc breakers has been proposed in this Chapter. The idea behind the strategy is to develop a dynamic protection scheme that can be utilized for any HVdc grids to prevent any shortcomings that are present in the traditional protection strategies. The methodology leverages to target specific frequencies that are most excited at the onset of a fault. Using wavelet transform, the distribution of energy due to fault at various levels are recorded. Experimental work has demonstrated the contribution of $D_3$ has the most impact indicative of the fault frequencies. This change in the energy of the signal along with directional change of current in the cables at the fault point can be utilized to detect the faulted cable. The ASCB design also offers an advantage over the other dc breakers - it allows the main breaker to operate at a lower current, and the fault current is shunted into the ASCB.

The proposed strategy is unique due to its dynamic nature and provides a superior solution among the alternatives considered for implementation in a complex multi-terminal grid. The control strategy is fast in detecting the faulted section of the grid and operating the breakers to isolate it from the grid in order to resume normal operations for the rest of the grid.

The fault signals are recorded simultaneously at both ends i.e. a double sided measurement, that have the same time reference. This is achieved with the help of Global Positioning System (GPS) devices. Traveling waves posses the advantages of not getting affected by fault resistance, system parameter, location of fault etc. The accuracy of GPS devices are dependent on the ability to capture wave peaks. High-

sampling frequency and data acquisition tools are necessary to record and perform analysis of the wave peaks to locate faults. Single-ended measurements that do not require a time synchronized device to record the signals are also utilized for fault locations. Single ended measurements are cheaper to realize but their accuracy is subject to the ability to capture wave reflections to accurately locate faults. Thus, a method utilizing cable current discharge after proper isolation has been proposed in Chapter 5.

# CHAPTER 4: FAULT DETECTION BASED ON LOCAL MEASUREMENTS

## 4.1 Overview

Fast and accurate methods of fault detection and isolation is a pre-emptive measure in MTdc. Zonal isolation of faults is necessary to prevent any misopertation of the dc breakers that can lead to a shutdown of the network. Existing techniques require fast-communication or data synchronization methods have their own disadvantages. This Chapter proposes a method for efficient fault zone isolation without the need of a communication link, that prevents any misoperation of the dc breakers in a radial MTdc. This method provides individual local measurement based control to the hybrid dcCB. Faults created outside the zone of protection for a breaker creates a change in the rate of change of current or voltage leading to misoperation.

HVdc transmission systems have made significant progress in power transmission owing to the advancements in power electronics. HVdc systems have been found beneficial for interlinking multiple ac asynchronous generation systems through underground cables or overhead transmission systems, that have accounted for transport of renewable generation from remote locations. Such benefits have led to the expansion of existing ac grids in the form of back-to-back links, MTdc systems.

Initially, HVdc systems were designed as back-to-back terminals with LCC. Though LCC designs could be developed for higher voltage ratings, but the lack of power reversal capability prevented further development [49]. The MMC has become a powerful candidate in the development of VSC-HVdc systems [50], [51]. In comparison to other multi-level topologies, the MMC has certain salient features including (1) higher efficiency; (2) better scalability; (3) absence of dc link capacitors [52]. The development of MTdc networks is hindered by the fault detection and isolation techniques for dc

networks.

One of the challenges faced by MMC is its operation under dc faults. Conventional MMC design, as shown in Figure 4.1, HBSM rather than full-bridge modules FBSM. FBSMs are fault tolerant, but have lower operational efficiency than HBSMs due to more semiconductor switches. The challenges pertaining to MMC operation include: (1) fast detection and isolation of the faulted transmission line and (2) avoiding false fault detection due to non-fault high frequency transients.

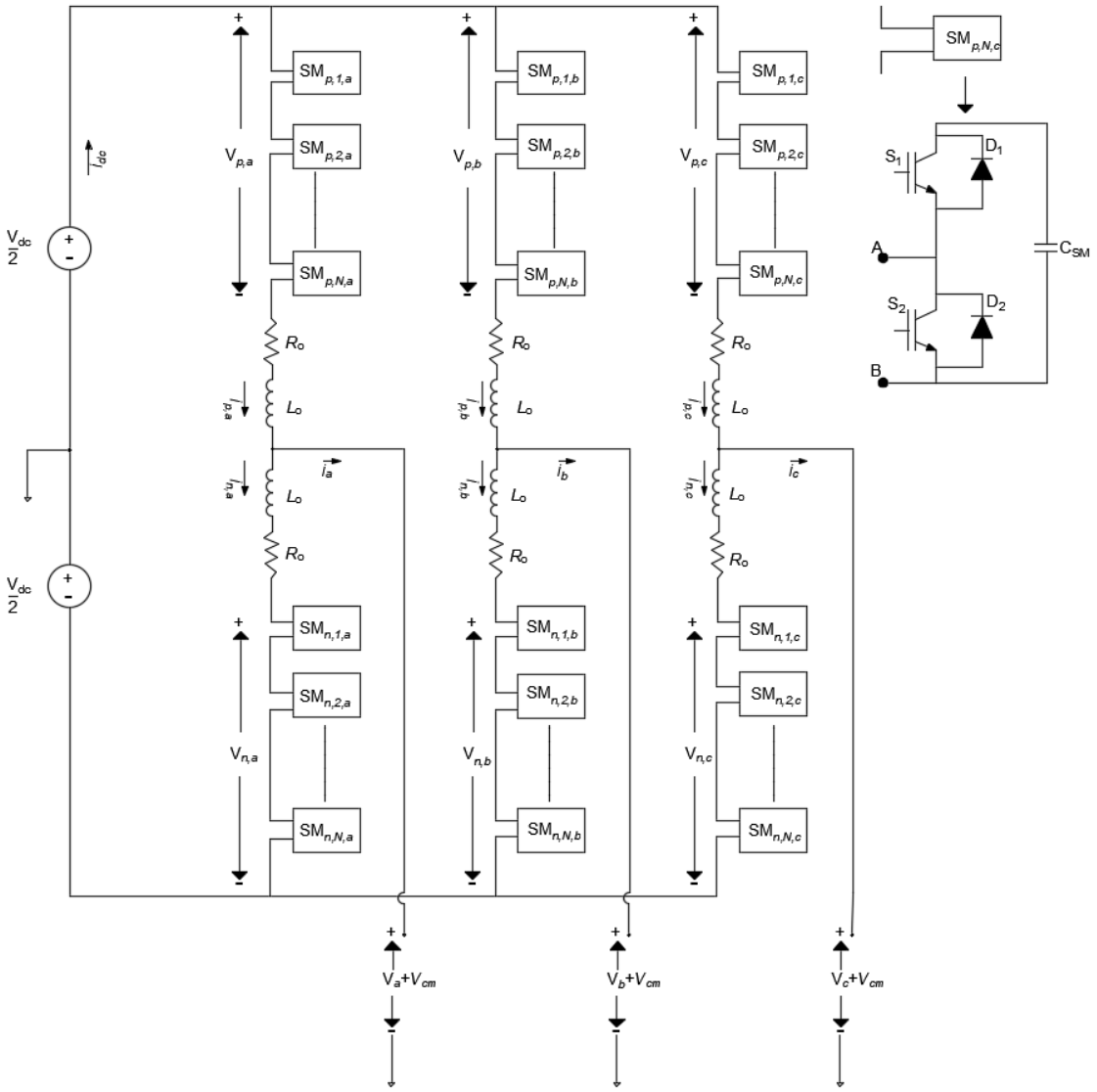



Figure 4.1: Detailed schematic of MMC

The work reported in [7] demonstrates the need for rapid fault detection and iso-

lation in the order of milliseconds to safe-guard the HVdc transmission system from commutation failure. Current and voltage thresholds are subject to sensitivity of fault transients, that leads to slow and incorrect fault detection [53].

A system fault causes a sudden change of voltage near the fault, causing electromagnetic transient waves in the form of travelling waves to propagate bilaterally through the network. Fault transients caused by the traveling waves contain information that provides us with the idea of time, location, etc. of the fault. An analysis of the traveling waves reveals the nature of the fault. Traveling almost at the speed of light, the waves caused by faults cause current doubling that necessitates a high speed fault detection mechanism.

Certain existing methods for protective relaying for MTdc networks include derivatives of voltage and current, over current and under voltage protection, detection of traveling waves etc [54]. Approaches in [55] and [56] involve comparison of current and voltages at the ends, that is used in detection of faults. These methods require a fast communication that is difficult to achieve and subject to reliability problems [57]. The detection and isolation method discussed in [58] does not require any communication, but involves isolation of certain healthy branches for some time interval, and a momentary shutdown of the entire system. Methods elaborated in [58] and [59] give us an understanding of the current and voltage discharge characteristics in the dc system but fail to provide any fault detection strategies. The dc voltage derivative method introduced in [21] emphasizes the quick isolation from dc faults, but neglects the influence of the arm reactor, and assumes the converter output dc voltage to be constant following a dc fault. A high rate of voltage derivative is observed after fault clearance by a breaker, leading to erroneous operation of the protection controller. The robustness of the algorithm to sensitivity of noise and fault resistance has not been evaluated. The method proposed in [22] analyzes the rate of change of dc reactor voltage and the minimum fault detection time. The selection of time intervals can be

complex under multiple converters feeding the fault current. Also the performance for line to ground fault has not been reported. The rate of change of current across the dc terminals has been considered for a communication-less fault detection scheme in [57], but the threshold parameter is subject to sensitivity to the change of current limiting inductance. To overcome the drawbacks of time-domain based protection algorithms, signal processing based methods have been proposed to extract the frequency components using STFT, wavelet transform and so on [60], [25]. The method suggested for fault detection in [61] uses wavelet transform for dc fault detection. Although this method shows good performance, it is subjected to a very high sampling frequency and complex calculations involving large computation time. The analysis performed in [28] evaluates only medium voltage dc systems (up to 20kV), whereas in [29], a machine learning based detection method is suggested, but the algorithm involves training a dataset, it has to be retrained when the operating conditions are changed and a new dataset is available, that requires significant time and effort and is computationally burdensome.

## 4.2 Contribution

The speed of fault propagation is faster than the current available communication technology, but the dc breakers need to be operated before the fault transient reaches its peak. Backup methods are usually kept in place in case of commutation failure, leading to further delay. Current approaches require the need for deployment of such communication channels for efficient fault detection and isolation.

This Chapter proposes the distinction and case-examples for fault detection methodology within the protection zone of the dc breakers based on the directional change of the current and voltage induced by the traveling waves in the faulted transmission line, and supported by the rate of change of the fault current and voltage. This ensures isolation of the faulted section of the transmission line from the rest of the non-faulted network, without the use of any communication channels. This Chap-

ter addresses the major features of the algorithm with regards to dc faults, such as (1) speed of detection; and (2) reliability and robustness. The hybrid dcCB's are controlled individually eliminating the use of any communication channels, that can introduce delays and is costly to realize. Sensitivity analysis performed under various operating conditions has been performed in MTdc systems using PSCAD/EMTDC studies. The results show the successful operation of the proposed detection algorithm.

## 4.3 Modeling

### 4.3.1 The MMC

The MMC model utilized in this Chapter is based on the design described in [62]. The detailed model is based on a 400 per arm HBSM. The simulation algorithm to speed-up the simulation of MMCs with a large number of SMs is based on the identification of numerical stiffness in the differential algebraic equations (DAE) defining the dynamics. Based on the identified numerical stiffness in the DAEs, they are discretized using hybrid discretization and relaxation algorithms described in [62]. The control of the MMCs is based on the strategies explained in [63], [64].

### 4.3.2 Multi Terminal dc Network

The model of a radial three-terminal HVdc system based on symmetric monopoles, as shown in Figure 4.2, has been developed in PSCAD/EMTDC. Additionally, the system is equipped with hybrid dc breakers at each MMC terminals. The distance between two adjacent HVdc substations is 1000 km with a dc-link voltage of $\pm$320 kV. Table 4.1 contains a detailed description of the system.

The overhead dc transmission lines have been designed as frequency dependent models having 6 conductors with a vertical spacing of 5m and horizontal spacing of 10m between the conductors. A detailed schematic of the transmission line parameters is presented in the Appendix B.

Table 4.1: System parameters

| | **Parameters** | **Value** |
|---|---|---|
| ac side | Voltage (L-L RMS) | 333 kV |
| | Length of transmission line 1 & 3 | 100 km |
| | Length of transmission line 2 | 150 km |
| | System Frequency | 60 Hz |
| | Transmission line resistance | 0.03206 Ω/km |
| dc side | Voltage (L-L) | 640 kV |
| | Length of transmission line | 1000 km |
| | Transmission line resistance | 0.03206 Ω/km |
| | MMC capacity | 1 GW |

### 4.3.3 Hybrid dc Circuit Breaker

The hybrid dc breaker model represents the breaker designed by ABB in [65]. The breaker design, as shown in Figure 1.5, comprises of three major sections, (1) load commutation branch, (2) main breaker branch and (3) the energy absorption branch. Under normal operating conditions the load commutation branch remains operational. As the fault detection command is generated the load commutation switches turn-off, the current recedes through the ultra-fast disconnector into the main breaker branch. On current zero detection the ultra-fast disconnect switch is opened. The fast mechanical switch protects the commutation switch from the entire dc line voltage during final interruption. The final interruption happens in the main breaker branch. The excess energy is absorbed by the MOV. The maximum time required to dissipate the energy depends on the capacity of the MOV banks. The MOV's were designed and rated at 800 kV. The introduction of two parallel branches reduces the on-state losses to 0.01% of the transmitted power [66], [67]. Faults occurring on the dc transmission line need to be interrupted very quickly. Current limiting inductors connected in series with the dc breakers acts as protective devices for the switches that limits the rate of change of current across them.

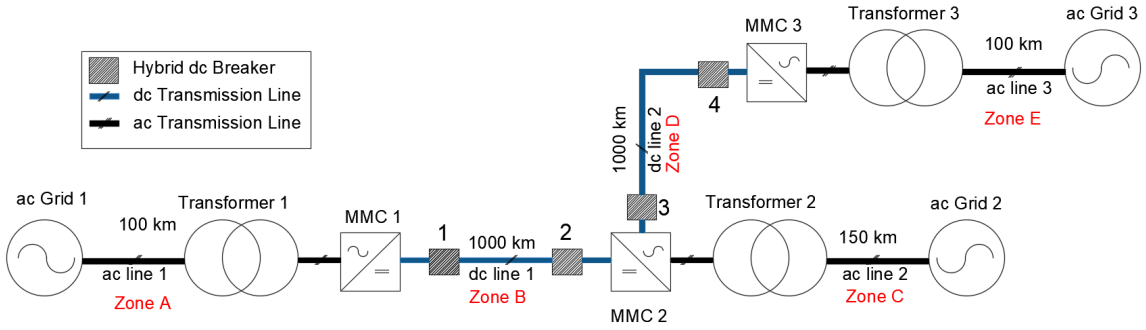



Figure 4.2: MTdc protection zones

## 4.4 Transient Analysis of Traveling Waves

Under normal operating conditions the dc voltage across the transmission line is constant. When a dc line-to-line or line-to-ground fault occur on a network it causes a rapid change of voltage. Electromagnetic waves in the form of traveling waves propagate throughout the network [68]. The post-fault voltage and current traveling waves are composed of steady state and transient components, that are expressed in (4.1).

$$\begin{aligned} i_{postfault} &= i_{prefault} + i_{transient} \\ v_{postfault} &= v_{prefault} + v_{transient} \end{aligned} \tag{4.1}$$

An analysis of $i_{transient}$ and $v_{transient}$ initiated by the fault on the system, provides the required information of the fault. The direction of arrival of the current and voltage waves as $i_{transient}$ and $v_{transient}$ respectively provides an indication of the fault occurrence zone.

Faults can be considered as the application of a fictitious voltage source that has been applied to the circuit of equal magnitude and opposite in sign to the pre-fault voltage. Figure 4.3 shows a schematic representation of different types of faults applied on ac-dc systems. The traveling waves generated travel away from the fault location towards the terminals at a velocity almost equal to $\sqrt{1/LC}$ m/s, where $L$

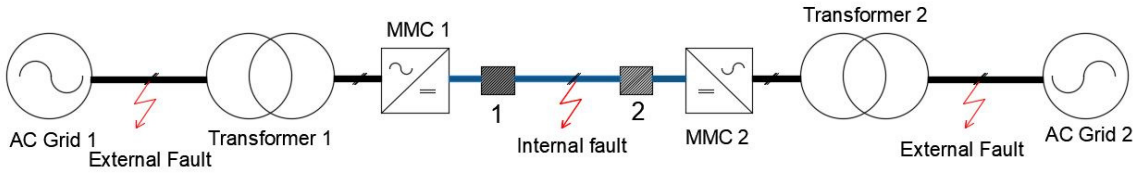



Figure 4.3: Fault classification

and $C$ are the per unit inductance and capacitance respectively of the transmission line.

Internal faults are described as any disruptions caused within the protection region of the concerned breakers, any other faults beyond it are considered to be external. Due to the shared dc bus architecture of HVdc systems, external faults can result in change of current and voltage in other healthy lines. Breakers in those lines can trip causing a disruption in service. A similar scenario can be observed for a fault in dc transmission line 1. Circuit breakers 2 and 3, shown in Figure 4.2, are located on two different transmission lines, but have the same $di/dt$ or $dv/dt$ due to the shared dc bus. Thus, a rate of change of voltage or current would cause an operation for both the breakers, creating a service interruption at the non-faulted dc transmission line 2.

A faulted transmission line can be realized by comparing the polarity of the arrival of $i_{transient}$ and $v_{transient}$. Voltage and current waves are superimposed on the dc transmission lines under a line-to-line or line-to-ground fault. The polarity of the imposed waves can be determined from the pre-fault polarity of the transmission line. Thus, on a positive transmission line, a negative voltage wave and a positive current waves are generated, and vice-versa. Table 4.2 shows the relationship of the pre-fault voltage with respective to $i_{transient}$ and $v_{transient}$.

As evident from Table 4.2, the polarity of $i_{transient}$ and $v_{transient}$ fail to provide a conclusive distinction about the faulted transmission line. Analyzing the polarity of transient waves alone can lead to misoperation of a circuit breaker on a healthy

transmission line, resulting in the shutdown of the entire system.

## 4.5 Rate of Change of Transient Current and Voltage at the Terminals

The MMC converter generates a rated dc voltage $V_{dc}$ under normal operating conditions. The upper and lower arm voltages $v_{upper}$ and $v_{lower}$ are given as (4.2);

$$\begin{aligned} v_{upper} &= \left(\tfrac{V_{dc}}{2}\right) - v_{ref} \\ v_{lower} &= \left(\tfrac{V_{dc}}{2}\right) + v_{ref} \end{aligned} \tag{4.2}$$

Similarly, the upper and lower arm currents are represented as (4.3);

$$\begin{aligned} i_{p,j} &= i_{circ,j} + \tfrac{i_j}{2} \\ i_{n,j} &= i_{circ,j} - \tfrac{i_j}{2} \end{aligned} \tag{4.3}$$

From Figure 4.1, the dynamic equations governing the dynamic behavior of MMC phase current and circulating current is given as [62];

$$\frac{V_{dc}}{2} - v_{upper,j} = L_o \frac{di_{upper,j}}{dt} + R_o i_{upper,j} + v_j + v_{cm} \tag{4.4}$$

$$\frac{V_{dc}}{2} - v_{lower,j} = L_o \frac{di_{lower,j}}{dt} + R_o i_{lower,j} - v_j - v_{cm} \tag{4.5}$$

where $j = a, b, c$ and $v_j$, $v_{cm}$ are the fundamental and common mode dc midpoint components of the MMC, $R_o$ and $L_o$ are the per phase inductance of the converter. Subtracting (4.4) from (4.5) and substituting $i_{p,j}$ and $i_{n,j}$ from (4.4), the phase current dynamics can be expressed as (4.6);

$$L_o \frac{di_{circ,j}}{dt} + R_o i_{circ,j} = \frac{V_{dc}}{2} - \left(\frac{v_{lower,j} + v_{upper,j}}{2}\right) \tag{4.6}$$

where, $i_{circ,j} = (i_{p,j} + i_{n,j})/2$.

During a dc fault the voltage drops below $V_{dc}$, consequently a high dc fault current is produced at the converter arms. From (4.6), it can be seen that the discharge of

Table 4.2: Change in polarity of $i_{transient}$ and $v_{transient}$ with respect to pre-fault voltage

| **Fault Location** | **Pre-fault Voltage** | **dcCB 1** | | **dcCB 2** | | **dcCB 3** | | **dcCB 4** | |
|---|---|---|---|---|---|---|---|---|---|
| | | $i_{transient}$ | $v_{transient}$ | $i_{transient}$ | $v_{transient}$ | $i_{transient}$ | $v_{transient}$ | $i_{transient}$ | $v_{transient}$ |
| dc transmission line 1 | +/- | +/- | -/+ | +/- | -/+ | -/+ | -/+ | +/- | -/+ |
| dc transmission line 2 | +/- | +/- | -/+ | -/+ | -/+ | +/- | -/+ | +/- | -/+ |
| ac transmission line 1 | +/- | -/+ | -/+ | -/+ | -/+ | -/+ | -/+ | -/+ | +/- |
| ac transmission line 2 | +/- | +/- | -/+ | -/+ | -/+ | -/+ | -/+ | +/- | -/+ |
| ac transmission line 3 | +/- | -/+ | +/- | -/+ | -/+ | -/+ | -/+ | -/+ | -/+ |

the dc fault current is governed by the dc components. The equivalent capacitance per phase of the MMC, under fault, can be obtained from [22] as $C_{eq} = 3C_{SM}/N_{arm}$, where $C_{SM}$ and $N_{arm}$ are the submodule capacitance and the number of submodules present.

From Figure. 4.4 the fault current can be deduced as [50];

$$\frac{\mathrm{d}^2 I_{fault}}{\mathrm{d}t^2} + \frac{R_{eq}}{L_{eq}}\frac{\mathrm{d}I_{fault}}{\mathrm{d}t} + \frac{1}{L_{eq}C_{eq}} i_{fault} = 0 \tag{4.7}$$

where $L_{eq} = L_o + L_{line} + L_{Limit}$ and $R_{eq} = R_o + R_{line}$, the second order differential equation can be solved under the under-damped condition $R_{eq} < 2\sqrt{\frac{L_{eq}}{C_{eq}}}$. The solution for (4.7), under the initial condition $I_{fault}(0)$=$I_{dc}$ is given as (4.8);

$$I_{fault}(t) = e^{-\delta t}\left[I_{dc}cos(\omega t) + \frac{(V_{dc}/L_{eq}) - \delta I_{dc}}{\omega} sin(\omega t)\right] \tag{4.8}$$

where,

$$\delta = R_{eq}/2L_{eq}$$

$$\omega = \sqrt{1/((L_{eq}C_{eq}) - (R_{eq}/2L_{eq})^2)}$$

Thus the rate of change of current can be analyzed by differentiating (4.8) at $t = 0$.

The dc fault current consists of the $i_{transient}$ component based on the analysis stated above. By monitoring consecutive samples of the dc fault current, the rate of change can be analyzed. If the sampled transient current exceeds $I_{Thres}$, a fault is detected utilizing (4.10);

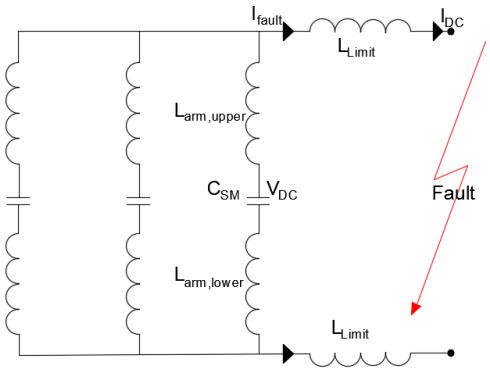
$$\triangle i_{transient} = i_{transient}(t) - i_{transient}(t + \triangle t) \tag{4.9}$$

$$\frac{\triangle i_{transient}}{\triangle t} > \frac{\triangle i_{Thres}}{\triangle t} \tag{4.10}$$

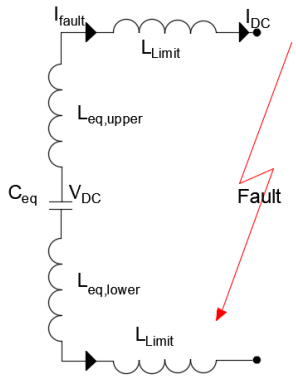
where $\triangle i_{Thres}$ is the predefined threshold of dc current across the current limiting inductor. Reference [22] discusses the change in voltage across the current limiting

inductor $L_{Limit}$ resulting in the change of $I_{fault}$ as (4.11);

$$I_{fault} = I_{DC} + \frac{1}{L_{Limit}} \int_0^T V_{Limit} dt \tag{4.11}$$




(a) MMC per phase equivalent circuit




(b) Equivalent model

Figure 4.4: MMC converter equivalent circuit under fault

The post fault voltage across the current limiting inductor remains steady under normal operating conditions. This Chapter proposes the analysis of the change in voltage across the terminal inductor only after the initial fault indication is triggered by directional change parameter. This prevents false identifications as a result of load change or other sensitivity changes across the transmission line. The rate of change of $v_{transient}$ is compared with the threshold $\triangle v_{Thres}$, if the compared value is less than

the threshold, a fault has occurred, is given in (4.12);

$$\frac{\triangle v_{transient}}{\triangle t} < \frac{\triangle v_{Thres}}{\triangle t} \tag{4.12}$$

The measurements were sampled at $f_s$= 10kHz, a typical sampling frequency used for dc system protection [69]. For real field measurements a certain quantity of noise and distortion appears on the signal. The signals are usually over-sampled by a factor $k$ that helps to reduce the noise distribution. Analyzing the rate of change of the current and voltage transients at the terminals, the fault can be quickly detected, leading to rapid isolation of the faulted transmission line from non-faulted segments without the use of a means of communication.

## 4.6 Fault Detection

As discussed in Section 4.4, the premise of detection is derived from the detection of the travelling waves at the onset of a fault in the system. Since the travelling waves travel at almost the speed of light, the change of current and voltage directions provides us with a fast and accurate dc fault detection in a radial MTdc systems. The voltage and current are updated at $\triangle t$ interval. As seen in Table 4.2, the voltage and current transients are complimentary to each other under an internal fault.

Terminals belonging to the unfaulted transmission line segment also see complimentary voltage and current changes, but to ensure a fail-safe operation, the change of current and voltage transients are monitored for a fixed time window. This step is only carried out if the previous criterion is met. This prevents any unnecessary breaker operations when normal power reversal operations are performed.

The algorithm has shown robustness under various sensitivity analysis, including change of fault impedance and fault locations along the transmission line. The continuous monitoring of $dv/dt$ or $di/dt$, as suggested in [70] is not performed to avoid misoperation of the breakers under conditions of load changes or power reversals.

As shown in (4.10) and (4.12), the rate of change of current transient and voltage transient respectively are compared against their respective threshold. If the change is initiated due to load variations or power reversals, the $I_{Thres}$ or $V_{Thres}$ is not reached and the fault detection algorithm does not trigger the breakers. The limit for the threshold was selected from a range of simulation experiments performed and it was maintained for the varying conditions and locations of fault as discussed in Section 4.7.3. Algorithm 2 discusses the proposed algorithm for fault detection and breaker operation.

## 4.7 Simulation and Results

For simplification, the entire system has been divided into several protection zones. As shown in Figure 4.2, the breakers are placed based on the zones of protection.

For hybrid breakers 1 and 2, zone B is their area of internal protection, and any fault beyond it is external to them. Similarly, for hybrid breakers 3 and 4, zone D is their area of internal protection, and any faults beyond it is external.

The following subsections elaborates the discussion of the proposed algorithm on a three terminal MTdc system described in Section 4.3.

### 4.7.1 Internal Faults

Faults created within the vicinity of zone B and zone D are internal faults to hybrid breaker pairs 1, 2 and 3, 4 respectively. A fault is simulated at $t = 2.5$ s on dc transmission line 1 (zone B), 100km from MMC 1 with a fault resistance of $R_f = 10\Omega$, within the protection vicinity of dcCB 1 and 2. The local measurement units placed at the terminals pick up the instantaneous change in both voltage and current directions on arrival of the traveling waves, as elaborated in Table 4.2. The breakers receiving the opposite directional changes of voltage and current transients, they are put on an enable high state. From Table 4.2, it can be seen that dcCB 1, 2 and 4 receive the enable high state. The rate of change of current and voltage transients are measured

**Algorithm 2:** Fault isolation using local measurement

Sampling Frequency ($f_s$) = 10 kHz; $\triangle$t = 0.1 ms;
At $T = 0$:
$I_{pre} = 0$; $V_{pre} = 0$;
Measure and store $I$ and $V$ at every $\triangle$t;
$Status_{Enable} = 0$; $Breaker_{State} = 1$ (Closed);
**while** *True* **do**
    Sample $I$ and $V$ at $\triangle t$;
    $I_{check}$ = $I$ - $I_{pre}$;
    $V_{check}$ = $V$ - $V_{pre}$;
    Assign I and V as $I_{pre}$ and $V_{pre}$ for next time step;
    $I_{pre} = I$;
    $V_{pre} = V$;
    **if** *($I_{check} > 0$ && $V_{check} < 0$) ||*
    *($I_{check} < 0$ && $V_{check} > 0$)* **then**
        $Status_{Enable} = 1$
    **else**
        $Status_{Enable} = 0$
    **end**
    **if** $Status_{Enable} = 1$ **then**
        Monitor $I_{check}$ and $V_{check}$ for a time window
    **else**
        **Continue**;
    **end**
    **if** $I_{rate} > I_{Thres}$ && $V_{rate} < V_{Thres}$ **then**
        **Fault Detected**;
        $Breaker_{State} = 0$ (Open);
        **Break**; Trip command sent to the breaker;
    **else**
        **Continue**;
    **end**
**end**

across the three devices, this operation is not performed throughout the course of operation as it might lead to erroneous detection of faults. The $di_{transient}/dt$ change for dcCB 1 and 2 reach their threshold. Similarly, the $dv_{transient}/dt$ is also compared against its threshold. When both conditions are satisfied as defined by (4.10) and (4.12), a trip command is sent to the concerned breakers. The relays implemented in this design has a directional sense and measurements leaving the terminals are considered as positive.

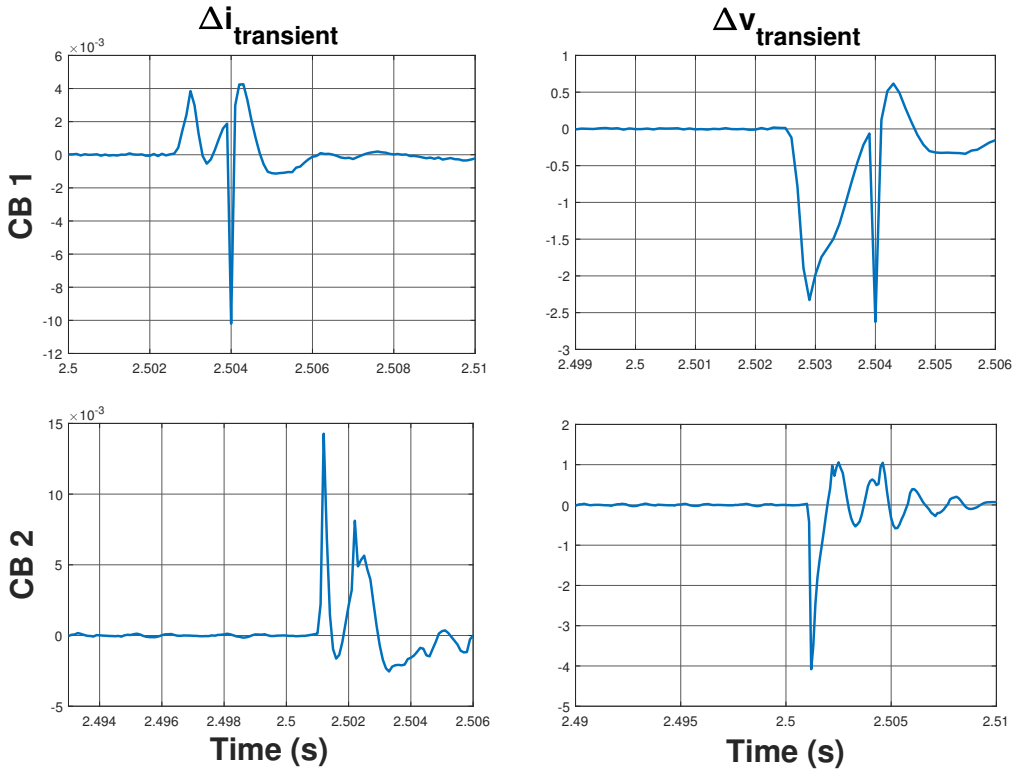
The load commutation switch instantly operates and the current begins to recede through the ultra-fast disconnector into the main breaker. After the ultra-fast disconnector senses zero current, it is turned off, and finally the main breaker is disconnected with the final interruption occurring at the energy absorption branch.

Figure 4.5, shows the opposite polarity of the initial arrival of the current and voltage traveling waves at circuit breakers 1 and 2. whereas similar polarity is seen for initial current and voltage waves in breaker 3, during fault in dc transmission line 1. The operational status of the hybrid breakers are shown in Figure 4.6.

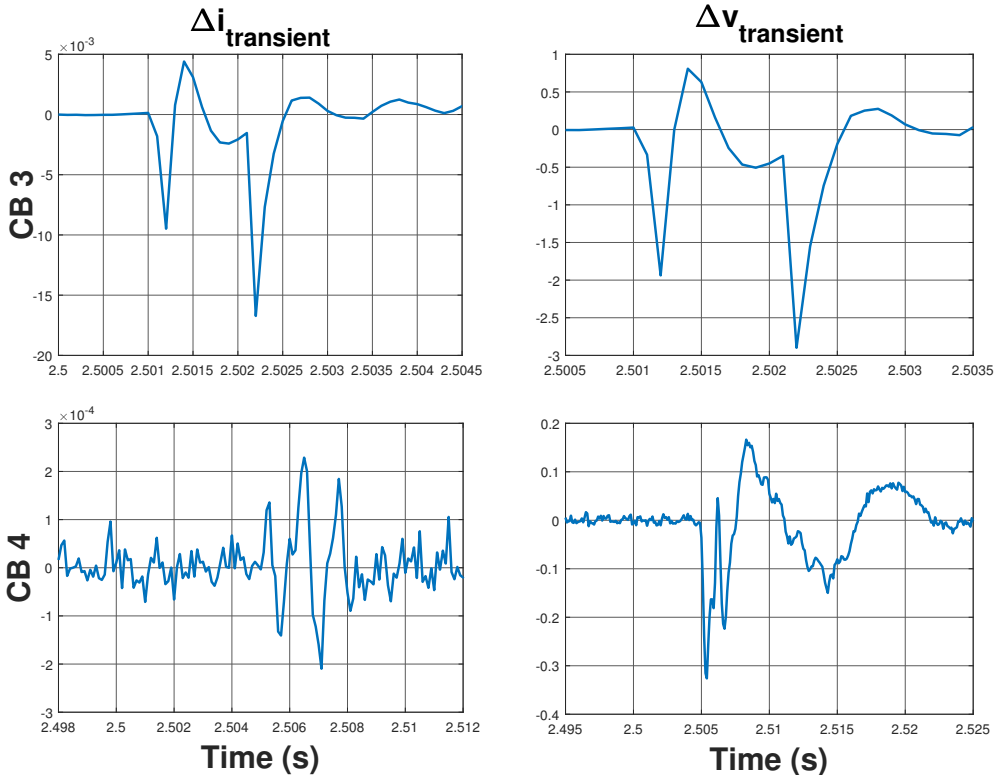
Similarly, a fault is simulated in dc transmission line 2 (zone D), 100 km from MMC 3, with a fault resistance $R_f = 10\Omega$, within the protection vicinity of dcCB 3 and 4. An opposite polarity of $i_{transient}$ and $v_{transient}$ is observed at dcCB 3 and 4. Figure. 4.8, shows polarity at arrival of $i_{transient}$ and $v_{transient}$ at dcCB 1, 2, 3 and 4. The arrival of $i_{transient}$ and $v_{transient}$ at dcCB 2 does not show opposite polarities, preventing the breaker from operating. The corresponding breaker states are also shown in Figure 4.9. The isolation of the faulted dc transmission line 2 is shown in Figure 4.10.

### 4.7.2 External Faults

Faults occurring beyond the protection region of dcCB 1, 2, 3 and 4 are deemed external. Faults were created on the ac transmission lines and operation of the hybrid breakers were verified. To verify the performance of the algorithm, a 3-phase to




(a) Arrival of current and voltage transients in dc cable 1




(b) Arrival of current and voltage transients in dc cable 2

Figure 4.5: Arrival of $i_{transient}$ and $v_{transient}$ under fault in dc transmission line 1

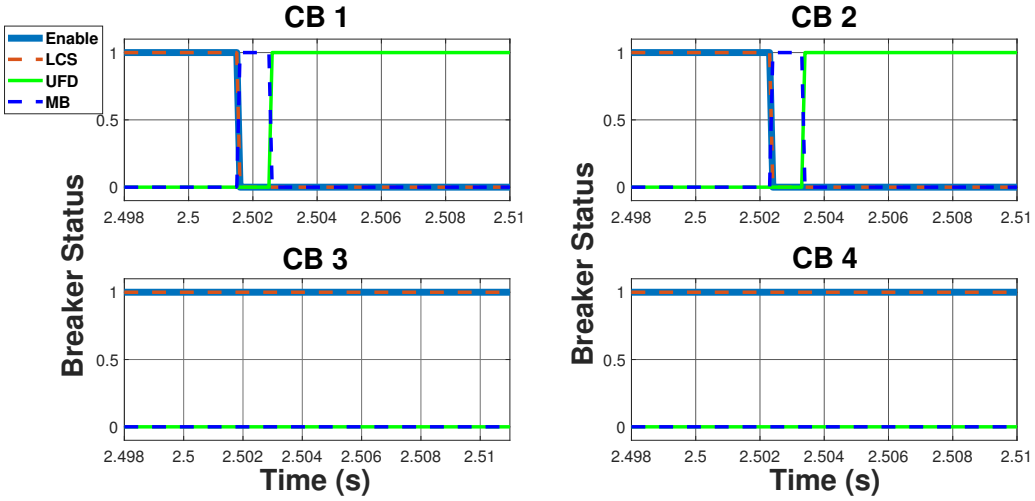



Figure 4.6: Breaker states under fault in dc transmission line 1 in t=2.5s

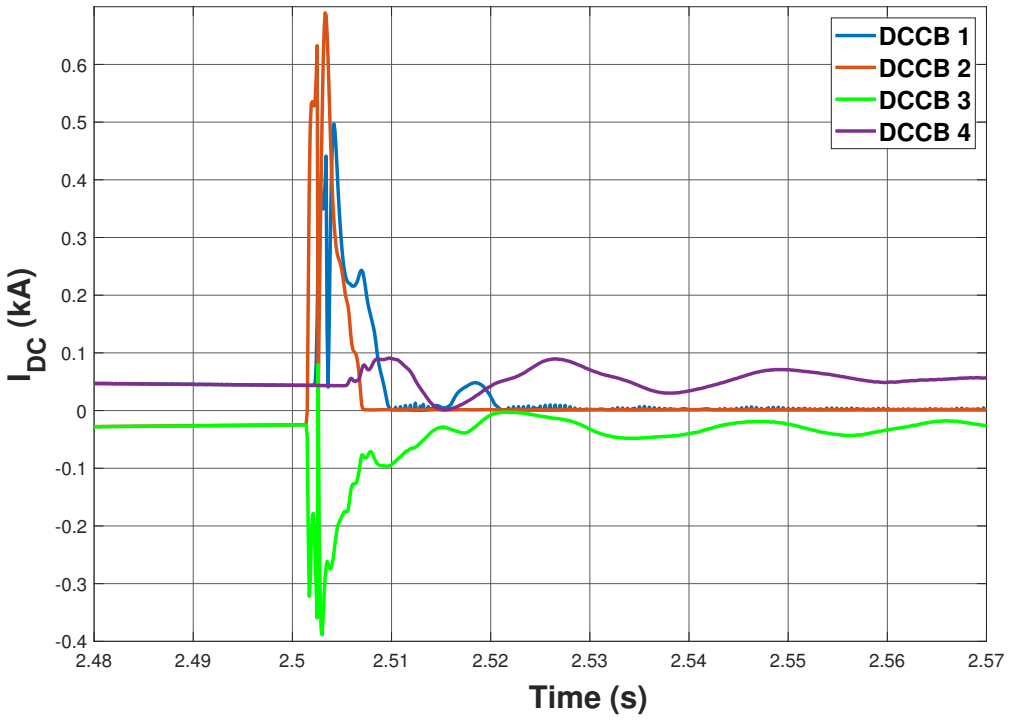
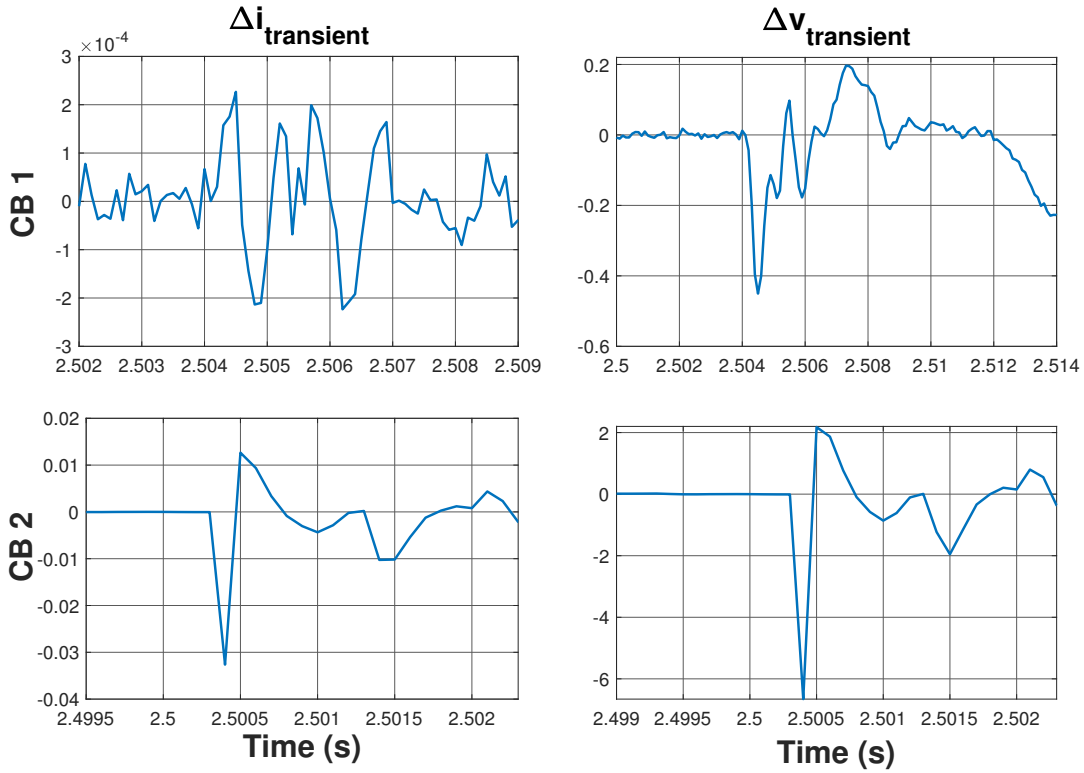
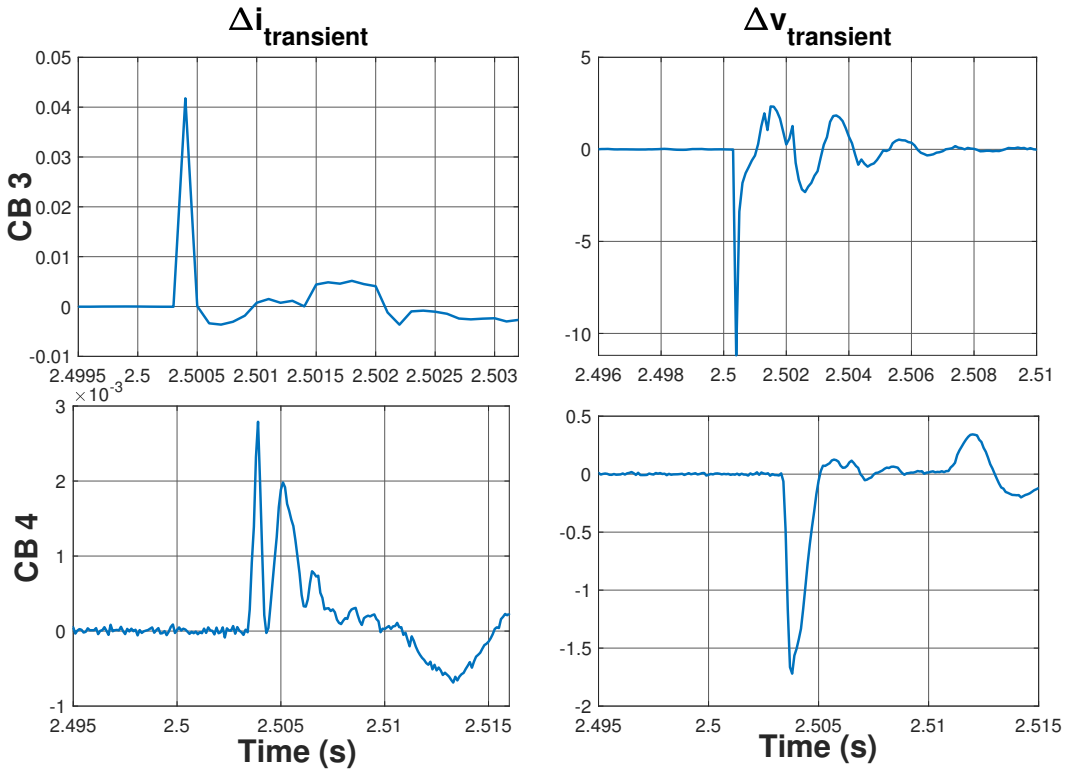



Figure 4.7: Current as measured at each terminal breaker location under fault in dc transmission line 1




(a) Arrival of current and voltage transients in dc transmission line 1




(b) Arrival of current and voltage transients in dc transmission line 2

Figure 4.8: Arrival of $i_{transient}$ and $v_{transient}$ under fault in dc transmission line 2

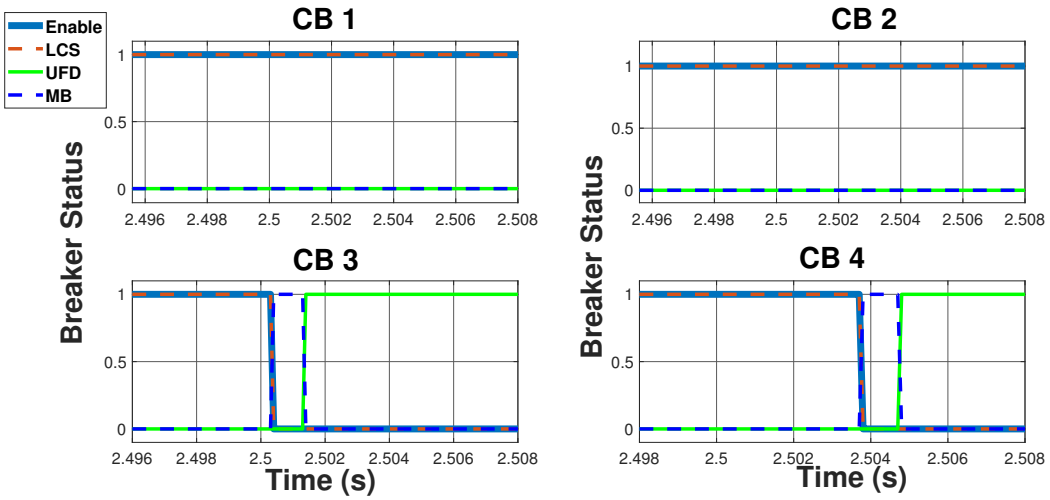



Figure 4.9: Breaker states under fault in dc transmission line 2 at t=2.5s

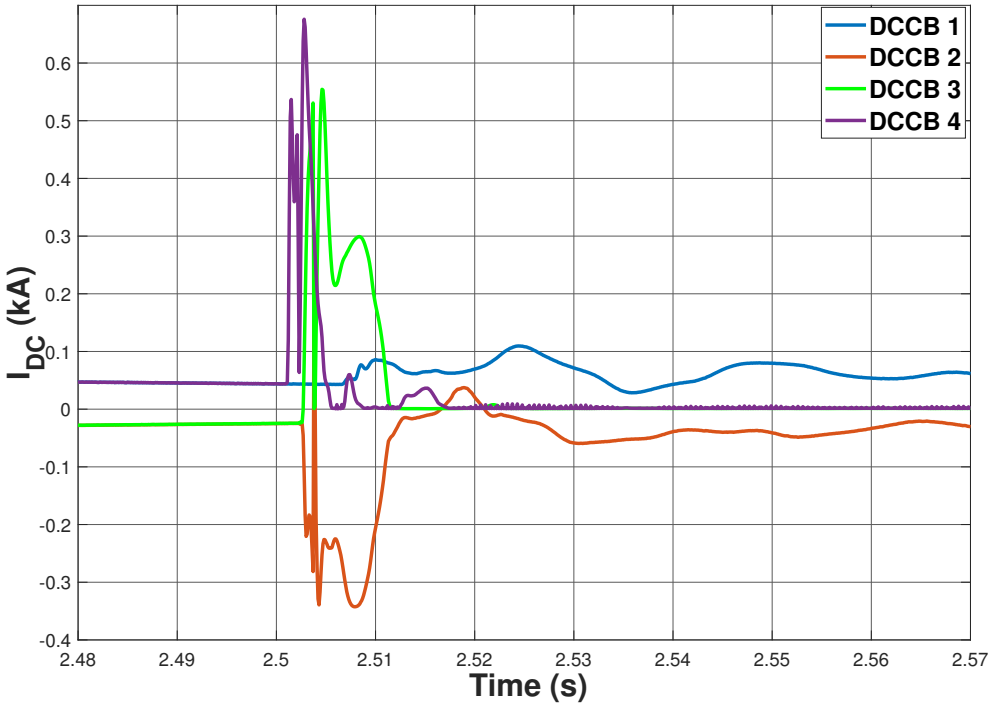



Figure 4.10: Current as measured at each terminal breaker location under fault in dc transmission line 2

ground fault was simulated at ac transmission line 2 (zone C), 70 km from ac grid 2, with a fault resistance $R_f = 0.01\Omega$, the operational states for the hybrid dcCB are shown in Figure 4.11.

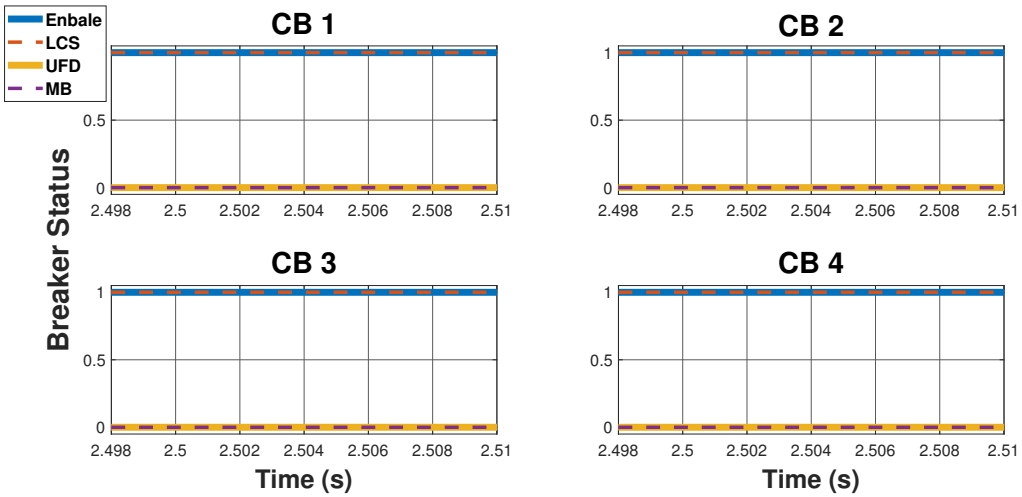



Figure 4.11: Breaker states under external fault in ac transmission line 2 at t=2.5s

### 4.7.3 Sensitivity Analysis

To demonstrate the robustness of the algorithm to measurement noise, fault impedance, fault resistance etc. various test cases were performed with faults applied across the length of the cable as shown in Table 4.3.

The sensitivity of the proposed algorithm was also tested by varying the limiting inductance at each terminal between 100 mH to 200 mH in steps of 20 mH. The other operating conditions were maintained the same as in the previous study. The performance of Algorithm 2 to the aforementioned sensitivity conditions were simulated and the operational states for the dc breakers were examined. The results demonstrated in Table 4.4, show the robustness of the fault detection algorithm to varying current limiting reactances. The breakers on the faulted transmission line operated correctly, while the other breakers did not detect a fault.

Changes in power transfer were performed at certain times to check if any false operations were identified. The converter output was increased to 1 GW, and the breakers did not operate under such conditions. Measurement noise was added to both the current and voltage readings to emulate real-field measurements. A comparison of the speed of detection proposed by some other non-communication based methods

is compared with the proposed method in Table 4.5. It can be seen that the proposed method is able to detect faults at similar time intervals and also addressing the drawbacks of the other methods. Our main objective to detect dc faults is dependent on parameters like reliability, robustness and speed. A trade-off needs to be achieved to achieve a proper fault detection. Keeping the detection speed similar to other proposed methods. this method helps to provide more reliability and robustness to dc fault detections.

Table 4.3: System performance under varying conditions in the test system

| **Location of Fault** | **Distance** | **Breakers Operated** | **Fault Detection Time** | **Breaker Operation Time** |
|---|---|---|---|---|
| From MMC 1 (dc transmission line 1) | 100 km | dcCB1, dcCB2 | 0.04 ms, 3.7 ms | 8 ms |
| | 300 km | dcCB1, dcCB2 | 1.2 ms, 2.7 ms | 7 ms |
| | 400 km | dcCB1, dcCB2 | 1.6 ms, 2.3 ms | 8 ms |
| | 800 km | dcCB1, dcCB2 | 3.4 ms 0.7 ms | 9 ms |
| From MMC 3 (dc transmission line 2) | 100 km | dcCB3, dcCB4 | 0.04 ms, 3.8 ms | 7 ms |
| | 300 km | dcCB3, dcCB4 | 1.2 ms 3.0 ms | 8 ms |
| | 450 km | dcCB3, dcCB4 | 1.7 ms, 2.3 ms | 7 ms |
| | 800 km | dcCB3, dcCB4 | 3.2 ms, 0.8 ms | 9 ms |
| From ac grid 1 (ac transmission line 1) | 30 km | None | External | N/A |
| | 70 km | None | External | N/A |
| From ac grid 2 (ac transmission line 2) | 30 km | None | External | N/A |
| | 70 km | None | External | N/A |
| | 100 km | None | External | N/A |
| From ac grid 3 (ac transmission line 3) | 30 km | None | External | N/A |
| | 70 km | None | External | N/A |

Table 4.4: Sensitivity analysis of the algorithm to current limiting inductance

| **Fault Location** | **Fault Detected at** | | | |
|---|---|---|---|---|
| | **dcCB 1** | **dcCB 2** | **dcCB 3** | **dcCB 4** |
| dc transmission line 1 700 km from MMC 1 $L_{Limit}$ = 200 mH | 2.9 ms | 1.1 ms | Not Identified | Not Identified |
| dc transmission line 1 700 km from MMC 1 $L_{Limit}$ = 180 mH | 2.8 ms | 1.2 ms | Not Identified | Not Identified |
| dc transmission line 2 200 km from MMC 2 $L_{Limit}$ = 160 mH | Not Identified | Not Identified | 0.8 ms | 3.4 ms |
| dc transmission line 2 200 km from MMC 2 $L_{Limit}$ = 120 mH | Not Identified | Not Identified | 2.7 ms | 1.2 ms |

Table 4.5: Speed of detection compared to other non-communication methods

| **Attribute** | **Proposed Method** | **Other Methods** |
|---|---|---|
| Speed | Between 0.04 ms to 3.7 ms | In [21], between 0.06 ms to 3.48 ms |
| | | In [22], between 0.09 ms to 3.25 ms |

## 4.8 Conclusion

In this work a novel communication less fault detection approach has been proposed. The method utilizes the principle of direction change of voltage and current transients from the fault-induced traveling waves. The rate of change of the transient voltage and current component in the fault are checked against their respective thresholds before a decision to operate the breaker is made. This method clearly distinguishes a faulted segment from a non-faulted segment in a radial MTdc transmission network.

The non-communication based method was verified against various conditions in the grid, such as faults in the ac and dc segments. It was also evaluated under varying current limiting inductance of the dcCB. The design of the HVdc transmission system

Table 4.6: Comparison of proposed algorithm with existing algorithms

| **Attribute** | **Proposed Algorithm** | **Other Methods** |
|---|---|---|
| Communication | Local measurements do not require communication | [9], [12] and [14] require communication |
| Sensitivity | Not sensitive to changes in limiting inductance | [11] and [14] are sensitive to the limiting inductance |
| Robustness | Robust to measurement noise | [9], [14] are sensitive to measurement noise |
| Speed | Detection is faster | [8], [10] and [12] are delayed due to communication networks |
| Cost | Low cost due to no telecommunication channels | Communication channels are costly to implement and maintain |

and operating principles have been discussed in this Chapter along with the hybrid dc breaker design has been utilized for fault isolation. A summary of the comparison between the proposed simulation algorithm and the existing algorithms is presented in Table 5.1.

Fault location methods by analyzing current and voltage transients have been suggested with the application of CWT or DWT. These methods are dependent on the time of arrival of the voltage and current transients, that can be accurately determined with devices having a high sampling frequency. The time of arrival of the transients at both ends require time synchronized devices requiring communication. Chapter 5 discusses a non-intrusive method for fault location in MTdc networks utilizing the transmission line discharge.

# CHAPTER 5: FAULT LOCATION USING NATURAL FREQUENCY OF RESPONSE

## 5.1 Overview

This Chapter discusses a novel fault location approach using double ended measurement. The natural dissipation of the circuit parameters are considered for fault location. A relationship between the natural frequency of oscillation of the transmission line current and fault location has been illustrated in this Chapter. The hybrid dcCB interrupts the fault current and the line current attenuates under the absence of any driving voltage source. The line capacitance discharges into the fault at a damping frequency and rate of attenuation. Utilizing this information, the fault location in a MTdc network can be predicted.

The electric grid is undergoing technological transformation as result of increasing environmental awareness to reduce carbon emission. The push for more renewable energy integration with distributed resources like solar, wind, tidal energy etc. where the generation is located at a distance far away from their load centers, HVdc transmission has taken prominence over HVac transmission [8]. Large power transfer capability, lower power losses and flexible control has made HVdc a popular choice [5].

Such advantages can be achieved through the implementation of VSC HVdc networks [71]. HVdc networks have also been found to be beneficial in interlinking multiple ac asynchronous generation systems with the help of underground cables and over head transmission cables. The MMC has emerged as a popular choice for VSC HVdc systems, due to certain salient features including (1) absence of large dc link capacitors; (2) better scalability; (3) higher operational efficiency etc. [52].

Given the remote locations of the HVdc lines it is a challenge to detect faults that

happen causing instability to the entire grid. Rapid isolation of fault is essential as it might cause indelible damage to the converter stations and the network infrastructure [7]. Extensive research has been carried out for ac transmission systems for fault location, but such techniques are not always applicable to HVdc systems [72].

Traditional ac systems utilize phasors and voltage angle information from Phasor Measurement Unit (PMU) [73] for fault location. Lack of phasor information and frequency data makes it difficult to use those methods. Multiple techniques have been used for identification of dc fault locations. They can be broadly classified in two categories (1) single-ended measurement and (2) double-ended measurement [33]. Current approaches mostly revolve around about the use of time-domain based fault-location algorithms [74], [75]. The high frequency fault transients contain information about the fault and its characteristics [69]. These traveling wave-based methods have gained prominence due to the presence of time-synchronised GPS devices. These devices are expensive, and their accuracy is dependent on the ability to capture the arrival wave peaks [76]. Traveling waves are not affected by fault resistance, system parameters, etc. [77]. Single ended measurements are cheaper but they tend to provide inaccurate results as the devices must have the capability to detect the reflected peak [78]. The reflected surge waves are usually weak, making it difficult to detect. The wave speed has an influence on the fault location accuracy. The surge propagation of the waves are dependent on the line parameters, controlling the accuracy of the results [79]. Modern methods also involve the use of digital signal processing methods requiring high sampling frequency to achieve the desired accuracy [69]. Simultaneous time-frequency based methods like wavelet transform has been widely used for fault location. DWT and CWT methods have been implemented. CWT tends to provide better resolution as compared to DWT. CWT involves a smooth shift of the mother wavelet over the time-domain, whereas in DWT the mother wavelet is shifted using a dyadic pattern over time [69], [80]. Active fault location

detection techniques using external injection of voltage using a Power Probe Unit (PPU) has been suggested in [56] or as a pre-charged capacitor connected to a circuit breaker [81]. The external oscillation circuit injects a signal whose under-damped oscillation and attenuation is used to locate the fault. The requirement of an external probe unit or a pre-charged capacitor has been suggested for Low Voltage direct current (LVdc) networks [82].

Use of artificial intelligence (AI) to locate faults and also improve its accuracy has been previously suggested in [83]. Measured voltages and currents are utilized as inputs to the neural network. The corresponding features are utilized for fault location on transmission systems. Other methods using statistical data classifications like space vector machine (SVM) have been studied in [84] for fault location in transmission lines. The data driven methods for fault location requires a training dataset and the neural network has to be retrained for every new dataset that requires significant time and effort and is computationally burdensome.

## 5.2 Contribution

Current methods for fault location in MTdc networks require the application and installation of complex time-synchronized GPS units that are capable to capture the peaks of the incident and the reflected traveling waves at the onset of the fault. Other suggested methods require an active injection of current or voltage signals for fault detection.These methods are difficult to achieve for large HVdc networks, as discharging a pre-charged external capacitance into the network can cause over voltage problem and can damage the infrastructure.

In this Chapter, a passive method for fault location using the natural attenuation of the transmission line current after the isolation of the fault using hybrid dcCB has been suggested. After fault isolation, the transmission line capacitance discharges into the fault through the line inductance and resistance into the fault. Under the absence of any active voltage source the damped response of the transmission line

Table 5.1: System parameters

| | **Parameters** | **Value** |
|---|---|---|
| ac side | Voltage (L-L RMS) | 333 kV |
| | Length of transmission line 1 & 3 | 100 km |
| | Length of transmission line 2 | 150 km |
| | System Frequency | 60 Hz |
| | Transmission line resistance | 0.03206 Ω/km |
| dc side | Voltage (L-L) | 640 kV |
| | Length of transmission line | 1000 km |
| | Transmission line resistance | 0.03206 Ω/km |
| | Transmission line inductance | 0.828 mH/m |
| | Transmission line capacitance | 0.305 $\mu$F/m |
| | MMC capacity | 1 GW |

current provides us with the rate of attenuation of the fault current. This information along with the damping frequency of the transmission line current calculated using fast Fourier transform (FFT) analysis has been suggested in the Chapter for fault location. The attenuation constant of the damped transmission line current is calculated using Linear Regression (LR) method [85]. This Chapter also investigates fault isolation using a hybrid dcCB and then the natural damping of the transmission line current helps to provide the fault location. A double ended local measurement is utilized for better accuracy in fault location. The passive method of fault location is achieved without any signal injection or external circuits, thereby reducing costs and complexities associated with it. The HVdc model used for this analysis has been modeled similar to Section 4.3. The detailed system parameters are listed in Table 5.1.

## 5.3 Fault Location Methodology

Fault detection is a challenge in MTdc systems and various works have been reported for the same in [69], [21], [22]. Once a fault has been detected the hybrid dcCB's operate to isolate the faulted section of the network. The other non-faulted sections remain operational. The entire MTdc network has been divided into multiple protection zones as shown in Figure 4.2. For a hybrid dcCB, faults occurring inter-

nally are in their zones of protection. Zone B and zone D are the internal zones of protection for dcCB 1 and 2, and dcCB 3 and 4 respectively. Once the fault current is interrupted, the stored energy in the transmission line capacitance discharges into the fault. The stored energy of the transmission line capacitance at a certain distance from the terminals is finite. Under the absence of any external voltage source the transmission line current $i_{cable}$ discharges into the fault over time. The rest of the isolated network up to the fault point can be considered a $RLC$ oscillating circuit, with the current resonating similarly as an $LC$ circuit and presence of the resistance decays the oscillations over a period of time. By analyzing the discharging transmission line current $i_{cable}(t)$ the fault location in the transmission line can be estimated.

### 5.3.1 Faulted Section Formulation

Once the faulted section of the cable is isolated, the remaining portion of the cable beyond the hybrid dcCB upto the fault point can be represented by an equivalent $RLC$ circuit as shown in Figure 5.1. Differential equations governing the state of the circuit can be calculated from KVL, and the constitutive equations for the cable indutance, resistance and stored capacitance can be given as (5.1);

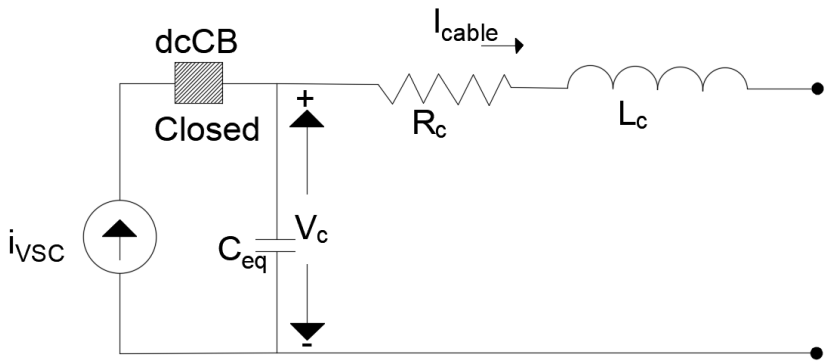
$$V_R + V_L + V_C = V(t) \tag{5.1}$$

where $V_R$, $V_L$ and $V_C$ are the voltages across the transmission line resistance, inductance and capacitance respectively. $V(t)$ is a time-varying voltage source. After the fault isolation in the absence of any time-varying voltage source $V(t) \to 0$. Substituting, $V_R = R_{tot} i_{cable}(t)$, $V_L = L_{tot} \frac{\mathrm{d}i_{cable}(t)}{\mathrm{d}t}$ and $V_C = \frac{1}{C}\int_0^t i_{cable}(t)dt$ in (5.1), is given by (5.2);

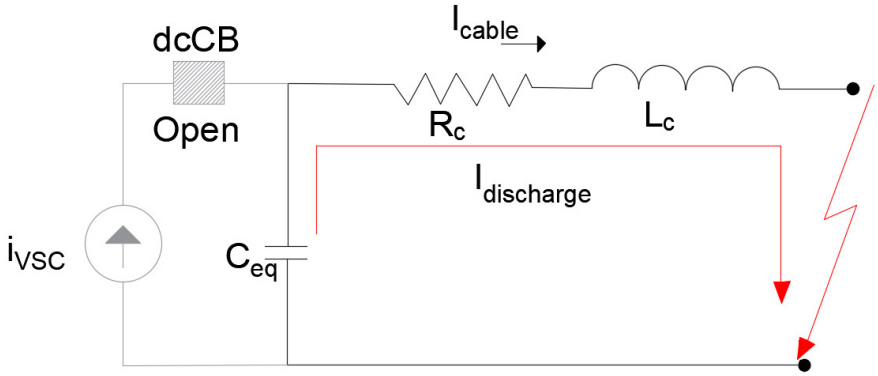
$$R_{tot} i_{cable}(t) + L_{tot} \frac{\mathrm{d}i_{cable}(t)}{\mathrm{d}t} + \frac{1}{C}\int_0^t i_{cable}(t)dt = 0 \tag{5.2}$$

Differentiating (5.2) with time, to get a second order differential equation (5.3);

$$\frac{\mathrm{d}^2 i_{cable}(t)}{\mathrm{d}t^2} + \frac{R_{tot}}{L_{tot}} \frac{\mathrm{d}i_{cable}(t)}{\mathrm{d}t} + \frac{1}{L_{tot}C} i_{cable}(t) = 0 \tag{5.3}$$




(a) Normal operation




(b) After dcCB operation

Figure 5.1: MMC converter equivalent circuit

Now $R_{tot}$ is the equivalent resistance upto the fault path including the transmission line resistance $R_{cable}$ and the fault resistance $R_{fault}$. $L_{tot}$ is the net overhead cable inductance $L_{cable}$ and $C$ is the equivalent capacitance from the point of consideration.

A more general solution to (5.3), can be given as (5.4);

$$\frac{\mathrm{d}^2 i_{cable}(t)}{\mathrm{d}t^2} + 2\alpha \frac{\mathrm{d}i_{cable}(t)}{\mathrm{d}t} + \omega_0^2 i_{cable}(t) = 0 \tag{5.4}$$

where $\omega_0$ is the natural frequency of oscillation, $\alpha$ is the rate of attenuation and

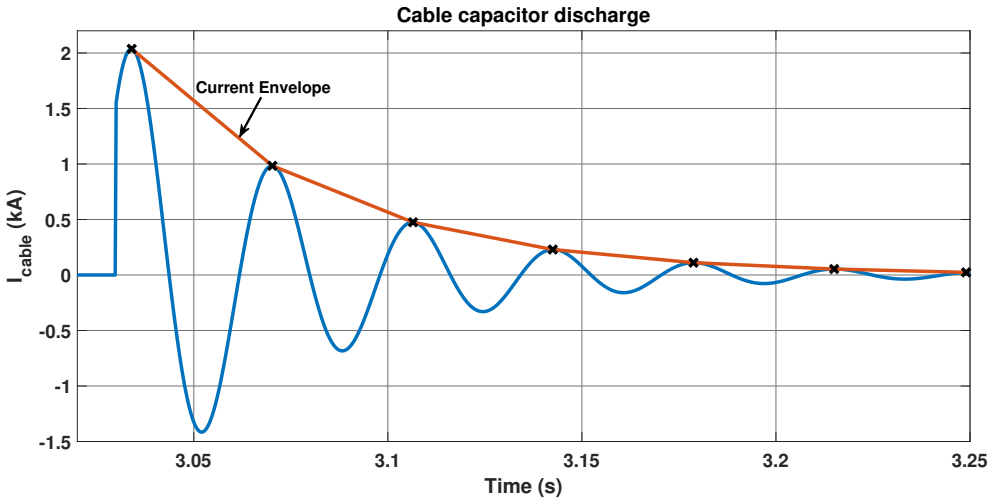



Figure 5.2: Capacitor discharge profile

they are represented as,

$$\alpha = \frac{R_{tot}}{2L_{tot}};\ \omega_0 = \frac{1}{\sqrt{L_{tot}C}}$$

. As stated previously under the absence of a driving voltage source other than the discharging transmission line capacitance, the solution for the transmission line current $i_{cable}$ can be given as an under-damped response for a $RLC$ circuit. The general solution for the under-damped response is given as (5.5);

$$i_{cable}(t) = D_1 e^{-\alpha t} cos(\omega_d t) + D_2 e^{-\alpha t} sin(\omega_d t) \tag{5.5}$$

where $\omega_d$ is the damping frequency of the capacitor and $\alpha$ is the rate at of attenuation of the stored energy of the capacitor. An example of the capacitor discharge current after the dcCB has operated is shown in Figure 5.2.

### 5.3.2 Attenuation Constant

The capacitor discharge upto the faulted point is an under-damped response. The attenuation constant can be calculated from the discharge current by considering and envelope of the oscillating signal. The measured under-damped oscillating current is sampled at regular intervals to obtain peaks of the signal. The envelope of the

under-damped oscillating current can be represented as (5.6);

$$I_{0cable}(t_n) = I_{0peak}(t_n)e^{-\alpha t_n} \tag{5.6}$$

The above equation can also be represented as (5.7);

$$ln(I_{0cable}(t_n)) = ln(I_{0peak}(t_n)) - \alpha t_n \tag{5.7}$$

The above equation takes the form of a straight line, as given by (5.8);

$$\begin{gathered} y = mx + c \\ y = ln(I_{0cable}(t)); m = -\alpha; c = ln(I_{0peak}(t)) \end{gathered} \tag{5.8}$$

Since (5.7) can be represented as (5.8), a linear approach can be considered to compute the slope of the line i.e. $\alpha$. From the data obtained by sampling $i_{cable}$ at regular intervals the unknown model parameter can be estimated. For a given set of observations the model takes the form (5.9);

$$\begin{gathered} y_1 = c_0 + m_1 x_1 \\ y_2 = c_0 + m_2 x_2 \\ y_3 = c_0 + m_3 x_3 \\ .... \\ y_i = c_0 + m_i x_i \\ where, i = 1, 2, ..., n \end{gathered} \tag{5.9}$$

The equivalent matrix form of (5.9), can be given as (5.10);

$$y = Ax^T$$

$$y = \begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ .. \\ y_i \end{bmatrix} ; x^T = \begin{bmatrix} 1 & x_1 \\ 1 & x_2 \\ 1 & x_3 \\ .. & .. \\ 1 & x_i \end{bmatrix} ; A = \begin{bmatrix} c \\ m \end{bmatrix} \tag{5.10}$$

Here $y$ is is the set of observed variables at different time-steps, $x$ is the set of exogenous or input variables. Solving (5.10), to calculate the attenuation $\alpha$ from the entries of matrix $A$.

### 5.3.3 Fast Fourier Transform

Using Fourier analysis, a signal a given sequence in time can be transformed into its respective frequency components using discrete Fourier transform (DFT) [18]. FFT is useful to perform the DFT of a sequence. FFT performs the computation of the DFT matrix as a product of sparse factors. The DFT for such a sequence can be given as (5.11);

$$X[k] = \sum_{n=0}^{N-1} x[n] e^{-j2\pi kn/N} \tag{5.11}$$

where $N$ is the length of the signal. To calculate the damping frequency of the capacitor discharge $\omega_d$, performing FFT analysis to determine the dominant frequency of the under-damped oscillating transmission line current. As stated earlier, the transmission line current $i_{cable}(t)$ decays at a frequency of $\omega_d$ as shown in (5.5). This damped oscillating frequency can be calculated as (5.12);

$$\omega_d^2 = \sqrt{\omega_0^2 - \alpha^2} \tag{5.12}$$

The damping frequency can be given as a factor of the damping factor $\zeta$ as (5.13);

$$\omega_d^2 = \omega_0 \sqrt{1 - \zeta^2} \tag{5.13}$$

where,

$$\zeta = \frac{\alpha}{\omega_0} = \frac{R_{tot}}{2} \sqrt{\frac{C}{L_{tot}}}$$

### 5.3.4 Fault Location Calculation

From the PSCAD transmission line modelling parameters, the per unit (p.u) line inductance ($L_k$), resistance ($R_k$) and the per unit capacitance ($C_k$) from the point of measurement can be calculated. The natural frequency of oscillation $\omega_0$ of the current discharge through the transmission line can be calculated as (5.14);

$$\omega_0^2 = \omega_d^2 + \alpha^2 \tag{5.14}$$

Thus, fault location $d_{cal}$ can be calculated as (5.15);

$$d_{cal} = \frac{1}{(\omega_d^2 + \alpha^2) L_k C_k} \tag{5.15}$$

where, $L_{tot} = L_k d_{cal}$. To verify the robustness of the algorithm, faults are created at various length of the transmission line and the fault resistance is also varied between $0.01\Omega$ and $10\Omega$. The error % between the actual fault location and the measured location is given by $\epsilon$ (5.16);

$$\epsilon = \left| \frac{d_{act} - d_{cal}}{d_{act}} \right| \times 100\% \tag{5.16}$$

where, $d_{act}$ is the actual location of the fault in the transmission line and $d_{cal}$ is the calculated fault location using (5.15).

### 5.3.5 Proposed Algorithm

The following section discusses in brief the proposed algorithm to detect the fault location, shown in Algorithm 3.

Local measurements of currents and voltages are sampled at each location in real-time. At the onset of the fault, the traveling waves are detected that help to isolate the faulted section of the transmission line. The fault detection algorithm is robust to various changes of sensitivity and measurement noise. After the breakers operate the current recorder devices starts to monitor the overhead cable discharge current. The recorded current $i_{discharge}$ is sampled at every 2ms to determine the peaks of the current envelope $I_{0peak}$. A FFT analysis is also performed on $i_{discharge}$ to determine the damping frequency. Finally, the location of fault can be found using (5.15).

**Algorithm 3:** Fault location using transmission line current discharge

```
Sampling Frequency (f_s) = 10kHz; △t = 0.1ms;
Fault occurs at T = t_s;
At T = t_brk:
Hybrid dcCB operate at their respective zones to isolate the fault;
if Breaker_Status = 0 (Open) then
    Enable fault location algorithm;
    Measure and store i_cable at △t as i_discharge;
    Sample i_discharge at 2ms to calculate I_0peak from (5.6);
    Calculate α using LR method from (5.10);
    FFT of i_discharge to extract ω_d using (5.11);
    Calculate the location of fault using (5.15);
else
    Continue Normal operation;
end
```

## 5.4 Simulation Results

To verify the accuracy of the proposed algorithm the radial MTdc network shown in Figure 4.2 was designed in PSCAD/EMTDC. Varying simulation conditions like fault distances and fault resistances were performed on the 1000 km long dc section of the transmission line. As discussed previously the proposed method does not require

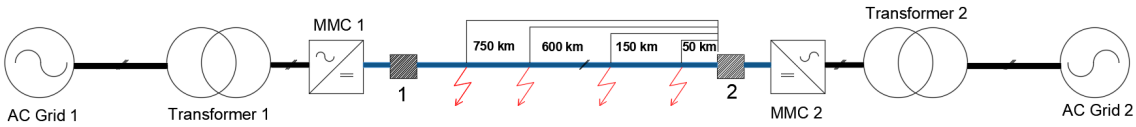



Figure 5.3: Fault locations

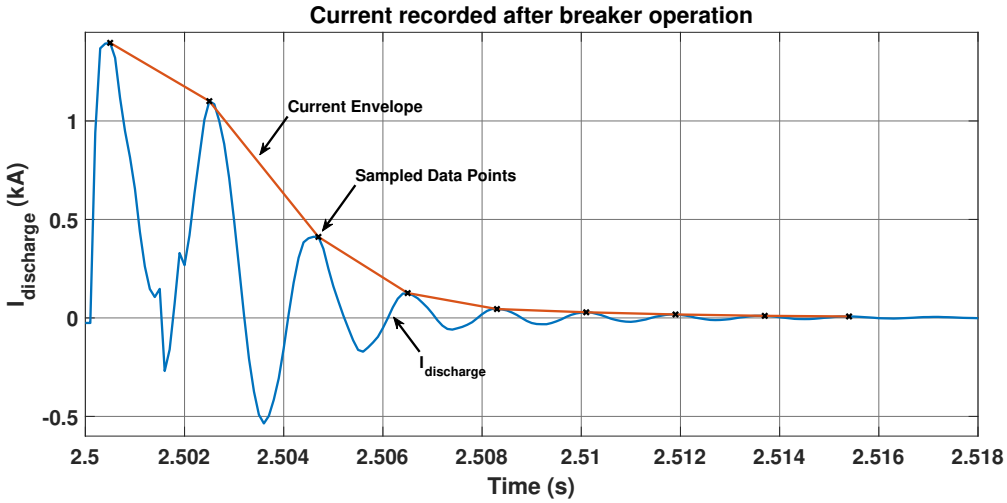



Figure 5.4: Recorded current discharge with current envelope

any external injection of current or voltage pulses into the network as proposed in [56], [81] and [82]. The fault detection algorithm detects the faults in the zone of internal protection as described in Section 5.3. The fault locations obtained by the proposed method was compared to the actual fault location and an error metric is calculated. A schematic for various fault locations is shown in Figure 5.3.

A fault was simulated on zone B, hybrid dcCB's 1 and 2 operated to isolate the fault. The actual location of the fault was 50 km from the recorder located at a distance from MMC 2. Figure 5.4 shows the sampled discharge current at the recorder location. An FFT analysis for the sampled current performed is shown in Figure 5.5. Using the sampled data points from the current envelope, to determine $\alpha$ from (5.10). Coefficient of determination that is used as a statistical measure for the performance of the regression model for the data, is found to be $R^2 = 0.9722$, indicating a high degree of linear relationship for the straight line regression model as explained in (5.8). Using the equations to calculate the actual fault distance is calculated to be

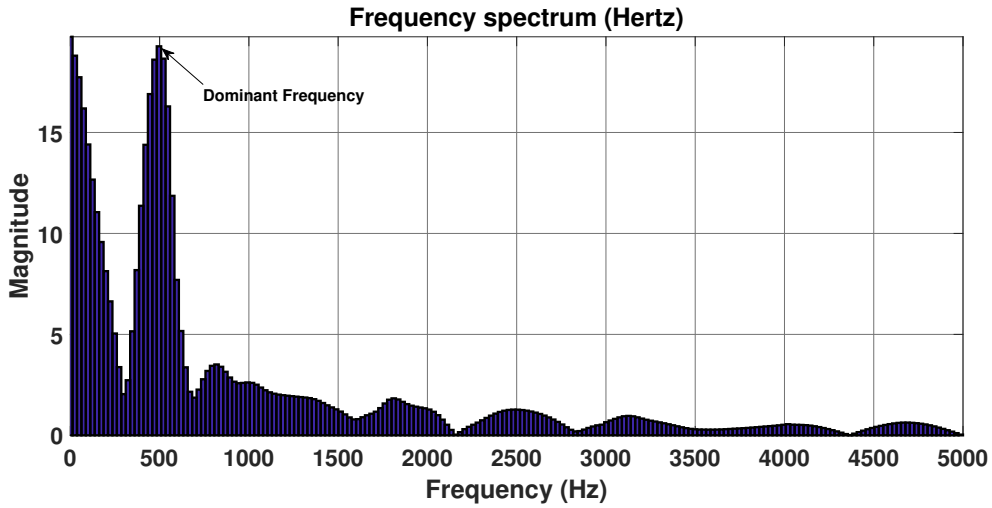



Figure 5.5: FFT analysis

Table 5.2: Fault distance estimation, without measurement noise

| $d_{act}(km)$ | $R_{fault}$ $(\Omega)$ | $\epsilon$ $(\%)$ | $R^2$ |
|---|---|---|---|
| 50 | 0.01 | 14 | 0.9722 |
| 150 | 0.01 | 9.33 | 0.9641 |
| 600 | 0.01 | 7.66 | 0.8399 |
| 750 | 0.01 | 13.33 | 0.9649 |
| 50 | 2 | 17.4 | 0.9796 |
| 150 | 2 | 10.67 | 0.9795 |
| 600 | 5 | 12.67 | 0.8045 |
| 750 | 5 | 10 | 0.9773 |
| 50 | 10 | 4 | 0.9821 |
| 150 | 10 | 11.2 | 0.9667 |
| 600 | 10 | 11.32 | 0.8145 |
| 750 | 10 | 9.33 | 0.9758 |

57 km. The predicted linear regression model is plotted against the measured data is shown in Figure 5.6.

Similar events of faults were performed across the transmission line as shown in Figure 5.3. Table 5.2 shows the various fault distance estimations, error and the coefficient of determination for the calculated regression model for $\alpha$.

Variations in fault resistance between $R_{fault} = 0.01\Omega$ to $10\Omega$, was performed. The fault locations were also varied and the algorithm was tested for faults in zone B and zone D.

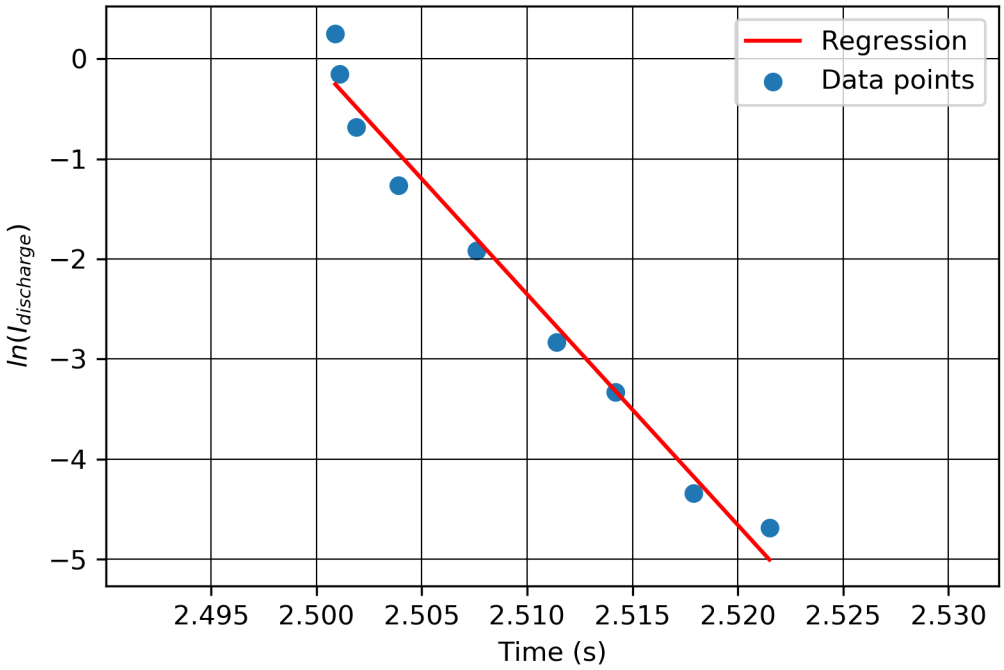



Figure 5.6: Linear regression model

Variation in error with changes in $R_{fault}$ and $d_{act}$ has been shown in Figure 5.7. From Table 5.2, it can be seen that the % error increases ever so slightly with the increment of $R_{fault}$, as the capacitor discharge attenuates at a higher rate due to the presence of a larger fault resistance. The frequency of attenuation is affected that causes the % error to increase slightly.

### 5.4.1 Measurement Noise

To verify the influence of the real field measurement noise on the fault location estimation, a Gaussian noise spectrum of signal noise ratio (SNR) 30dB was added to the measured data as suggested in [86]. Figure 5.8 shows a current discharge profile with added measurement noise. The fault location estimation is summarized in Table 5.3.

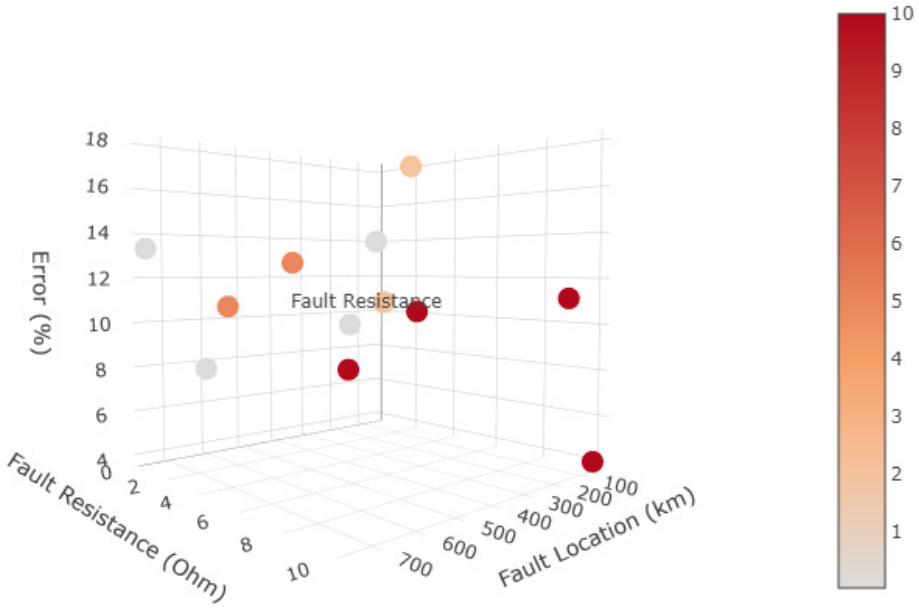



Figure 5.7: Variation of error with $R_{fault}$ and location

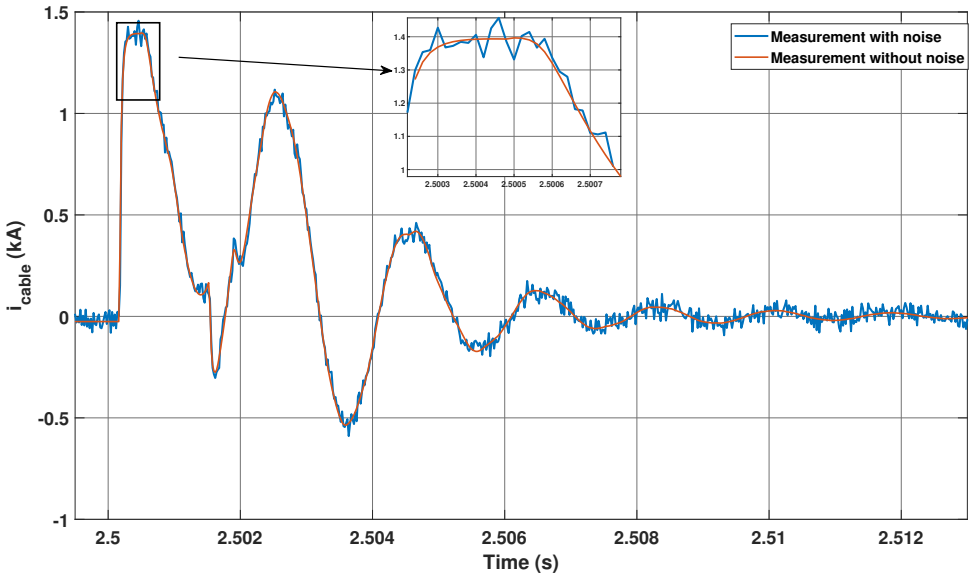



Figure 5.8: Current discharge considering measurement noise

Table 5.3: Fault distance estimation, with measurement noise

| $d_{act}(km)$ | $R_{fault}$ $(\Omega)$ | $\epsilon$ $(\%)$ | $R^2$ |
|---|---|---|---|
| 50 | 0.01 | 14.22 | 0.9712 |
| 150 | 0.01 | 9.32 | 0.9641 |
| 600 | 0.01 | 7.56 | 0.8399 |
| 750 | 0.01 | 13.3 | 0.9649 |
| 50 | 2 | 17.38 | 0.9796 |
| 150 | 2 | 10.65 | 0.9715 |
| 600 | 5 | 12.77 | 0.8040 |
| 750 | 5 | 10.28 | 0.9743 |
| 50 | 10 | 3.53 | 0.9832 |
| 150 | 10 | 11.19 | 0.9667 |
| 600 | 10 | 11.33 | 0.8144 |
| 750 | 10 | 9.83 | 0.9748 |

## 5.5 Discussion

The proposed method for identification of fault location has been achieved using linear regression method to calculate the attenuation constant for the under-damped current oscillation. After successful fault detection and isolation, the methodology discussed is utilized for location of fault on the concerned transmission line. Robustness of the method has been proposed against variation of fault resistance and the accuracy has been verified. Measurement noise was also added to the simulated data to mimic real field measurements and the fault location accuracy do not differ from the measurements without the influence of noise.

## 5.6 Conclusion

To accurately locate faults in a MTdc network, a method using the natural discharge of the transmission line current has been proposed. After a fault is detected in a particular zone the hybrid dcCB's in the faulted section operate to isolate the faulted transmission line. Once the faulted transmission line is interrupted the rest of the network forms an under damped oscillating $RLC$ circuit in the absence of a driving voltage source up to the fault point. A relationship between the oscillating fre-

quency and the rate of attenuation was established. The method of linear regression was utilised for calculation of attenuation. The robustness of the proposed scheme was verified against various fault resistances and different fault locations. Measurement noise did not have a great influence on the proposed method. This Chapter thus provided a successful passive fault location method without the injection of any external current or voltage signals.

# CHAPTER 6: CONCLUSION AND FUTURE WORK

This dissertation presents the challenges associated with detection and isolation of faults on MTdc networks. Fast and accurate fault detection is of utmost importance to ensure proper operation of MTdc networks. Some methods and techniques have been proposed in this dissertation that address the challenges associated with current methodologies. These methods have been validated for their responses to sensitivity, measurement noise and other parameters to justify the robustness of the proposed fault detection algorithms.

In Chapter 2, the various stages of fault for a VSC (two-level and MMC) has been analyzed. VSCs form the backbone of development of MTdc networks. Thus, fast detection and isolation is required. The various stages of faults from a line-to-line and line-to-ground fault has been analyzed. Due to the fast rate of rise of fault current in dc systems, ac breakers are not capable in fault interruption within a short period of time. Thus, the need for specially designed dc breakers has been emphasized. The dc breakers depend when the fault has been detected that triggers the breakers. From the analysis of fault currents in the dc breakers, certain factors can be deduced that drive the selection of fault detection methods.

In Chapter 3, a method for fault detection has been highlighted using spectral analysis of the fault signal. During faults the energy storage components across the network fail to release the stored energy abruptly, and electric and magnetic fields build around the conductor giving rise to high frequency electromagnetic waves that traverse the grid called traveling waves. The incident waves traveling almost at the speed of light reach the sensors located closest to the point of the fault. The discussed method of analyzing the fault signal using wavelet transform highlights the need to

target specific bands of high frequencies that are highlighted on the onset of faults using MRA. With the use of wavelet transform for analysis the change in energy distribution of the faulted transmission line can be compared with a non-faulted section of the network. This information, extracted from the traveling waves, is utilized in the fault detection.

In Chapter 4, another method for fault detection has been evaluated in a radial MTdc network emphasizing the use of local measurements for fault detections. Various methods for fault detection has been evaluated in literature that require a communication channel for decision making. Communication channels can introduce delays in fault detection and is also difficult to realize. The proposed method leverages the direction of arrival of fault transients in the form of current and voltage signals at the hybrid dcCB locations. The rate of change of the current and voltage transients are compared to their respective thresholds before a fault is detected.

This non-communication based method was analyzed against varying system conditions and fault locations. The robustness of the detection algorithm has been discussed in Section 4.7.3. The speed of detection was compared with other existing methods, and it was found to be around the similar time-frame. This method also helps to identify between internal and external faults of a breaker. Thus, faults occurring outside the protection zone do not affect a non-faulted section of the network.

In Chapter 5, a novel non-intrusive fault location method has been proposed for fault location in MTdc networks. The proposed method analyzes the natural transmission line current discharge after fault detection and isolation using methods discussed in Chapter 3 and Chapter 4. Once the breakers have isolated the fault the rest of the network can be treated as an under damped oscillating $RLC$ network. From the under damped oscillating discharge of the transmission line capacitance the oscillating frequency and attenuation can be calculated using methods of linear regression. A relationship between the oscillating frequency and fault location was established.

Table 6.1: Summarized results of the proposed methods

| **Attribute** | **Proposed Methods** |
|---|---|
| Reliability | The proposed methods were able to distinguish faulted sections of the network and breakers were operated accordingly, this helped in easier fault location. The methods were 100% reliable to isolate and locate faults |
| Speed | The speed of detection was achieved in milliseconds, similar to the other proposed methods in literature, use of non-communication based approach in Chapter 4 helped to avoid communication delays |
| Robustness | The proposed algorithms were 100% robust to varying system parameters like fault location, current limiting inductance etc. |
| Cost | Application of regular voltage and current sensors are required to implement the proposed methods |

The proposed method was analyzed with the influence of measurement noise and fault location in various sections of the transmission line. Others methods in the literature have been able to provide fault location in dc transmission lines with the injection of external voltage or current signals, but the proposed method was able to locate faults without the use of external signal injections.

The proposed methods meets the objectives that are essential for fault detection and location. Table 6.1 summarizes the findings from the previous Chapters. A comparison metric based on speed, reliability etc., between the two fault detection strategies using wavelets and direction of current and voltage transients as discussed in Chapter 3 and Chapter 4 respectively, is listed in Table 6.2.

## 6.1 Future Work

Although multiple fault detection methods and their applications were considered in this dissertation, many more opportunities lie ahead in terms of research in this emerging field. As realization of MTdc networks start becoming a reality, fault detection in multiple grid intersections is going to be a challenge.

Validation of the proposed algorithms in a controller hardware in the loop test will

Table 6.2: Comparison of the fault detection methods proposed in Chapter 3 and Chapter 4

| **Attribute** | **Wavelet based fault detection** | **Direction of current and voltage transients** |
|---|---|---|
| Reliability | Calculating the energy change across a large network can become challenging, any communication delay or outage can cause the system to collapse under a fault | The rate of change of current and voltage transients are observed against a set threshold to detect a fault, calculating the correct threshold is a challenging task and can be affected by sampling frequency |
| Speed | The method requires a central decision making unit that communicates with the breakers connected to the network, thus communication delays cannot be avoided. For a larger network such an integration can be challenging | The breakers are operated individually and communication is not required for their operation. The detection at the breaker is faster compared to the other proposed method |
| Robustness | Fault transients travel across the network causing variations in the energy between the faulted section and non-faulted section, this is independent of the fault location and system parameters | Voltage and current transients at the onset of a fault arrive at the breaker locations and is not affected by system parameters, fault location, fault resistance etc. |
| Cost | This would require a communication channel and a central decision making unit that would control the breakers | The breakers are operated individually, communication channel cost is avoided |

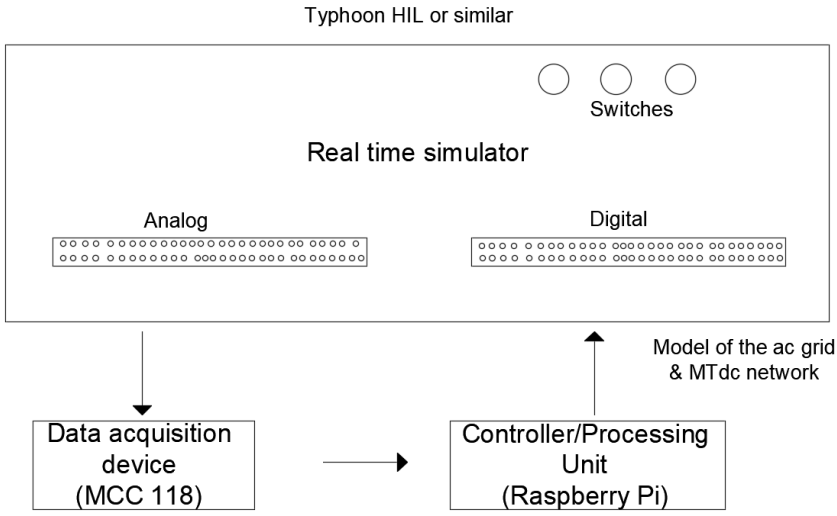



Figure 6.1: Hardware setup for real-time controller in loop

help to set the bench-mark in this developing field. Development of a real time controller performing analysis of traveling waves in real time using multiple applications of signal processing can be realized. Most toolboxes provide the platform for offline analysis for the same, but currently no such controller has been developed. Such a controller development can be realized with the use of a Raspberry Pi and a data acquisition tool like MCC 118 [87]. A schematic representation for such a realization is shown in Figure 6.1.

Realization of high power rating converter setup in a laboratory is difficult, but as discussed, real-time simulations to mimic MTdc networks are going to become an indispensable tool. Methods like Adams-Bashforth, Runge-Kutta, Backward Euler have been used widely for representation of mathematical based models of converters. But these methods have some of their own specific drawbacks. Methods like Forward Euler and Runge-Kutta are suited for non-stiff differential equations. These drawbacks can be addressed using the Adomian decomposition method. The Adomian decomposition method can be used to approximate such analytical solutions of non-linear differential equations as a sum of an infinite series decomposed into sev-

eral functions. These solutions can be utilized to model the highly non-linear switch functions for MMC and also speed the convergence of the solutions.

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# APPENDIX A: CABLE DESIGN

The cable design cross section utilised for modeling of the three terminal VSC network in Chapter 3 is shown below in Figure A.1.

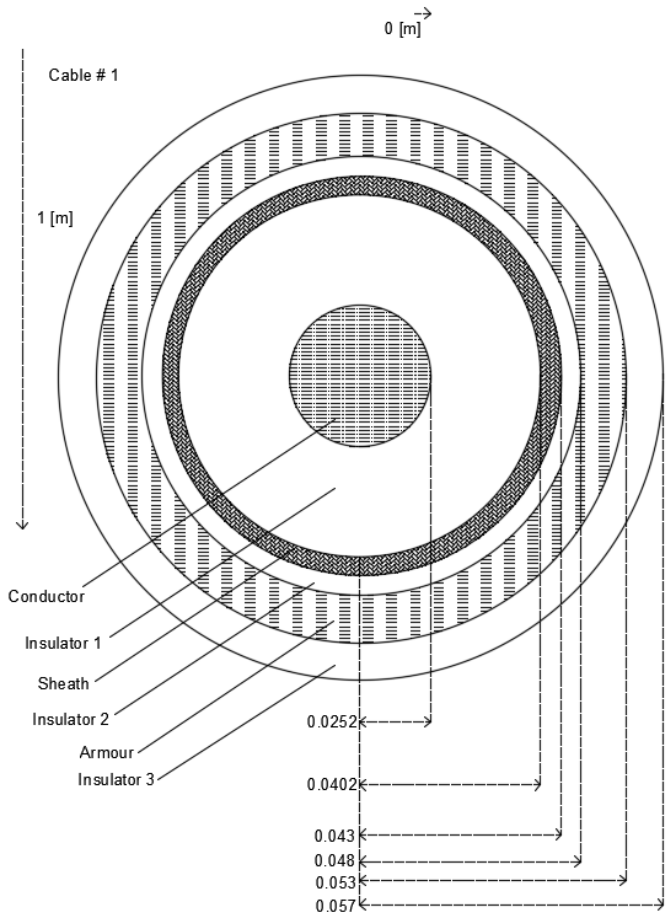


Figure A.1: Cable cross-section

# APPENDIX B: TRANSMISSION LINE DESIGN

The transmission line designed utilised in modeling of the radial MTdc network in Chapter 4 is shown below in Figure B.1.

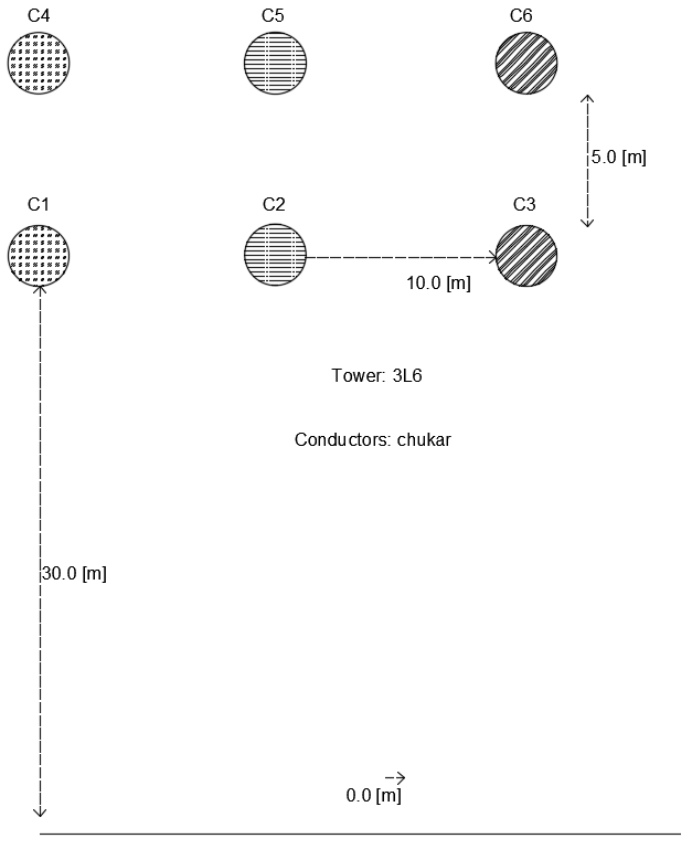


Figure B.1: Transmission line model

# VITA

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