INVESTIGATIONS ON TOPOLOGY, ANALYSIS AND EXPERIMENTAL VERIFICATION OF CENTER-POINT-CLAMPED POWER LINE CONDITIONER

by

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ABSTRACT

PANKAJ KUMAR BHOWMIK. Investigations on Topology, Analysis and Experimental Verification of Center-Point-Clamped Power Line Conditioner. (Under the direction of DR. MADHAV MANJREKAR)

A new approach for power line conditioning has been presented in this dissertation. Prevalent state of the art line-conditioning devices like Static Voltage Restorer (SVR), Dynamic Voltage Restorer (DVR) and AC-AC power line conditioner offers higher bandwidth and low filter size requirement due to their high switching frequencies. However, commercial utilization of such devices is restricted by voltage blocking capability of power semiconductor switches employed in these converters. Recent literature reports a Center-Point-Clamped AC-AC Converter topology based on Neutral-Point Clamped DC-AC inverter, where the grid voltage is clamped to its midpoint to reduce the voltage stress on the bi-directional switches employed in the converter by 50%. This document introduces a Power Line Conditioner based on Center-Point-Clamped AC-AC Converter topology, where the grid voltage is clamped to its midpoint to reduce the voltage stress on the bi-directional switches employed in the converter to half the summation of grid input and load output voltage. This power line conditioner is coined as Center-Point-Clamped Power Line Conditioner (CPC PLC). A duty cycle control scheme has also been implemented for feedback control of CPC PLC. An experimental prototype has been built in the laboratory. The results verify that proposed CPC PLC offers reduced voltage stress on the bi-directional switches. It may also be that CPC PLC is capable of mitigating grid voltage sag up to 90% and grid voltage swell up to 10%, which comprise of about 74% of the grid power quality issues. Furthermore, these results verify that the designed duty-cycle based control scheme has excellent load voltage regulation under dynamic line voltage conditions.

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1. Chapter One: Introduction

1.1. Introduction to Power Quality

The modern grid with its aging infrastructure has been susceptible to issues related to quality of power supplied to customers. Traditionally, power quality would be assessed by the ability of utilities in providing uninterrupted electrical power to its customers. But the rapid technological advancement in the past few decades have changed meaning of power quality.

Table 1-1: List of current standards on power quality issues [1]

Standards	Description
IEEE Standard 519-1992	Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems
IEEE Standard 1159-1995	Recommended Practice for Monitoring Electric Power Quality
IEEE Standard 1100-1999	Recommended Practice for Powering and Grounding Sensitive Electronic Equipment
IEEE Standard 1250-1995	Guide for Service to Equipment Sensitive to Momentary Voltage Disturbances
IEEE Standard 1366-2012	Electric Power Distribution Reliability Indices
IEC 61000-2-2	Compatibility Levels for Low-Frequency Conducted Disturbances and Signaling in Public Supply Systems
IEC 61000-2-4	Compatibility Levels in Industrial Plants for Low-Frequency Conducted Disturbances
IEC 61000-3-2	Limits for Harmonic Current Emissions (Equipment Input Current Up to and Including 16A Per Phase)
IEC 61000-4-15	Flicker Meter – Functional and Design Specifications
EN 50160	Voltage Characteristics of Public Distribution Systems

The current definition of power quality includes comprehensively any disturbance, like voltage swells, voltage sags, transients, EMI and RFI noise, brownouts, blackouts, and also harmonic distortion to the perfect sinusoidal ac voltage waveform. Over the years, several

standards worldwide have been introduced to quantify power quality. Some of the current standards on power quality are tabulated in Table 1-1.

1.2. Power Quality Terms

Some of the common terms used to quantify or describe issues related to power quality has been defined in detail in IEEE standards [1], [2].

- Flicker: The steady fluctuation of light intensity with time which can be perceived by visual inspection.
- Fundamental (component): The first component with the order of n=1 of the Fourier series of a periodic and continuous signal containing nth term.
- Harmonic (component): The component of the Fourier series of a periodic and continuous signal which has a frequency equal to integral multiple of the fundamental frequency.
- Interharmonic (component): The component of the Fourier series of a periodic and continuous signal which has a frequency equal to non-integral multiple of the fundamental frequency.
- Imbalance or Unbalance (current or voltage): The percentage deviation of the negative sequence component from the positive sequence. It is defined as the ratio of negative to positive sequence component.
- Voltage Imbalance: The ratio of negative sequence voltage to positive sequence voltage.
- Impulsive Transient: A sudden change in amplitude of voltage or current from steady-state value, which is unidirectional in polarity, either in positive cycle or negative cycle.

- Oscillatory Transient: A sudden, non-power frequency change in the steady state value of current, voltage or both that has both positive and negative polarity values.
- Instantaneous: Any event that has a duration from 0.5 to 30 cycles of power frequency.
- Momentary: Any event that has a duration from 30 cycles of power frequency to 3 seconds.
- Temporary: Any event that has a duration greater than 3 seconds but less than 1 minute.
- Sustained: Any event that has a duration greater than 1 minute.
- Interruption: An event that forces a signal amplitude to be less than 10% of the desired amplitude.
- Sag: An event that forces a signal amplitude to be between 10%-90% of the desired amplitude.
- Swell: An event that forces a signal amplitude to be between 110%-180% of the desired amplitude.
- Short duration variation: A variation in the amplitude of the voltage or current signal from desired value for a duration from 0.5 cycle of power frequency to 1 minute.
- Long duration variation: A variation in the amplitude of the voltage or current signal from desired value for a duration greater than 1 minute.
- Undervoltage: A variation in the amplitude of the voltage signal where it gets to 80%-90% of desired value for a duration greater than 1 minute.

- Overvoltage: A variation in the amplitude of the voltage signal where it gets to 110%-120% of desired value for a duration greater than 1 minute.
- Waveform distortion: Any steady-state deviation from the shape of a sinusoid at its fundamental frequency.
- DC offset: A steady-state dc value being added to the sine wave, thereby forcing the mean of sine wave over one period to be either a positive or a negative value.
- Notching: A disturbance which is typically caused when two phases of a polyphase network gets repeatedly short-circuited. This event is akin to transient but repetitive.
- Noise: Unwanted electrical signals that create undesirable effects in sensing instruments and control circuitry of a device.
- Voltage fluctuation: A series of periodic variations in the voltage signal.
- Phase shift: The relative time displacement between two sine waves of same frequency, popularly seen in polyphase networks.
- Total Harmonic Distortion (THD): The ratio of summation of rms value of harmonic waves at different harmonic frequencies to rms value of sine wave at fundamental frequency.
- Power frequency variation: Any deviation of electrical power frequency from desired value for a duration from several cycles to several hours.
- Voltage regulation: The degree of controllability of output load voltage at desired value.

All of these terms are issued to quantify power quality issues, which are displayed in Table 1-2.

Table 1-2: Categorization of Power Quality Issues [3], [4]

Problems	Category	Categorization	Causes	Effects
Transients	Impulsive	Peak, rise time and duration	Lightning strikes, transformer energization, capacitor switching	Power system resonance
	Oscillatory	Peak magnitude and frequency components	Line, capacitor, or load switching	System resonance
Short-duration voltage variation	Sag	Magnitude, duration	Motor starting, single line to ground faults	Protection malfunction, loss of production
	Swell	Magnitude, duration	Capacitor switching, large load switching, faults	Protection malfunction, stress on computers and home appliances
	Interruption	Duration	Temporary faults	Loss of production, malfunction of fire alarms
Long-duration voltage variation	Sustained Interruption	Duration	Faults	Loss of production
	Undervoltage	Magnitude, duration	Switching on loads, capacitor de-energization	Increased losses, heating
	Overvoltage	Magnitude, duration	Switching off loads, capacitor energization	Damage to household appliances
Voltage Imbalance		Symmetrical components	Single-phase load, single-phasing	Heating of motors
Waveform Distortion	DC offset	Volts, amperes	Geomagnetic disturbance, rectification	Saturation in transformers
	Harmonics	THD, harmonic spectrum	ASDs, nonlinear loads	Increased losses, poor power factor
	Interharmonics	THD, harmonic spectrum	ASDs, nonlinear loads	Acoustic noise in power equipment
	Notching	THD, harmonic spectrum	Power electronic converters	Damage to capacitive components
	Noise	THD, harmonic spectrum	Arc furnaces, arc lamps, power converters	Capacitor overloading, disturbances to appliances
Voltage flicker		Frequency of occurrence, modulating frequency	Arc furnaces, arc lamps	Human health, irritation, headache, migraine
Voltage fluctuations		Intermittent	Load changes	Protection malfunction, light intensity changes
Power frequency variations			Faults, disturbances in isolated customer-owned systems and islanding operations	Damage to generator and turbine shafts

These power quality issues may be further quantified into various categories as shown in above table using Table 1-3.

Table 1-3: Quantification of Power Quality Issues [5]

Problems	Category	Sub-categories	Typical Spectral Content	Typical Duration	Typical voltage magnitude
Transients	Impulsive	Nanosecond	5ns rise	<50ns	
		Microsecond	1μs rise	50ns-1ms	
		Millisecond	0.1ms rise	>1ms	
	Oscillatory	Low frequency	<5kHz	0.3-50ms	0-4pu
		Medium frequency	5-500kHz	20μs	0-8pu
		High frequency	0.5-5MHz	5μs	0-4pu
Short-duration voltage variation	Instantaneous	Interruption		0.5-30cycles	<0.1pu
		Sag		0.5-30cycles	0.1-0.9pu
		Swell		0.5-30cycles	1.1-1.8pu
	Momentary	Interruption		30cycles-3seconds	<0.1pu
		Sag		30cycles-3seconds	0.1-0.9pu
		Swell		30cycles-3seconds	1.1-1.4pu
	Temporary	Interruption		3seconds-1minute	<0.1pu
		Sag		3seconds-1minute	0.1-0.9pu
		Swell		3seconds-1minute	1.1-1.2pu
Long-duration voltage variation	Sustained Interruption			>1minute	0.0pu
	Undervoltage			>1minute	0.8-0.9pu
	Overvoltage			>1minute	1.1-1.2pu
Voltage Imbalance				Steady State	0.5-2%
Waveform Distortion	DC offset			Steady State	0-0.1%
	Harmonics		0-100th harmonic	Steady State	0-20%
	Interharmonics		0-6kHz	Steady State	0-2%
	Notching			Steady State	
	Noise		Broadband	Steady State	0-1%
Voltage flicker					0.2-2Pst
Voltage fluctuations			<25Hz	Intermittent	0.1-7%
Power frequency variations				<10s	

1.3. Power Quality Definitions

Institute of Electrical and Electronics Engineers (IEEE) Std 1100-1999 defines Power Quality as "Power Quality is the concept of powering and grounding sensitive equipment in a matter that is suitable to the operation of that equipment." International Electrotechnical Commission (IEC) includes power quality within "Electromagnetic Compatibility". IEC Standard 61000-1-1 says "Electromagnetic Compatibility is the ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment."

1.4. Impact of Power Quality Issues

IEEE defines any grid issue as a power quality problem when, "Any power problem manifested in voltage, current, or frequency deviations that results in failure or misoperation of customer equipment." The increasing use of smart devices controlled by microprocessors, electronic power converter-based loads, adjustable speed drives and the introduction of automated manufacturing processes have led to rise in issues related to reliability and quality of the power supplied by the utilities [6], [7]. The traditional grid used to promise a reliability of 3-nines which may be interpreted as 99.9% reliable or 9 hours downtime in a year. But the microprocessors used in e-commerce industry for high speed computing require 9-nines reliability which may be computed to 31.5569 milliseconds in a year [8].

Table 1-4: Uptime and Maximum Downtime per year

Reliability	**Uptime**	**Maximum Downtime per Year**
Nine Nines	99.9999999%	31.5 milliseconds
Eight Nines	99.999999%	315 milliseconds
Seven Nines	99.99999%	3.15 seconds
Six Nines	99.9999%	31.5 seconds
Five Nines	99.999%	5 minutes 35 seconds
Four Nines	99.99%	52 minutes 33 seconds
Three Nines	99.9%	8 hours 46 minutes
Two Nines	99.0%	87 hours 36 minutes
One Nine	90.0%	36 days 12 hours

The estimate of budget requirement for achieving each additional nine of reliability is not linear. In residential grid, the utility could get away with a three nine reliability. But commercial retail outlets would like to improve to five nines reliability to minimize sales loss as most of the transactions are electronic. These outlets would also agree to pay higher tariff rates to the utilities in order to improve customer satisfaction. Similarly, e-commerce, telecom, manufacturing and finance industries might be willing to pay higher tariff rates to ensure nine nines reliability. For instance, on 16th August 2013, Amazon web-services had a temporary outage for 30 minutes, which reportedly cost them $66,240 per minute of outage, which may be estimated at a total loss of nearly $2 million for Amazon itself [9]. Since then, Amazon has come a long way as it ensures nine nines reliability to all its web-services clients. They introduced redundant energy storage systems for their data-centers.

1.5. Causes of poor Power Quality

There has been a paradigm technological shift in the field of power systems ranging from transmission networks to the very edge of the distribution network. This transformation has been pushed into effect due to a multitude of reasons. The major motivation behind this transcendental change has been the following [10-18]:

- Increase in utilization of power electronic converter-based loads.
- Increase in grid penetration of Renewable Energy Resources
- Increase in load demand
- Increase in Distributed Energy Resources
- Increase in popularity of Electric vehicles
- Increase in fossil fuel costs
- Increase in Environmental Pollution

All of the above-mentioned events have adversely affected the power systems from utility perspective. It has introduced voltage sags and surges in the utility-maintained power grid since we have a new unprecedented scenario in utility perspective which is the phenomenon of bidirectional active and reactive power flow to the grid. It affects the conventional voltage regulation equipment like the tap changing transformer which has been installed in the conventional grid to step change for voltage regulation only in case of unidirectional power flow.

The existing conventional power grid was designed keeping in mind the demand and complexity of the power system decades ago. But with the advent of twenty first century,

we have seen a sudden rise in the integration of Distributed Energy Resources (DERs), electronic loads, Electric Vehicles, etc. into the conventional power grid. This unprecedented intrusion of DERs has caught the utility industry off-guard as they have laid out the outline of their conventional power grid in accordance to the then available conventional energy resources [19].

Also, another alarming reality faced by the utility industry is their inability to control the integration of Renewable Energy Resources based DERs [19]. This makes energy supply side management very intimidating for the utility thereby resulting in power voltage regulation at the customers end. The rise in DERs and exponential rise in load demand with increasing economy has also effected poor demand side management from utility perspective as they have to constantly monitor the load demand and adaptively control their supply resources to continue to serve their customers with electric power conforming to the standard permissible limits.

The rising economy has boosted the establishment of new medium scale industries which necessitates a sudden surge in electrical energy. Although the utilities have been able to provide this ever-increasing customer load demand, it starts to get complicated from the utility perspective when these medium scale industry customers start switching their loads depending on their requirements. This unpredictability of industry load switching makes voltage regulation with regards to load forecasting extremely tricky as these load swings have a deep impact on the voltage quality of the grid which also suffers from sudden sags and surges, thereby impacting all the customers connected to the grid.

We can argue that the conventional grid has tap changing transformers which switch according to the voltage levels to different taps to provide the downstream customers power

at their desired voltage levels. But it has to be also taken into consideration that frequent tap changing operation impacts the lifetime of these voltage regulators as they are rated for a certain number of tap changing operations in their operational lifetime. It may be argued that the utilities may install more tap changing transformers to regulate the grid, but the major issue faced by them is the ever-changing landscape of the power scenario due to customers embracing the concept of self-generation of electrical energy using renewable energy resources which requires minimal capital investment on their parts as well as minimal maintenance and installation area [20].

1.6. Proposed Solution to Power Quality Issue

Recent advances in power semiconductor industry have facilitated the use of power line conditioners like inverter-based DVR, matrix converter, ac-ac buck converter, ac-ac buck-boost converter and other to maintain the power quality as well as voltage profile of the grid within acceptable tolerances [1]-[28]. The ac-ac direct power converter is unlike inverter-based ac-dc-ac converters where additional energy storage is required in the form of dc link capacitor. Direct ac-ac power converters, without energy storage elements offer advantages such as better efficiency because of single-stage power conversion and smaller footprint because of reduced number of components. But the practical realization of power line conditioner topologies remains challenging due to non-availability of power semiconductor devices rated at utility scale voltage and power levels. A novel topology of Power Line Conditioner, coined as ‘Center-Point-Clamped Power Line Conditioner’ is being proposed as a candidate solution for mitigation of grid power quality issues pertaining to voltage sags, swells and harmonic distortions. This converter topology is based on the principle of Center-Point-Clamped AC-AC Converter topology [21]. The

advantage of this converter over existing power electronic solutions is its utilization of power semiconductor devices rated at half the utility scale voltages. This reduction in power semiconductor device voltage stress enables the use of commercially available low voltage rated, fast switching power semiconductor devices, thereby paving the way for a much smaller footprint and quicker implementation in the real world.

2. Chapter Two: Review of Power Line Conditioners (PLC)

Power Quality issues are monitored using power quality meters, which can monitor and record raw data that can be processed to observe issues ranging from voltage sags, swells and transients to harmonics and power interruptions. This raw data may be interpreted using pie-charts, which helps utilities to understand the frequency and type of events that mostly effect its customers. One such power quality issue data is represented as pie-charts in Figure 2-1 [22].

Figure 2-1: Analysis of Power Quality events

It may be seen from Figure 2-1, that voltage sags and swells comprise 74% of the power quality events in a year. It may be further be noticed that 46% of the power quality events in a year have a huge impact upon the customers.

The probable solutions for these power quality events, especially voltage sags and swells, are being discussed in the literature survey that is being presented in this chapter. These power electronic converter-based power quality solutions have been classified into the categories of power quality issues in Table 2-1 [23].

Table 2-1: Analysis of Power Quality Issues resolved by prevalent power quality solutions

Power Quality Solution → / Disturbance↓			Tap-Changing Transformer	Dynamic Sag Corrector (DySC)	Dynamic Voltage Restorer (DVR)	Unified Power Quality Conditioner (UPQC)	Solid State Transformer (SST)	Three-Phase AC Line Conditioner
Transients	Impulsive						✓	
	Oscillatory							
Short-duration voltage variation	Instantaneous	Interruption			✓		✓	
		Sag	✓	✓	✓		✓	✓
		Swell	✓		✓		✓	✓
	Momentary	Interruption			✓		✓	
		Sag	✓	✓	✓		✓	✓
		Swell	✓		✓		✓	✓
	Temporary	Interruption			✓		✓	
		Sag	✓	✓	✓		✓	✓
		Swell	✓		✓		✓	✓
Long-duration voltage variation	Sustained Interruption							
	Undervoltage		✓	✓	✓			✓
	Overvoltage		✓		✓			✓
Voltage Imbalance							✓	
Waveform Distortion	DC offset							
	Harmonics				✓		✓	
	Interharmonics							
	Notching							
	Noise							
Voltage flicker							✓	
Voltage fluctuations					✓		✓	✓
Power frequency variations							✓	

2.1. Tap-Changing Transformer

The first instance of practical implementation of a voltage regulation device for the power grid may be traced back to 1925, when tap-changing transformers were operated to regulate the grid voltage to desired value [24].

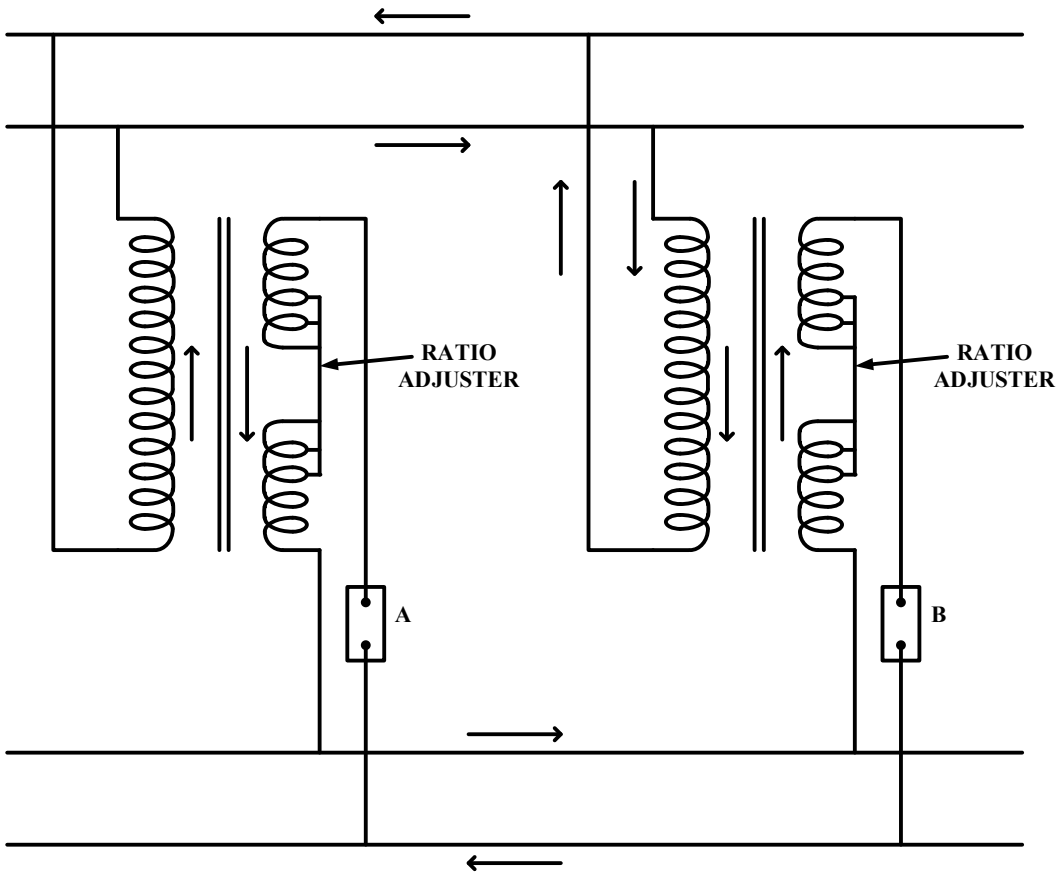


Figure 2-2: Simplified schematic of two tap changing transformer in a utility power line

As may be seen from Figure 2-2, two transformers are connected in parallel across the high and low voltage power distribution lines. They share the loads during normal operating conditions. In case of load voltage regulation operation, the circuit breaker A connected to the low voltage side is opened, which results in the load side being supplied only by the second transformer attached to breaker B. The excitation in the first transformer still remains intact as the high voltage side is still connected to the transformer primary

side. The taps in the secondary windings of the first transformer are then changed to achieve desired load voltage using the Ratio Adjuster. Once the operation is complete, the breaker A is closed to connect the first transfer to the low voltage side. Since the two transformers are now operating with unequal turns ratio, circulating current flows between them in the direction demonstrated by arrows. Now breaker B is closed to change the tap ratio of the second transformer and similar operation procedure as the first transformer tap-changing process is followed in this case. Once the taps are change, breaker B is closed and as the second transformer returns back to normal operation, the circulating current no longer exists as the two transformers have equal turns ratio.

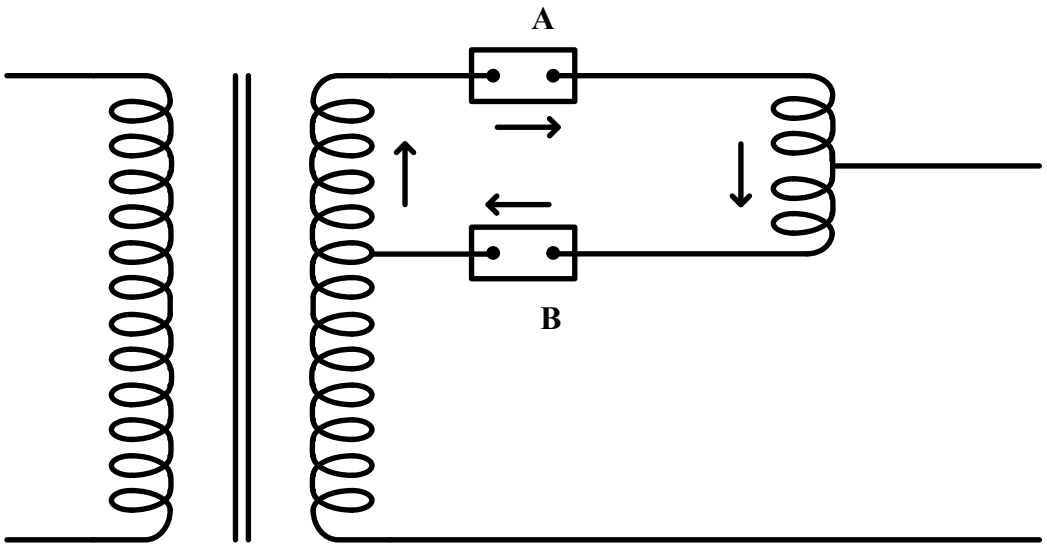


Figure 2-3: Simplified schematic of modified tap changing transformer in a utility power line

This method of voltage regulation has inherent disadvantages, since we need two transformers to achieved line voltage regulation. In order to mitigate this issue, each of the transformer low voltage side taps may be connected to breakers [24], [25]. Each breaker will open depending on the desired tap requirement in the secondary side to achieved desired secondary line voltage. During the transition operation two breakers will be

connected to the secondary side which will generate a circulating current between them in the direction shown by arrows in Figure 2-3. This current may be limited by applying appropriate current limiting reactance on each breaker connection.

It may be seen from the above discussion that tap changing transformers require mechanical circuit breakers or relays to achieve line voltage regulation through its tap changing operation. It may be noted that the mechanical breakers or relay have slower operational speed than power semiconductor-based switching devices. With the advent of power semiconductor devices at the later half of twentieth century, power electronic solutions based on semiconductor devices were proposed for line voltage regulation. One-such solution is known as Dynamic Sag Corrector.

2.2. Dynamic Sag Corrector (DySC)

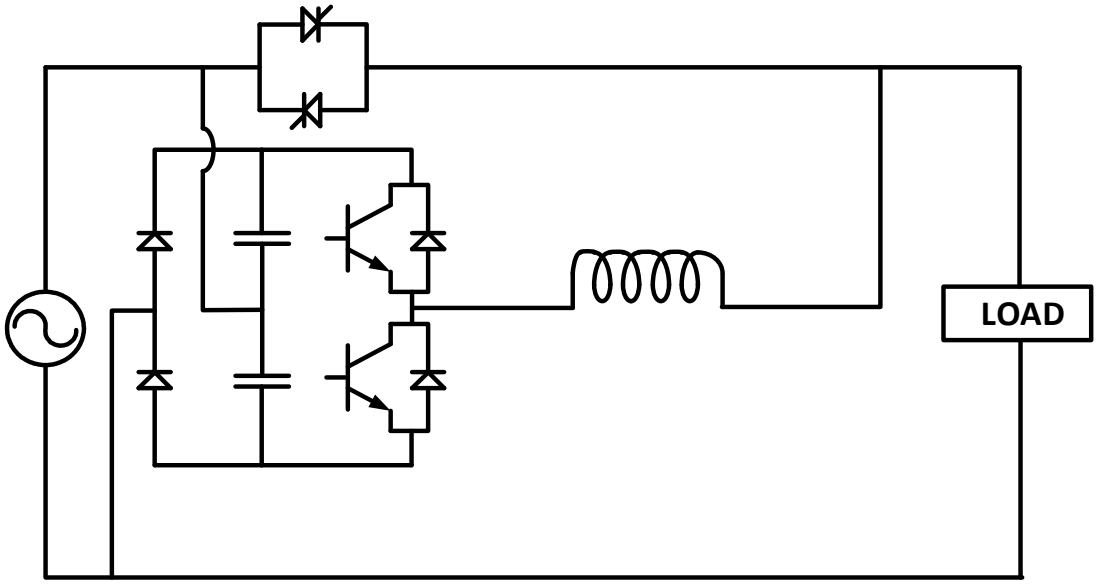


Figure 2-4: Circuit Schematic of a Single-phase Dynamic Sag Corrector (DySC) topology

A study concluded by EPRI has estimated that about 92% of the Power Quality (PQ) issues are caused by voltage sags and lasts less than 2 seconds. A new technique for power line conditioning was reported in [26]. The simplified schematic of the power conditioning device, known as single-phase Dynamic Sag Corrector (MiniDySC) is shown in Figure 2-4. The converter operates in a bypass mode when the grid is operating under rated conditions and customer is supplied power at desired voltage specifications. In bypass mode, the bi-directional thyristor-based switches are always on. In the scenario when the grid voltage does not meet desired customer voltage specifications, the bypass switch turns off and the ac voltage is transformer to dc using a half-bridge diode rectifier. This dc voltage is then boosted to desired ac voltage using a half-bridge inverter. The dc bus capacitance may be designed in such a way that it is able to provide desired customer voltage for grid-side voltage sags up to 50%. The time for detection of sag condition,

commutating the thyristor-based bypass switch and providing the customer with boosted voltage has been reported to be less than 2 ms. The three-phase equivalent of a Dynamic Sag Corrector is shown in Figure 2-5. It is known as Mega Dynamic Sag Corrector (MegaDySC) [26]. It employs a shunt converter to rectify the grid ac voltage to dc voltage, which is then boosted to desired voltage according to load specifications. Under normal grid operating conditions, the bypass switches allow the grid voltage to supply the customer loads.

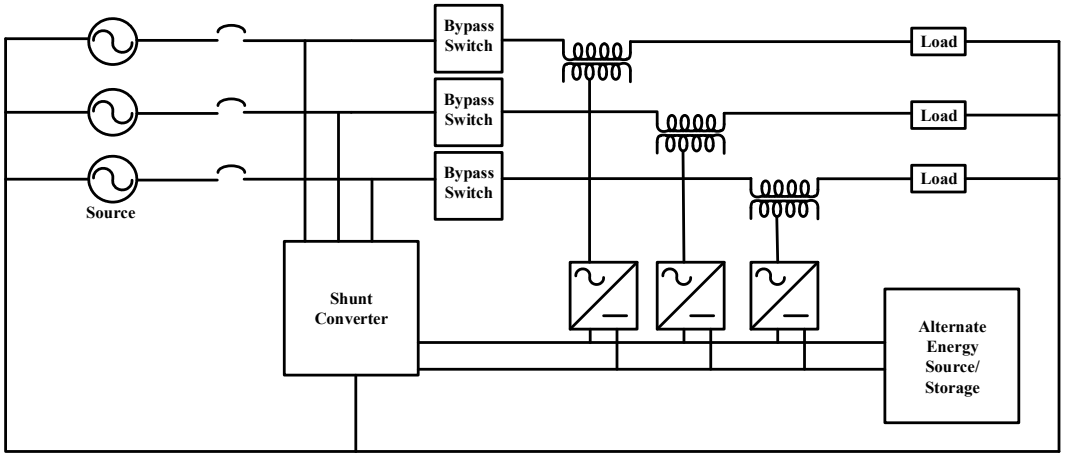


Figure 2-5: Circuit Schematic of a Three-phase Mega Dynamic Sag Corrector (MegaDySC) topology

The advantage of such Dynamic Sag corrector is its transformerless implementation as compared to similar alternative solutions for power line-conditioning, such as Westinghouse's Dynamic Voltage Regulator (DVR), General Electric's SSVR. These other solutions use a transformer to inject voltage in series to the grid voltage to compensate for grid voltage sag and surge conditions.

2.3. Dynamic Voltage Restorer (DVR)

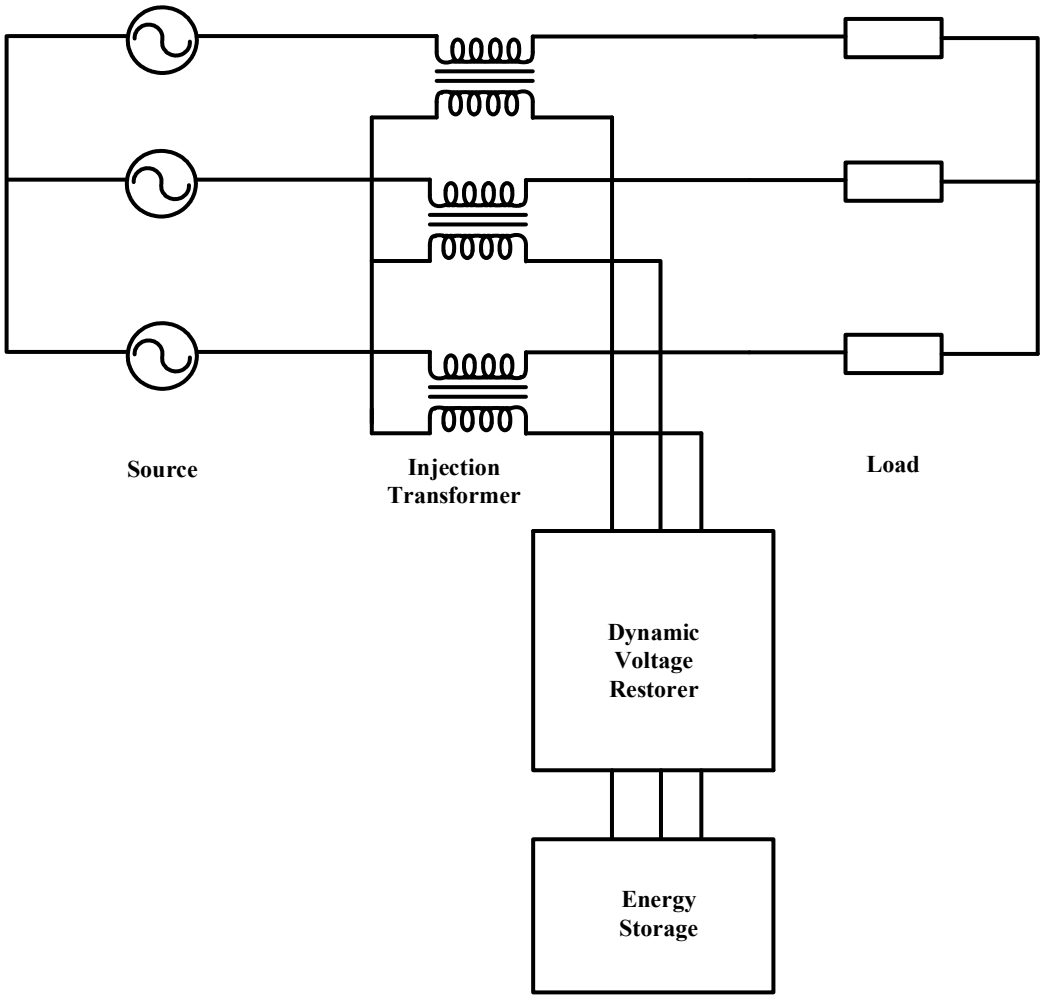


Figure 2-6: Circuit Schematic of a Dynamic Voltage Restorer (DVR)

An alternate solution for restoring grid power quality issues related to voltage quality is a Dynamic Voltage Restorer (DVR). A DVR has an energy storage system attached to it, wherein the energy may be supplied through a Battery Energy or a Flywheel based Energy Storage System. Upon grid voltage sag or swell conditions, the DVR injects a voltage in series to the grid voltage to provide customer load with desired voltage specifications.

The DVR may be constructed using voltage source power electronic converters, such as H-bridge converter, H-bridge cascaded multilevel converter, back to back converter and

matrix converter [27], [28], [29-36]. Upon normal operating conditions, the DVR does not inject any voltage in series with the grid voltage, thereby allowing the grid voltage to supply the load.

The operating principle of a DVR has two main control strategies, detection of power quality issue and generation of reference signal for the current or voltage control methodology [37]. Various literatures have reported detection techniques, such as rms, peak or dq0 components measurements, phasor measurements techniques using Kalman Filter or Fourier transformation, or wavelet method. The generation of reference signal depends on active power supply capability of energy storage system and type of customer loads. Four techniques for customer load voltage control using DVR have been reported in [37]. These techniques are in-phase, pre-sag, energy minimized and hybrid voltage compensation methodology. A brief discussion of the four techniques has been discussed in this sub-section. In-phase technique allows the reference signal to be generated in synchronization with the grid voltage. Thus, the injected DVR voltage is in phase with the grid voltage irrespective of pre-fault conditions. Pre-sag method takes into consideration the load voltage under pre-fault conditions and generates a reference signal in such a way the load voltage is stored to the same voltage as in pre-fault conditions. The in-phase and pre-sag methods utilized the active power supplied by the energy storage to compensate for the load voltage sag. But the energy minimized method utilizes reactive power available in the dc bus of the DVR to compensate for the load voltage sag. This method may be utilized for shallow voltage sags as it requires higher dc link voltage to compensate for deep load voltage sags. The hybrid method is a combination of in-phase and pre-sag technique to generate the reference signal for injection of DVR voltage to compensate for

the load voltage sag. The DVR requires an energy storage system to compensate for voltage sags. Another alternate solution for grid power conditioning, known as Unified Power Quality Conditioner, has been reported in literature which does not require any energy storage system to **compensate for grid voltage disturbances.**

2.4. Unified Power Quality Conditioner (UPQC)

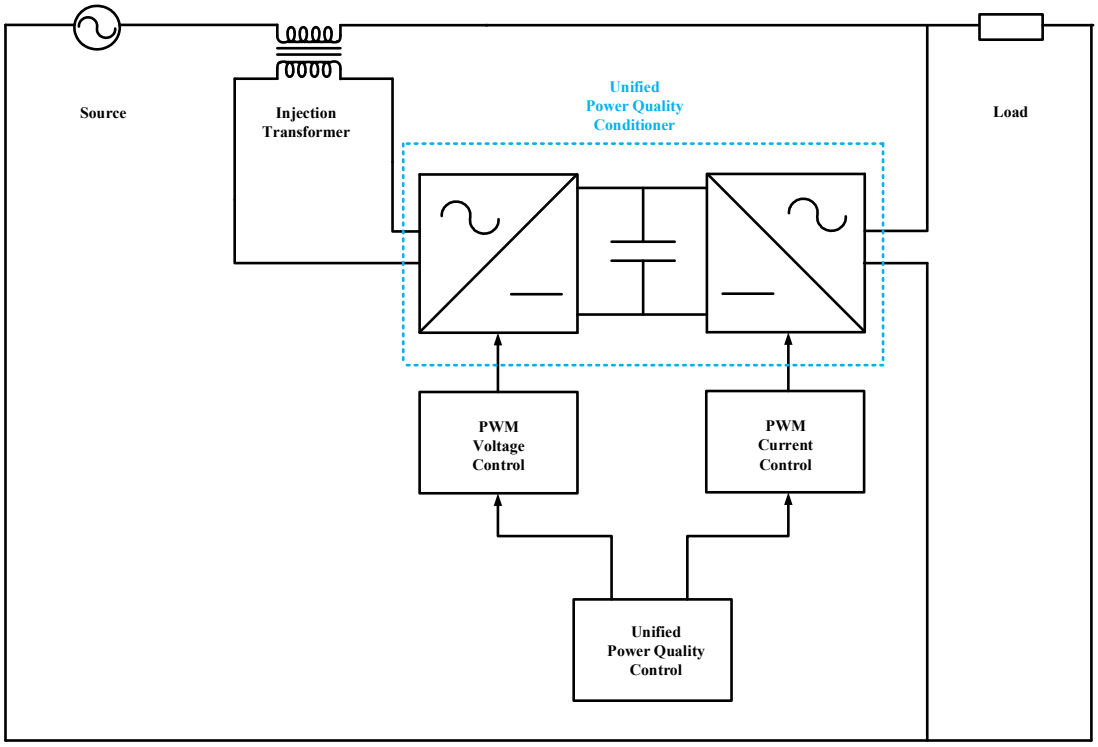


Figure 2-7: Circuit Schematic of a single-phase Unified Power Quality Conditioner (UPQC)

The circuit schematic of a UPQC has been shown in Figure 2-7. It may be seen that UPQC is a combination of series and shunt active power filters [38], [39-43]. It may be used to compensate for grid voltage disturbances and harmonics. The operating principle of the UPQC is such that it generates the reference signal from the fundamental frequency term of the Fourier expansion of the grid voltage. This is voltage is then used as reference signal for the voltage control of the series filter connected to the injection transformer. The shunt

filter is current controlled in such a way that it compensates for harmonic compensates of the load current.

2.5. Solid State Transformer (SST)

The advent of Solid-State Transformers may be traced backed to 1968 when William McMurray first came up with a single-phase solid-state power converter circuit with high frequency ac link, operating as an electronic transformer for a dc supply or a low frequency or power line frequency (60Hz) ac supply. It performs current limiting, current interruption, current regulation and voltage regulation functions. As may be seen from Figure 2-8, the power converter circuit chiefly comprises of eight power transistors, sixteen diodes and a high frequency transformer link.

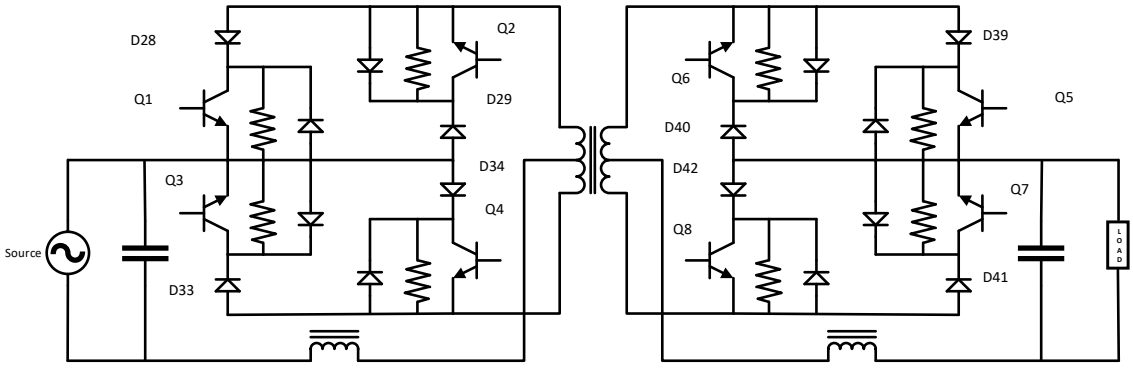


Figure 2-8: Power Converter Circuit having a High Frequency Link

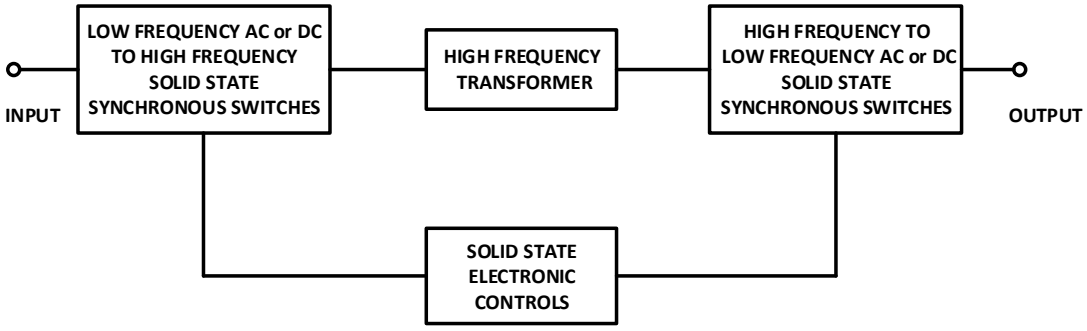


Figure 2-9: Control Schematic for Power Converter Circuit

The published patent paper [44] discusses the operating principle of the Power Converter Circuit as shown in fig. 3. The power semiconductor switches, Q1 and Q2 in the primary side of the high frequency ac link are switched on as the switches, Q3 and Q4 are turned off. Also, the switches Q5 and Q6 on the secondary side of the coupling transformer are also closed synchronously with the transistors, Q1 and Q2, which switching off Q7 and Q8. During the first half of the high frequency switching cycle, assuming that input low frequency ac potential is at positive half cycle, current flows through diode 29 and transistor Q2 and the dot end of the coupling transformer has a positive polarity. Whereas, on the secondary winding of the high frequency transformer, current flows out through its dot end through forward biased diode 39 and transistor Q5. Thus, the load connected to the terminal 36 has a positive polarity with respect to terminal 37. On the other half of high frequency switching cycle, semiconductor switches Q3 and Q4 in primary side are switched on synchronously with transistors Q7 and Q8 in secondary side of the switched converter circuit. It may be observed that the high frequency cycle is switching at relatively much higher rate than low frequency of the ac source, the input terminal still has positive polarity and as such conduction of current takes place through diode 34 and transistor Q4 so that the no dot end of the coupling transformer has a positive polarity with respect to center-tap. Similarly, in the secondary side of the switched circuit, diode 41 and transistor Q7 conducts such that the load terminal 36 is positive with respect to terminal 37. Contrary to the positive low frequency half cycle, in case of negative part of ac sine source signal when input terminal 25 is negative with respect to terminal 26, the other transistors in each of the inverse-parallel connected bidirectional conducting pairs, are rendered conductive

in each high frequency half cycle so that the output terminal 36 is negative with respect to the terminal 37.

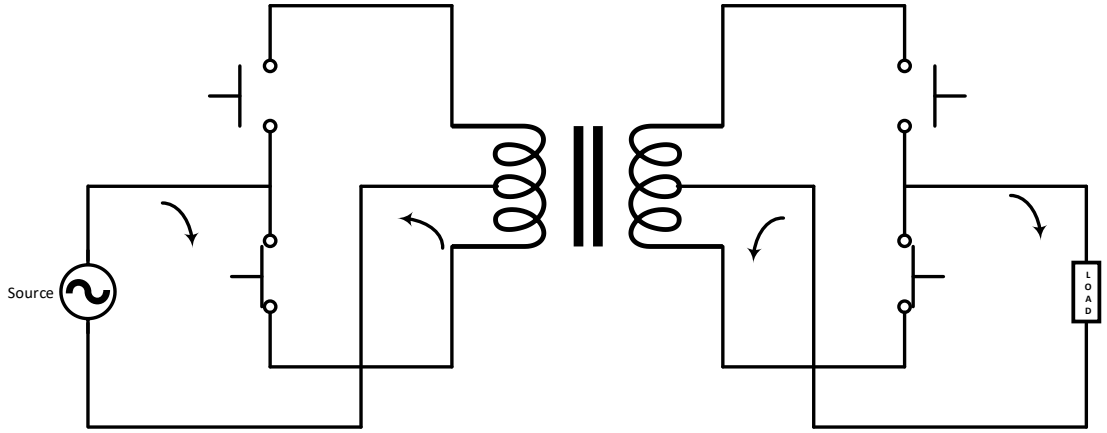


Figure 2-10: Power Converter Circuit during positive half cycle of sine wave

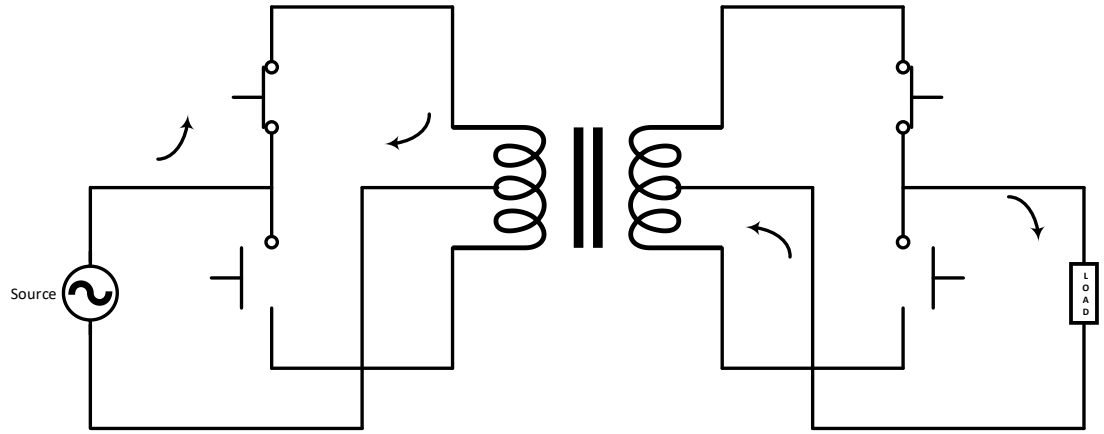


Figure 2-11: Power Converter Circuit during negative half cycle of sine wave

This converter supports bidirectional power flow from source to load as well as from a power generating load to the source. It may be noted that since thyristor switching devices were typically used for higher power and voltage levels in place of power transistors, the thyristor switched converter circuits needed natural commutation which was achieved through shaping of the coupling transformer current into sinusoidal pulses with a natural zero crossing by means of adding a series resonant capacitor was additionally proposed by

McMurray, also in 1968 [44]. This type of resonant converter is known as Half Cycle-Discontinuous Conduction Mode Series Resonant Converter (HC-DCM SRC), due to the discontinuous shape of the transformer current pulses.

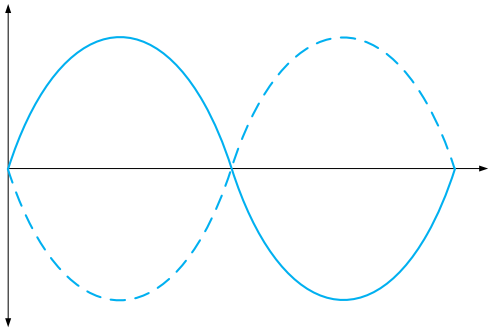


Figure 2-12: Input source signal

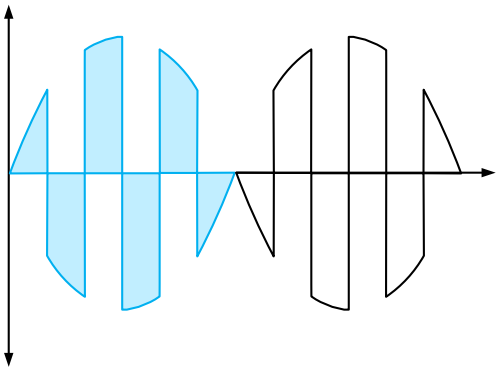


Figure 2-13: Input signal switched at 360Hz switching frequency

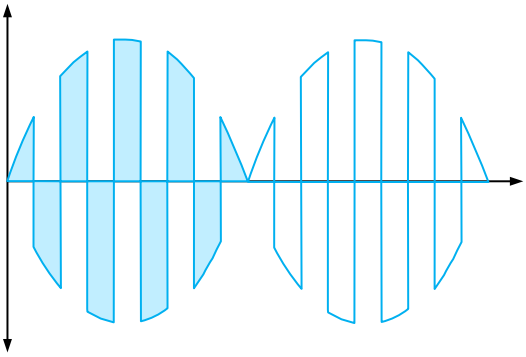


Figure 2-14: Input signal switched at 540 Hz switching frequency

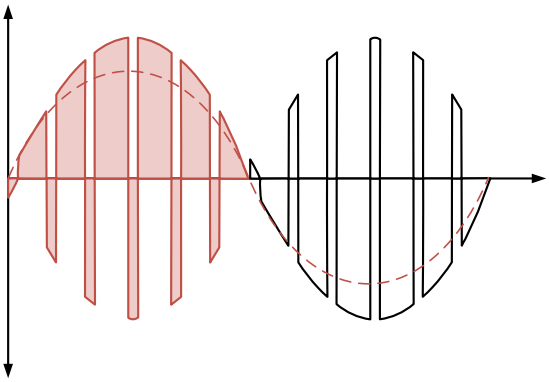


Figure 2-15: Input signal switched at 720 Hz switching frequency

Thus, it may be concluded that this power electronic converter circuit behaves as an ac-ac or dc-dc transformer with fixed voltage turns ratio defined by the winding ratio of the MF transformer. Therefore, it may be seen that even though McMurray used thyristors which needed a zero-crossing operation to get turned off, the power semiconductor devices currently commercially available may be easily used to design McMurray's power converter circuit and as such serves as the backbone for many modern Solid State Transformer (SST) topologies.

Since William McMurray's foray into the world of Solid-State Transformers, there has been extensive research and development in the field of SSTs with many researchers in industry and academia across the globe proposing a myriad of switched converter circuit topologies in the past couple of decades. A survey of recent literature reveals an attempt made by Jonas E. Huber and Johann W. Kolar in classifying these SST/PET topologies into five major classes [45-52], viz.

- Matrix Type AC-AC SST
- Isolated Back End SST
- Isolated Front End SST
- Isolated Modular Multilevel Converter SST
- Single Cell Approach SST

These five major classifications were based on the identification of a few key concepts for SSTs which may be described as follows:

- SST is a means to interface power electronic converter circuits to Medium Voltage Grid, which may be either ac or dc in nature.
- SST also involves an isolation transformer which operates in the Medium Frequency range, which is in the order of a few kHz or MHz. This gives added benefit as compared to line frequency transformers, due to the fact that the physical size or the core volume of a transformer may be defined by this relationship:

$$A_{Core}A_{Wdg} = \frac{\sqrt{2}}{\pi}.\frac{P}{k_w J_{rms}\hat{B}_{max}f}$$

$$\Longrightarrow V \propto (A_{Core}A_{Wdg})^{\frac{3}{4}} \propto \frac{1}{f^{3/4}}$$

Where A_{Core} defines the area of the magnetic core cross section, A_{Wdg} is the area of the winding window, P denotes the power transferred through the transformer, winding current density is written as J_{rms} , the maximum core flux density as $\widehat{B}_{max}$ and f denotes the transformer operating frequency, and k_w is the winding window filling factor.

It may be seen from the relation that Volume of the transformer is inversely proportional to the operating frequency. SST utilizes this fact to significantly reduce the size and weight of the isolation transformer by operating in the range of kHz to MHz.

- SST behaves as a control methodology to generate input and output voltage and current waveform of desired amplitude, phase and frequency. It may also be deemed as a means for power system protection in case of disturbances in the load side or the grid side by isolating the fault section from the rest of the grid.
- SSTs may also provide a means to integrate renewable energy based DERs to the grid by providing an internal dc bus for their integration to the AC utility grid.

The operation and control methodology of the five major classes of SST as described in this paper is as follows:

2.5.1. Matrix Type AC-AC SST

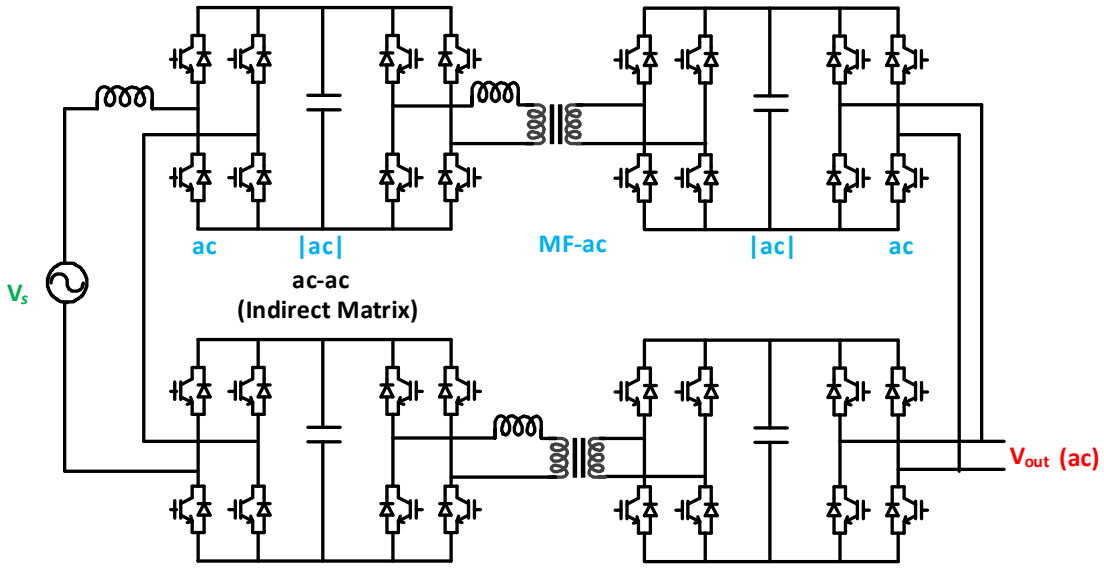


Figure 2-16: Simplified circuit schematic of a typical matrix-type AC-AC SST topology

This topology of AC-AC SST, as shown in Figure 2-16, is connected to the ac grid where there is a full bridge ac rectifier, which behaves as an unfolding stage which converts the line frequency grid ac voltage into a rectified ac voltage. This rectified ac is then converted to a MF-ac voltage with Medium Frequency (several kHz to MHz) switched ac-ac conversion. This MF-ac is then applied to an isolation transformer whose secondary is connected to another MF ac0ac switching circuit, which is then folded using a full-bridge inverter to generate line frequency ac output voltage of desired amplitude, phase and frequency. This SST topology shown in Figure 7 has been patented by General Electric (GE) in 2008 [30].

2.5.2. Isolated Back End SST

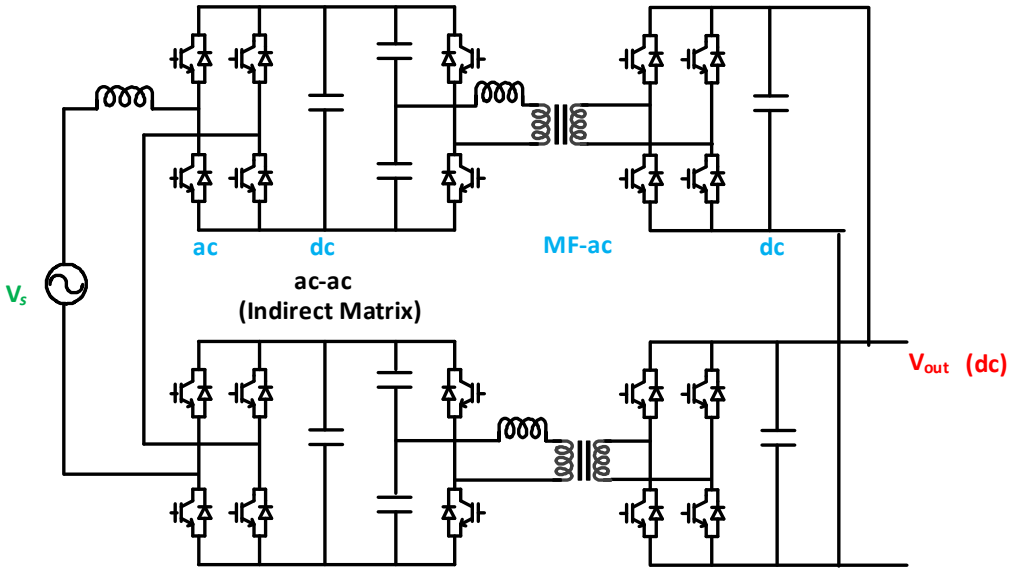


Figure 2-17: Simplified circuit schematic of a typical IBE type SST Topology

As may be seen from the SST topology shown in Figure 2-17, the input grid side voltage is rectified to a dc output voltage using a full-bridge rectifier. This dc output is then clamped at the neutral point and the control methodology allows multilevel switched ac output at medium frequency. This MF-ac output is then impressed upon an isolation transformer operating at MF which is then folded to a dc output using a full bridge rectifier. The Control methodology also allows generation of a stepped / multi-level ac output which facilitates the reduction in size of the output filter in the load side. Since the control for the rectification of the ac voltage and the generation of a multilevel converter-based ac output is dependent on the primary side part of the converter circuit, this topology may be termed as an Isolated Back-End type SST topology. This SST topology has been adopted by ABB for a shunting locomotive which was deployed on Swiss Railroad. The ABB design incorporates interfacing 15-kV, 16-Hz Swiss Traction Grid with power rated up to 1.2 MW. It used 6.5 kV rated Si-IGBTs for a conversion efficiency of 96% and a power to weight

improvement of about 0.4 kVA/kg as compared to a typical Low Frequency traction grid transformer [53].

2.5.3. Isolated Front End SST

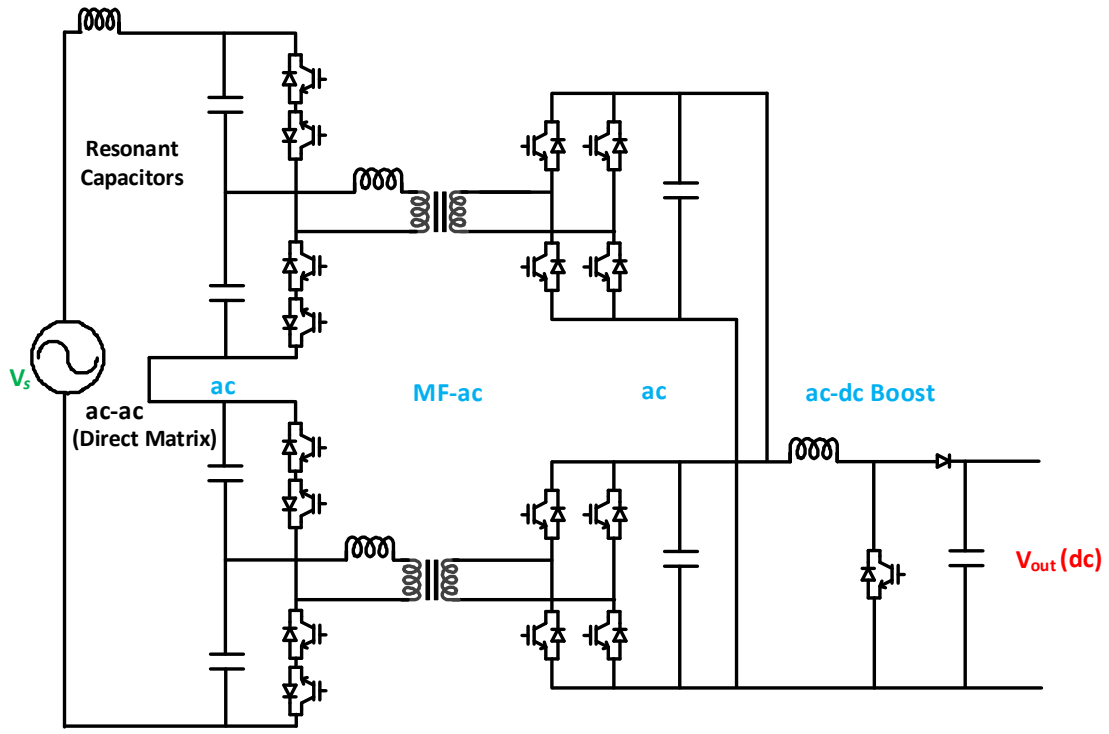


Figure 2-18: Simplified circuit schematic of a typical IFE type SST Topology

As may be seen from Figure 2-18, the converter circuit attached to the primary winding of the Medium Frequency transformer transforms the grid side ac voltage at low frequency to medium frequency ac-voltage. This medium frequency ac voltage is then folded to a rectified ac (dc) voltage using a full-bridge rectifier. This dc voltage is then impressed upon a boost converter whose control methodology allows to draw an output current proportional to folded input voltage on primary side of the isolation transformer, thereby ensuring unity power factor operation on the grid side. Since the control methodology of the output voltage amplitude is dependent on the secondary side of the isolation transformer, this type of topology has been termed as Isolated Front End type SST topology. In recent times, this

SST topology has been adopted by Power Electronics Systems Laboratory of ETH Zurich for utilization in proving concepts for Smart Grid Technologies [54].

2.5.4. Isolated Modular Multilevel Converter SST

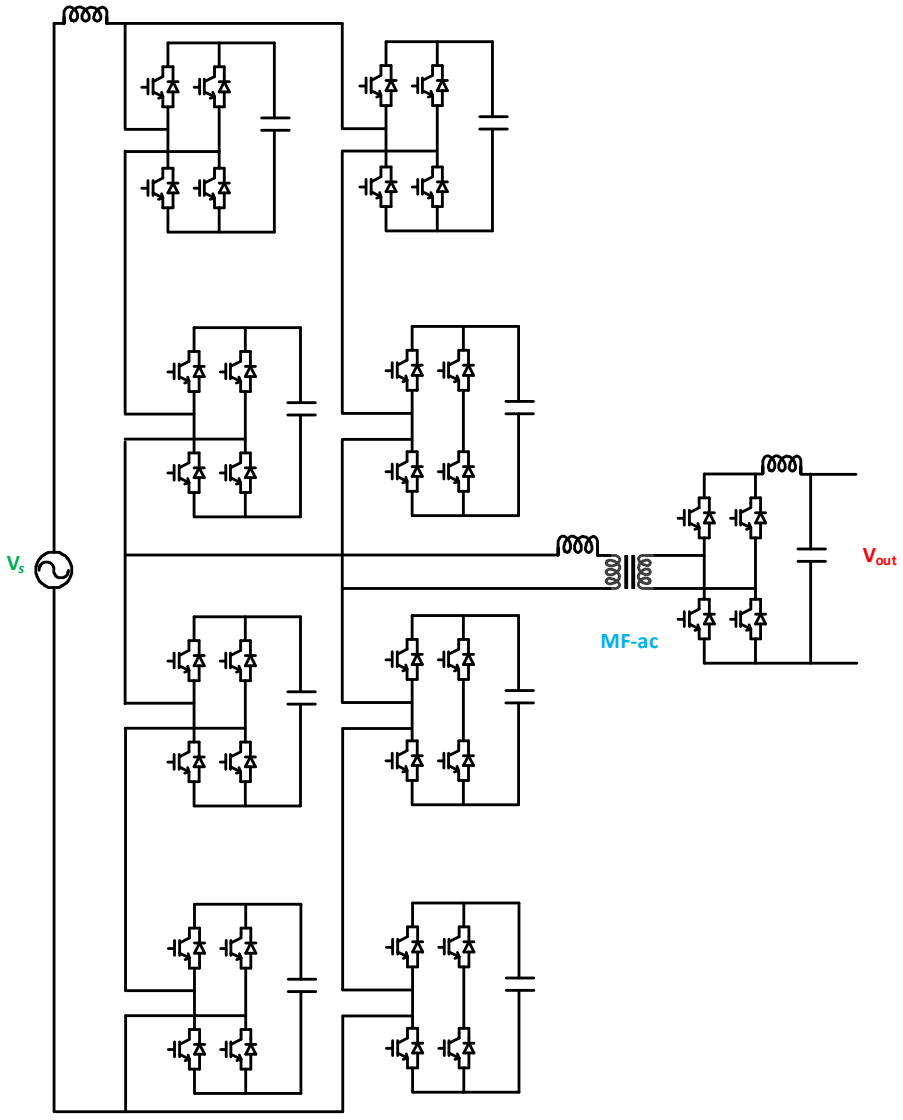


Figure 2-19: Simplified circuit schematic of a typical Isolated Modular Multilevel Converter type SST Topology

As may be seen from Figure 2-19, this SST topology has cascaded modules of a full bridge rectifier which serves as the folding stage for the grid side ac voltage. These modules help

reduce the voltage stress on the power semiconductor devices, thereby necessitating the use of semiconductor devices rated at much lower voltage than the grid voltage. This rectified ac is then passed through an isolation transformer which operates at Medium Frequency. This MF-ac is then inverted to an ac output using a full bridge inverter which serves the purpose of unfolding stage. Thus, this type of SST topology is known as Modular Multilevel Converter type SST topology. This SST topology was suggested for traction grid system [55].

2.5.5. Single Cell Approach SST

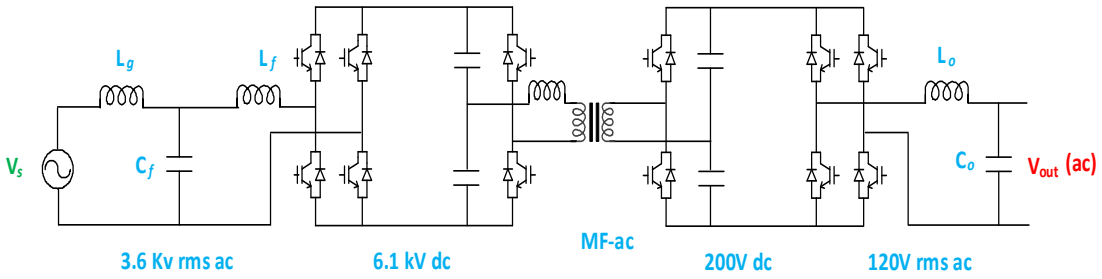


Figure 2-20: Simplified circuit schematic of a typical Single Cell Approach based SST Topology

The recent trends in semiconductor technology have facilitated the utilization of power semiconductor devices rated at Medium Voltage with high switching frequencies ranging upto 1 MHz. The topology shown in Figure 11 was adopted by Future Renewable Electric Energy Delivery and Management (FREEDM) project which employs SiC devices to interface a 13.8-kV Medium Voltage grid [56]. As may be seen from Figure 2-20, the grid ac voltage is rectified to a dc output which is then unfolded to obtain a MF-ac voltage. This MF-ac voltage is impressed upon an isolation transformer operating at medium frequency, which is then again passed through a folding stage to obtain dc output. This dc output is

again unfolded using a full bridge inverter to generate ac output voltage of desired magnitude, phase and frequency.

2.6. Three-Phase AC Line Conditioner

This sub-section discusses a three-phase ac line conditioner, that was reported in [57]. It employs a three-phase ac-ac buck-boost converter for power line conditioning. This topology has major advantages in terms of its simplicity in structure and control design as compared to the previously discussed power conditioning solutions in this chapter. It also does not involve any dc stage in the power conversion. The circuit schematic of the converter topology is shown in Figure 2-21.

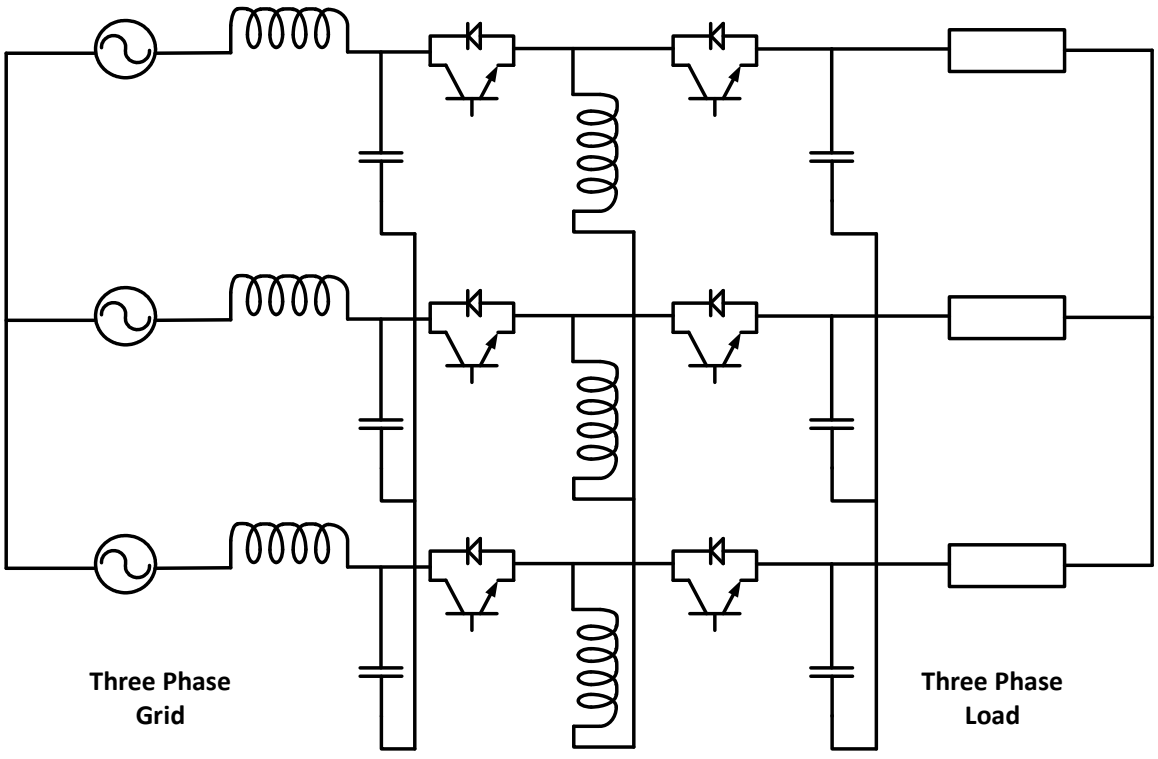


Figure 2-21: Circuit Schematic of a three phase PWM ac-ac buck-boost converter

As may be seen from Figure 2-21, this ac line conditioner is comprised of a three-phase ac-ac buck-boost converter. This power conditioning solution may be used to compensate for line and load voltage sags as well as surges. The operating principle of this converter is similar to a dc-dc buck-boost converter. The output voltage may be controlled to regulate the load voltage to desired customer specifications by controlling the duty ratio of the IGBT switches employed in the converter. This topology is simple to construct and as such very suitable for commercial implementation, but the major disadvantage for practical realization is the voltage rating of the power semiconductor devices employed in the converter structure, which is the summation of input and output voltage. It may be noted that this document presents a new topology of ac-ac buck-boost converter with center-point-clamping technique which reduces the voltage stress on the devices to half the summation of input and output voltage.

3. Chapter Three: Principle of Center-Point-Clamping

3.1. Introduction

This chapter introduces a single stage direct ac-ac power conversion technique based on center-point-clamped ac-ac direct power converter topology. It demonstrates a method to reduce the voltage blocking requirements of the power semiconductor switches, by clamping the device blocking voltage to half the input source voltage. This approach of center-point-clamping allows the utilization of lower voltage rated power devices for higher voltage rating utility grid. The following section presents a brief overview of the evolution of ac-ac direct power converter circuits, which serves as motivation for the center-point-clamped direct ac-ac power converter topology.

3.2. Motivation for Center-Point-Clamped AC-AC Converter

As already presented in Section 1.6, an ac-ac direct power converter is a competitive candidate in keeping this as a low-cost solution with high system reliability. But there are difficulties associated with scaling them to utility level voltages and power that have been a critical issue in their widespread acceptance in the industry. Challenges faced when operating at high voltage and power levels are due to the high voltage blocking and high current carrying capability that the semiconductor devices are required to handle.

Commercially available 1700V/1200A Insulated Gate Bipolar Transistors (IGBTs) that are low cost have been a workhorse for industrial applications operating at $480V_{line\text{-}line}$ [2]. These devices operate with relatively high switching frequencies. However the use of these devices at distribution voltage levels in the range of 4.16kV – 13.8kV becomes challenging. Specifically, the phase-neutral peak voltage in a $4.16kV_{line\text{-}line}$ system is 3.4kV. To ensure

that devices work reliably within their Safe Operating Area (SOA), it is required to employ either a 6.6kV IGBT or a series connection of two 3.3kV devices for this application. Because of lack of widely available 6.6kV devices, alternative has been to employ series connection of 3.3kV IGBTs. This increases complexity and cost of system due to issues associated with static and dynamic voltage sharing of series connected IGBTs [7]. With the presented center-point-clamped ac-ac converter topology, it may be seen that one can reliably design a power conditioning solution for 4.16kV applications that uses 3.3kV IGBTs.

3.3. Evolution of Center-Point-Clamped AC-AC Converter

This sub-section discusses briefly about evolution of the concept of center-point-clamping.

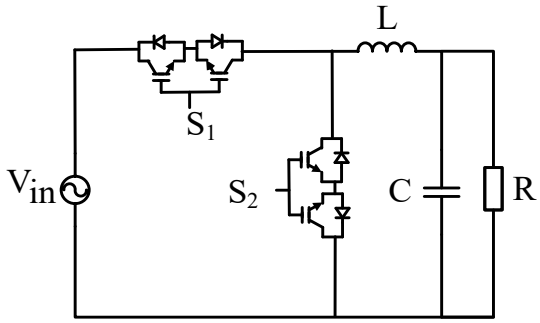


Figure 3-1: Simplified circuit schematic of the ac-ac buck converter.

As may be seen from Figure 3-1, it represents an ac-ac buck converter with two bi-directional switches, S_1 and S_2. Each of this bi-directional switch operates in a complementary fashion to generate a switched ac output waveform. This switched ac voltage is then applied across the load through a low-pass filter which filters out the high frequency switching component and generates a sinusoidal ac waveform at fundamental

frequency. It may be noted that the source voltage is impressed across each bi-directional switch when they are in operating in voltage blocking mode. To reduce the voltage stress on the devices, a series connection of two bi-directional switches is employed. This enables the utilization of low voltage rated power semiconductor devices for designing a converter system that may be used in a higher voltage grid. Figure 3-2 shows the schematic of an ac-ac converter with series connected bi-directional switches. As may be seen from Figure 3-2, the upper rail has series-connected bidirectional switches S_1 and S_4, whereas switches S_2 and S_3 are connected in shunt across the load. It may be seen that when switches S_1, S_4, and, S_2, S_3 are operated in complementary fashion, input voltage is impressed upon them. But since S_1 and S_4 or S_2 and S_3 are series connected, they are expected to share the input voltage equally amongst each other and as such the voltage stress on each switch is reduced to half of input voltage.

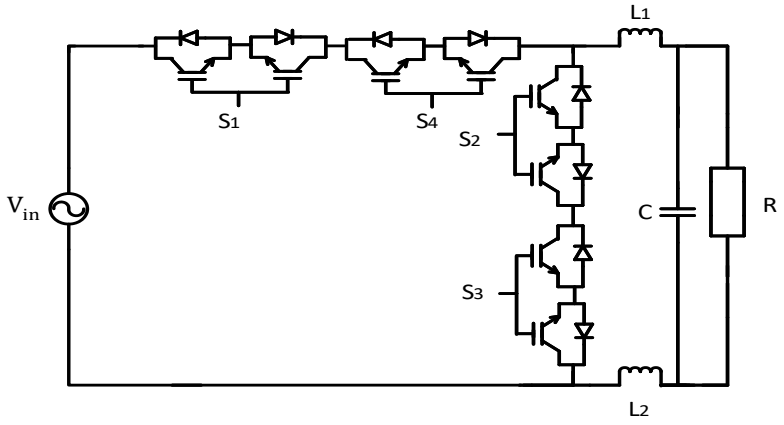


Figure 3-2: Simplified circuit schematic of the ac-ac converter with series connected IGBTs.

The switches S_1, S_4, and, S_2, S_3 are rearranged in such a way that the circuit topology appears more symmetric but maintaining the voltage stress across each switch to half of input source voltage. The converter structure is displayed in Figure 3-3.

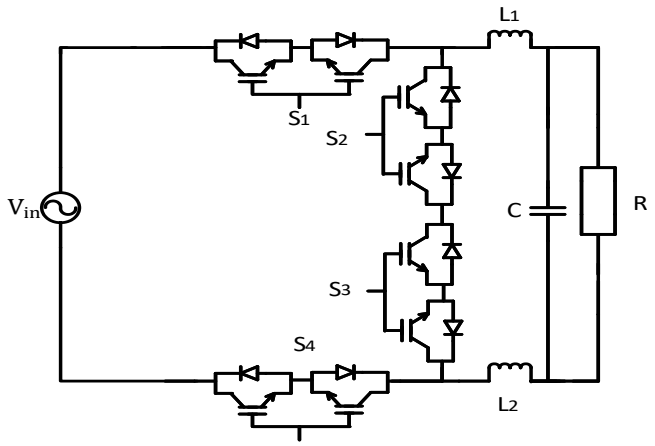


Figure 3-3: Simplified circuit schematic of the ac-ac converter with series connected IGBTs in a symmetrical configuration.

As may be seen from Figure 3-3, the switches S_1 and S_4 are operated in alternate switching cycles as compared to S_2 and S_3. As is well-known, it is challenging to ensure that the voltages across two series connected devices are distributed evenly during steady state and dynamic conditions. Now, to ensure equal distribution of voltages across all four bi-directional switches under all operating conditions, a center-point is constructed on the source side with two capacitors and is tied to the mid-point between switches S_2 and S_3. This arrangement leads to design of center-point-clamped ac-ac converter topology, as shown in Figure 3-4.

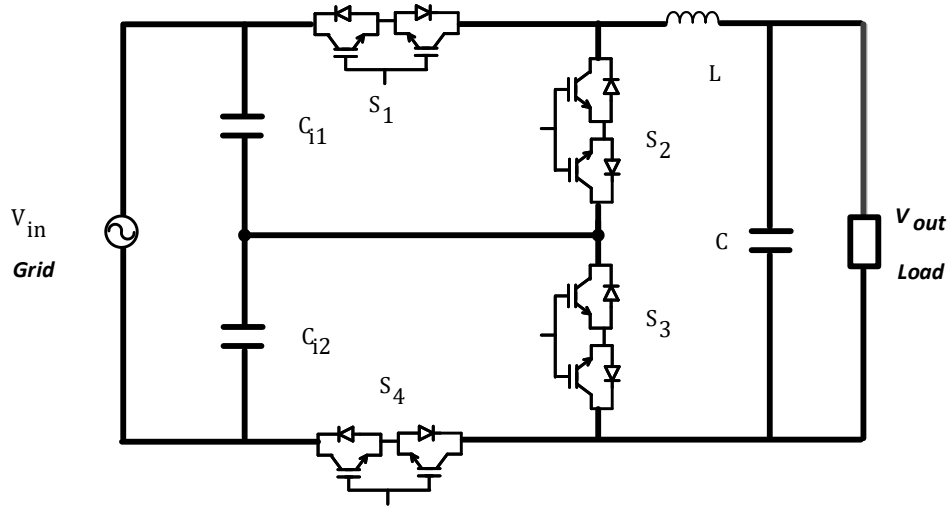


Figure 3-4: Simplified circuit schematic of the center-point-clamped ac-ac buck converter.

3.4. Center-Point-Clamped AC-AC Buck Converter

This section discusses the operating principle of the CPC ac-ac buck converter and presents results supporting the methodology of center-point-clamping

3.4.1. Hardware Circuit Configuration

This section refers to the hardware circuit configuration as shown in Figure 3-4. The converter has two input capacitors, C_{i1} and C_{i2}, which provide access to the center-point of the input voltage, V_{in} at the junction of the two-capacitor connection. There are 4 bi-directional switches employed in the circuit, each comprising of two IGBTs with anti-parallel diodes, connected in common emitter configuration. Switch S_1 and S_2 are connected in series with the line voltage, whereas Switch S_3 and S_4 are connected across the L-C filter. The junction of switches S_2 and S_3 are tied to the junction of the two input capacitors to provide access to the center-point voltage at the output. The output L-C filter is followed by a load, whose voltage is represented as v_{out}.

3.4.2. Operating Principle

Table 3-1: Switching principle of center-point-clamped ac-ac buck converter

Command v_{out} (desired output)	**between 0 and $v_{in}/2$**	**between $v_{in}/2$ and v_{in}**
State 1	S_2 S_3 closed S_1 S_4 open	S_1 S_4 closed S_2 S_3 open
State 2	S_2 S_4 closed S_1 S_3 open	S_2 S_4 closed S_1 S_3 open
State 3	S_2 S_3 closed S_1 S_4 open	S_1 S_4 closed S_2 S_3 open
State 4	S_1 S_3 closed S_2 S_4 open	S_1 S_3 closed S_2 S_4 open

The operating principle of this center-point-clamped ac-ac converter can be thought of as similar to neutral-point-clamped dc-ac inverter [58] in the sense that output can be clamped to the center point of the input. However, instead of generating three 'dc' levels at the pole output ($-V_{dc}/2$, 0, $+V_{dc}/2$) as obtained in a conventional neutral-point-clamped inverter, ability to realize three distinct 'differential ac' outputs is the key point that distinguishes this topology. It may be observed from Table 3-1, that when switches S_1, S_4 are closed and switches S_2, S_3 are open, resultant output voltage is equal to input voltage v_{in}. However, because the mid-point between switches S_2 and S_3 is tied to center point on the source, the distribution of voltage between these two open switches S_2 and S_3 is identical and is equal to $v_{in}/2$. Similarly, when switches S_2, S_3 are closed and switches S_1, S_4 are open, the resultant output voltage is zero (0). Again, the distribution of voltage between two open

switches S_1 and S_4 is identical and is equal to $v_{in}/2$ because of clamp to the center point. Finally, when switches S_1 and S_3 are closed, the resultant output voltage is half the input voltage i.e. $v_{in}/2$. It may be noted that another combination with switches S_2 and S_4 closed gives the same result of voltage $v_{in}/2$ across the load. However, the difference between these two operating conditions is the capacitor that gets connected to the load. Similar to the classical neutral-point-clamped dc-ac inverter [58], these two states are alternately employed so as to evenly balance the voltages across the two capacitors.

3.4.3. Capacitor Voltage Balancing

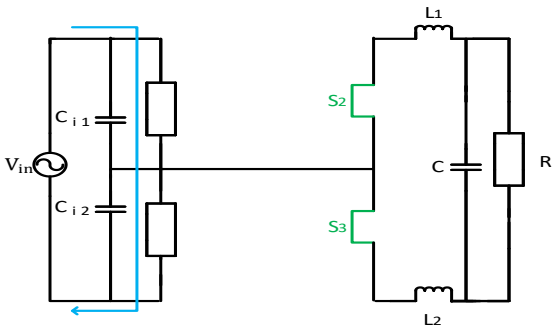


Figure 3-5: Simplified circuit schematic of the converter during states 1, 3 of switching sequence when command v_{oref} is between 0 and $v_{in}/2$.

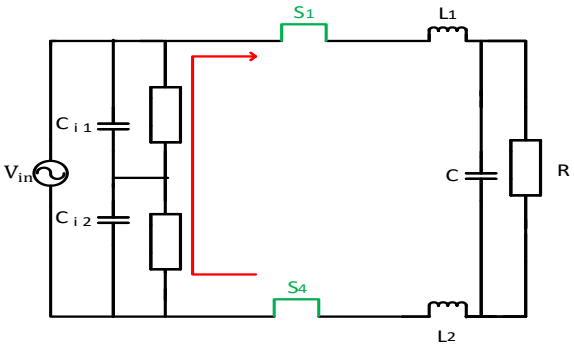


Figure 3-6: Simplified circuit schematic of the converter during states 1, 3 of switching sequence when command v_{oref} is between $v_{in}/2$ and v_{in}.

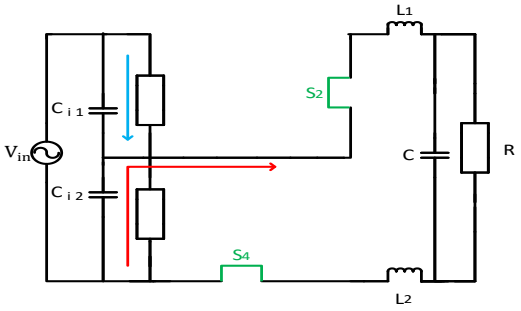


Figure 3-7: Simplified circuit schematic of the converter during state 2.

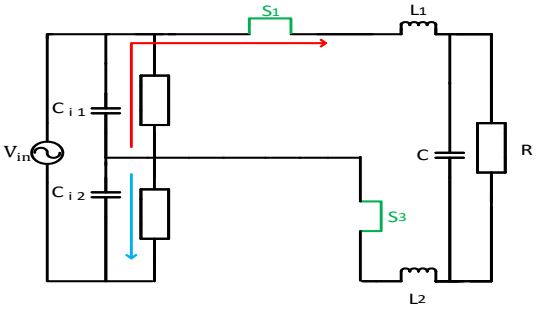


Figure 3-8: Simplified circuit schematic of the converter during state 4.

As may be seen from the switching pattern in Table 1, when switches S_2 and S_3 are closed and opened to achieve zero output voltage level and voltage level v_{in} respectively, capacitors C_{i1} and C_{i2} get charged equally. This is shown in Figure 3-5 and Figure 3-6.

In order to achieve output voltage $v_{in}/2$ in State 2, switches S_2 and S_4 are closed as displayed in Figure 3-7. This results in discharging of C_{i2} and charging of C_{i1}. Similarly, for State 4, instead of closing S_2 and S_4 to get $v_{in}/2$, we close S_1 and S_3 as shown in Figure 3-8. Thus, in this state C_{i1} gets discharged whereas C_{i2} gets charged. This alternate charging and discharging sequence of capacitors C_{i1} and C_{i2} ensures input capacitor voltage balancing. Also, the resistors connected in parallel with the input capacitors serve as a voltage divider circuit to provide the center-point voltage at the junction of the two capacitors.

3.4.4. Verification Results and Discussions

The converter topology as may be seen from Figure 3-4 is modelled using Matlab-Simulink for v_{in} =120V_{rms}. The simulation results from the designed model are presented in this sub-section which verify the operation methodology of a center-point-clamped ac-ac buck converter as discussed in subsections (3.2.2) and (3.2.3).

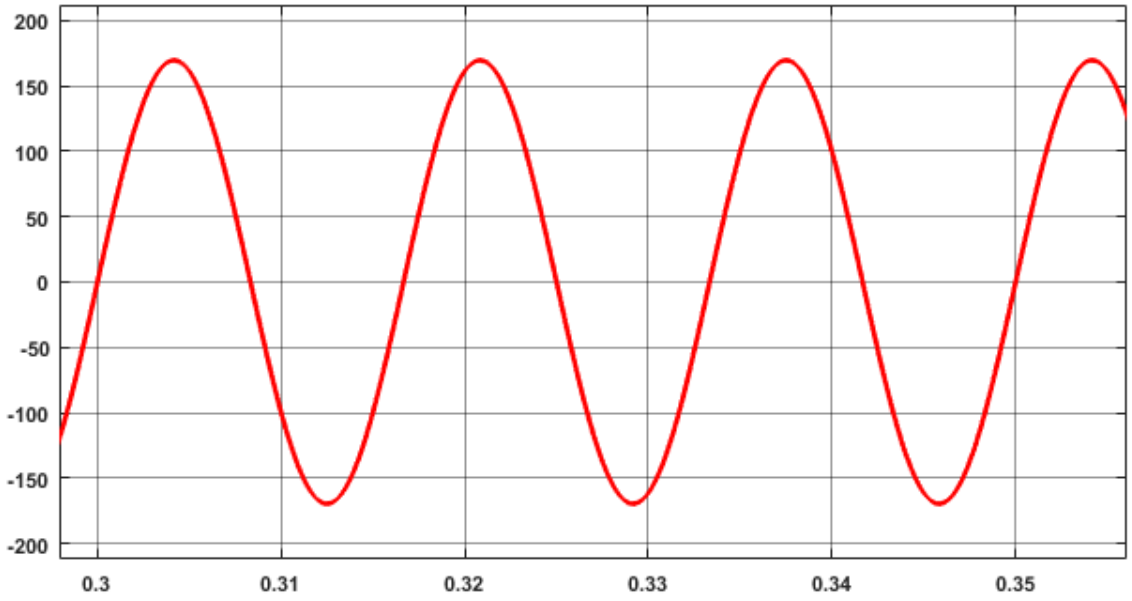


Figure 3-9: Input source voltage applied to CPC ac-ac buck converter.

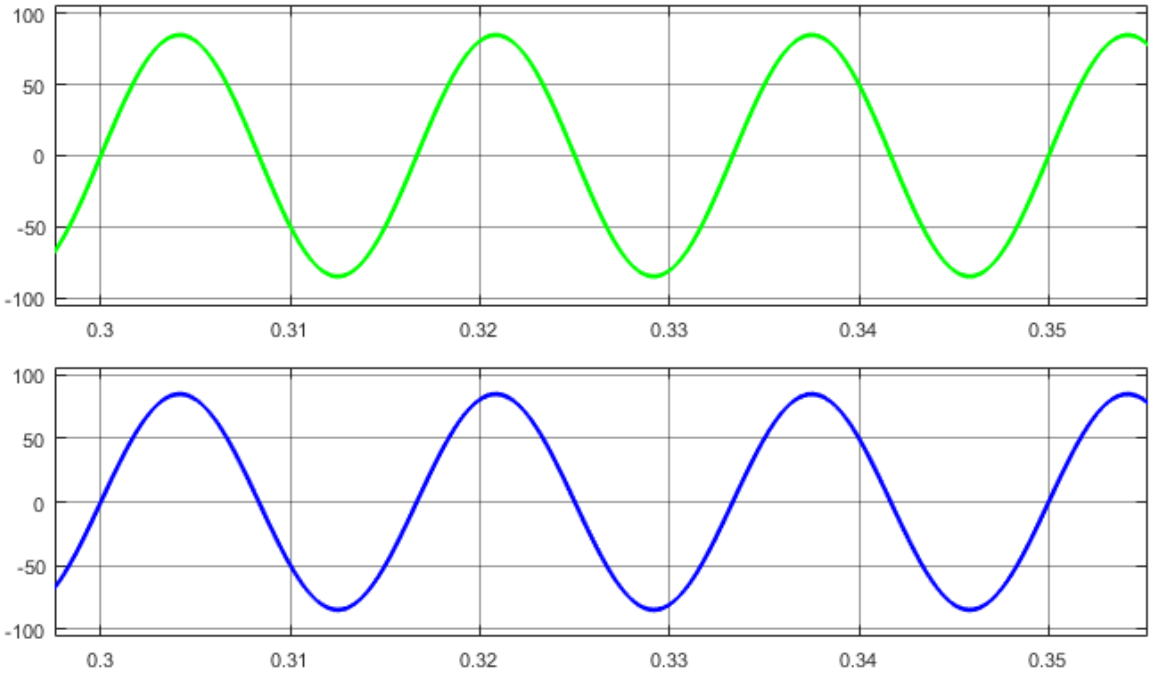


Figure 3-10: Voltage across the two input capacitors, C_{i1} and C_{i2}

It may be seen from Figure 3-9 and Figure 3-10, that for a source voltage of $120V_{acrms}$, the input capacitor, C_{i1} and the input capacitor, C_{i2} has an ac voltage of $60V_{acrms}$, which is an

equal distribution of source voltage and are clamped to center-point of the input voltage. This validates technique of capacitor voltage balancing as discussed in sub-section (3.2.3).

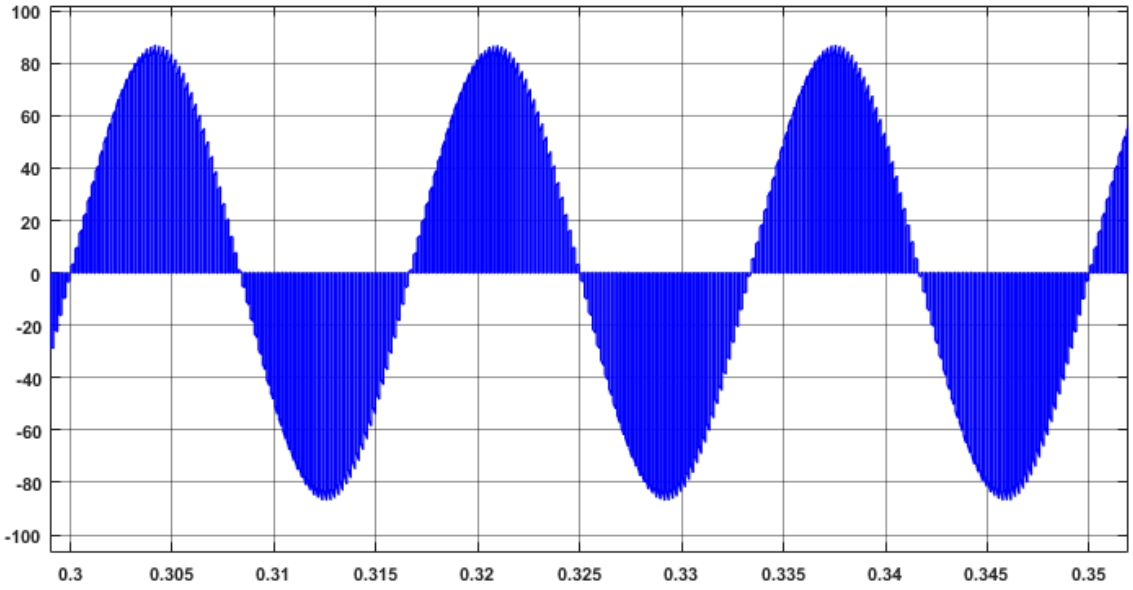


Figure 3-11: Voltage stress across each bi-directional switch S_1, S_2, S_3 and S_4.

Next, it may be observed from Figure 3-11, that the peak voltage stress across each bi-directional is $85V_{acpeak}$, which is equal to half of peak input source voltage, $170V_{acpeak}$. This demonstrates the reduction in voltage stress across each bi-directional switch due to center-point-clamping technique. Furthermore, the output voltage reference command, v_{oref} has been changed to demonstrate an output voltage corresponding to a duty ratio of 0.3 and 0.8, which verifies the working principle of two different switching sequence based on whether the desired output voltage is between 0 to $v_{in}/2$ or, $v_{in}/2$ to v_{in}. The waveforms pertaining to the two regions of operation, as may be seen from Table 3-1, are shown in Figure 3-12 and Figure 3-13.

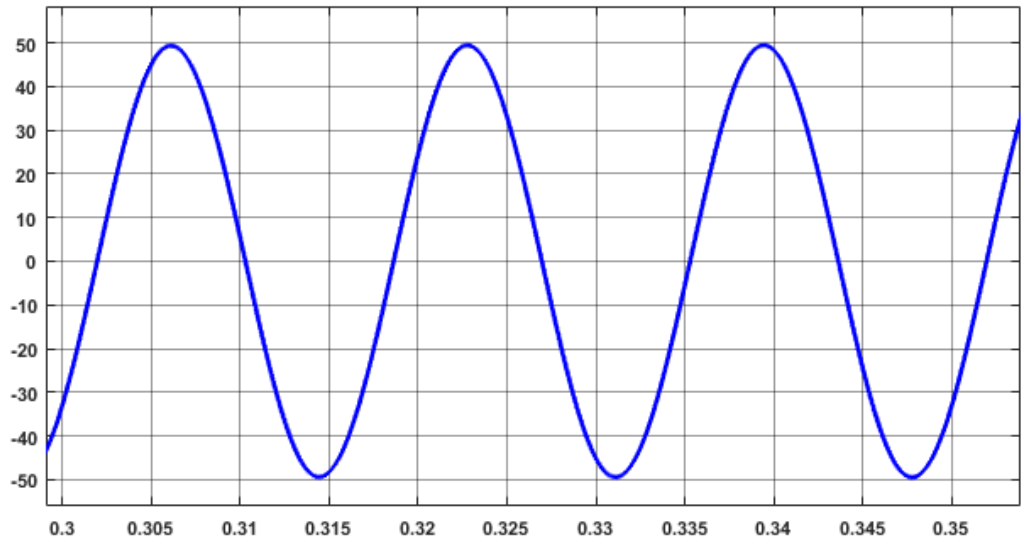


Figure 3-12: Output voltage of CPC ac-ac buck converter for duty ratio of 0.3.

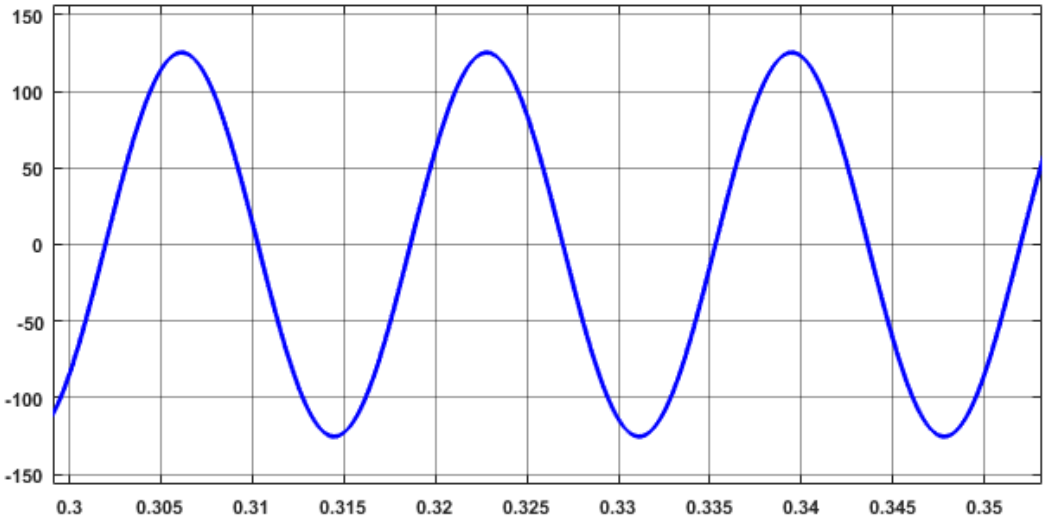


Figure 3-13: Output voltage of CPC ac-ac buck converter for duty ratio of 0.8.

For further verification, a laboratory prototype of a single-phase center-point-clamped ac-ac buck converter has been constructed and tested for v_{in} =120-V_{rms}. The experimental waveforms are presented here to confirm the operation methodology of a center-point-clamped ac-ac buck converter. The input source voltage waveform for the CPC ac-ac buck converter is shown in Figure 3-14.

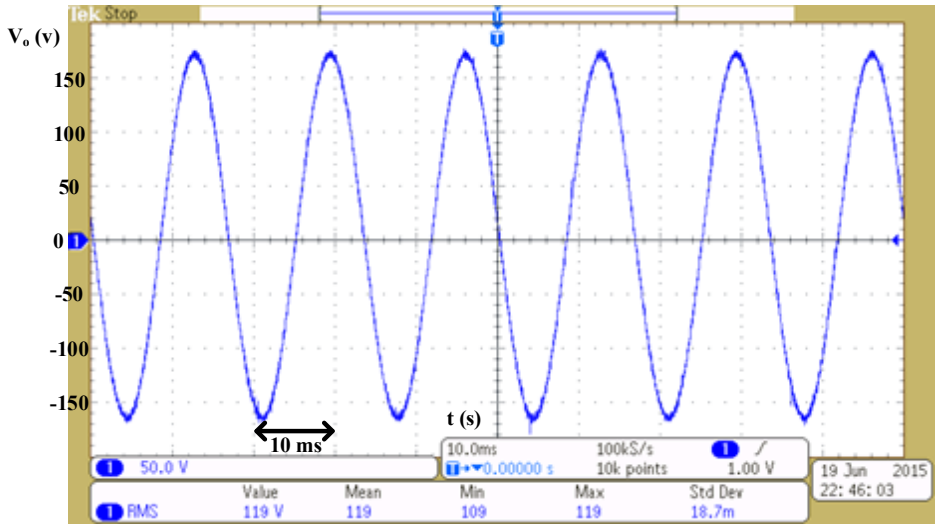


Figure 3-14: Input source voltage of CPC ac-ac buck converter

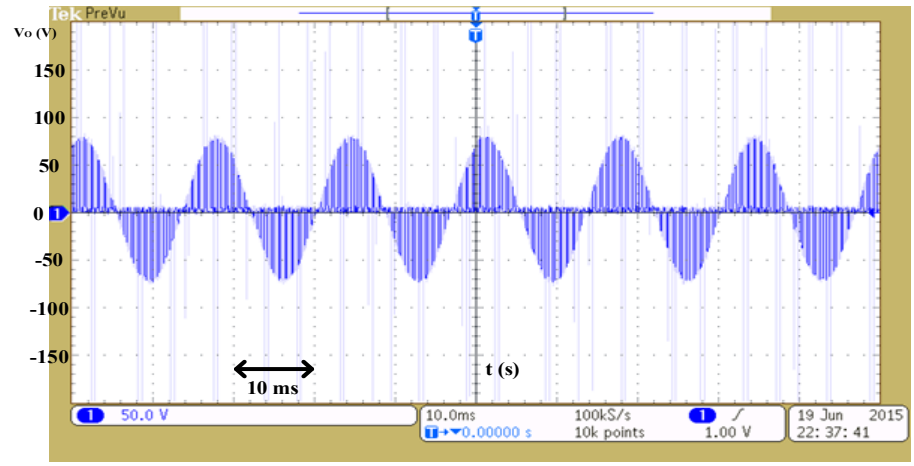


Figure 3-15: Voltage stress across each bi-directional switch, S_1, S_2, S_3 and S_4.

As may be seen from Figure 3-15, the blocking voltage impressed upon each bi-directional switch has a peak amplitude of $85V_{acpeak}$. This verifies the utilization of bi-directional switches rated at lower voltages using center-point-clamping for a system exceeding the power semiconductor device voltage ratings.

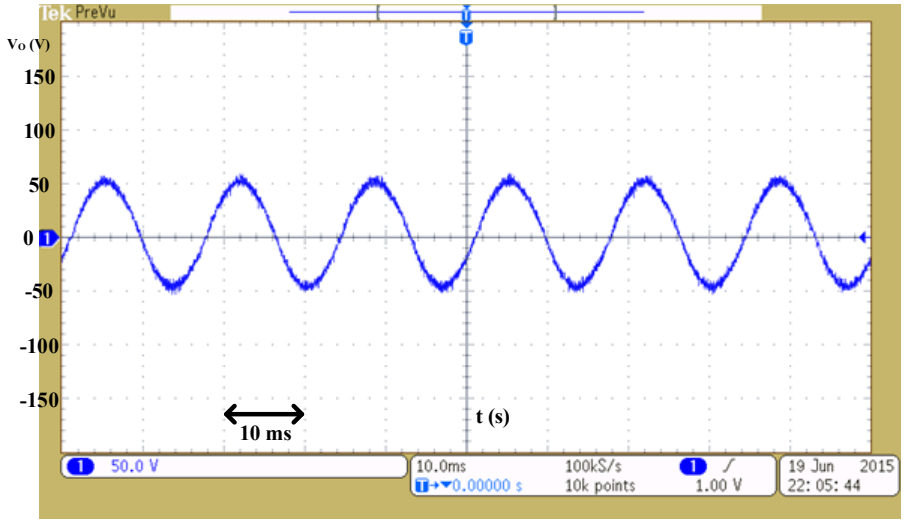


Figure 3-16: Output voltage of CPC ac-ac buck converter for duty ratio of 0.3.

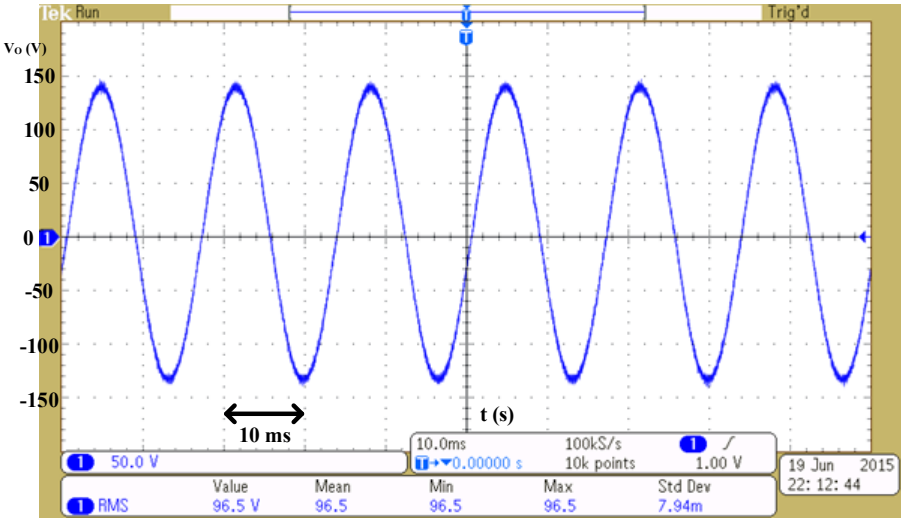


Figure 3-17: Output voltage of CPC ac-ac buck converter for duty ratio of 0.8.

Figure 3-16 and Figure 3-17 verify the buck-operation the center-point-clamped ac-ac converter using the switching principle presented in Table 3-1.

3.5. Center-Point-Clamped AC-AC 1-Ø Buck-Boost Converter

This section discusses the operating principle of the CPC ac-ac 1-Ø buck-boost converter and presents results supporting the methodology of center-point-clamping.

3.5.1. Hardware Circuit Configuration

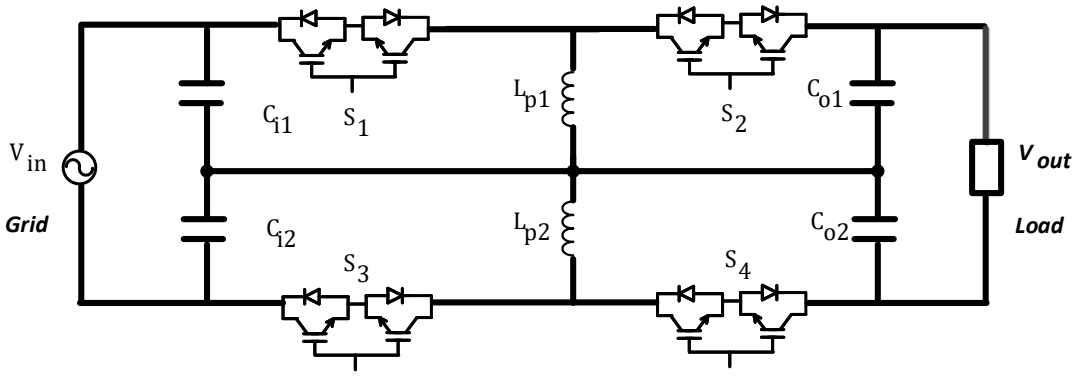


Figure 3-18: Simplified circuit schematic of the center-point-clamped ac-ac buck-boost converter.

The hardware circuit design to realize a CPC buck-boost converter may be derived from the cpc buck converter presented in Figure 3-4, is shown in Figure 3-18. There are two input side capacitors, C_{i1} and C_{i2}, connected across input voltage to provide access to the center-point-voltage at the junction of two capacitors. There are 4 bi-directional switches in this circuit configuration, two in series with the input voltage, S_1 and S_3 and two in series with the output voltage, S_2 and S_4. There are two buck-boost inductors, L_{p1} and L_{p2} connected in series across the junction of S_1, S_2 and S_3, S_4. The junction of the two inductors is connected to the junction of the two capacitors to access the input source mid-point voltage. At the output side of converter, there are two capacitors, C_{o1} and C_{o2} connected in series across the load, which provides access to the center-point of the load voltage. The junction of C_{o1} and C_{o2} are connected to the junction of the buck-boost inductors to complete the circuit of CPC buck-boost converter.

3.5.2. Operating Principle

Table 3-2: Switching principle of center-point-clamped ac-ac buck-boost converter

Command v_{out} (desired output)	**between v_{in} and $n.v_{in}$**
State 1	S_1 S_3 closed S_2 S_4 open
State 2	S_2 S_4 closed S_1 S_3 open

The center-point clamped ac-ac buck-boost converter structure uses four bidirectional switches S_1, S_2, S_3, and S_4. It may be observed from Table 3-2, when switches S_1, S_4 are closed and switches S_2, S_3 are open, resultant input voltage gets impressed upon the energy transferring inductors, L_{p1} and L_{p2}. However, because the center-point on the two buck-boost inductors is tied to the mid-point of the load voltage, distribution of voltage between the two open switches S_2 and S_3 is identical and is equal to $\frac{v_{in}+ v_{out}}{2}$. Similarly, when switches S_2, S_3 are closed and switches S_1, S_4 are open, the energy in the inductors get transferred to the load. Again, the distribution of voltage between two open switches S_1 and S_4 is identical and is equal to $\frac{v_{in}+ v_{out}}{2}$ because of clamp at the center-point of the source.

3.5.3. Verification Results and Discussions

The CPC ac-ac buck-boost converter as shown in Figure 3-18, is modelled in Matlab-Simulink to verify its working principle. As may be seen from Figure 3-19, the input source voltage applied to the converter is $120V_{acrms}$.

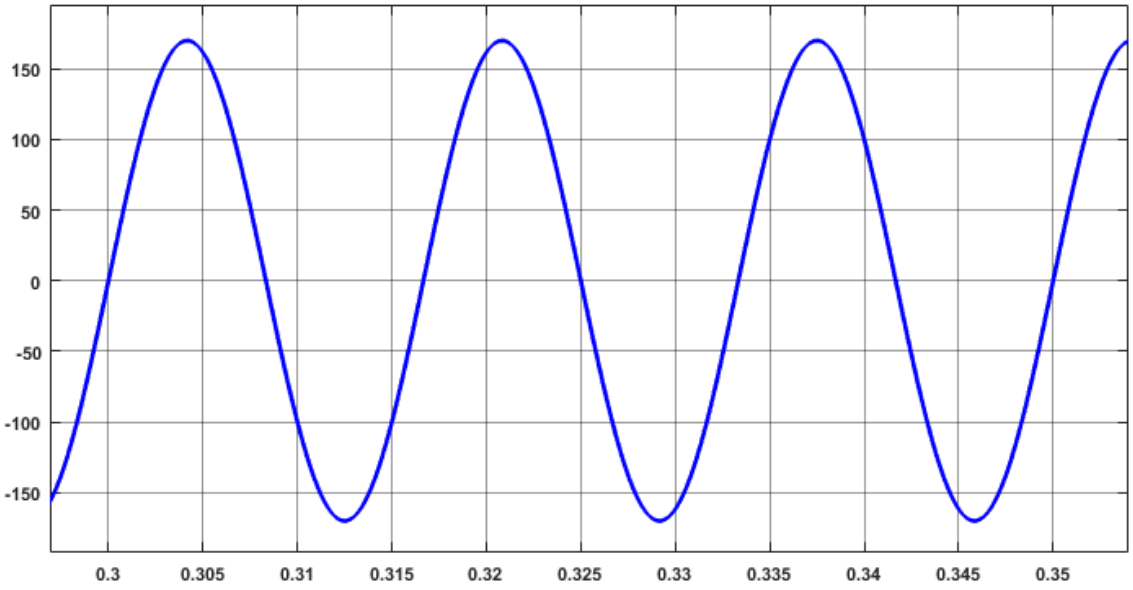


Figure 3-19: Input source voltage of center-point-clamped ac-ac buck-boost converter

It has been discussed in the principle that input capacitors equally distribute the line voltage across each other, thereby displaying a voltage of $60V_{acrms}$, which is equal to half of the input voltage. The two input capacitor voltages are shown in Figure 3-20. It may also be seen from Figure 3-21 that the voltage stress across each bi-directional switch in the converter topology is half the summation of input and output voltage, which is equal to $170V_{acpeak}$. This demonstrates the reduction in voltage stress on each bi-directional switch due to center-point-clamping.

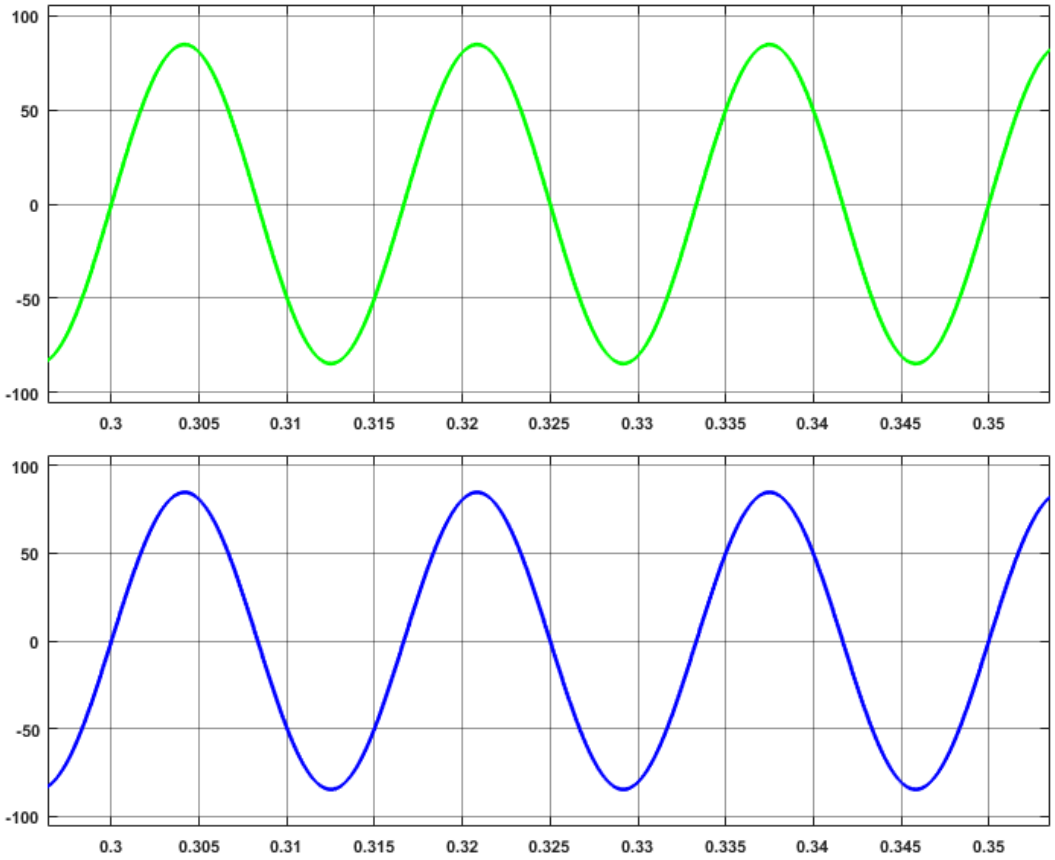


Figure 3-20: Voltage across the two input capacitors, C_{i1} (green) and C_{i2} (blue).

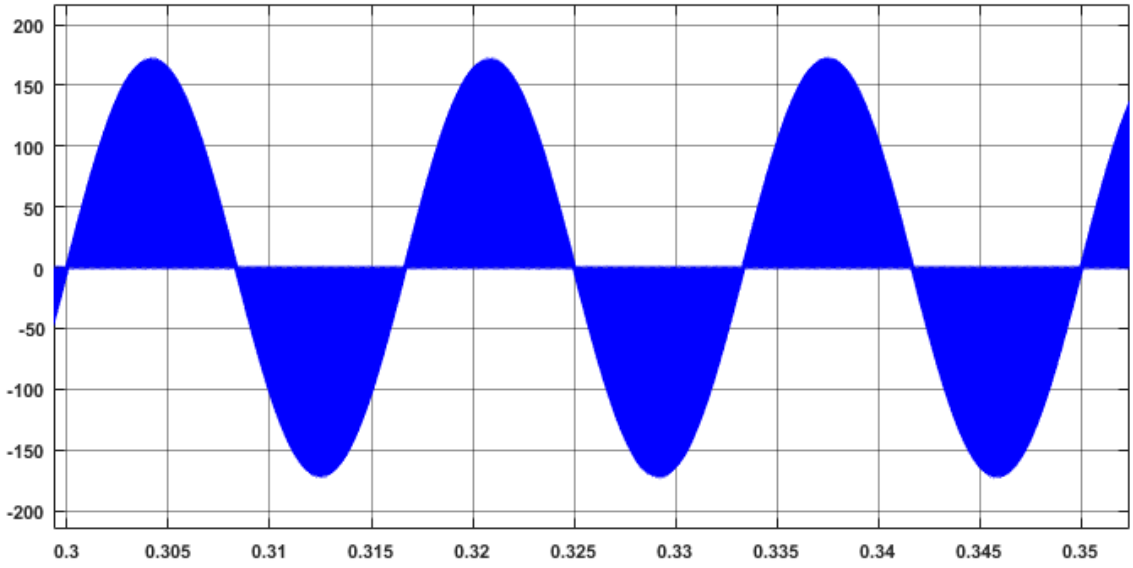


Figure 3-21: Voltage stress across each bi-directional switch S_1, S_2, S_3 and S_4.

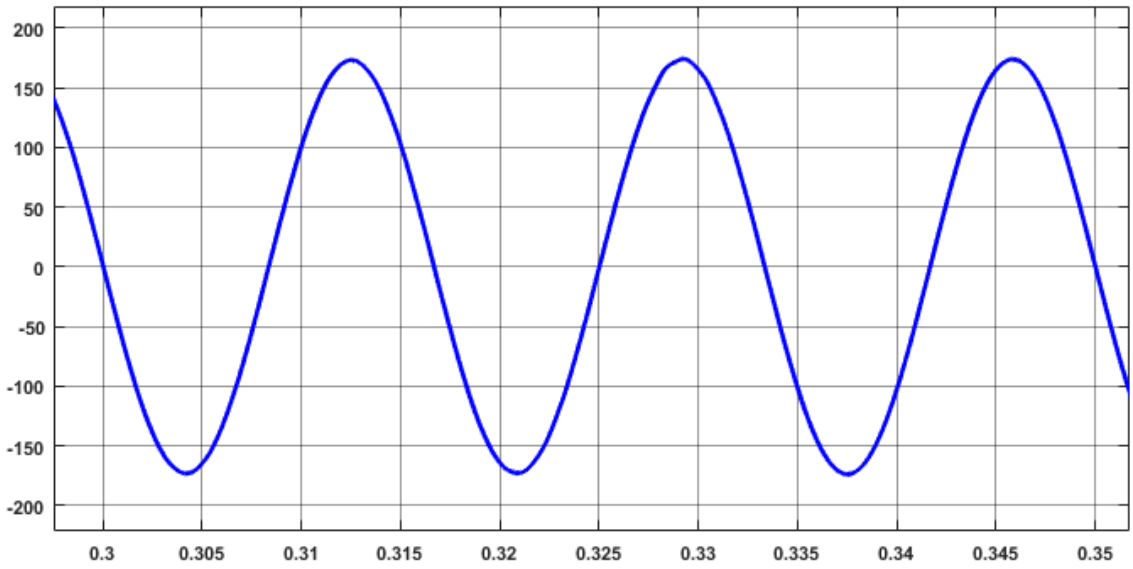


Figure 3-22: Output voltage of CPC ac-ac buck converter for duty ratio of 0.5.

It may be observed from Figure 3-22, that output voltage of the converter for a duty ratio of 0.5 is equal to $120V_{acrms}$. It may also be noted from output voltage waveform that the switching harmonics introduced to input voltage by the converter have been filtered out. Furthermore, an experiment prototype has been constructed for verification of operation methodology of the converter topology. The experimental results are presented in the following figures.

As may be seen from Figure 3-23, source voltage (yellow) is $120V_{acrms}$, and the bi-directional switch voltage stress (green) has a peak of $85V_{acpeak}$. This demonstrates the principle of center-point-clamping which reduces the blocking voltage of the device to the center-point of input voltage.

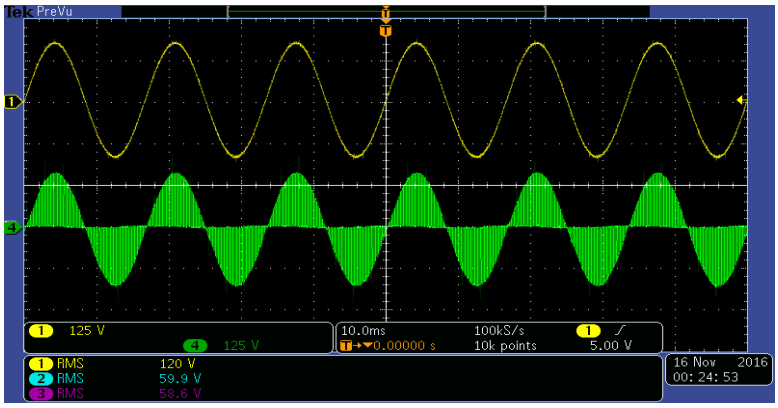


Figure 3-23: Input Voltage (yellow) and Voltage Stress on a bi-directional switch (green) of CPC ac-ac buck-boost converter

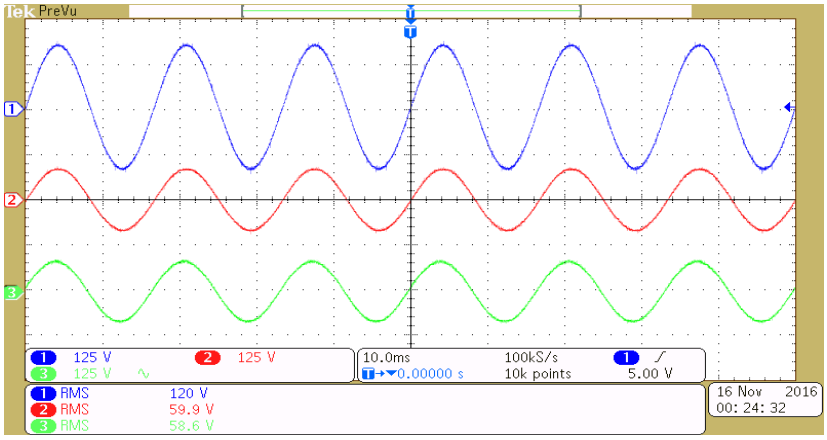


Figure 3-24: Input Voltage (blue), Input Capacitor 1 voltage (red) and Input Capacitor 2 voltage (green) waveforms of CPC ac-ac buck-boost converter.

It may further be seen from Figure 3-24, that the method of capacitor voltage balancing is also implemented as both the input capacitors are equally balanced at the center-point of source voltage at about $60V_{acrms}$.

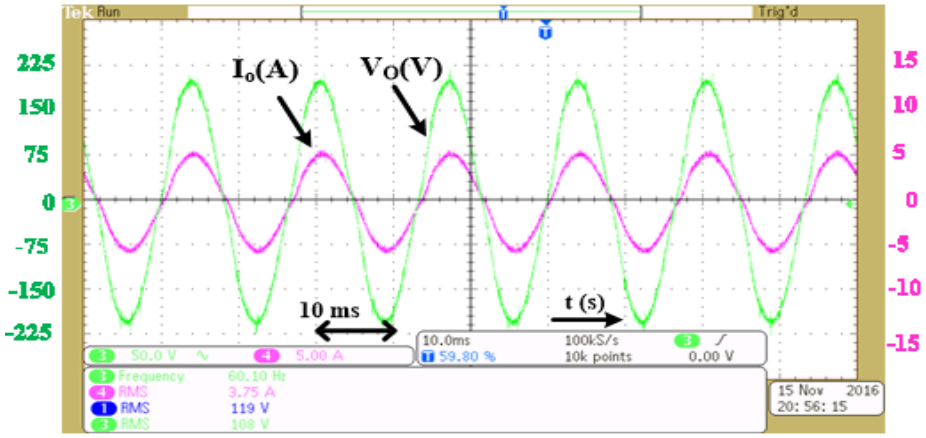


Figure 3-25: Output voltage (green) and output current (purple) waveform for a duty ratio of 0.5.

The output voltage waveform has a magnitude of $120V_{acrms}$, which corresponds to a duty ratio of 0.5. It may be seen that the experimental prototype waveform has minimal harmonic distortion as the switching harmonics have been filtered out.

Thus, we may conclude from the above results that the simulation results obtained from the experimental results provided from the laboratory prototype of the converter topology closely follow the converter model in Matlab-Simulink. These results also verify the working principle of the converter discussed in sub-section 3.4.2. Therefore, center-point-clamping technique has been successfully employed to derive a 1-Ø ac-ac buck-boost converter. The next sub-section will discuss the design of a 3-Ø CPC ac-ac buck-boost converter for 3-Ø power line applications.

3.6. Center-Point-Clamped AC-AC 3-Ø Buck-Boost Converter

This section discusses the operating principle of final topology of CPC ac-ac 3-Ø buck-boost converter and presents results supporting the methodology of center-point-clamping.

3.6.1. Circuit Configuration

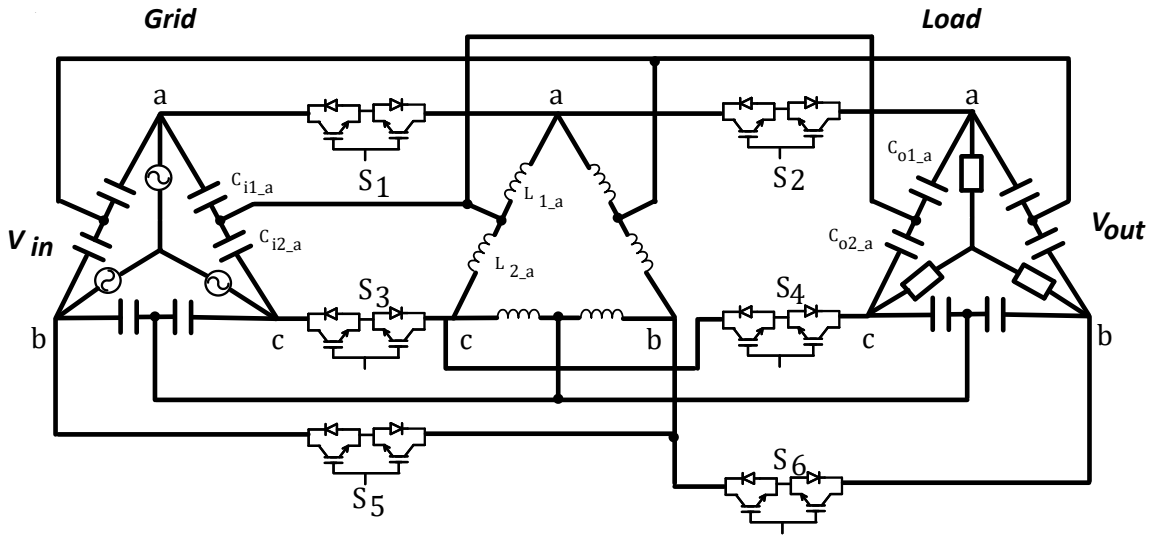


Figure 3-26: Simplified circuit schematic of the final topology of 3-Ø center-point-clamped ac-ac buck-boost converter.

As may be seen from Figure 3-26, the center-point-clamped ac-ac buck-boost converter has one bi-directional switch in each phase connection at the input and output side between input side capacitors, buck-boost inductors, and output side capacitors. Each bi-directional switch is comprised of two IGBTs connected in common emitter configuration. The converter has six bi-directional switches, S_1, S_2, S_3, S_4, S_5 and S_6. There are two series-connected capacitors, C_{i1_a} and C_{i2_a} in parallel across phase a and b. Thus, the center-point of input source voltage may be accessed at the junction of the two input capacitors. This center-point is then connected to the junction of two series connected buck-boost inductors across phase a and b. The center-point connection does not have any switch in this topology. To access the center-point voltage for the output side, there are two

capacitors connected in series across phase a and b. The junction of the two output capacitors is connected to connected to the junction of the two buck-boost inductors to reduce the voltage stress across the output bi-directional switches to the output side-center-point voltage. The input side capacitors, buck-boost inductors and output capacitors are all connected in delta configuration for the 3-Ø connection. It may be seen in the results section that voltage stress across the bi-directional switches in this topology is equal to $\frac{v_{in}+ v_{out}}{2}$. This topology has been selected for further analysis in the following chapters of this thesis and a hardware prototype has been built based on this converter structure to verify the operating principles and efficacy of the converter features.

3.6.2. Operating Principle

Table 3-3: Switching principle of center-point-clamped ac-ac buck-boost converter

Command v_{out} (desired output)	**between v_{in} and $n.v_{in}$**
State 1	S_1 S_3 S_5 closed S_2 S_4 S_6 open
State 2	S_2 S_4 S_6 closed S_1 S_3 S_5 open

This topology of center-point clamped 3-Ø ac-ac buck-boost converter structure uses six bidirectional switches S_1, S_2, S_3, S_4, S_5 and S_6. It may be observed from Table 3-3, when switches S_1, S_3, S_5 are closed and switches S_2, S_4, S_6 are open, resultant input voltage gets impressed upon the energy transferring inductors, L_{p1} and L_{p2}. However, because the center point on the two buck-boost inductors is tied to the mid-point of the load voltage,

distribution of voltage between the two open switches S_1, S_3 across phase a and b is identical and is equal to $\frac{v_{in}+ v_{out}}{2}$. Similarly, when switches S_2, S_4 are closed and switches S_1, S_3 are open, the energy in the inductors get transferred to the load. Again, the distribution of voltage between two open switches S_1 and S_3 is identical and is equal to $\frac{v_{in}+ v_{out}}{2}$ because of clamp at the center-point of the source. It may also be seen from the results presented in following sub-section that the capacitor voltages are balanced.

3.6.3. Verification Results and Discussions

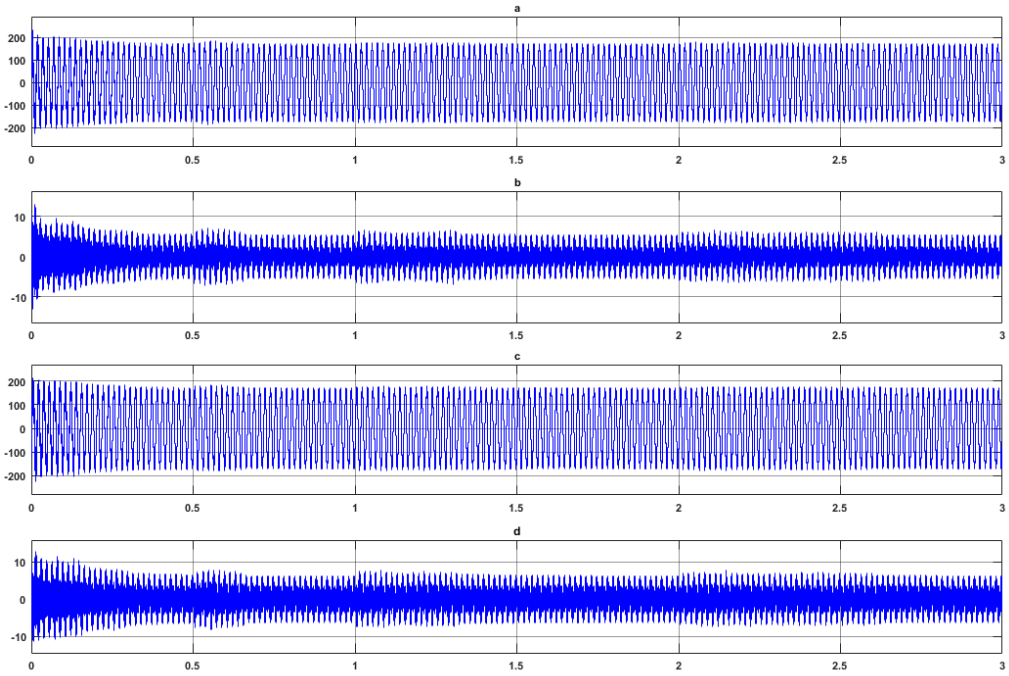


Figure 3-27: (a) Voltage across input capacitor, C_{i1_a}, (b) Current through C_{i1_a}, (c) Voltage across input capacitor, C_{i2_a}, and (d) Current through switch, C_{i2_a}.

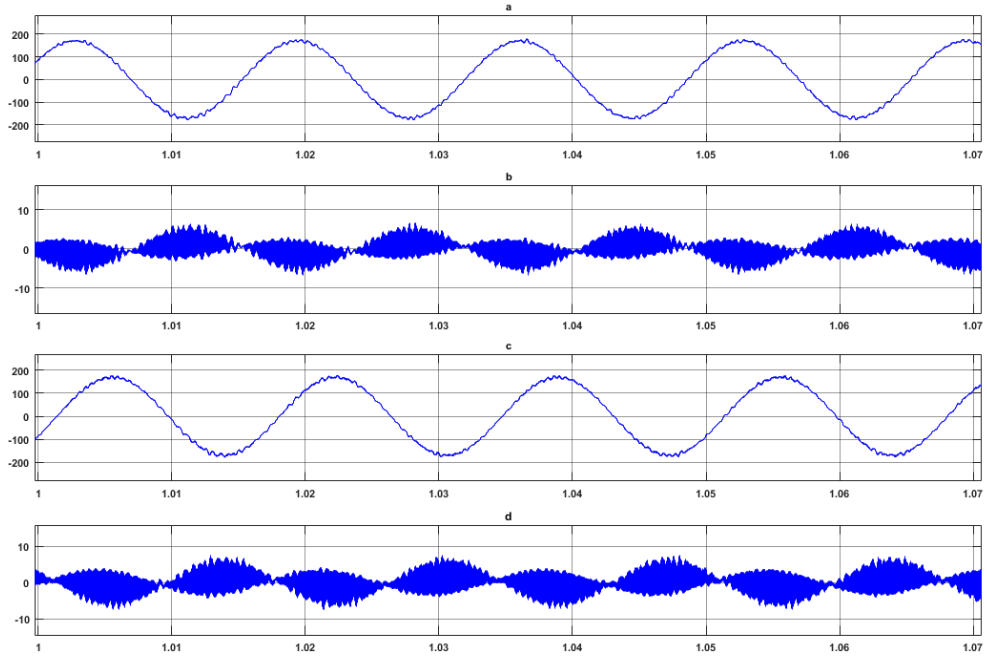


Figure 3-28: (a) Voltage across input capacitor, C_{i1_a}, (b) Current through C_{i1_a}, (c) Voltage across input capacitor, C_{i2_a}, and (d) Current through switch, C_{i2_a}.

The converter is operated according to the switching scheme displayed in Table 3-3. As may be seen from Figure 3-27 and Figure 3-28, the voltage applied across the two series connected capacitors is $\frac{v_{in}}{2}$, which shows that input source line voltage is equally distributed across two input capacitors, C_{i1_a} and C_{i2_a}. It may also be noted that the capacitor currents seem to be symmetrical in positive and negative cycle with no dc offset. But it may also be discerned that in this topology, capacitor voltages are equally balanced, and voltage stress across each of the IGBT switch is the peak of $\frac{v_{in}+ v_{out}}{2}$, which is equal to 294$V_{ac\text{-}peak}$. The voltage stress across each switch and the switched currents flowing through them are displayed in Figure 3-29 and Figure 3-30.

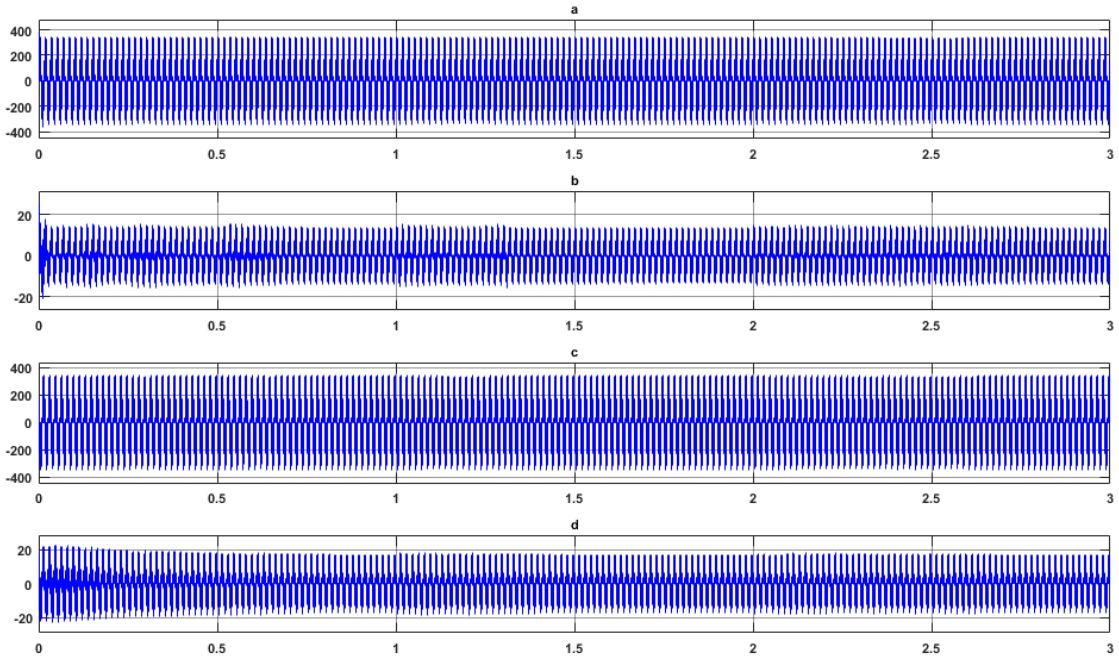


Figure 3-29: (a) Voltage across switch, S_1, (b) Current through switch, S_1, (c) Voltage across switch, S_3 and, (d) Current through switch, S_3

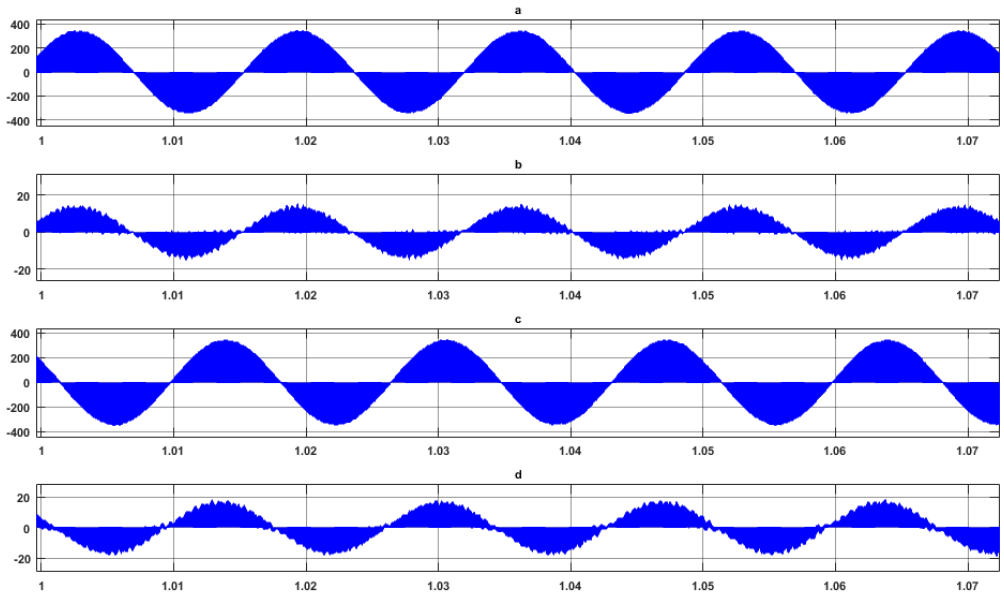


Figure 3-30: (a) Voltage across switch, S_1, (b) Current through switch, S_1, (c) Voltage across switch, S_3 and, (d) Current through switch, S_3

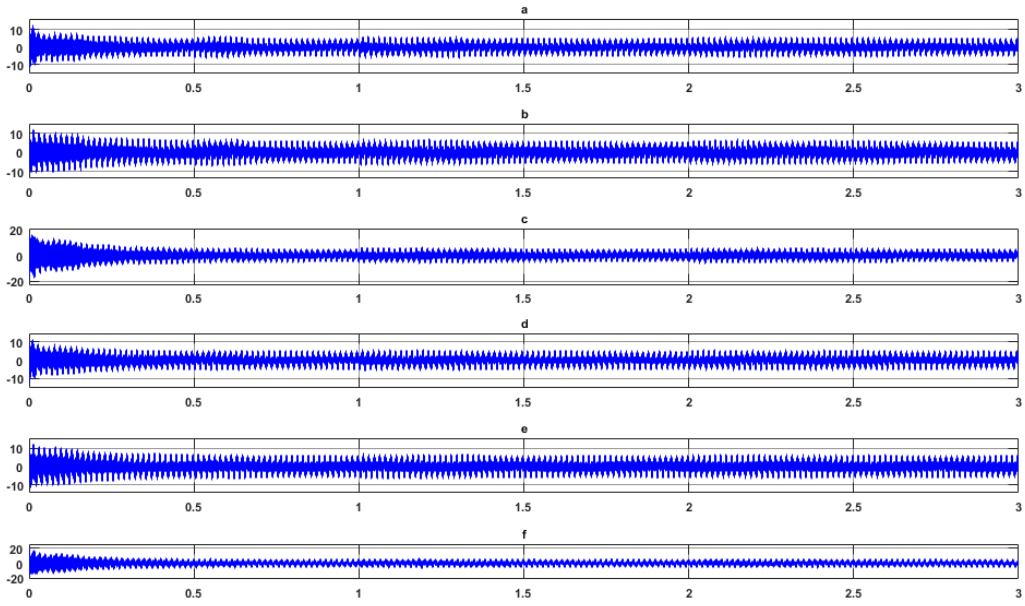


Figure 3-31: (a) Current through capacitor, C_{i1_a}, (b) Current through capacitor, C_{i2_a}, (c) Current through center-point connection between input capacitors and inductor junction, $I_{in\_centerpoint\_ab}$, (d) Current through capacitor, C_{o1_a}, (e) Current through capacitor, C_{o2_a}, (f) Current through center-point connection between output capacitors and inductor junction, $I_{out\_centerpoint\_ab}$.

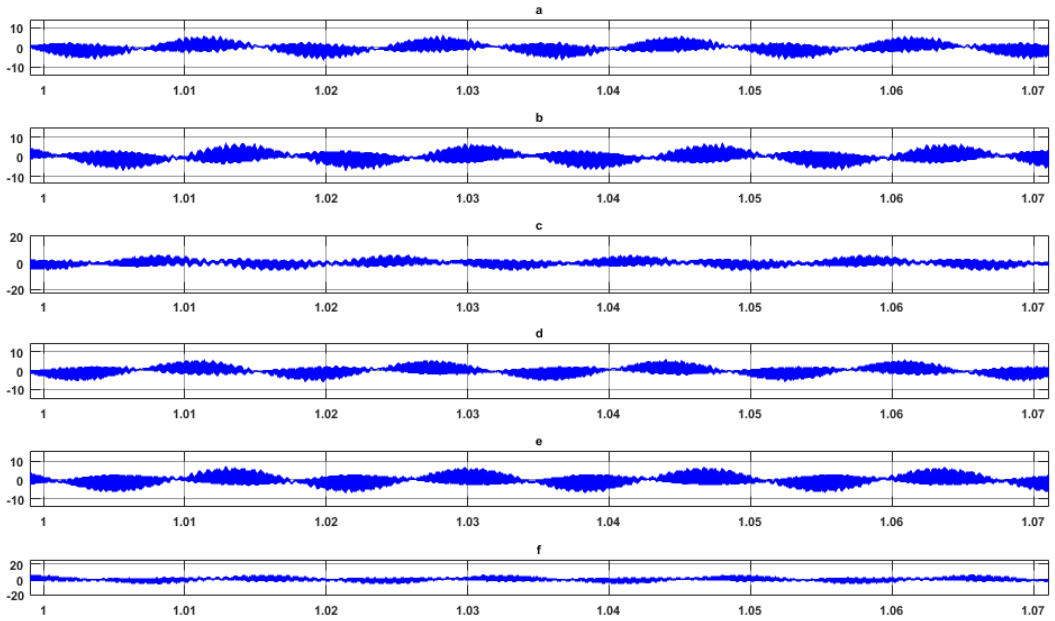


Figure 3-32: (a) Current through capacitor, C_{i1_a}, (b) Current through capacitor, C_{i2_a}, (c) Current through center-point connection between input capacitors and inductor junction, $I_{in\_centerpoint\_ab}$, (d) Current through capacitor, C_{o1_a}, (e) Current through capacitor, C_{o2_a}, (f) Current through center-point connection between output capacitors and inductor junction, $I_{out\_centerpoint\_ab}$.

As may be seen from Figure 3-31 and Figure 3-32, currents flowing through both input capacitors are in phase and equal in magnitude. It may also be noted that there is negligible current flowing through the center-point connection in this topology due to the introduction of an IGBT based switch in that connection. As regards to output side series-connected capacitors across each phase, voltages are equally balanced with their magnitude equal to the peak of $\frac{v_{in}+v_{out}}{2}$, which is $294V_{ac\text{-}peak}$. This balanced output capacitor voltage waveforms may be verified from Figure 3-33 . It may further be noted from Figure 3-33 and Figure 3-34, that currents through the two capacitors are minimal and there is negligible current flowing through the center-point connection between inductors and output capacitors.

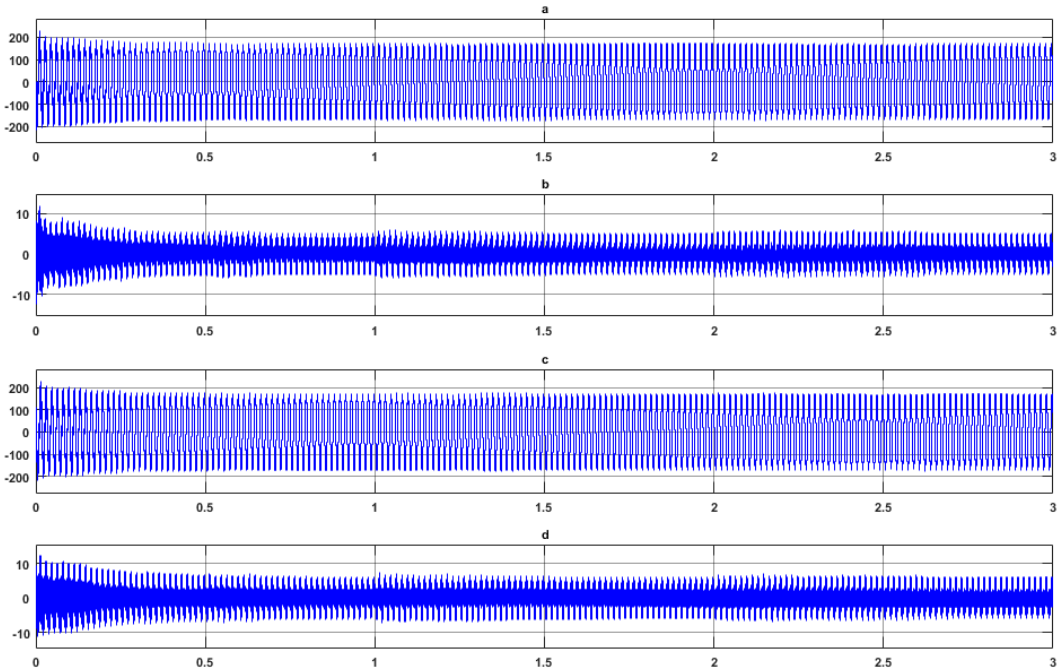


Figure 3-33: (a) Voltage across output capacitor, C_{o1_a}, (b) Current through C_{o1_a}, (c) Voltage across output capacitor, C_{o2_a} and (d) Current through switch, C_{o2_a}

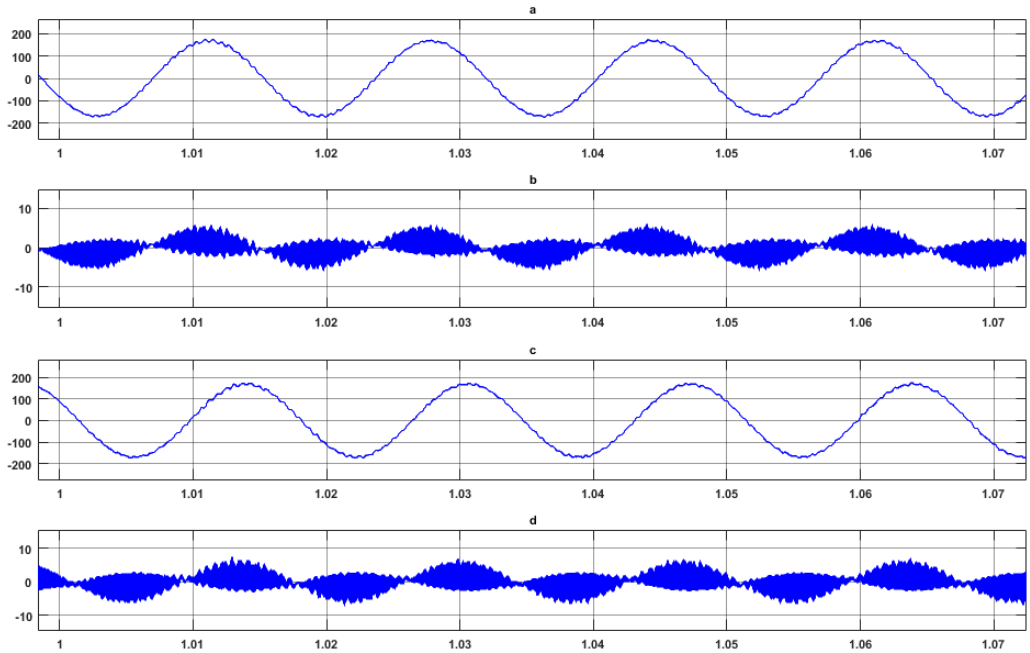


Figure 3-34: (a) Voltage across output capacitor, C_{o1_a}, (b) Current through C_{o1_a}, (c) Voltage across output capacitor, C_{o2_a} and (d) Current through switch, C_{o2_a}

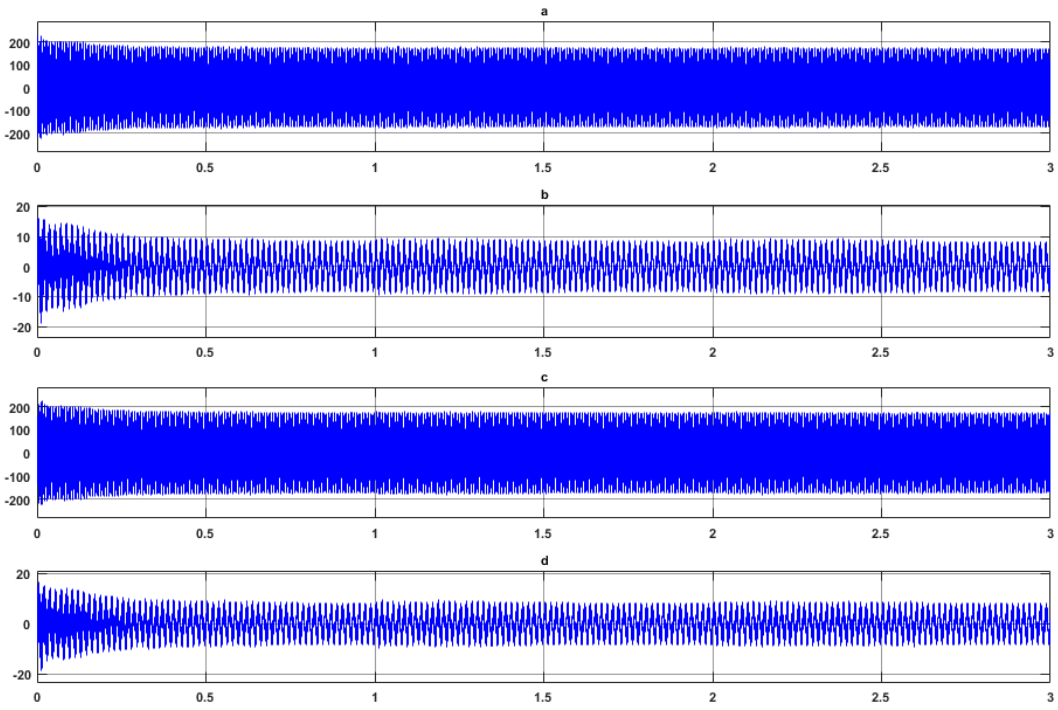


Figure 3-35: (a) Voltage across inductor, L_{1_a}, (b) Current through L_{1_a}, (c) Voltage across inductor, L_{2_a} and, (d) Current through L_{2_a}.

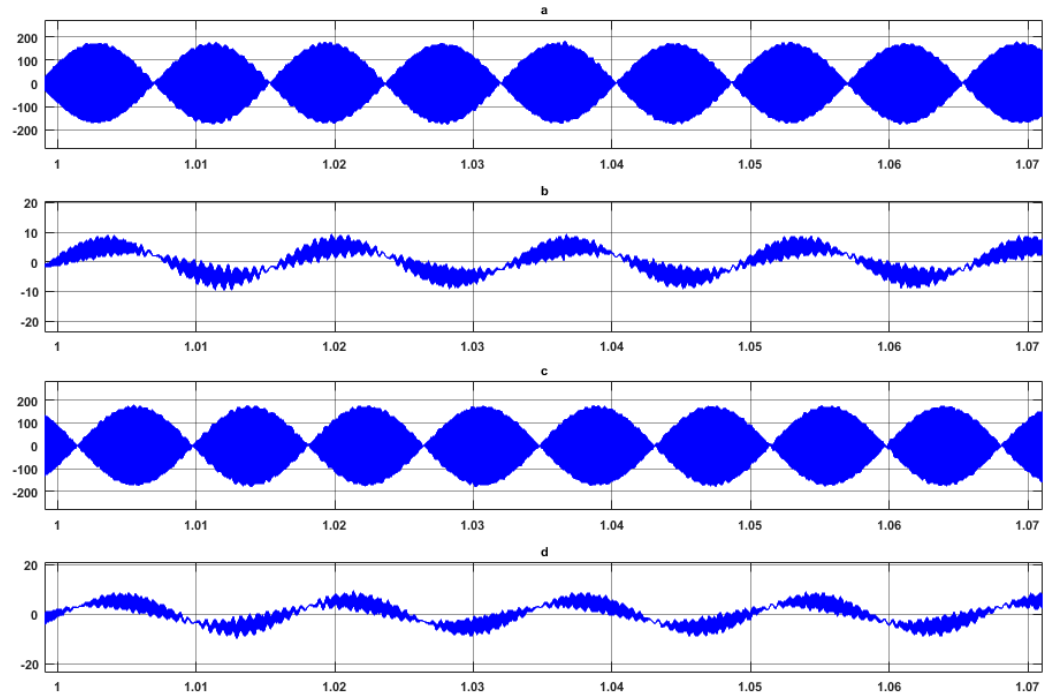


Figure 3-36: (a) Voltage across inductor, L_{1_a}, (b) Current through L_{1_a}, (c) Voltage across inductor, L_{2_a} and, (d) Current through L_{2_a}.

It may be noted that since the converter circuit represents a buck-boost topology, inductor is the medium of energy transfer between the input and the output side. During one switching instance when input switches, S_1, S_3, S_5, are closed and output switches S_2, S_4, S_6, are open, input voltage source gets applied across inductor and load side is disconnected from inductor. It may be observed during this switching instance that inductor voltage is in phase with input voltage, but during the next switching instance when input switches, S_1, S_3, S_5, are open and output switches S_2, S_4, S_6, are closed, the inductor voltage reverses, since the inductor current in order to stay continuous, starts flowing through the output switches in reverse direction as compared to the input switches. This reversal of voltage to maintain the continuity of inductor current flow makes the output voltage appear 180 degrees out of phase to input voltage in case of a buck-boost converter.

It may also be seen from Figure 3-35 and Figure 3-36, that inductor voltages are also balanced and equal to peak of $\frac{v_{in}+ v_{out}}{2}$, which is $294V_{ac\text{-}peak}$.

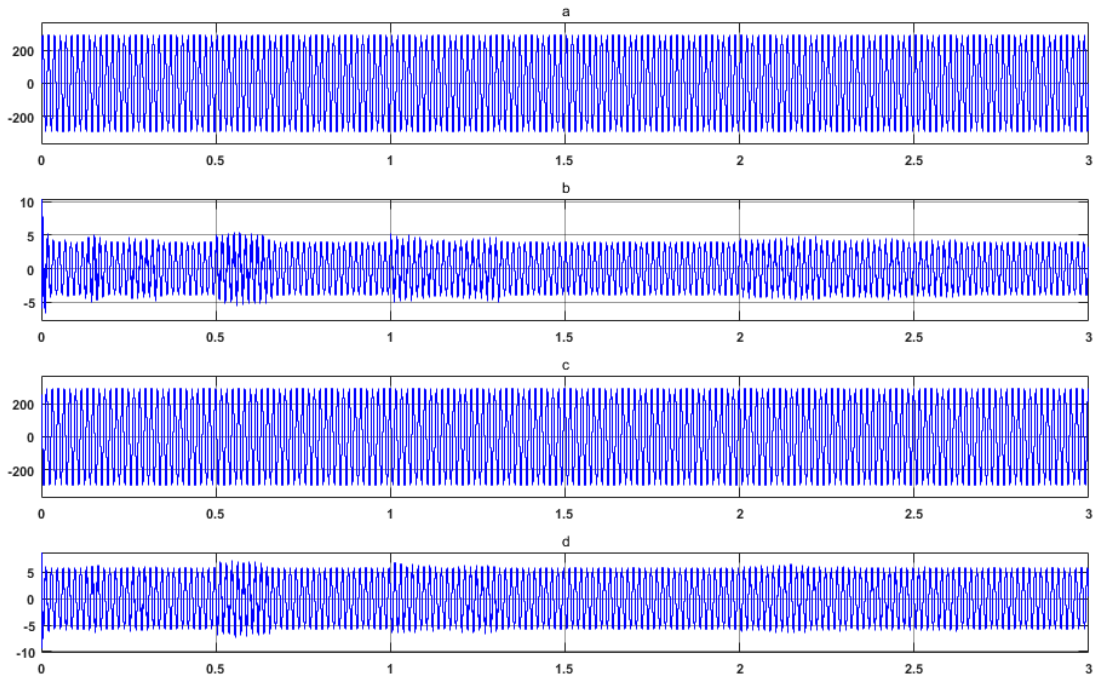


Figure 3-37: (a) Input voltage across phase ab, V_{inab}, (b) Input current through phase a, I_{ina}, (c) Input voltage across phase bc, V_{inbc}, and (d) Input current through phase b, I_{inb}.

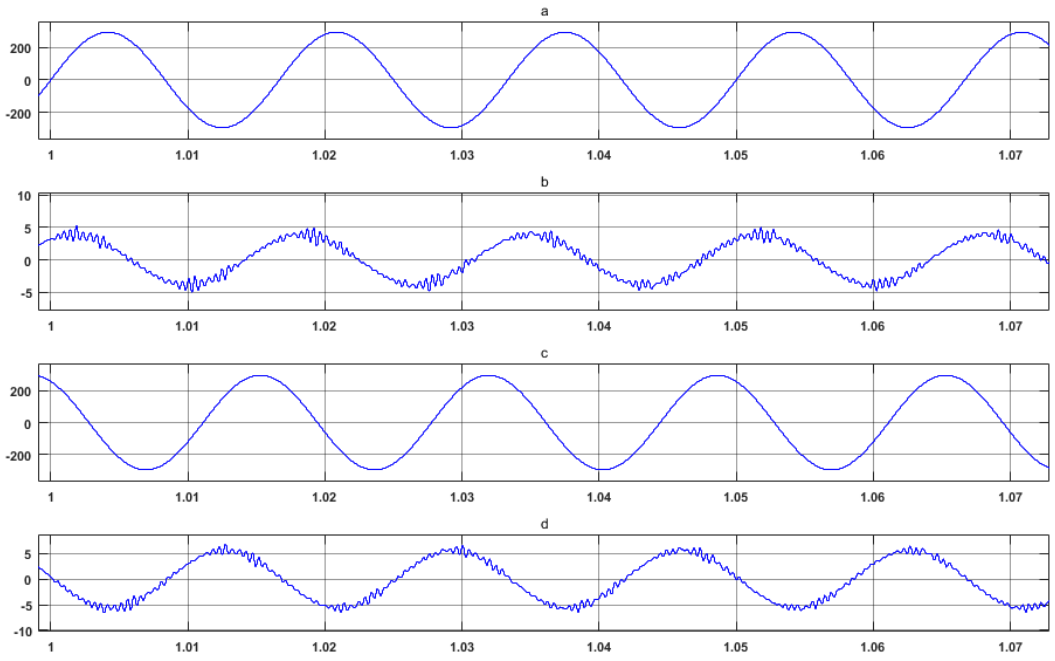


Figure 3-38: (a) Input voltage across phase ab, V_{inab}, (b) Input current through phase a, I_{ina}, (c) Input voltage across phase bc, V_{inbc}, and (d) Input current through phase b, I_{inb}.

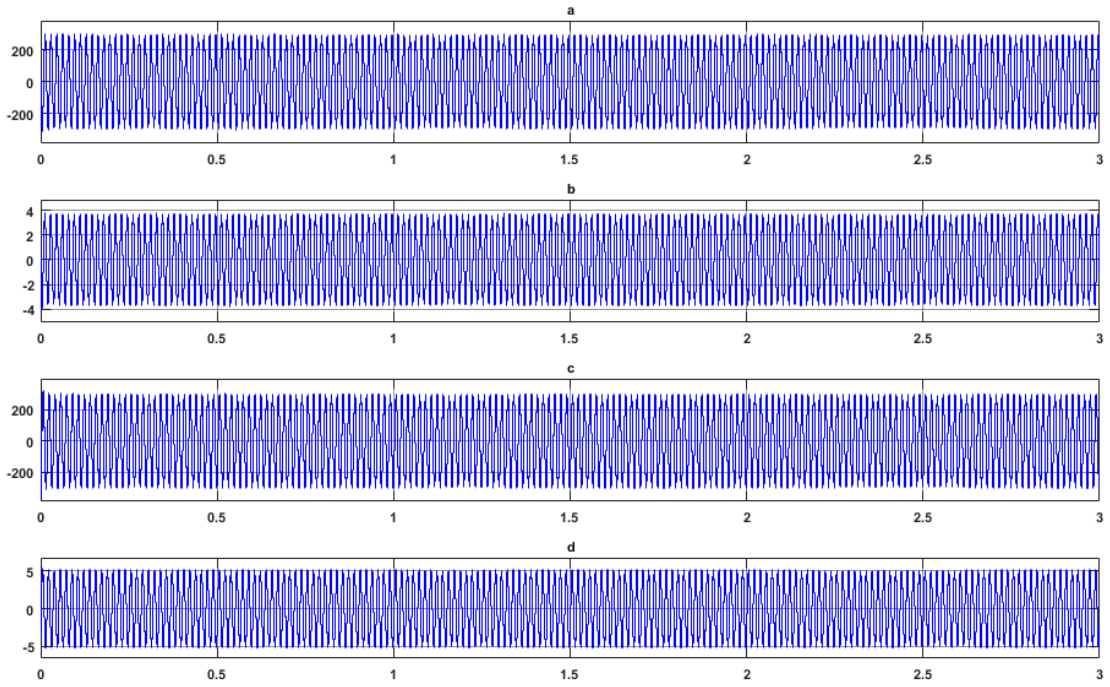


Figure 3-39: (a) Output voltage across phase ab, V_{outab}, (b) Output current through phase a, I_{outa}, (c) Output voltage across phase bc, V_{outbc}, and, (d) Output current through phase b, I_{outb}.

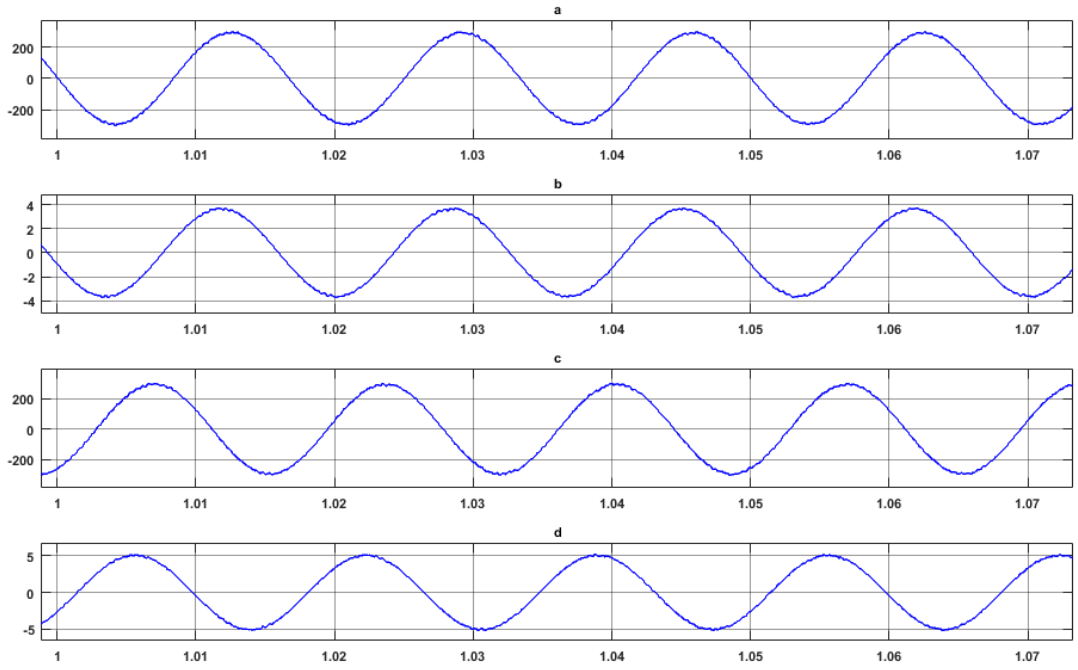


Figure 3-40: (a) Output voltage across phase ab, V_{outab}, (b) Output current through phase a, I_{outa}, (c) Output voltage across phase bc, V_{outbc}, and, (d) Output current through phase b, I_{outb}

Figure 3-37 and Figure 3-38 displays the phase a and phase b input line voltages and currents. As may be seen from the figure, the input line currents are smooth with no switching harmonics being fed back into the source which is being attenuated by the input line filter. The converter is operating at about 50% duty cycle which generates an output voltage with a rms value of $208V_{line\text{-}line}$. The output voltage and current waveforms are shown in Figure 3-39 and Figure 3-40. The output current waveform has a peak value of $4A_{acrms}$. It may be noted that the output voltage and currents are sinusoidal with minimal THD since the switching harmonics have been attenuated by the output filter.

As may be seen from Figure 3-41, both input and corresponding output line-line voltages have same magnitude and are out of phase by 180 degrees since it is a buck-boost converter. Also, it may be noted that each phase of either three phase input or output voltages are phase shifted by 120 degrees.

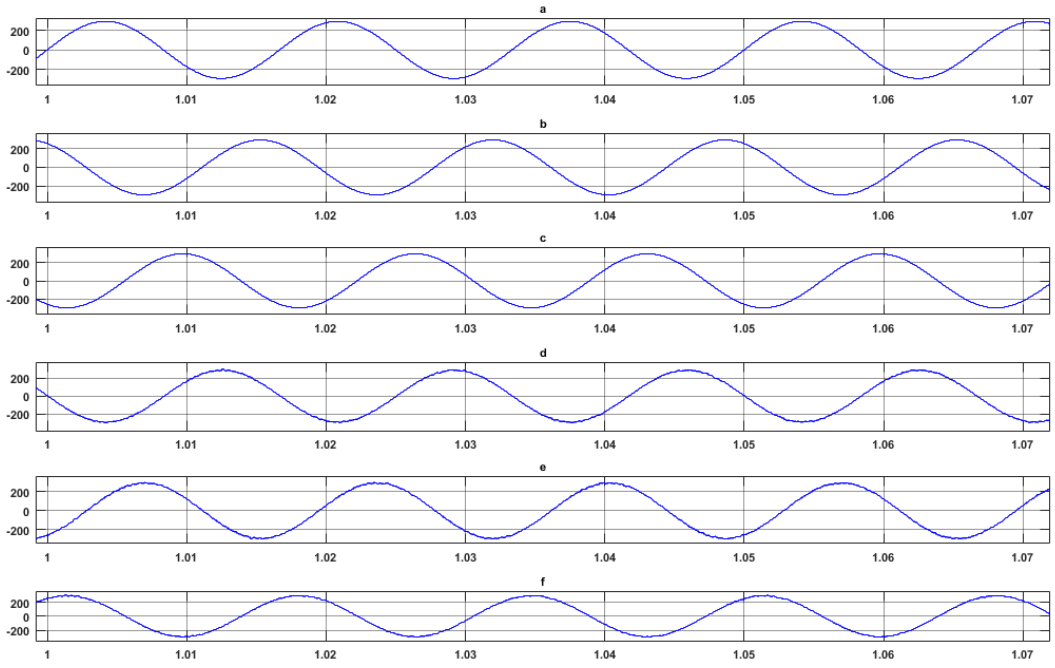


Figure 3-41: (a) Input Voltage across phase ab, V_{inab}, (b) Input voltage across phase bc, V_{inbc}, (c) Input Voltage across phase ca, V_{inca}, (c) Output voltage across phase ab, V_{outab}, (d) Output voltage across phase bc, V_{outbc}, (e) Output voltage across phase ca, V_{outca}.

3.6.4. Center-Point-Clamped 3-Ø Power Line Conditioner

An ac power line conditioner is required to regulate the output voltage to a desired value, irrespective of the input source voltage [59]. It may be noted that the 3-Ø CPC ac-ac buck-boost converter may also be utilized to regulate the output voltage, irrespective of the input source voltage through duty ratio control of the modulation signal applied to each bi-directional switch.

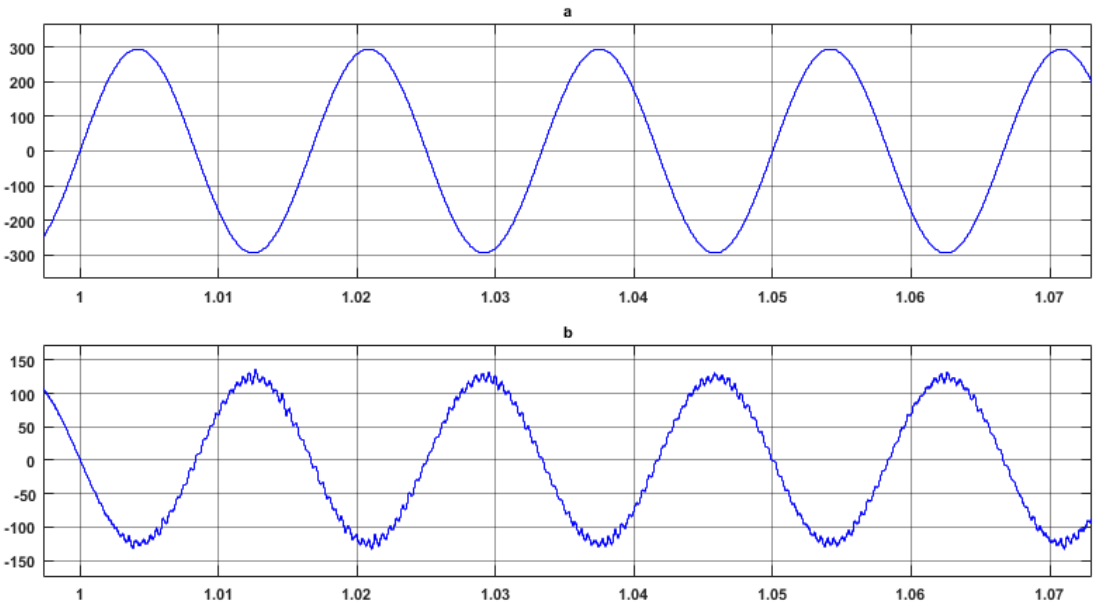


Figure 3-42: (a) Input source voltage, and (b) output voltage, for a duty ratio of 0.3.

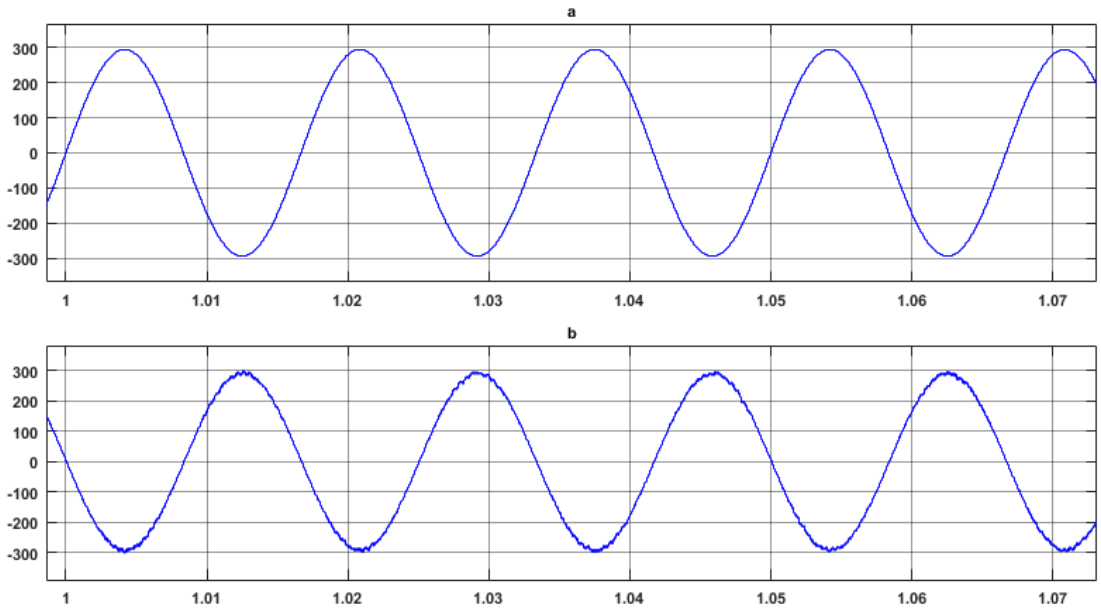


Figure 3-43: (a) Input source voltage, and (b) output voltage, for a duty ratio of 0.5.

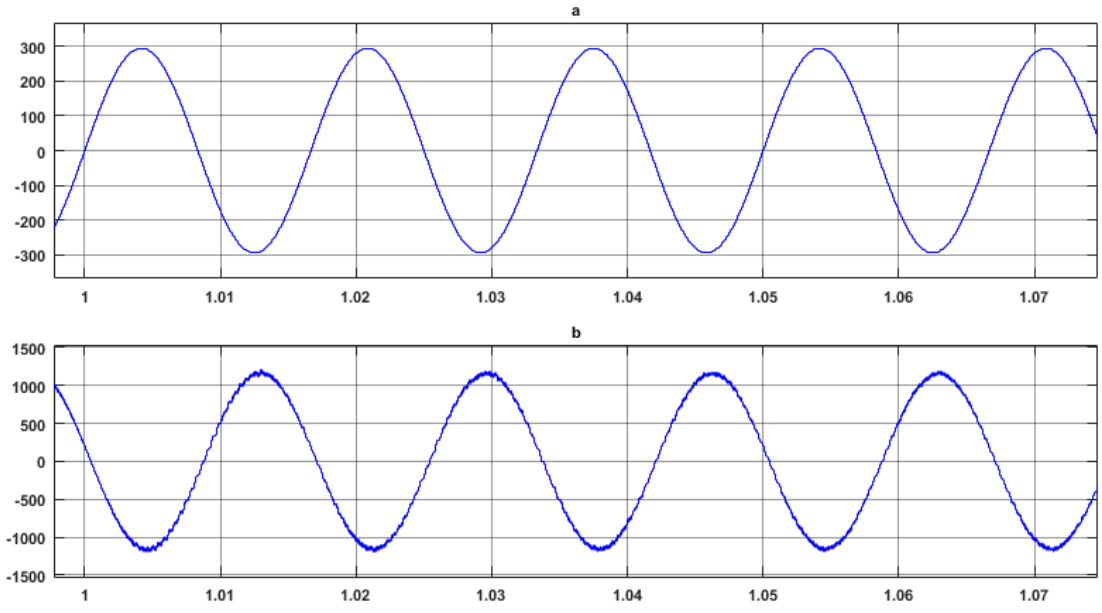


Figure 3-44: (a) Input source voltage, and (b) output voltage, for a duty ratio of 0.8.

It may be seen from Figure 3-42, that for a duty ratio of 0.3, the input voltage which has a rms value of $208V_{line\text{-}line}$ may be regulated to generate an output voltage with an rms value of $126V_{line\text{-}line}$. It may be noted that the voltage waveforms have only been presented for phase-a for better understanding.

Figure 3-43 shows the input and output voltage waveform for a modulation index of 0.5 which regulates an output voltage of rms value, $208V_{line\text{-}line}$, which is equal to input source voltage. In contrast, Figure 3-44 shows the input voltage and corresponding output voltage waveform for a duty ratio of 0.8. It may be observed from the waveforms that output voltage is phase-shifted from input voltage by 180 degrees, which has been discussed earlier in the sub-section 3.5.3.

Therefore, it may be concluded from results presented above that 3-Ø CPC ac-ac buck-boost converter may be used to regulate the output voltage to a desired value similar to a ac-ac Power-Line Conditioner (PLC). Thus, the converter topology is termed as Center-Point-Clamped AC-AC Power-Line Conditioner or in short may be written as CPC PLC.

3.6.5. Center-Point-Clamped 3-Ø Power Line Conditioner for 4.16kV application

It may be seen from the motivation discussed in section 3.2, that the center-point-clamped ac-ac converter technology can be used reliably to construct a power conditioning solution for power quality issues faced by utilities in distribution systems operating at 4.16kV. The results verifying the operating principle of a center-point-clamped ac-ac converter topology in sections 3.3, 3.5, 3.6 and 3.6 have been shown for 208-$V_{line\text{-}line}$ 3-Ø ac applications. It is so because the laboratory hardware prototype to verify the operational methodology has been scaled down to 208-$V_{line\text{-}line}$ 3-Ø ac system, which may also be seen from chapter 4.

But to demonstrate the practical realization of a power conditioning solution based on the principle of center-point-clamping, this sub-section presents the simulated results based on Matlab-Simulink for a 4.16kV 3-Ø ac application. As presented in the motivation for this dissertation, major challenges in employing power semiconductor devices-based power quality solutions is due to the fact that power semiconductor devices rated more than utility level voltage and power levels are not commercially readily available. The center-point-clamped ac-ac converter topology may be used to construct power quality solutions for utility rated voltages using power semiconductor devices rated at half the voltage and power ratings required to build prevalent solutions presented in literature.

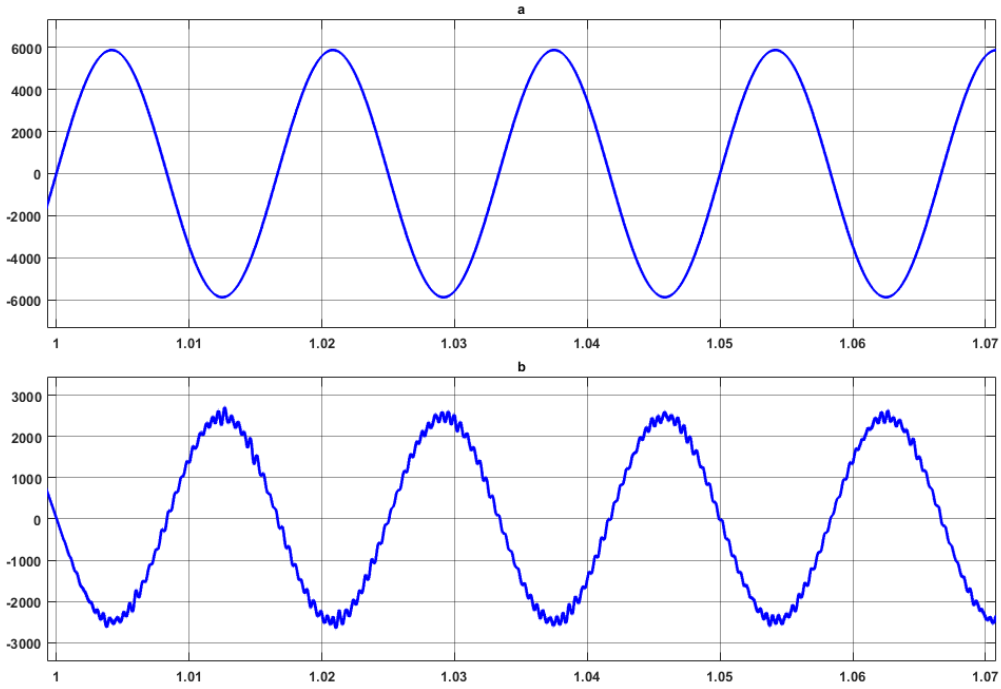


Figure 3-45: (a) Input source voltage, and (b) output voltage, for a duty ratio of 0.3.

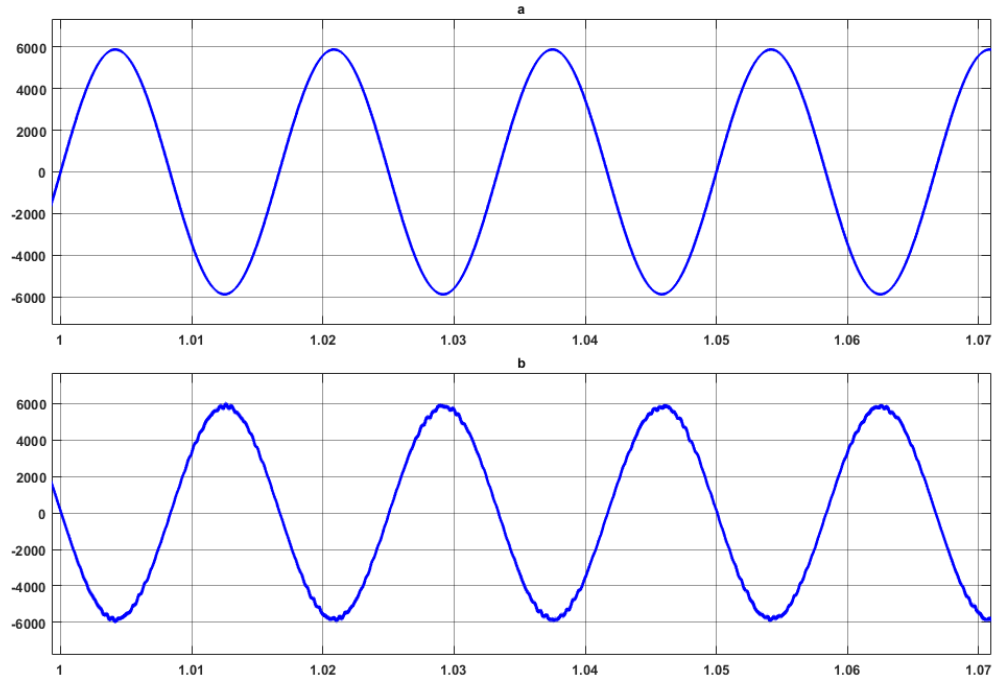


Figure 3-46: (a) Input source voltage, and (b) output voltage, for a duty ratio of 0.5.

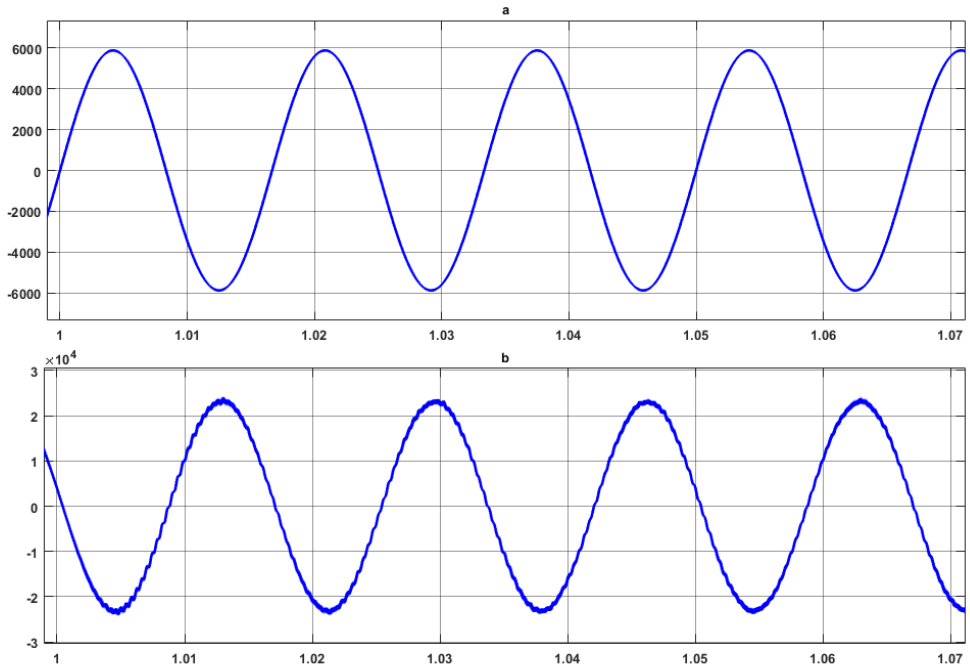


Figure 3-47: (a) Input source voltage, and (b) output voltage, for a duty ratio of 0.8.

Figure 3-45, Figure 3-46 and Figure 3-47 shows the input source and output load voltage waveforms of the CPC PLC for 4.16 $kV_{line\text{-}line}$ utility distribution level voltage. It may be seen that output load voltages of CPC PLC may be regulated to 1.78 $kV_{line\text{-}line}$, 4.16 $kV_{line\text{-}line}$ and 16.64 $kV_{line\text{-}line}$, respectively, by utilizing duty-ratio control. This shows the voltage regulation capability of CPC PLC for utility distribution level voltage. As may be seen from the voltage stress waveforms shown in Figure 3-48 and Figure 3-49, each bi-directional switch voltage stress is reduced to half the value of summation of input and output voltage, $\frac{v_{in}+ v_{out}}{2}$.

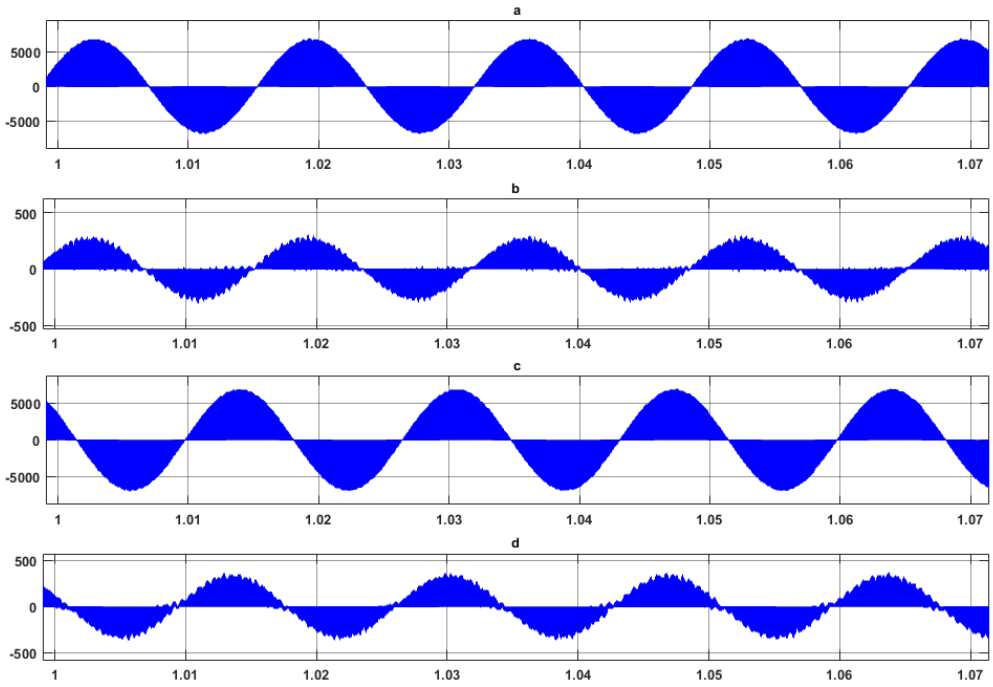


Figure 3-48: (a) Voltage across switch, S_1, (b) Current through switch, S_1, (c) Voltage across switch, S_3 and, (d) Current through switch, S_3

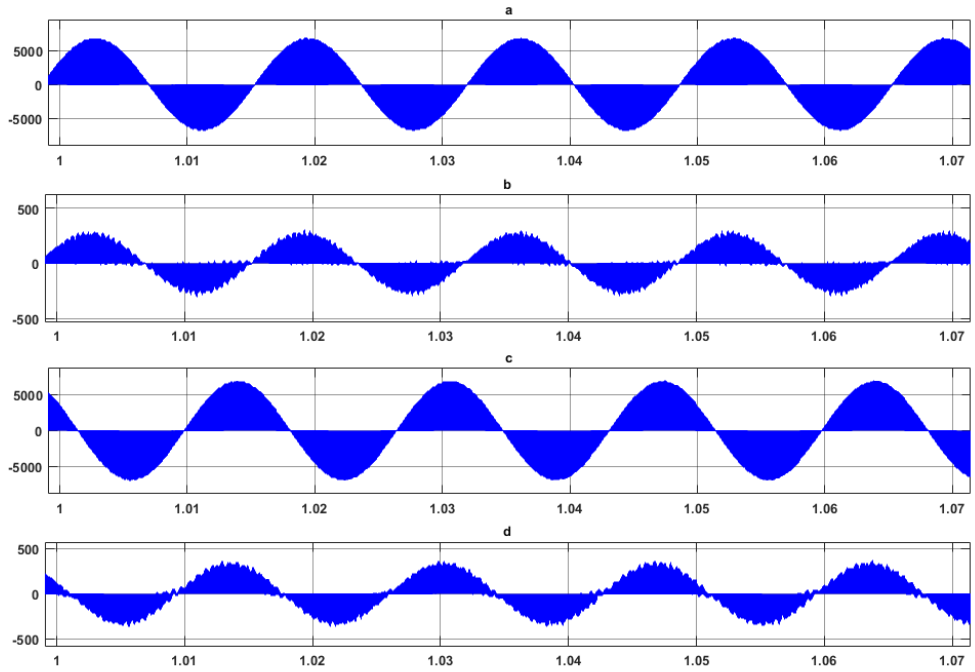


Figure 3-49: (a) Voltage across switch, S_2, (b) Current through switch, S_2, (c) Voltage across switch, S_4 and, (d) Current through switch, S_4

Finally, it may be concluded from the results and discussions presented in this chapter that CPC PLC does achieve capacitor voltage balancing, which reduces the voltage stress on the IGBT devices employed to build the converter circuit. The next chapter presents the analysis of this selected topology of CPC PLC with bi-directional switches, where capacitor voltages are perfectly balanced as well as each bi-directional switch voltage stress is reduced to half the value of summation of input and output voltage, $\frac{v_{in}+ v_{out}}{2}$.. The analysis discusses the design of the reactive components (L and C) employed in the converter circuit.

4. Chapter Four: Hardware Circuit Design of Center-Point-Clamped Power Line Conditioner (CPC PLC)

4.1. Introduction

This chapter discusses the design considerations for power circuit design of CPC PLC. The operating principle of this topology has been discussed in Section 3.6. This design discusses voltage and current stresses on each components of converter circuit. The analysis and design methods applied to design the component parameters for this topology are found to be similar to corresponding dc-dc converters due to their design and functional similarities.

4.2. Circuit Description

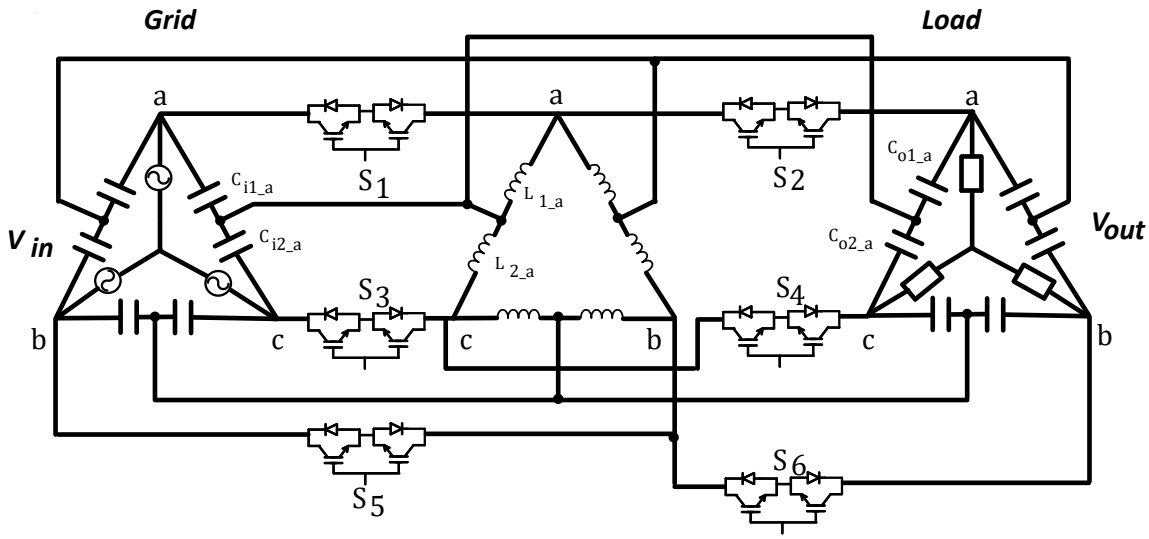


Figure 4-1: Simplified circuit schematic of the 3-Ø CPC PLC.

A simplified circuit schematic of the 3-Ø CPC PLC is shown in Figure 4-1. As may be seen, the circuit involves six capacitors in the input and six capacitors at the output to achieve input and output voltage center-point-clamping. It also involves six buck-boost inductors, which are the mode of transfer of energy from input to output side during the

two-switching sequences as mentioned in Table 3-3. There are six bi-directional switches, S_1, S_2, S_3, S_4, S_5, and S_6, which has been realized by twelve Insulated Gate Bipolar Transistors (IGBTs), that are switched at 25kHz (f_{sw} – switching frequency). The converter is rated for operation up to $120V_{rms\text{-}line}$, 1kW. It may be noted from Figure 4-1, that the converter structure is symmetrical across three phases. Therefore, the circuit design analysis has been performed for only one phase with the appropriate voltage and current rating for each component. The equivalent single-phase circuit schematic is shown in Figure 4-2.

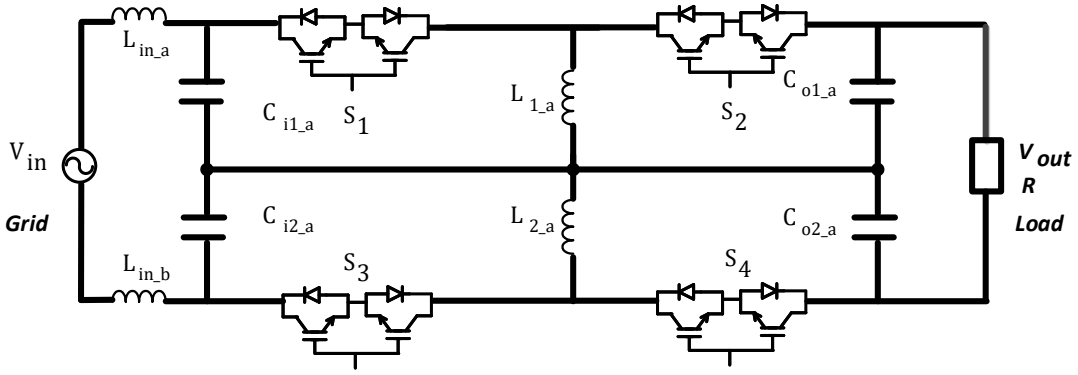


Figure 4-2: Single phase equivalent circuit schematic of the CPC PLC.

As may be seen from Figure 4-2, the converter topology has an input inductor in series across each phase, L_{in_a} and L_{in_b}. These inductors serve as input filters to attenuate any switching harmonics from being fed back to the input source side. There are two series capacitors, C_{i1_a} and C_{i2_a}, which are used to achieve input center-point voltage at the junction of two capacitors. Similar arrangement may be seen in output side with two series capacitors, C_{o1_a} and C_{o2_a}, to achieve output center-point voltage. There are two buck-boost inductors, L_{1_a} and L_{2_a}. The load is represented by a resistor *R*.

4.3. Selection of Power Semiconductor Device

The power semiconductor devices used in these ac-ac converters operate at two different switching sequences, i.e. on or off as shown in Table 3-3. It may be noted that in this converter topology, the voltage stress across the switches is reduced due to center-point-clamping at the source and load side. It may be noted from Table 3-3, that switches S_1 S_3 and S_2 S_4 are turned on and off in complementary fashion during the two switching states. The desired output voltage for our analysis design is achieved at a duty ratio of about 50%. This duty ratio generates an output voltage which is equal in magnitude to the input voltage, but 180 degrees out of phase, due to buck-boost inductor operation, which has been explained in Chapter 3. The voltage stress across each power semiconductor device is $\frac{v_{in}+ v_{out}}{2}$, which is equal to $120V_{rms\text{-}line}$. The switching frequency for operating this converter is rated at 25kHz. A semiconductor device rated at 1200V, 100A which may be switched up to 50kHz. This device has been purchased from Mircosemi and the device part number is 'APT100GT120JRDQ4'. A screenshot of datasheet of the IGBT structure with its ratings has been displayed in Figure 4-3.

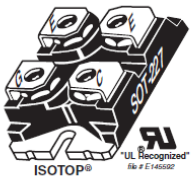
Microsemi
POWER PRODUCTS GROUP

APT100GT120JRDQ4

1200V, 100A, $V_{CE(ON)}$ = 3.2V Typical

Thunderbolt IGBT®

The Thunderbolt IGBT® is a new generation of high voltage power IGBTs. Using Non-Punch-Through Technology, the Thunderbolt IGBT® offers superior ruggedness and ultrafast switching speed.



ISOTOP®

Features

- Low Forward Voltage Drop
- Low Tail Current
- Integrated Gate Resistor
  Low EMI, High Reliability
- RoHS Compliant
- RBSOA and SCSOA Rated
- High Frequency Switching to 50KHz
- Ultra Low Leakage Current

Unless stated otherwise, Microsemi discrete IGBTs contain a single IGBT die. This device is made with two parallel IGBT die. It is intended for switch-mode operation. It is not suitable for linear mode operation.

Maximum Ratings All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	1200	Volts
V_{GE}	Gate-Emitter Voltage	±20	
I_{C1}	Continuous Collector Current @ T_C = 25°C	123	Amps
I_{C2}	Continuous Collector Current @ T_C = 100°C	67	
I_{CM}	Pulsed Collector Current①	200	
SSOA	Switching Safe Operating Area @ T_J = 150°C	200A @ 1200V	
P_D	Total Power Dissipation	570	Watts
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Max. Lead Temp. for Soldering: 0.063" from Case for 10 Sec.	300	

Figure 4-3: Screenshot of selected IGBT datasheet from Digikey.

4.4 **Selection of Passive Components in converter circuit, L & C**

The selection of parameters for each of the passive components, inductors and capacitors requires analysis of the circuit node voltages and currents during the switching sequence displayed in Table 3-3. For sake of simplicity, the steady state analysis is performed on the single-phase equivalent circuit of CPC PLC. The detailed analysis has been presented in following sub-section 4.4.1.

4.4.1. **Steady State Circuit Analysis**

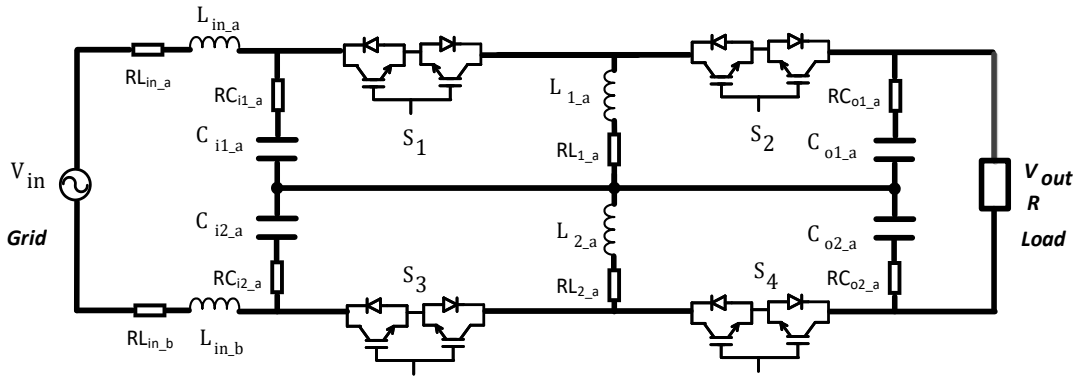


Figure 4-4: Detailed single-phase equivalent circuit schematic of the CPC PLC.

The detailed single-phase converter topology is shown in Figure 4-4. As may be seen from the figure, it incorporates the parasitics involved with inductors and capacitors. The switching scheme of this circuit model is shown in following Table 4-1.

Table 4-1: Switching principle of CPC PLC

Command v_{out} (desired output)	**between v_{in} and $n.v_{in}$**
State 1	S_1 S_3 closed S_2 S_4 open
State 2	S_2 S_4 closed S_1 S_3 open

As may be seen from Table 4-1, the converter has two switching states. The steady state analysis discusses the Kirchoff's Voltage Law (KVL) and Kirchoff's Current Law (KCL) for both the states and derives equation for determining the required inductance and capacitance values used in designing the converter.

State 1: (S_1 S_3 closed & S_2 S_4 open)

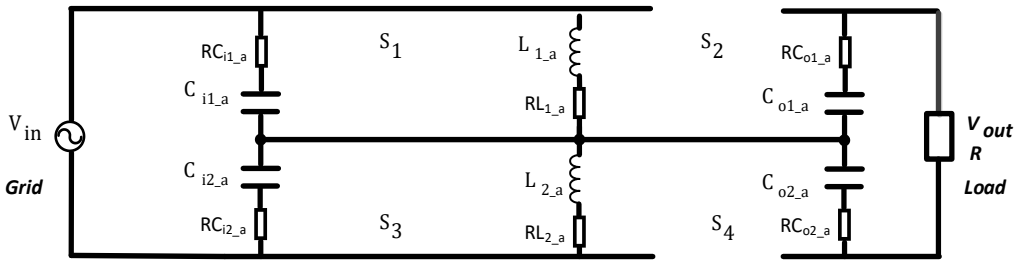


Figure 4-5: Detailed single-phase equivalent circuit schematic of the CPC PLC during switching state 1 (S_1 S_3 closed & S_2 S_4 open).

Applying Kirchhoff's voltage laws, we get

$$v_{in} - v_{Ci1_a} - i_{Ci1_a}.R_{Ci1_a} - v_{Ci2_a} - i_{Ci2_a}.R_{Ci2_a} = 0 \quad 4.1$$

$$v_{in} - v_{L1_a} - i_{L1_a}.R_{L1_a} - v_{L2_a} - i_{L2_a}.R_{L2_a} = 0 \quad 4.2$$

$$v_{Ci1_a} + i_{Ci1_a}.R_{Ci1_a} - v_{L1_a} - i_{L1_a}.R_{L1_a} = 0 \quad 4.3$$

$$v_{Ci2_a} + i_{Ci2_a}.R_{Ci2_a} - v_{L2_a} - i_{L2_a}.R_{L2_a} = 0 \quad 4.4$$

$$v_{Co1_a} + i_{Co1_a}.R_{Co1_a} + v_{Co2_a} + i_{Co2_a}.R_{Co2_a} + v_{out} = 0 \quad 4.5$$

Applying Kirchhoff's current laws, we get

$$i_{in} - i_{Ci1_a} - i_{L1_a} = 0 \quad 4.6$$

$$i_{in} - i_{Ci2_a} - i_{L2_a} = 0 \quad 4.7$$

$$i_{out} = i_{Co1_a} = i_{Co2_a} \quad 4.8$$

Let the time period be T and d be the duty ratio. Thus, dT is the time when switches S_1 S_3 are closed and S_2 S_4 are open, which represents the switching state 1.

Let us represent f_{sw} as the switching frequency, which may be represented as

$$T = \frac{1}{f_{sw}} \tag{4.9}$$

State 2: (S_1 S_3 open & S_2 S_4 closed)

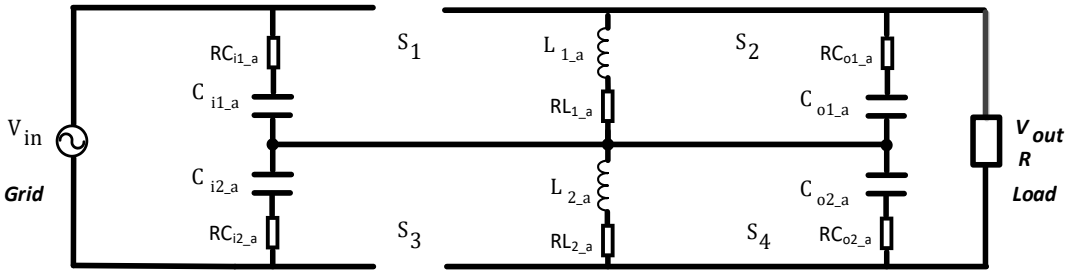


Figure 4-6: Detailed single-phase equivalent circuit schematic of the CPC PLC during switching state 1 (S_1 S_3 open & S_2 S_4 closed).

Applying Kirchoff's voltage laws, we get

$$v_{in} - v_{Ci1_a} - i_{Ci1_a}.R_{Ci1_a} - v_{Ci2_a} - i_{Ci2_a}.R_{Ci2_a} = 0 \tag{4.10}$$

$$v_{out} + v_{L1_a} + i_{L1_a}.R_{L1_a} + v_{L2_a} + i_{L2_a}.R_{L2_a} = 0 \tag{4.11}$$

$$v_{Co1_a} + i_{Co1_a}.R_{Co1_a} - v_{L1_a} - i_{L1_a}.R_{L1_a} = 0 \tag{4.12}$$

$$v_{Co2_a} + i_{Co2_a}.R_{Co2_a} - v_{L2_a} - i_{L2_a}.R_{L2_a} = 0 \tag{4.13}$$

$$v_{Co1_a} + i_{Co1_a}.R_{Co1_a} + v_{Co2_a} + i_{Co2_a}.R_{Co2_a} + v_{out} = 0 \tag{4.14}$$

Applying Kirchoff's current laws, we get

$$i_{in} = i_{Ci1_a} = i_{Ci2_a} \tag{4.15}$$

$$i_{L1_a} - i_{Co1_a} + i_{out} = 0 \tag{4.16}$$

$$i_{L2_a} - i_{Co2_a} + i_{out} = 0 \tag{4.17}$$

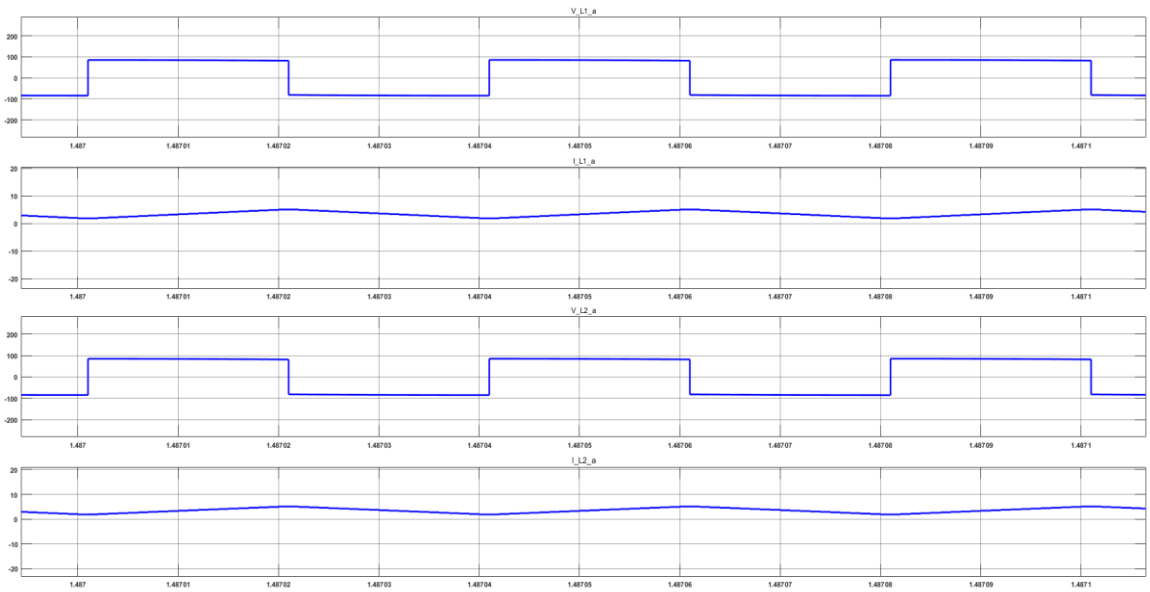


Figure 4-7: Inductor Voltage, V_{L1_a} and V_{L2_a} and their corresponding inductor currents, I_{L1_a} and I_{L2_a}

As may be seen from Figure 4-7, the average inductor voltage is zero for both the series connected inductors across one time-period, which is 40µs in this case. It may be noted from the inductor current behavior that during state-1 of switching sequence, the inductor is connected to the input source side and gets energized, whereas in state-2, the inductor is connected to the output load side and gets de-energized. The presented converter analysis has been conducted for Continuous Conduction Mode (CCM) of operation, which is evident from the inductor current waveforms. Since this topology allows equal capacitor voltage balancing for both the series-connected input and output capacitors, the following assumptions may be made

$$v_{Ci1_a} = v_{Ci2_a} = \frac{v_{in}}{2} \tag{4.18}$$

$$v_{Co1_a} = v_{Co2_a} = \frac{v_{out}}{2} \tag{4.19}$$

By applying the principle of inductor volt-second balance on L_{1_a} and using equations (4.3), (4.123), and assuming dT as the time interval for state 1, and $(1-d)T$ as the time interval for state-2, we may represent the average inductor voltage, $\langle v_{L1_a} \rangle$ across a switching cycle as

$$\langle v_{L1_a} \rangle = d\left(v_{Ci1_a} + i_{Ci1_a}.R_{Ci1_a} - i_{L1_a}.R_{L1_a}\right) + (1-d).\left(v_{Co1_a} + i_{Co1_a}.R_{Co1_a} - i_{L1_a}.R_{L1_a}\right) = 0 \quad (4.20)$$

Now, using equation (4.18) and (4.19), equation (4.20) may be rewritten as

$$d\left(\frac{v_{in}}{2}\right) + (1-d)\left(\frac{v_{out}}{2}\right) + d\left(i_{Ci1_a}.R_{Ci1_a}\right) + (1-d)\left(i_{Co1_a}.R_{Co1_a}\right) - \left(i_{L1_a}.R_{L1_a}\right) = 0 \quad (4.21)$$

Since, the voltage drop across parasitic resistance of input and output capacitors and inductors may be considered as negligible, equation 4.21 may be written in a much-simplified form as follows:

$$d\left(\frac{v_{in}}{2}\right) + (1-d)\left(\frac{v_{out}}{2}\right) = 0 \quad (4.22)$$

$$\frac{v_{out}}{v_{in}} = -\frac{d}{(1-d)} \quad (4.23)$$

Equation 4.23 shows the voltage gain for the proposed buck-boost converter topology, which is similar to a traditional buck-boost converter in case of CCM mode of operation.

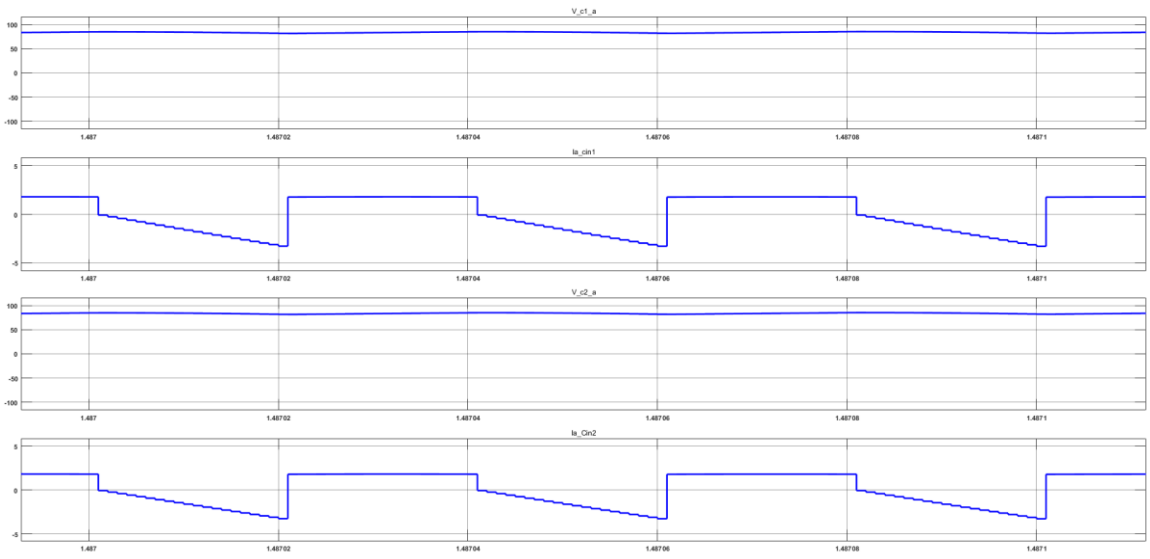


Figure 4-8: Input Capacitor Voltage, V_{Ci1_a} and V_{Ci2_a} and their corresponding capacitor currents, I_{Ci1_a} and I_{Ci2_a}

As may be seen from Figure 4-8, the input capacitor voltages are equally balanced. The capacitor current waveforms demonstrate the charging of capacitors in state-1 of switching operation and discharge during state-2. It may be noted that the average capacitor current is about zero for one time-period, T, which is about 40µs in this case. By applying the principle of ampere-second balance on C_{i1_a} and using equations (4.6), (4.7) and (4.15), and, assuming dT as the time interval for state 1 and $(1-d)T$ as the time interval for state-2, we may represent average input capacitor current, $\langle i_{Ci1_a} \rangle$, across a switching cycle as,

$$\langle i_{Ci1_a} \rangle = d\left(i_{in} - i_{L1_a}\right) + (1-d)i_{in} = 0 \qquad 4.24$$

$$i_{in} = d\left(i_{L1_a}\right) \qquad 4.25$$

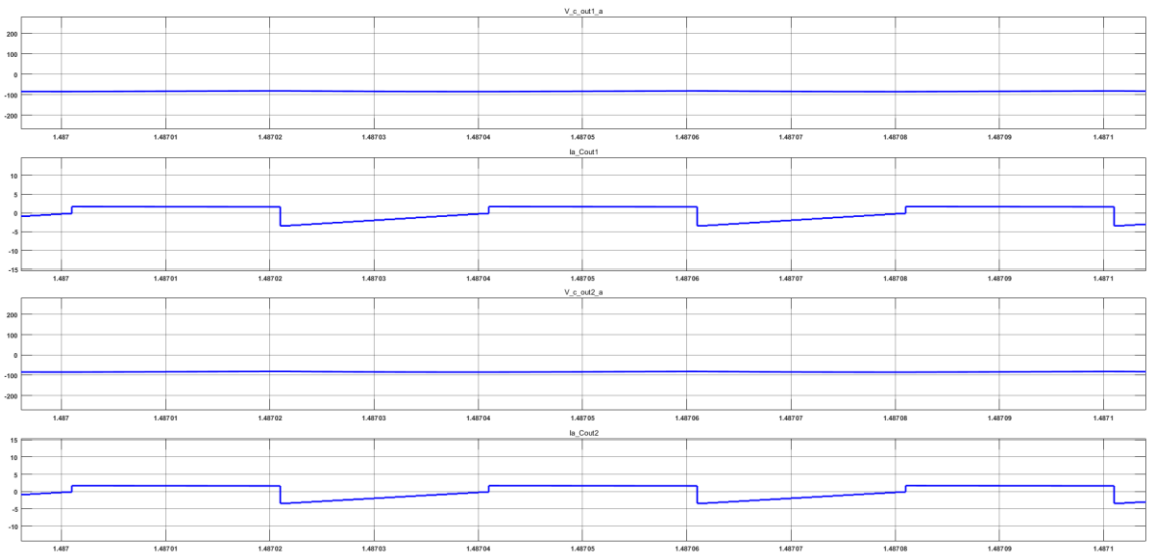


Figure 4-9: Output Capacitor Voltage, V_{Co1_a} and V_{Co2_a} and their corresponding capacitor currents, I_{Co1_a} and I_{Co2_a}

As may be seen from Figure 4-9, the output capacitor voltages are equally balanced. The output capacitor current waveforms demonstrate the charging of capacitor in state-1 of switching operation and discharge during state-2. It may be noted that the average capacitor current is about zero for one time-period, T, which is about 40µs in this case. By applying the principle of ampere-second balance on C_{o1_a} and using equations (4.8), (4.16) and (4.17), and, assuming dT as the time interval for state 1 and $(1-d)T$ as the time interval for state-2, we may represent average output capacitor current, $\langle i_{Ci1_a} \rangle$, across a switching cycle as,

$$\langle i_{Co1_a} \rangle = d i_{out} + (1-d)\left(i_{out} + i_{L1_a}\right) = 0 \qquad 4.26$$

$$i_{out} = -(1-d)\left(i_{L1_a}\right) \qquad 4.27$$

4.4.2. **Selection of L and C values**

For the selection of L & C values, we assume the parasitic resistance of the capacitors and inductors are very much less than the load resistance as shown in equation (4.28). Thus, we can neglect the voltage drop across those parasitics.

$$R_{Ci1_a}, R_{Ci2_a}, R_{Co1_a}, R_{Co2_a}, R_{L1_a}, R_{L2_a} \ll R \tag{4.28}$$

Also, we assume inductor current ripple is about 20% of the actual inductor current. Therefore, we can say,

$$\Delta i_{L1_a} \ll 20\%. i_{L1_a} \tag{4.29}$$

Now, for state-1, using KVL, from equation (4.3), we have,

$$v_{Ci1_a} + i_{Ci1_a}. R_{Ci1_a} - v_{L1_a} - i_{L1_a}. R_{L1_a} = 0 \tag{4.30}$$

Since, we know, the capacitors are equally balance in this topology and using equation (4.28), equation (4.30) may be rewritten as,

$$\frac{v_{in}}{2} - v_{L1_a} = 0 \tag{4.31}$$

$$\Longrightarrow v_{L1_a} = \frac{v_{in}}{2} \tag{4.32}$$

$$\Longrightarrow L. \frac{\Delta i_{L1_a}}{DT_{sw}} = \frac{v_{in}}{2} \tag{4.33}$$

$$L. \Delta i_{L1_a} = \frac{v_{in}}{2}. DT_{sw} \tag{4.34}$$

$$L = \frac{v_{in}}{2}. DT_{sw}. \frac{1}{\Delta i_{L1_a}} \tag{4.35}$$

Since our operating region involves operating in +/- 10% of $120V_{rms\ line\text{-}line}$, we can say,

$$v_{in} \in (108, 132\ ) \tag{4.36}$$

Since we will be designing a power line conditioner, the input and output voltage should be equal and as such operating duty ratio would be about 0.5%, which is in the range presented in equation (4.37).

$$D€(0.476,0.526) \quad 4.37$$

Here, using equations (4.35), (4.36) and (4.37), the desired values of inductance for different operating points for a 3-Ø power of about 1-kVA are presented in Table 4-2.

Table 4-2: Inductance values for different operating points

v_{in}	v_{out}	D	i_{L1_a}	Δi_{L1_a} ($20\%\ of\ i_{L1_a}$)	T_{sw}	**L** (values for $\boldsymbol{L1_a}$ and $\boldsymbol{L2_a}$)
$108V_{rms}$	$120V_{rms}$	0.526	$5A_{rms}$	$1A_{rms}$	40µs	**1.256mH**
$120V_{rms}$	$120V_{rms}$	0.5	$5A_{rms}$	$1A_{rms}$	40µs	**1.2mH**
$132V_{rms}$	$120V_{rms}$	0.476	$5A_{rms}$	$1A_{rms}$	40µs	**1.136mH**

Similar analysis is performed to tabulate the input and output capacitor values for the proposed center-point-clamped buck-boost converter circuit.

For determining the input capacitor value, we utilize the equations (4.15) and (4.28) and assume capacitor voltage ripple is about 20% of the actual capacitor voltage.

$$\Delta v_{Ci1_a} \ll 20\%.\, v_{Ci1_a} \quad 4.38$$

$$i_{in} = i_{Ci1_a} \quad 4.39$$

$$\Longrightarrow C.\frac{\Delta v_{Ci1_a}}{(1-D)T_{sw}} = i_{in} \quad 4.40$$

$$\Longrightarrow C = i_{in}.(1-D).T_{sw}.\frac{1}{\Delta v_{Ci1_a}} \quad 4.41$$

Using equation (4.41), the desired values of capacitance for different operating region is displayed in Table 4-3.

Table 4-3: Input capacitance values for different operating points

v_{in}	v_{out}	D	i_{in}	$\Delta v_{Ci1_a} or \Delta v_{Ci2_a}$ ($20\% \, of \, v_{Ci1_a}$ $or \, v_{Ci2_a}$)	T_{sw}	**C** (values for $\boldsymbol{Ci1_a}$ and $\boldsymbol{Ci2_a}$)
$108V_{rms}$	$120V_{rms}$	0.526	$5A_{rms}$	$10.8V_{rms}$	40µs	**9.74µF**
$120V_{rms}$	$120V_{rms}$	0.5	$5A_{rms}$	$12V_{rms}$	40µs	**8.33µF**
$132V_{rms}$	$120V_{rms}$	0.476	$5A_{rms}$	$13.2V_{rms}$	40µs	**7.21µF**

For ascertaining the output capacitor value, we utilize the equations (4.8) and (4.28) and assume capacitor voltage ripple is about 20% of the actual capacitor voltage.

$$\Delta v_{Co1_a} \ll 20\%.v_{Co1_a} \quad 4.42$$

$$i_{out} = i_{Co1_a} \quad 4.43$$

$$\Longrightarrow C.\frac{\Delta v_{Co1_a}}{DT_{sw}} = i_{out} \quad 4.44$$

$$\Longrightarrow C = i_{out}.DT_{sw}.\frac{1}{\Delta v_{Co1_a}} \quad 4.45$$

Using equation (4.45), the desired values of capacitance for different operating region is displayed in Table 4-4.

Table 4-4: Output capacitance values for different operating points

v_{in}	v_{out}	D	i_{out}	$\Delta v_{Ci1_a} or \Delta v_{Ci2_a}$ ($20\% \; of \; v_{Ci1_a}$ $or \; v_{Ci2_a}$)	T_{sw}	**C** (values for $\boldsymbol{Co1_a}$ and $\boldsymbol{Co2_a}$)
$108V_{rms}$	$120V_{rms}$	0.526	$5A_{rms}$	$10.8V_{rms}$	40µs	**9.74µF**
$120V_{rms}$	$120V_{rms}$	0.5	$5A_{rms}$	$12V_{rms}$	40µs	**8.33µF**
$132V_{rms}$	$120V_{rms}$	0.476	$5A_{rms}$	$13.2V_{rms}$	40µs	**7.21µF**

The following values have been selected for the inductance and capacitance for further analysis and experimentation:

Components	Values	Part Number	Part Supplier
$\boldsymbol{L_{1a} = L_{2a}}$	0.5mH	DLFP-0147-12D5	Mouser
$\boldsymbol{C_{i1a} = C_{i2a}}$	10µF	80-C276CCF5100LG0J	Mouser
$\boldsymbol{C_{o1a} = C_{o2a}}$	10µF	80-C276CCF5100LG0J	Mouser

The design of the input filter will be discussed in detail in the next chapter, where the loop gain of the converter circuit will be studied using dynamic analysis of presented topology.

5. Chapter Five: Dynamic Analysis and Controller Design for Center-Point-Clamped Power Line Conditioner (CPC PLC)

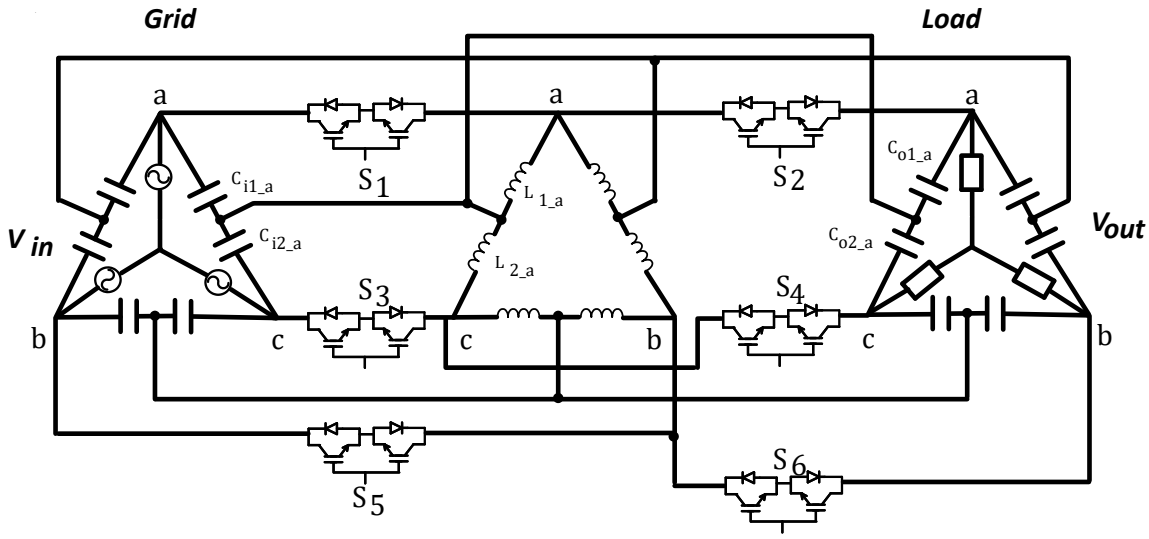


Figure 5-1: Simplified circuit schematic of CPC PLC.

Figure 5-1 shows simplified circuit schematic for the CPC 3-Ø CPC PLC. It may be seen that the converter topology may be used to regulate load side voltage to achieve desired voltage by controlling duty ratio of the switches according to Table 5-1.

Table 5-1: Switching principle of CPC PLC

Command v_{out} (desired output)	**between v_{in} and $n.v_{in}$**
State 1	S_1 S_3 S_5 closed S_2 S_4 S_6 open
State 2	S_2 S_4 S_6 closed S_1 S_3 S_5 open

As we simplified our steady state analysis by analyzing the single-phase circuit equivalent circuit of 3-Ø CPC PLC, we will consider the same single phase detailed circuit considering the parasitics associated with each component for dynamic analysis. The detailed single-phase circuit is displayed in Figure 5-2. This chapter presents the design of closed-loop controller for load voltage regulation. The design has been performed using state-space modelling technique in frequency domain.

5.1. State Space Averaging

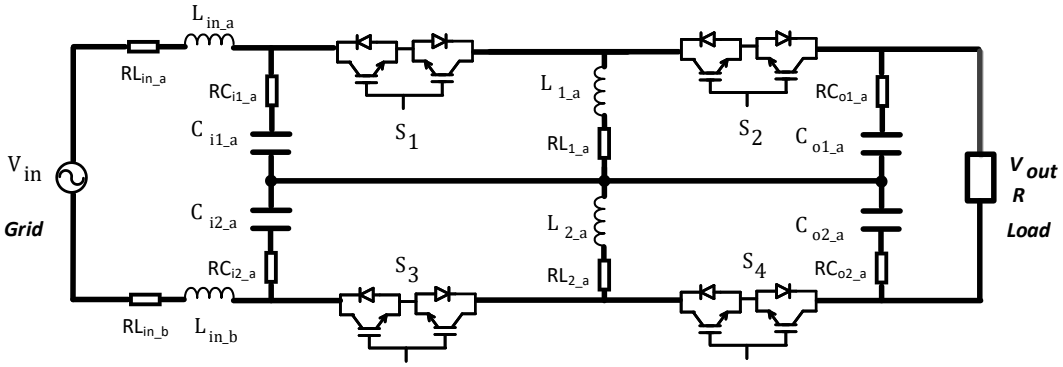


Figure 5-2: Detailed single-phase equivalent circuit schematic of the center-point-clamped ac-ac buck-boost converter

For the initial dynamic circuit analysis, the input line inductances, L_{in_a}, L_{in_b} and the parasitics associated with them, RL_{in_a}, RL_{in_b} have been considered for state space modelling. In this converter system, the state variables have been identified as the input line inductance, L_{in_a}, current, i_{Lin_a} input line inductance, L_{in_b}, current, i_{Lin_b}, buck-boost inductor L_{1_a}, current, i_{L1_a}, buck-boost inductor L_{2_a}, current, i_{L2_a}, input capacitor C_{i1_a}, voltage, v_{Ci1_a}, input capacitor C_{i2_a}, voltage, v_{Ci2_a}, output capacitor C_{o1_a}, voltage, v_{Co1_a}, and output capacitor C_{o2_a}, voltage, v_{Co2_a}. The state-space equations for both states of the switching sequence for CPC buck-boost converter has been derived in this sub-section. It

may be stated that state space equations for generic switched circuit that is operated in two states of switching sequence, dT and d/T, are represented as follows:

I. Interval dT of switching sequence:

$$\dot{x} = a_1 x + b_1 u \quad 5.1$$

$$y = c_1^T x + d_1 u \quad 5.2$$

II. Interval d/T of switching sequence:

$$\dot{x} = a_2 x + b_2 u \quad 5.3$$

$$y = c_2^T x + d_2 u \quad 5.4$$

Where, x is state vector which represents state of the system, u is input (or control) vector which represents input to system, y is output vector which represents output of the system, a_1, a_2 are state (or system) matrices, b_1, b_2 are input matrices, c_1^T, c_2^T are output matrices. Since the system does not consider any feedforward signal, the feedforward matrices, d_1, d_2 may be considered as zero matrices.

It may be worth mentioning that the converter system may be considered as a linear time-invariant system, since the response to a sinusoidal input voltage at the input of the converter is an output voltage sinusoid of same frequency, but different amplitude and phase depending on circuit parameters. This may be seen from the steady state analysis performed in previous chapter, which derives the relationship between input and output voltage and current waveforms. Now, the above state space equations may be averaged by considering the duty ratio of the intervals and may be represented as follows:

$$\dot{x} = d(a_1 x + b_1 u) + d/(a_2 x + b_2 u) \quad 5.5$$

$$y = dc_1^T x + d/c_2^T x \quad 5.6$$

Equations (5.5) and (5.6) present the state space averaged equations for the representative 1-Ø ac-ac cpc PLC. The node voltages and currents are derived in this section using Kirchhoff's voltage and current laws to determine the state vector, x, the input vector, u, the output vector, y, and the associated matrices with the equations, a_1, a_2, b_1, b_2, c_1^T, c_2^T. The simplified block diagram representation of the state space equations is shown in Figure 5-3.

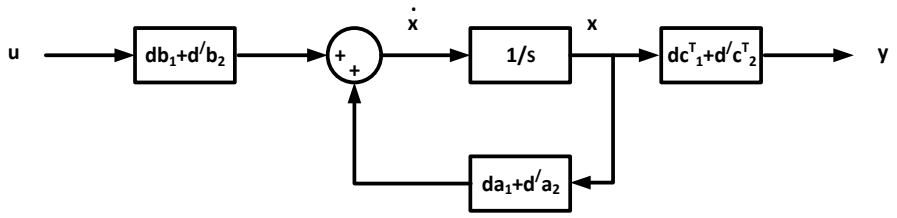


Figure 5-3: Simplified block diagram representation of state space averaged converter equation.

State 1: (S_1 S_3 closed & S_2 S_4 open)

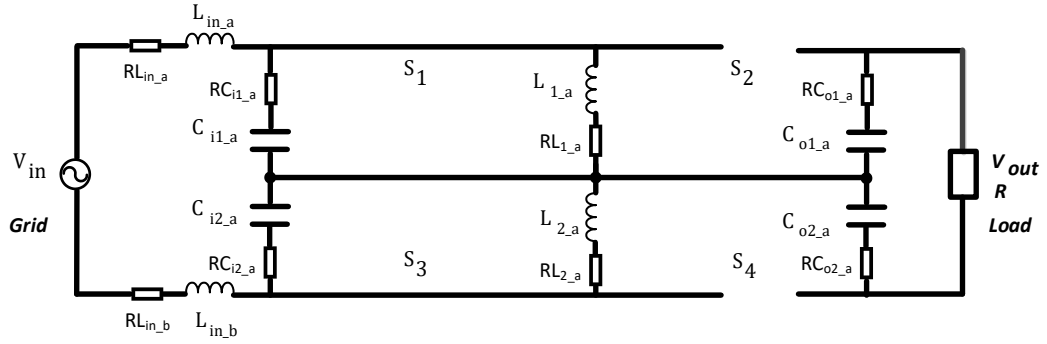


Figure 5-4: Detailed single-phase equivalent circuit schematic of the center-point-clamped ac-ac buck-boost converter during switching state 1 (S_1 S_3 closed & S_2 S_4 open).

As we have assumed in steady-state analysis in Chapter-4 the input capacitor currents, input inductor voltages, buck-boost inductor voltages and output capacitor voltages are

equal, and parasitics associated with each of these passive components are negligible as compared to the load resistance, we may further simplify the detailed circuit schematic to as shown in Figure 5-6.

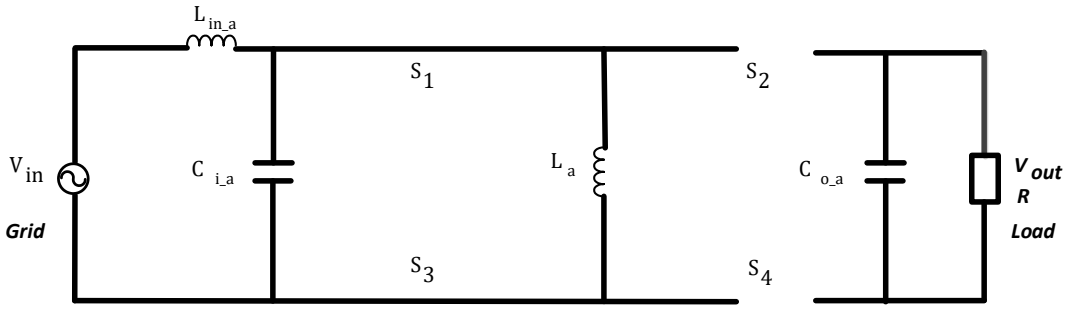


Figure 5-5: Simplified single-phase equivalent circuit schematic of the center-point-clamped ac-ac buck-boost converter during switching state 1 (S_1 S_3 closed & S_2 S_4 open).

The circuit voltage equations and current flow equations have been analyzed using Kirchhoff's laws for state-1 of switching sequence for the circuit shown in Figure 5-6.

Applying Kirchhoff's voltage laws to the representative circuit shown in Figure 5-6, we have,

$$v_{in} - v_{Lin_a} - v_{Ci_a} = 0 \tag{5.7}$$

$$v_{Ci_a} - v_{L_a} = 0 \tag{5.8}$$

$$v_{Co_a} - v_{out} = 0 \tag{5.9}$$

Now, introducing Kirchhoff's current laws to the converter topology shown in Figure 5-6, we have,

$$i_{Lin_a} - i_{Ci_a} - i_{L_a} = 0 \tag{5.10}$$

$$i_{Co_a} = -\frac{v_{out}}{R} = -\frac{v_{Co_a}}{R} \tag{5.11}$$

Considering the state space equations presented in equations (5.1) and (5.2) and the above circuit equations for state-1 of switching sequence, we have,

$$\dot{x} = \begin{bmatrix} \frac{di_{Lin_a}}{dt} \\ \frac{dv_{Ci_a}}{dt} \\ \frac{di_{L_a}}{dt} \\ \frac{dv_{Co_a}}{dt} \end{bmatrix} \tag{5.12}$$

$$x = \begin{bmatrix} i_{Lin_a} \\ v_{Ci_a} \\ i_{L_a} \\ v_{Co_a} \end{bmatrix} \tag{5.13}$$

$$u = v_{in} \tag{5.14}$$

$$y = v_{out} \tag{5.15}$$

Using the equations presented in (5.7) - (5.11), the matrices, a_1, b_1, c_1, may be derived as

$$a_1 = \begin{bmatrix} 0 & -\frac{1}{Lin_a} & 0 & 0 \\ \frac{1}{Ci_a} & 0 & -\frac{1}{Ci_a} & 0 \\ 0 & \frac{1}{L_a} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R.Co_a} \end{bmatrix}, b_1 = \begin{bmatrix} \frac{1}{Lin_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} \text{ and } c_1 = [0 \quad 0 \quad 0 \quad 1]$$

The complete representation of the state equations with the matrices are shown in equations (5.16) – (5.18).

$$\begin{bmatrix} \frac{di_{Lin_a}}{dt} \\ \frac{dv_{Ci_a}}{dt} \\ \frac{di_{L_a}}{dt} \\ \frac{dv_{Co_a}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{Lin_a} & 0 & 0 \\ \frac{1}{Ci_a} & 0 & -\frac{1}{Ci_a} & 0 \\ 0 & \frac{1}{L_a} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R.Co_a} \end{bmatrix} * \begin{bmatrix} i_{Lin_a} \\ v_{Ci_a} \\ i_{L_a} \\ v_{Co_a} \end{bmatrix} + \begin{bmatrix} \frac{1}{Lin_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} . v_{in} \qquad 5.16$$

Now, since equation (5.16) is derived for state-1 of switching sequence, it may be rewritten to demonstrate duty ratio, 'd' of the switching time period, T.

$$\begin{bmatrix} \frac{di_{Lin_a}}{dt} \\ \frac{dv_{Ci_a}}{dt} \\ \frac{di_{L_a}}{dt} \\ \frac{dv_{Co_a}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{Lin_a} & 0 & 0 \\ \frac{1}{Ci_a} & 0 & -\frac{1}{Ci_a} & 0 \\ 0 & \frac{1}{L_a} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R.Co_a} \end{bmatrix} * d * \begin{bmatrix} i_{Lin_a} \\ v_{Ci_a} \\ i_{L_a} \\ v_{Co_a} \end{bmatrix} + \begin{bmatrix} \frac{1}{Lin_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} * d * v_{in} \qquad 5.17$$

$$v_{out} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} * d * \begin{bmatrix} i_{Lin_a} \\ v_{Ci_a} \\ i_{L_a} \\ v_{Co_a} \end{bmatrix} \qquad 5.18$$

State 2: (S_1 S_3 open & S_2 S_4 closed)

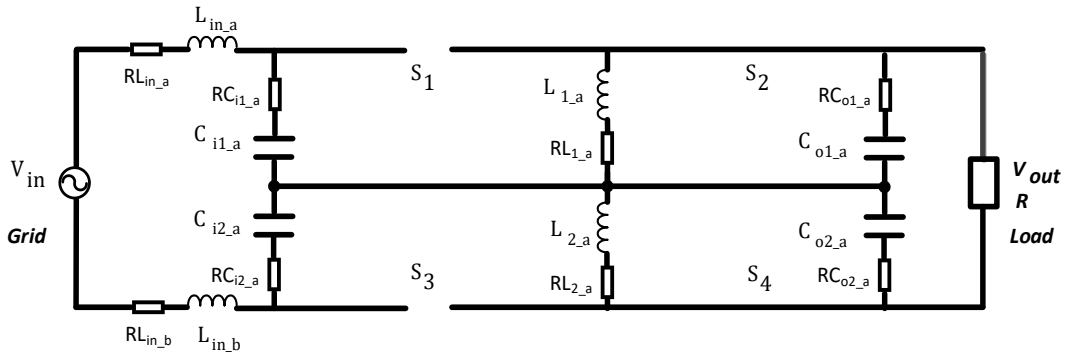


Figure 5-6: Detailed single-phase equivalent circuit schematic of the center-point-clamped ac-ac buck-boost converter during switching state 2 (S_1 S_3 open & S_2 S_4 closed).

Considering the circuit assumptions discussed in State-1 analysis, the new simplified circuit schematic is presented in Figure 5-7.

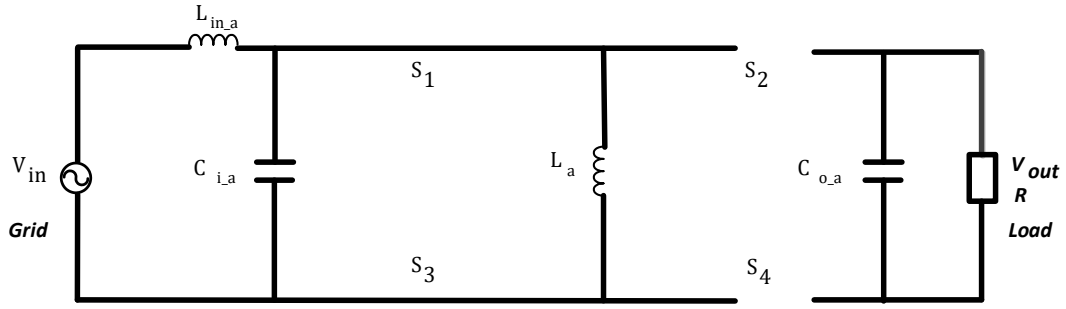


Figure 5-7: Simplified single-phase equivalent circuit schematic of the center-point-clamped ac-ac buck-boost converter during switching state 1 (S_1 S_3 closed & S_2 S_4 open).

The circuit voltage equations and current flow equations for circuit schematic shown in Figure 5-7 have been analyzed using Kirchhoff's laws for state-2 of switching sequence.

Applying Kirchhoff's voltage laws, we have,

$$v_{in} - v_{Lin_a} - v_{Ci_a} = 0 \tag{5.19}$$

$$v_{L_a} + v_{Co_a} = 0 \tag{5.20}$$

$$v_{out} = v_{Co_a} \tag{5.21}$$

Now, introducing Kirchhoff's current laws to the converter topology shown in Figure 5-7, we have,

$$i_{Lin_a} - i_{Ci_a} = 0 \tag{5.21}$$

$$i_{Co_a} = i_{L_a} - \frac{v_{out}}{R} \tag{5.22}$$

Considering the state space equations presented in equations (5.3) and (5.4) and the above circuit equations for state-2 of switching sequence, we have,

$$\dot{x} = \begin{bmatrix} \frac{di_{Lin_a}}{dt} \\ \frac{dv_{Ci_a}}{dt} \\ \frac{di_{L_a}}{dt} \\ \frac{dv_{Co_a}}{dt} \end{bmatrix} \tag{5.23}$$

$$x = \begin{bmatrix} i_{Lin_a} \\ v_{Ci_a} \\ i_{L_a} \\ v_{Co_a} \end{bmatrix} \tag{5.24}$$

$$u = v_{in} \tag{5.25}$$

$$y = v_{out} \tag{5.26}$$

Using the equations presented in (5.19) - (5.22), the matrices, a_2, b_2, c_2, may be derived as

$$a_2 = \begin{bmatrix} 0 & -\frac{1}{Lin_a} & 0 & 0 \\ \frac{1}{Ci_a} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_a} \\ 0 & 0 & \frac{1}{Co_a} & -\frac{1}{R.Co_a} \end{bmatrix}, b_2 = \begin{bmatrix} \frac{1}{Lin_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} \text{ and } c_2 = [0 \quad 0 \quad 0 \quad 1]$$

The complete representation of the state equations with the matrices are shown in equations (5.54) – (5.56).

$$\begin{bmatrix} \frac{di_{Lin_a}}{dt} \\ \frac{dv_{Ci_a}}{dt} \\ \frac{di_{L_a}}{dt} \\ \frac{dv_{Co_a}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{Lin_a} & 0 & 0 \\ \frac{1}{Ci_a} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_a} \\ 0 & 0 & \frac{1}{Co_a} & -\frac{1}{R.Co_a} \end{bmatrix} * \begin{bmatrix} i_{Lin_a} \\ v_{Ci_a} \\ i_{L_a} \\ v_{Co_a} \end{bmatrix} + \begin{bmatrix} \frac{1}{Lin_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} . v_{in} \qquad 5.27$$

Now, since equation (5.27) is derived for state-2 of switching sequence, it may be rewritten to demonstrate duty ratio, '$d^{/}$' of the switching cycle.

$$\begin{bmatrix} \frac{di_{Lin_a}}{dt} \\ \frac{dv_{Ci_a}}{dt} \\ \frac{di_{L_a}}{dt} \\ \frac{dv_{Co_a}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{Lin_a} & 0 & 0 \\ \frac{1}{Ci_a} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_a} \\ 0 & 0 & \frac{1}{Co_a} & -\frac{1}{R.Co_a} \end{bmatrix} * d^{/} * \begin{bmatrix} i_{Lin_a} \\ v_{Ci_a} \\ i_{L_a} \\ v_{Co_a} \end{bmatrix} + \begin{bmatrix} \frac{1}{Lin_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} * d^{/} * v_{in} \qquad 5.28$$

$$v_{out} = [0 \quad 0 \quad 0 \quad 1] * d^{/} * \begin{bmatrix} i_{Lin_a} \\ v_{Ci_a} \\ i_{L_a} \\ v_{Co_a} \end{bmatrix} \qquad 5.29$$

5.2. Small Signal Modelling

This sub-section discusses the small-signal modelling, which considers a small perturbation around a fixed operating point. Introducing a small perturbation in input inductor currents, $i_{Lin_a}$and i_{Lin_b}, input capacitor voltages, $v_{Ci1_a}$and v_{Ci2_a}, buck-boost inductor currents, $i_{L1_a}$and i_{L2_a}, output capacitor voltages, $v_{Co1_a}$and v_{Co2_a}, input source voltage, v_{in}, output voltage, v_{out}, duty ratio of the semi-conductor switches, d and $d^{/}$causes a corresponding perturbation in the state variables represented by those circuit parameters. The perturbed state-space equation variables are displayed in equations (5.30) – (5.37).

$$i_{Lin_a} = I_{Lin_a} + \widehat{i_{Lin_a}} \tag{5.30}$$

$$v_{Ci_a} = V_{Ci_a} + \widehat{v_{Ci_a}} \tag{5.31}$$

$$i_{L_a} = I_{L_a} + \widehat{i_{L_a}} \tag{5.32}$$

$$v_{Co_a} = V_{Co_a} + \widehat{v_{Co_a}} \tag{5.33}$$

$$v_{in} = V_{in} + \widehat{v_{in}} \tag{5.34}$$

$$v_{out} = V_{out} + \widehat{v_{out}} \tag{5.35}$$

$$d = D + \hat{d} \tag{5.36}$$

$$d^{/} = D^{/} - \hat{d} \tag{5.37}$$

In the above equations, the capitalized state variables represent the steady state values at a fixed operating point. The state variables in hat (^) representation are the small perturbations introduced in steady state parameters. It may be assumed that these perturbed variables are negligible as compared to the steady state values. Introducing the perturbed

variables in the equations (5.17), (5.18), (5.28) and (5.29), the new equations are displayed in (5.38), (5.39), (5.40) and (5.41).

$$\begin{bmatrix} \frac{d\left(I_{Lin_a}+\widehat{i_{Lin_a}}\right)}{dt} \\ \frac{d\left(V_{Ci_a}+\widehat{v_{Ci_a}}\right)}{dt} \\ \frac{d\left(I_{L_a}+\widehat{i_{L_a}}\right)}{dt} \\ \frac{d\left(V_{Co_a}+\widehat{v_{Co_a}}\right)}{dt} \end{bmatrix} \tag{5.38}$$

$$= \begin{bmatrix} 0 & -\frac{1}{Lin_a} & 0 & 0 \\ \frac{1}{Ci_a} & 0 & -\frac{1}{Ci_a} & 0 \\ 0 & \frac{1}{L_a} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R.Co_a} \end{bmatrix} * \left(D+\hat{d}\right) * \begin{bmatrix} I_{Lin_a}+\widehat{i_{Lin_a}} \\ V_{Ci_a}+\widehat{v_{Ci_a}} \\ I_{L_a}+\widehat{i_{L_a}} \\ V_{Co_a}+\widehat{v_{Co_a}} \end{bmatrix} + \begin{bmatrix} \frac{1}{Lin_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} * \left(D+\hat{d}\right) * \left(V_{in}+\widehat{v_{in}}\right)$$

$$V_{out}+\widehat{v_{out}} = [0 \quad 0 \quad 0 \quad 1] * \left(D+\hat{d}\right) * \begin{bmatrix} I_{Lin_a}+\widehat{i_{Lin_a}} \\ V_{Ci_a}+\widehat{v_{Ci_a}} \\ I_{L_a}+\widehat{i_{L_a}} \\ V_{Co_a}+\widehat{v_{Co_a}} \end{bmatrix} \tag{5.39}$$

$$\begin{bmatrix} \frac{d\left(I_{Lin_a}+\widehat{i_{Lin_a}}\right)}{dt} \\ \frac{d\left(V_{Ci_a}+\widehat{v_{Ci_a}}\right)}{dt} \\ \frac{d\left(I_{L_a}+\widehat{i_{L_a}}\right)}{dt} \\ \frac{d\left(V_{Co_a}+\widehat{v_{Co_a}}\right)}{dt} \end{bmatrix} \tag{5.40}$$

$$= \begin{bmatrix} 0 & -\frac{1}{Lin_a} & 0 & 0 \\ \frac{1}{Ci_a} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_a} \\ 0 & 0 & \frac{1}{Co_a} & -\frac{1}{R.Co_a} \end{bmatrix} * \left(D'-\hat{d}\right) * \begin{bmatrix} I_{Lin_a}+\widehat{i_{Lin_a}} \\ V_{Ci_a}+\widehat{v_{Ci_a}} \\ I_{L_a}+\widehat{i_{L_a}} \\ V_{Co_a}+\widehat{v_{Co_a}} \end{bmatrix} + \begin{bmatrix} \frac{1}{Lin_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} * \left(D'-\hat{d}\right) * \left(V_{in}+\widehat{v_{in}}\right)$$

$$V_{out} + \widehat{v_{out}} = [0 \quad 0 \quad 0 \quad 1] * \left(D^{/} - \hat{d}\right) * \begin{bmatrix} I_{Lin_a} + \widehat{i_{Lin_a}} \\ V_{Ci_a} + \widehat{v_{Ci_a}} \\ I_{L_a} + \widehat{i_{L_a}} \\ V_{Co_a} + \widehat{v_{Co_a}} \end{bmatrix} \tag{5.41}$$

In order to simplify the matrix operations of the perturbed state space averaged equations, the equations (5.38) - (5.41) derived in this sub-section may be written in the following representation as shown in equations (5.42) - (5.45).

$$\dot{x} + \hat{\dot{x}} = a_1 * \left(D + \hat{d}\right) * (X + \hat{x}) + b_1 * \left(D + \hat{d}\right) * (V_{in} + \widehat{v_{in}}) \tag{5.42}$$

$$V_{out} + \widehat{v_{out}} = c_1 * \left(D + \hat{d}\right) * (X + \hat{x}) \tag{5.43}$$

$$\dot{x} + \hat{\dot{x}} = a_2 * \left(D^{/} - \hat{d}\right) * (X + \hat{x}) + b_2 * \left(D^{/} - \hat{d}\right) * (V_{in} + \widehat{v_{in}}) \tag{5.44}$$

$$V_{out} + \widehat{v_{out}} = c_2 * \left(D^{/} - \hat{d}\right) * (X + \hat{x}) \tag{5.45}$$

The steady-state variables presented in equations (5.38) - (5.41) may be eliminated since upon averaging the equations pertaining to different steady-state duty ratios, D and $D^{/}$equate to zero since the average inductor voltage and capacitor currents equate to zero in a switching period, T_{sw}. Thus, these equations may be rewritten with only the perturbed average state variables. Also, the terms involving second-order perturbed variables on multiplication of the perturbed duty ratio and the perturbed system variables and input, output variables may also be neglected as they are very miniscule as compared to the steady state variables.

$$\hat{\dot{x}} = a_1 * D * \hat{x} + a_1 * \hat{d} * X + b_1 * D * \widehat{v_{in}} + b_1 * \hat{d} * V_{in} \tag{5.46}$$

$$\widehat{v_{out}} = c_1 * D * \hat{x} + c_1 * \hat{d} * X \tag{5.47}$$

$$\hat{\dot{x}} = a_2 * D^{/} * \hat{x} - a_2 * \hat{d} * X + b_2 * D^{/} * \widehat{v_{in}} - b_2 * \hat{d} * V_{in} \tag{5.48}$$

$$\widehat{v_{out}} = c_2 * D^{/} * \hat{x} - c_2 * \hat{d} * X \tag{5.49}$$

Now, for the sake of simplicity of matrix operations and to derive the transfer functions for determining the relation between output voltage and duty ratio and output voltage to input voltage, these time domain equations have been averaged and the averaged equations are shown in equations (5.50) - (5.53).

$$\hat{\dot{x}} = a_1 * D * \hat{x} + a_1 * \hat{d} * X + b_1 * D * \widehat{v_{in}} + b_1 * \hat{d} * V_{in} + a_2 * D' * \hat{x} - a_2 * \hat{d} * X + b_2 * D' * \widehat{v_{in}} - b_2 * \hat{d} * V_{in} \quad (5.50)$$

$$\Longrightarrow \hat{\dot{x}} = \left(a_1.D + a_2.D'\right) * \hat{x} + (a_1 - a_2) * \hat{d} * X + \left(b_1.D + b_2.D'\right) * \widehat{v_{in}} + (b_1 - b_2) * \hat{d} * V_{in} \quad (5.51)$$

$$\widehat{v_{out}} = c_1 * D * \hat{x} + c_1 * \hat{d} * \hat{x} + c_2 * D' * \hat{x} - c_2 * \hat{d} * X \quad (5.52)$$

$$\Longrightarrow \widehat{v_{out}} = \left(c_1.D + c_2.D'\right) * \hat{x} + (c_1 - c_2) * \hat{d} * X \quad (5.53)$$

For the sake of simplicity, equations (5.51) and (5.53) may be transformed to frequency domain using Laplace transformation. The new frequency domain state space equations may be seen in following subsection 5.3.

5.3. Open Loop Frequency Domain Plots

On applying Laplace transformation to equations (5.51) and (5.53), the equations may be re-written as follows:

$$sI\widehat{x(s)} = \left(a_1.D + a_2.D'\right) * \widehat{x(s)} + (a_1 - a_2) * \widehat{d(s)} * X(s) + \left(b_1.D + b_2.D'\right) * \widehat{v_{in}(s)} + (b_1 - b_2) * \widehat{d(s)} * V_{in}(s) \quad (5.54)$$

$$\Longrightarrow \left[sI - \left(a_1.D + a_2.D'\right)\right]\widehat{x(s)} = (a_1 - a_2) * \widehat{d(s)} * X(s) + \left(b_1.D + b_2.D'\right) * \widehat{v_{in}(s)} + (b_1 - b_2) * \widehat{d(s)} * V_{in}(s) \quad (5.55)$$

$$\Rightarrow \widehat{x(s)} = \left[sI - \left(a_1.D + a_2.D'\right)\right]^{-1}$$

$$* \begin{Bmatrix} (a_1 - a_2) * \widehat{d(s)} * X(s) \\ +\left(b_1.D + b_2.D'\right) * \widehat{v_{in}(s)} + (b_1 - b_2) * \widehat{d(s)} * V_{in}(s) \end{Bmatrix} \quad 5.56$$

$$\widehat{v_{out}} = \left(c_1.D + c_2.D'\right) * \hat{x} + (c_1 - c_2) * \hat{d} * X \quad 5.57$$

$$\Rightarrow \widehat{v_{out}(s)} = \left(c_1.D + c_2.D'\right) * \widehat{x(s)} + (c_1 - c_2) * \widehat{d(s)} * X \quad 5.58$$

Substituting $\widehat{x(s)}$ from equation (5.56) into equation (5.58), we have,

$$\Rightarrow \widehat{v_{out}(s)} = \left(c_1.D + c_2.D'\right) * \left[sI - \left(a_1.D + a_2.D'\right)\right]^{-1}$$

$$* \begin{Bmatrix} (a_1 - a_2) * \widehat{d(s)} * X(s) \\ +\left(b_1.D + b_2.D'\right) * \widehat{v_{in}(s)} + (b_1 - b_2) * \widehat{d(s)} * V_{in}(s) \end{Bmatrix} \quad 5.59$$

$$+(c_1 - c_2) * \widehat{d(s)} * X$$

It may be noted that the selection of components of the 3-Ø CPC PLC have already been discussed in Chapter 4. The parameters of each components that are required to derive the matrices a_1, a_2, b_1, b_2, c_1, and c_2 are tabulated in Table 5-2.

Table 5-2: List of values from selected components for state space variables

Parameters	Values
Lin_a	0.5mH
Ci_a	10µF
Co_a	10µF
L_a	0.5mH
R	100-Ω

The values of the parameters pertaining to the operating condition of the 3-Ø CPC -PLC are displayed in Table 5-3.

Table 5-3: Operating condition parameters

Parameters	Values
V_{in}	$170V_{peakline-line}$
V_{out}	$170V_{peakline-line}$
D	0.5
$D^{/}$	0.5
I_{Lin_a}	$5A_{peak}$
V_{Ci_a}	$170V_{peakline-line}$
I_{L_a}	$5A_{peak}$
V_{Co_a}	$170V_{peakline-line}$

Equation (5.59) have been computed using the values from Table 5-2 and Table 5-3. For ease of computation, a Matlab program has been written to enter the parameters, derive the matrices and finally deduce the equation (5.59) in numerical format with all the values plugged in. Matlab computed matrices a_1, a_2, b_1, b_2, c_1, and c_2 and their values are shown below:

$$a_1 = (1.0 * 10^5) * \begin{bmatrix} 0 & -0.02 & 0 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & 0.02 & 0 & 0 \\ 0 & 0 & 0 & -0.01 \end{bmatrix},$$

$$a_2 = \left(1.0 * 10^5\right) * \begin{bmatrix} 0 & -0.02 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -0.02 \\ 0 & 0 & 1 & -0.01 \end{bmatrix}$$

$$b_1 = \begin{bmatrix} 2000 \\ 0 \\ 0 \\ 0 \end{bmatrix} \text{ and } c_1 = [0 \quad 0 \quad 0 \quad 1]$$

$$b_2 = \begin{bmatrix} 2000 \\ 0 \\ 0 \\ 0 \end{bmatrix} \text{ and } c_2 = [0 \quad 0 \quad 0 \quad 1]$$

Introducing these numerical matrices a_1, a_2, b_1, b_2, c_1, and c_2 in equation (5.59), we may derive two transfer functions. One of these transfer functions represent the relation between perturbed output voltage variable to perturbed duty ratio, known as output to duty ratio transfer function, whereas the other transfer function shows the relation between perturbed output voltage and perturbed input voltage, known as output to input transfer function.

In designing the closed loop controller to determine duty ratio based on desired output voltage reference command, the output to duty ratio transfer function is studied in this sub-section and a controller transfer function is derived in the following sub-section to improve the command-following and transient performance of the 3-Ø CPC -PLC.

Matlab-computed output to duty ratio transfer function is displayed below:

$$G_{vod} = \frac{\widehat{v_{out}}}{\hat{d}} \tag{5.60}$$

$$G_{vod} = \frac{-(5 * 10^5)s^3 + (34 * 10^9)s^2 - (150 * 10^{12})s + (6.8 * 10^{18})}{s^4 + 1000s^3 + (3 * 10^8)s^2 + (2.5 * 10^{11})s + (1 * 10^{16})} \tag{5.61}$$

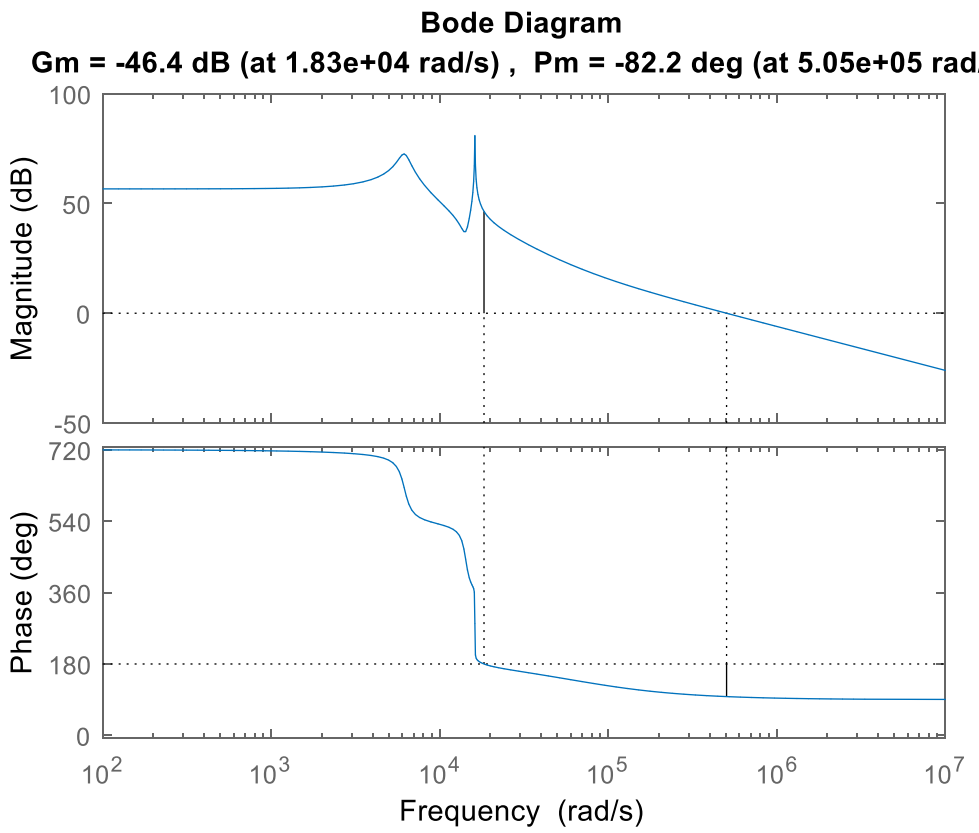


Figure 5-8: Bode magnitude and phase plot for output to duty ratio transfer function,G_{vod}.

As may be seen from Figure 5-8, the Bode magnitude plot has a gain margin of -46.4 dB at a phase cross-over angular frequency of $1.83*10^4$ rad/sec. It implies the system is unstable and any attempt at closing the loop with a feedback would result in a highly unstable system where the system output magnitude would continue increasing until it reaches saturation limit depending on the circuit. It may also be seen that the phase margin is -82.2 degrees at a gain cross-over angular frequency of $5.05*10^5$ rad/sec. This implies any perturbation in system phase or any signal time delay error would be magnified instead of being reduced by the controller. In order to gain better understanding of the system, the pole zero map of the system for G_{vod} is shown in Figure 5-9.

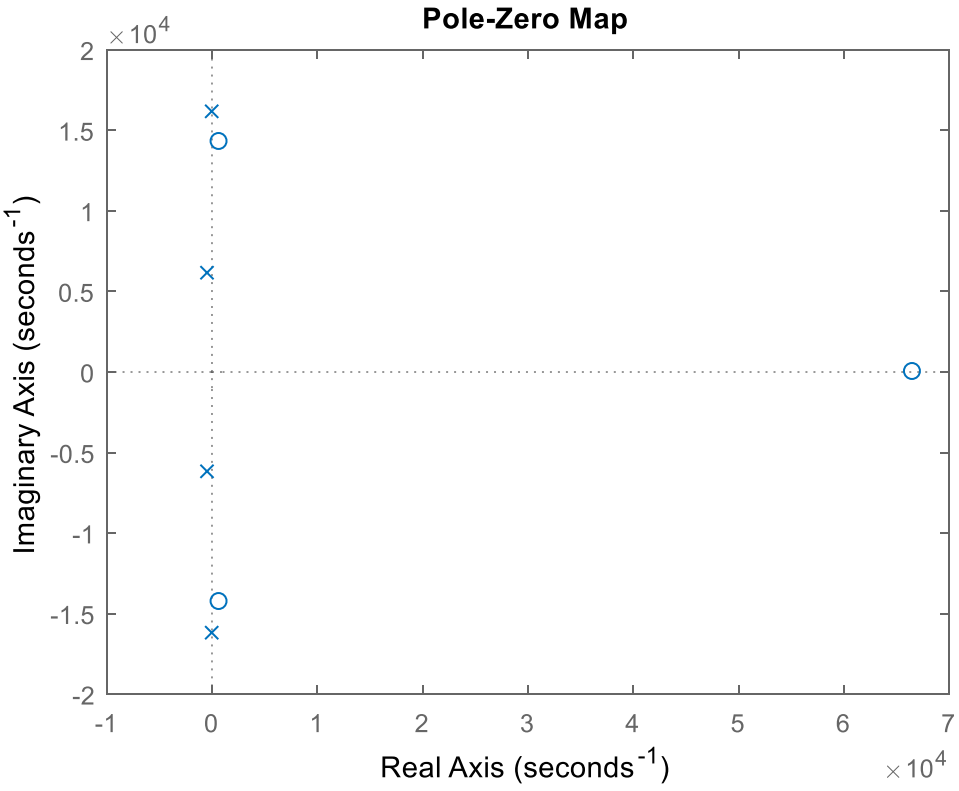


Figure 5-9: Pole-zero map for output to duty ratio transfer function, G_{vod} (poles are marked as 'x' and zeros are marked as 'o').

As may be seen from Figure 5-9, there is one right-half plane zero which is far from the imaginary axis. The poles are located on the left-hand side of the imaginary axis or on the axis itself, whereas there are two more zeros which are near to imaginary axis but located on the right-hand side of the axis. This tells us the controller needs to introduce a pole which should negate the effect of the zeros. The design of the controller is discussed in the next sub-section.

5.4. Controller Design

As we analyzed the system in sub-section (5.2), we perturbed the system and tried to observe the system dynamics in sub-section (5.3). This sub-section discusses the design of a feedback controller to achieve desired command input operation of the system and also to improve system dynamics under transient conditions.

5.4.1 Controllability Test

We know, a system is controllable when we can achieve desired dynamic operation of the system under a controlled command input as reference. It may be determined if the designed converter system is controllable or observable by applying the Controllability and Observability Test which was conceptualized for the first time by R. Kalman in 1960 [xx]. This test states that in frequency domain analysis, for a system with state space equation in the format displayed in equations (5.5) and (5.6), the system is controllable and observable only and only if the transfer function has no zeros and poles which cancel each other. Now, if there are pole-zero cancellations, then the system might be uncontrollable or unobservable or both uncontrollable and unobservable.

$$H_c(s) = C(sI - A)^{-1}B \qquad 5.62$$

Where $C = c_1^T d + c_2^T d/$

$$A = a_1 d + a_2 d/$$

$$B = b_1 d + b_2 d/$$

Using the values of matrices, a_1, a_2, b_1, b_2, c_1, c_2 ,and duty ratio, d and $d/$ presented in sub-section (5.3), we use Matlab to determine if the transfer function $H_c(s)$ has any pole-zero cancellation.

The controllability transfer function for CPC PLC is shown in equation (5.63).

$$H_c(s) = \frac{1 * 10^{16}}{s^4 + 1000s^3 + (3 * 10^8)s^2 + (2.5 * 10^{11})s + (1 * 10^{16})} \qquad 5.63$$

The poles and zeros are tabulated below for the above transfer function equation (5.63) in Table 5-4.

Table 5-4: Poles and zeros of transfer function $H_c(s)$

Poles	Zeros
-2.627071657443980*10^{01} + 1.617851730212626*10^{04}i	0
-2.627071657443980*10^{01} - 1.617851730212626*10^{04}i	
-4.737292834255615*10^{02} + 6.162847352427699*10^{03} i	
-4.737292834255615*10^{02} - 6.162847352427699*10^{03} i	

It may be seen from Table 5-4 that no pole and zero cancel each other in the pole-zero plane in frequency domain (s-plane). This demonstrates the fact that the designed converter system is both controllable and observable. The next sub-section (5.4.2) discusses the controller design for CPC PLC converter.

5.4.2. Controller Transfer Function

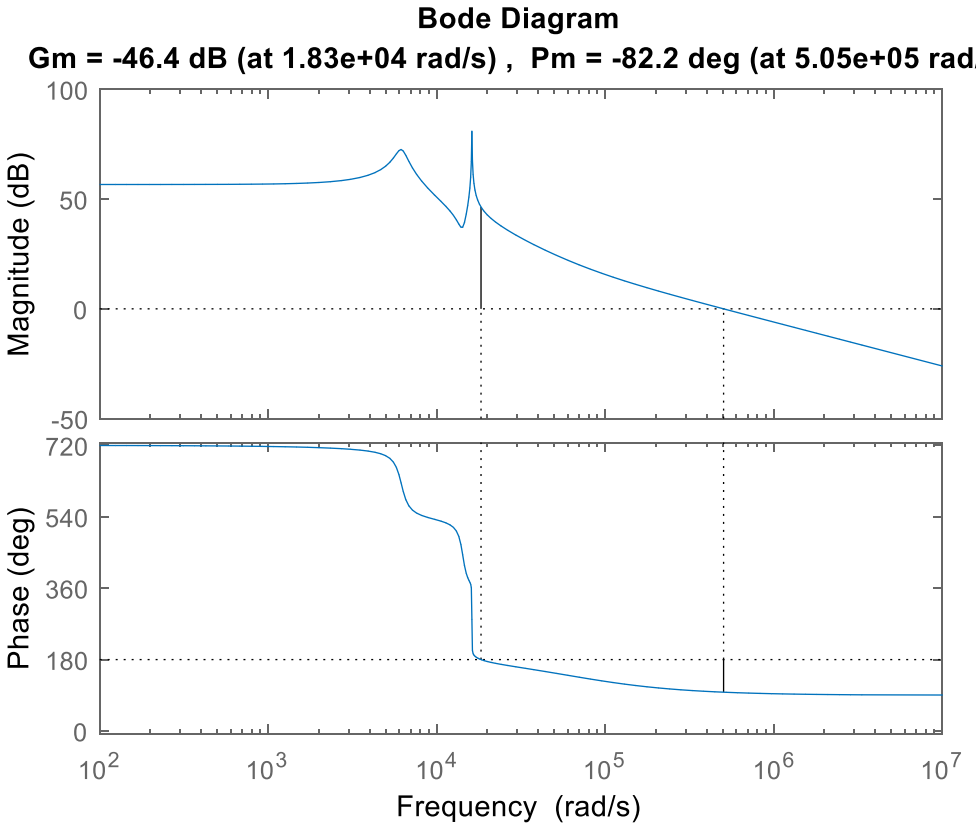


Figure 5-10: Bode magnitude and phase plot for uncompensated output to duty ratio transfer function, G_{vod}

The Bode magnitude and phase plots for uncompensated output to duty ratio transfer function, G_{vod}, displayed in Figure 5-10, is utilized to determine the feedback compensator design. The design principle presented in this sub-section is to establish required gain magnitude at phase cross-over frequency before the resonant frequency as well as to achieve desired phase margin at gain cross-over frequency. The objective of this design is to achieve a gain margin of at least 10 dB as well as to achieve a phase margin greater than 60 degrees. Another goal of this design approach is also to have high negative gain magnitude at higher frequencies to achieve attenuation of high frequency disturbances.

An integral controller is first introduced to the system, which represents a pole at the origin. This achieves the rejection of high frequency harmonics as well as introduces a negative phase shift of 90 degrees. The transfer function of compensator, H_{comp} in frequency domain is shown in equation (5.87).

$$H_{comp} = \frac{k_I}{s} \tag{5.87}$$

Here, k_I is the integral gain which has been considered as 0.5. The Bode magnitude and plot of the compensator is shown in Figure 5-11.

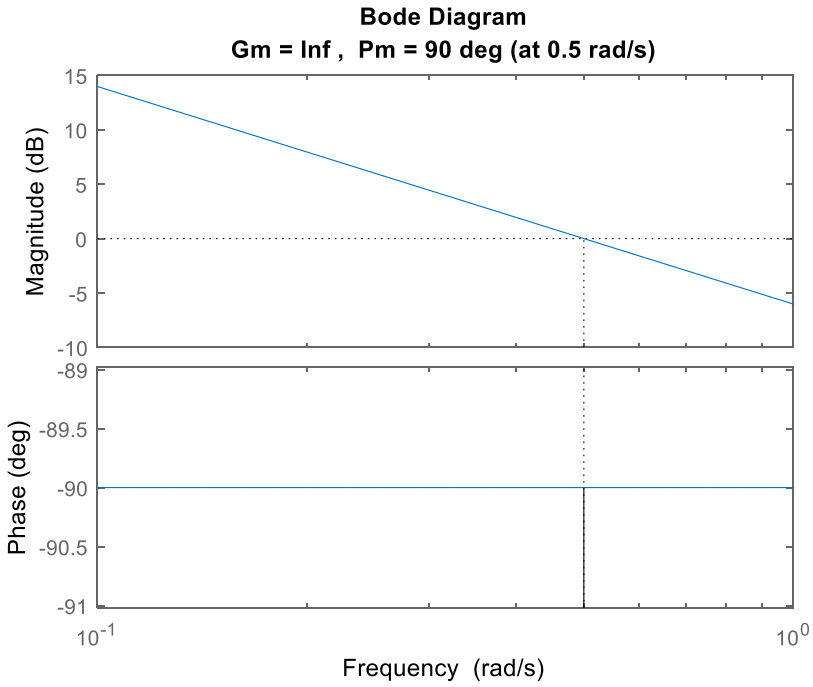


Figure 5-11: Bode magnitude and phase plots for compensator transfer function, H_{comp}

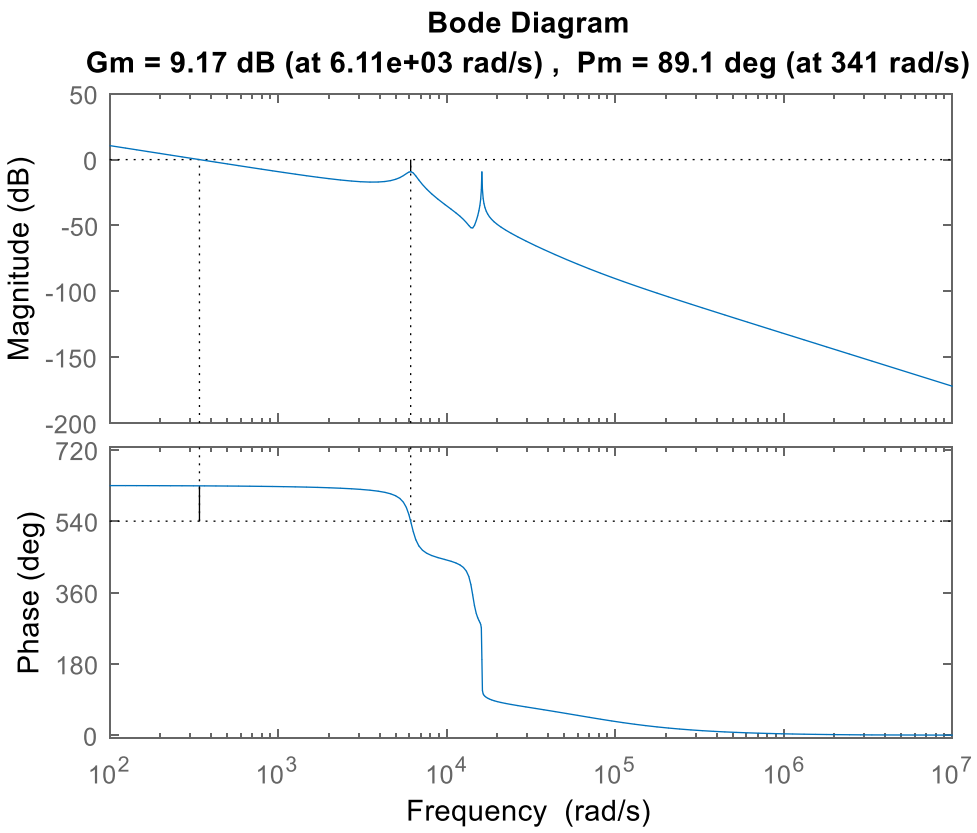


Figure 5-12: Bode magnitude and phase plots for compensated transfer function, $Gvod_{oltf} * H_{comp}$

It may be seen from Figure 5-12 that the compensated bode plot shows a gain margin of about 10 db at the phase cross-over angular frequency of $6.11*10^4$ rad/sec. Now, it may be further seen from the Bode magnitude plot that desired gain magnitude before the cross over frequency is also achieved. The Bode phase plot shows a Phase margin of 89.1 degrees at the gain cross-over angular frequency of 341 rad/sec. This is the effect induced by the integral compensator, which may be understood by observing the Bode magnitude and phase plots displayed in Figure 5-11. This integral compensator design seems to also have high attenuation at higher frequencies. To further verify the performance of the system during transient conditions, the unit step response plot for the system is displayed in the following figures.

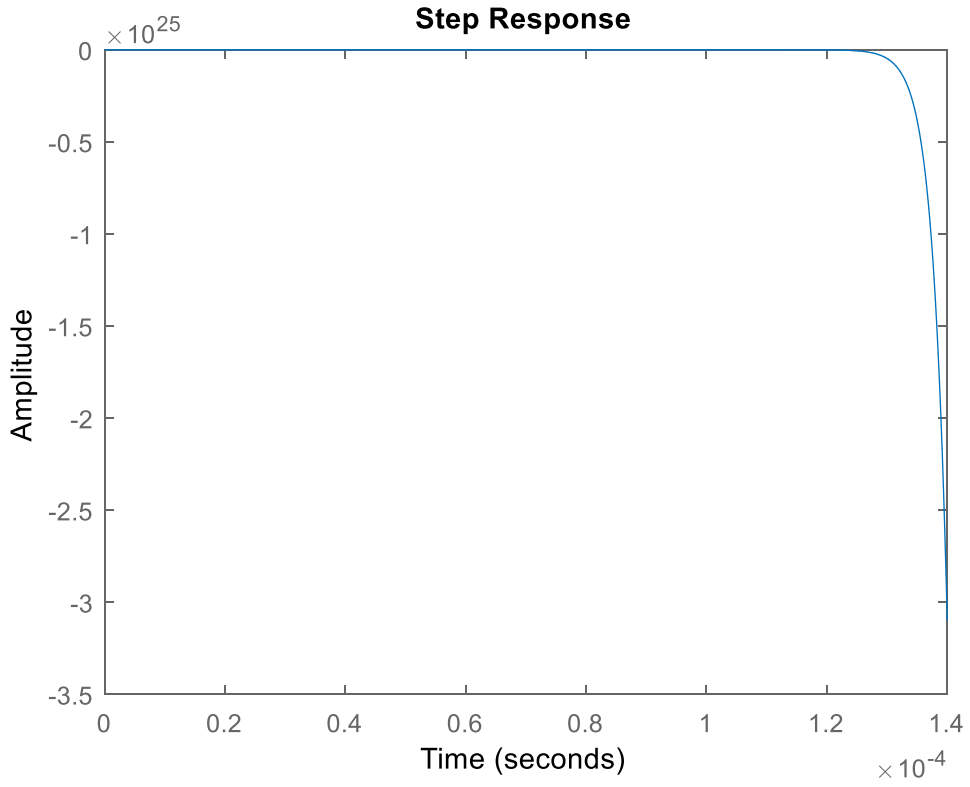


Figure 5-13: Step response plot for uncompensated output to duty ratio transfer function,G_{vod}

As may be observed from Figure 5-13, with step change in input which is duty ratio for the system represented by this transfer function, the system goes unstable at 0.14ms. This shows that the system is inherently marginally stable. In order to stabilize the system to demonstrate command -following performance, the controller is added to the system. The performance of the system with the controller designed in this sub-section may be analyzed from the step response plot of the compensated transfer function, $Gvod_{oltf} * H_{comp}$. This plot is displayed in Figure 5-14.

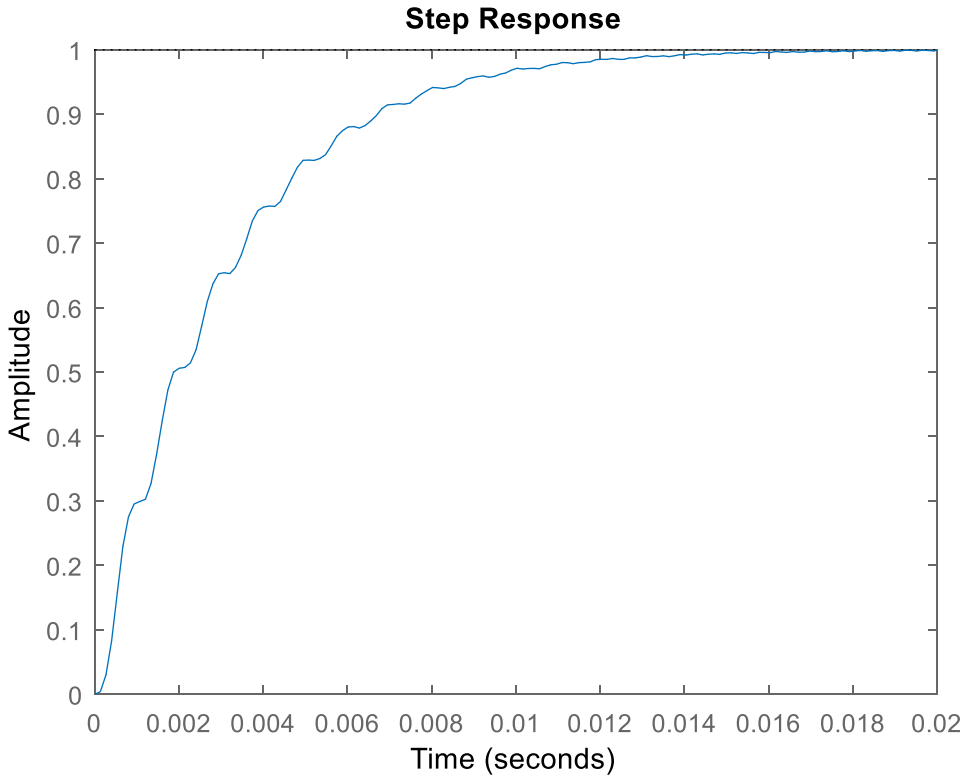


Figure 5-14: Step response plot of the compensated transfer function, $Gvod_{oltf} * H_{comp}$

It may be seen from Figure 5-14, that with introduction of the controller, with step change in duty cycle, the system reacts in an overdamped manner and settles to the desired new output value with a settling time of 16ms. This observation is critical as we know the time-period of a single cycle of an ac voltage signal is 16ms. Thus, it may be noted that with step change in desired output command, the converter controller will change the duty cycle in such a way the converter output voltage will settle to the desired new output value within one cycle of the voltage signal.

Therefore, it may be concluded that the design objectives for the feedback compensator specified at the beginning of this sub-section have been achieved. This feedback compensator will be implemented in the detailed Matlab-Simulink model of CPC PLC for controlling the output voltage at desired command reference. The simulation model and its analysis are discussed in detail in Chapter-8.

6. Chapter Six: Simulation Results

6.1 Introduction

This chapter presents a simulation model of 3-Ø Center-Point-Clamped Power Line Conditioner (CPC PLC). This model has been designed in Matlab-Simulink for a $120V_{rmsline\text{-}line,}$ 500W 3-Ø application. A detailed representative circuit of 3-Ø CPC PLC, which has been modelled in Matlab-Simulink has been presented in Figure 6-1.

Table 6-1: List of values from selected components for state space variables

Parameters	Values
Lin_a, Lin_b, Lin_c	0.5-mH
$R_{Lin_a}, R_{Lin_b}, R_{Lin_c}$	38-mΩ
$Ci1_a, Ci2_a, Ci1_b, Ci2_b, Ci1_c, Ci2_c$	10-µF
$R_{Ci1_a}, R_{Ci2_a}, R_{Ci1_b}, R_{Ci2_b}, R_{Ci1_c}, R_{Ci2_c}$	22- mΩ
$L1_a, L2_a, L1_b, L2_b, L1_c, L2_c$	0.5-mH
$R_{L1_a}, R_{L2_a}, R_{L1_b}, R_{L2_b}, R_{L1_c}, R_{L2_c}$	38-mΩ
$Co1_a, Co2_a, Co1_b, Co2_b, Co1_c, Co2_c$	10-µF
$R_{Co1_a}, R_{Co2_a}, R_{Co1_b}, R_{Co2_b}, R_{Co1_c}, R_{Co2_c}$	22- mΩ
R_a, R_b, R_c	100-Ω

The values of the circuit parameters of 3-Ø CPC PLC are shown in Table 3-1Table 6-1. The Matlab-Simulink model has been modelled with the values from the table presented above. The simulation results verifying the operation methodology of 3-Ø CPC PLC has been discussed in the subsequent sub-sections of this chapter.

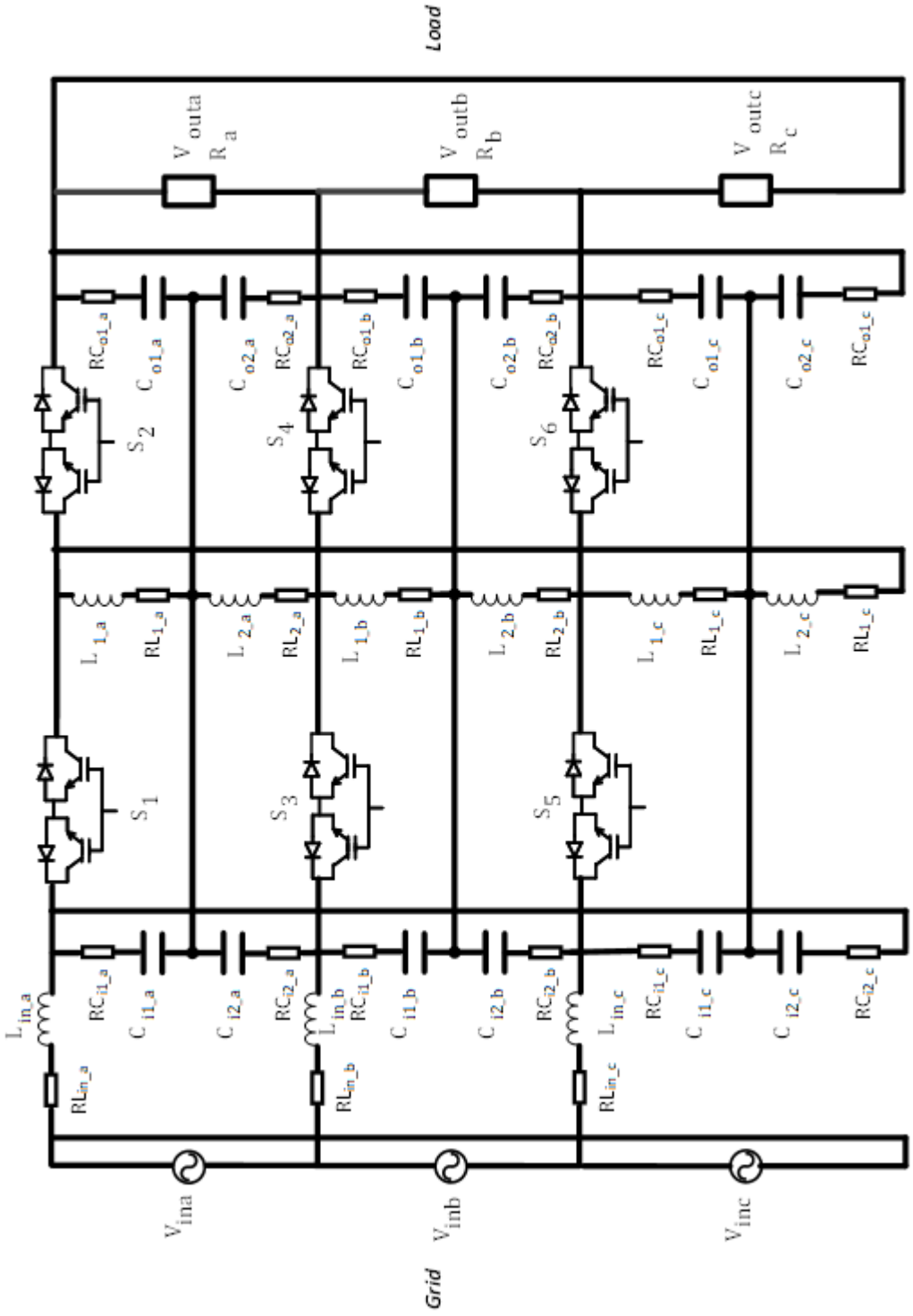


Figure 6-1: Detailed circuit schematic of the 3-Ø CPC PLC.

As may be seen from Figure 6-1: Detailed circuit schematic of the 3-Ø CPC PLC., the 3-Ø CPC PLC has three phase voltage input with V_{in_a}, $V_{in_b}$and, V_{in_c} being the voltages across the three phase which are connected in delta configuration. There are inductors, Lin_a, Lin_b, Lin_c in between the source and the converter topology to attenuate switching harmonics from being fed back into the source. The parasitic resistances, $R_{Lin_a}, R_{Lin_b}, R_{Lin_c}$ associated with the inductors are also shown in the converter schematic. There are three pairs of capacitor, $Ci1_a, Ci2_a, Ci1_b, Ci2_b, Ci1_c, Ci2_c$ in the input side for providing access to the center-point of each line voltage. The parasitic resistances, $R_{Ci1_a}, R_{Ci2_a}, R_{Ci1_b}, R_{Ci2_b}, R_{Ci1_c}, R_{Ci2_c}$ associated with these capacitors are also included the converter schematic. There are three bi-directional switches in the circuit schematic which may be termed as input switches, S_1, S_3 and, S_5. There are three pairs of inductors, $L1_a, L2_a, L1_b, L2_b, L1_c, L2_c$ after the input switches, which are the buck-boost energy transferring inductors. The parasitic resistances, $R_{L1_a}, R_{L2_a}, R_{L1_b}, R_{L2_b}, R_{L1_c}, R_{L2_c}$ associated with these inductors have also been considered for modelling. There are three more bi-directional switches, S_2, S_4 and, S_6, which may be termed as output switches. The output switches are followed by three pairs of output capacitors, $Co1_a, Co2_a, Co1_b, Co2_b, Co1_c, Co2_c$ connected in delta configuration for providing access to the center-point of the output voltage. They have modelled with the parasitic resistances, $R_{Co1_a}, R_{Co2_a}, R_{Co1_b}, R_{Co2_b}, R_{Co1_c}, R_{Co2_c}$ associated with them. The output is connected to a 3-Ø delta-connected resistive load, R_a, R_b, R_c. The Matlab-Simulink based simulation model presented in Figure 6-2 exactly follows the representative 3-Ø CPC PLC circuit shown in Figure 6-1.

6.2. Open-Loop 3-Ø CPC PLC Simulation Model

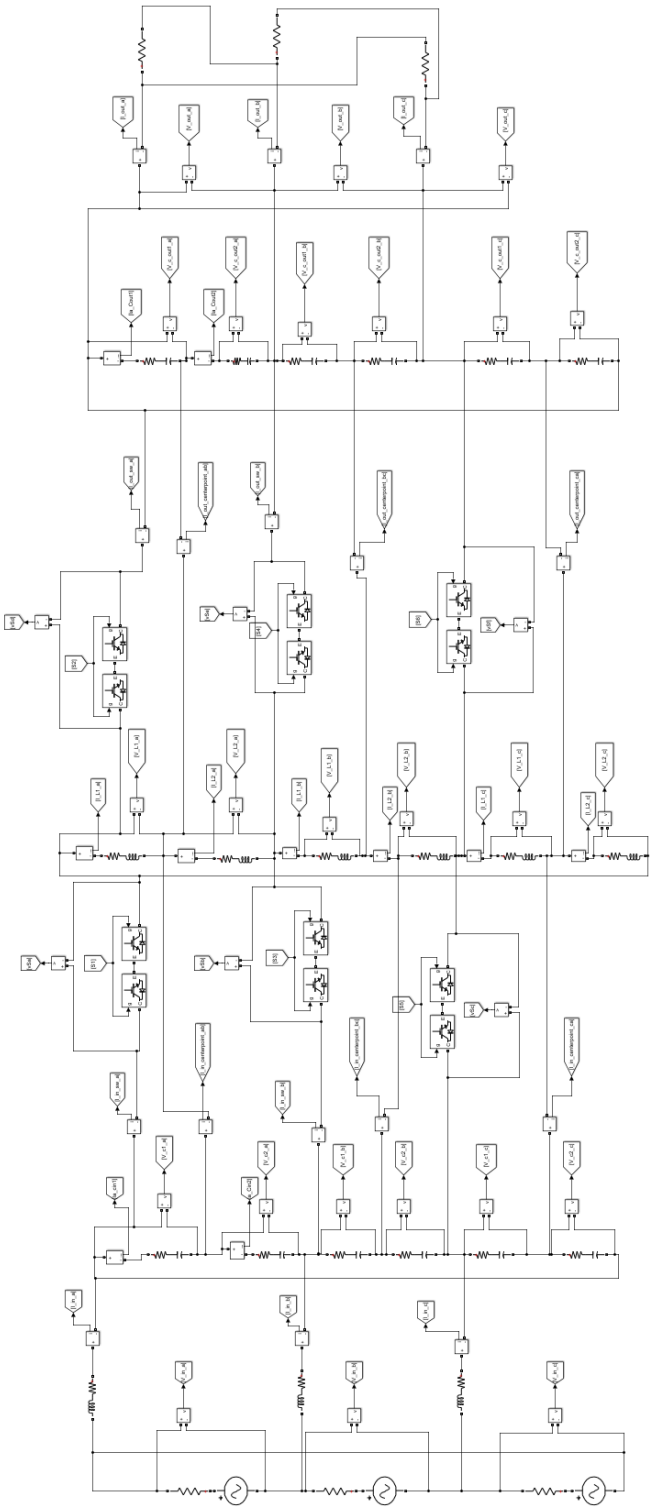


Figure 6-2: Snapshot of Matlab-Simulink model of 3-Ø CPC PLC

A snapshot of the simulation model designed in Matlab-Simulink is provided in Figure 6-2. It may be observed that current and voltage sensors have been placed to measure the voltage and current applied to each individual components of the circuit. These voltage and current waveforms associated with each circuit components for open-loop duty ratio operation of 3-Ø CPC PLC has been presented in this sub-section (6.3.1).

As may be seen from Figure 6-3, the input source voltage to CPC PLC has a rms value of $120V_{line\text{-}line}$. Each phase of the input source voltage are 120 degrees apart from each other. The corresponding load voltage for an open-loop duty ratio of 0.5 is displayed in Figure 6-4. It may be observed that the output load voltage also has a rms value of $120V_{line\text{-}line,}$ but phase a of input source voltage and phase a of output load voltage has a phase-shift of 180 degrees. This is a classical characteristic of a buck-boost converter which has been earlier explained in Chapter-3. Furthermore, each phase of the output voltage are 180 degrees apart from each other.

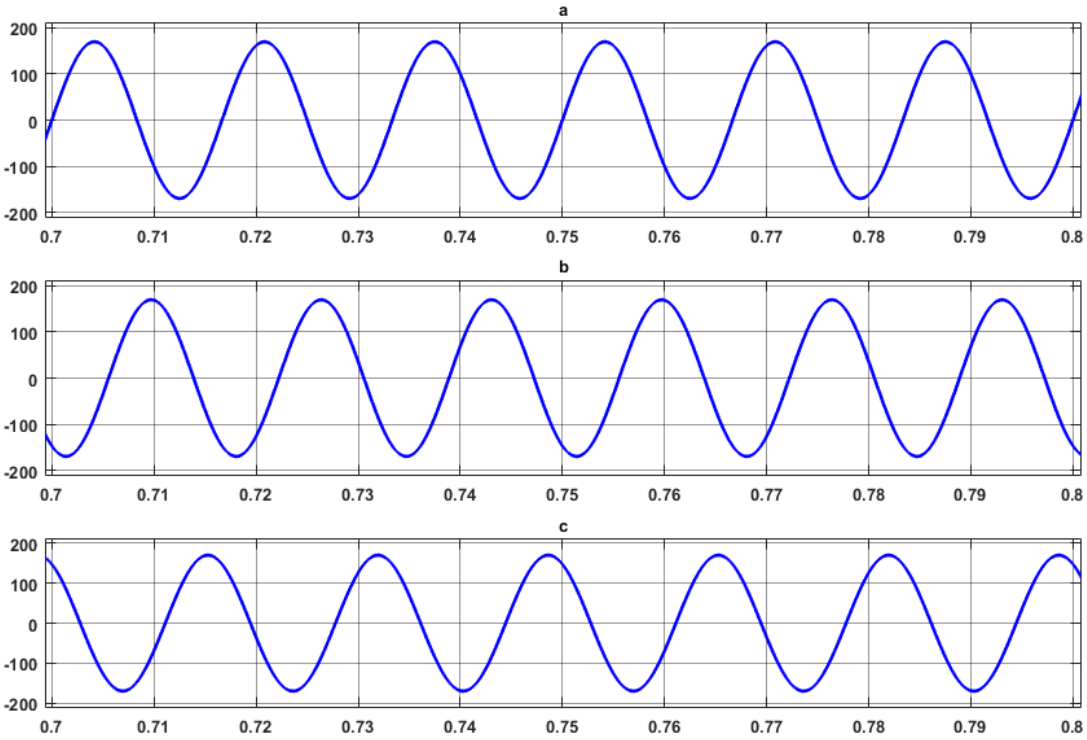


Figure 6-3: Input source voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

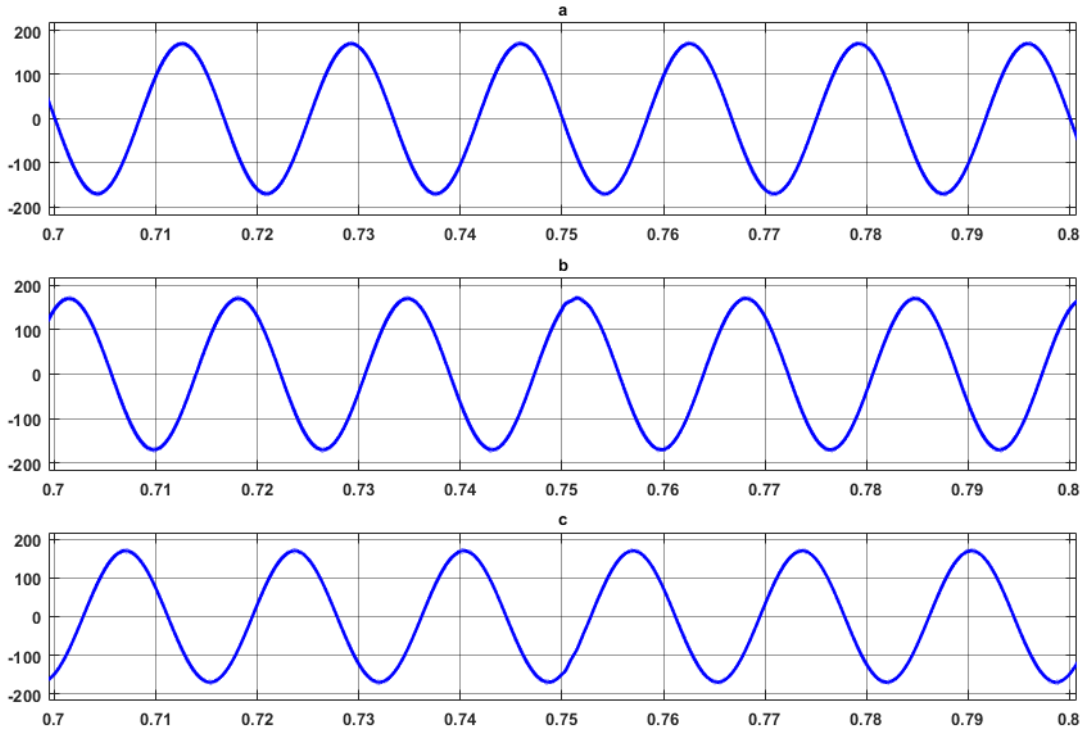


Figure 6-4: Output load voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

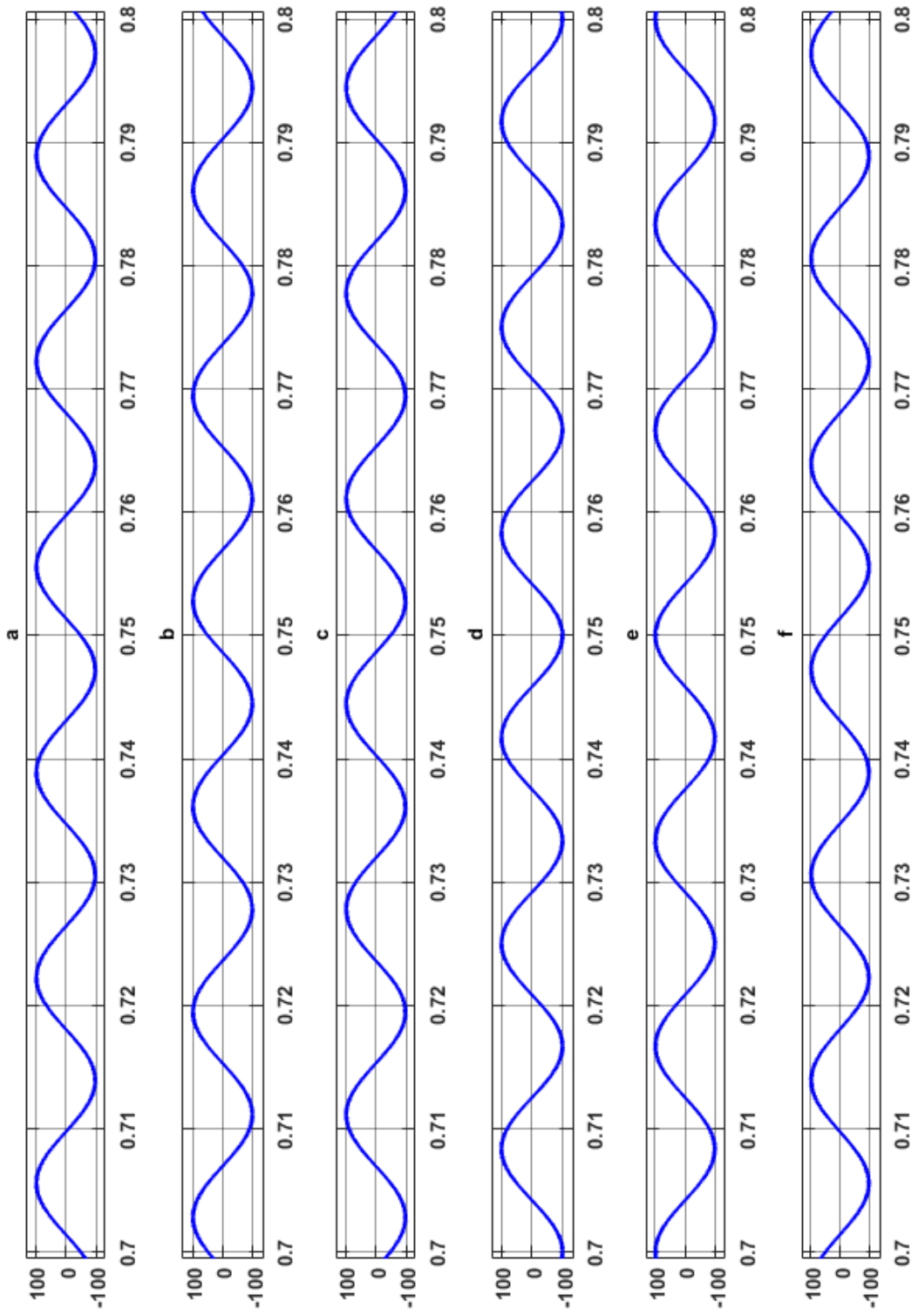


Figure 6-5: Input capacitor voltages (a) Voltage across input capacitor, C_{i1_a}, (b) Voltage across input capacitor, C_{i2_a}, (c) Voltage across input capacitor, C_{i1_b}, (d) Voltage across input capacitor, C_{i2_b}, (c) Voltage across input capacitor, C_{i1_c}, and (d) Voltage across input capacitor, C_{i2_c}.

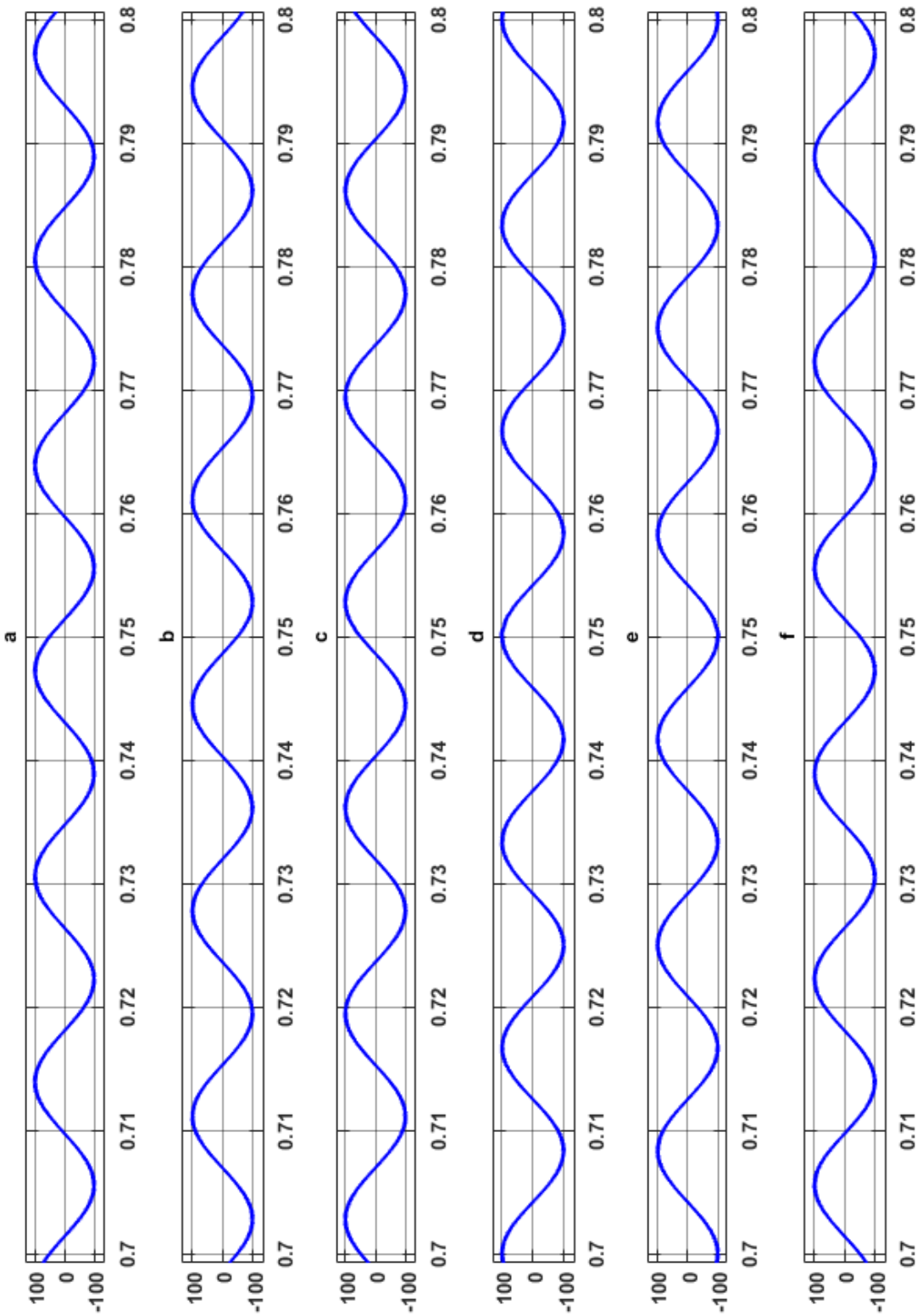


Figure 6-6: Output capacitor voltages a) Voltage across input capacitor, C_{o1_a}, (b) Voltage across input capacitor, C_{o2_a}, (c) Voltage across input capacitor, C_{o1_b}, (d) Voltage across input capacitor, C_{o2_b}, (c) Voltage across input capacitor, C_{o1_c}, and (d) Voltage across input capacitor, C_{o2_c}.

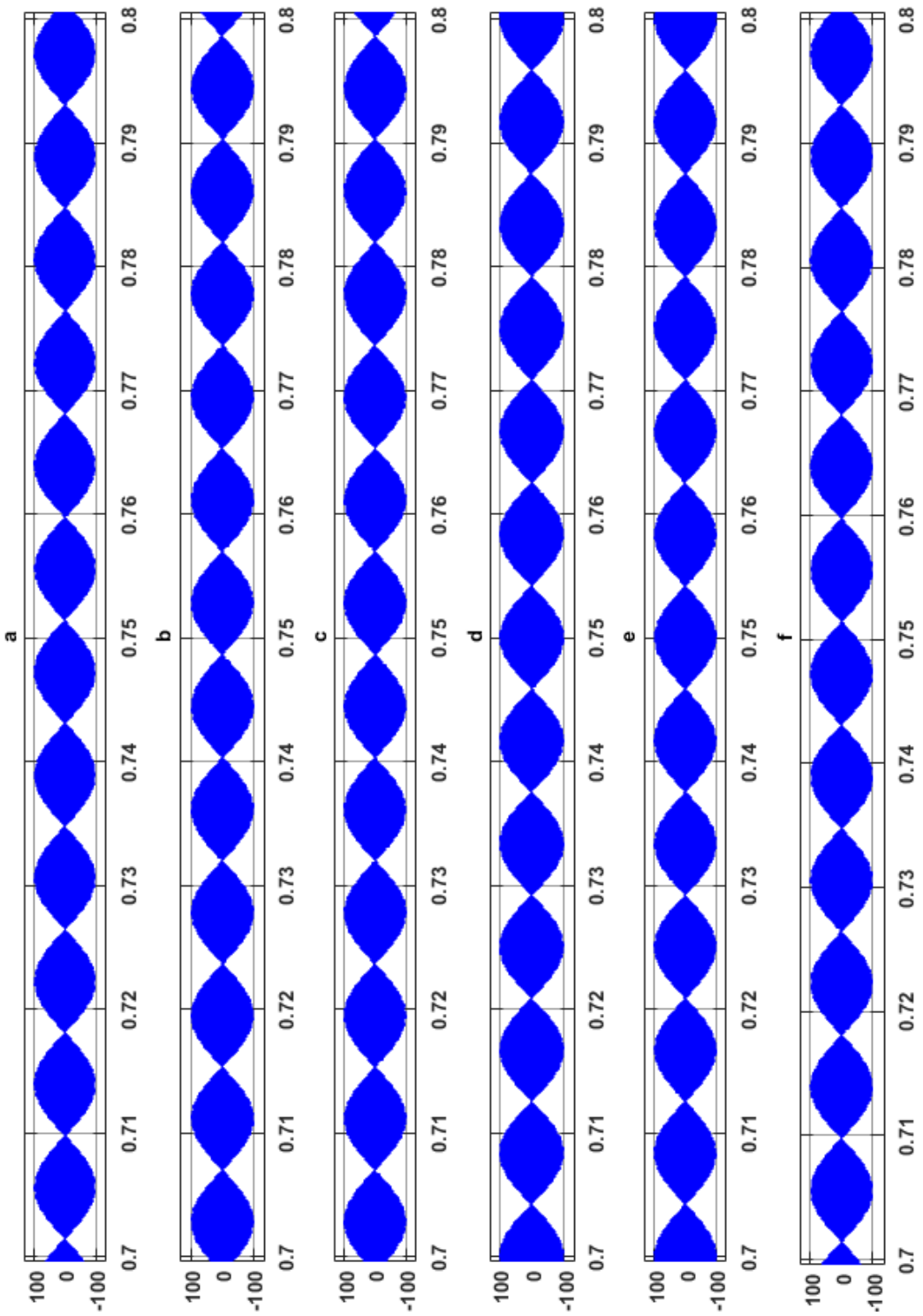


Figure 6-7: Buck-boost inductor voltages (a) Voltage across inductor, L_{1_a}, (b) Voltage across inductor, L_{2_a}, (c) Voltage across inductor, L_{1_b}, (d) Voltage across inductor, L_{2_b}, (e) Voltage across inductor, L_{1_c}, and (f) Voltage across inductor, L_{2_c}

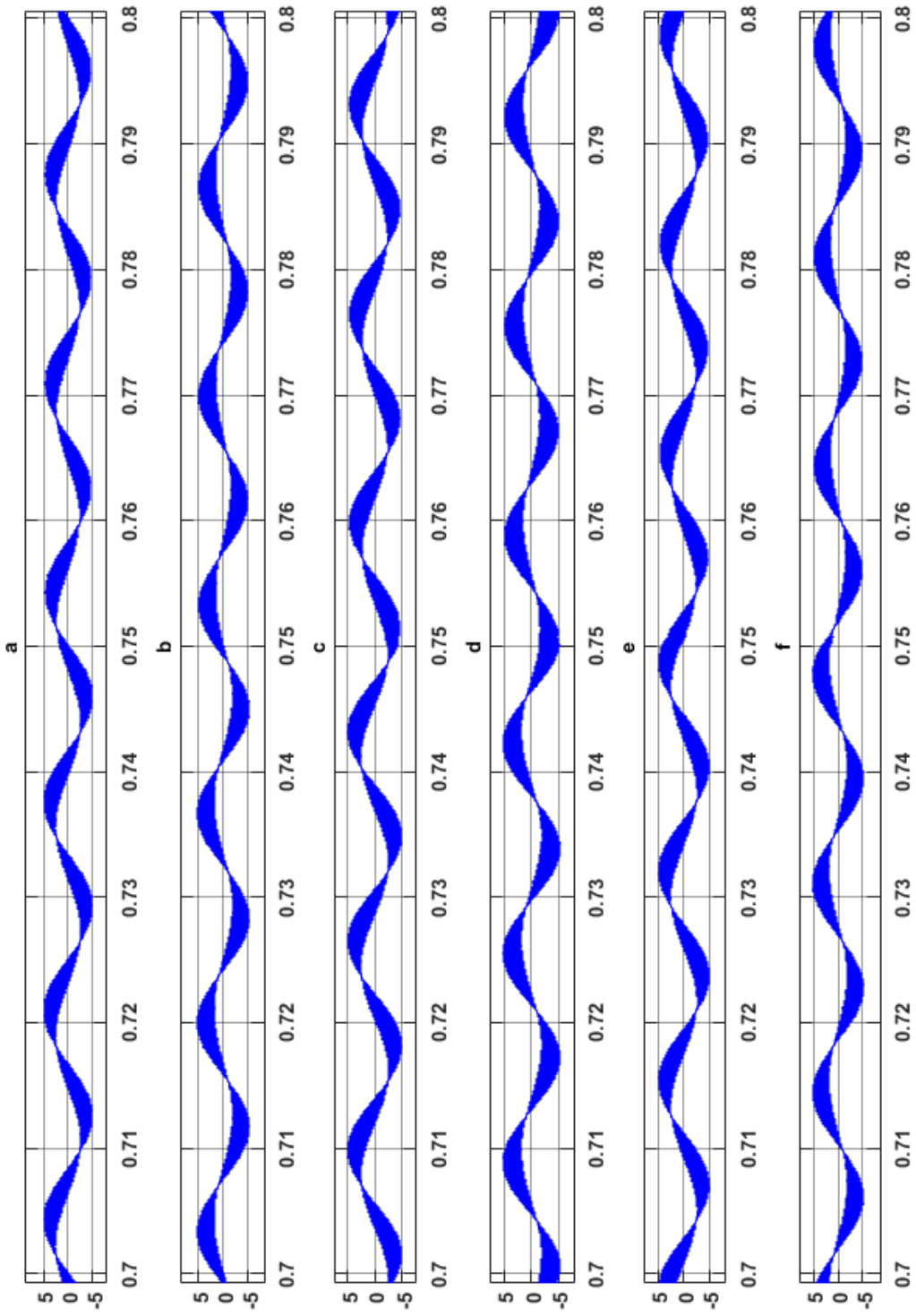


Figure 6-8: Buck-boost inductor currents (a) Current across inductor, L_{1_a}, (b) Current across inductor, L_{2_a}, (c) Current across inductor, L_{1_b}, (d) Current across inductor, L_{2_b}, (e) Current across inductor, L_{1_c}, and (f) Current across inductor, L_{2_c}

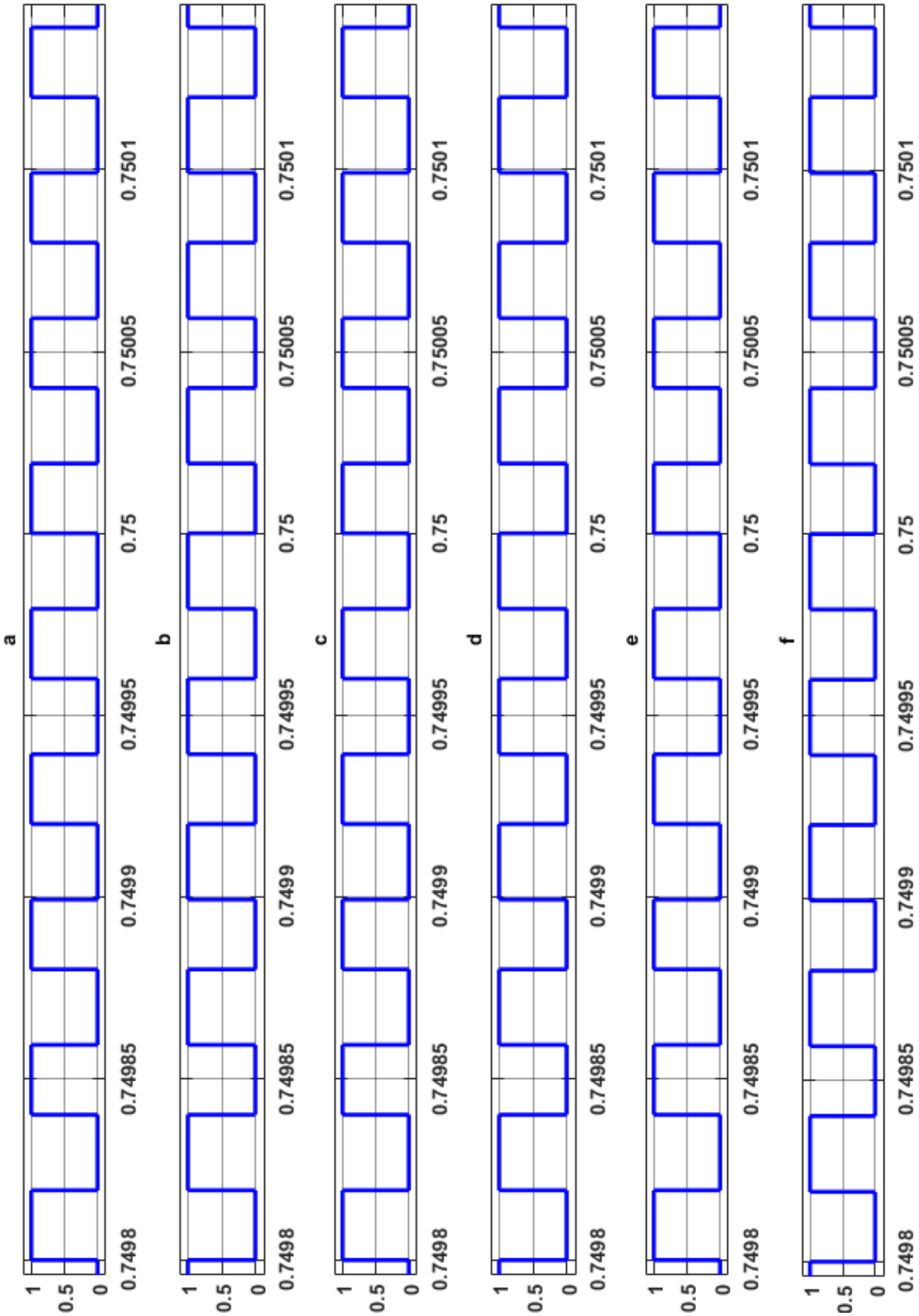


Figure 6-9: Duty cycle for each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

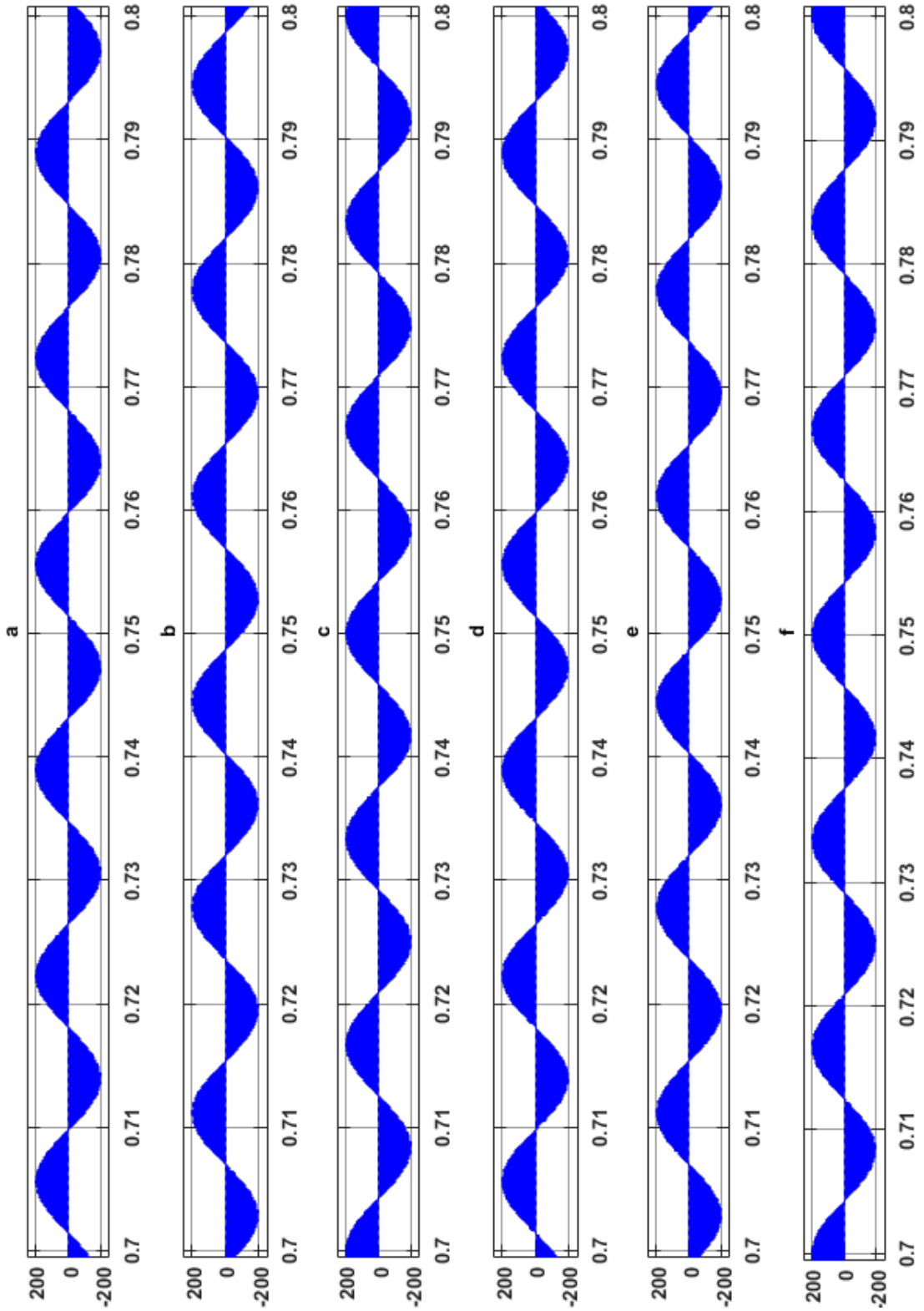


Figure 6-10: Voltage stress across each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

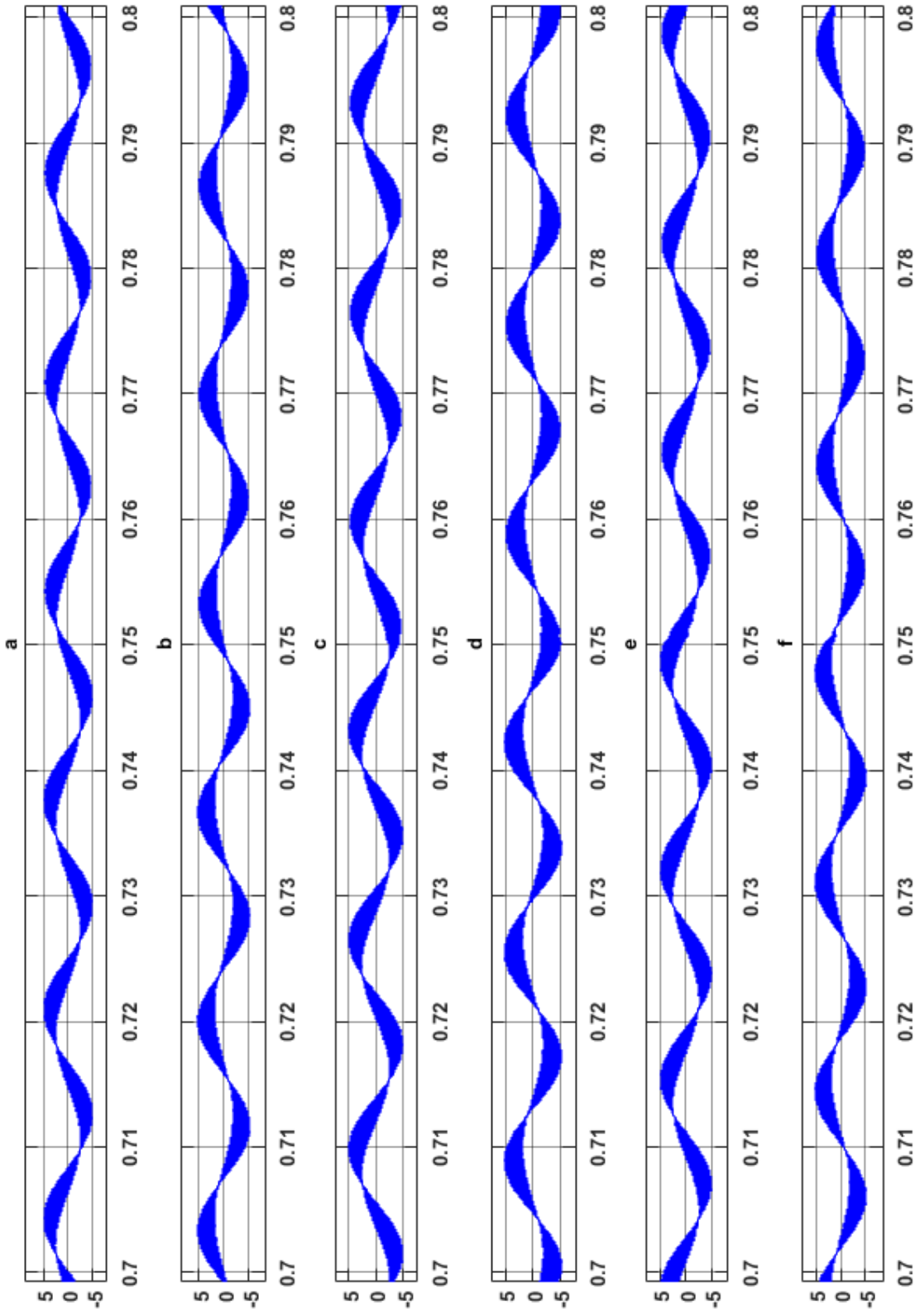


Figure 6-11: Center-point currents

Figure 6-5 displays the input capacitor voltages for each phase. It may be observed that each input capacitor voltage has a rms voltage of $60V_{line\text{-}line}$ applied across its terminals. This voltage division demonstrates the access to the mid-point of input voltage across each phase of CPC PLC. Similar voltage division may also noticed from Figure 6-6, where each output capacitor voltage has a rms value of $60V_{line\text{-}line}$ applied across its terminals. This ensures access to the center-point voltage of the output load voltage. The voltages across the buck-boost inductors in CPC PLC converter topology have been presented in Figure 6-7. The voltage across each inductor also has a rms voltage of $60V_{line\text{-}line}$. But the inductor voltages also demonstrate the switching phenomenon, since it changes polarity at every transition of switching states from duty cycle 'D' to '$D^{/}$'. This is a characteristic of buck-boost inductor where it maintains continuity of its current, but in order to maintain continuity, the voltage impressed during state-1 of switching sequence is 180 degrees phase-shifted from the voltage across the inductor during state-2 of switching sequence. This principle has also been explained in Chapter-3. The current through the buck-boost inductors have also been captured in Figure 6-8. Since the input and output capacitor voltages are balanced, the peak voltage stress across the switches are equal to half the summation of input and output voltage, which is equal to a peak voltage of $170V_{ac}$. The voltage stress waveforms are displayed in Figure 6-10. The current flowing through the center-point connections in the input side as well as the output side are shown in Figure 6-11.

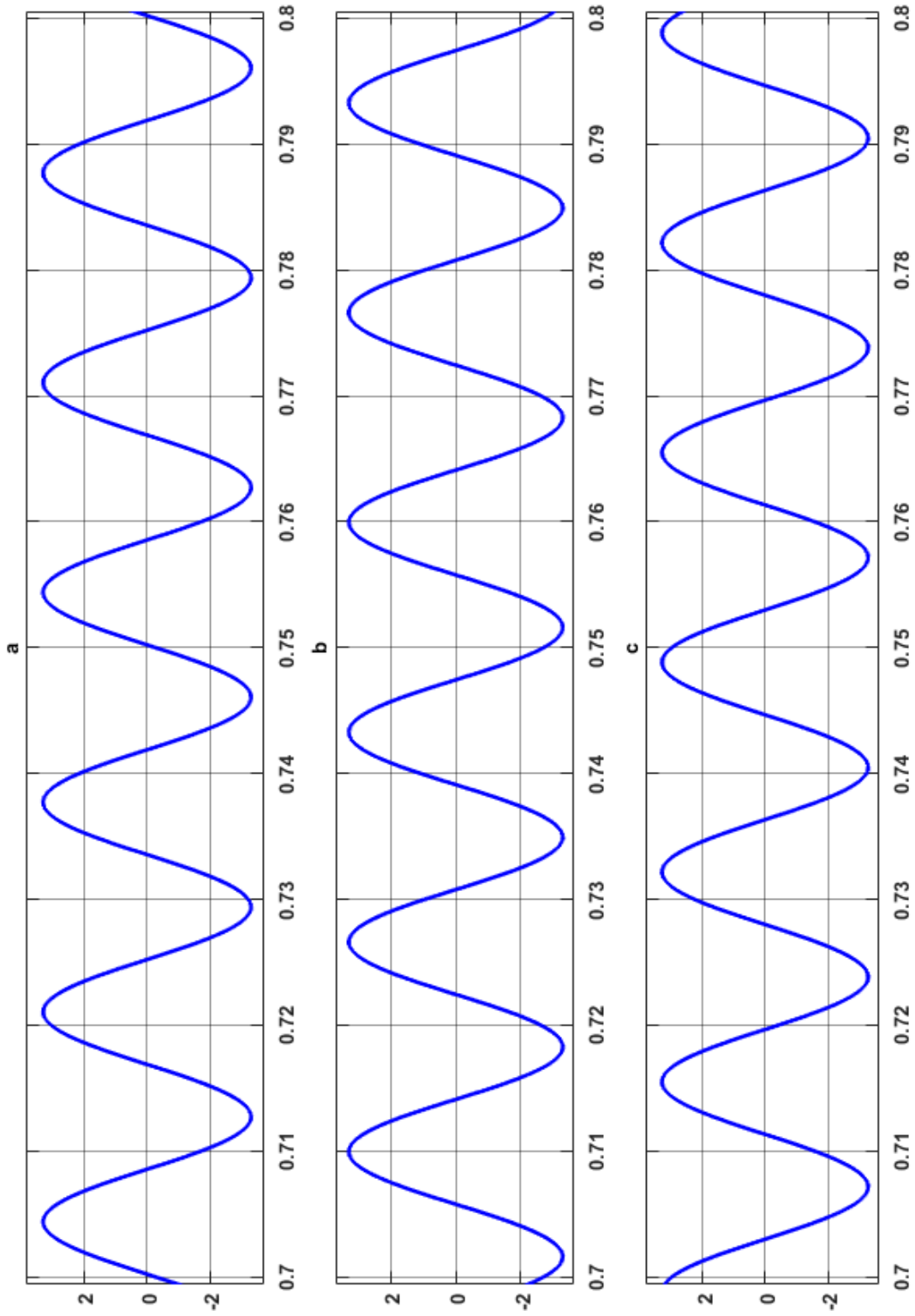


Figure 6-12: Input source currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

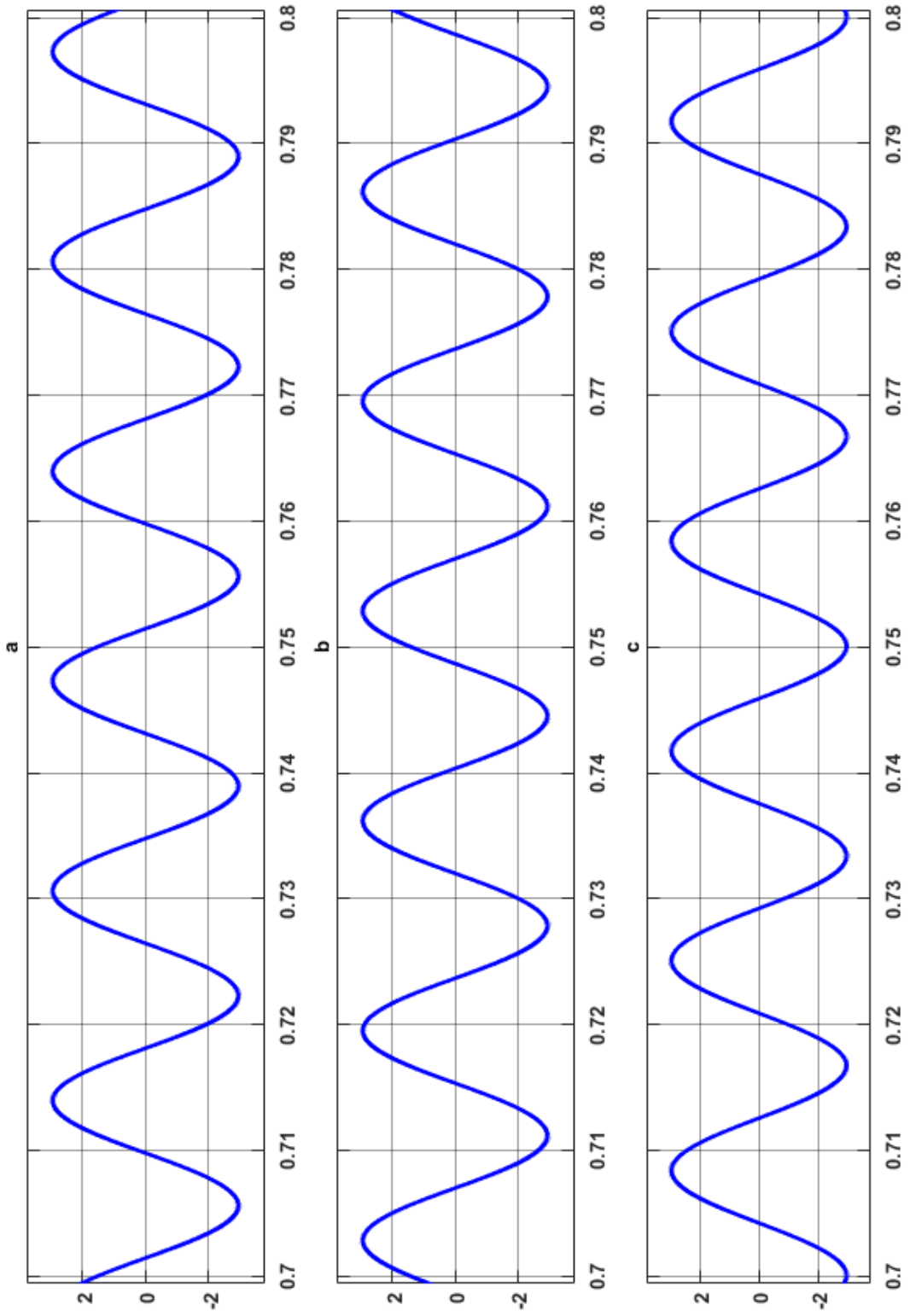


Figure 6-13: Output load currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

Figure 6-12 and Figure 6-13 shows each phase of source input currents and output load currents. It may be seen that input source current and output load current have a peak value of 3A, for a resistive load of 100Ω connected across each phase in delta - configuration. Since the load is resistive, it may be noted that the voltage across each phase is in phase with the current through each phase. The next sub-section discusses the closed-loop operation of CPC PLC.

6.3. Closed-Loop 3-Ø CPC PLC Simulation

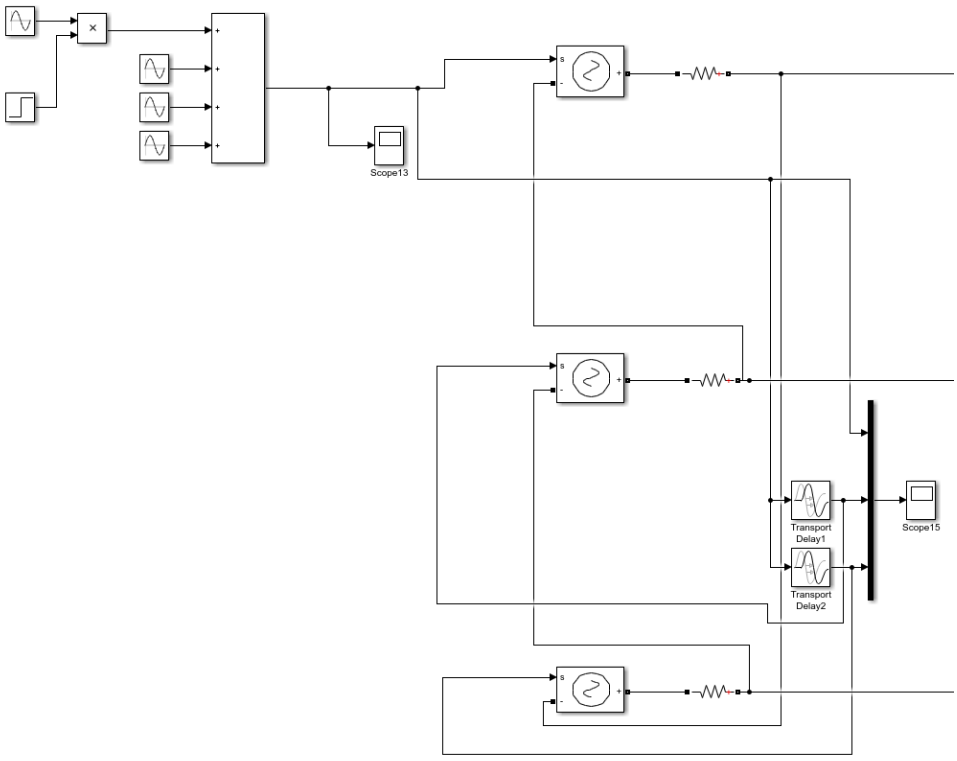


Figure 6-14: Snapshot of the Matlab-Simulink model of the source for closed loop simulation

As may be seen from Figure 6-14, the 3-Ø input source model may be used to introduce a step change in the source voltage. As may be seen from the results presented

in this sub-section, a step change in source voltage is introduced at 0.75 seconds of simulation for verifying the line-regulation performance of CPC PLC.

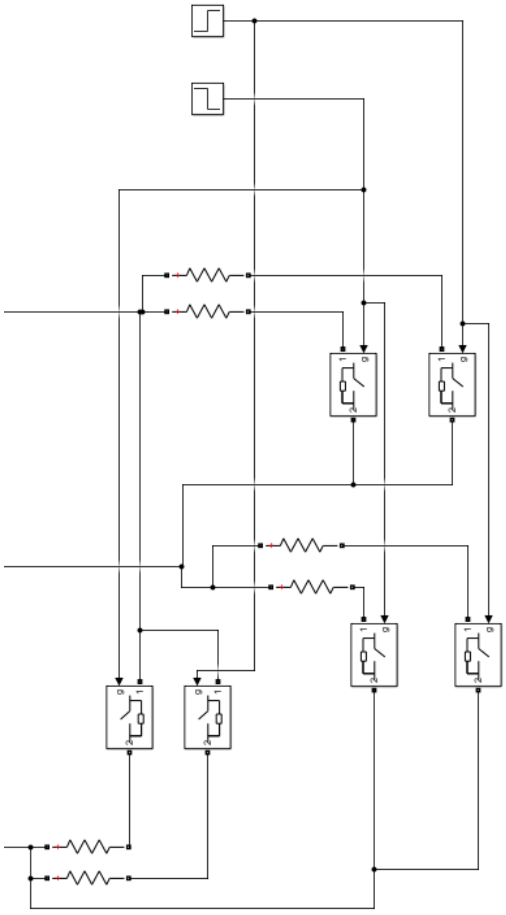


Figure 6-15: Snapshot of the Matlab-Simulink model of the load for closed loop simulation

Figure 6-15 shows the Matlab-Simulink model of the output load. It has been such designed that it will introduce a step change in the load at desired simulation time. For observing the load-regulation performance of CPC PLC, a step change in load is introduce at 0.75 seconds. The CPC PLC circuit is shown in Figure 6-16. It may be noted that voltage and current sensors have been implemented in the model to measure the voltage and currents of each passive and active components of CPC PLC.

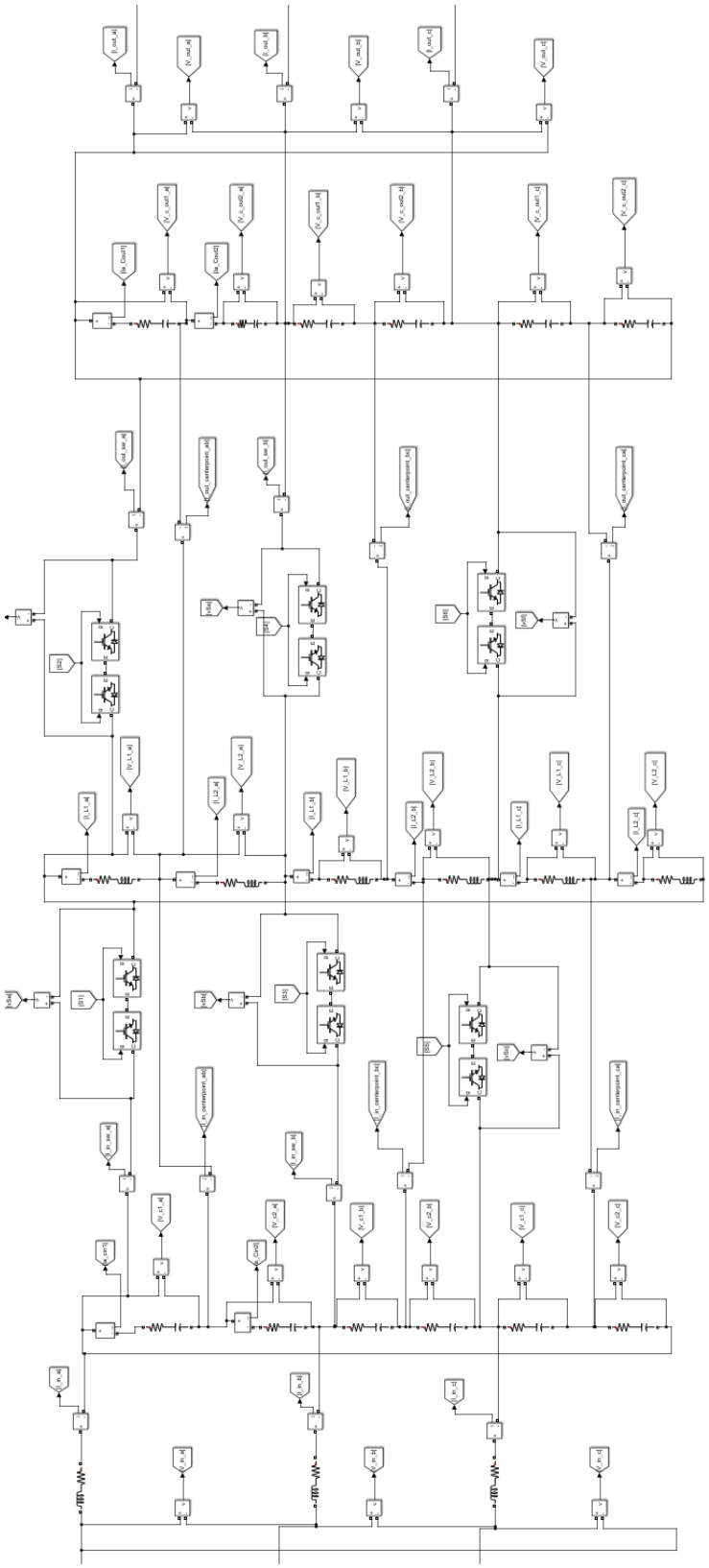


Figure 6-16: Snapshot of the Matlab-Simulink model of CPC PLC circuit topology

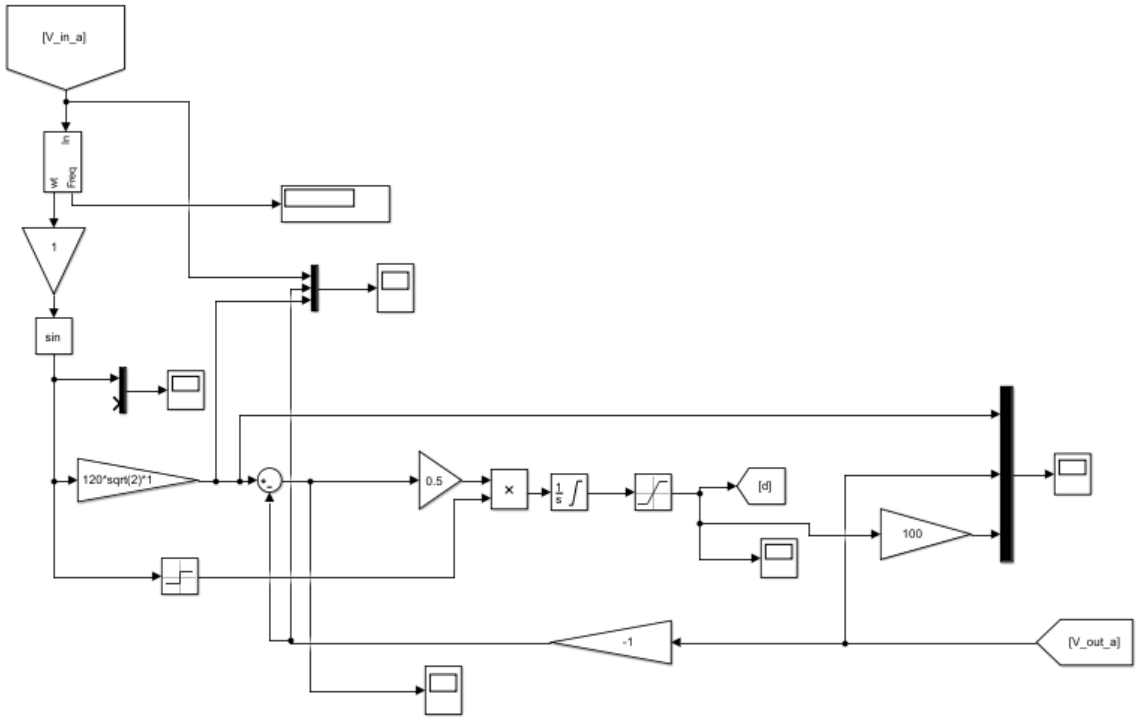


Figure 6-17: Snapshot of the Matlab-Simulink model of feedback controller

It may be seen from Figure 6-17, that closed loop controller uses the same integral controller designed in Chapter-5. It senses input voltage and generates a unity amplitude sine wave in phase with the input voltage and is scaled to desired amplitude output voltage. This is the command reference signal generated for the feedback controller. This signal is then compared with the sensed output voltage which has been multiplied by a gain of -1 to bring it to same phase as input voltage. The error is then passed through the controller transfer function designed in Chapter-5, which generates duty cycle for generating the switching signals for switches incorporated in CPC PLC.

6.3.1. Line-Regulation Performance of 3-Ø CPC PLC for low input voltage

This sub-section presents the simulation results for closed loop operation of 3-Ø CPC PLC for step change in input line voltage when it is decreased from $120V_{acrms}$ to $108V_{acrms}$. The step change in input voltage is introduced at 0.75 seconds of simulation time. The source input voltage for each of the phase of 3-Ø CPC PLC is shown in Figure 6-18. It may be seen that at0.75seconds, the input voltage gets reduced by 10%. Figure 6-19

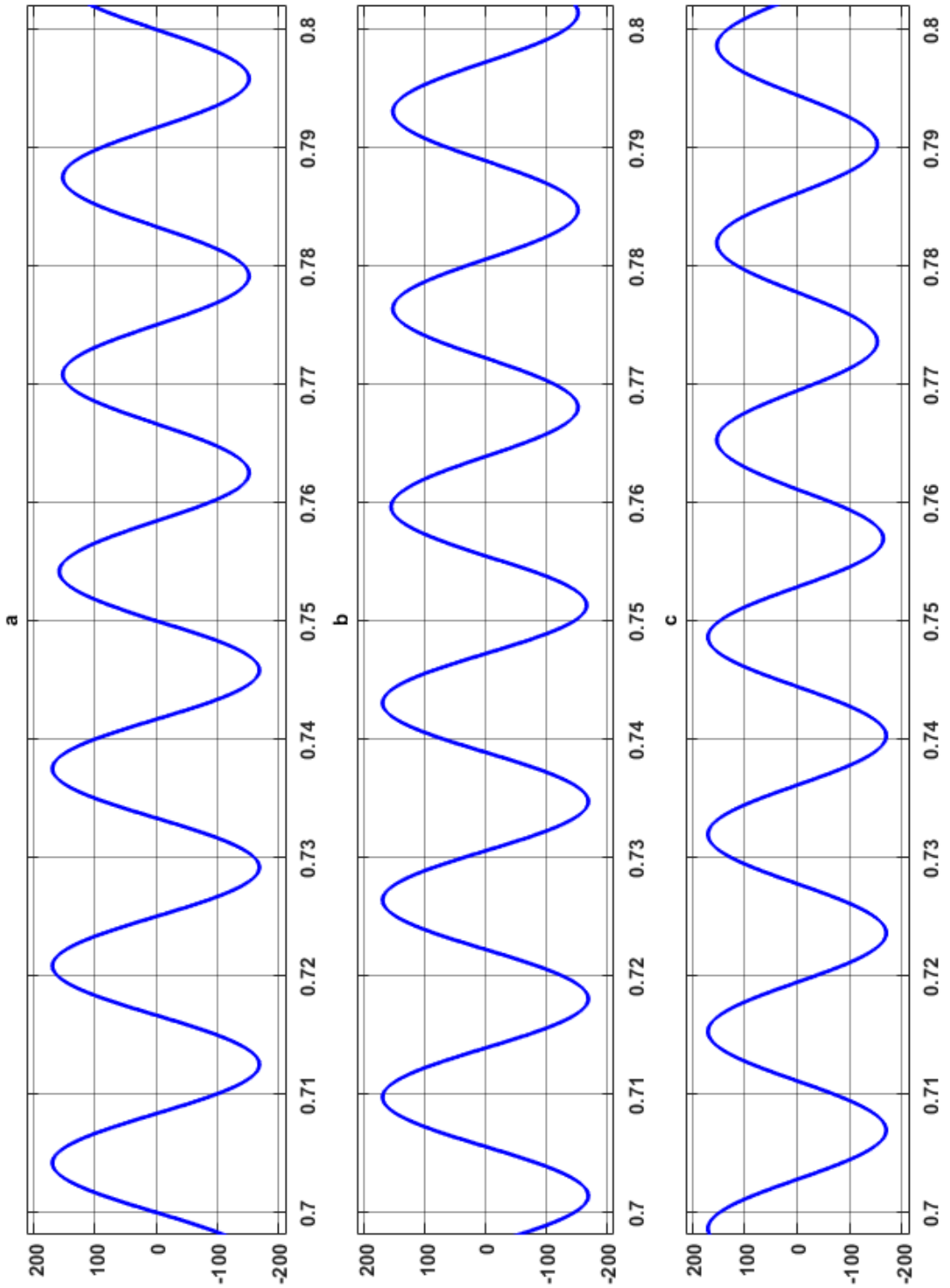


Figure 6-18: Input source voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

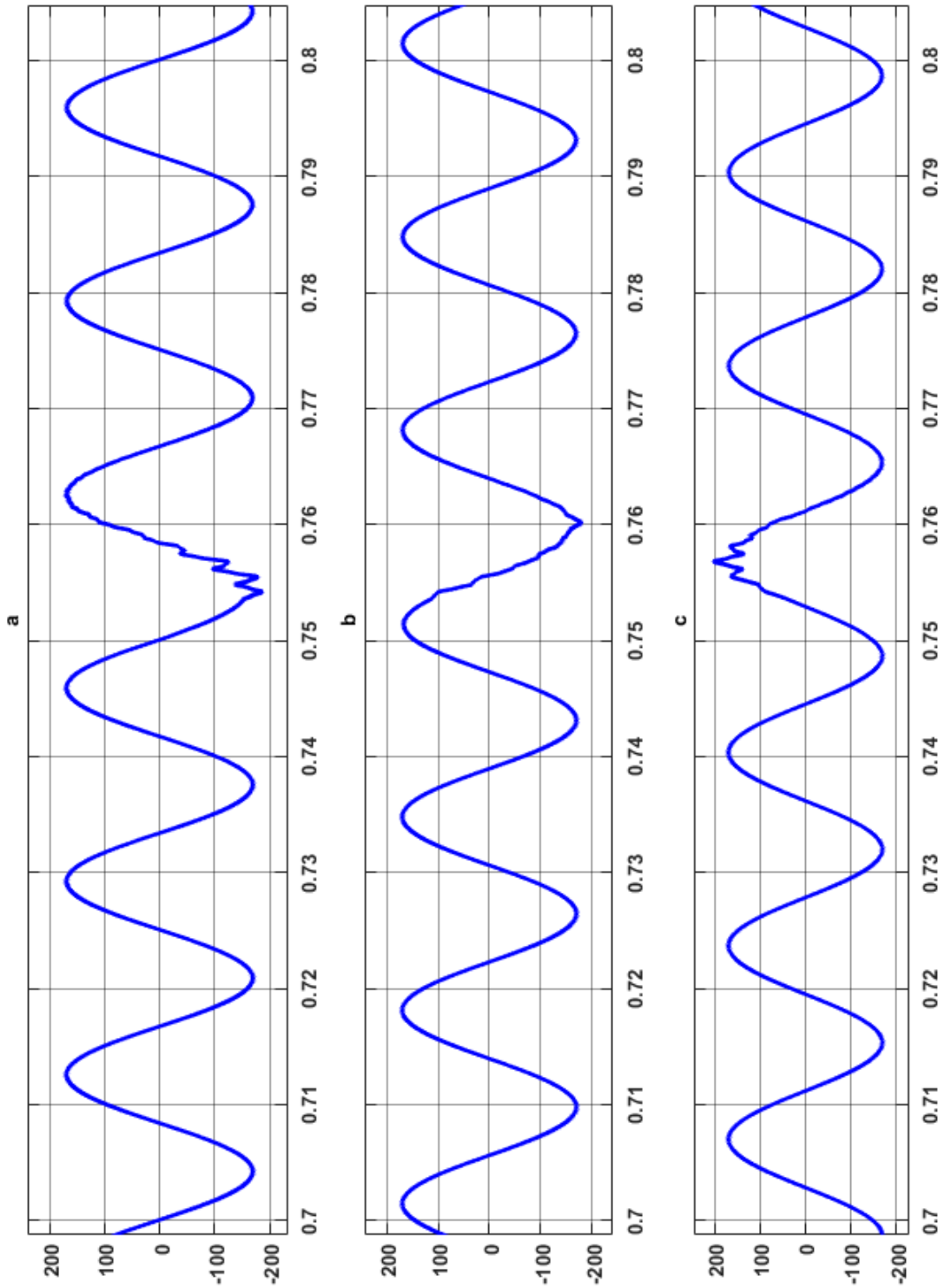


Figure 6-19: Output load voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

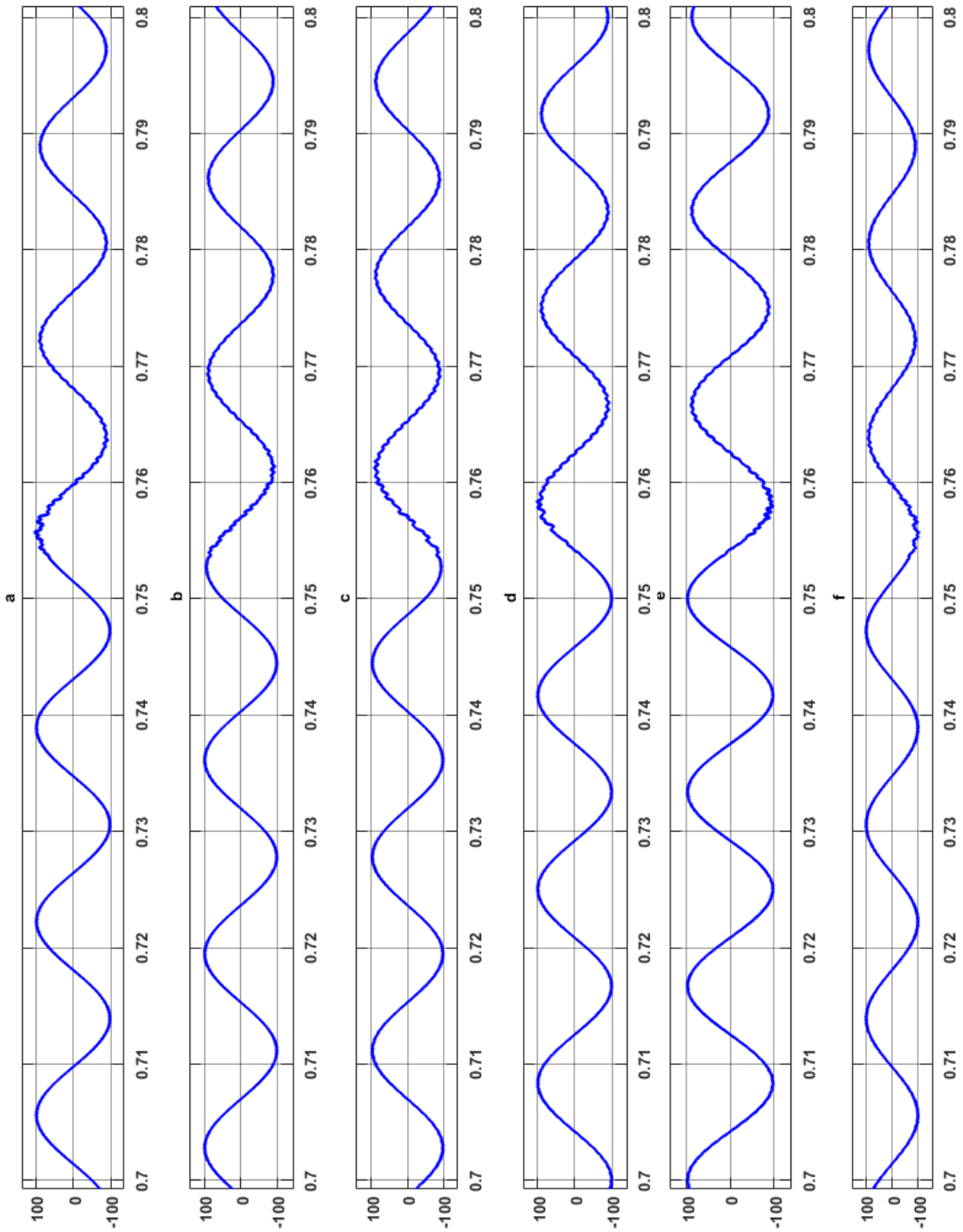


Figure 6-20: Input capacitor voltages (a) Voltage across input capacitor, C_{i1_a}, (b) Voltage across input capacitor, C_{i2_a}, (c) Voltage across input capacitor, C_{i1_b}, (d) Voltage across input capacitor, C_{i2_b}, (c) Voltage across input capacitor, C_{i1_c}, and (d) Voltage across input capacitor, C_{i2_c}.

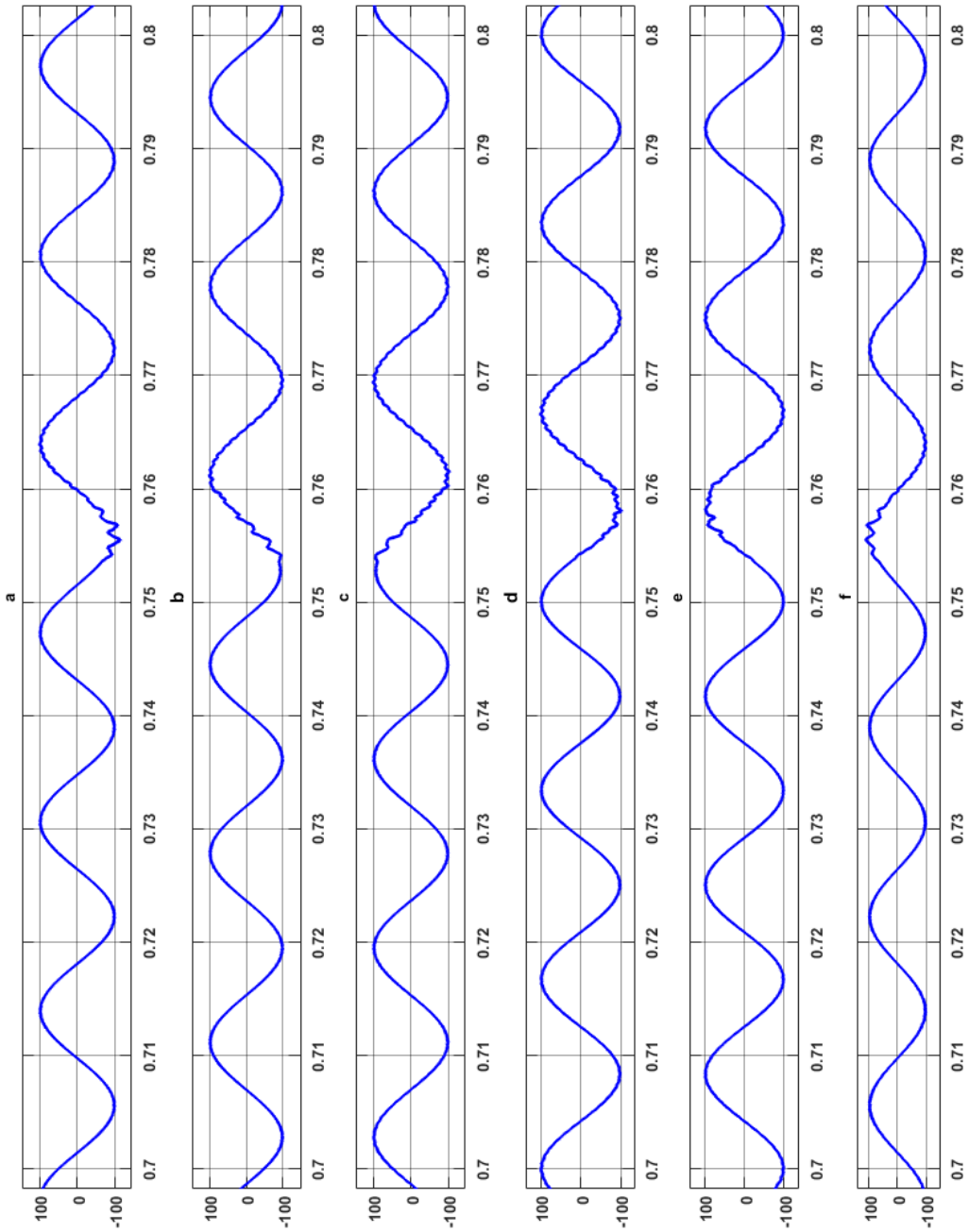


Figure 6-21: Output capacitor voltages a) Voltage across input capacitor, C_{o1_a}, (b) Voltage across input capacitor, C_{o2_a}, (c) Voltage across input capacitor, C_{o1_b}, (d) Voltage across input capacitor, C_{o2_b}, (c) Voltage across input capacitor, C_{o1_c}, and (d) Voltage across input capacitor, C_{o2_c}.

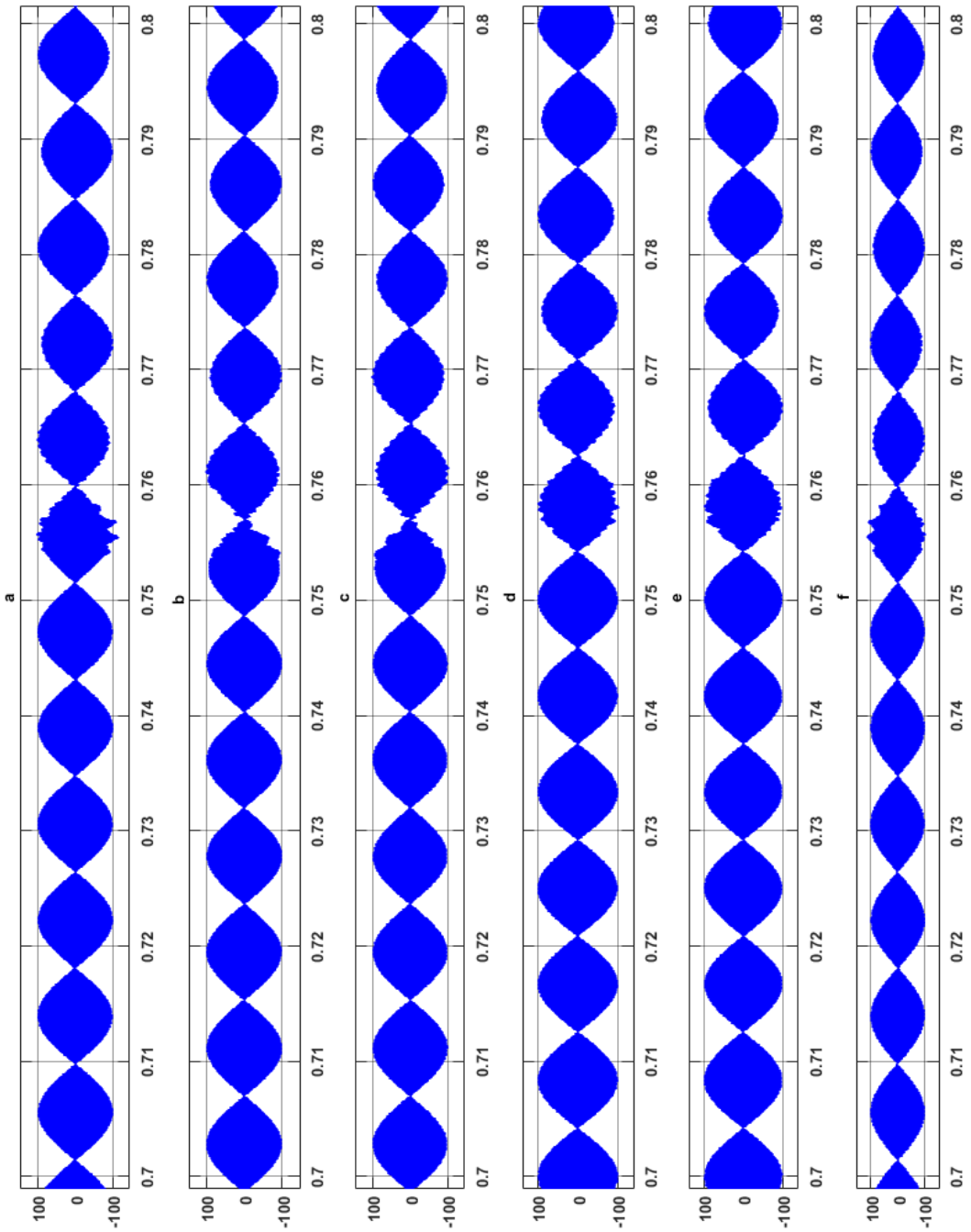


Figure 6-22: Buck-boost inductor voltages (a) Voltage across inductor, L_{1_a}, (b) Voltage across inductor, L_{2_a}, (c) Voltage across inductor, L_{1_b}, (d) Voltage across inductor, L_{2_b}, (e) Voltage across inductor, L_{1_c}, and (f) Voltage across inductor, L_{2_c}

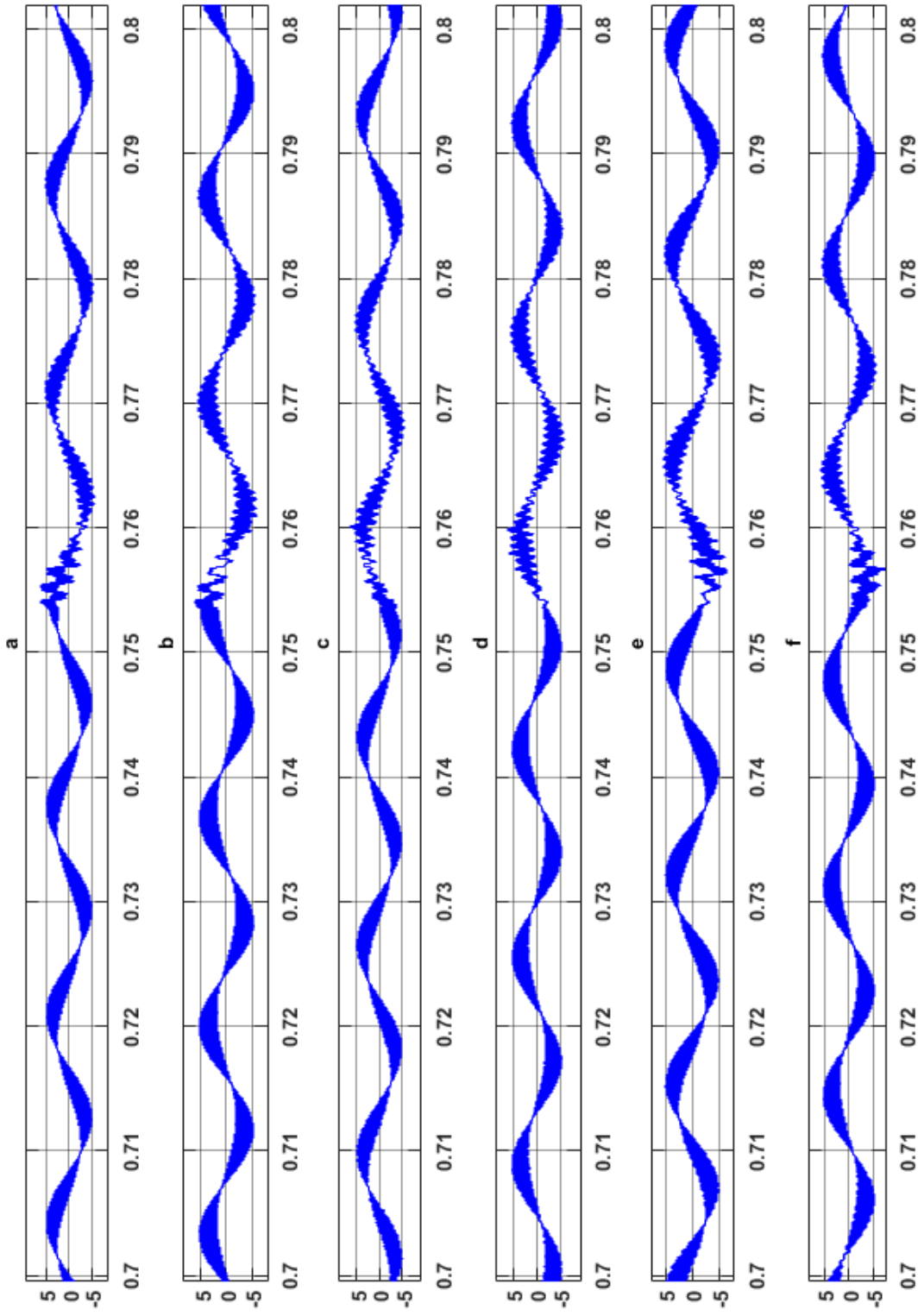


Figure 6-23: Buck-boost inductor currents (a) Current across inductor, L_{1_a}, (b) Current across inductor, L_{2_a}, (c) Current across inductor, L_{1_b}, (d) Current across inductor, L_{2_b}, (e) Current across inductor, L_{1_c}, and (f) Current across inductor, L_{2_c}

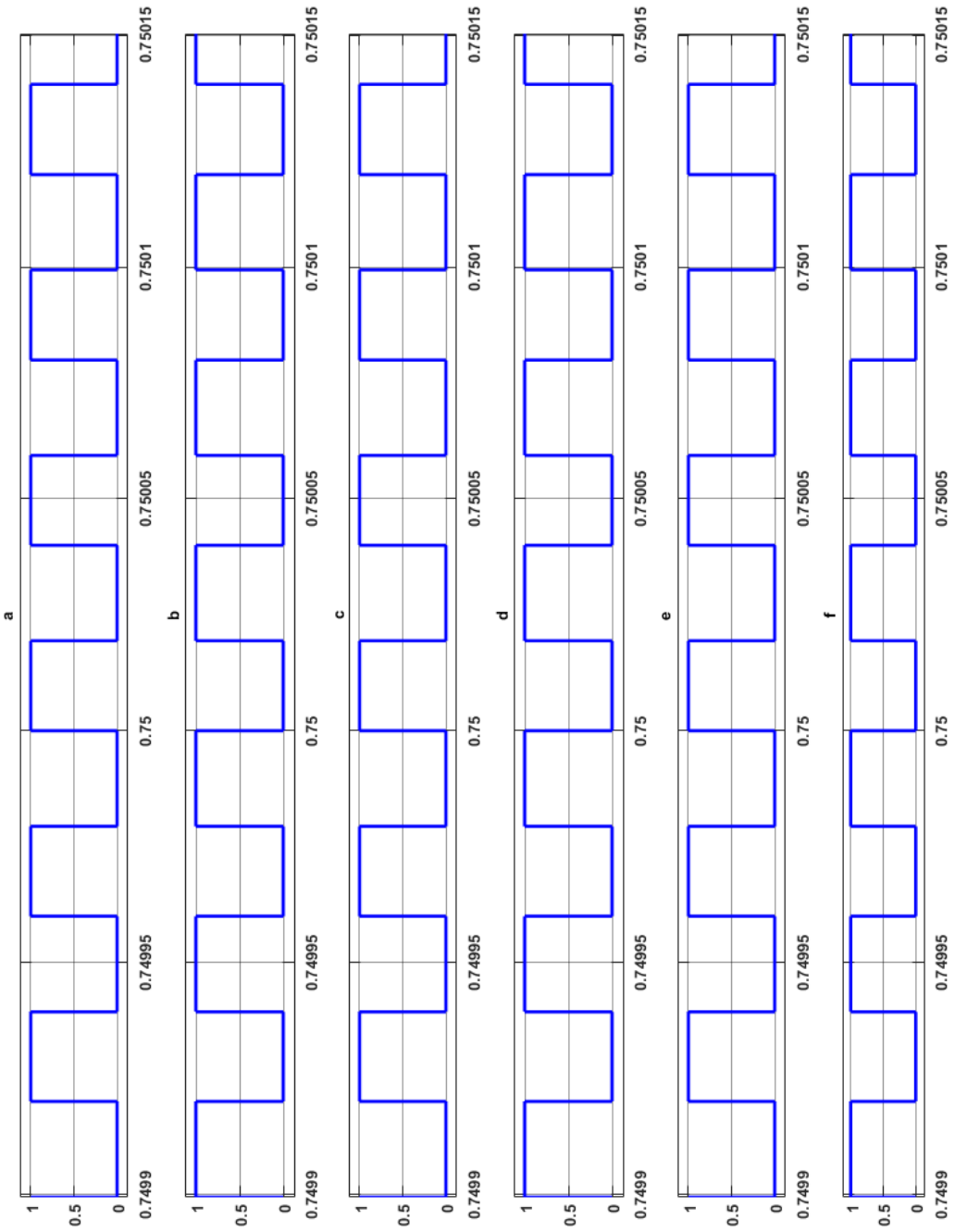


Figure 6-24: Duty Cycle for each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

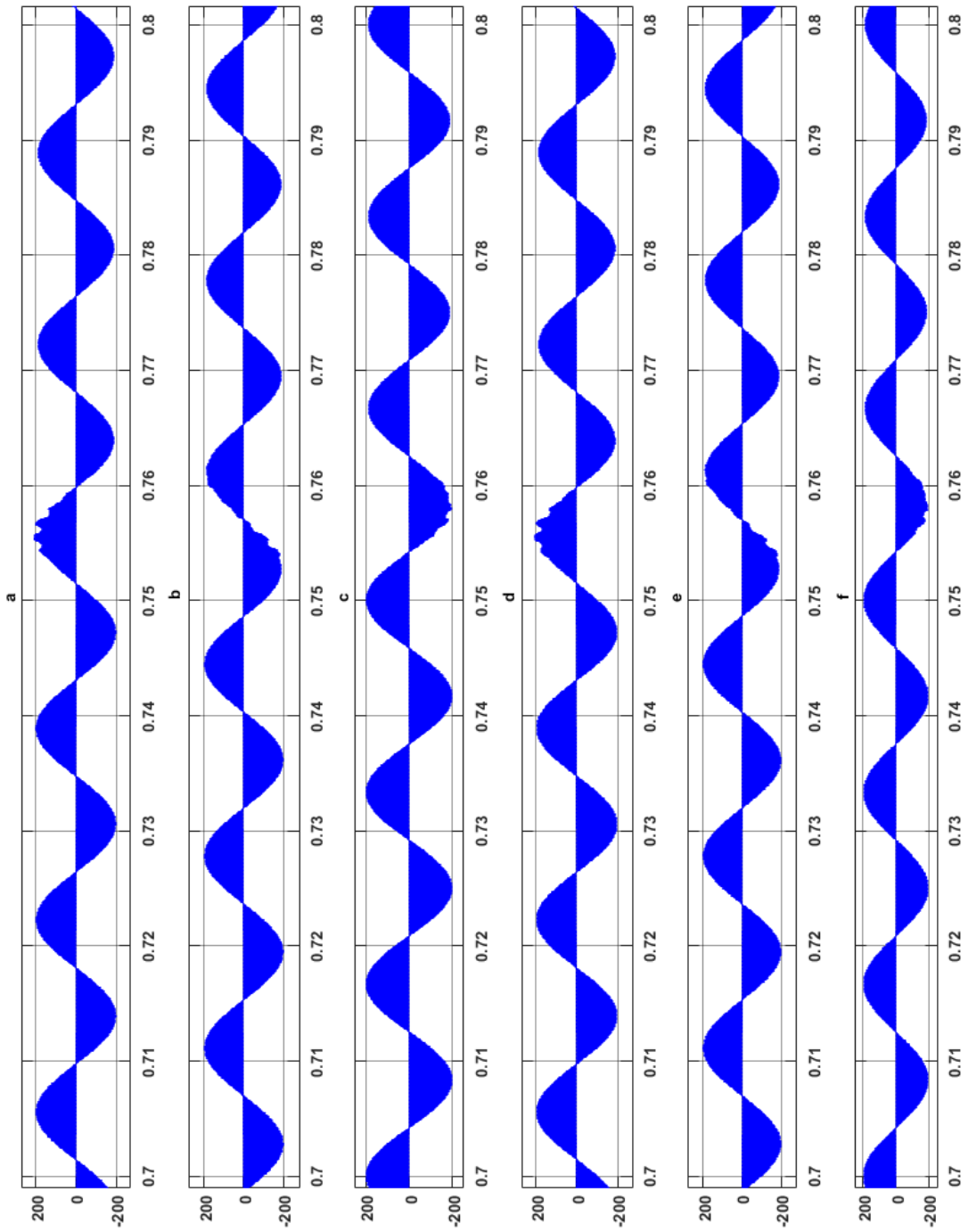


Figure 6-25: Voltage Stress on each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

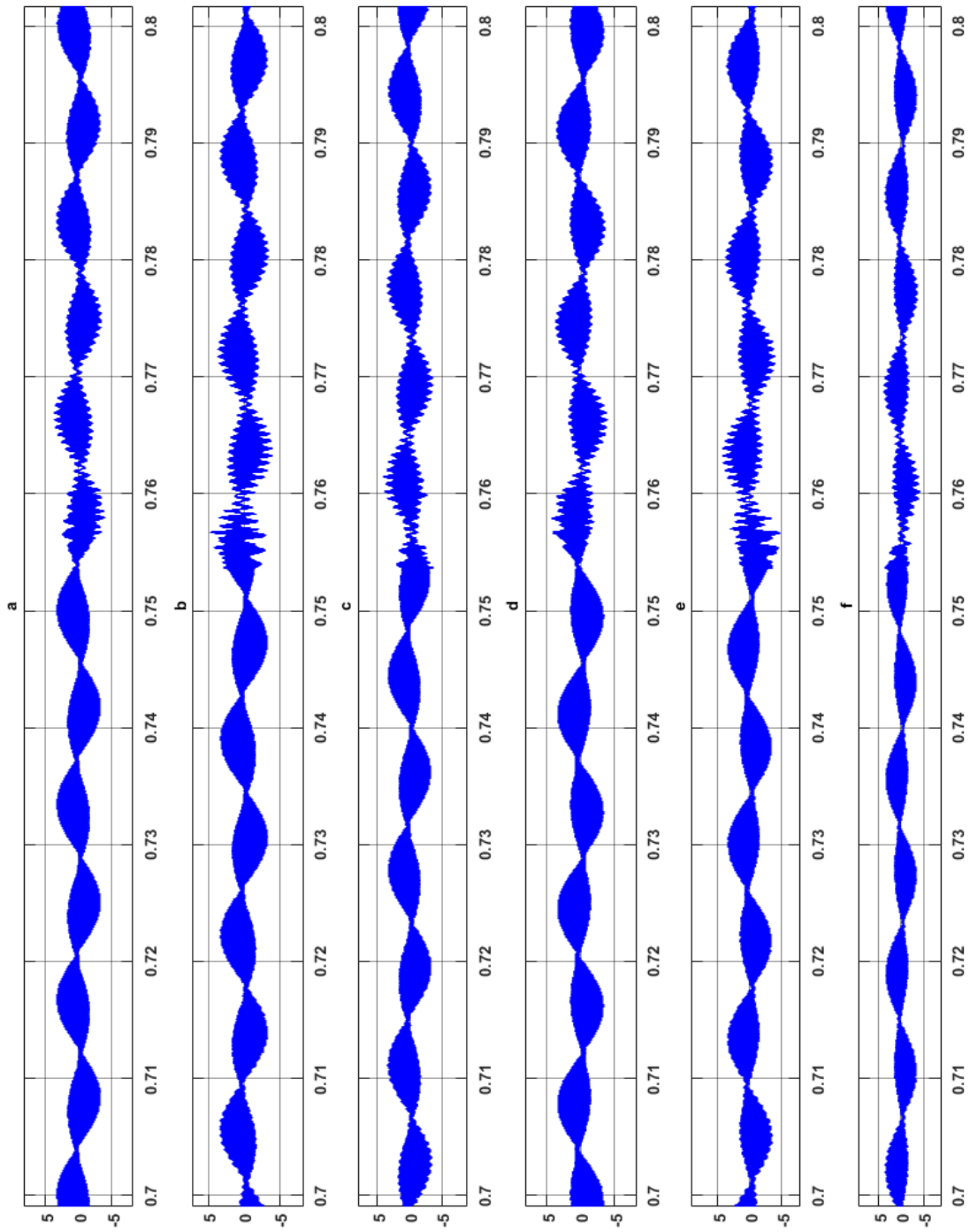


Figure 6-26: Center-Point-Currents

Figure 6-20displays the input capacitor voltages for each phase. It may be observed that each input capacitor voltage has a rms voltage of $60V_{line\text{-}line}$ applied across its terminals. This voltage division demonstrates the access to the mid-point of input voltage across each phase of CPC PLC. Similar voltage division may also noticed from Figure 6-20, where each output capacitor voltage has a rms value of $60V_{line\text{-}line}$ applied across its terminals. This ensures access to the center-point voltage of the output load voltage. Also, it may be seen that due to step decrease in input voltage by 10% at 0.75sec, input capacitor voltages also exhibit step decrement by 10% at 0.75 sec. But due to command following reference of the controller, output capacitor voltages do not get reduced by 10%. These capacitor voltages get back to half of the desired output voltage within one cycle. The voltages across the buck-boost inductors in CPC PLC converter topology have been presented in Figure 6-22. The voltage across each inductor also has a rms voltage of $60V_{line\text{-}line}$. But step change in input voltage reflects in the inductor voltage as well, where it settles to a voltage, such that the output voltage is controlled to desired voltage reference. The current through the buck-boost inductors have also been captured in Figure 6-23. The duty cycle waveforms are shown in Figure 6-24. Since the input and output capacitor voltages are balanced, the peak voltage stress across the switches are equal to half the summation of input and output voltage, which is equal to a peak voltage of $170V_{ac}$. The voltage stress waveforms are displayed in Figure 6-25. The current flowing through the center-point connections in the input side as well as the output side are shown in Figure 6-26.

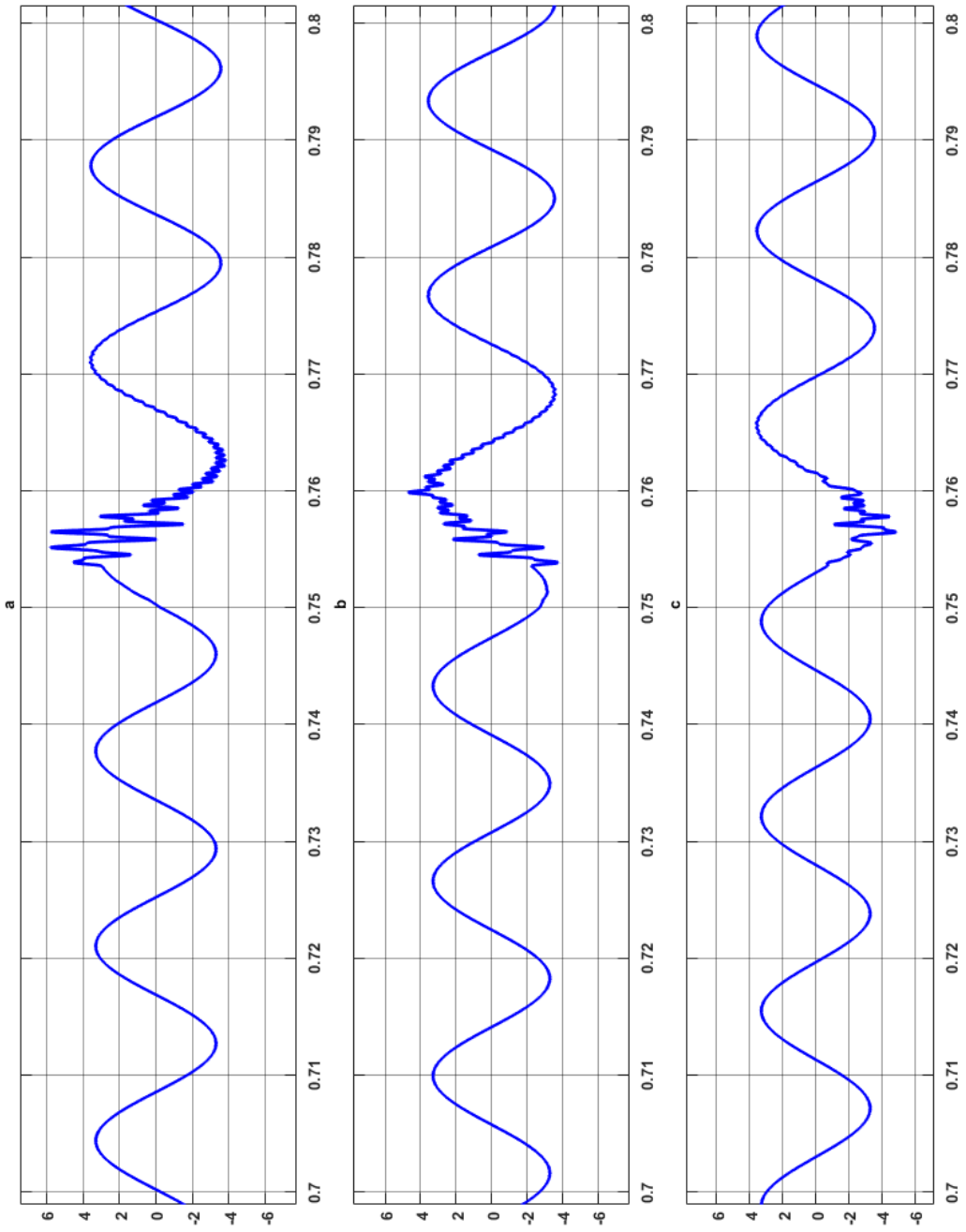


Figure 6-27: Input source currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

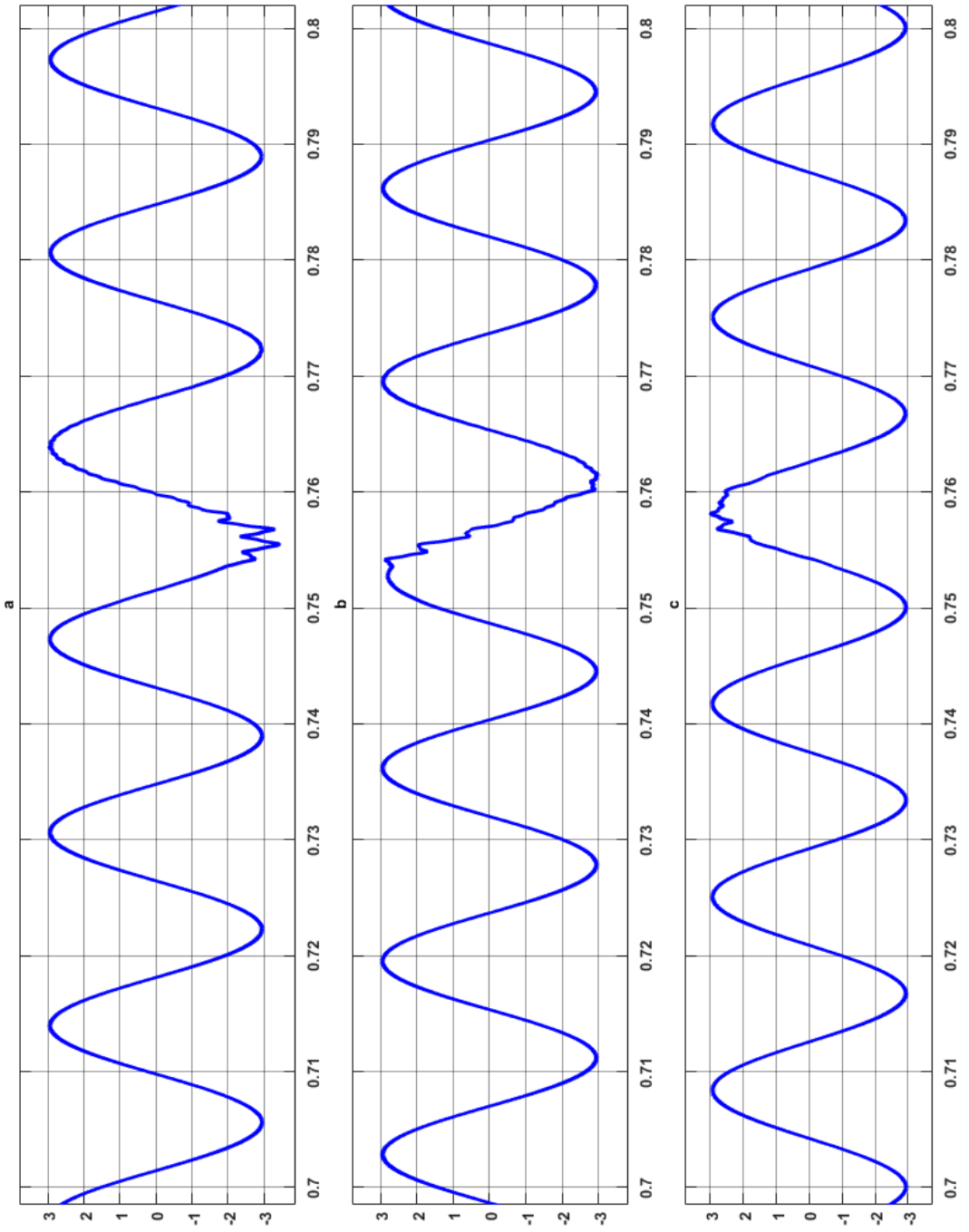


Figure 6-28: Output load currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

It may be seen from Figure 6-27 and Figure 6-28, with step decrease in input voltage at 0.75seconds, the input line current gets increased to compensate for the decrease in voltage, as the controller modulates the duty cycle to regulate constant desired line output voltage. The output line current is still regulated at the same peak value as it was before the step change in input voltage at 0.75seconds.

The next sub-section discusses simulation results for a step-increase in input voltage at 0.75 seconds.

6.3.2. Line-Regulation Performance of 3-Ø CPC PLC for high input voltage

This sub-section presents the simulation results for closed loop operation of 3-Ø CPC PLC for step change in input line voltage when it is increased from $120V_{acrms}$ to $132V_{acrms}$. The step change in input voltage is introduced at 0.75 seconds of simulation time. The source input voltage for each of the phase of 3-Ø CPC PLC is shown in Figure 6-29. It may be seen that at 0.75seconds, the input voltage gets reduced by 10%. But it may be seen from Figure 6-30, the controller regulates the duty cycle to achieve desired reference output voltage within one fundamental cycle.

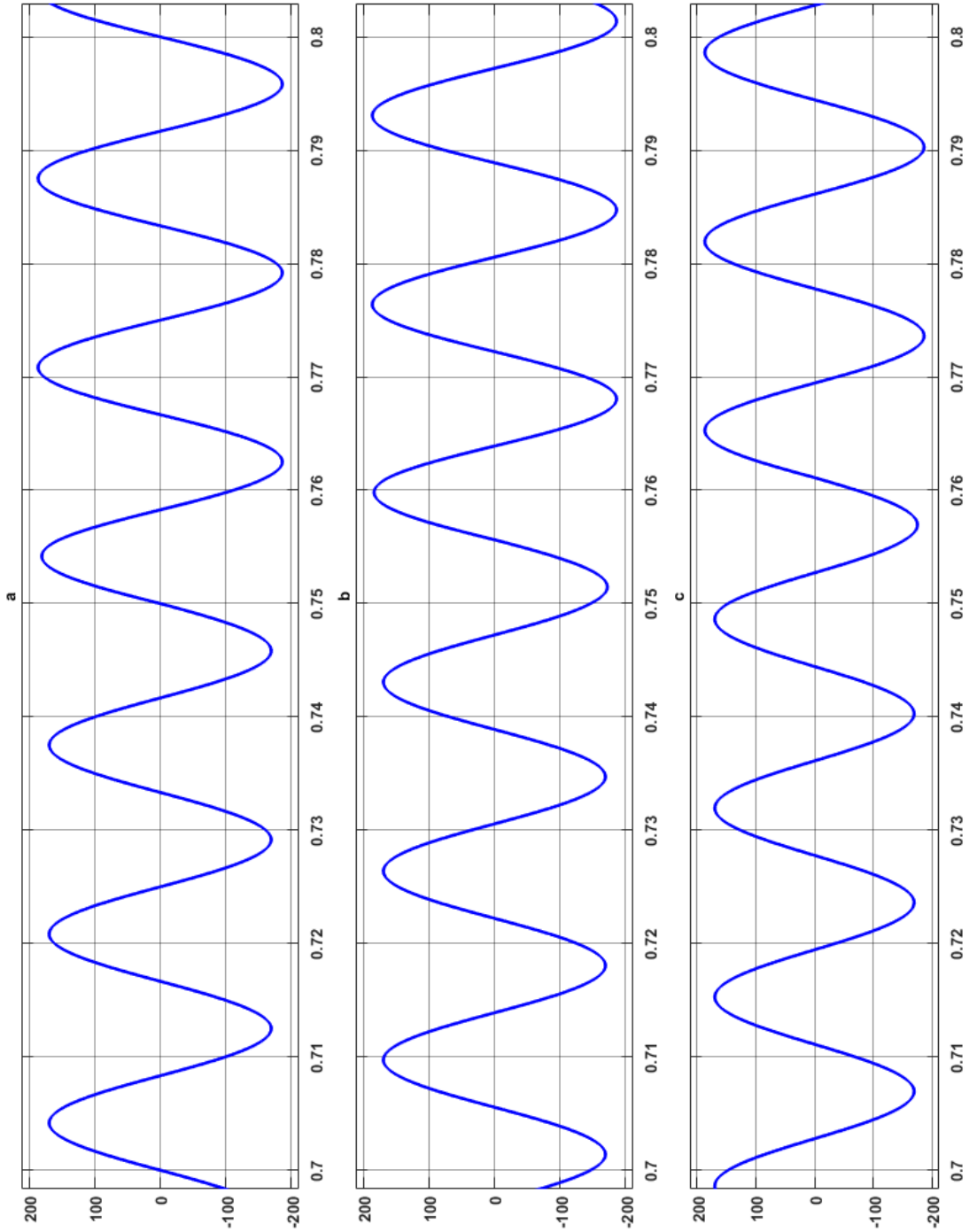


Figure 6-29: Input source voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

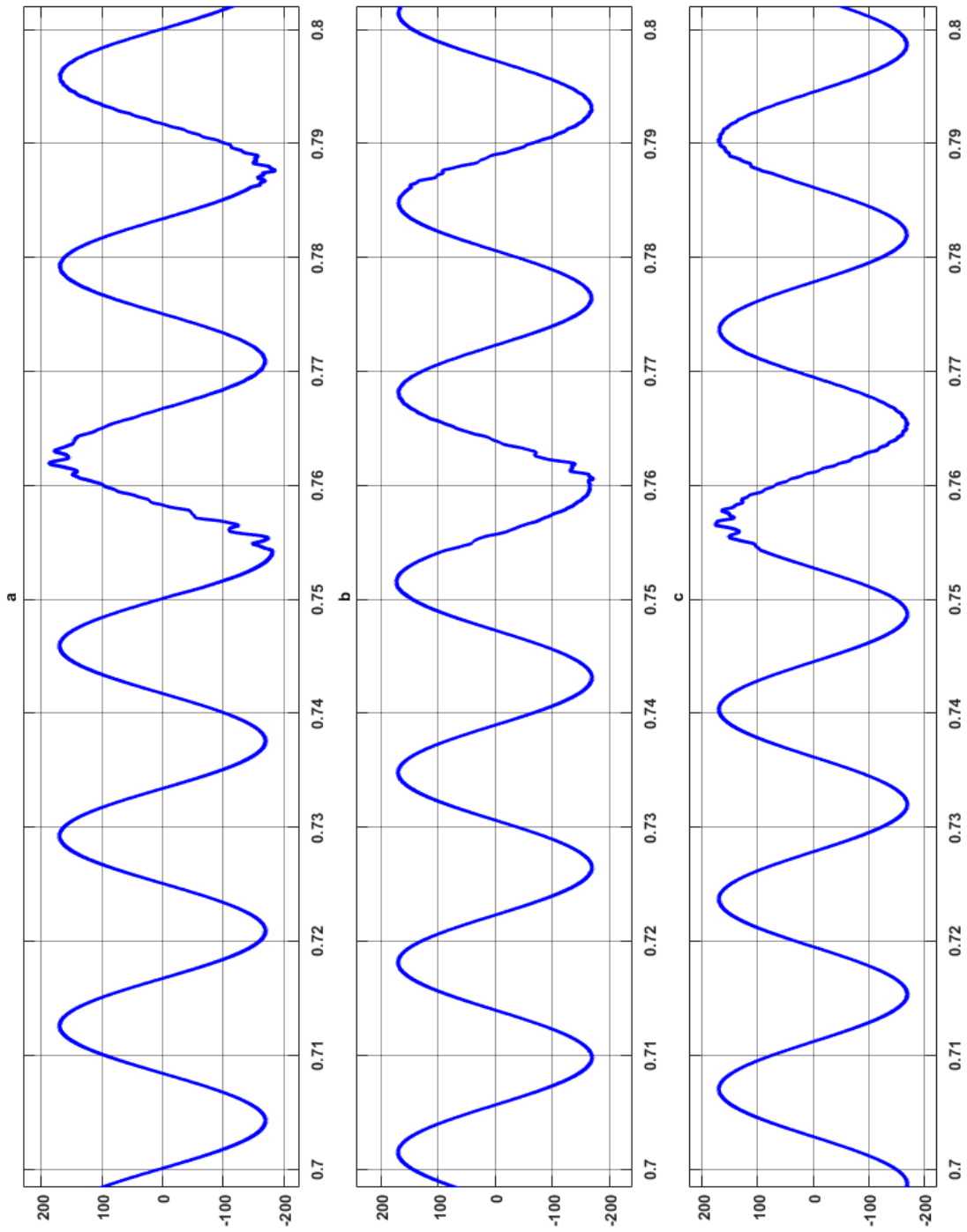


Figure 6-30: Output load voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

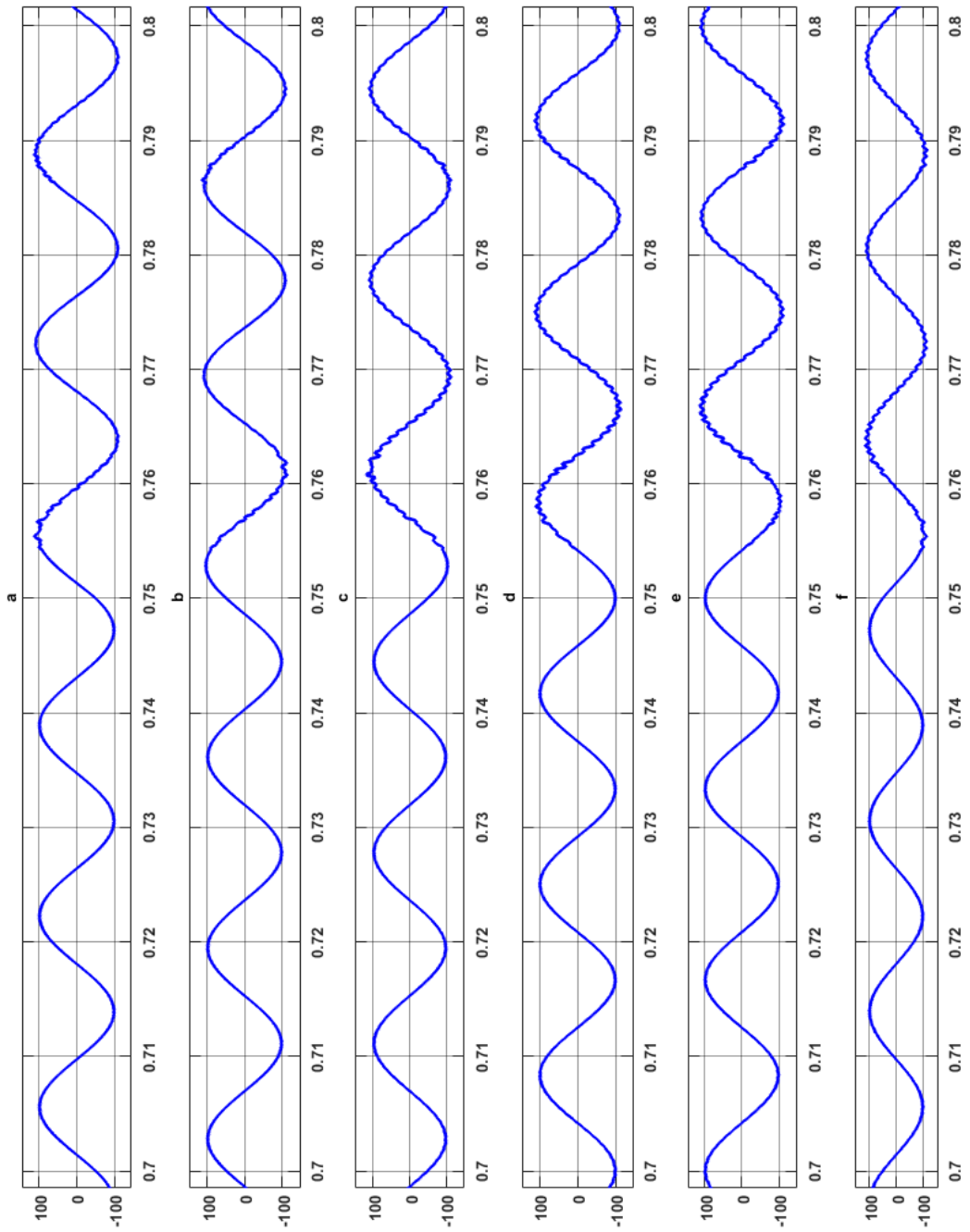


Figure 6-31: Input capacitor voltages (a) Voltage across input capacitor, C_{i1_a}, (b) Voltage across input capacitor, C_{i2_a}, (c) Voltage across input capacitor, C_{i1_b}, (d) Voltage across input capacitor, C_{i2_b}, (c) Voltage across input capacitor, C_{i1_c}, and (d) Voltage across input capacitor, C_{i2_c}.

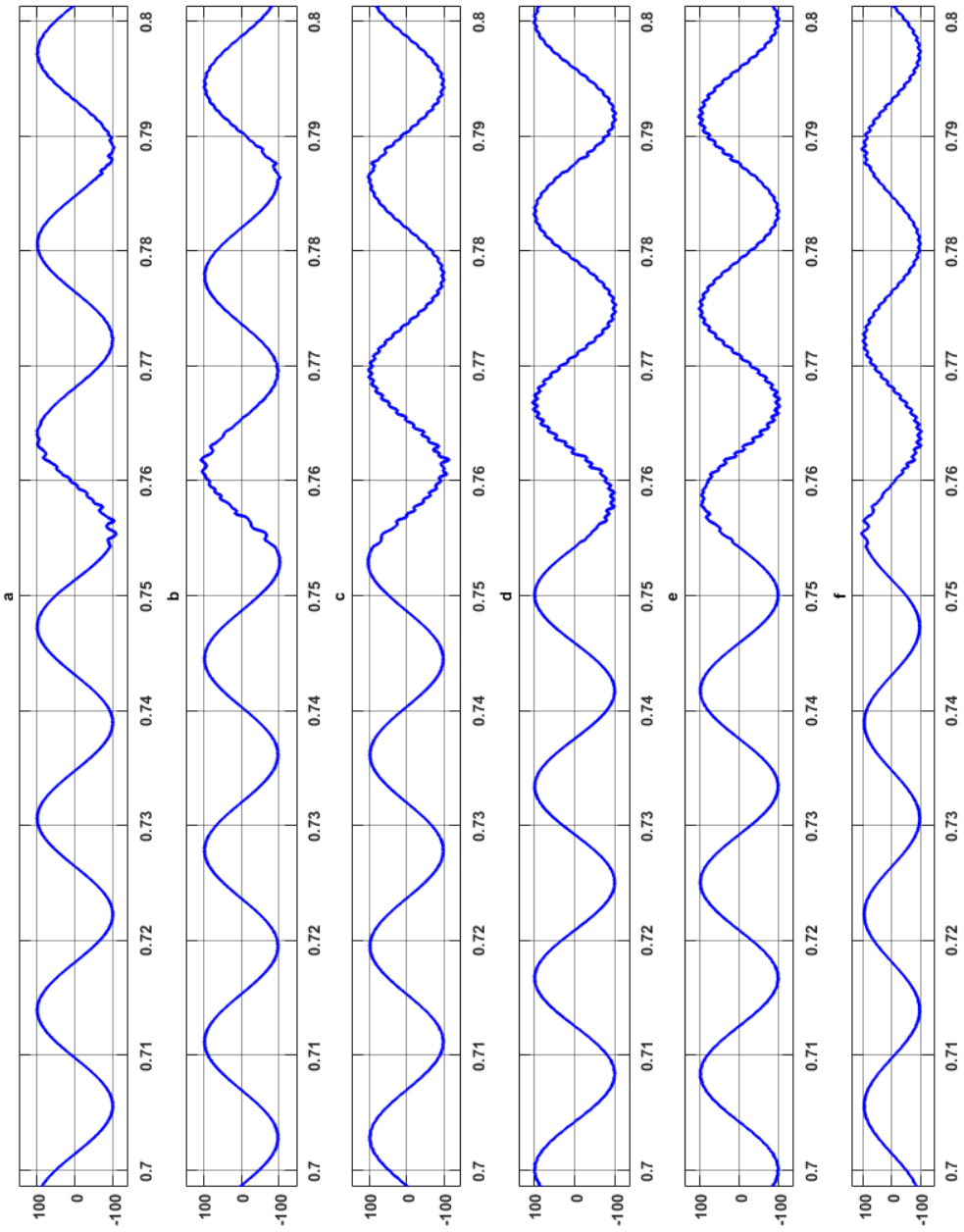


Figure 6-32: Output capacitor voltages a) Voltage across input capacitor, C_{o1_a}, (b) Voltage across input capacitor, C_{o2_a}, (c) Voltage across input capacitor, C_{o1_b}, (d) Voltage across input capacitor, C_{o2_b}, (c) Voltage across input capacitor, C_{o1_c}, and (d) Voltage across input capacitor, C_{o2_c}.

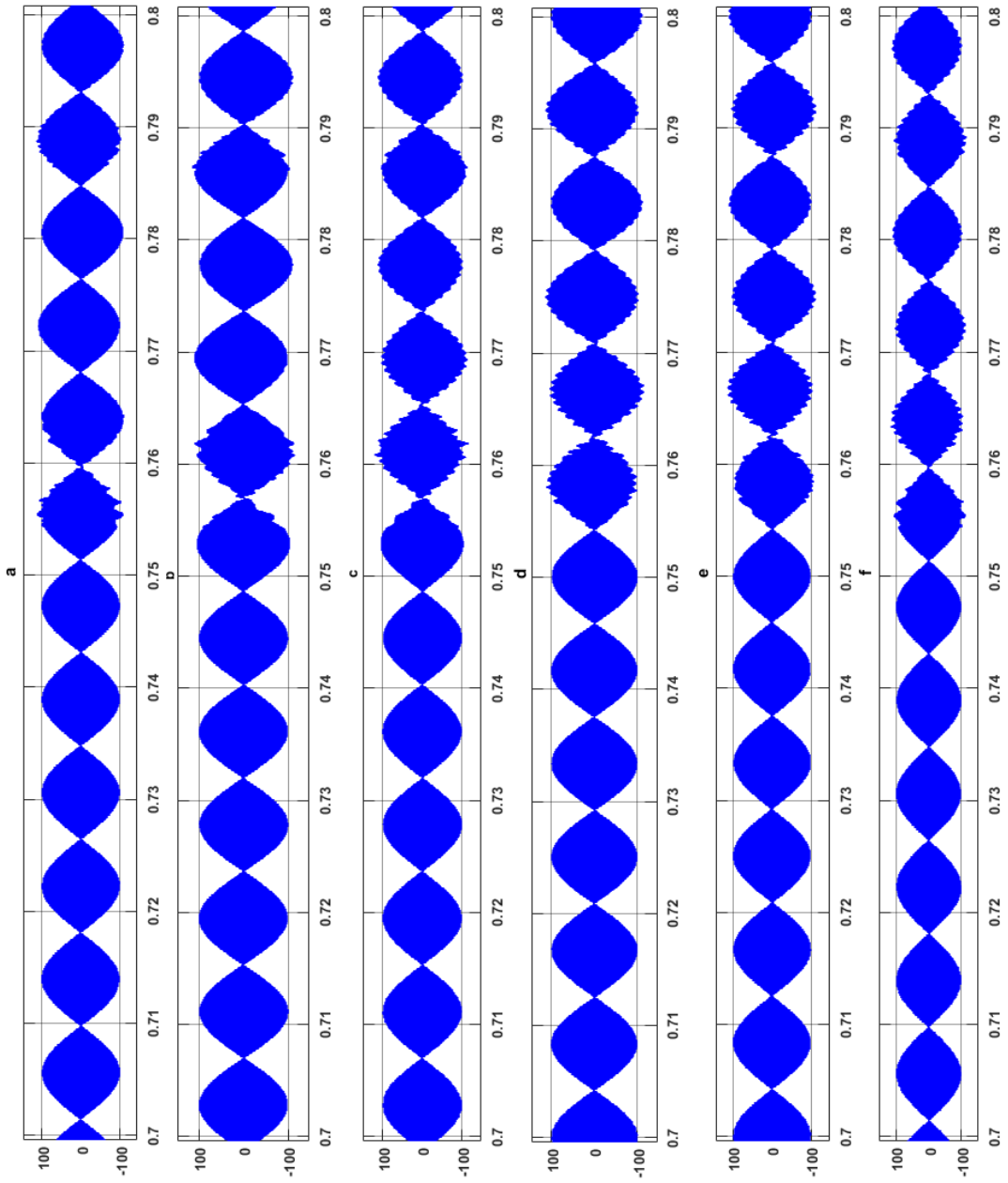


Figure 6-33: Buck-boost inductor voltages (a) Voltage across inductor, L_{1_a}, (b) Voltage across inductor, L_{2_a}, (c) Voltage across inductor, $L_{1\_b,}$ (d) Voltage across inductor, L_{2_b}, (e) Voltage across inductor, $L_{1\_c,}$ and (f) Voltage across inductor, L_{2_c}

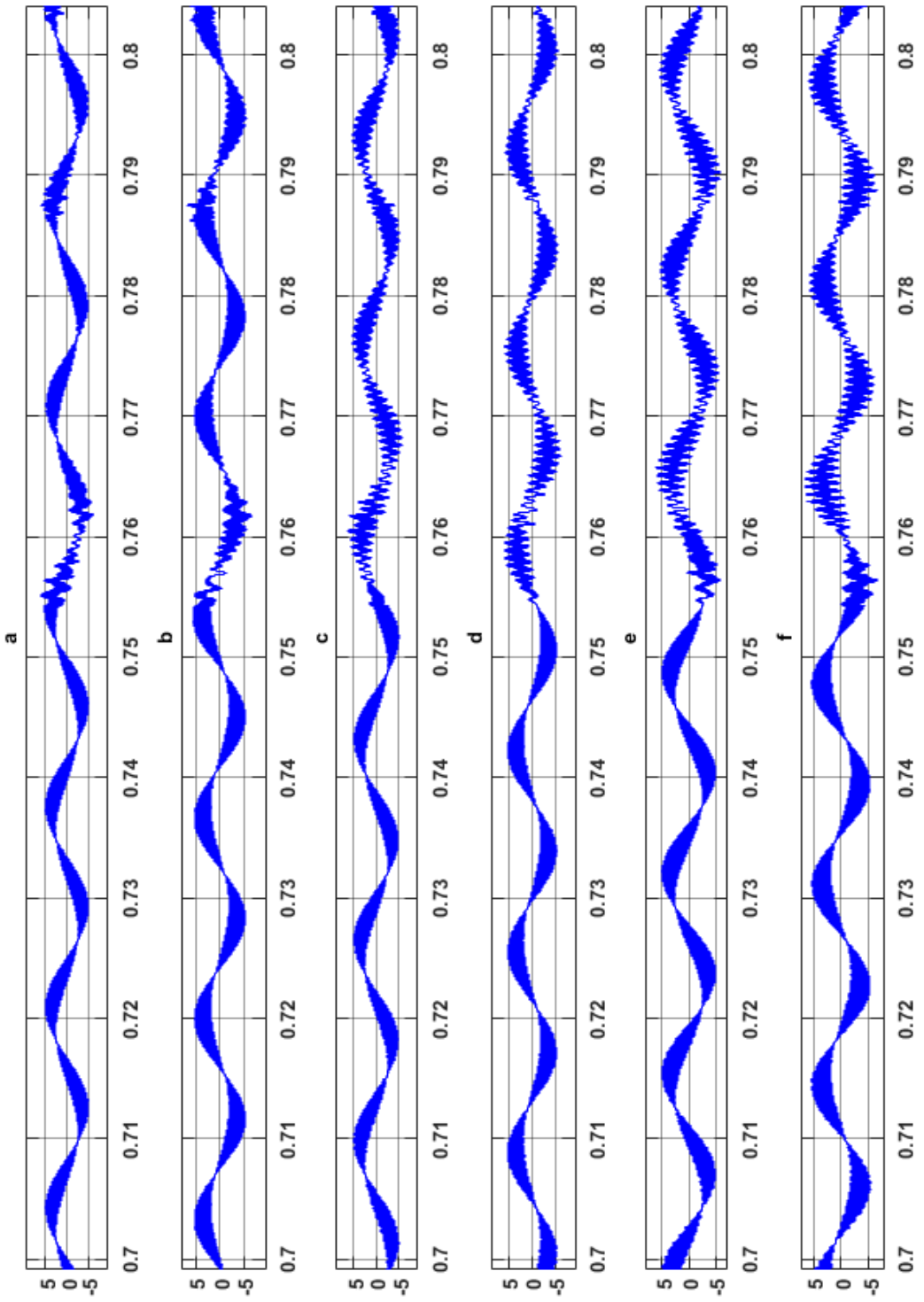


Figure 6-34: Buck-boost inductor currents (a) Current across inductor, L_{1_a}, (b) Current across inductor, L_{2_a}, (c) Current across inductor, $L_{1\_b,}$ (d) Current across inductor, L_{2_b}, (e) Current across inductor, $L_{1\_c,}$ and (f) Current across inductor, L_{2_c}

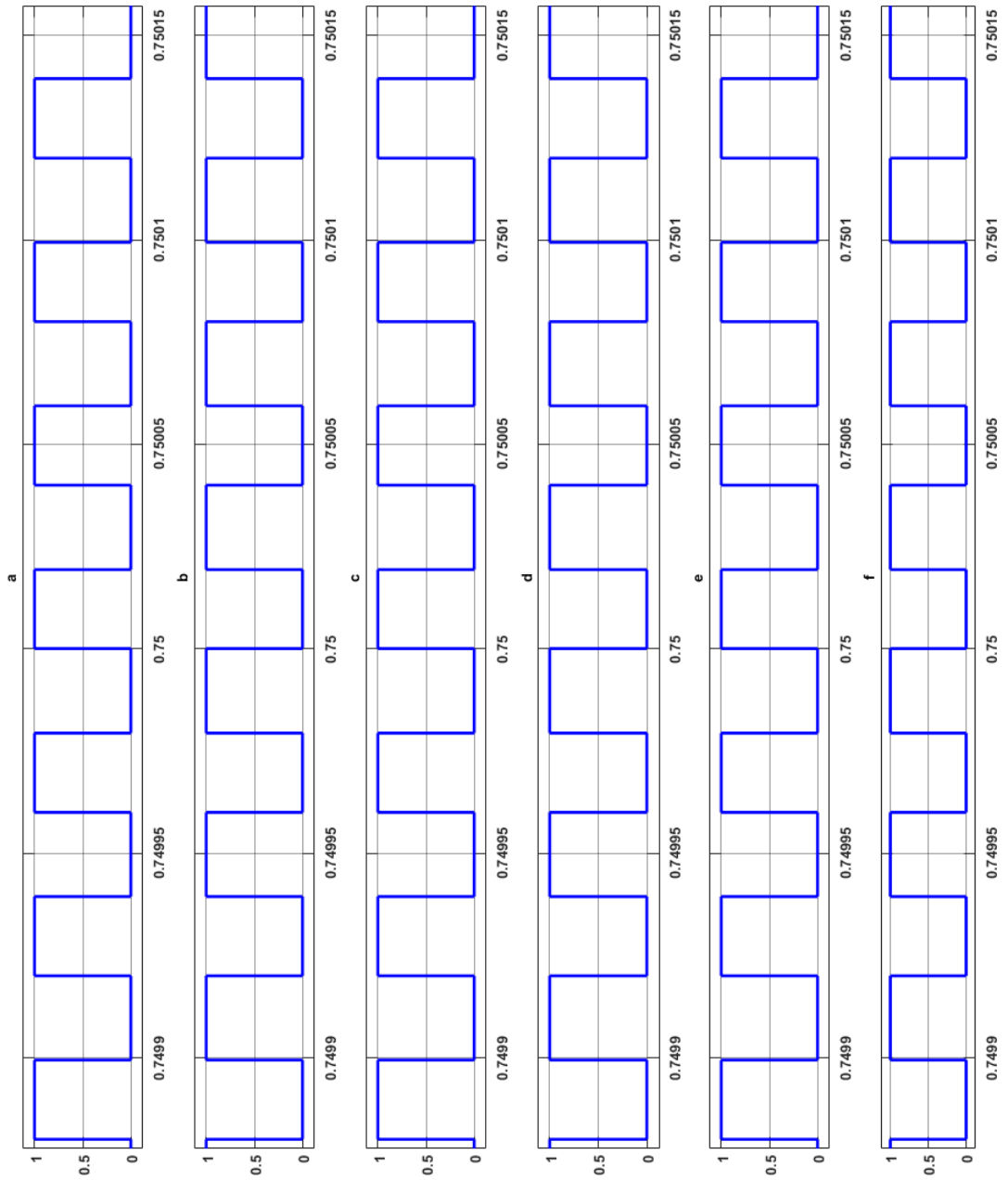


Figure 6-35: Duty Cycle for each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

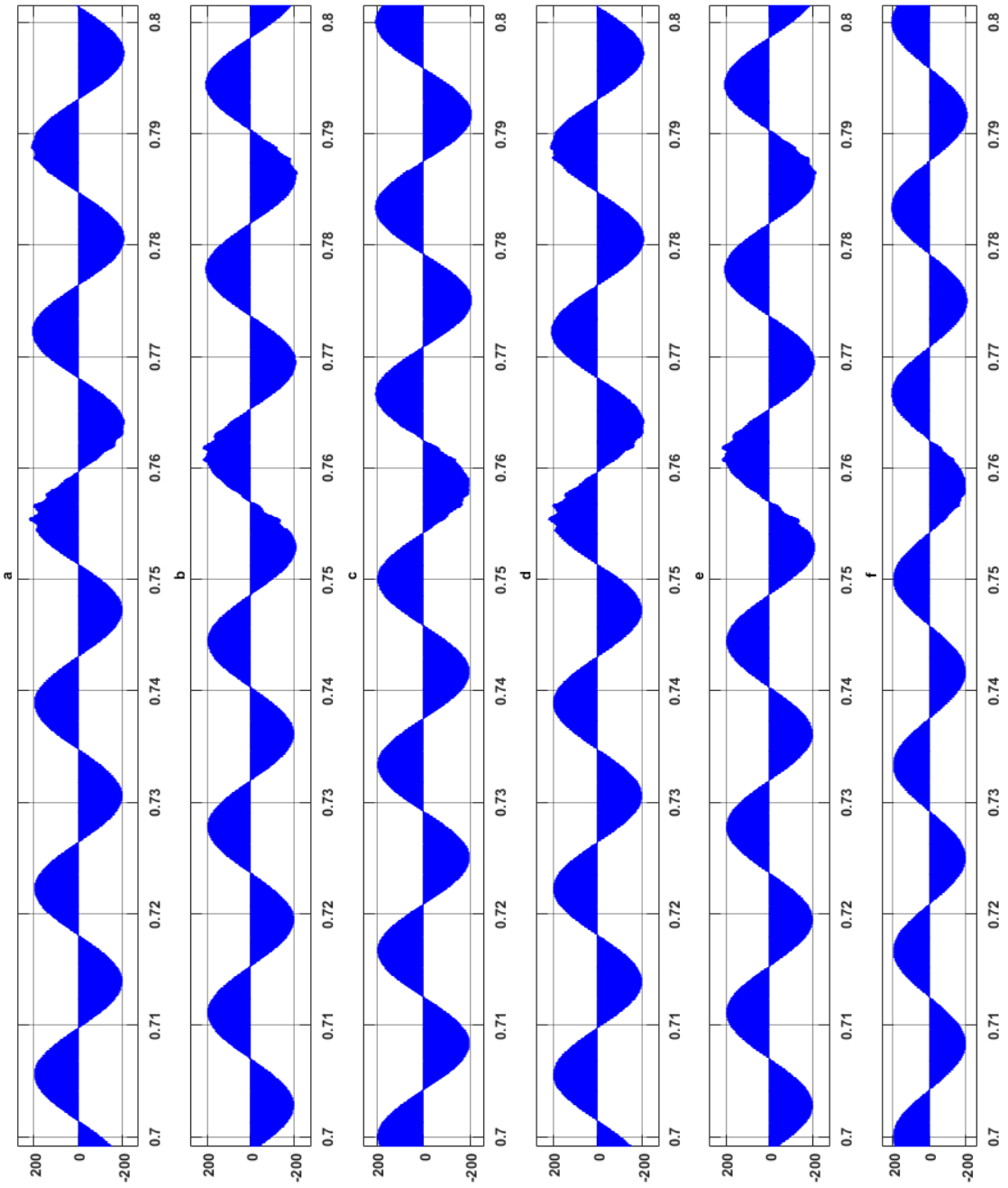


Figure 6-36: Voltage Stress on each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

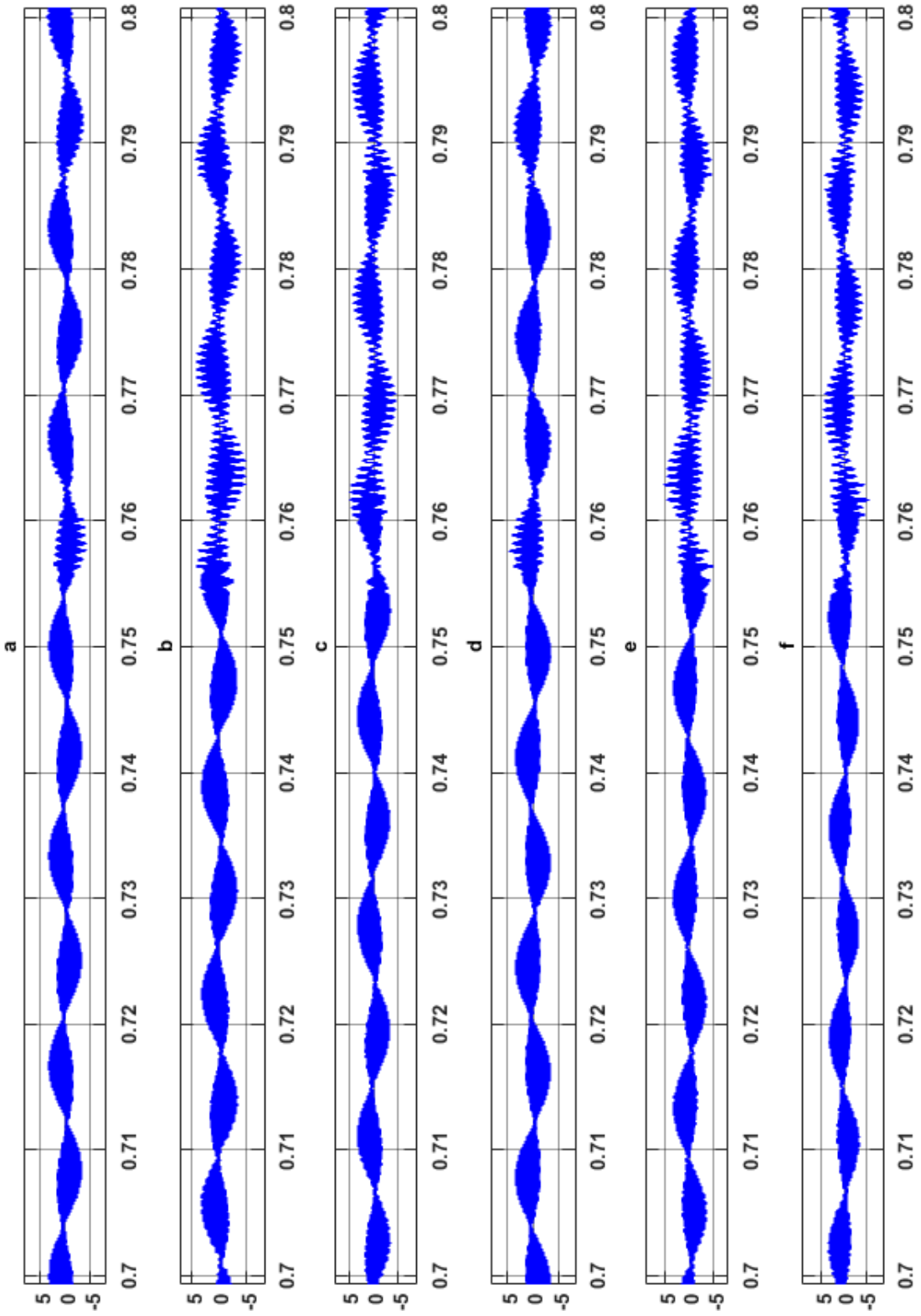


Figure 6-37: Center-Point-Currents

Figure 6-31 displays the input capacitor voltages for each phase. It may be observed that each input capacitor voltage has a rms voltage of $60V_{line\text{-}line}$ applied across its terminals. This voltage division demonstrates the access to the mid-point of input voltage across each phase of CPC PLC. Similar voltage division may also noticed from Figure 6-32, where each output capacitor voltage has a rms value of $60V_{line\text{-}line}$ applied across its terminals. This ensures access to the center-point voltage of the output load voltage. Also, it may be seen that due to step increase in input voltage by 10% at 0.75sec, input capacitor voltages also exhibit step increment by 10% at 0.75 sec. But due to command following reference of the controller, output capacitor voltages do not get increased by 10%. These capacitor voltages get back to half of the desired output voltage within one cycle. The voltages across the buck-boost inductors in CPC PLC converter topology have been presented in Figure 6-33. The voltage across each inductor also has a rms voltage of $60V_{line\text{-}line}$. But step change in input voltage reflects in the inductor voltage as well, where it settles to a voltage, such that the output voltage is controlled to desired voltage reference. The current through the buck-boost inductors have also been captured in Figure 6-34. The duty cycle waveforms are shown in Figure 6-35. Since the input and output capacitor voltages are balanced, the peak voltage stress across the switches are equal to half the summation of input and output voltage, which is equal to a peak voltage of $170V_{ac}$. The voltage stress waveforms are displayed in Figure 6-36. The current flowing through the center-point connections in the input side as well as the output side are shown in Figure 6-37.

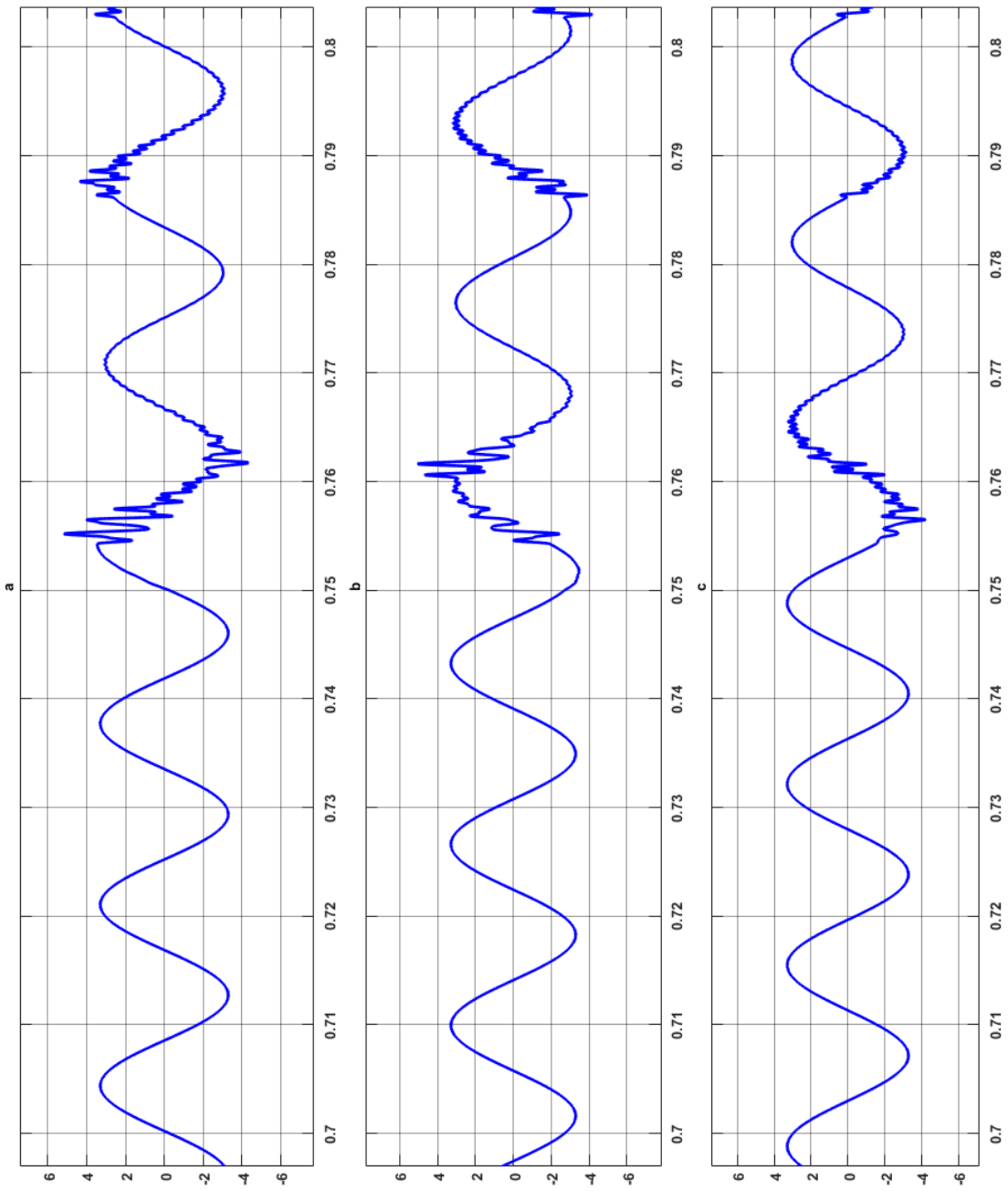


Figure 6-38: Input source currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

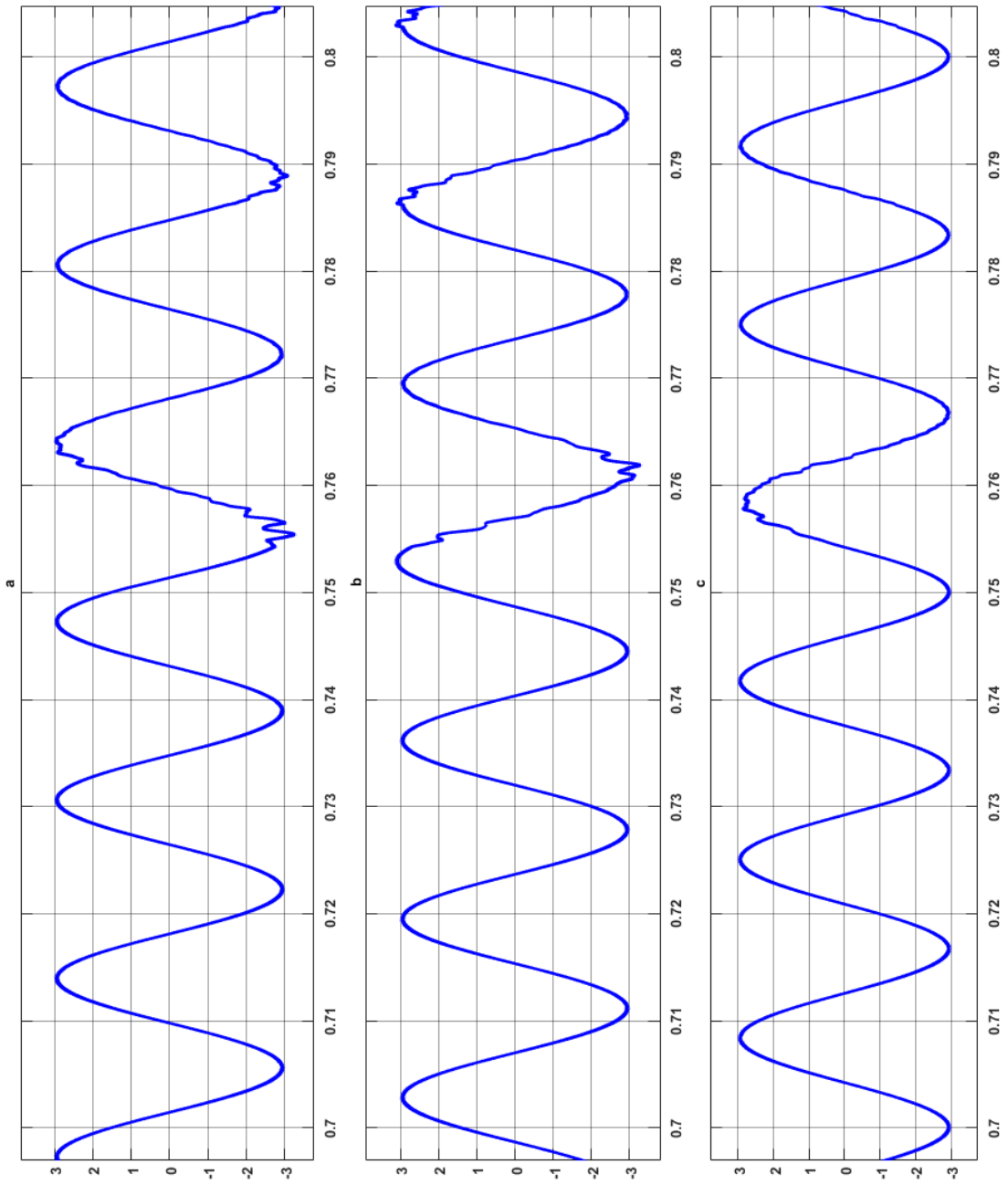


Figure 6-39: Output load currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

It may be seen from Figure 6-38 and Figure 6-39, with step increase in input voltage at 0.75seconds, the input line current gets decreased to compensate for the increase in voltage, as the controller modulates the duty cycle to regulate constant desired line output voltage. The output line current is still regulated at the same peak value as it was before the step change in input voltage at 0.75seconds.

The next sub-section discusses simulation results for a step-decrease in load at 0.75 seconds.

6.3.3. Load Regulation Performance of 3-Ø CPC PLC for low output load

This sub-section presents the simulation results for closed loop operation of 3-Ø CPC PLC for step change in output resistive load when it is decreased from 100ohms to 90ohms. The step change in input voltage is introduced at 0.75 seconds of simulation time. The source input voltage for each of the phase of 3-Ø CPC PLC is shown in Figure 6-40. It may be seen that at 0.75seconds of simulation time, the input voltage remains steady at $120V_{acrms}$. But it may be seen from Figure 6-41, the controller regulates the output voltage to desired reference output voltage within one fundamental cycle.

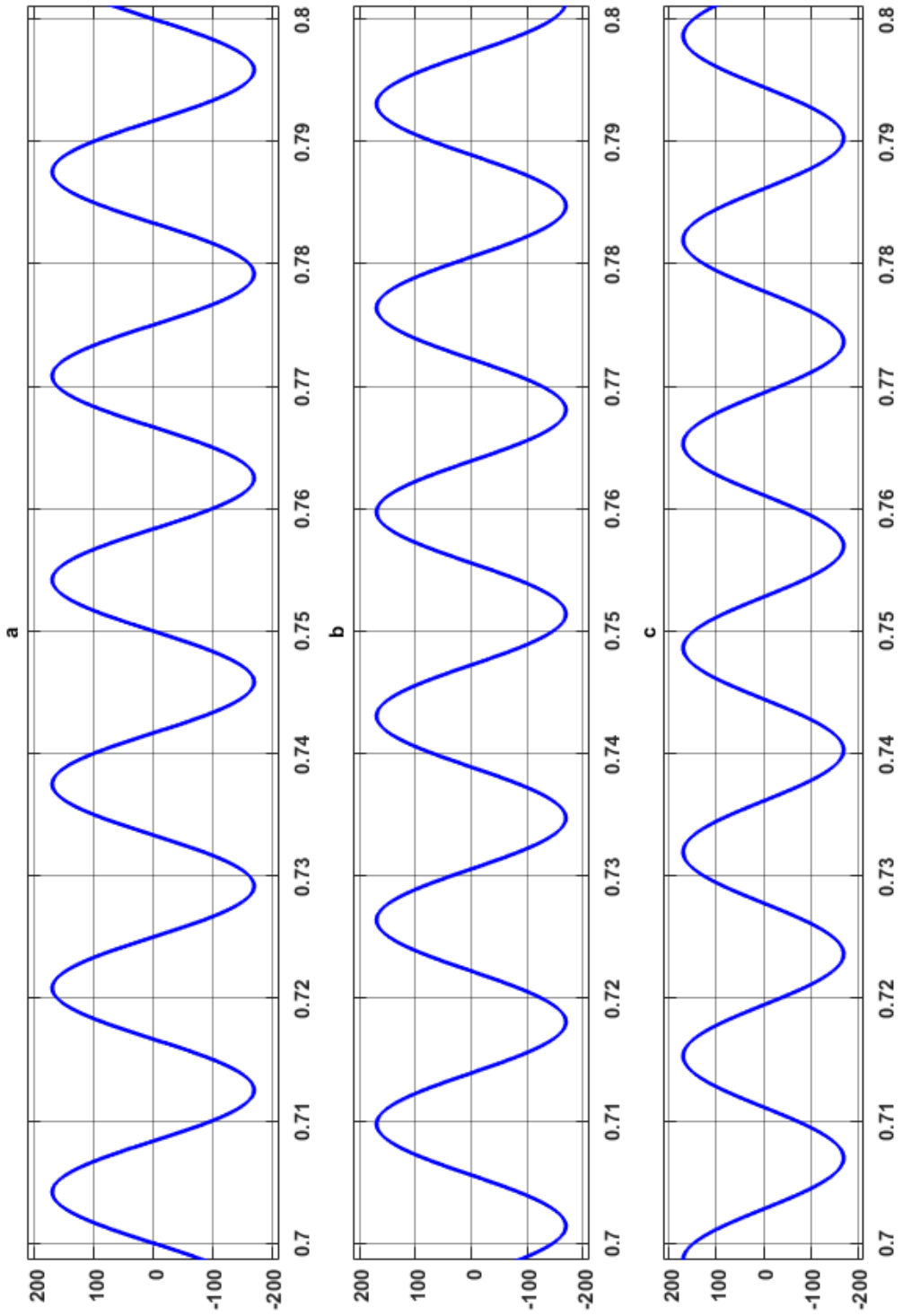


Figure 6-40: Input source voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

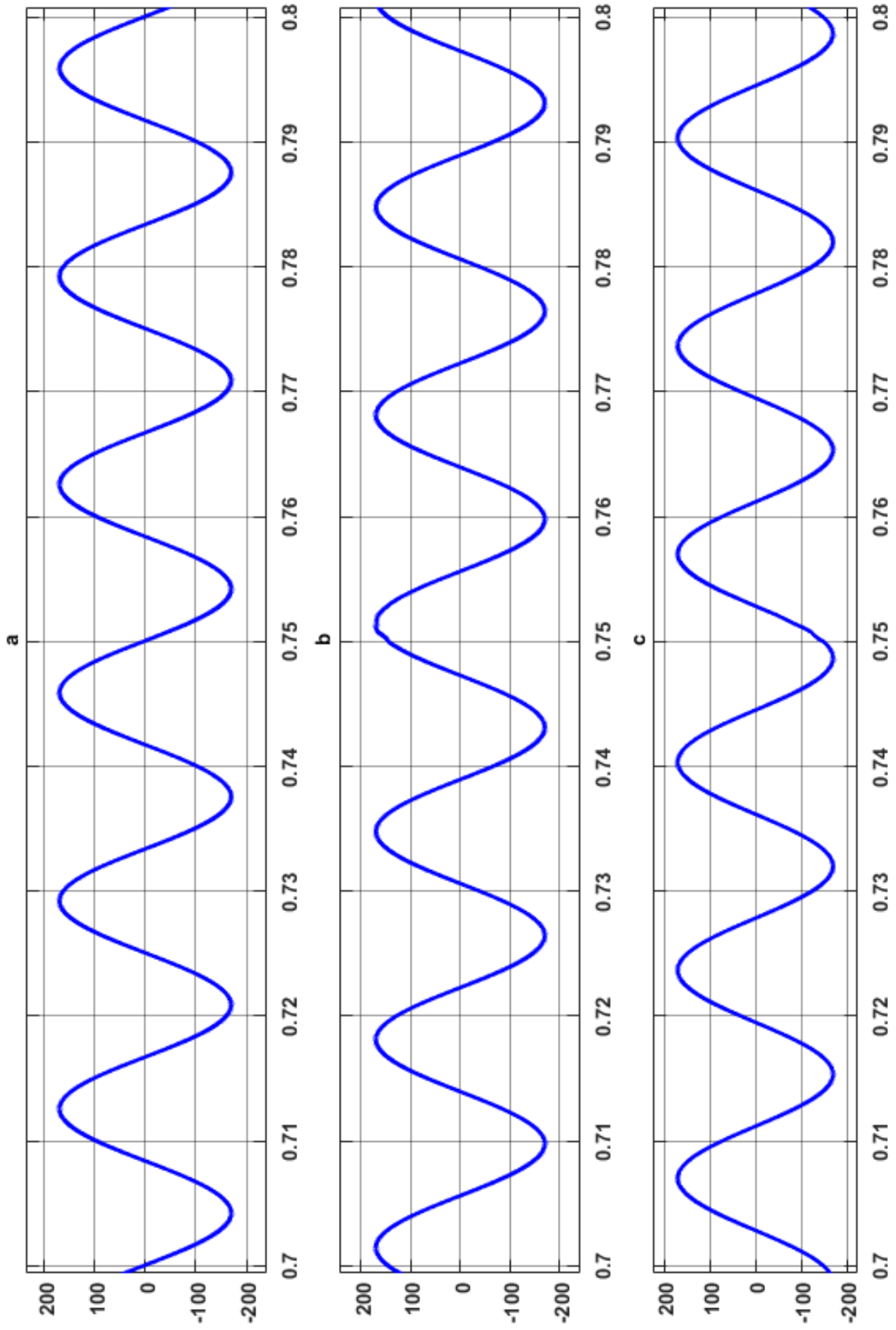


Figure 6-41: Output load voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

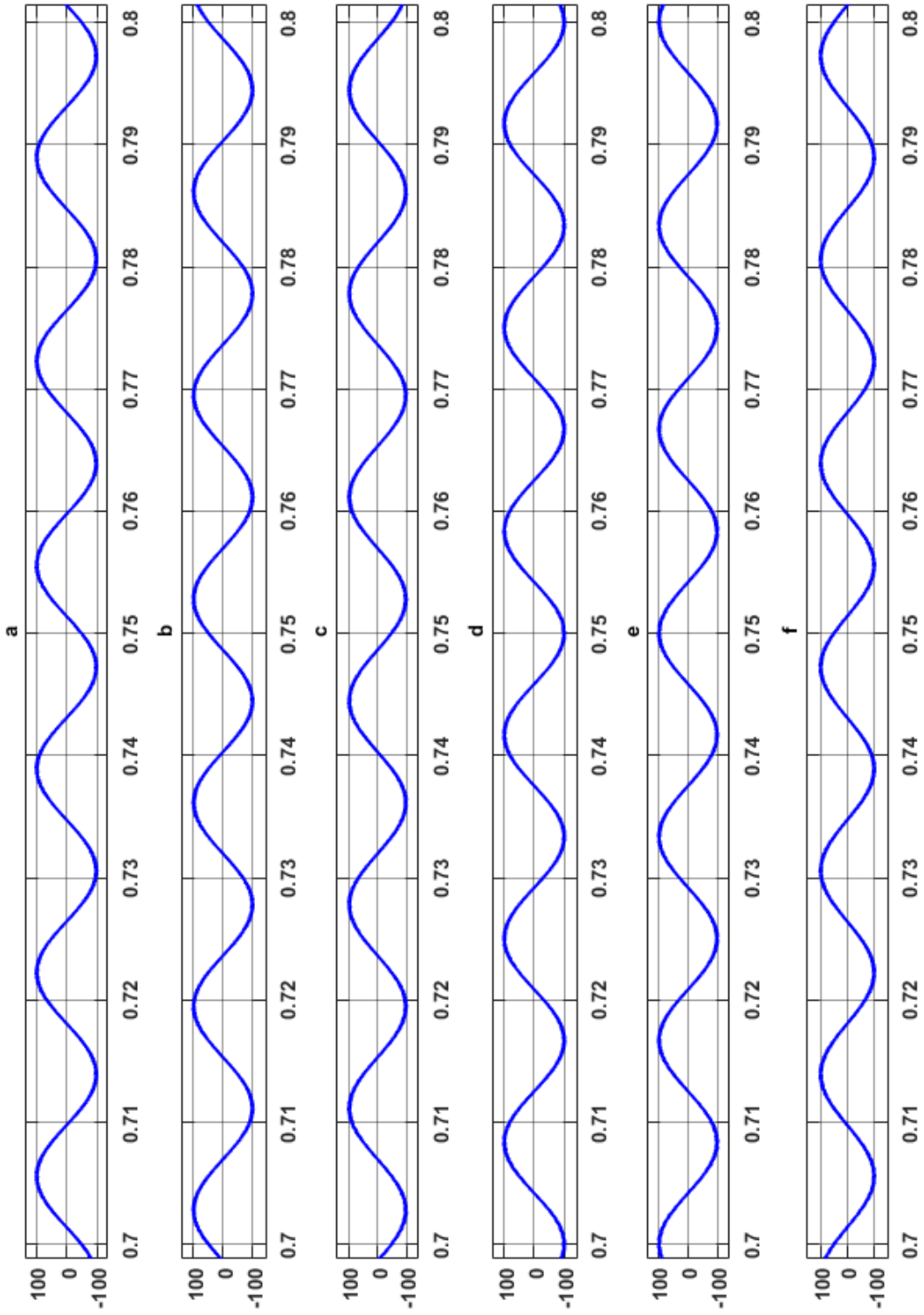


Figure 6-42: Input capacitor voltages (a) Voltage across input capacitor, C_{i1_a}, (b) Voltage across input capacitor, C_{i2_a}, (c) Voltage across input capacitor, C_{i1_b}, (d) Voltage across input capacitor, C_{i2_b}, (c) Voltage across input capacitor, C_{i1_c}, and (d) Voltage across input capacitor, C_{i2_c}.

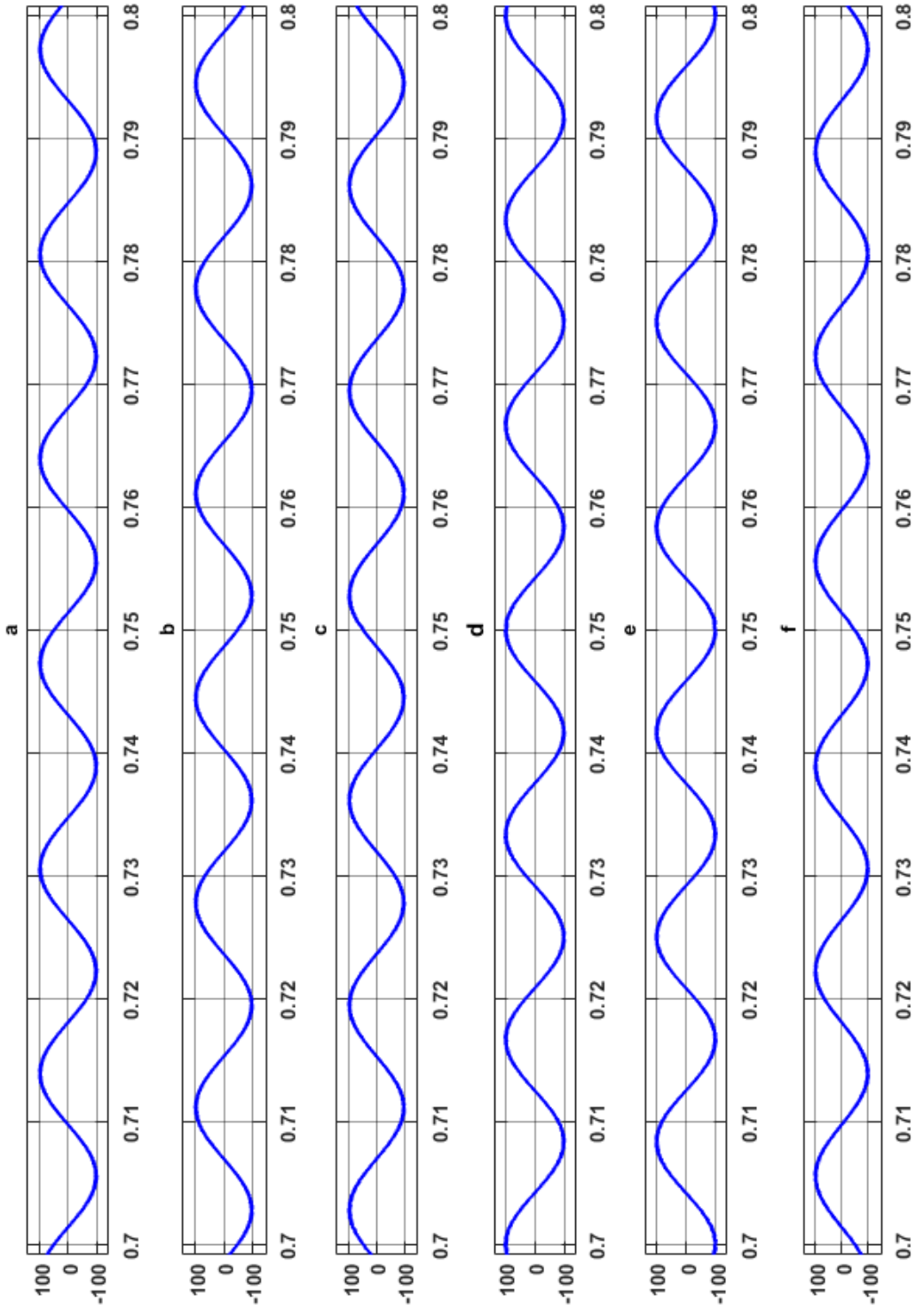


Figure 6-43: Output capacitor voltages a) Voltage across input capacitor, C_{o1_a}, (b) Voltage across input capacitor, C_{o2_a}, (c) Voltage across input capacitor, C_{o1_b}, (d) Voltage across input capacitor, C_{o2_b}, (c) Voltage across input capacitor, C_{o1_c}, and (d) Voltage across input capacitor, C_{o2_c}.

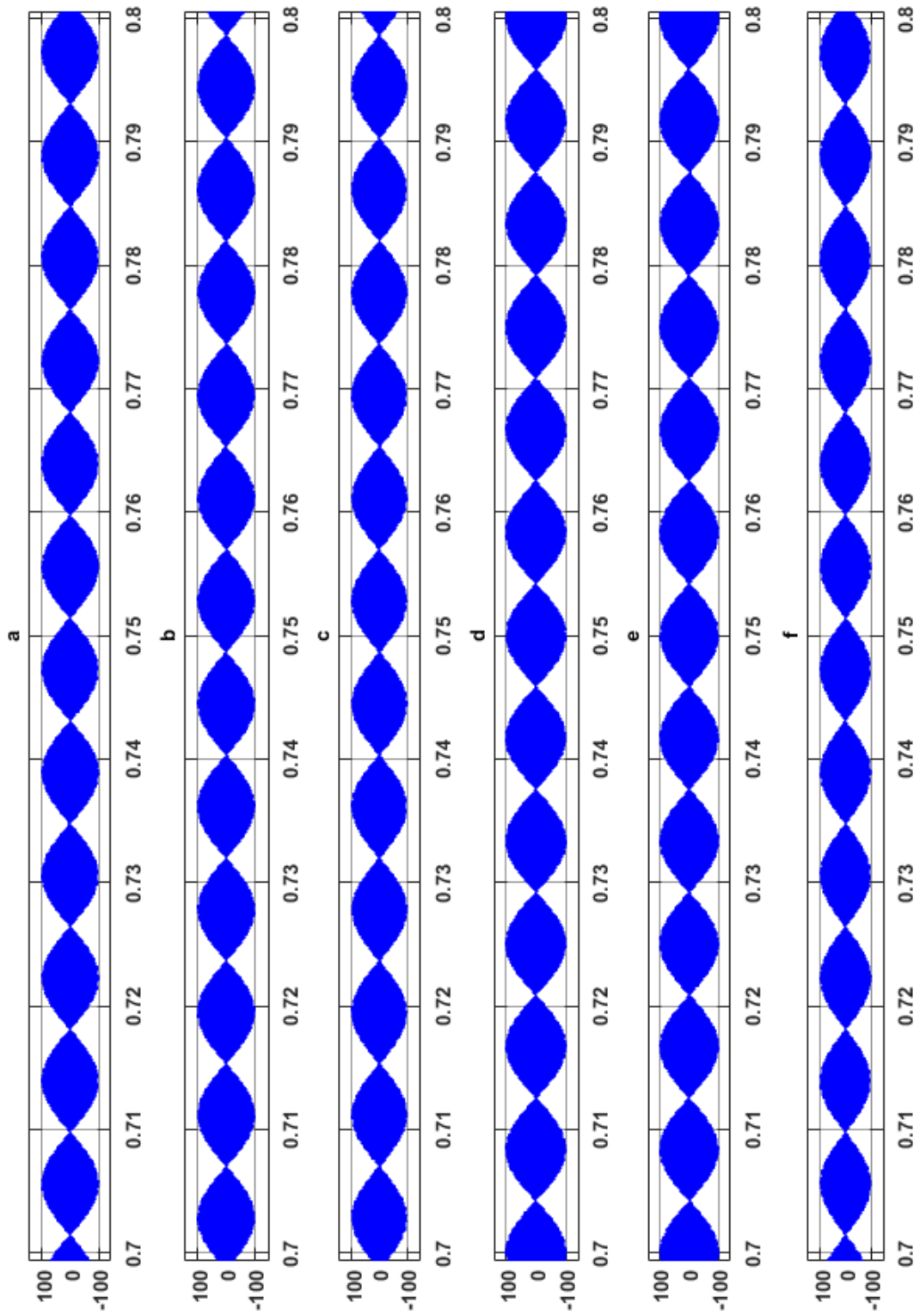


Figure 6-44: Buck-boost inductor voltages (a) Voltage across inductor, L_{1_a}, (b) Voltage across inductor, L_{2_a}, (c) Voltage across inductor, L_{1_b}, (d) Voltage across inductor, L_{2_b}, (e) Voltage across inductor, L_{1_c}, and (f) Voltage across inductor, L_{2_c}

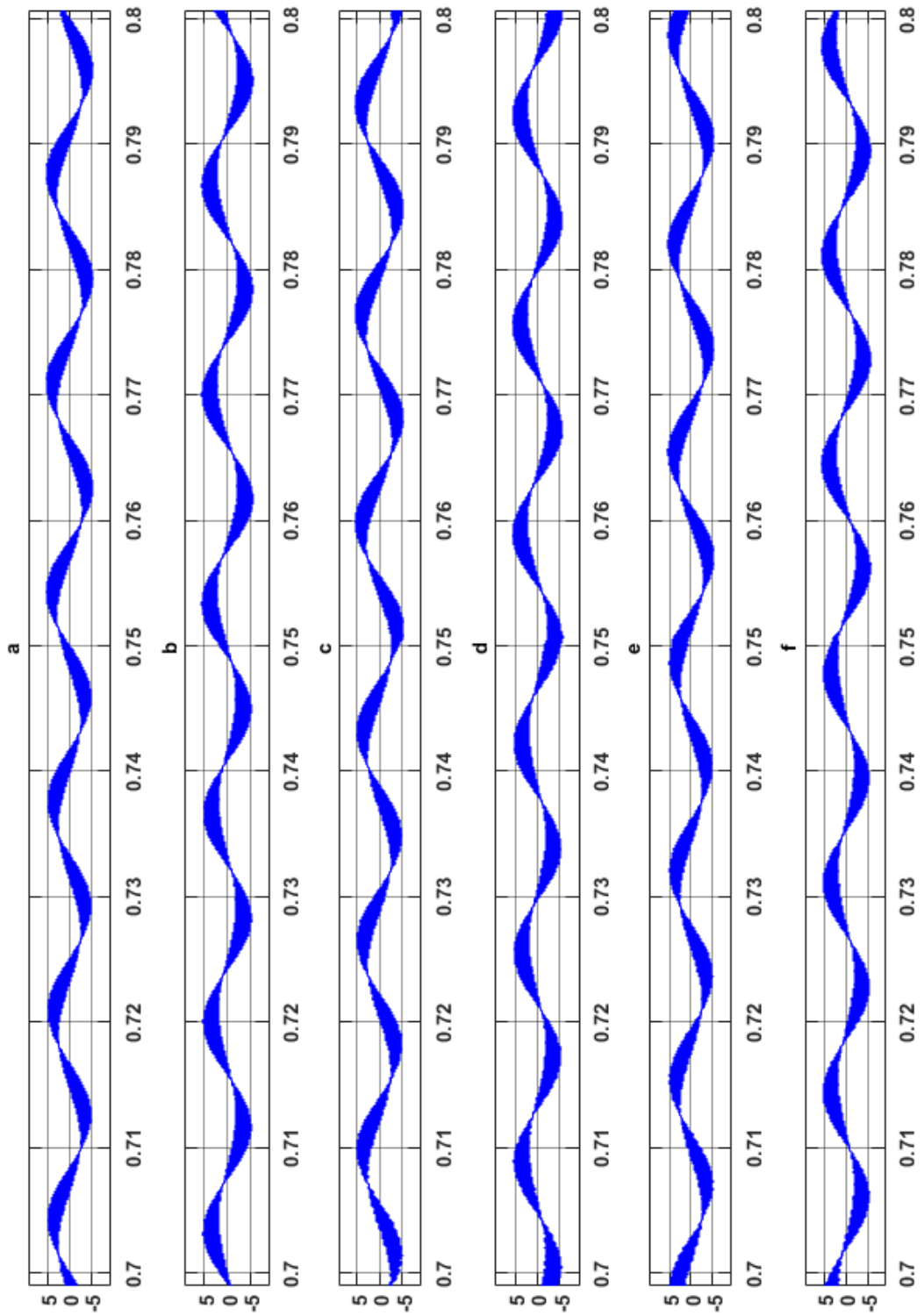


Figure 6-45: Buck-boost inductor currents (a) Current across inductor, L_{1_a}, (b) Current across inductor, L_{2_a}, (c) Current across inductor, L_{1_b}, (d) Current across inductor, L_{2_b}, (e) Current across inductor, L_{1_c}, and (f) Current across inductor, L_{2_c}

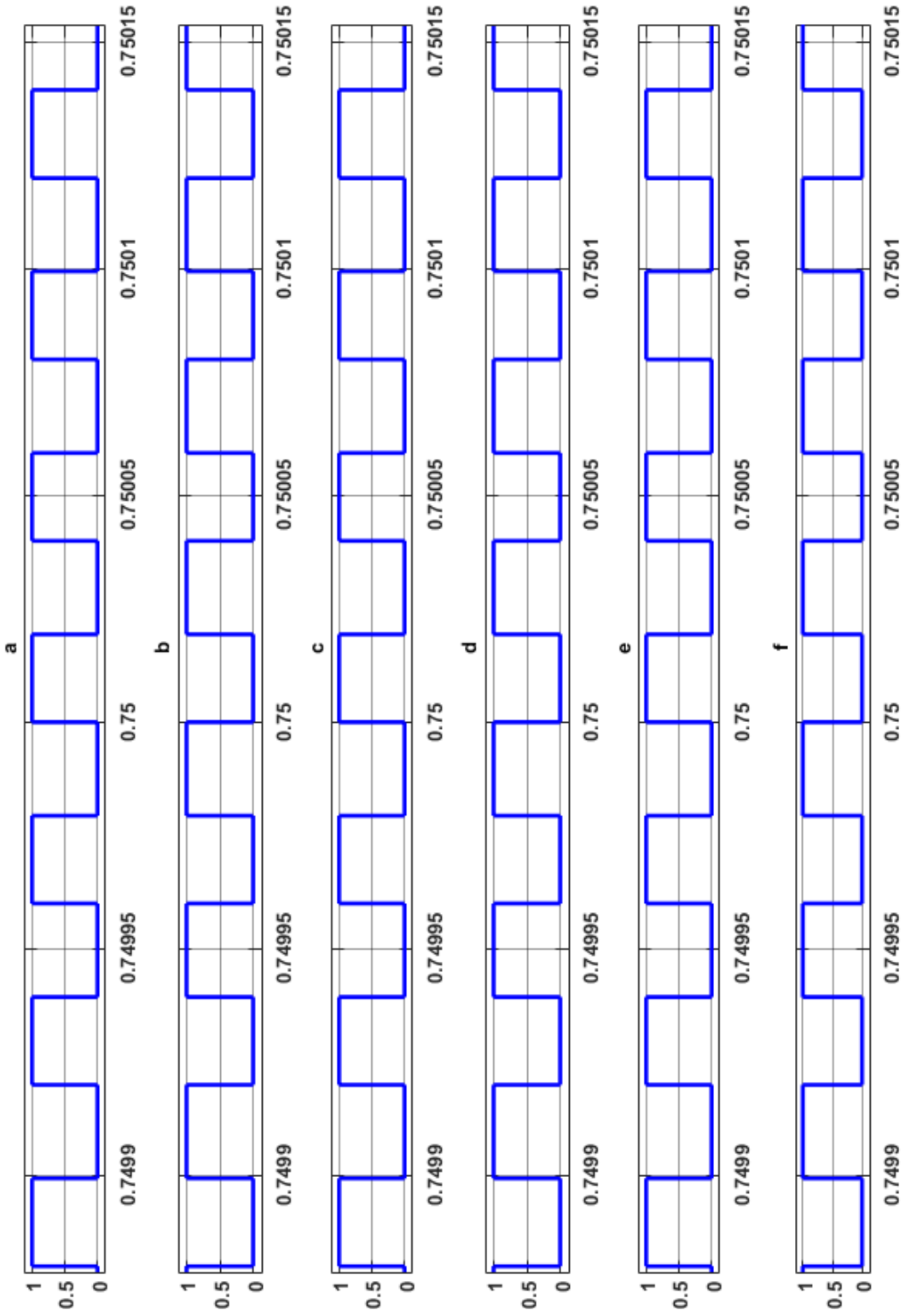


Figure 6-46: Duty Cycle for each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

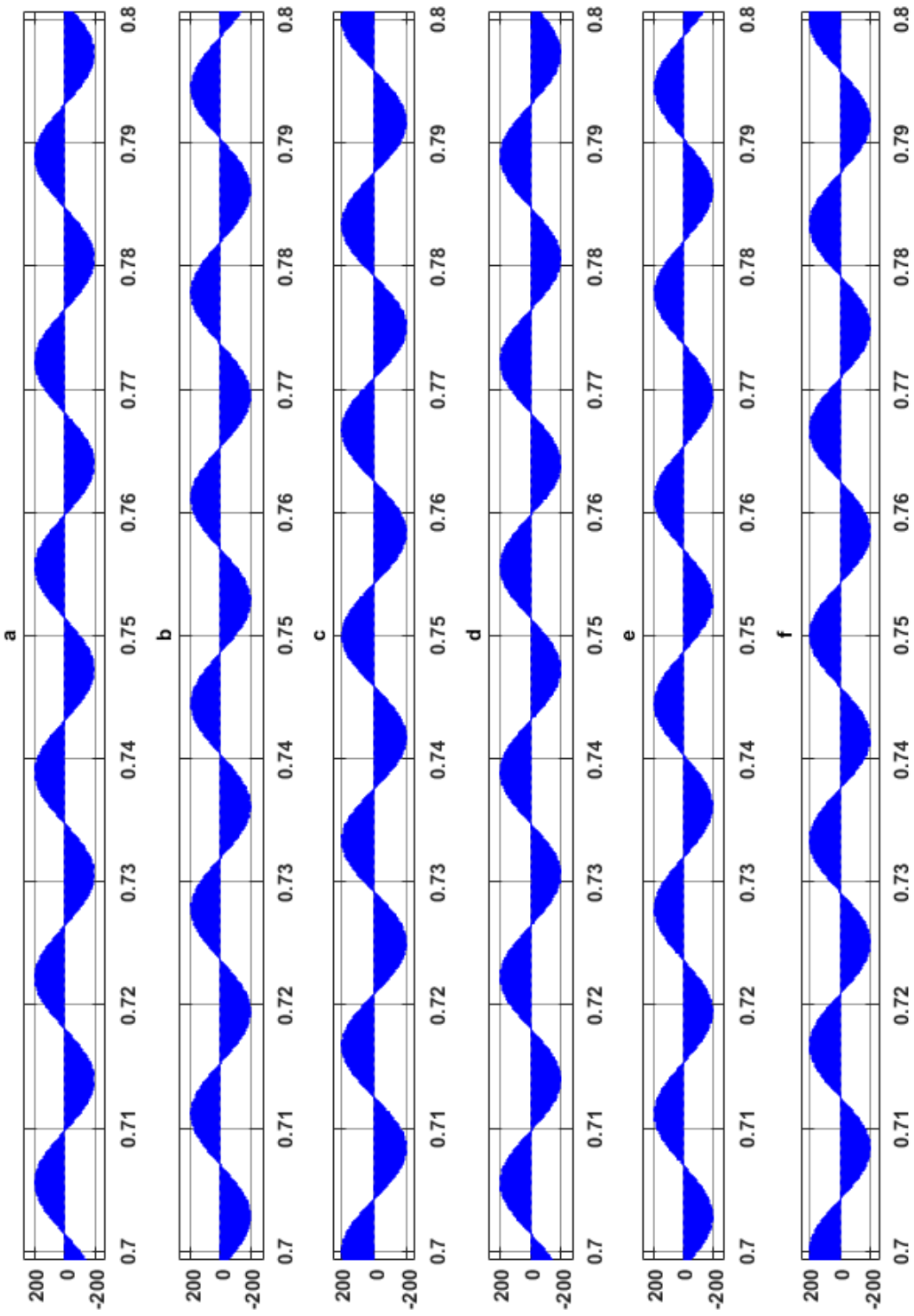


Figure 6-47: Voltage Stress on each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

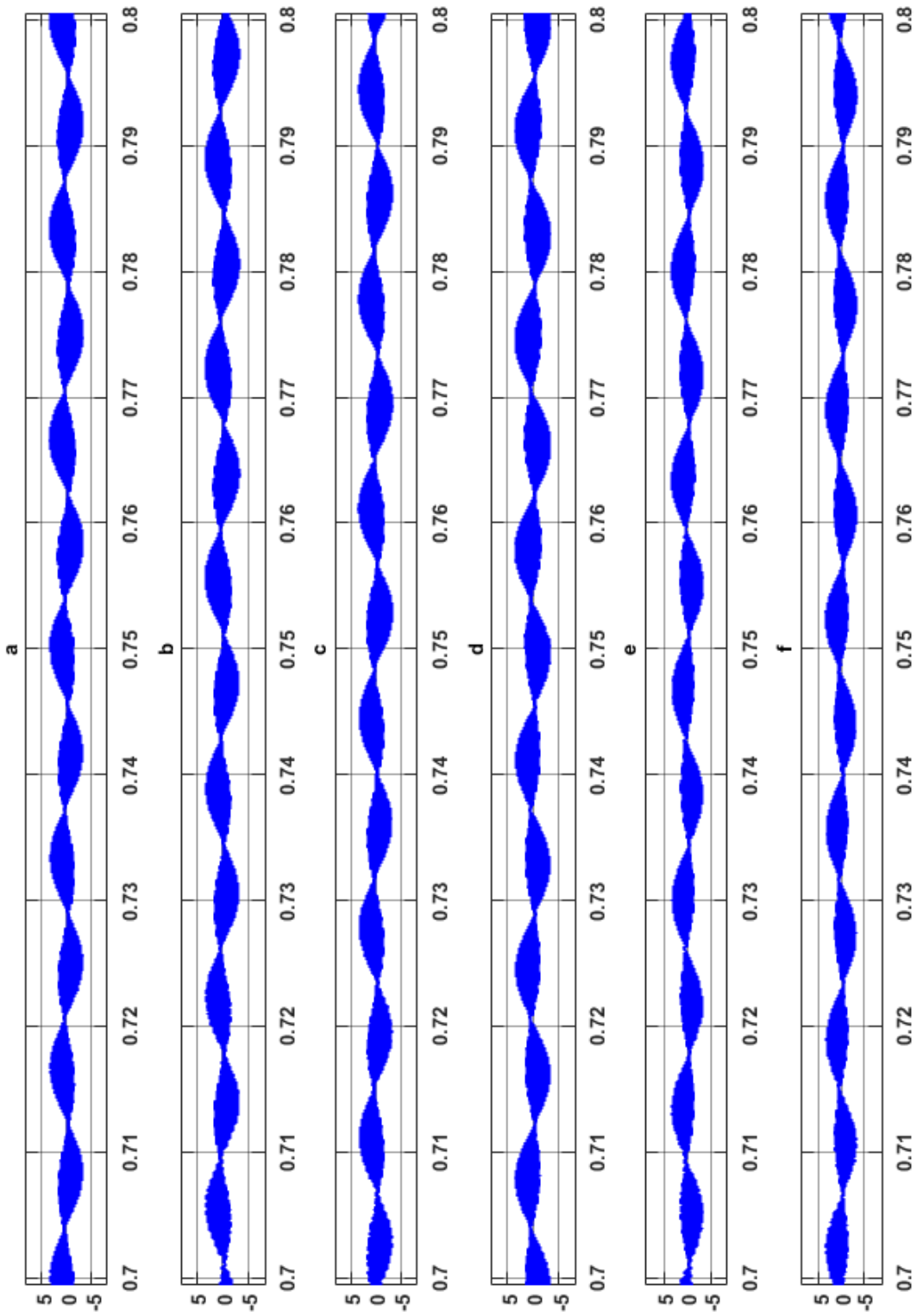


Figure 6-48: Center-Point currents

Figure 6-42 displays the input capacitor voltages for each phase. It may be observed that each input capacitor voltage has a rms voltage of $60V_{line\text{-}line}$ applied across its terminals. This voltage division demonstrates the access to the mid-point of input voltage across each phase of CPC PLC. Similar voltage division may also noticed from Figure 6-43, where each output capacitor voltage has a rms value of $60V_{line\text{-}line}$ applied across its terminals. This ensures access to the center-point voltage of the output load voltage. Also, it may be seen that due to step decrease in load by 10% at 0.75sec, input capacitor voltages remain steady at $60V_{line\text{-}line}$. But due to command following reference of the controller, output capacitor voltages get back to half of the desired output voltage within one cycle. The voltages across the buck-boost inductors in CPC PLC converter topology have been presented in Figure 6-44. The voltage across each inductor also has a rms voltage of $60V_{line\text{-}line}$. The current through the buck-boost inductors have also been captured in Figure 6-45. But step change in output load reflects in the inductor current as well, where it settles to a new value according to load demand. The duty cycle waveforms are shown in Figure 6-46. Since the input and output capacitor voltages are balanced, the peak voltage stress across the switches are equal to half the summation of input and output voltage, which is equal to a peak voltage of $170V_{ac}$. The voltage stress waveforms are displayed in Figure 6-47. The current flowing through the center-point connections in the input side as well as the output side are shown in Figure 6-48.

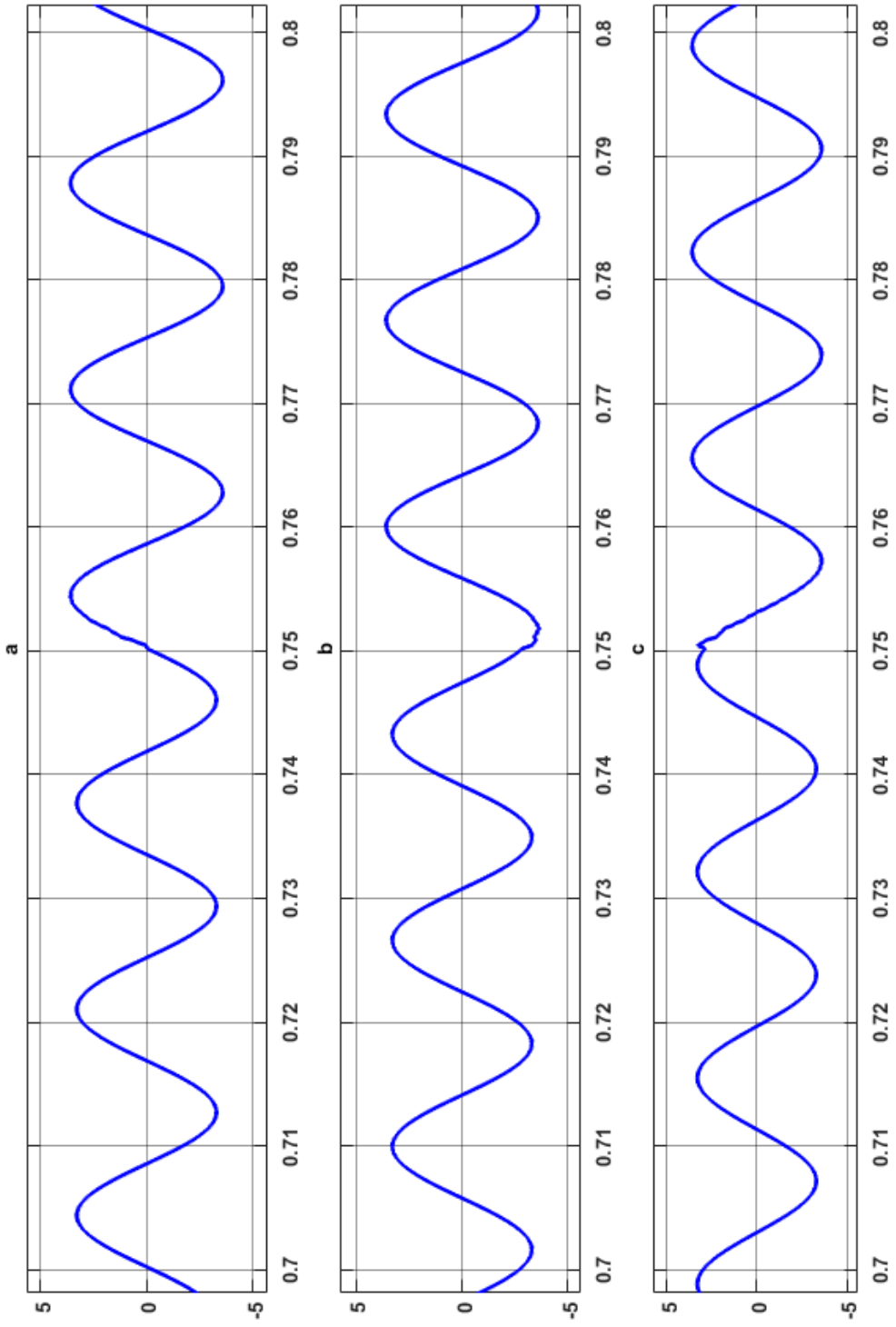


Figure 6-49: Input source currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

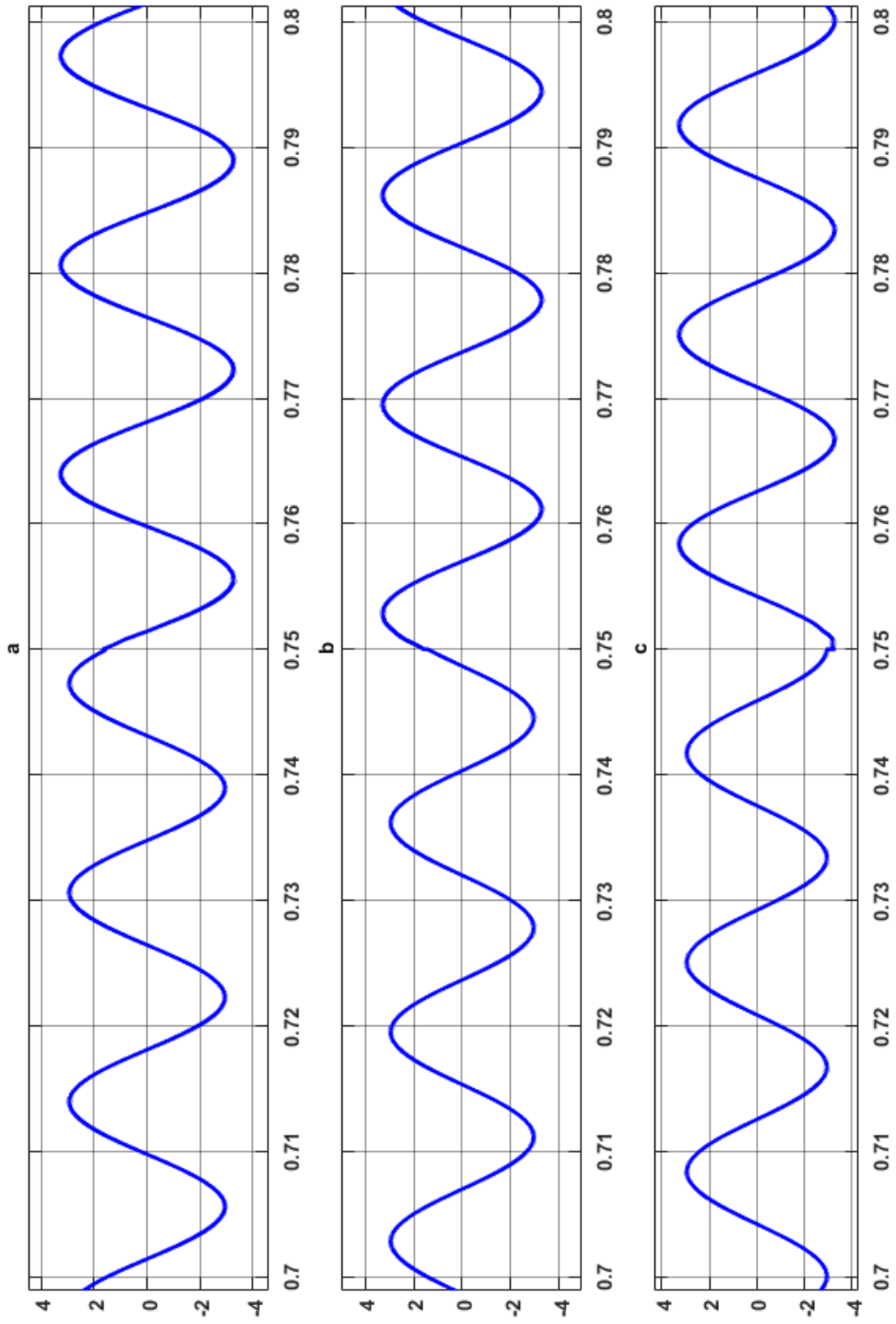


Figure 6-50: Output load currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

It may be seen from Figure 6-27 and Figure 6-28, with step decrease in output load at 0.75seconds, the input line current gets increased by 10% to compensate for the increase in output load demand, as the controller modulates the duty cycle to regulate constant desired line output voltage. The output line current also gets increased by 10% with the step decrease in output load by 10% at 0.75seconds.

The next sub-section discusses simulation results for a step-increase in output load at 0.75 seconds.

6.3.4. Load Regulation Performance of 3-Ø CPC PLC for high output load

This sub-section presents the simulation results for closed loop operation of 3-Ø CPC PLC for step change in output load when it is increased from 100ohms to 110ohms. The step change in input voltage is introduced at 0.75 seconds of simulation time. The source input voltage for each of the phase of 3-Ø CPC PLC is shown in Figure 6-51. It may be seen that at 0.75seconds of simulation time, the input voltage remains steady at $120V_{acrms}$. But it may be seen from Figure 6-52, the controller regulates the output voltage to desired reference output voltage within one fundamental cycle.

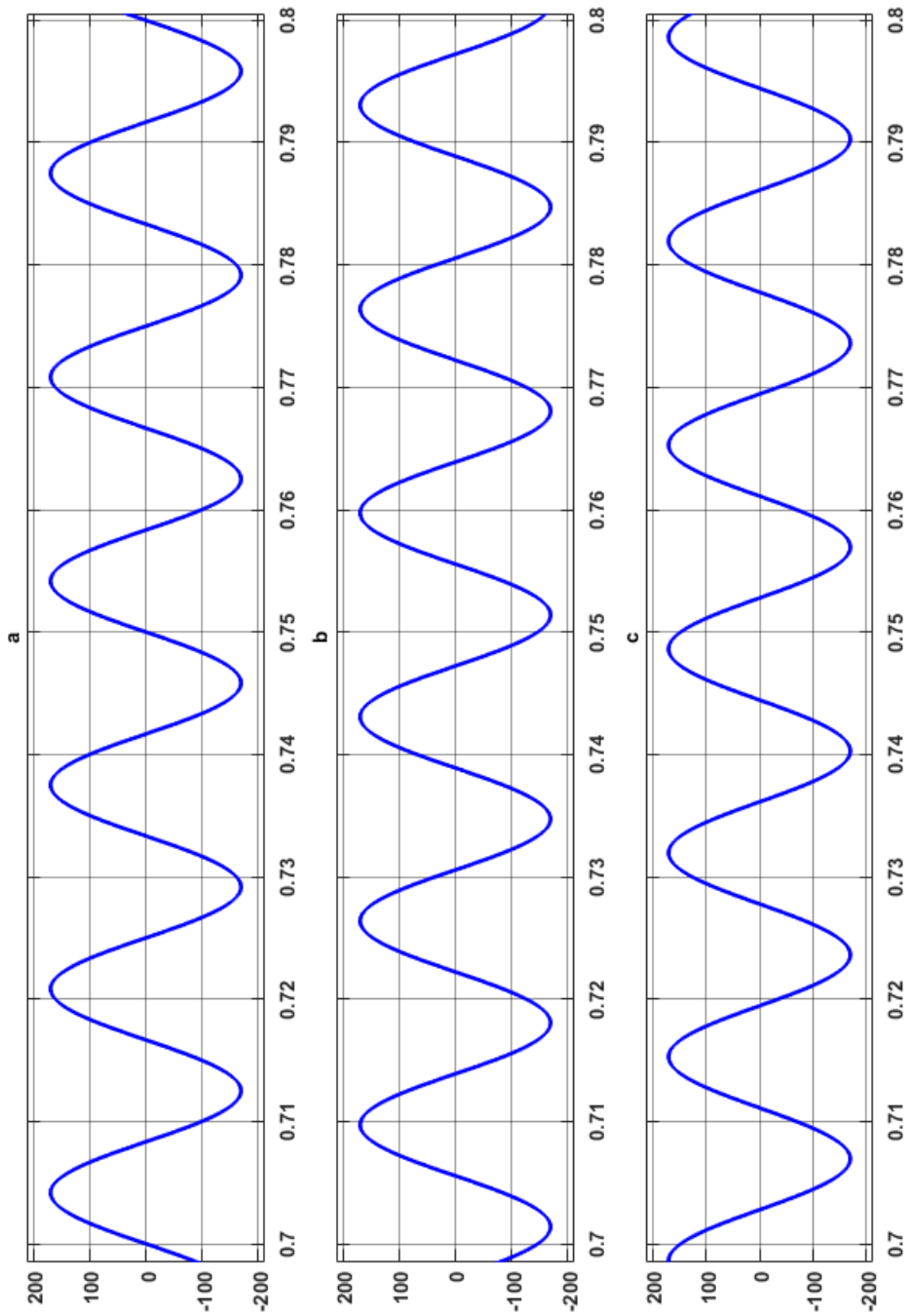


Figure 6-51: Input source voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

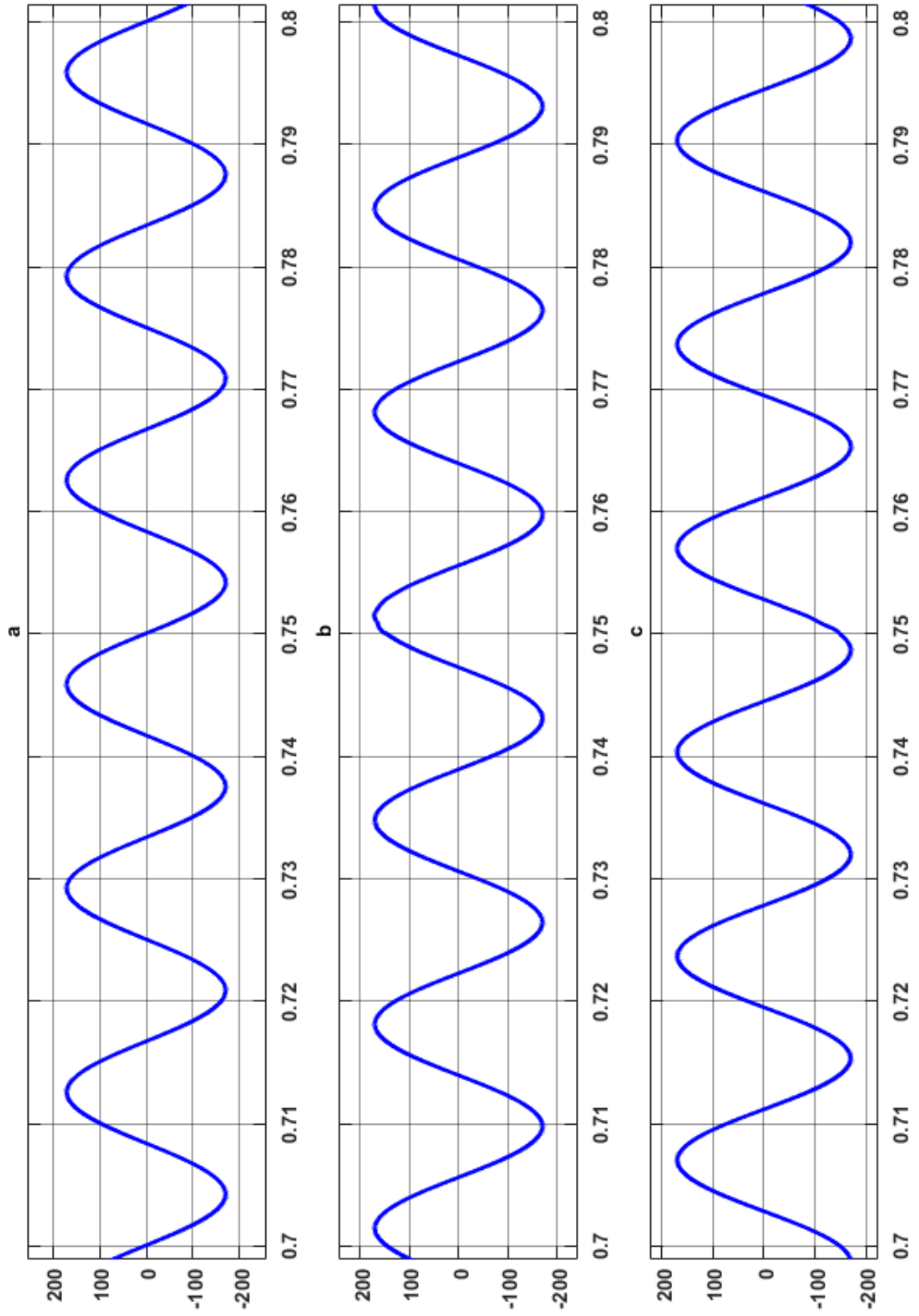


Figure 6-52: Output load voltage of 3-Ø CPC PLC (a) Phase-a line-line voltage, (b) Phase-b line-line voltage, and (c) Phase-c line-line voltage.

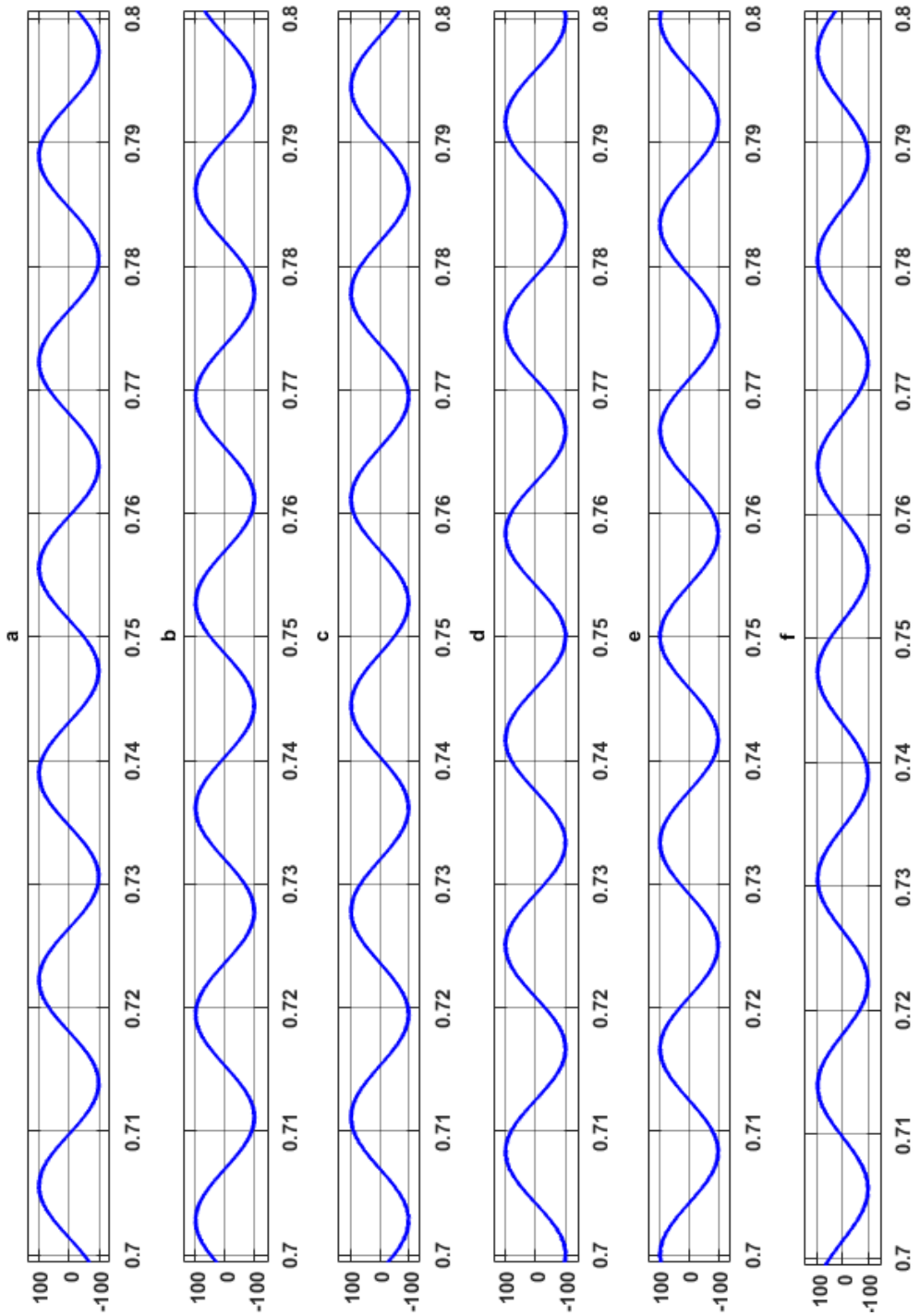


Figure 6-53: Input capacitor voltages (a) Voltage across input capacitor, C_{i1_a}, (b) Voltage across input capacitor, C_{i2_a}, (c) Voltage across input capacitor, C_{i1_b}, (d) Voltage across input capacitor, C_{i2_b}, (c) Voltage across input capacitor, C_{i1_c}, and (d) Voltage across input capacitor, C_{i2_c}.

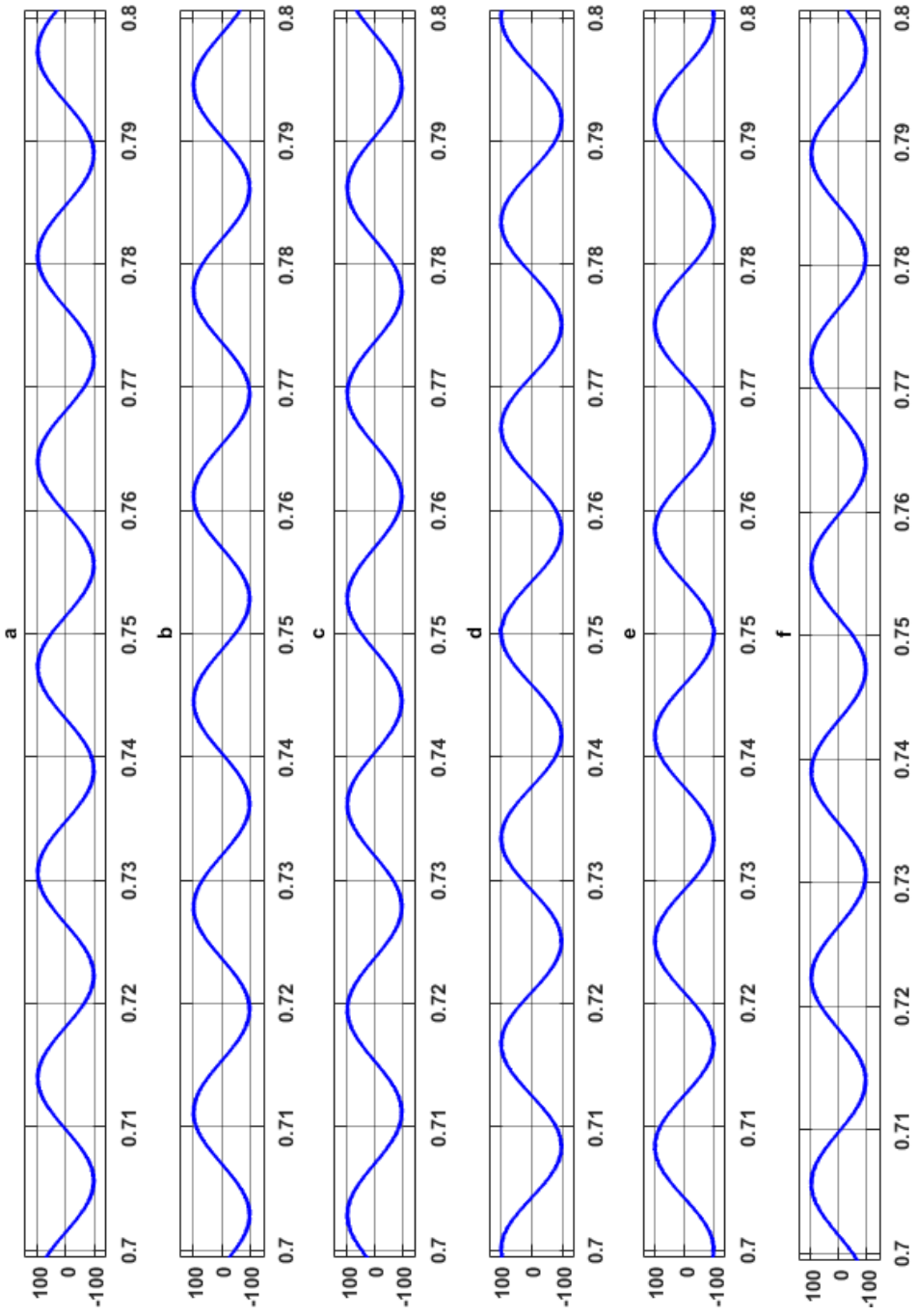


Figure 6-54: Output capacitor voltages a) Voltage across input capacitor, C_{o1_a}, (b) Voltage across input capacitor, C_{o2_a}, (c) Voltage across input capacitor, C_{o1_b}, (d) Voltage across input capacitor, C_{o2_b}, (c) Voltage across input capacitor, C_{o1_c}, and (d) Voltage across input capacitor, C_{o2_c}.

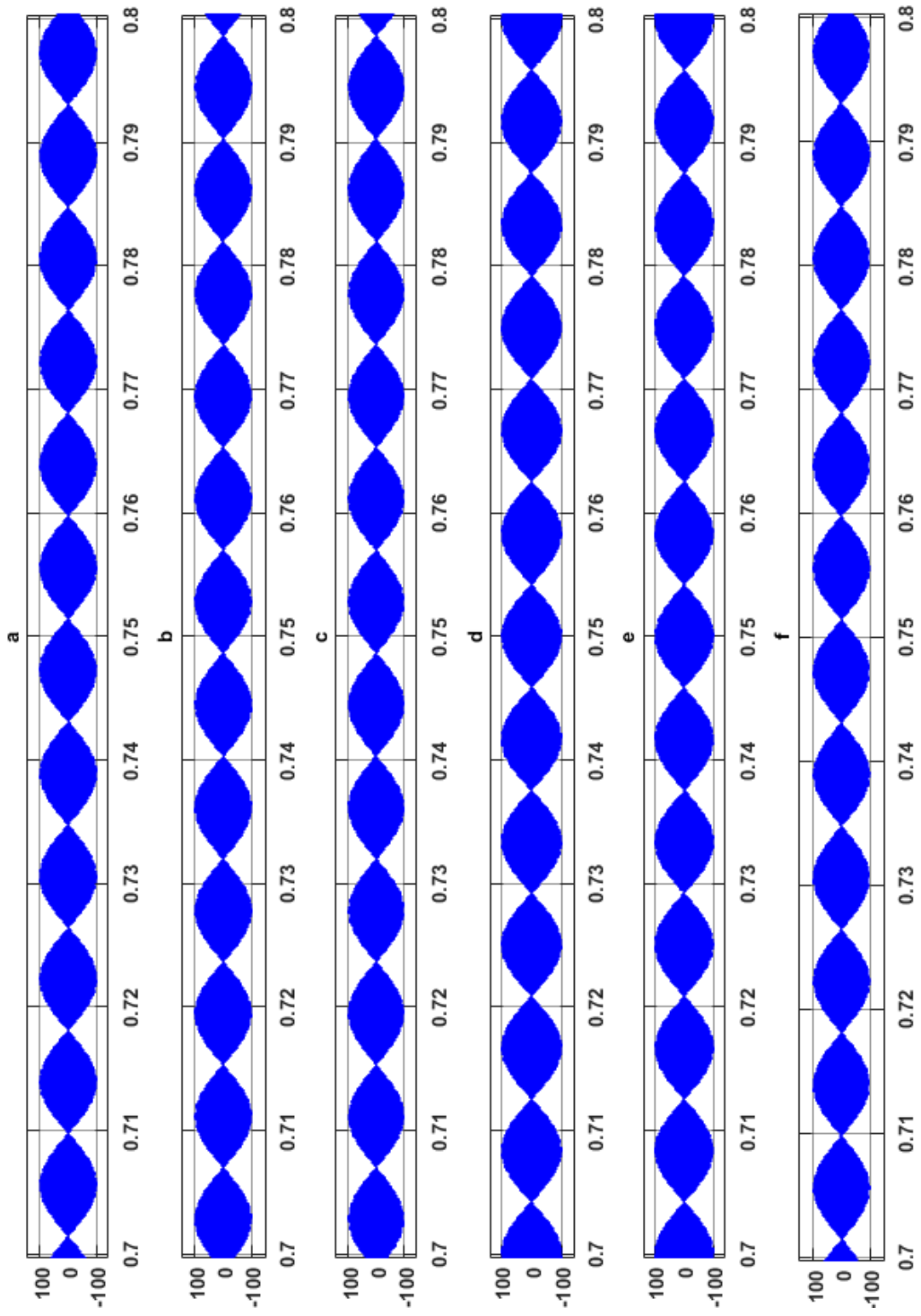


Figure 6-55: Buck-boost inductor voltages (a) Voltage across inductor, L_{1_a}, (b) Voltage across inductor, L_{2_a}, (c) Voltage across inductor, L_{1_b}, (d) Voltage across inductor, L_{2_b}, (e) Voltage across inductor, L_{1_c}, and (f) Voltage across inductor, L_{2_c}

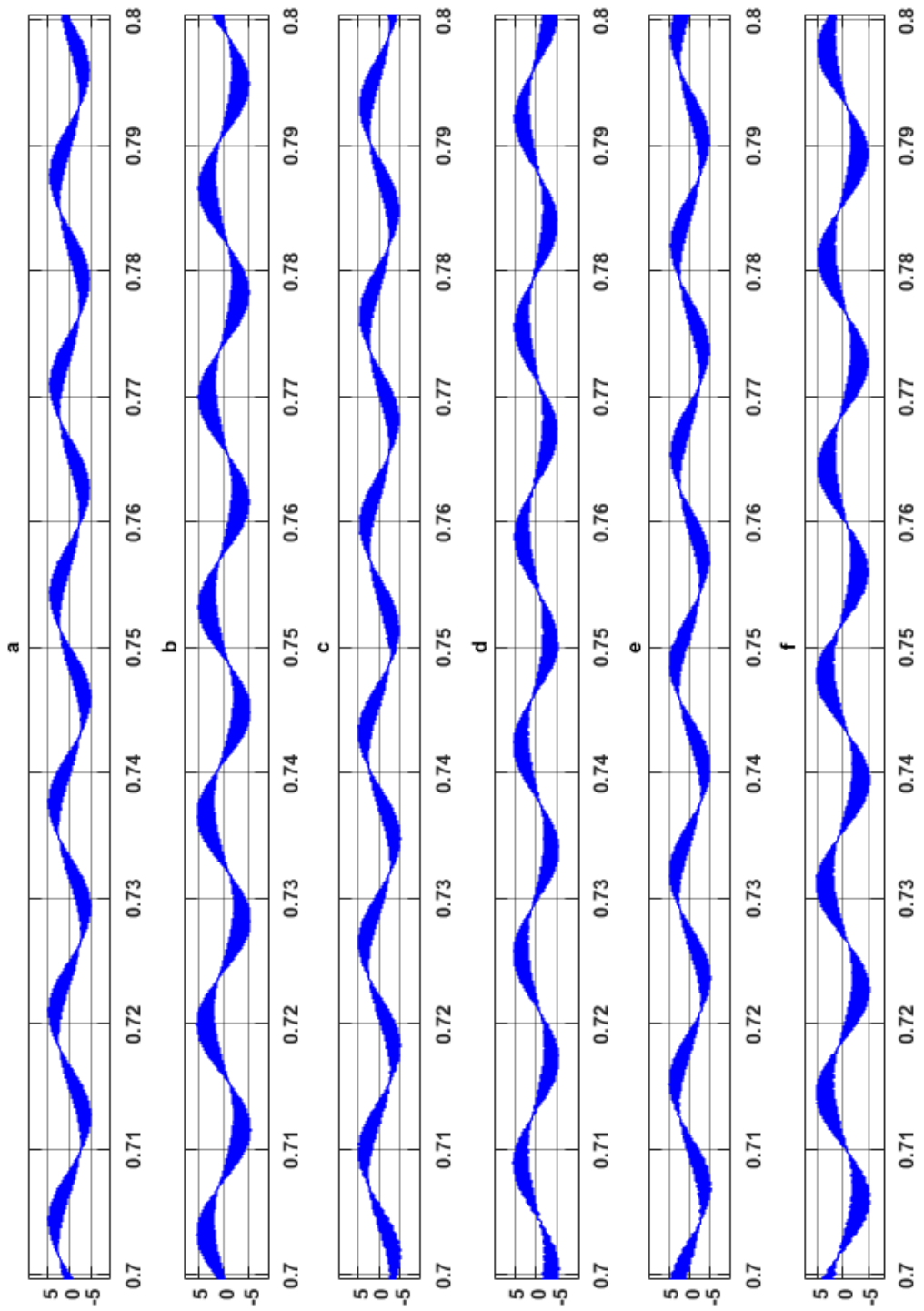


Figure 6-56: Buck-boost inductor currents (a) Current across inductor, L_{1_a}, (b) Current across inductor, L_{2_a}, (c) Current across inductor, $L_{1\_b,}$ (d) Current across inductor, L_{2_b}, (e) Current across inductor, $L_{1\_c,}$ and (f) Current across inductor, L_{2_c}

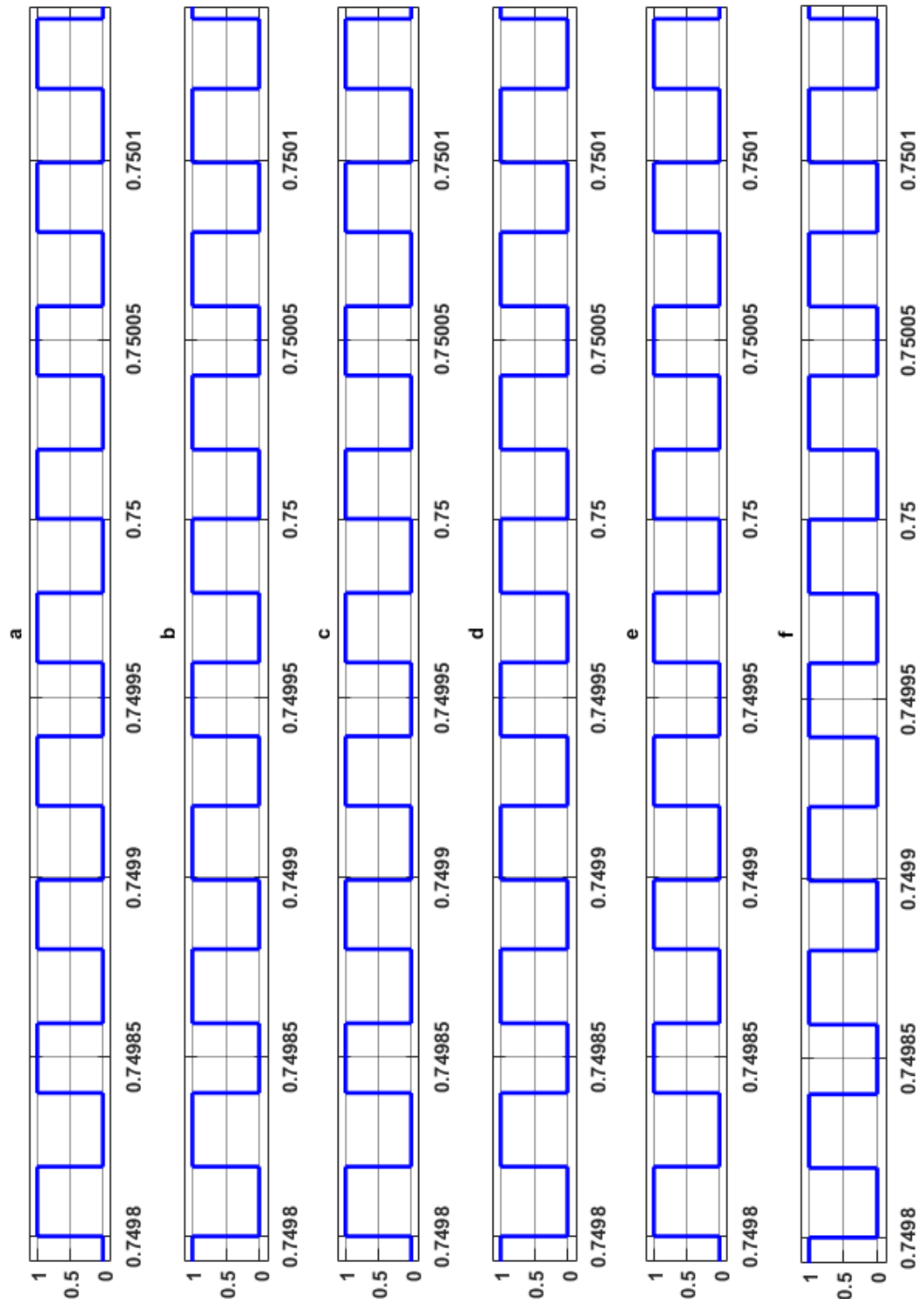


Figure 6-57: Duty Cycle for each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

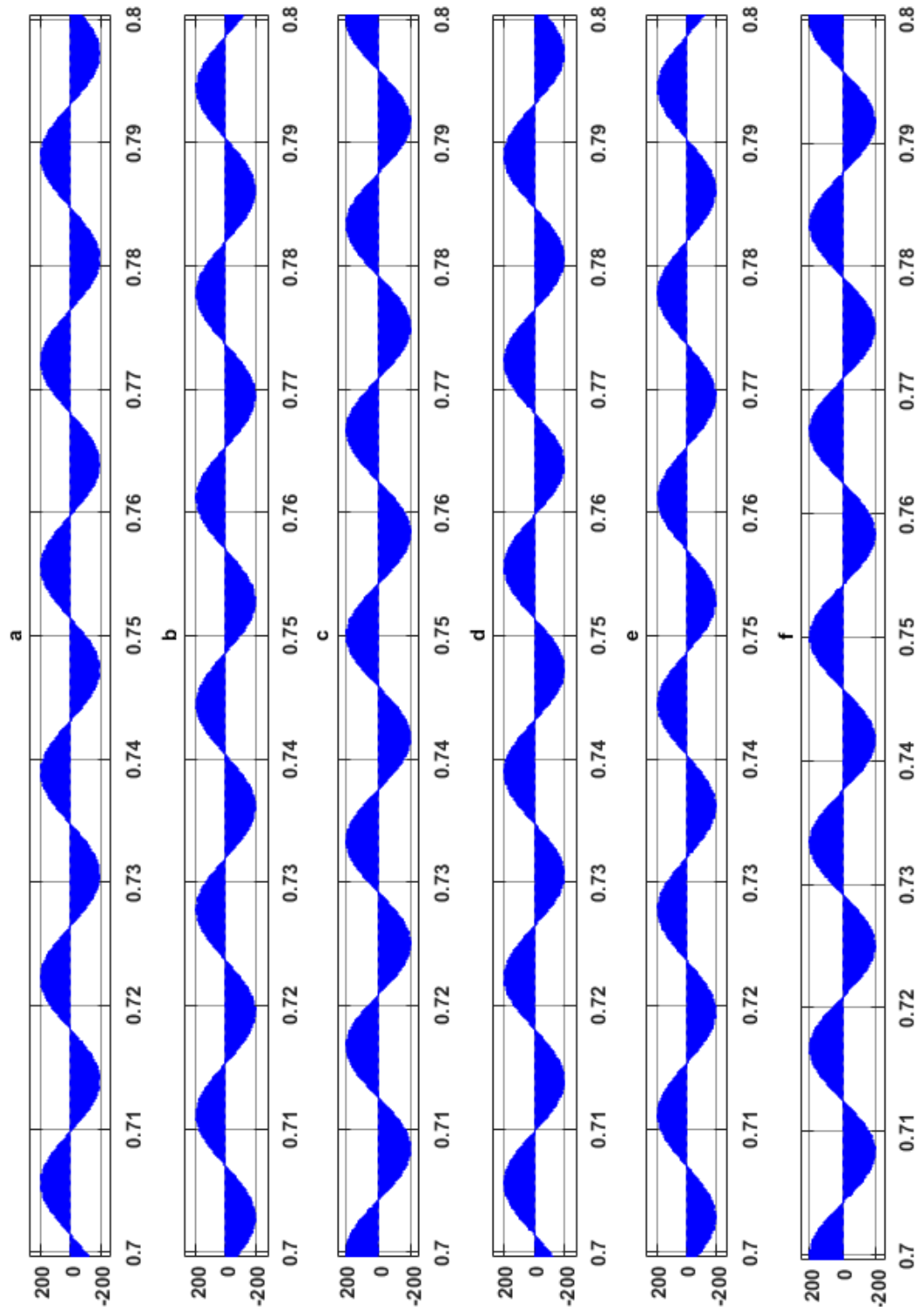


Figure 6-58: Voltage Stress on each switch (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5, and, (f) S_6

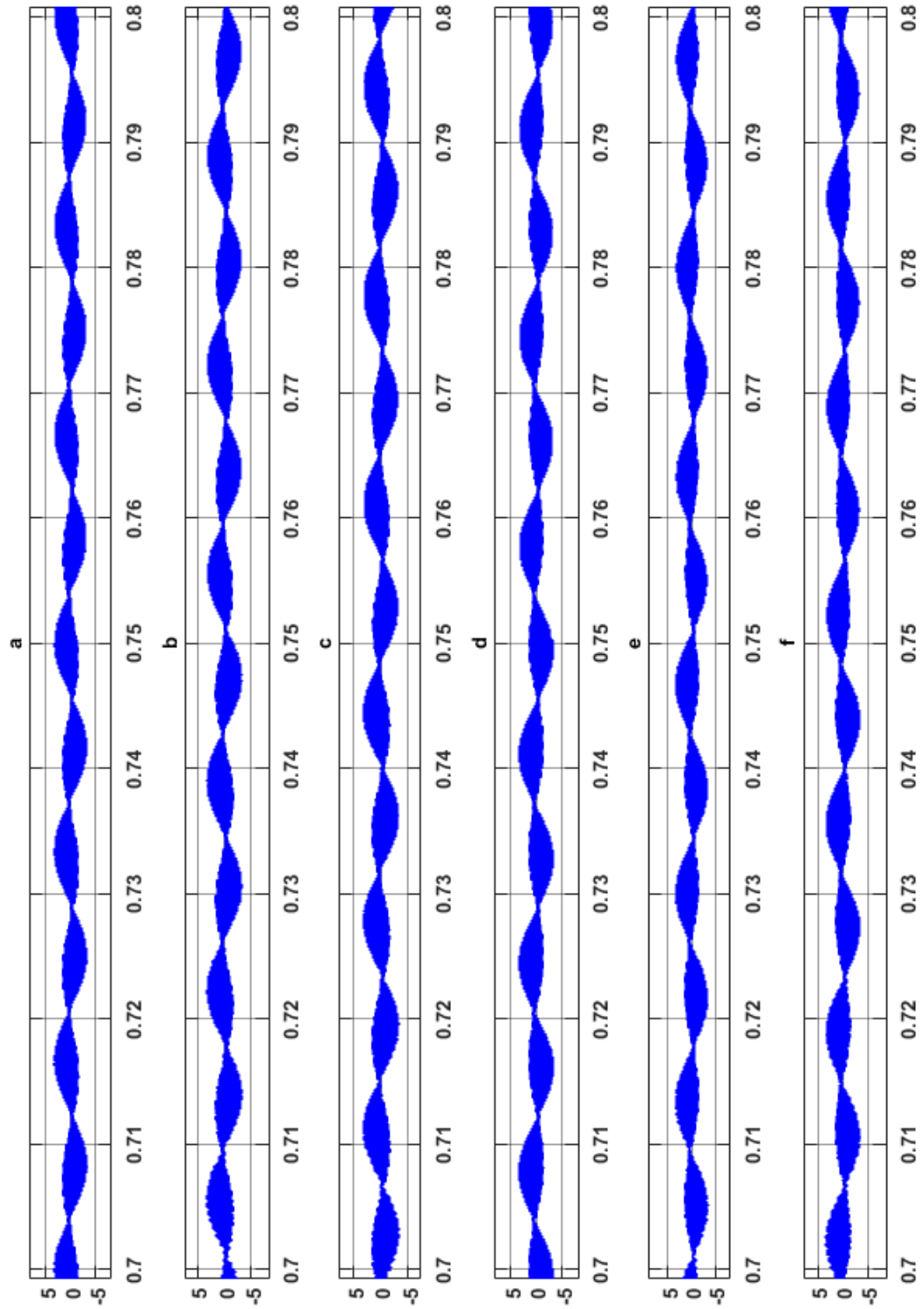


Figure 6-59: Center-Point-Currents

Figure 6-53 displays the input capacitor voltages for each phase. It may be observed that each input capacitor voltage has a rms voltage of $60V_{line\text{-}line}$ applied across its terminals. This voltage division demonstrates the access to the mid-point of input voltage across each phase of CPC PLC. Similar voltage division may also noticed from Figure 6-54, where each output capacitor voltage has a rms value of $60V_{line\text{-}line}$ applied across its terminals. This ensures access to the center-point voltage of the output load voltage. Also, it may be seen that due to step increase in load by 10% at 0.75sec, input capacitor voltages remain steady at $60V_{line\text{-}line}$. But due to command following reference of the controller, output capacitor voltages get back to half of the desired output voltage within one cycle. The voltages across the buck-boost inductors in CPC PLC converter topology have been presented in Figure 6-55. The voltage across each inductor also has a rms voltage of $60V_{line\text{-}line}$. The current through the buck-boost inductors have also been captured in Figure 6-56. But step change in output load reflects in the inductor current as well, where it settles to a new value according to load demand. The duty cycle waveforms are shown in Figure 6-57. Since the input and output capacitor voltages are balanced, the peak voltage stress across the switches are equal to half the summation of input and output voltage, which is equal to a peak voltage of $170V_{ac}$. The voltage stress waveforms are displayed in Figure 6-58. The current flowing through the center-point connections in the input side as well as the output side are shown in Figure 6-59.

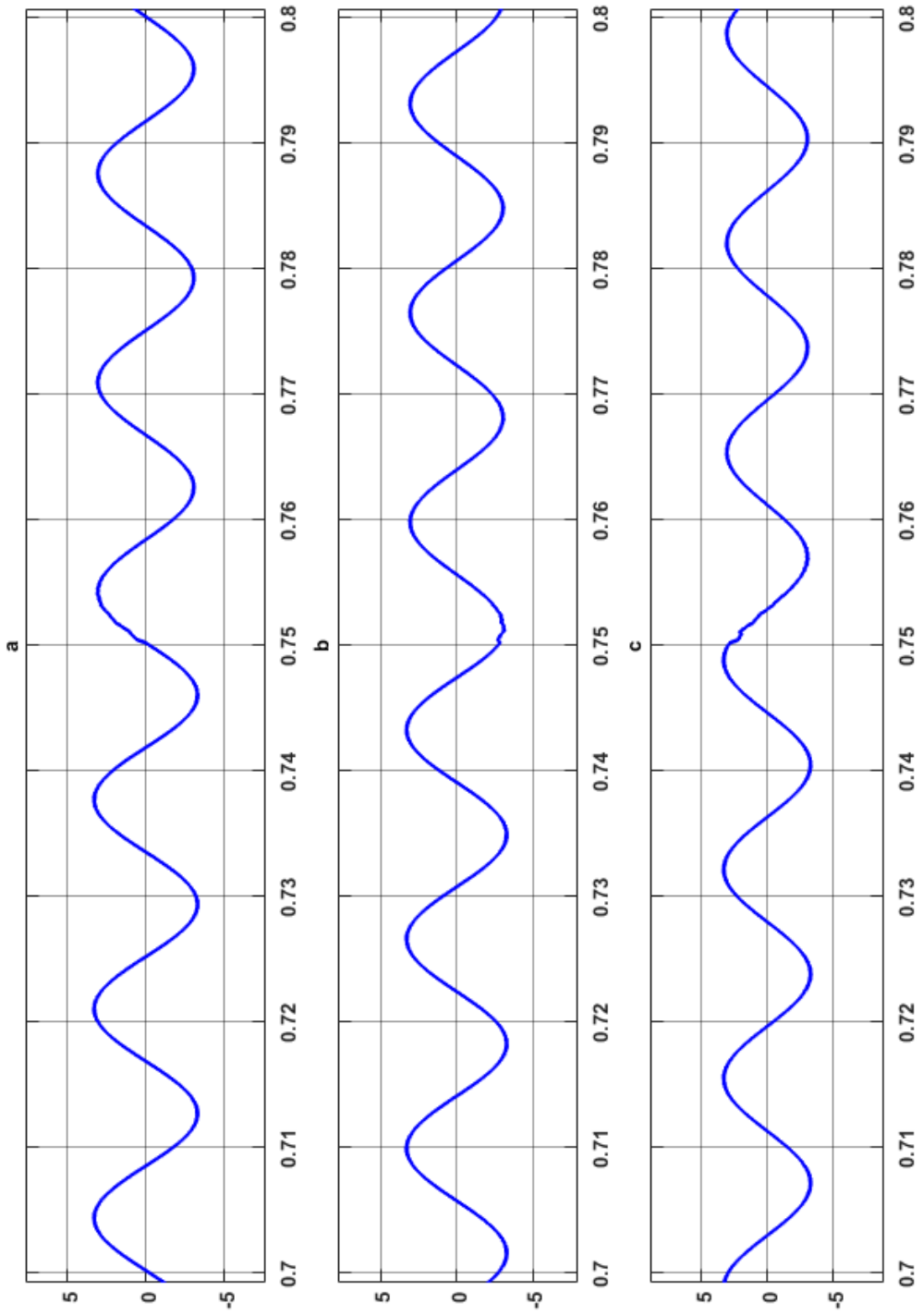


Figure 6-60: Input source currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

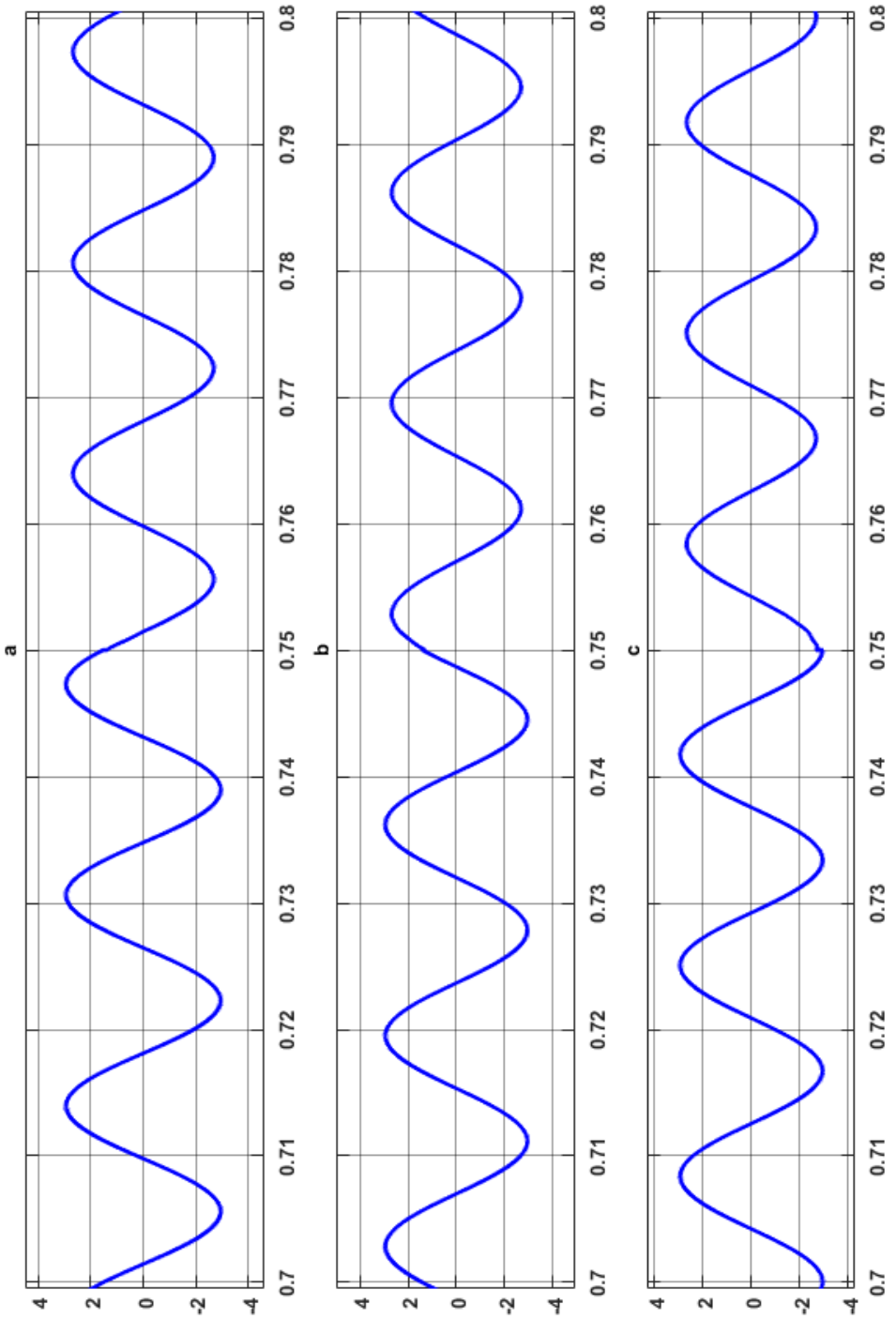


Figure 6-61: Output load currents of 3-Ø CPC PLC (a) Phase-a line-line current, (b) Phase-b line-line current, and (c) Phase-c line-line current.

It may be seen from Figure 6-60 and Figure 6-61, with step increase in output load at 0.75seconds, the input line current gets decreased by 10% to compensate for the increase in output load, as the controller modulates the duty cycle to regulate constant desired line output voltage. The output line current also gets decreased by 10% with the step increase in output load by 10% at 0.75seconds.

This chapter verifies the operation methodology of CPC PLC and its dynamic performance under varying line voltage and output load conditions. This also demonstrates the command following performance of CPC PLC to regulate the desired output voltage at the customer side.

7. Chapter Seven: Experimental Setup

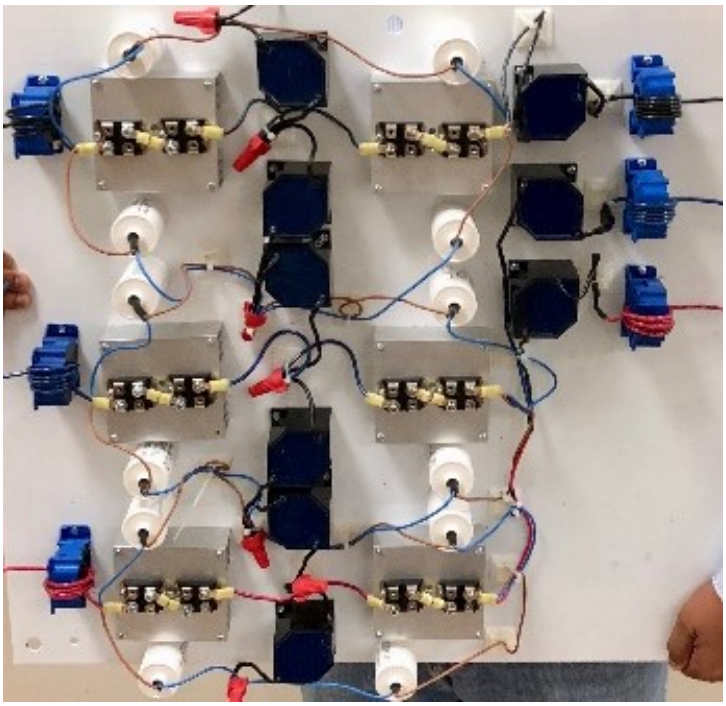


Figure 7-1: Picture of the experimental setup for Center-Point-Clamped Power Line Conditioner (CPC PLC)

A picture of the experimental setup for 3-Ø CPC PLC is shown in Figure 7-1. It may be seen that the components used to build this hardware has already been discussed in Chapter-4.

7.1. Single-Phase Hardware Results

A photograph of bench prototype of the proposed center-point clamped ac-ac power line conditioner, rated for single phase (phase-neutral voltage v_{in} =120V$_{\text{line-neutral}}$) of 208V line-line, 0.5 kW, has been shown in Figure 7-2.

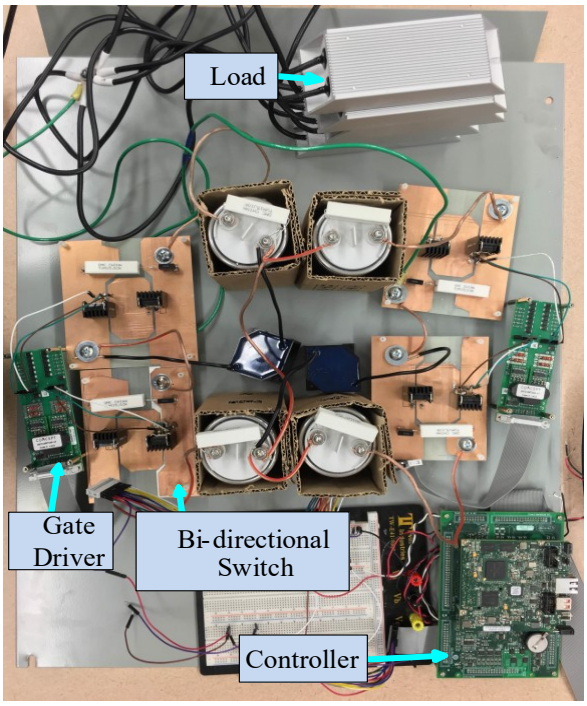


Figure 7-2: Photograph of the experimental setup in laboratory.

As may be seen from Figure 7-2, the experimental setup consists of four bi-directional IGBT (IRGP4072DPbF) based switches which are built on a PCB, rated at 300V and 50A. The gate drive logic is generated using NI LabVIEW FPGA and fed into the gate driver using NI General Purpose Inverter Controller (GPIC) having a base clock frequency of 40 MHz. An isolated IGBT gate driver from CONCEPT Technologies is used to drive the switches. The output voltage is stepped down using a transformer and sensed by NI GPIC for feedback control. The GPIC sensed output voltage is then fed into a single-phase Phase

Locked Loop (PLL) LabVIEW VI to determine rms value of the output voltage. The experimental results displayed here have been generated using Tektronix MSO-3014 Oscilloscope. The experimental parameters for the single phase CPC PLC have been given in Table III.

Table 7-1: EXPERIMENTAL PARAMETERS OF CENTER-POINT-CLAMPED POWER LINE CONDITIONER

Parameter	Description	Values (Units)
$P_{3-\emptyset}$	Three phase power	1.5 kW
$v_{line-line}$	Line-line voltage	208 V
$v_{line-neutral}$	Phase voltage	120 V
$Ci1, Ci2$	Input filter capacitors	100 µF
$Lp1, Lp2$	Buck-boost inductors	167 µH
$Co1, Co2$	Output filter capacitor	100 µF

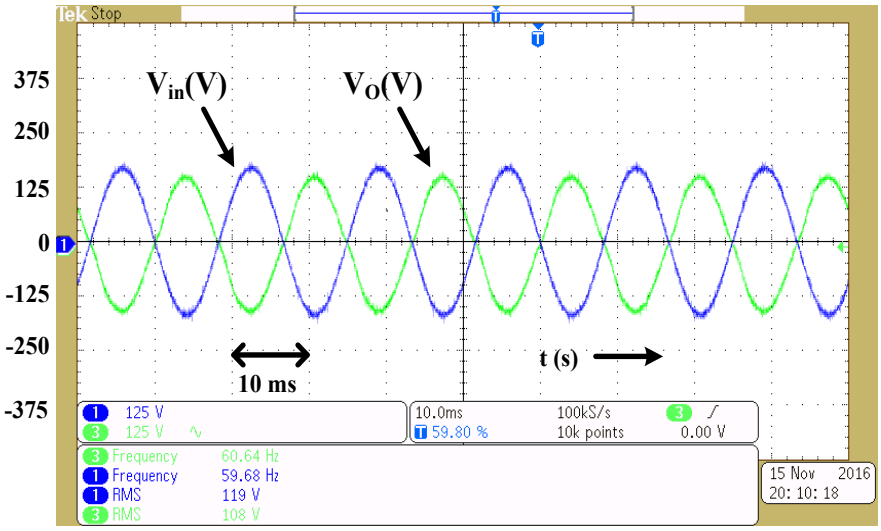


Figure 7-3: Input Voltage (blue) and Output Voltage (green) waveforms of the proposed Power Line Conditioner.

As it may be seen from Figure 7-3, the center-point-clamped power line conditioner is being operated about a duty cycle of 0.5, which ensures input voltage level is same as the output voltage level. Also, it may be observed that the input voltage is 180° out of phase

with the output voltage, which is a typical characteristic of ac-ac buck-boost converter topology.

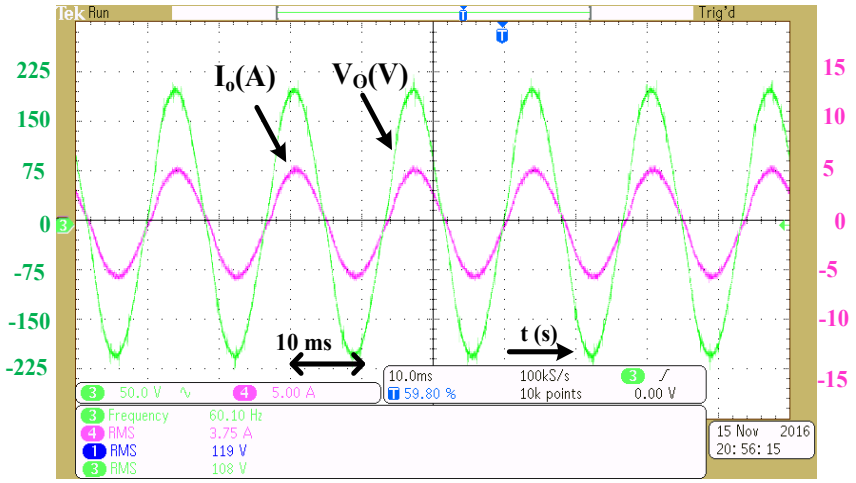


Figure 7-4: Output Voltage (green) and Output Current (pink) waveforms of the proposed Power Line Conditioner.

Since a purely resistive load has been applied on the output side of the proposed power line conditioner, the output voltage (120V rms) and current (4A rms) are in phase with each other as displayed in Figure 7-4.

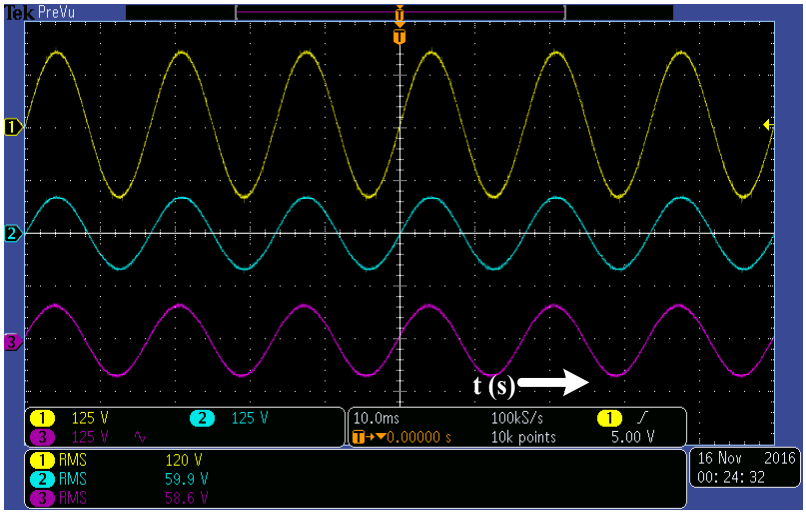


Figure 7-5: Input Voltage (yellow), Input Capacitor 1 Voltage (blue) and Input Capacitor 2 Voltage (pink) waveforms of the proposed Power Line Conditioner.

It may be noticed from Figure 7-5, that the input voltage is equally divided among the two input capacitors 1 and 2. This ensures that the voltage at the midpoint of the two input capacitors is clamped to the center-point of the input voltage. Similarly, the voltage across the output capacitors are also clamped to the center-point of the output voltage. Thus, this center-point-clamping technique ensures that the voltage stress across each bidirectional switch is equal to $\frac{v_{in}+ v_o}{2}$. This reduction in voltage stress may be confirmed from Figure 7-6.

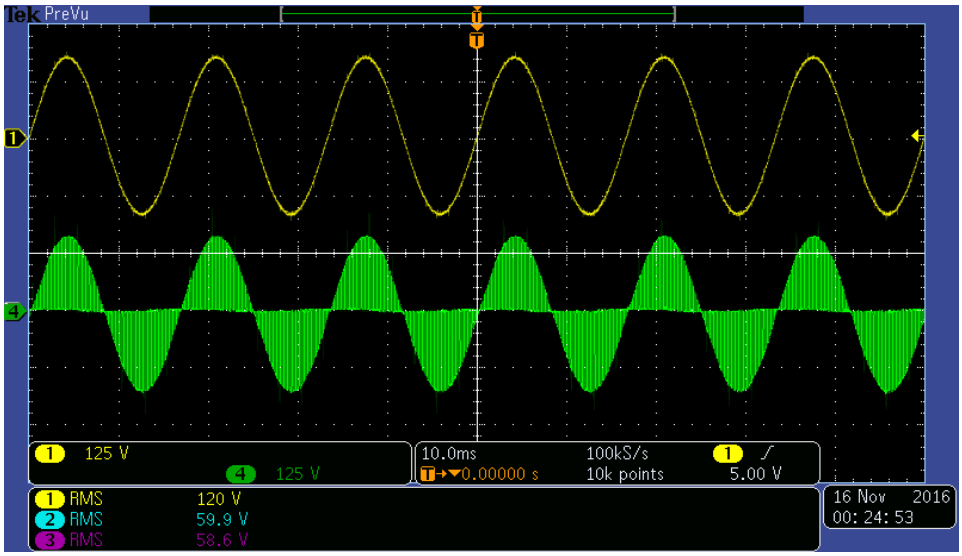


Figure 7-6: Input Voltage (yellow) and Voltage Stress on a bi-directional switch (green) of Power Line Conditioner.

Furthermore, it may be seen from Figure 7-7 and Figure 7-8 that on either 10% step increase or decrease in line voltage from 120Vrms, the output voltage is regulated 120Vrms within a few fundamental cycles. This demonstrates the excellent command following performance of the designed feedback compensator for the proposed power line conditioner.

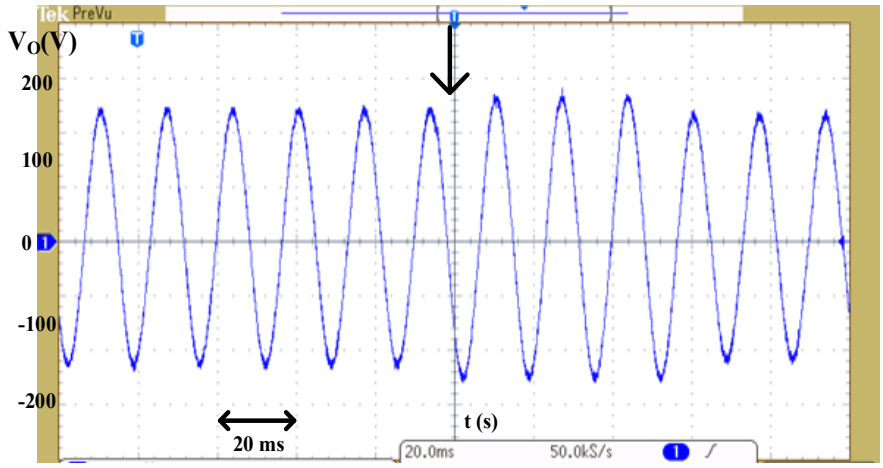


Figure 7-7: Line regulation: performance upon 10% step increase in line voltage.

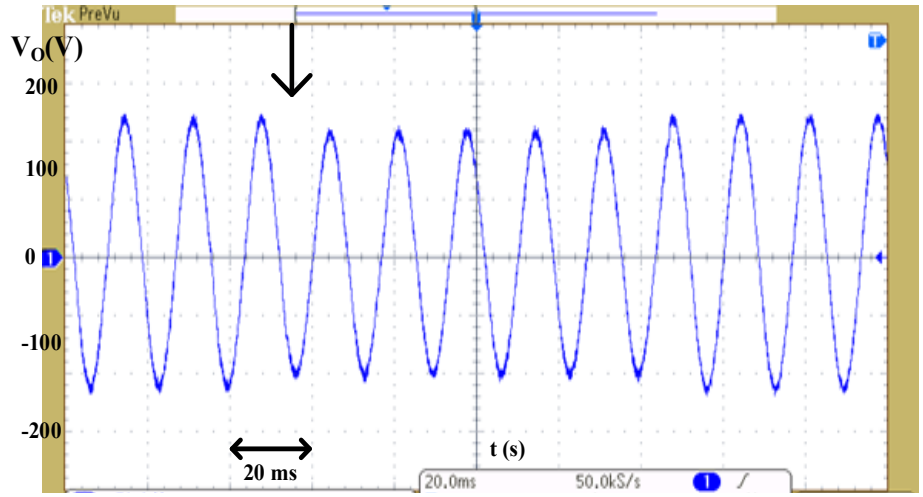


Figure 7-8: Line regulation: performance upon 10% step decrease in line voltage.

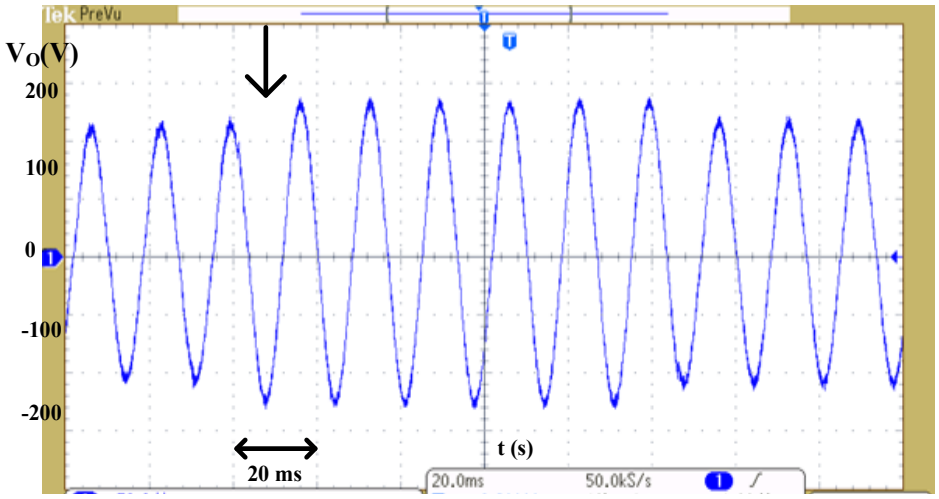


Figure 7-9: Load regulation: performance upon step decrease in load current.

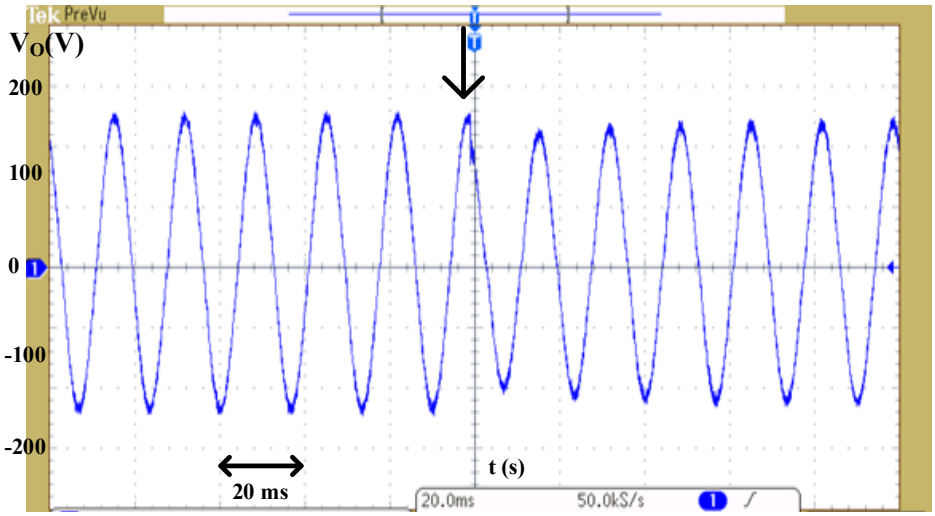


Figure 7-10: Load regulation: performance upon step increase in load current.

Similar behavior is seen in the load regulation performance results displayed in Figure 7-9 and Figure 7-10, where the line conditioner through duty ratio modulation controls the load voltage to a command reference voltage of 120Vrms. This demonstrates the excellent dynamic performance of the designed control scheme as well as efficacy of the proposed Center-Point-Clamped AC-AC Power Line Conditioner in mitigating issues like voltage sags, surges and flicker.

7.2. Three-phase Hardware Results

This sub-section discusses and presents the hardware set-up and the waveforms for the 3-Ø CPC PLC.

7.2.1. Power Stage Hardware Design

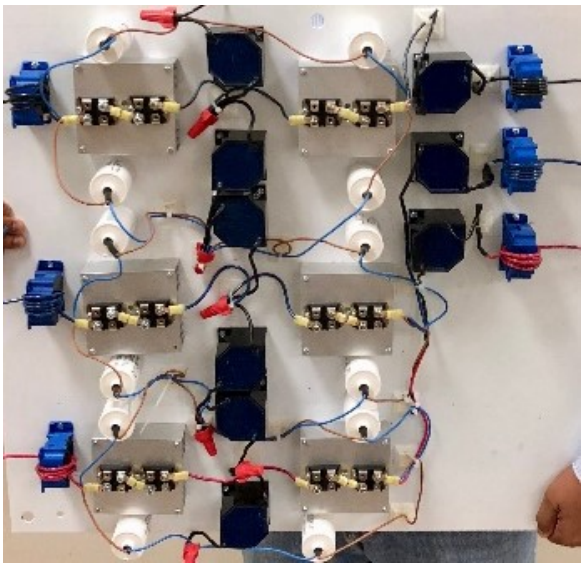


Figure 7-11: Picture of the experimental setup for Center-Point-Clamped Power Line Conditioner (CPC PLC)

A picture of the experimental setup for 3-Ø CPC PLC is shown in Figure 7-11. A detailed discussion of components selected to build the 3-Ø CPC PLC has been presented in Chapter-4.

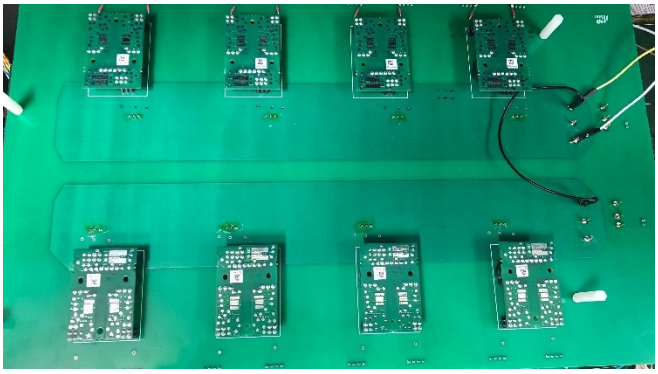


Figure 7-12: Picture of the Gate Drive Board setup

It may be seen from Figure 7-12 that the gate drive modules have been installed in a printed circuit board. The gate drive modules used for this prototype are from Power Integrations.

Figure 7-13: Picture of Gate drive module

Each of the gate drive modules, 2SC0108T2F1-17 can independently drive two IGBT switches. It is galvanically isolated with the following features [60]:

- Voltage blocking capability up to 1700V.
- Switching frequency up to 50 kHz.
- Regulated gate drive voltage of +15V/-8V
- Gate current capability up to +/- 8A
- 2x1 W output power which is supplied by an external power supply
- Protection features like supply undervoltage lockout, IGBT short circuit protection

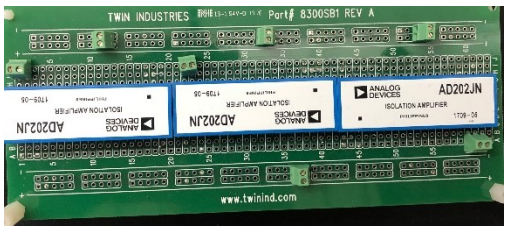


Figure 7-14: Picture of Sensing Circuit Board

The sensing circuit board has an isolation amplifier AD202JN from Analog Devices, which is a transformer coupled isolation amplifier. It consumes 75mW for one module, which is again supplied by an external power supply at a regulated supply voltage of 15V. The sensing input voltage is capable of handling up to +/- 2000 Vpeak and the sensing output can provide up to +/- 5Vpeak which may be tuned according to microcontroller specifications [61].

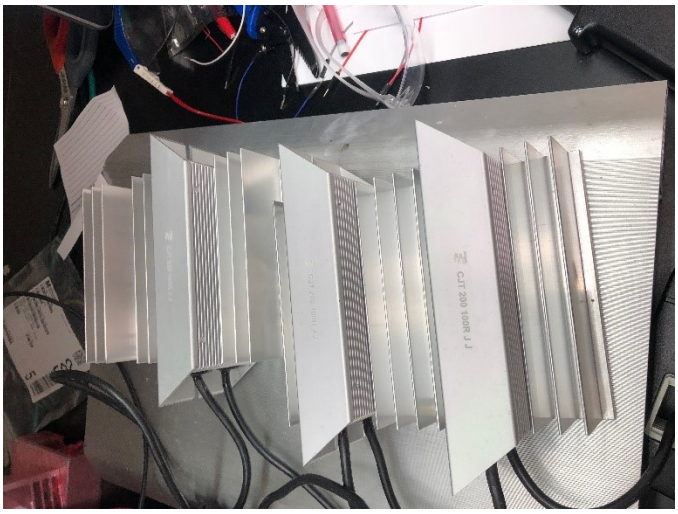


Figure 7-15: Picture of resistive load with heat sink

As may be seen from Figure 7-15, the three-phase load is connected in wye configuration. The load used for each line of the wye connection is purely resistive with a resistance of 100Ω.

7.2.2. Controller Algorithm Design in LabVIEW FPGA

Figure 7-16: Picture of NI-9606 microcontroller

As may be seen from Figure 7-16, NI-9606 microntroller has been used as the control platform for this protype. It is a 400MHz CPU, 512 MB DRAM, 512MB storage, Spartan-6 LX45 FPGA CompactRIO Single-Board Controller It requires 9-30Vdc power supply, which is provided by an external power supply. It has a capability of simultaneously sending up to 14 digital switching signals of 3.3V through its half-bridge digital output pins which are provided in an external NI-9683 board. It can also sense 16 ac analog inputs up to a peak of +/-10V simultaneously. The controller algorithm has been designed using NI-LabView FPGA. LabView FPGA is specifically designed as modular block schematic-based programming platform to support rapid intuitive control design.

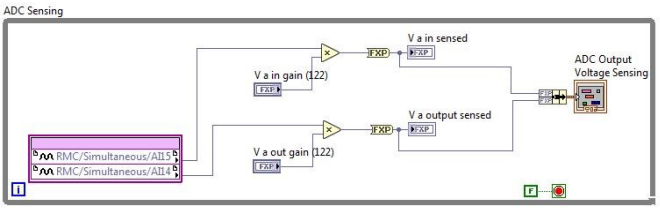


Figure 7-17: Picture of LabVIEW implementation of ADC Sensing loop

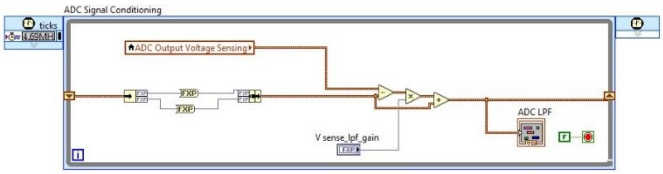


Figure 7-18: Picture of LabVIEW implementation of ADC Signal conditioning loop

As may be seen from Figure 7-17 and Figure 7-18, the output and the input voltage signal is sensed by the analog input channels of the NI-GPIC (General Purpose Inverter Controller) and then filtered to remove any high frequency signals. The filtered sensed signals are then passed through the phase locked loop to generate a unity amplitude signal in phase with the output voltage. The in-phase unity signal is then utilized to generate the desired voltage reference as may be seen in Figure 7-19 and Figure 7-20.

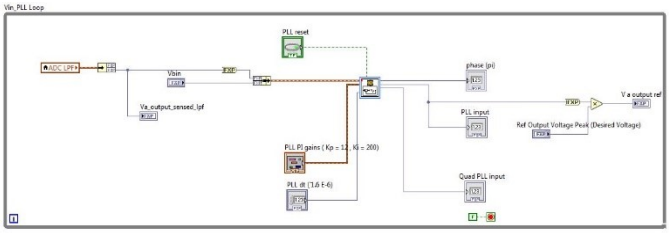


Figure 7-19: Picture of LabVIEW implementation of Phase Locked Loop

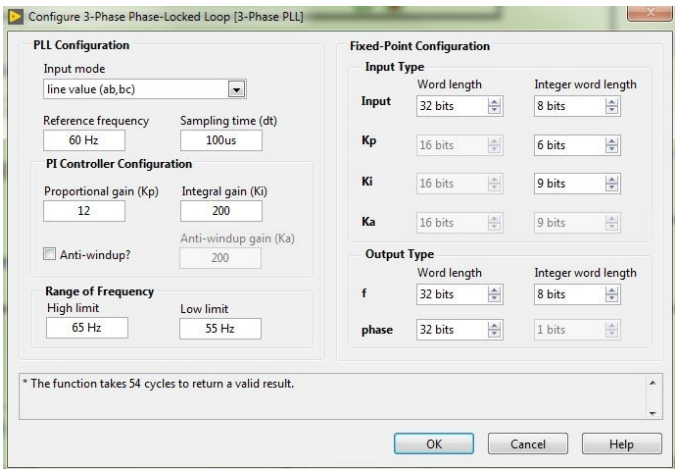


Figure 7-20: Picture of LabVIEW implementation of gains for PLL

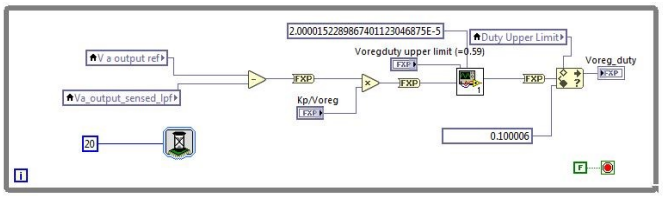


Figure 7-21: Picture of LabVIEW implementation of Controller for output voltage regulation

The controller for voltage regulation has been implemented to regulate the output voltage at desired voltage specifications, as displayed in Figure 7-21. The generated modulation ratio from the control loop is then passed on to the gate driver signal loop, shown in Figure 7-22, where it is compared to a triangle wave of 25kHz to generate the PWM signals. The PWM signals are then sent out through the half-bridge digital output pins of the microcontroller to respective gate dive modules.

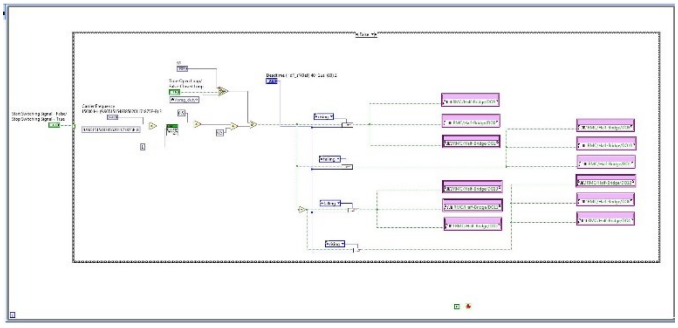


Figure 7-22: Picture of LabVIEW implementation of Gate Driver Signals

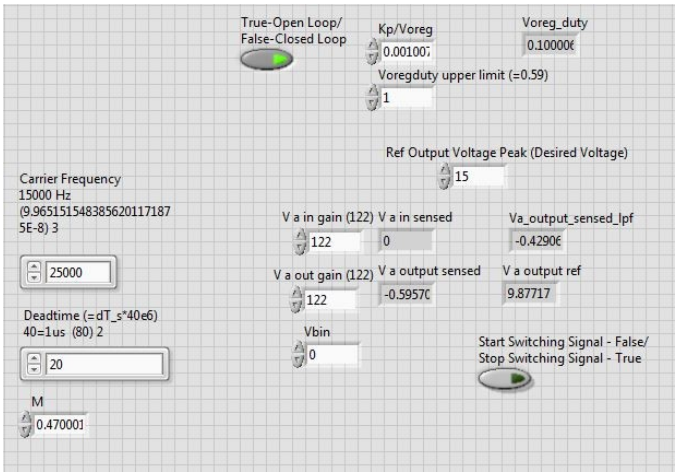


Figure 7-23: Picture of LabVIEW Front Panel as the user interface

The front panel of a LabVIEW program is the user interface which may used to command the controller to generate desired output voltage in real time. As may be seen from Figure 7-23, the program is designed to change the carrier frequency of the PWM signal to observe the performance of the designed converter in real time.

7.2.3. Experimental Waveforms

This sub-section presents the results from the prototype to demonstrate the functionality of presented three-phase CPC PLC. The Pulse-Width Modulation based gate drive signals for a duty ratio of 0.45 are shown in Figure 7-24. As may be seen, the gate drive outputs have a maximum of +15V and a minimum of -8V for driving the IGBT switches. The switches are operating at a frequency of 25 kHz.

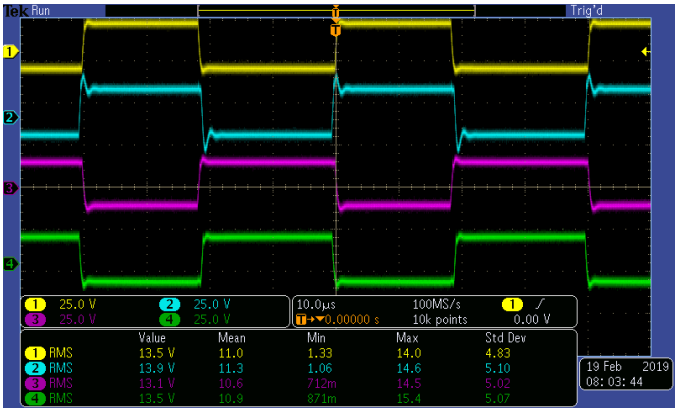


Figure 7-24: Gate Drive switching signals for duty ratio of 0.45

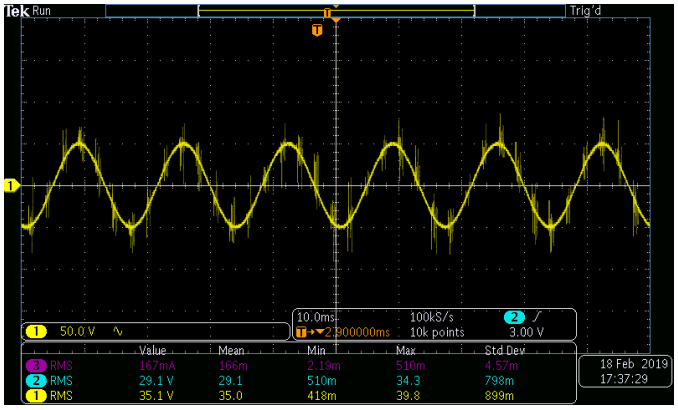


Figure 7-25: Input voltage signal for duty ratio of 0.45

The input voltage waveform for phase a is shown in Figure 7-25. It has a line-line rms value of 35V. It may be seen that the input voltage signal has a high frequency component which is an artifact of the switching phenomenon. The switching of the

IGBTs inject high frequency signal to the input voltage which may be attenuated by the introduction of a series inductance in each phase of the converter as a low-pass filter in the input side. The output voltage is shown in Figure 7-26, which has a line-line rms value of 29V, which demonstrates voltage buck capability of the CPC PLC.

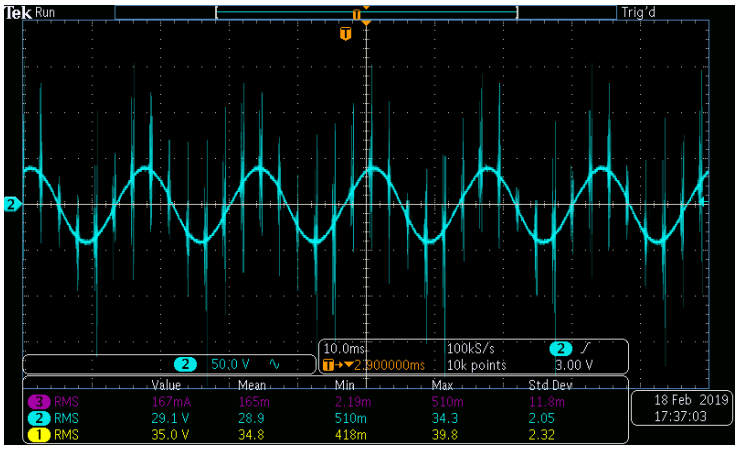


Figure 7-26: Output voltage signal for duty ratio of 0.45

The switch voltage stress for each bi-directional switch is shown in Figure 7-27. It may be noted that the peak of the voltage stress is equal to the peak of the summation of the input and output voltage.

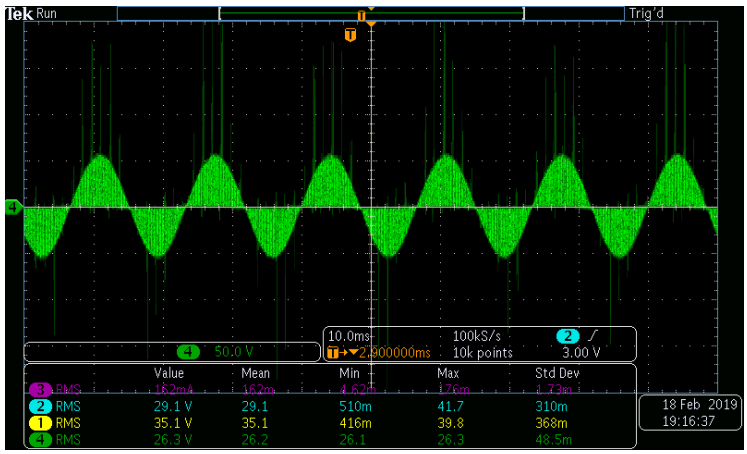


Figure 7-27: Switch voltage stress for V_{in} = 35V, V_{out} = 29V

The output current waveforms for the phase a of the three-phase load is shown in Figure 7-28. It has a line-line rms value of 0.16 A.

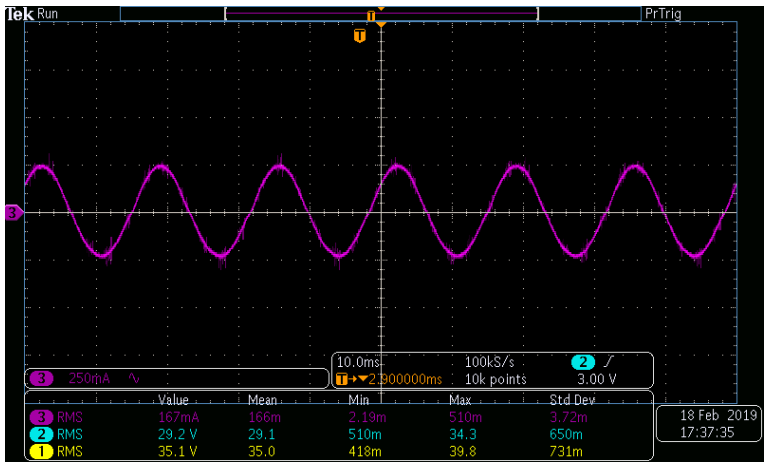


Figure 7-28: Output current for V_{out} = 29 V, V_{in}=35V, D=0.45

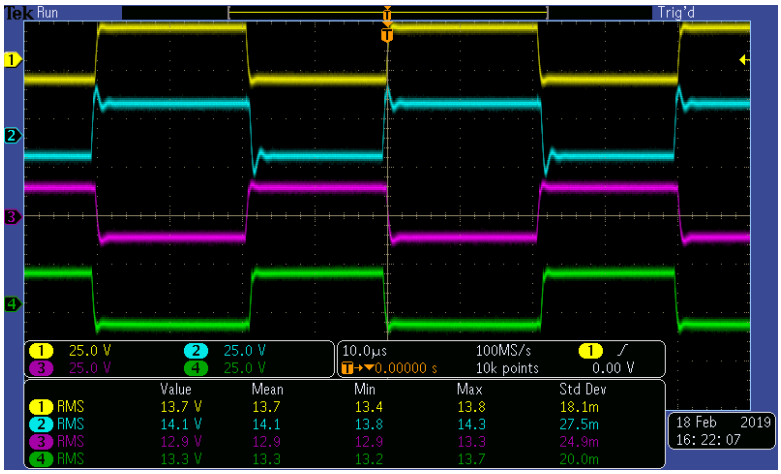


Figure 7-29: Gate Drive switching signals for duty ratio of 0.50

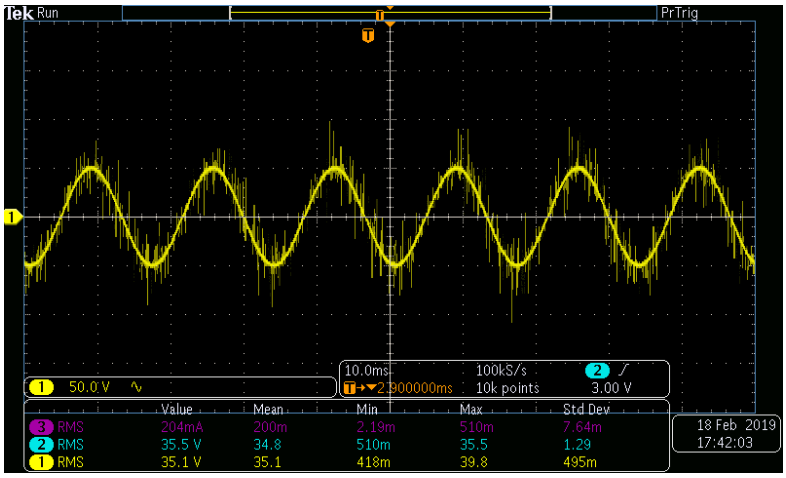


Figure 7-30: Input voltage signal for duty ratio of 0.50

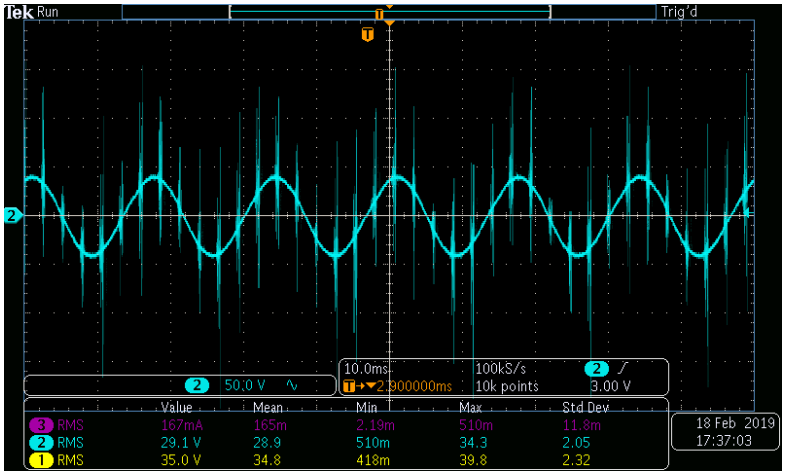


Figure 7-31: Output voltage signal for duty ratio of 0.50

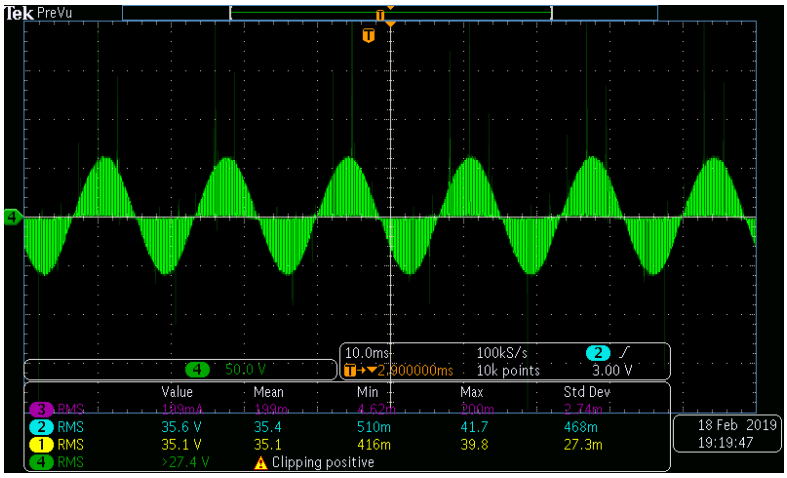


Figure 7-32: Switch voltage stress for V_{in} = 35V, V_{out} = 35V

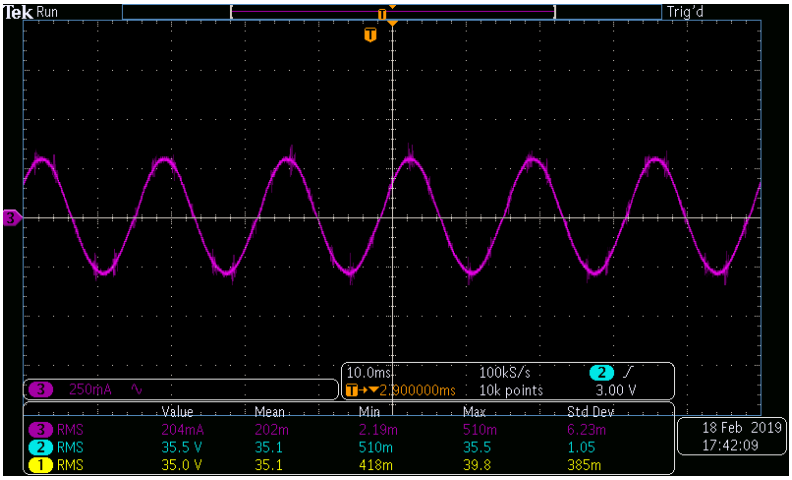


Figure 7-33: Output Current for V_{out} = 35 V, V_{in}=35V, D=0.50

The phase-a waveforms for gate drive switching signals, input voltage, output voltage, switch voltage stress and output current for a duty ratio operation of 0.50 has been displayed in Figure 7-29, Figure 7-30, Figure 7-31, Figure 7-32, and Figure 7-33 respectively. It demonstrates the line regulation capability of the CPC PLC, where the input voltage is equivalent to the output voltage of the converter. It may also be seen that in this case of operation, the peak of the voltage stress across each bi-directional switch is equal to the summation of the peak of input and output voltage.

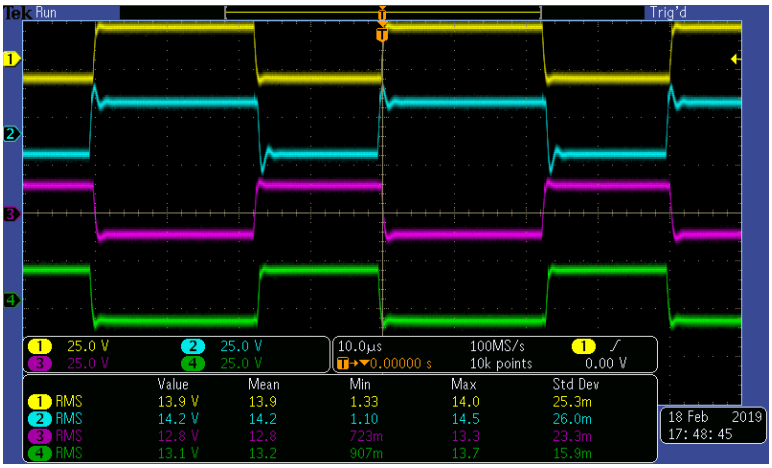


Figure 7-34: Gate Drive switching signals for duty ratio of 0.55

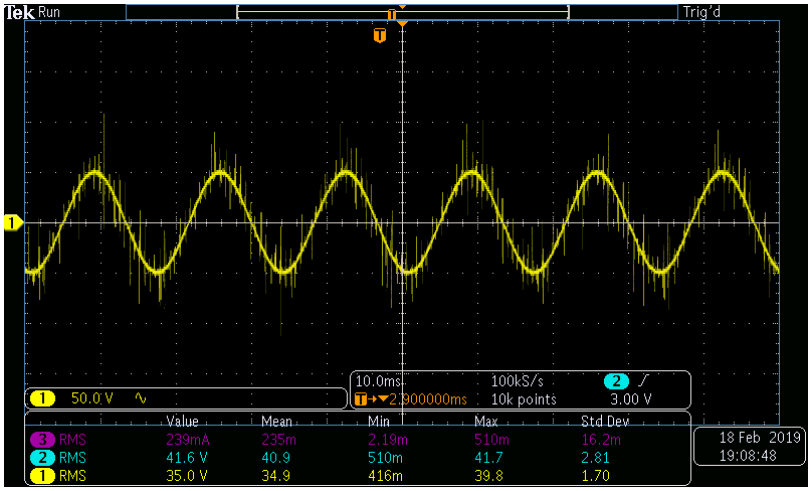


Figure 7-35: Input voltage signal for duty ratio of 0.55

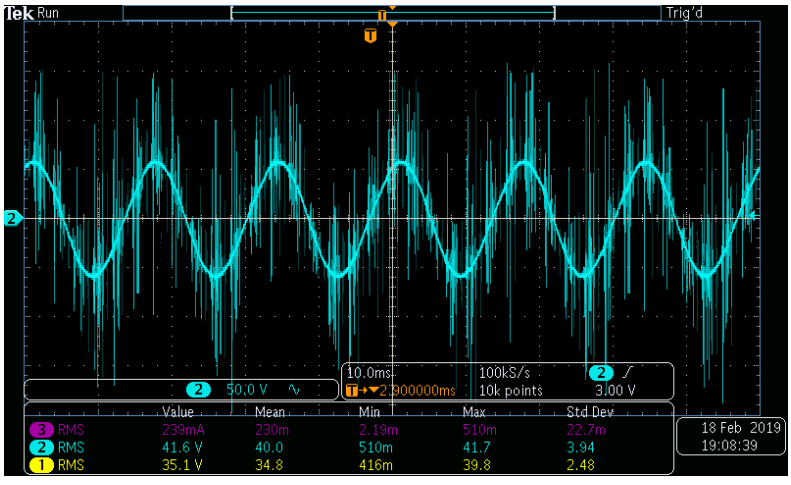


Figure 7-36: Output voltage signal for duty ratio of 0.55

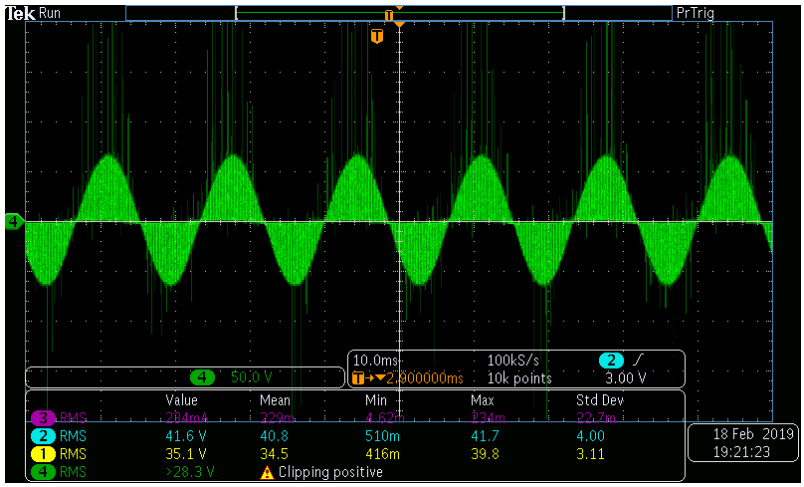


Figure 7-37: Switch voltage stress for V_{in} = 35V, V_{out} = 41V

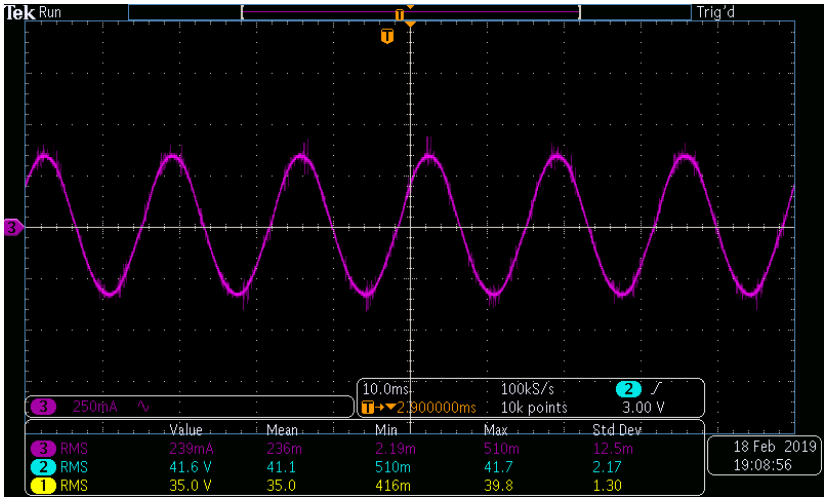


Figure 7-38: Output current for V_{out} = 41 V, V_{in}=35V, D=0.55

The phase-a waveforms for gate drive switching signals, input voltage, output voltage, switch voltage stress and output current for a duty ratio operation of 0.50 has been displayed in Figure 7-34, Figure 7-35, Figure 7-36, Figure 7-37 and Figure 7-38 respectively. It demonstrates the voltage boosting capability of the CPC PLC, where the input voltage is equivalent to the output voltage of the converter. It may also be seen that in this case of operation, the peak of the voltage stress across each bi-directional switch is equal to the summation of the peak of input and output voltage.

8. Chapter Eight: Capability Verification of CPC PLC

It has been presented in the dissertation that 3-Ø CPC PLC may be used to mitigate grid voltage sag and swells up to 10%. It may also be stated that the percentage of voltage regulation is also dependent on the design of the passive components required to build the CPC PLC. As it has been already discussed that the design has been performed keeping in mind the availability of components for the experimental verification of 3-Ø CPC PLC. This chapter discusses the verification of capability of 3-Ø CPC PLC to mitigate voltage sags up to 90% and the design methodology of the passive components to achieve that capability.

8.1. Design of Passive Components of CPC PLC for 4.16 kV application

The design constraints and equations to derive the values of capacitance and inductance has already been derived and presented in Chapter 4 and Chapter 5. This section will consider those equations and provide the values for inductance and capacitance for varying Voltage Sag percentages.

Rewriting the Inductance Design Equation 4.35 from Chapter-4, we have,

	$L = \frac{v_{in}}{2}.DT_{sw}.\frac{1}{\Delta i_{L1_a}}$	8.1

Now, Considering the design for 4.16 kV utility distribution scale voltage, which is the targeted design application for 3-Ø CPC PLC, the tabulated values for the fixed parameters are shown in Table 8-1.

Table 8-1: Fixed inductor design parameters for 3-Ø CPC PLC

Parameters	Values
v_{out}	4.16 kV
F_{sw}	20 kHz
$P_{3-\emptyset}$	10 kVA
Δi_{L1_a}	10 % of load current

The equation for Duty Cycle has already been derived as

$$D = \frac{v_{out}}{v_{out} + v_{in}} \quad (8.2)$$

Substituting the fixed design parameters from Table 8-1 and equation (8.1) into equation (8.2), we have,

$$L = \frac{v_{in}}{2} \cdot \frac{v_{out}}{(v_{out} + v_{in})} \cdot \frac{1}{F_{sw}} \cdot \frac{1}{\Delta i_{L1_a}} \quad (8.3)$$

This equation (8.3) gives us a relationship that will allows us to determine the value of inductance required to achieve 4.16 kV voltage load regulation irrespective of input voltage variation.

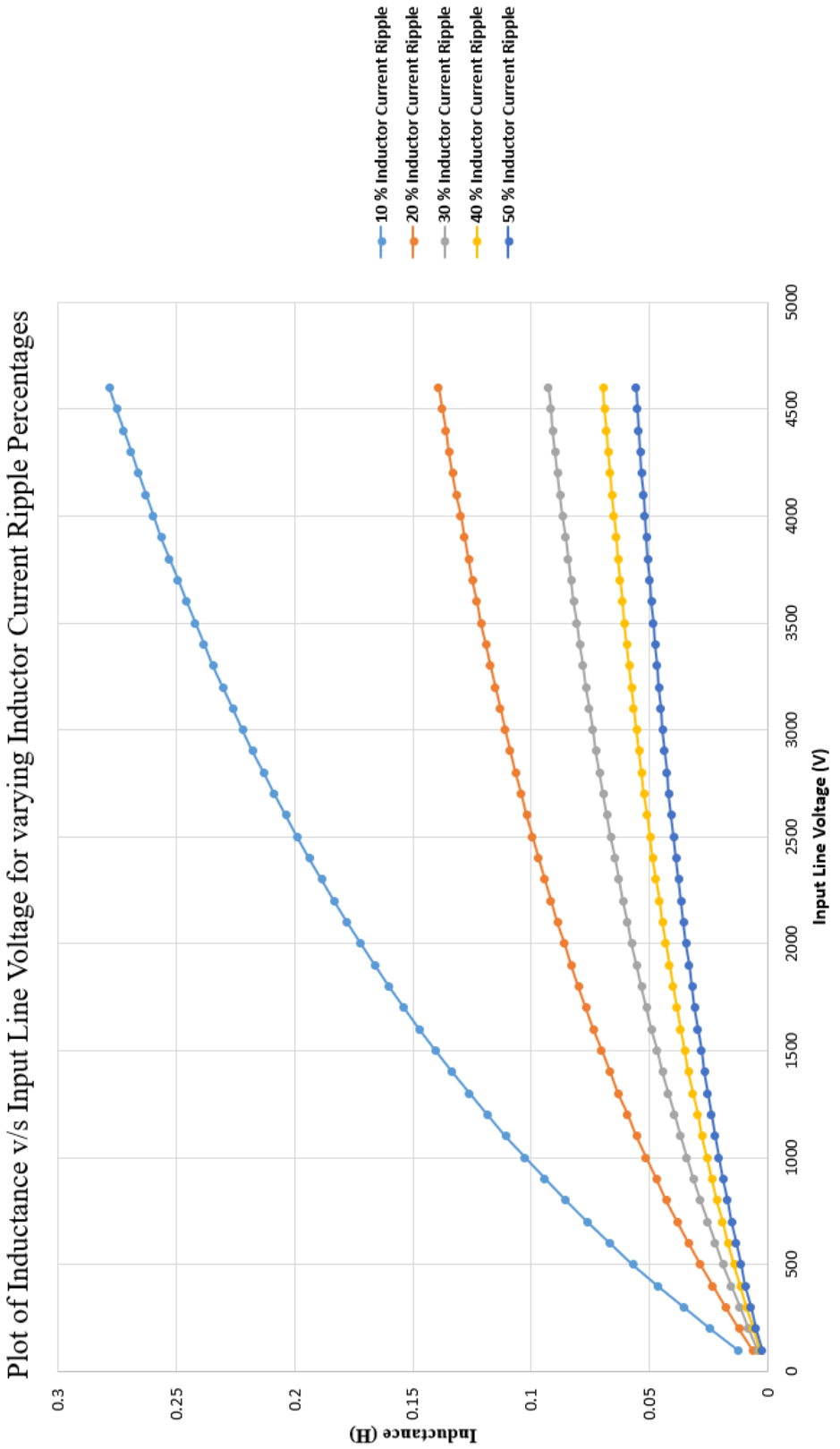


Figure 8-1: Plot of inductance value (H) versus input line voltage (V) for various percentages of inductor current ripple.

It may be seen from Figure 8-1, that the inductance value is proportional to the increase in input line voltage. It may also be observed that with increase in inductor current ripple, the inductance value decreases for a given input line voltage.

Similarly, the input and output capacitor design equations (4.41) and (4.45) as may be rewritten from Chapter 4 as follows:

	$C_{in1} = i_{in}.(1-D).T_{sw}.\frac{1}{\Delta v_{Ci1_a}}$	8.4
	$C_{out1} = i_{out}.(1-D).T_{sw}.\frac{1}{\Delta v_{Co1_a}}$	8.5

Table 8-2: Fixed capacitor design parameters for 3-Ø CPC PLC

Parameters	Values
v_{out}	4.16 kV
F_{sw}	20 kHz
$P_{3-Ø}$	10 kVA
Δv_{Ci1_a}	10 % of input capacitor voltage
Δv_{Ci1_a}	10 % of input capacitor voltage

Using the values obtained from Table 8-1, the equations (8.4) and (8.5) may be rewritten as follows:

	$C_{in1} = i_{in}.\left(1-\frac{v_{out}}{(v_{out}+v_{in})}\right).\frac{1}{F_{sw}}.\frac{1}{\Delta v_{Ci1_a}}$	8.4
	$C_{out1} = i_{out}.\left(1-\frac{v_{out}}{(v_{out}+v_{in})}\right).\frac{1}{F_{sw}}.\frac{1}{\Delta v_{Co1_a}}$	8.5

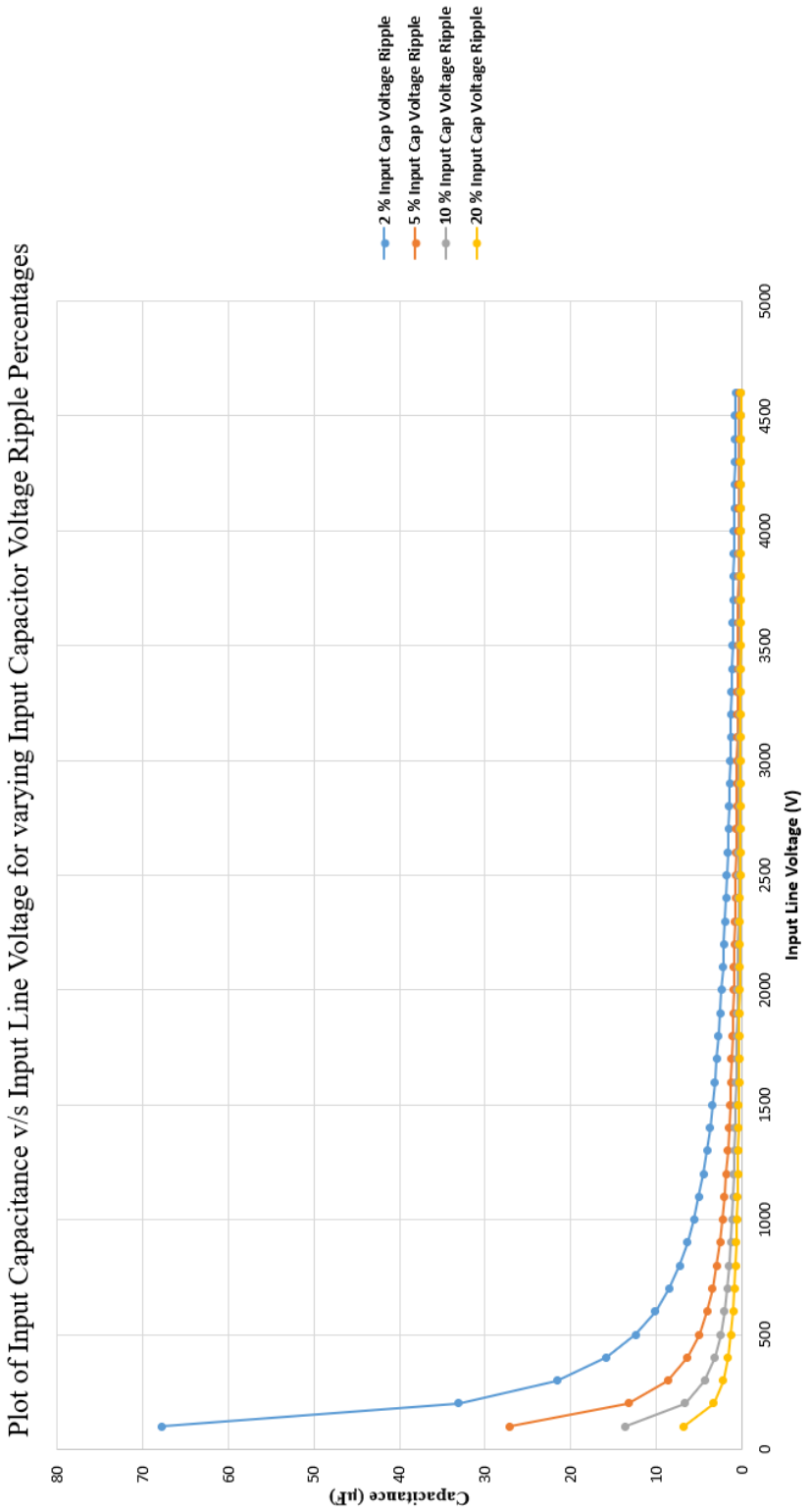


Figure 8-2: Plot of input capacitance value (µF) versus input line voltage (V) for various percentages of capacitor voltage ripple.

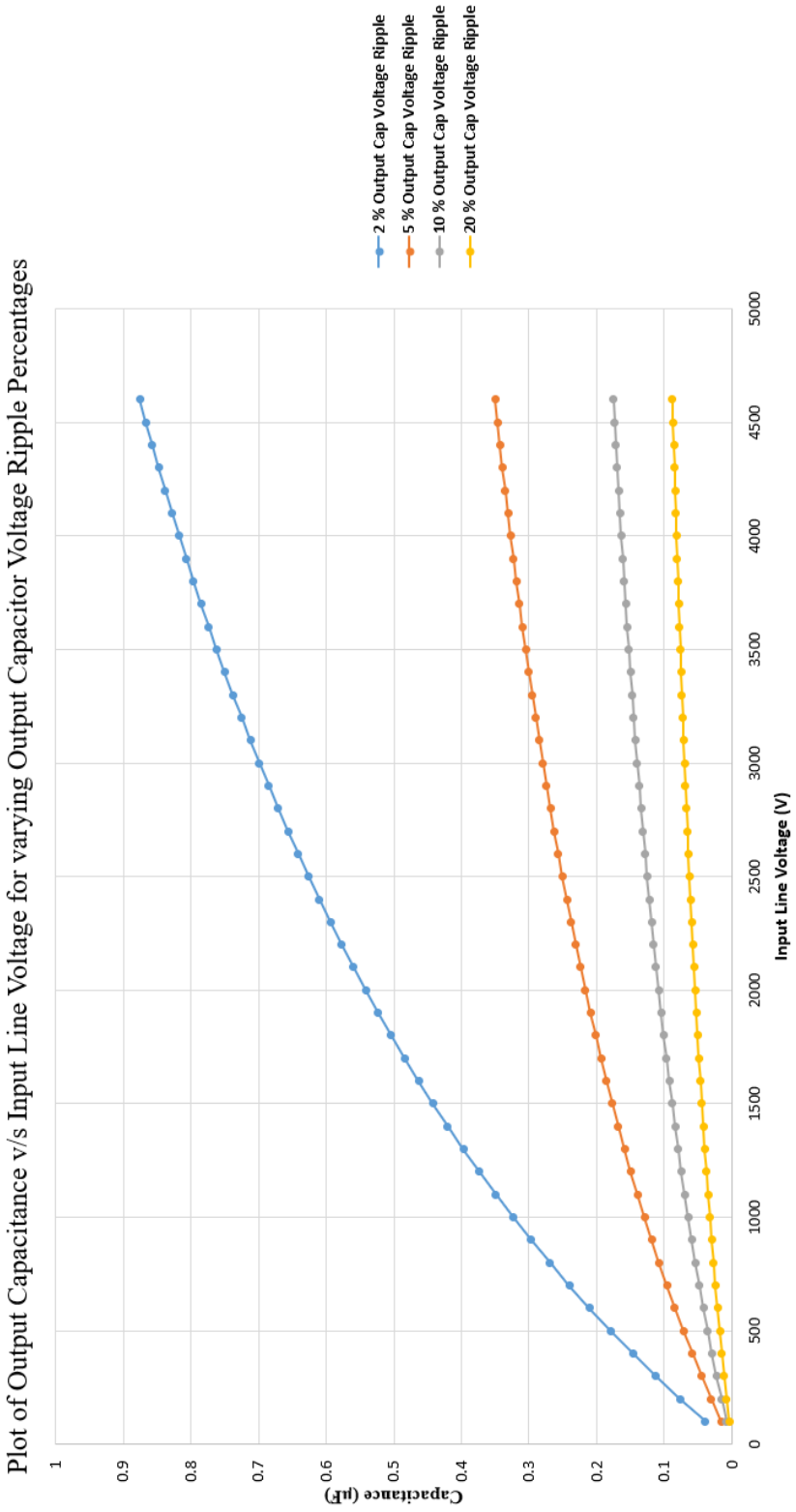


Figure 8-3: Plot of output capacitance value (μF) versus input line voltage (V) for various percentages of capacitor voltage ripple.

It may be noticed from Figure 8-2 that with increase in input line voltage, the desired value of input capacitance decreases and for a given input line voltage, the input capacitance value decreases with increase in percentage of capacitor voltage ripple.

Lastly, Figure 8-3 shows that the desired value of output capacitance increase with increase in input line voltage, but for a given input line voltage, the output capacitance value decreases with increase in percentage of capacitor voltage ripple.

8.2. Performance of 4.16 kV Application CPC PLC model for Varying Voltage Sag

This section presents the closed loop results for CPC PLC model designed for 4.16 kV applications. In this 4.16 kV model for 3-Ø CPC PLC, the input voltage is dynamically reduced during simulation run-time to emulate a input grid voltage sag. The closed loop duty cycle control of the CPC PLC allows the control of the duty ratio in such a way that desired output load voltage may be achieved, irrespective of input voltage variation. The model has been tested for various percentages of rated grid voltage of 4.16 kV.

8.2.1. Grid Voltage Sag: 10 % of 4.16 kV

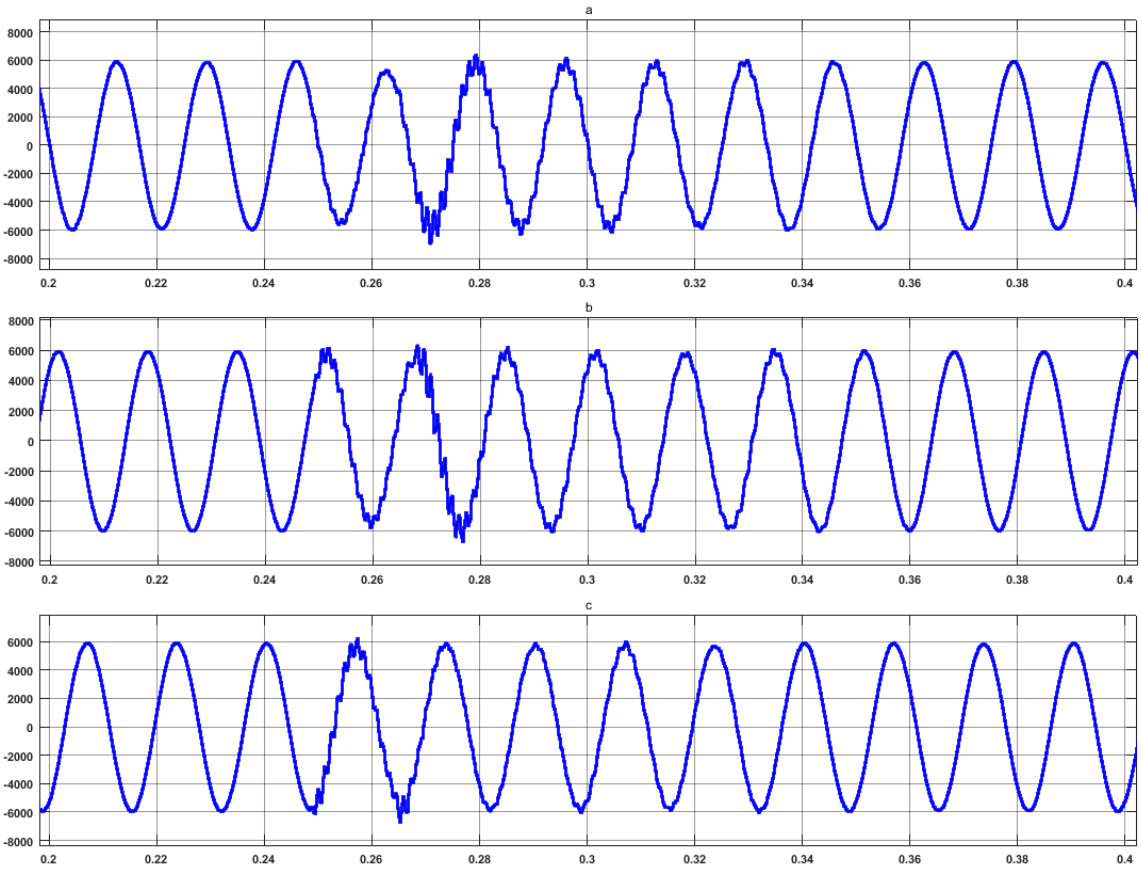


Figure 8-4: Input Grid Voltage for 10% sag introduced at 0.25 sec of simulation time

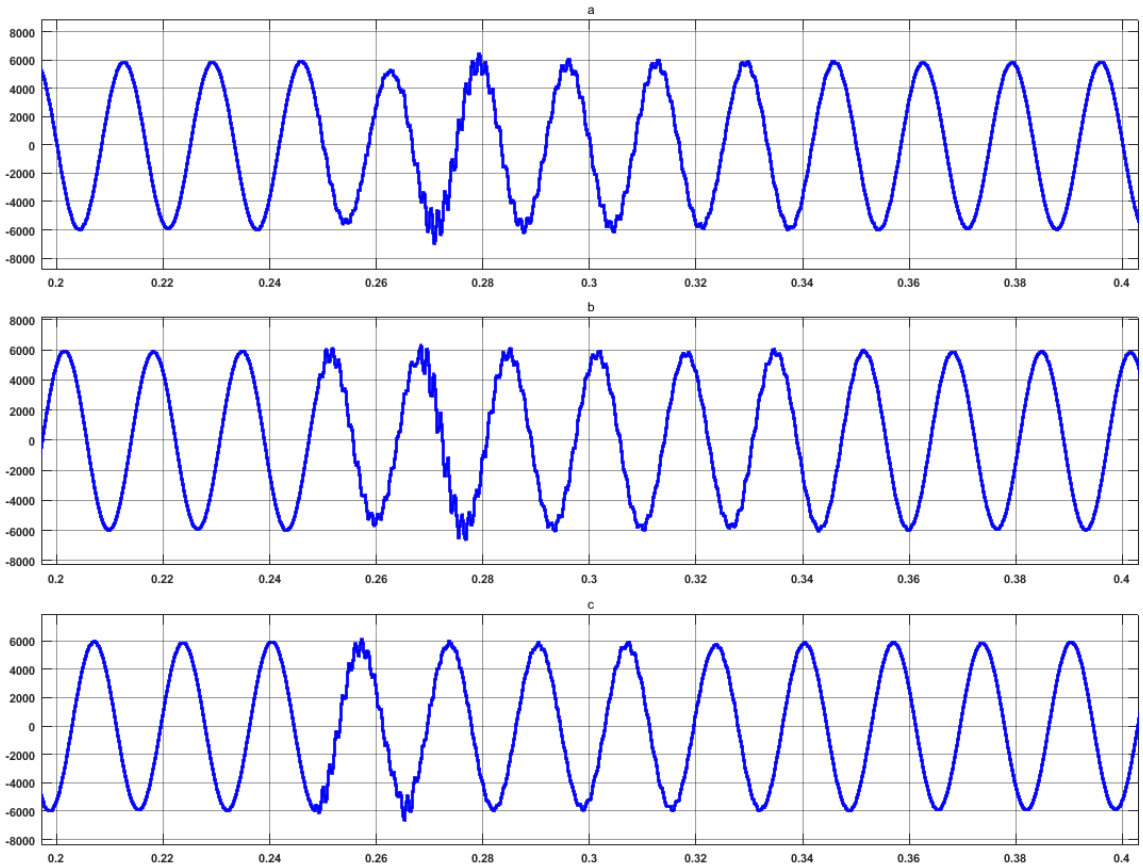


Figure 8-5: Output Load Voltage for 10% sag introduced at 0.25 sec of simulation time

It may be seen from Figure 8-4 and Figure 8-5, that with 10% sag in input grid voltage, the output load voltage may be regulated to desired value within one fundamental cycle. This verifies the line voltage regulation performance of CPC PLC at 10% input grid voltage sag.

8.2.2. Grid Voltage Sag: 20% of 4.16 kV

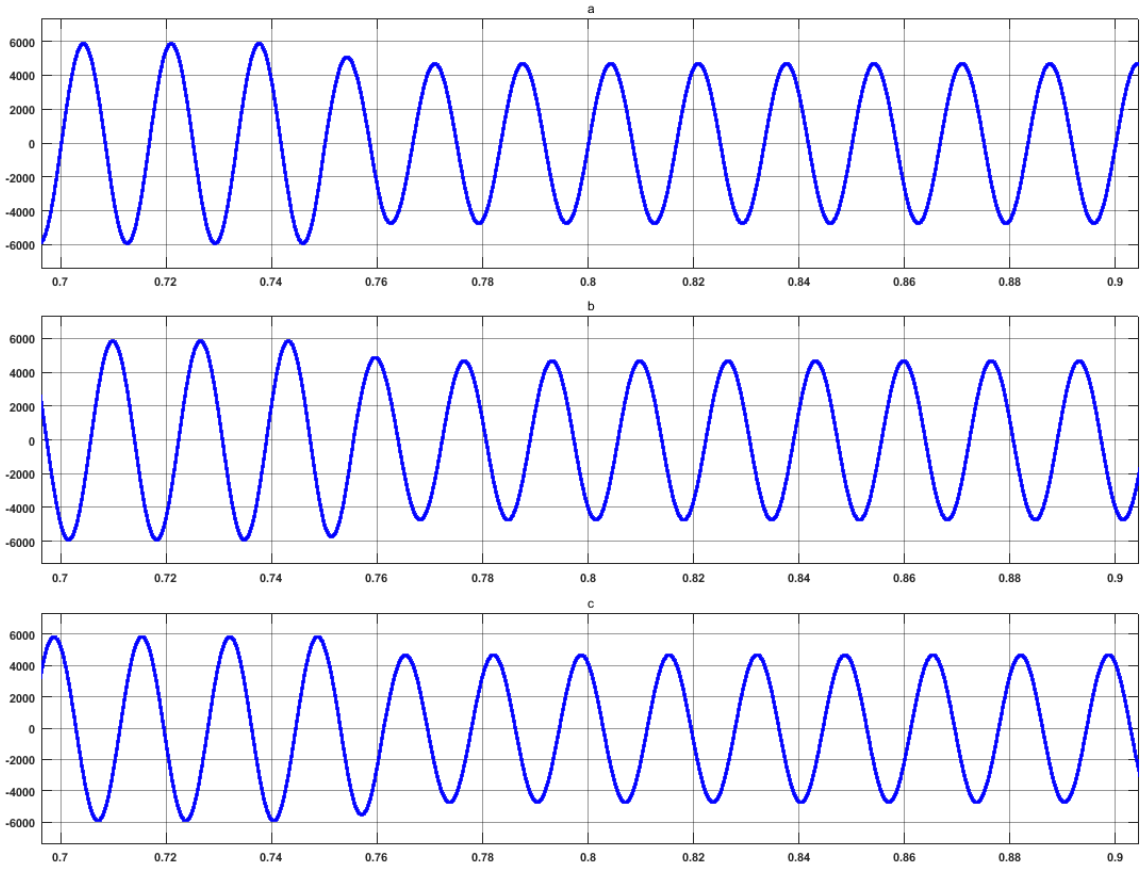


Figure 8-6: Input Grid Voltage for 20% sag introduced at 0.75 sec of simulation time

It may be observed from Figure 8-6, that a 20% voltage sag of the rated input grid voltage is introduced in the model at 0.75 seconds of simulation time. Figure 8-7 shows that the CPC PLC is able to regulate the output load voltage to desired reference value of 4.16 kV within a few fundamental cycles, irrespective of 20% sag in input grid voltage.

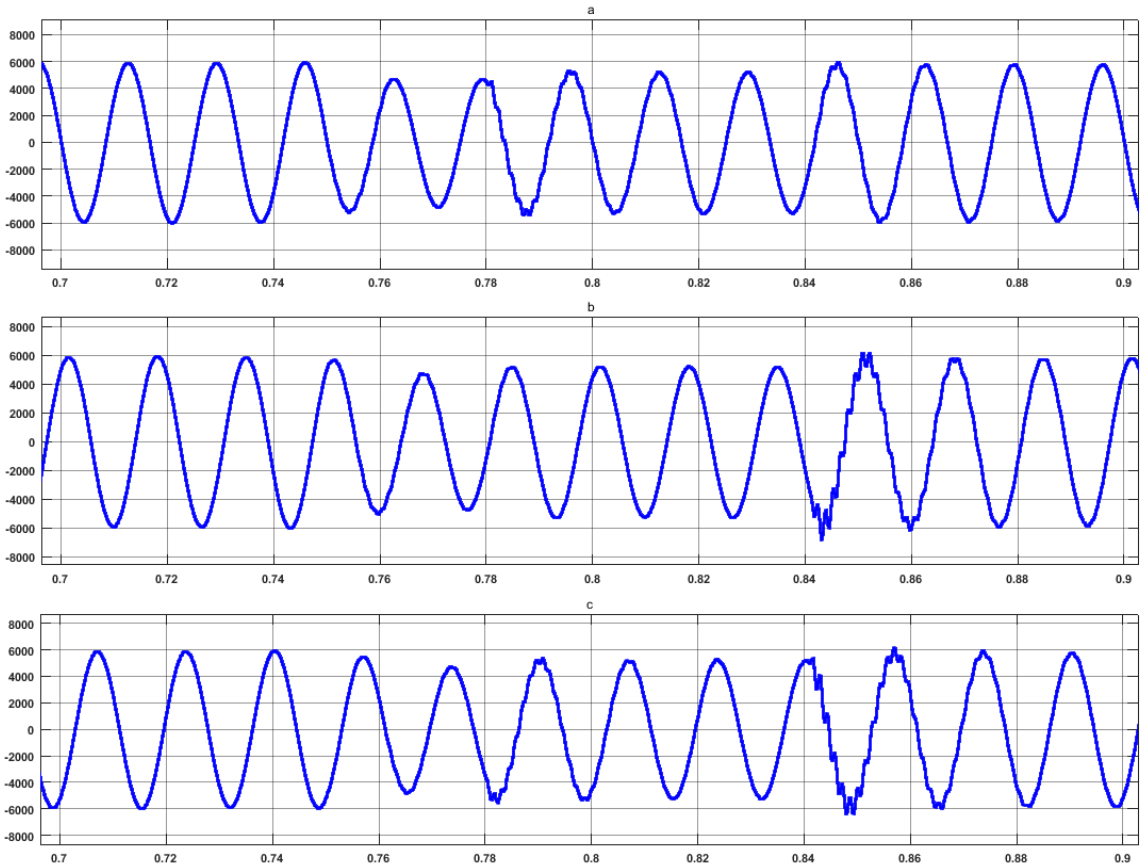


Figure 8-7: Output Load Voltage for 20% sag introduced at 0.75 sec of simulation time

8.3.3. Grid Voltage Sag: 50 % of 4.16 kV

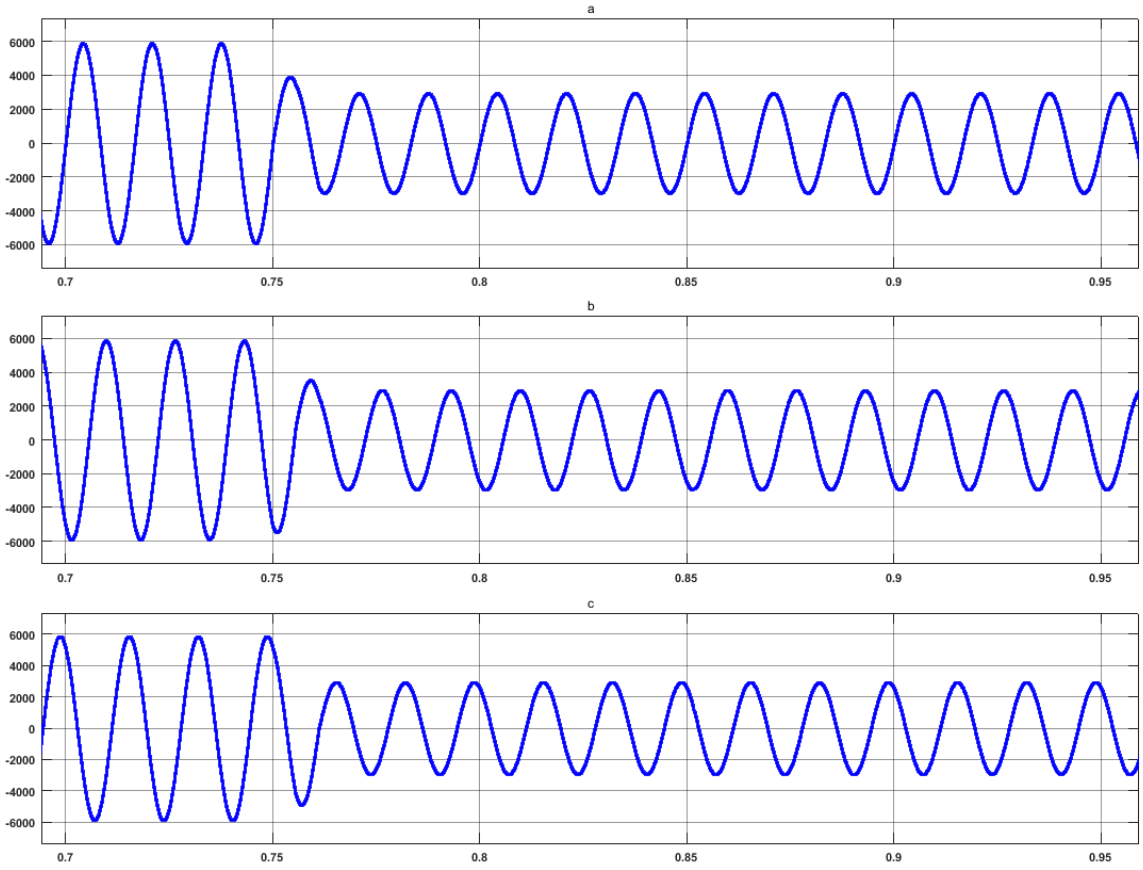


Figure 8-8: Input Grid Voltage for 50% sag introduced at 0.75 sec of simulation time

Figure 8-8 shows the input grid voltage with 50% voltage sag introduced at 0.75 seconds of the simulation time. It may be seen from Figure 8-9, that the CPC PLC may be used to regulate the output load voltage to desired value within a few fundamental cycles.

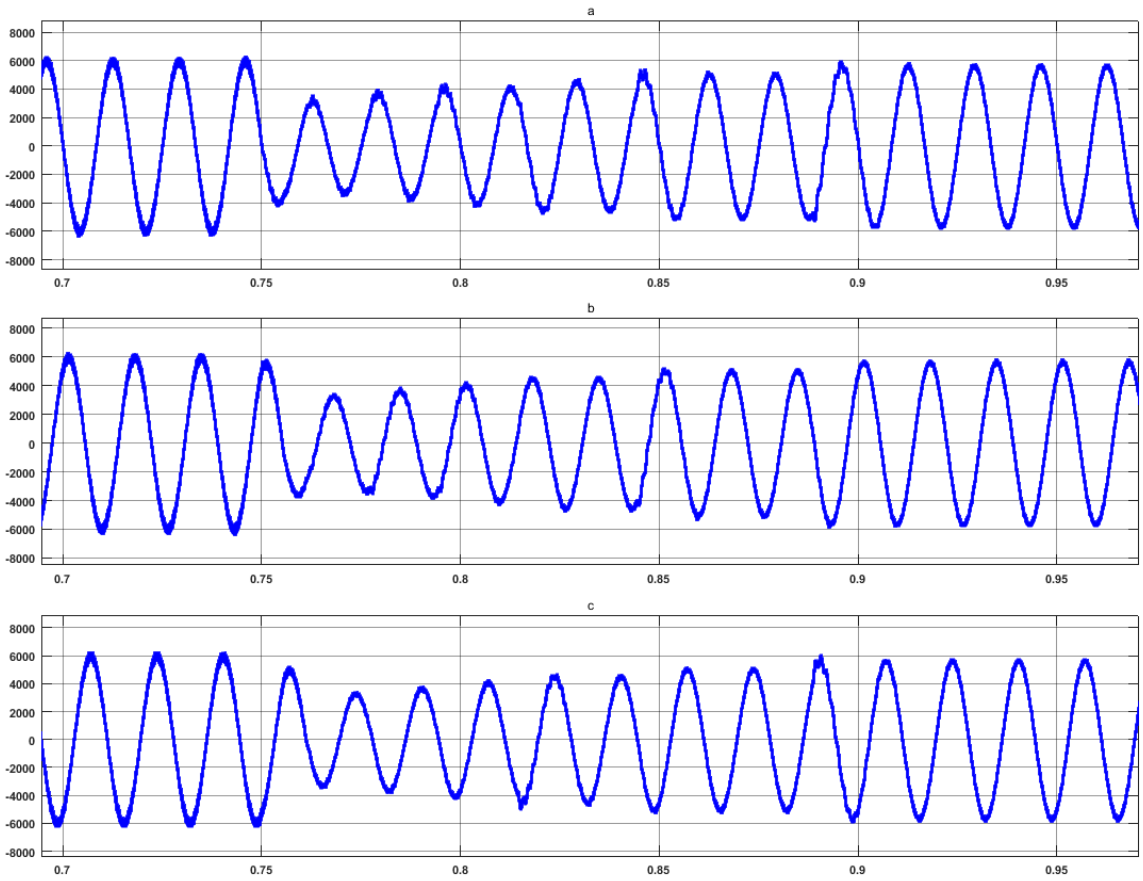


Figure 8-9: Output Load Voltage for 50% sag introduced at 0.75 sec of simulation time

8.3.4. Grid Voltage Sag: 80% of 4.16 kV

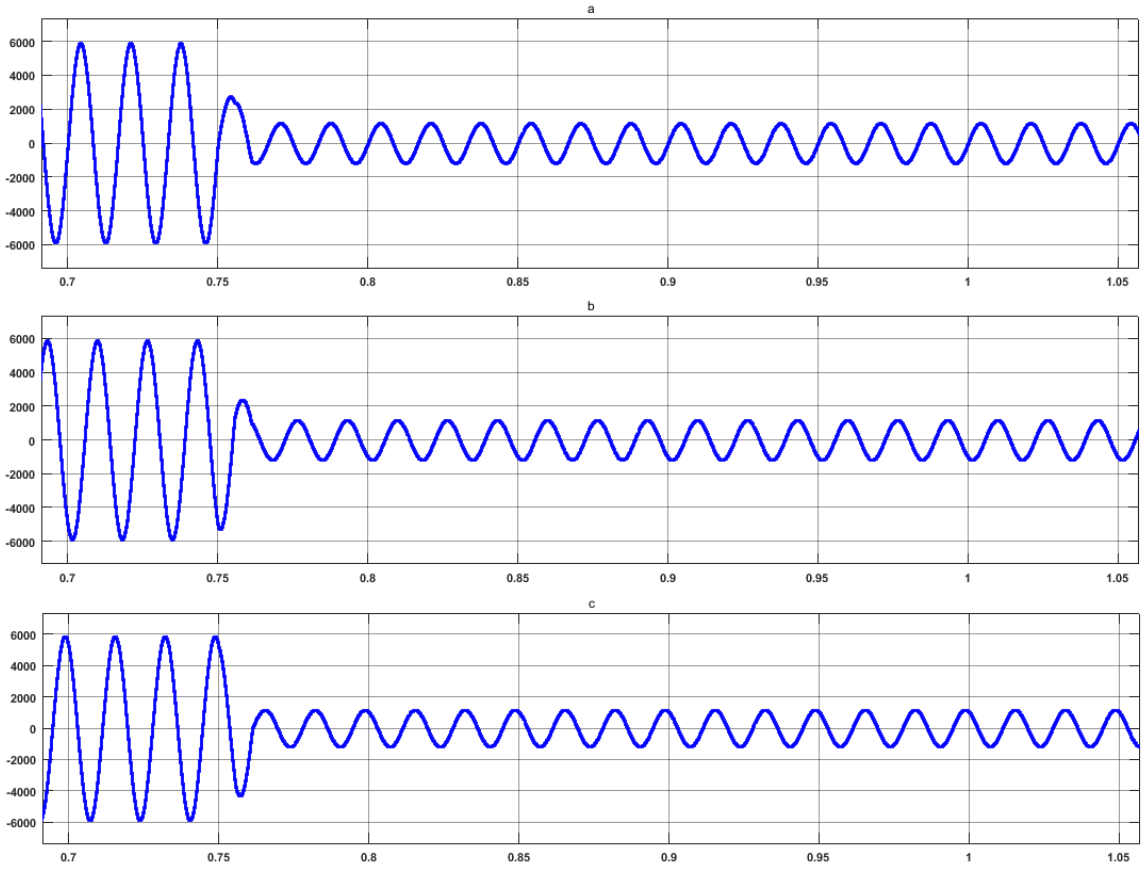


Figure 8-10: Input Grid Voltage for 80% sag introduced at 0.75 sec of simulation time

A voltage sag of 80% of the nominal grid voltage of 4.16 kV has been introduced to the CPC PLC simulation model at 0.75 seconds of the simulation time. It may be seen that the output load voltage has been regulated to desired nominal voltage of 4.16 kV by the CPC PLC within a few fundamental cycles of operation.

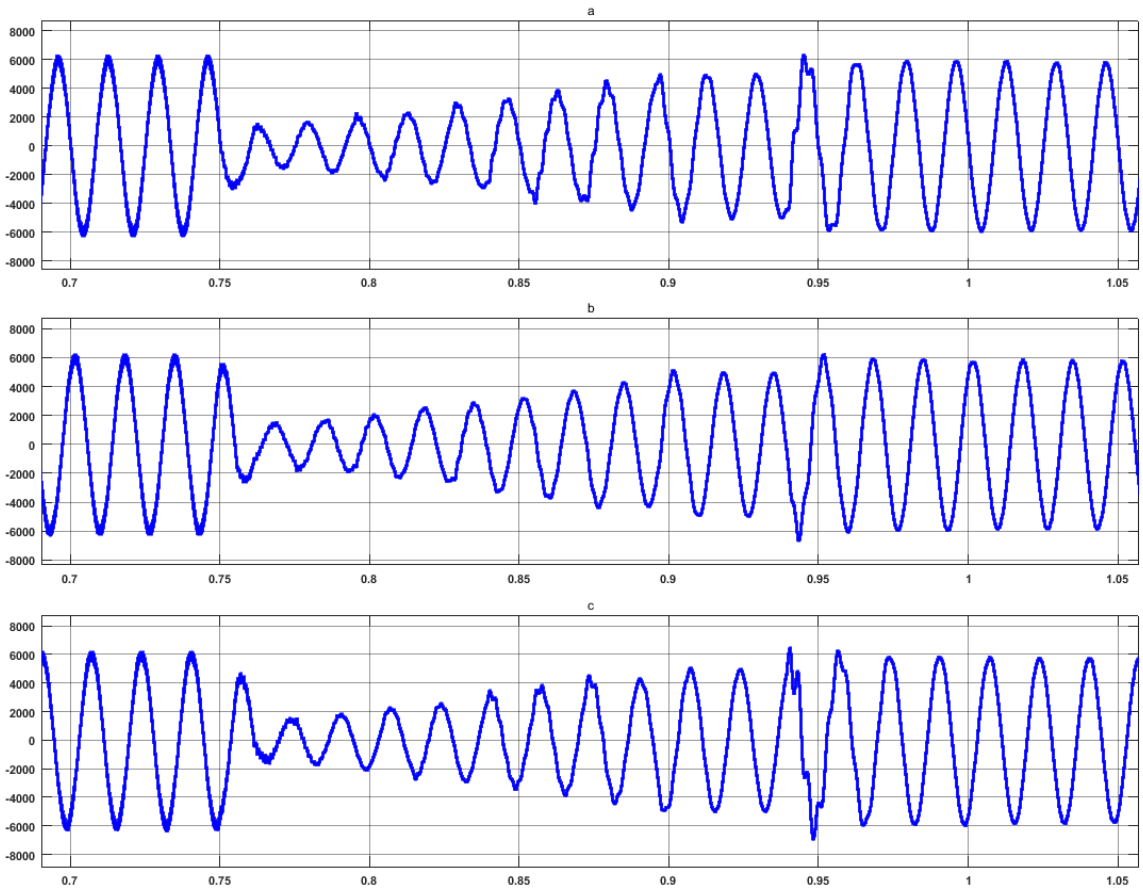


Figure 8-11: Output Load Voltage for 80% sag introduced at 0.75 sec of simulation time

8.3.5. Grid Voltage Sag: 90% of 4.16 kV

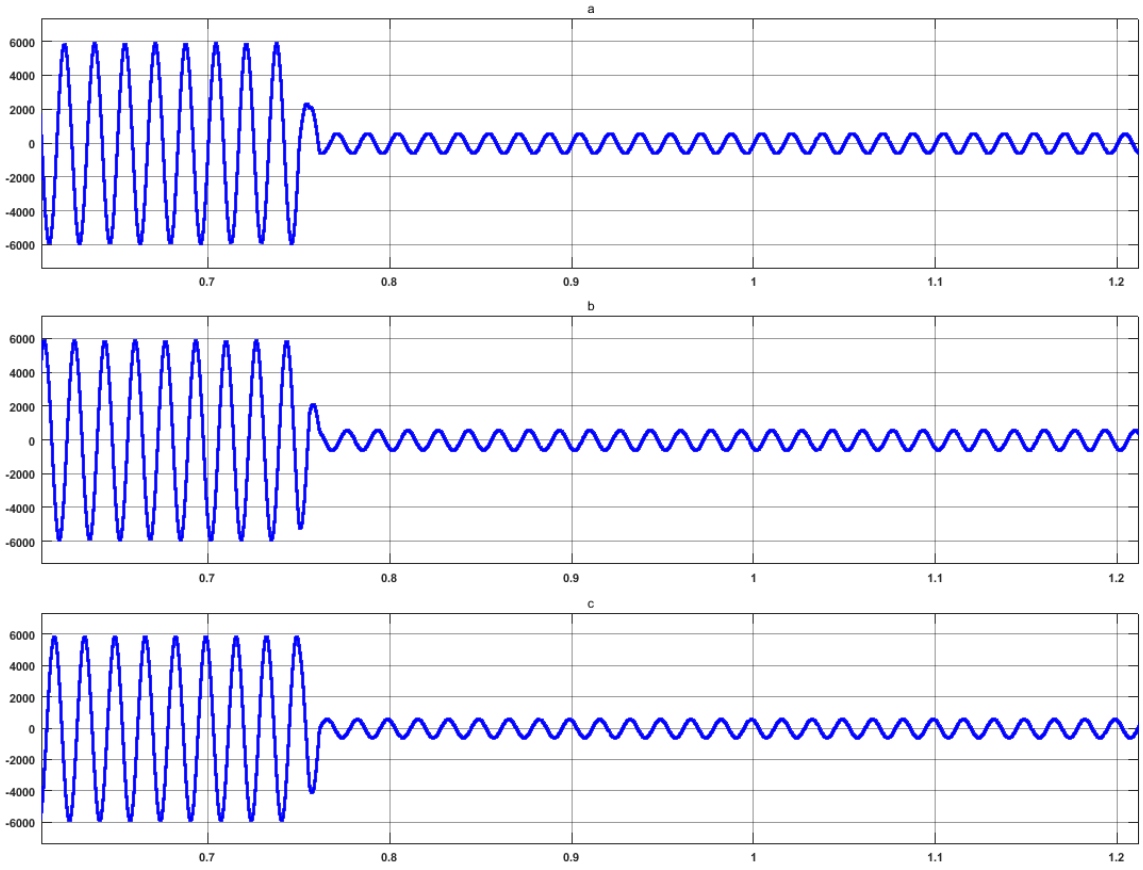


Figure 8-12: Input Grid Voltage for 90% sag introduced at 0.75 sec of simulation time

A voltage sag of 90% of the nominal grid voltage of 4.16 kV has been introduced to the CPC PLC simulation model at 0.75 seconds of the simulation time. It may be observed that the output load voltage has been regulated to desired nominal voltage of 4.16 kV by the CPC PLC within a few fundamental cycles of operation.

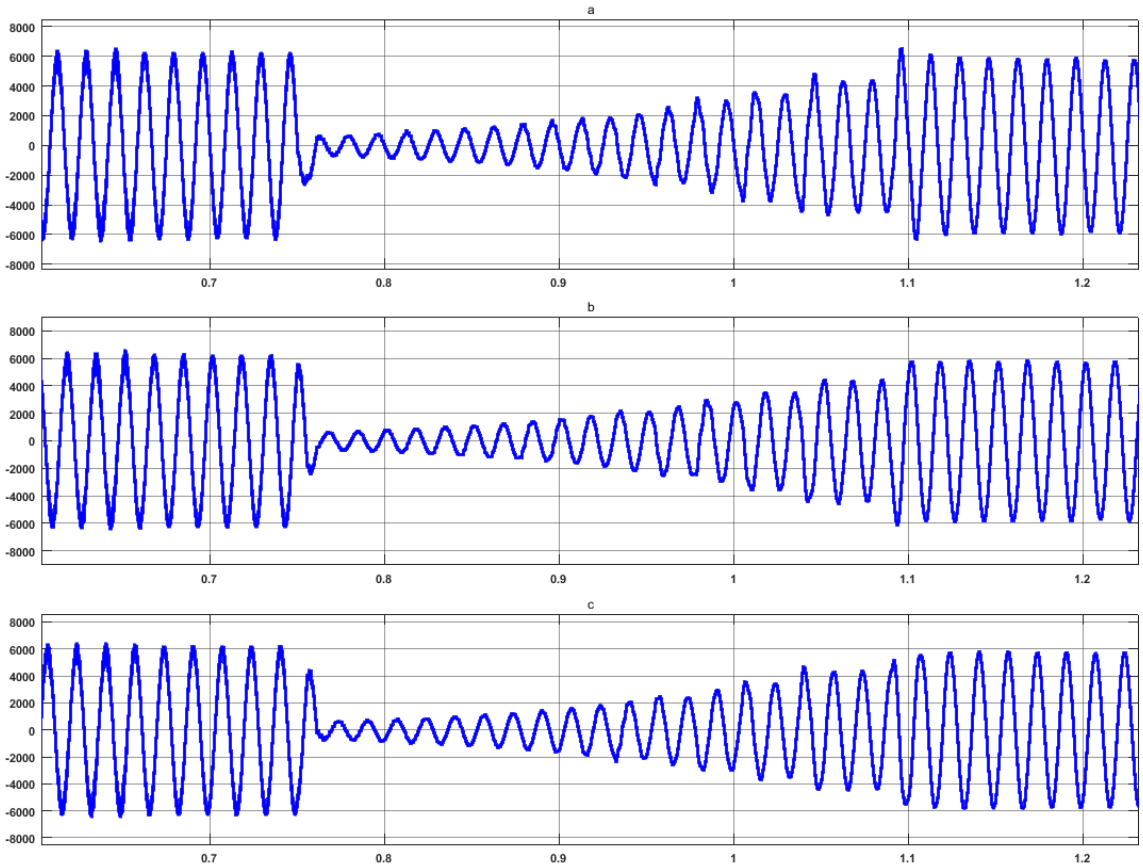


Figure 8-13: Output Load Voltage for 90% sag introduced at 0.75 sec of simulation time

8.3.6. Grid Voltage Swell: 10% of 4.16 kV

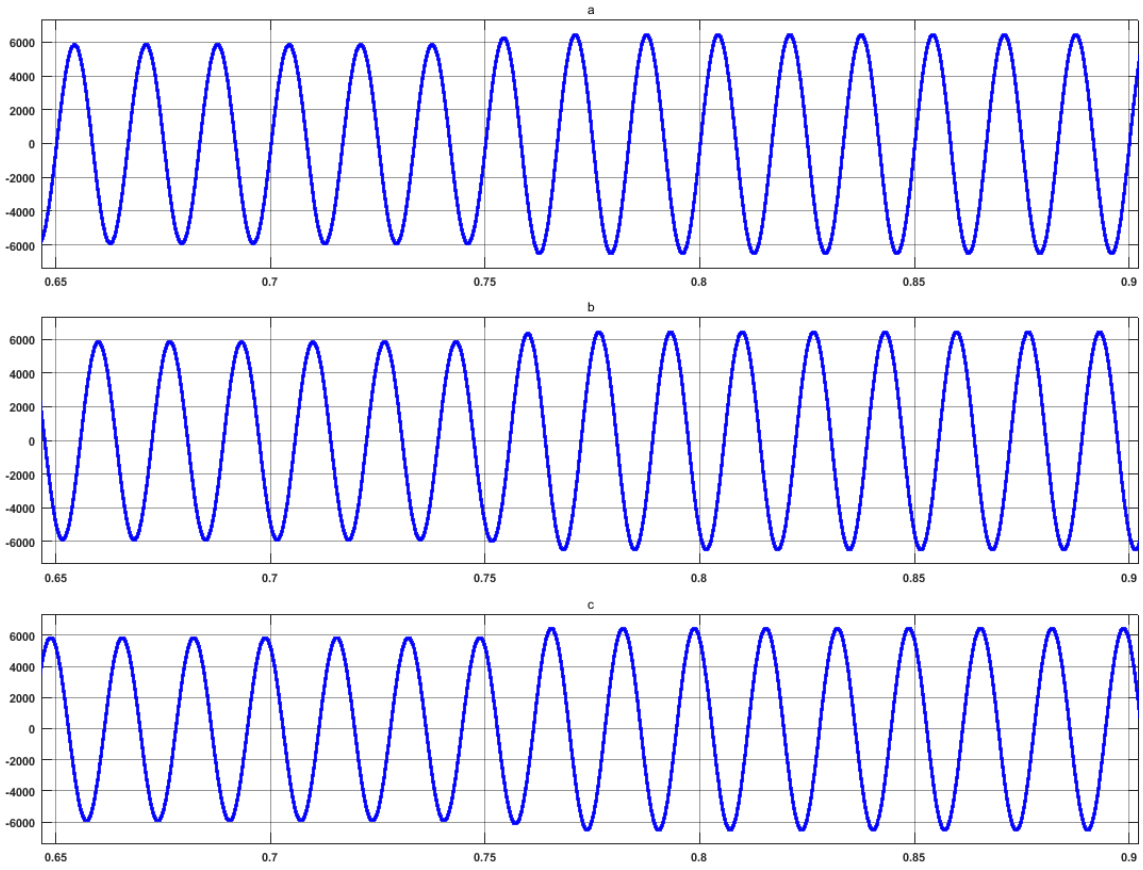


Figure 8-14: Input Grid Voltage for 10% swell introduced at 0.75 sec of simulation time

A voltage sag of 80% of the nominal grid voltage of 4.16 kV has been introduced to the CPC PLC simulation model at 0.75 seconds of the simulation time. It may be seen from Figure 8-15 that the output load voltage has been regulated to desired nominal voltage of 4.16 kV by the CPC PLC within a few fundamental cycles of operation.

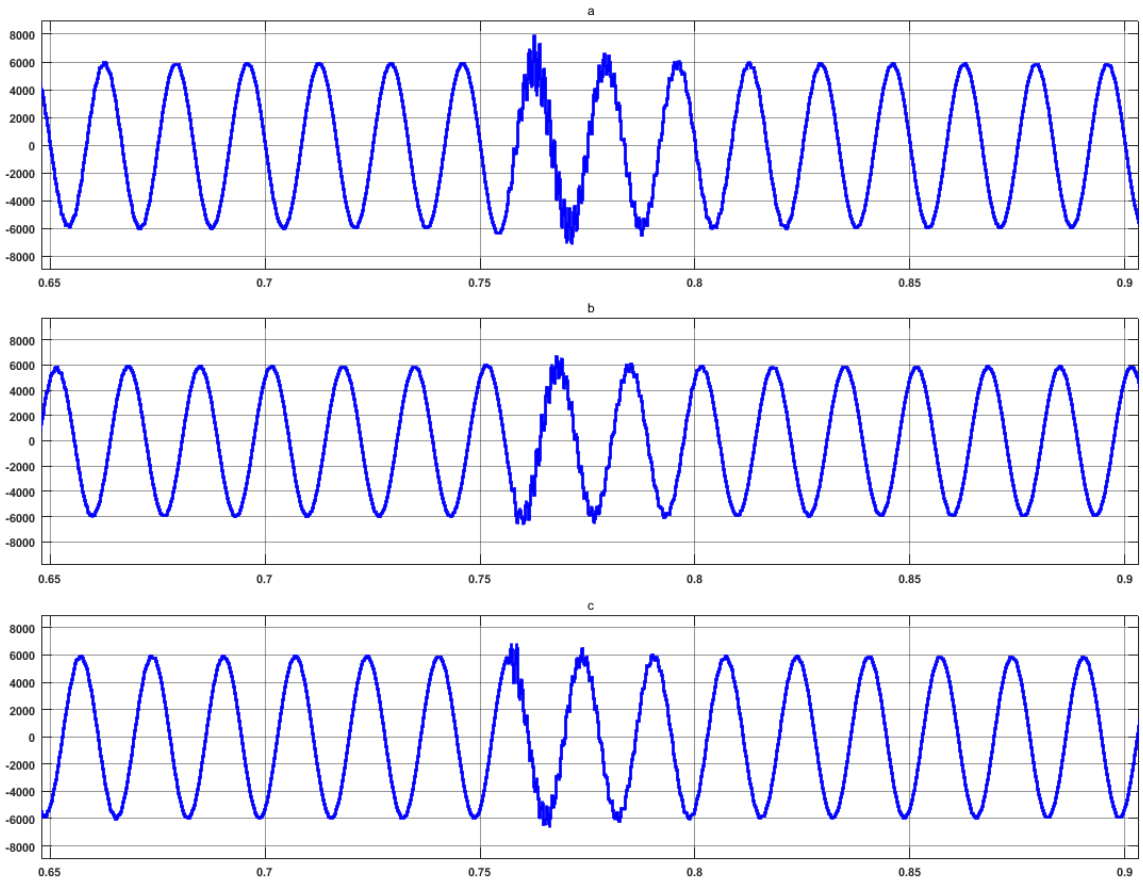


Figure 8-15: Output Load Voltage for 10% swell introduced at 0.75 sec of simulation time

8.3.7. Discussion on Performance of CPC PLC

The results demonstrated in this section evaluate the performance and capability of CPC PLC to mitigate grid voltage sags up to 80%. It may be noted that grid voltage sag of more than 90 % would amount to interruption. An interruption may only be mitigated by a power electronic converter which incorporates energy source other than grid like battery storage or solar energy in its design to supply the desired load voltage. Therefore, it may be concluded that CPC PLC may be used to mitigate grid voltage sag issues which constitutes 55 % of the grid power quality issues.

9. Chapter Nine: Conclusions

This chapter summarizes the principles and results pertaining to CPC PLC that has been presented in this dissertation document. It also proposes future scope for research in CPC PLC.

9.1. Comparative Evaluation of CPC PLC versus related power electronic solutions for power line conditioning

This section presents the salient features of CPC PLC as compared to the available power electronic converter-based solutions for power line conditioning.

Table 9-1: Comparison of CPC PLC versus Prevalent Power Quality Solutions based on design features

Converter Topologies→ **Features ↓**	**Dynamic Sag Corrector**	**Dynamic Voltage Restorer**	**Unified Power Quality Conditioner**	**Solid State Transformer**	**Three-Phase AC Line Conditioner**	**Center-Point-Clamped Power Line Conditioner**
No. of Power Conversion Stages (AC/DC OR DC/AC)	2	1	2	2(min) 4(max)	0	0
Types of Losses Involved	• Switching • Conduction	• Switching • Conduction	• Switching • Conduction	• Switching • Conduction	• Switching • Conduction	• Switching • Conduction
Device Voltage Rating	(Grid Line Voltage + Load Voltage)	(Grid Line Voltage + Load Voltage)	(Grid Line Voltage + Load Voltage)	(Grid Line Voltage + Load Voltage)	(Grid Line Voltage + Load Voltage)	$\frac{1}{2}$x (Grid Line Voltage + Load Voltage)
Control Complexity	Moderate	Moderate	Complex	Complex	Simple	Simple

Table 9-1 shows that CPC PLC has salient design advantages in terms of no. of power conversion stages as it is an ac-ac direct power converter, similar to three-phase ac line

conditioner. It also utilizes a simpler switching sequence as compared to the other prevalent power electronic solutions. The major advantage is its device voltage rating which is half the voltage stress as compared to other solutions. This allows use of lower voltage rated power semiconductor devices to design CPC PLC for higher utility scale voltages.

Table 9-2: Comparison of CPC PLC versus prevalent Power Quality Solutions based on power quality issue mitigation

Power Quality Solution → / **Disturbance↓**			**Tap-Changing Transformer**	**Dynamic Sag Corrector (DySC)**	**Dynamic Voltage Restorer (DVR)**	**Unified Power Quality Conditioner (UPQC)**	**Solid State Transformer (SST)**	**Three-Phase AC Line Conditioner**	**Center-Point-Clamped Power Line Conditioner**
Transients	**Impulsive**					✓	✓		
	Oscillatory								
Short-duration voltage variation	**Instantaneous**	**Interruption**			✓	✓	✓		
		Sag	✓	✓	✓	✓	✓	✓	✓
		Swell	✓		✓	✓	✓	✓	✓
	Momentary	**Interruption**			✓	✓	✓		
		Sag	✓	✓	✓	✓	✓	✓	✓
		Swell	✓		✓	✓	✓	✓	✓
	Temporary	**Interruption**			✓	✓	✓		
		Sag	✓	✓	✓	✓	✓	✓	✓
		Swell	✓		✓	✓	✓	✓	✓
Long-duration voltage variation	**Sustained Interruption**								
	Undervoltage		✓	✓	✓			✓	✓
	Overvoltage		✓		✓			✓	✓
Voltage Imbalance						✓	✓		
Waveform Distortion	**DC offset**								
	Harmonics				✓	✓	✓		
	Interharmonics								
	Notching								
	Noise								
Voltage flicker						✓	✓		✓
Voltage fluctuations					✓	✓	✓	✓	✓
Power frequency variations						✓	✓		

Table 9-2 shows a comparison of the capability of CPC PLC with respect to other prevalent grid power quality solutions. It may be observed that all these power quality solutions focus on grid voltage sag and swell compensation. It is so because it has been already presented in the dissertation Chapter-2 that voltage sag-related grid power quality events contribute ot 55% of all the grid power quality events.

9.2. Summary

This dissertation presents a novel topology of Center-Point-Clamped Power Line Conditioner, which is based on Center-Point-Clamped AC-AC Converter topology. The major contribution that the dissertation contributes is a center-point-clamping technique to reduce the voltage stress of power semiconductor-based switches that may be utilized to implement traditional and well researched simple converter topologies, like buck, boost and buck-boost converter for reducing voltage sag and swell in utility distribution grid. The buck-boost converter has been chosen to analyze and implement in this dissertation because it has the capability of both voltage buck and boost to provide the customer loads according to desired specifications, in the events of grid voltage sag and swell. The design of the Center-point-Clamped Power Line Conditioner (CPC PLC) which is based on buck-boost converter topology has been analyzed and discussed in the dissertation. The operating principle of CPC PLC has been demonstrated as well as simulation result waveforms from Matlab-Simulink model of CPC PLC verifying its operation methodology has been presented. The design of the components for hardware implementation of CPC PLC has also been analyzed in this document. The analysis of CPC PLC under dynamic operating conditions has been performed and discussed elaborately in this document. The design of a closed-loop output voltage controller to regulate the output voltage, irrespective of changes in source voltage or output load conditions have been presented in this document. Simulation results of the detailed circuit schematic model of CPC PLC with closed loop control of output voltage has been shown in this document. These simulation results verify the ability of CPC PLC to control the output load voltage at the desired customer output voltage. Finally, the experimental verification of the CPC PLC for both single-phase and

three-phase applications have been provided in the dissertation. The experiments waveforms further verify the operation methodology of center-point-clamping technique to reduce the voltage stress of the power semiconductor devices. Thus, it may be concluded that this technique allows the implementation of commercially readily available lower voltage rated devices to build power quality solutions for utility distribution grid level voltages. Furthermore, it also allows the implementation of simple direct ac-ac converter topologies as compared to ac-dc-ac converter topologies with multiple conversion stages. This is an advantage as multiple conversion stages contribute to further power loss in the conversion process as it involves more power electronic switches and passive devices.

9.3. Scope for future research

The CPC PLC topology may be further investigated to introduce a high frequency transformer in place of the inductor to provide galvanic isolation between the input and the output side of the converter. This introduction of a high frequency transformer can potentially lead to the evolution of a Center-point-Clamped Power Electronic Transformer.

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