FAULT-TOLERANT DESIGN FOR CONTINUOUS REAL-TIME MONITORING AND MODULATION OF THE HUMAN BRAIN

by

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ABSTRACT

IPSITA ACHARYA. Fault-tolerant design for real-time monitoring and modulation of the human brain. (Under the direction of DR. BHARAT JOSHI)

An era of brain implantable devices has been ushered in recent years. These devices are currently being used to treat neurological disorders such as Parkinson's depression and epilepsy and are increasingly being proposed for a wide range of neurological and neuropsychiatric disorders including chronic-pain and post-traumatic stress disorder. Given the seriousness of these brain disorders the accurate operation of these brain implantable devices is critical to the well-being of a patient. For example, a brain implantable device may be the only thing that may prevent a patient from entering depression or experiencing and acting on suicidal ideations. Hence, these devices are critical and need fault-tolerance.

In recent years, the design of brain implantable devices has also been driven by an increasing need for dense sensor arrays together with a need for a fully implantable signal monitoring and modulating circuitry that consumes low power (≈ few μWatts), occupies a small area (≈ few mm^2) and has the ability to wirelessly communicate with the external environment while monitoring bio-potential signals *in vivo*. The rapid scaling of CMOS technology in recent years has assisted this need for a low area-power design criteria in becoming a reality. However, it has also added a fresh set of reliability issues to the existing implantable designs which surprisingly do not incorporate fault-tolerance strategies which are *de rigueur* for other critical engineering devices.

This dissertation presents an argument for the inclusion of fault-tolerance in brain implantable devices to extend their dependability, and addresses the issue by proposing

possible fault-tolerant designs for these devices. A systems approach has been adopted to achieve the proposed fault-tolerant designs for the brain implantable system. This system includes an array of electrodes also known as the Multi-electrode Array or MEA to sense the underlying neural activity and, an implantable electronic circuitry to process and transmit the captured neural activity to an external recording and monitoring unit. Such an implantable device can also possess the ability to stimulate neurons or deliver drugs locally based on feedback received from the external unit. A hardware redundancy approach has been employed to provide a possible long-term solution to resolve the reliability issues in such implantable systems that are chronically implanted for long periods of time.

Two redundancy based solutions are proposed to improve the dependability of the brain implantable MEA. The first solution uses rows or columns of spare units to replace primary faulty sensors within the device. The second solution uses space redundancy with local reconfiguration capability. Here spare sensors are placed in interstitial sites and can replace neighboring primary faulty sensors. Different fault-tolerant solutions with varying degrees of redundancy and the equivalent graph models for these solutions are described. A maximum matching algorithm is described to match faulty primary to available spare modules for reconfiguration.

Three fault-tolerant designs are proposed to increase the reliability and availability of the brain implantable device. The fault-tolerant designs are analyzed and compared in terms of the area occupied, the power consumed and the overall system reliability to a benchmark design proposed for future brain implantable designs. The performance of these solutions is analyzed under different fault conditions to characterize the dependability of a fault-tolerant implantable system as a function of the redundancy introduced. The area-

power trade-off versus the degree of reliability included in the fault-tolerant device has been analyzed for a standard 0.18μm CMOS process. Results of the analyses demonstrate that a considerable improvement in the reliability of an implantable system can be achieved with a well-designed increase in redundancy.

DEDICATION

To my parents, my *bou* and *nana* and my ever-supportive and loving husband, *Anup*.

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TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION

1.1. Importance of Continuous Real-time Monitoring and Modulation of Neural Activity of the Human Brain

Understanding how the trillions of neural impulses of the brain's billions of neurons produce our thoughts, perceptions, and actions is one of the most intriguing challenges of the 21st century science. The ability to translate these neural communications to more interpretable electrical signals has presented new opportunities to treat a variety of neural disorders using neural prosthetic devices. For instance, epilepsy is one of the most common neurological disorders that affects 0.4% to 1% of the world's population [1]. Pharmacology, the first line of treatment for epilepsy, is helpful for controlling seizures in approximately 64% of patients [2]. For the remaining approximately 10-20 million patients worldwide with uncontrolled seizures a second line of treatment, where available, is brain surgery [3], and a third line of treatment which has emerged in recent years is the use of brain implantable devices [4]. Currently brain implantable devices employ electrical stimulation to control seizures [5], [6], [7]. Other implantable devices under development seek to warn of an impending seizure, deliver drugs locally or cool the brain to control seizures. Epilepsy surgery may require multi-day intracranial monitoring of the brain to locate the source of seizures and brain implantable devices to control seizures require permanent monitoring of brain activity to detect or predict a seizure. Parallel to this effort in epilepsy is an independent effort to develop a brain machine interface (BMI) to detect brain activity and typically activate an external actuator such as a robotic arm or make a

decision [8]. In the BMI field the effort is primarily focused on detection and analysis of single unit or multi-unit activity and to a lesser extent on the measurement and analysis of the local field potential.

Though there are differences between the epilepsy and BMI fields, there are also similarities in that both fields endeavor to measure neuronal activity directly from the brain and increasingly for a long period of time up to the life of the patient. There is also mounting evidence that the sensing solution in these efforts will involve increasingly larger numbers of electrode contacts which are often placed in a dense arrangement [9], [10]. For example, a first generation implantable device has 96 contacts in a dense 2D array arrangement. Among the second generation devices which are being proposed are some which will have 1,000 or more contacts arranged in a dense 2D grid. Recent years have witnessed the development of micro-fabricated neural probes such as the Utah and Michigan arrays that have been in use in experimental labs as well as in clinical applications for brain-machine interface for treating patients with paralysis [11].

As it would be true for any portable or implantable device, these neural-activity recording systems require miniature electronics locally in order to amplify the weak neural signals, filter out noise and out-of-band signals and digitize the amplified neural signal for transmission to an external monitoring unit. The recent advancements in modern semiconductor technology has sparked significant research activity in the development of such miniature electronics, particularly in the last decade [12], [13], [14], [15], [16], [17], [18], [19], [20], [21].

More recent efforts have been spurred by Defense Advanced Research Projects Agency (DARPA, an agency of the United States Department of Defense) programs funded by the

presidential Brain Research through Advancing Innovative Neurotechnologies (BRAIN) initiative. This initiative has been recently undertaken to improve our understanding of the human brain, the most complex biological structure in the known universe. The BRAIN initiative funded DARPA programs include Systems-Based Neurotechnology for Emerging Therapies (SUBNETS) and Restoring Active Memory (RAM). DARPA SUBNETS seeks to improve the health of U.S. service members, veterans, and civilians from the effects of neuropsychological illness brought on by war, traumatic injuries, and other experiences while the RAM program is targeted towards military personnel and civilians suffering from Traumatic Brain Injury (TBI). In addition to DARPA, the NIH, NSF, FDA, and IARPA have also announced brain initiative programs towards the goal of improving our understanding of the human brain. These agencies are following a 12 year plan outlined in the BRAIN 2025 report with the first several years being focused on developing the tools and technologies needed to make the next leap in understanding the human brain [22].

1.2. Demands and Challenges of Next Generation Brain Implantable Devices

A close look at a typical brain implantable device shows that it consists of two layers – the layer nearest to the neural tissue is a group of sensors or electrodes. The second layer includes a neural signal processing block. The sensing layer consists of an array of electrodes that are either distributed or concentrated to capture the underlying neural activity. And, the neural signal processing block usually includes an analog-front-end unit which consists of three main blocks: (1) the bio-potential amplifier, (2) a band pass filter, and (3) a unity gain buffer. Recent years has witnessed a growing demand for small size, low-power, and ambulatory physiological signal acquisition system [23]. In addition to

these constraints/requirements the details of the electrode material, the electrode-tissue interface and the type of neural signal itself present further challenges to the implanted microelectronics. The observed neural signals contain an electrode offset potential as well as extracellular action potentials (EAPs) and local field potentials (LFPs). The EAPs typically have amplitudes of 25μV- 1mV with a signal band of 100Hz – 3KHz, whereas the LFPs have amplitudes up to 5mV with a signal band of 0.5 – 300 Hz. Additionally, the electrode-electrolyte interface introduces an offset that can be several 100's of mV, with the microelectrodes themselves contributing thermal noise due to their relatively high impedance [24]. All the above factors, in particular the desire to make such systems implantable (i.e. enabling wireless communication with an external unit) dictate the limits on the size and thermal dissipation (to avoid tissue damage) of the implantable system. And, with the next generation neural interfaces targeting 100s to 1000s of channels and requiring continuous real-time monitoring, resource constraints for implantable systems in such applications will be extremely stringent.

Unlike other critical applications, the currently available as well as the proposed solutions for continuous real-time monitoring of the electrical activity of the brain are all intolerant to faults [25]. There are several aspects of an implantable sensing device which can fail. These include the reference electrode, sensors, signal conditioning and digitization circuitry, and computation, power and communication sub-systems. Faults can arise either in the sensing electrodes or in the neuroelectronic circuitry. Faults which affect sensing can arise because of sensor failure due to mechanical stress on the sensor or the connecting wires during surgery to place electrodes or due to stress from changes in the brain and the surrounding milieu thereafter. Sensor failure can also arise due to the brain tissue response

to chronically implanted sensors possibly resulting in encapsulation of a sensor due to gliosis, which can further lead to neuronal death at the sensing site [26]. In case of erroneous behavior of the implanted sensor or the neuroelectronic circuit, the electrical activity recorded will not be observed correctly, thereby impairing the purpose of the implanted device. For epilepsy surgery this may require the approximation of information from neighboring sensors if they exist, and a second surgery to replace failed sensors in extreme instances. In the case of a seizure control device the failure of error free monitoring of the electrical activity of the brain may necessitate surgery to remove the malfunctioning sensor and re-implantation of a new set of electrodes or a new implantable device altogether. While the initial surgery to place sensors carries a risk, surgery to replace sensors and a device can involve further risk with associated morbidity and mortality which remain to be determined but is expected to be equal to or greater than that of the surgery to place the first set of sensors.

While there is a need to monitor the brain in real-time for extended periods of time with very densely spaced sensors, the progress in developing such systems has been limited by semiconductor technology. It is well known that there is a massive complementary metal-oxide semiconductor (CMOS) scaling effort that will continue to shrink device size. However, there is an increasing performance gap between CMOS device technology and its ability to deliver performance that is proportional to the device density. Moreover, power consumption and heat dissipation pose additional challenges. Recognizing that these factors may render Moore’s law of scaling less attractive in future, researchers have started to focus on the nanoelectronics research, such as carbon nanotube transistors, molecular electronics, and spintronics. These emerging technologies together with the scaling of the

CMOS devices are expected to revolutionize biomedical systems, including brain implantable devices. But as the electronic devices get smaller and enter nanoscale levels, these nanodevices will have higher manufacturing-defects leading to higher number of errors in the implantable neuroelectronic circuits. This together with the need for continuous real-time monitoring of neural activity of brain for extended periods of time has created an urgent need to address the issue of inability to tolerate faults in such systems. Thus effective fault tolerant strategies have to be incorporated into the architecture to tolerate intermittent and permanent faults so that the systems can be used reliably for extended periods of time. It is imperative to believe that reliable sensing of the human brain for an extended period of time necessitates fault-tolerant design to assure reliability of the implantable design. That is, fault-tolerance should be incorporated into the architecture of the implantable device.

1.3. Dissertation Contribution

This dissertation presents an argument to incorporate fault-tolerance into the architecture of brain implantable devices. Reliability analysis of a system must be preceded by the knowledge of the level of abstraction for the possible faults that are anticipated to occur in the system. The analyses in this piece of work involves a fully implantable integrated chip that includes a neural interface to sense the underlying neural activity, its corresponding microelectronic circuit to process the signals in order to monitor and record them at an external unit, and a feedback mechanism to enable neural stimulation or local drug delivery. The choice of the level of abstraction for faults should be decided such that, it permits a manageable reliability analyses without losing much information. Hence, only functional-level faults are considered in this work.

A hardware-redundancy philosophy is adapted to incorporate fault-tolerance in the implantable device. Redundancy at the system level will possibly lead to a fault reconfiguration which will be time-consuming, expensive and risky (due to the need for re-surgery to replace the faulty system) to achieve. Redundancy at the circuit-level will need a highly complex fault-detection and location mechanism to achieve system reconfiguration from faults. In between the above two extreme layers of abstraction of the system, lies the component-level, in which, the fault-detection and diagnosis is easier to achieve than at the circuit-level and the fault-reconfiguration process will be faster, cheaper and safer than at the system-level. Hence, a component-level redundancy approach is adopted to increase the dependability of brain implantable devices intended to be used chronically for long periods of time.

Every component in the integrated device will have a specialized function to achieve. If the fault-tolerant mechanism detects a functional failure in the component a reconfiguration mechanism will be initiated to replace the faulty component. For example, the neural interface of the implantable system will include additional spare electrodes that can replace the primary electrodes in case of a failure of the primary electrode(s). Multiple configurations have been explored to place the spare electrodes in the primary grid and the reliability of each of the explored configuration has been analyzed. The neural microelectronic circuitry incorporates fault-tolerance by including redundant units of the major components such as the neural-front-end, and the analog-to-digital converter.

Five fault-tolerant solutions have been proposed to increase the dependability of brain implantable devices. They can be broadly categorized into two groups based on the location where the redundant units are incorporated in the implantable system. The first

two fault-tolerant solutions are aimed towards increasing the dependability of MEAs. The MEA consists of a grid of spare and primary modules, where each module has a sensor and the corresponding signal conditioning circuitry. The first solution utilizes rows or columns of spare modules to replace faulty primary modules. The second solution uses space redundancy with local configuration capability where spare modules are placed in the interstitial sites of the MEA and can replace their neighboring faulty primary modules [27]. A patent related to this piece of work has been filed and published [28].

A second category of fault-tolerant solution is proposed in which the sensor array and its accompanying signal conditioning circuits are considered to be separate entities and have different degrees of redundancy. This category offers three fault-tolerant architecture designs. The first architecture includes redundant electrodes in the sensor array. This architecture includes the least amount of redundancy hence it is more attractive as a relatively low cost design focusing on enhancing the dependability of the device by increasing the reliability of the sensor array, that typically includes inactive components such as metal contacts to capture the neural activity.

The second fault-tolerant architecture proposed introduces redundancy in the neural-front-end (NFE) unit of the fully implantable neuroelectronic circuitry in addition to the redundancy in the sensor array. The neural-front-end unit is responsible to amplify and filter the neural signals, without which the monitoring of the weak neural data captured by the underlying sensors will not be possible. This fault-tolerant design can have multiple variations depending on the level of redundancy involved in the design. The possible variations of this fault-tolerant architecture are further discussed in detail in Chapter 4.

A third fault-tolerant architecture proposed involves the idea of hardware redundancy in the sensor array, the neural-front-end and analog-to-digital-converter units of the neural microelectronics layer. In comparison with the two above-mentioned fault-tolerant designs this design is believed to have the highest degree of reliability. However it might not be cost effective due to the fact that incorporating redundancy in all the major neuroelectronic components might be expensive. Chapter 4 includes an analysis of the reliabilities of each of the proposed fault-tolerant architectures. Therein, the performance parameters, such as area, power and reliability of the proposed fault-tolerant architectures fabricated on a 0.18μm CMOS technology are calculated and compared to a benchmark design that is proposed for future brain implantable architectures, in order to justify the feasibility of the proposed fault-tolerant architectures and to highlight the possible advantages of the proposed designs.

The fault-tolerant strategy will include a built-in system testing methodology that can test the major components of the device in real-time to detect faults in the system. Once a fault is detected the fault reconfiguration algorithm is initiated that isolates the faulty unit and replaces it with a spare if available for the failed unit. This dissertation considers fault-tolerant approaches for intermittent and permanent faults only. A permanent fault is one which exists indefinitely in absence of a corrective action while an intermittent fault is one which appears and disappears repeatedly. A transient fault exists for a limited duration. Transient faults typically do not require system reconfiguration and thus are not considered.

The remaining of the dissertation is organized as follows: Chapter 2 introduces fault-tolerance and describes the existing neural signal monitoring and modulating techniques for brain implantable devices. Chapter 3 describes and analyzes two proposed

fault-tolerant solutions designed to improve the reliability of a fully implantable multi-electrode array. Chapter 4 describes and analyzes three other fault-tolerant designs aimed to improve the dependability of implantable neural devices with different levels of redundancy in the sensing and the neural signal monitoring and modulating circuitry of a brain implantable device. The design of the benchmark architecture that is used in our work for comparison and analyses of the proposed fault-tolerant architectures, is also discussed in Chapter 4. And finally, Chapter 5 concludes the presented work with possible future work and some final thoughts on this work.

CHAPTER 2: BACKGROUND

2.1. Fault-tolerance and Dependability

Fault tolerant operation can be defined as the process by which a system continues to perform its specified tasks correctly in the presence of faults. These faults could occur either in the hardware or the software, and can be caused by faults due to manufacturing defects, wear and tear and environmental effects. They could also be caused by external environments or simply due to ageing of the components. The goal of fault tolerant design is to improve system dependability which is defined as the ability of a system to deliver a service at an acceptable level of confidence. Dependability is most commonly characterized in terms of the attributes of reliability and availability [29]. A fault-tolerant solution requires the use of redundancy in some form or the other. The amount of redundancy can be quantified by the redundancy ratio of a fault-tolerant design, which is defined as the ratio of the number of spares to the number of primaries in the fault-tolerant unit. We define the reliability of a system as the conditional probability that the system performs its tasks correctly during a time interval (t_0, t), given that the system was performing them correctly at time t_0. And, the availability of a system is defined as the probability that the system is available to perform its tasks correctly at time t. It is evident that any type of fault tolerance technique requires the use of some form of redundancy, incorporating which will increase both the cost and the development time of the system. Furthermore, redundancy can also have impact on the system's performance, power

consumption, size and weight. Thus a good fault tolerant design requires a trade-off between the level of dependency provided and the amount of redundancy used. The amount of redundancy incorporated can be effectively quantified by the redundancy ratio of the fault-tolerant system.

2.2. Existing Neural Signal Monitoring and Modulating Techniques

Acquiring brain signals from within the brain requires the presence of a neural interface in a brain computer interface (BCI) system, which is a piece of hardware that detects brain signals so that the sensed neural signals can be sent to the neural signal conditioning components of the BCI for analysis and translation into useful commands. BCI neural interfaces can be broadly classified into three categories: (i) Electroencephalographic (EEG) scalp electrode arrays, that attach non-invasively to the skin to record field potentials with relatively low information content from very large and widely distributed sets of neurons and synapses; (ii) Electrocorticographic (ECoG) electrode arrays that are surgically positioned on the surface of the brain i.e. on the cerebral cortex, to record field potentials with moderate information content from smaller more localized sets of neurons and synapses; and (iii) miniaturized microelectrode arrays that are surgically inserted into the cerebral cortex to record neuronal action potentials (APs or spikes) from individual neurons and/or local field potentials (LFPs) from small highly localized sets of neurons and synapses and that yield high information content. Figure 1 shows the recording domains of different types of neural interfaces.

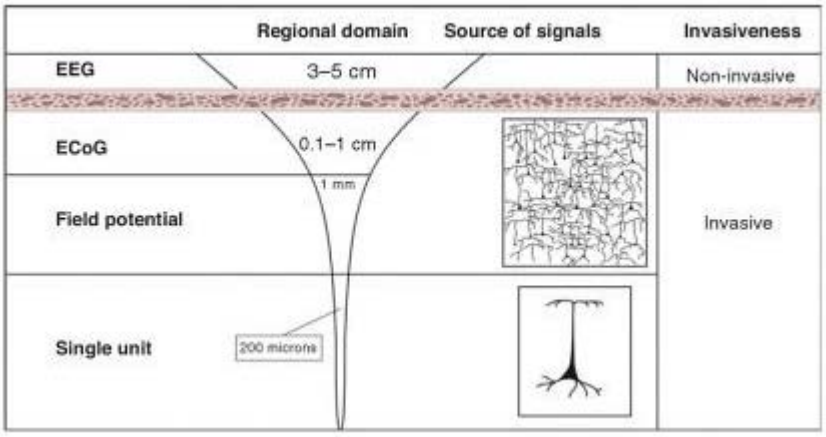


Figure 1: Neural recording domains for single unit, LFP, ECoG and EEG recordings [30].

EEG signals present a relatively poor signal characteristics, i.e. few centimeters in spatial resolution and a bandwidth of 0 – 70 Hz, with respect to ECoG, LFPs and APs. This poor signal characteristics is due to volume conduction through the tissue between the brain and the electrode, which makes the signals spread and blur as it passes through the dura, fluids, skull and skin. Hence, in order to achieve sensing resolution required to seamlessly operate a BCI system and the ability to provide a possible feedback (ex. local drug delivery or to provide neural stimulation), invasive neural recording techniques are required.

Electrocorticography (ECoG), which is also known as intracranial EEG or iEEG represents a midway between scalp recorded EEG signals at one end and intracortically recorded single unit action potentials (APs) and local field potentials (LFPs) at the other. ECoG signals can be recorded either from the surface of the dura mater (i.e. epidurally) in which the electrodes are placed on the dura or from beneath the dura (i.e. subdurally) in which the electrodes are placed directly on the surface of the brain [10].

There are two types of implantable microelectrode arrays for BCIs: microwire electrodes and silicon micro machined electrodes. Microwire electrodes (*Tucker Davis*

technologies) consist of an array of thin wires soldered to a connector in two or more rows with a wire diameter of 25-50 µm, having only one recording location at the tip of each wire and are capable of recording from deep cortex (up to 5 mm) [31]. The silicon based micro machined probes involve microfabrication of silicon and polymer structures for miniaturized sensors, actuators and integrated microsystems. Two of the most well-known silicon probes are the Utah Electrode Array and the Michigan-Style Probe. Like the Microwire Array, the Utah Electrode Array has only one recording tip at every electrode site [32]. The Michigan-Style Probe has multiple electrode sites located on the sides of each of the penetrating shanks [33], [34]. Although the microelectrode arrays are capable of providing high spatial and temporal resolution of neural activity, the recording signal-to-noise-ratio (SNR) gradually degrades over time and uniformly fails over time with a life-time ranging from several-weeks to several-months, due to the brain-tissue response to the implanted microelectrode arrays [35]. These devices can potentially cause hemorrhage and inflammatory tissue responses from immediate insertion and if implanted for long periods of time, due to the rigidness of the penetrating electrodes which are incapable of conforming to the movements of the brain. In order to obtain stable, long-term recordings from a large population of neurons from across the brain some BCI researchers have indicated the advantages of flexible electrode arrays of subdural electrodes that can maintain signal quality over extended periods of time [36], [37].

In order to acquire the signals picked up by the implanted microelectrode array of electrodes, the weak neural signals first needs to be amplified. To do so, researchers at University of Utah produced a skull-mounted interface electronics for neural signal acquisition, called the Integrated Neural Interface (INI1 and INI2). In which, the Utah

Electrode Array was connected to the skull-mounted interface electronics called the *head-stage*, via a thin wire cable through a tiny hole in the skull [12], [32]. However, the INI1 and INI2 chips were not stand alone devices and required a number of external components for operation, that involved tethering of the subject to external neural signal decoding electronics and had to be powered from a battery source. An improved version of the INI chip, the INI3 was developed to overcome the shortcomings of the previous versions of the chip such as dependency on external devices that limit the mobility of the subject under study, the need for a low-power IC to reduce surrounding tissue damage and the necessity for a wireless link for communications [38]. To acquire neural signals from the Michigan-style electrode array, the penetrating shanks are integrated with a thin-film ribbon cable, which is then integrated with a silicon substrate containing the bond-pads. This is then bonded to a connector which interfaces to an instrumentation system [39], [40]. The in-vivo performance of the Michigan-style probe is described well in [41], [42] and [43].

The benefits that a fully-implantable wireless BCI system presents includes elimination of the risk of infection due to any percutaneous connections, reduction in the mechanical vulnerability of a skull-mounted unit to accidental impacts (example: an epileptic patient), and a host of clinical and health care benefits such as possibilities of 'scaling-up' the available recording sites to access larger brain locations, non-tethering of the patient to external devices, and design flexibility to enable bidirectional communication with the brain. To avail the benefits of fully implantable wireless BCI systems researchers at Brown University have demonstrated an implantable concept known as '*Braingate*', a fully-implantable neural signal acquisition device that can support a maximum of 100

recording channels [44], [45], [46], [47], [48]. A similar motivation is evident in the work of [49], [50], [51].

There is mounting evidence that the future of neural sensing solutions will involve increasingly larger numbers of electrode contacts which are often placed in a dense arrangement [9], [10]. For example, a first generation implantable device has 96 contacts in a dense 2D array arrangement. Among the second generation devices which are being proposed are some which will have 1,000 or more contacts arranged in a dense 2D grid. The demand for monitoring higher number of recording channels than before will evidently increase the area consumed by the implantable device and the power-dissipated by it into the surrounding tissue. Fortunately, due to the advancements in semiconductor technology it is possible that the implantable IC can be implemented at smaller feature size, thereby achieving the size constraints applicable in such devices. However, an increase in temperature of the surrounding tissue cannot be allowed, because even a mere 1.0 °C can result in neuronal death. Hence, to achieve a dense recording with fully implantable wireless signal acquisition systems have been proposed in [12], [44], [52], [53], [54], [55], [56], [57], [58], [59]. To ensure that such stems can operate continuously for long periods of time, the individual components of the implantable integrated circuit (IC) that processes the neural signals must consume very low-power and occupy a small area. Several efforts have been proposed to achieve the area-power limitations in [12], [18], [60], [61], [62].

2.3. Brain Implantable Architecture

Typically the architecture of a brain implantable device used for recording neuronal activity of the brain consists of a group of sensors connected to an amplifier to amplify the weak neural signals captured by the sensors, an analog multiplexer to route the signals from

multiple sensing sites to the next processing unit, and an analog-to-digital converter to convert the neural signals from analog domain to the digital domain so that it can be easily transmitted to an external monitoring unit where further analysis can be done on the neural signals. The same architecture may include other electronic circuits required for neural modulation and computation.

The architecture of the implantable device, considered here, consists of a MEA with multiple electrode contacts (sensors) and circuitry to condition and digitize the sensed signals. Each sensor in the sensor grid is connected to signal conditioning and processing circuitry that includes an amplifier, one or more filters, an A/D converter and a D/A converter, if one is needed. For simplicity, a modular design is considered, where a sensor and its accompanying signal conditioning and processing circuitry are considered to be a module. This circuitry may be connected to additional modules for computation, communication and intervention.

2.3.1. Multi-electrode Array

A multi-electrode array or as it will further be referred as MEA in this document is an array of electrodes that is a vital block for any brain implantable device that is designed to monitor the underlying neural signals and in some cases for stimulating areas of brain to facilitate a treatment procedure and/or to enable a local cooling mechanism via drug delivery.

2.3.2. Neural Activity Monitoring and Modulating Circuit

Figure 2, represents the block diagram of neural microelectronic circuitry that is expected to monitor and modulate neural activity. Monitoring the neural signals occurs in

the direction of the flow of the directed arrows. Modulation or stimulation signals are directed to the electrodes in the MEA from a neuromodulator block.

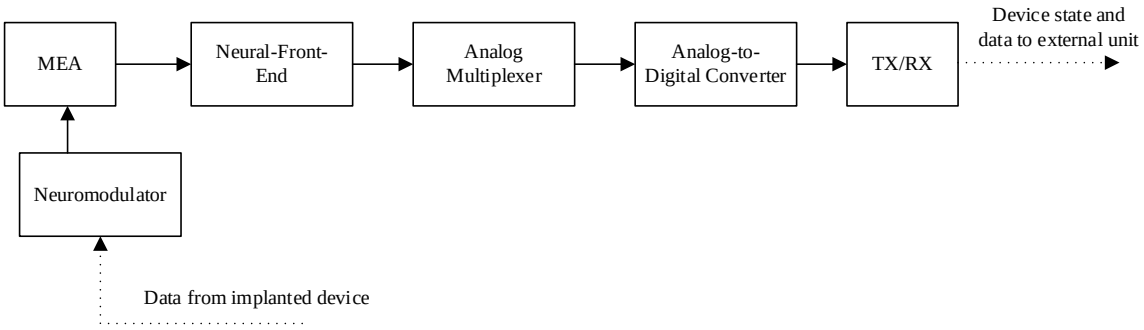


Figure 2: Block diagram of a basic neuroelectronic circuit for monitoring and modulating neural activity

The neuroelectronic circuit is responsible for processing the weak neural signals captured by the array of electrodes in the MEA. In addition to the low strength of the sensed physiological signals, the recording electrodes may pick up many other unneeded interferences or artifact signals. Hence, a low-noise-amplifier (LNA) is necessary at the first stage of the neural signal processing block in order to amplify the weak neural signal level from sub-mV to 10's of mV, so that the later stages can have relaxed noise performance. Although the LNA can provide first order low pass filtering, dedicated band-pass filters are used to (1) reject the out-of-band LFPs (high pass), and (2) prevent aliasing (low pass). The high pass cut-off frequency is typically set between 100-300 Hz and low pass cut-off frequency is between 3- 10 kHz. A dedicated unity-gain-buffer may be used before the next stage of neural signal processing which is the analog multiplexer. The low-noise-amplifier (LNA), the band-pass filter (BPF) and the unity-gain-buffer (UGB) create the neural-front-end also referred to as the NFE.

The next stage is the analog multiplexer which communicates the neural signals from the NFE to the analog-to-digital-converter (ADC) to obtain a digital version of the

captured physiological signal. The main design parameter for ADC is the resolution and sampling rate which is typically 8-10 bits and 16-32kS/s respectively [24]. Next, this digital data is processed by a microprocessor, typically located on the exterior of the patient's body and is then transmitted to an external monitoring and recording device.

CHAPTER 3: DESIGN OF FAULT-TOLERANT MULTI ELECTRODE ARRAYS (MEAs)

This chapter presents fault-tolerant solutions for multi electrode arrays (MEAs) based on hardware redundancy, wherein the goal is to detect and locate a faulty primary module and reconfigure the MEA after isolating and replacing the faulty primary module with a working spare module. For simplicity, a modular design is considered, where a an MEA grid comprises of sensing electrodes and its accompanying signal conditioning and processing circuitry, and is considered to be a single module on the grid. This circuitry may be connected to additional modules for computation, communication and intervention.

This type of reconfiguration strategy is appropriate since recent observations indicate surprising amount of redundancy within the spatial representation of information on the cortex and in sub-cortical structures. Based on these we consider the spatial structure to take the form of a neuronal ensemble or network structure [2], as opposed to discrete representation. Thus, the quality of information extracted from the measurements after reconfiguration will not be compromised. The term *fault detection* in this article is defined as the process by which it is recognized that a fault has occurred in the system under analysis. *Fault location* is defined as the process of determining where the fault has occurred within the system and *reconfiguration* is defined as the process of isolating a faulty component from the remainder of the system and restoring the system performance to an acceptable level of operation. The two fault-tolerant techniques discussed in this work follow a hardware redundancy approach for fault-tolerance by incorporating redundant

modules within the implantable device. In the first approach spare rows and/or spare columns are placed around the electrode grid array while in the second approach spare modules are integrated within the grid based on a defined geometry. The fault-tolerant methods are designed with cold spare modules, where a spare module is switched on only if it is brought on-line during reconfiguration. Cold spare reconfiguration helps conserve power, facilitate thermal management, and increase the efficiency of the implantable device.

3.1. Row or Column Redundancy

We assume the implanted MEA consists of *n* rows and *m* columns of primary modules as shown in Figure 3. In the first solution, we will incorporate *s* columns of spare modules in addition to the primary modules.

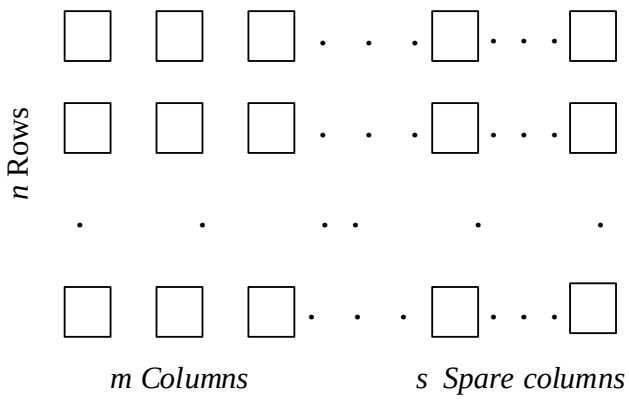


Figure 3: An n-by-m array of modules with s spare columns placed to the right of the array of primary modules.

The motivation for this solution is derived from [63], [64], [65], [66]. The spare columns or rows can be located at the edge of the MEA or within the MEA. Here, for simplicity of exposition, it is assumed that spare columns are located at the right edge and spare rows, if incorporated in the design, are located at the bottom edge of the MEA. Once a faulty primary module is identified a reconfiguration process is initiated in which the faulty module is replaced by its nearest fault-free spare neighbor on the right. Under this

reconfiguration scheme, sensor (*i*, *j*) can be connected to one of the following modules: (*i*, *j*), (*i*, *j+1*), … (*i*, *j+s*), where *s* is the number of spare columns. To evaluate the reliability of the system it is assumed that the system is operating in the useful life phase of the bathtub curve [29]. In this piece of work, the failure rate, that is failures per unit time, is considered to have a constant value, λ. Under this assumption it can be shown that the reliability of each module is given by the following equation:

$$R_m(t) = e^{-\lambda t} \qquad \text{Equation (1)}$$

This exponential relationship between module reliability and time is known as the exponential failure law. It states that when the failure rate function is a constant, reliability is proportional to a decaying exponential as a function of time. If the MEA can tolerate *r* failed modules, for the (*m* + *s*) modules in each row, where (*r* < *m* + *s*), then the reliability of each row of modules is

$$R_{row}(t) = \sum_{i=0}^{r} \binom{m+s}{i} R^{m+s-i}(t)(1-R(t))^i \qquad \text{Equation (2)}$$

$$\text{where, } \binom{m+s}{i} = \frac{(m+s)!}{(m+s-i)!i!}$$

In this research it is assumed that module failures occur independently. If *k* rows have to be operational, where $k \leq n$, then the reliability of the MEA is

$$R(t) = \sum_{j=0}^{n-k} \binom{n}{j} R_{row}^{n-j}(t)(1-R_{row}(t))^j C \qquad \text{Equation (3)}$$

Where '*C*' represents the fault coverage.

Fault coverage, *C*, is a measure of system's ability to recover from faults and continue to operate correctly. It is expressed as the probability that the system recovers

from the fault given the existence of the fault. As an example, we simulated the performance of the proposed solution for a MEA with the number of rows fixed at 100 and fault coverage $C = 1$. In this evaluation, module reliability (i.e., the probability that primary module is working in the time interval (t_0, t), was assumed to be 0.9, and $k = n$, i.e. all the rows had to be operational. Figure 4 shows the reliability of MEAs with the number of columns ranging from 10 to 90 and redundancy ratio ranging between 0 and 0.5. As indicated above a higher redundancy ratio implies that a higher percentage of modules in the MEA are spares.

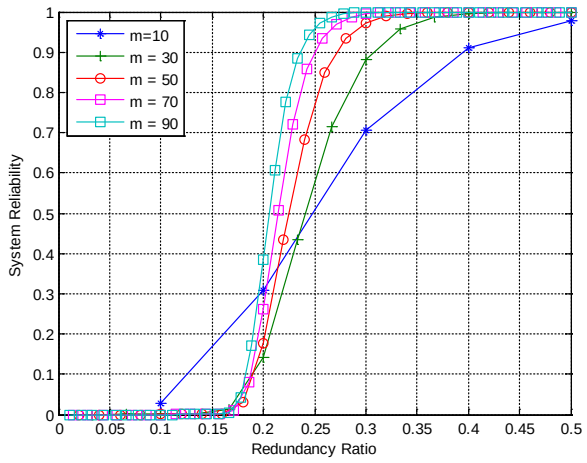


Figure 4: Reliability as a function of redundancy ratio for a fault-tolerant solution which incorporates spare columns in the MEA. Here the number of rows, $n = 100$, fault coverage $C = 1$, $k = n$, and module reliability is assumed to be 0.9.

For example, a redundancy ratio of 1 implies there is a spare module for each primary module. We observe that the reliability increases for a given redundancy ratio with increasing non-spare columns. This suggests that with this solution it is possible to create a highly reliable MEA using a lower percentage of spare modules. Spare columns are used in this solution for the above example. However, the method can be modified to incorporate both spare columns and spare rows. While the reconfiguration is systematic, i.e. a faulty module is replaced by the nearest fault-free module to its right (or below if spare rows are

used), the reconfiguration will likely involve replacement of several fault-free primary modules in addition to the faulty primary module. This increases the hardware overhead. In order to address this inefficiency, a second redundancy solution, known as interstitial redundancy, is discussed in the next section. This second design reconfigures a faulty MEA without reconfiguration of fault-free modules.

3.2. Interstitial Redundancy

Figure 5(a) shows a (*m*, *n*) array of primary modules (gray) where *m* is the number of rows and *n* is the number of columns. Embedded within this array of primary modules is an array of spare modules (black). The spare modules are placed in interstitial sites between primary modules. Such a fault-tolerant MEA architecture is referred as a (*s*, *p*) interstitial redundancy array (IRA). In a (*s*, *p*) IRA, each non-boundary primary module can be replaced by one of *s* spare modules and each non-boundary spare module can serve as a spare for *p* primary modules. IRAs can have a different degree of redundancy depending on the number and location of spare modules.

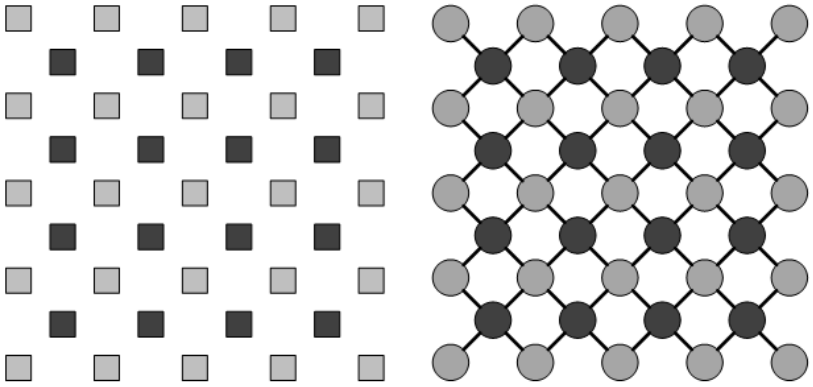


Figure 5: (a) An example of (4, 4) IRA with spare modules (black) at the interstitial sites of the primary modules (gray), (b) The corresponding graph model for the (4, 4) IRA shown in (a) where each node in the graph represents a primary or spare module. Note, in the graph representation each primary module is connected to the spare modules which can replace it, and each spare module is connected to the primary modules it can replace.

For example, consider the (4, 4) IRA shown in Figure 5(a) where each non-boundary primary module can be replaced by any one of the four available spare modules adjacent to it, and each spare module is available to its four neighboring primary modules. Furthermore, each of the four corner primary modules can be replaced by one spare module and the remaining boundary modules can be replaced by one of two spare modules. This relationship can be effectively captured by a graph model for this IRA. Figure 5(b) shows the graph model of the (4, 4) IRA shown in Figure 5(a). As before, gray nodes in the graph represent primary modules while black nodes represent spare modules. If a spare node can replace a primary node, then there is an edge between the two nodes in the graph. It can be observed that no two gray nodes are neighbors in the graph since a primary module cannot replace another primary module. Further, an undirected graph $G(V, E)$ is defined as a structure which consists of a set of vertices $V = \{v_1, v_2, \cdots\}$ and a set of edges $E = \{e_1, e_2, \cdots\}$ each edge e is incident to the elements of an unordered pair of vertices (u, v) which are not necessarily distinct.

3.3. Reconfiguration of Interstitial Redundancy Arrays

In the interstitial redundancy scheme of fault-tolerance design, we place spare modules in interstitial spaces of the MEA. This allows the use of a local approach for reconfiguration in the presence of faults. Here, when a faulty primary module is identified a reconfiguration procedure is initiated and the detected faulty primary module is replaced by an available neighboring fault-free spare module. The reconfiguration procedure that is employed to make the implantable system tolerant to faults is based on a graph matching approach. A *maximum matching algorithm* is used in this reconfiguration solution and is described in the next section.

3.4. Maximum Matching Algorithm

The replacement of a faulty primary module by a spare module can be performed in an optimum manner by using a maximum matching algorithm from graph theory [67]. The reconfiguration procedure can be further illustrated through an example. Consider, for example the (4, 4) IRA and its graph model shown in Figures 6(a) and 6(b), respectively. This is a 5 x 5 MEA with 16 spare modules arranged in a 4 x 4 array. Four of the primary modules are faulty and none of the spare modules are faulty.

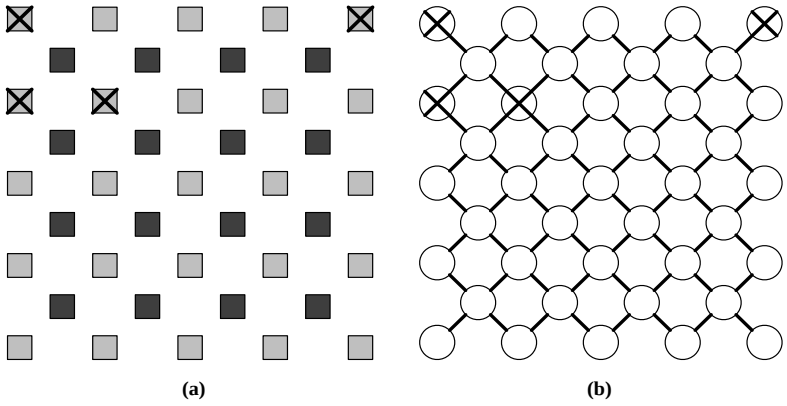


Figure 6: (a) A (4, 4) IRA with an example set of faults. Here, primary modules (1, 1), (2, 1), (2, 2), and (1, 5) are faulty. Faulty modules are marked with an 'X'. (b) The corresponding graph model for the (4, 4) IRA shown in (a).

Definition 1: Given an undirected graph G = (*V*, *E*), a matching is defined as a subset of edges $M \subseteq E$ such that for all vertices $v \in V$, at most one edge of *M* is incident on *v*. A vertex *v* is matched by matching *M* if some edge in *M* is incident on *v*; otherwise *v* is unmatched. And, an edge *e* is a free edge if and only if $e \notin M$.

Definition 2: A maximum matching is a matching of maximum cardinality, that is, a matching *M* such that for any matching M', $|M| \geq |M'|$.

From the graph model of an IRA (Figure 6(b)) a subgraph can be constructed consisting of nodes corresponding to faulty primary modules and spare modules that can potentially replace these faulty nodes as shown in figure 7(a). In this subgraph an edge

between a primary node and a fault-free spare node exists if and only if the spare node can replace the primary node. It can be observed that this graph is a bipartite graph since no two primary nodes and no two spare nodes are adjacent.

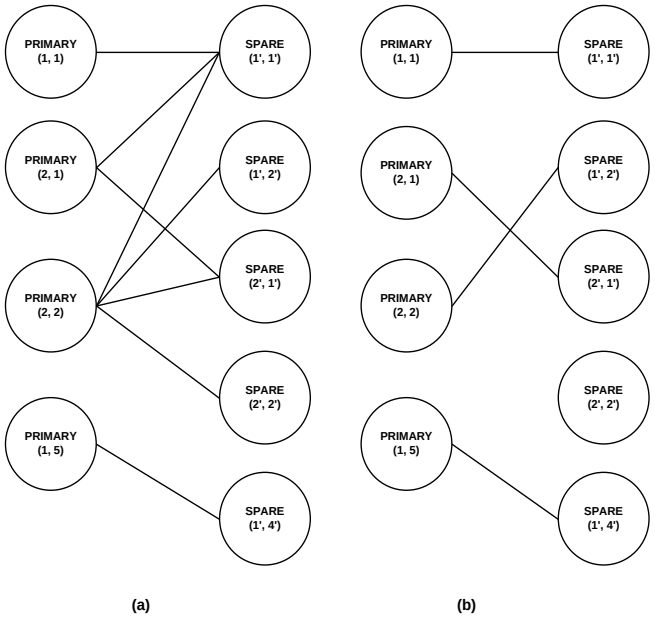


Figure 7: (a) A subgraph for the (4, 4) IRA with four faulty primary modules shown in Figure 6(a) and 6(b) and the spare modules which can replace the faulty modules. This sub-graph is a bipartite graph. (b) A maximum matching solution of the bipartite graph.

Definition 3: A bipartite graph is a graph in which $V = X \cup Y$ and $X \cap Y = \emptyset$ and each edge has one end vertex in X and one in Y.

For a given set of faulty primary modules, we can construct the bipartite graph of the IRA with the vertex set partition $\{X, Y\}$, and the edge set E, where X is the set of faulty primary nodes and Y is the set of all the neighboring fault-free spare nodes. Note, that in such a bipartite graph, any pair of matched vertices incident on an edge e, $e \in M$ will consist of one faulty primary module and one spare module such that the spare module corresponding to the matched node can replace the corresponding faulty primary module. It is evident from definitions 1 and 2 that the maximum matching involves finding δ, the maximum number of mutually disjoint edges in E, such that, no two edges share the same

node, implying that a spare module can replace no more than one primary module at any given time and a given faulty primary module cannot be replaced by more than one spare module. For this work, the interest is in determining if $\delta = |X|$ that is, whether every faulty primary module can be replaced by a fault-free spare module.

A maximum matching for a bipartite graph can be obtained using any method that is based on the following theorem.

Theorem 1: The number of edges in a maximum matching of a bipartite graph *G* is equal to the maximum flow, *F*, in its corresponding network, *N*(*G*) [67].

The key idea here is to construct a network *N*(*G*) whose directed graph $\bar{G}(\bar{V},\bar{E})$ is defined as follows:

$$\bar{V} = \{s,t\} \bigcup V, \qquad \text{Equation (4)}$$

And,

$$\bar{E} = \{s \to u \,|\, x \in X\} \bigcup \{y \to t \,|\, y \in Y\} \bigcup \{x \to y \,|\, x - y \text{ in } G\}. \qquad \text{Equation (5)}$$

There is an edge from node *s* to every node *x*, $x \in X$. Similarly, an edge exists from every node *y*, $y \in Y$ to node *t*. As an example, consider the (4, 4) IRA with four faulty primary modules (see figure 6(a)). The corresponding graph model is shown in figure 6(b). Bipartite graphs for the sub-graph containing the faulty primary nodes and connected spare nodes are shown in Figure 7(a) and Figure 7(b). The directed graph of the network *N*(*G*) is shown in Figure 8.

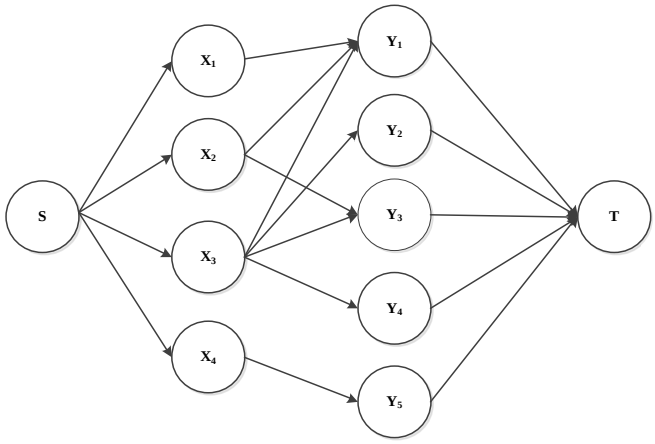


Figure 8: Directed graph of the network of the bipartite graph shown in Figure 7(a).

Any algorithm for maximum flow can be applied to the directed bipartite graph in Figure 8 to determine the maximum flow from *S* to *T* [68]. From Theorem 1 the maximum flow will give the maximum matching. For example, Dinic's algorithm for maximum flow, which runs in $O(\sqrt{V}E)$ when applied to the directed graph of Figure 8 leads to a maximum matching graph, such as the one shown in Figure 7(b).

A fault-identifying procedure is used to continuously examine module performance to detect a fault. Once a fault is detected a second algorithm may be used, if necessary, to locate the faulty module. These algorithms can run on a controller that is embedded in the fault tolerant MEA or implantable device or on an external computer which can communicate with the MEA. The location of a fault triggers the reconfiguration process wherein the faulty module is disconnected and replaced with a healthy and available spare module.

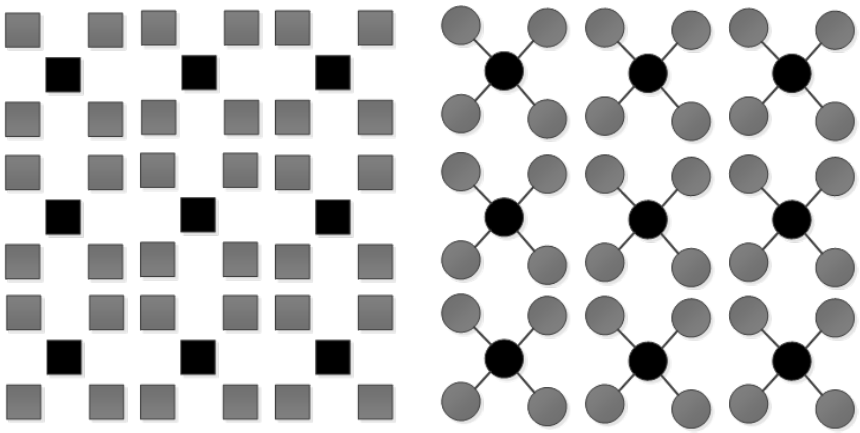
3.5. Reliability Analysis of Interstitial Redundancy Arrays (IRAs)

This section introduces four IRA designs with redundancy ratios ranging from 0.25 to 1.0. The reliability of the IRAs are then evaluated analytically to prove that an incorporating hardware redundancy will improve the dependability of the system. Each of

the IRA designs are compared with the other designs in terms of the reliabilities to conclude with the highest reliable design. Further in this chapter the reliability analysis is simulated for the 'best' possible IRA design.

3.5.1. Reliability Analysis of a (1, 4) IRA

In a (1, 4) IRA (Figure 9(a)) each primary module can be replaced by a spare module, while each spare module can replace one of four primary modules. The redundancy ratio for a (1, 4) IRA is 0.25.



(a) (b)

Figure 9: (a) An example of (1, 4) IRA with spare module (black) at the interstitial sites of the primary modules (gray), and (b) the corresponding graph model.

In this analysis, unless indicated otherwise, it is assumed that the primary and the spare modules have equal failure rates since both have the same structure and function. As indicated above, the failure rate for each module is considered to be a constant value, λ, with the reliability, R_m, specified by equation (1).

Let the grid of primary modules be of size m x n where m and n are even numbers. There are, then, mn clusters each with four primary modules and one spare module.

The reliability of each cluster is given by:

$$R_{cluster(1,4)}(t) = \sum_{i=0}^{1} \binom{5}{i} R_m^{5-i}(t) C\left(1 - R_m(t)\right)^i \qquad \text{Equation (6).}$$

Thus the reliability of a (1, 4) IRA of size $m \times n$ is given by

$$R_{(1,4)}(t) = \left(\sum_{i=0}^{1} \binom{5}{i} R_m^{5-i}(t) C\left(1 - R_m(t)\right)^i \right)^{\frac{mn}{4}}$$
$$= \left(R_m^5(t) + 5R_m^4(t)(1 - R(t)) \right)^{\frac{mn}{4}} \qquad \text{Equation (7).}$$

Where the fault coverage, C, is assumed to be 1.

Figure 10 shows the reliability of a (1, 4) IRA for different values of R_m and N, where $N = mn$. Compare the reliability of an N module redundant MEA with its corresponding N module MEA without redundancy.

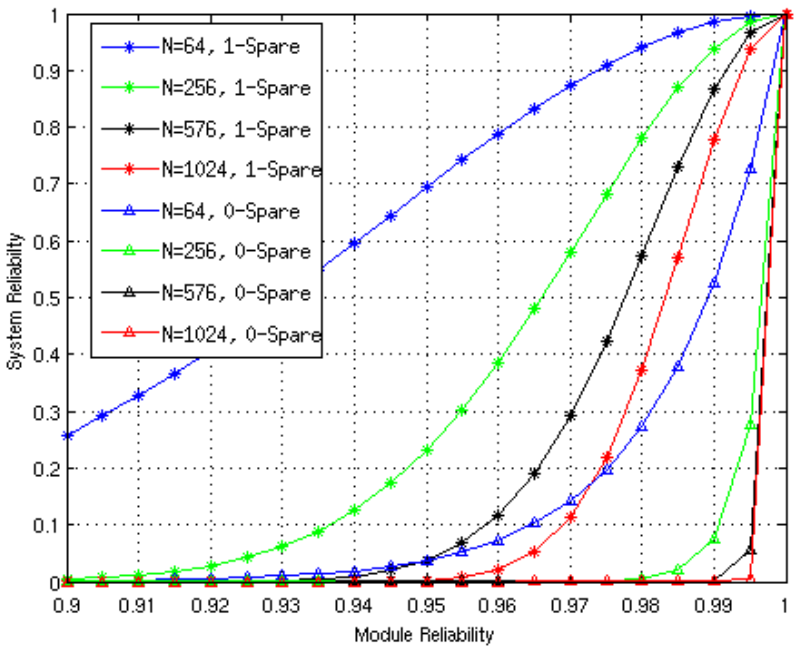


Figure 10: The reliability of (1, 4) IRA MEA with redundancy ratio of 0.25, $C = 1$, and $N = mn = 64$, 256, 576 and 1024. The (1, 4) IRA MEAs are compared to the corresponding MEAs without redundancy. It is evident that there is an increase in MEA reliability MEA reliability with the IRA solution.

It can be observed that interstitial redundancy improves MEA reliability. From the plots it may appear that the MEA becomes less reliable when the number of electrodes increases. This is true only when it is assumed that the MEA is considered to be operational when each cluster is operational, i.e., not more than one electrode can fail. However, it should be noted that the total number of faults tolerated are higher for larger MEAs. Moreover, if graceful degradation is acceptable, then larger systems tend to have better performance.

3.5.2. Reliability Analysis of a (1, 6) IRA

In a (1, 6) IRA (figure 11(a)) each primary module can be replaced by a spare module, while each spare module can replace one of six primary modules. The redundancy ratio for a (1, 6) IRA is 0.1667.

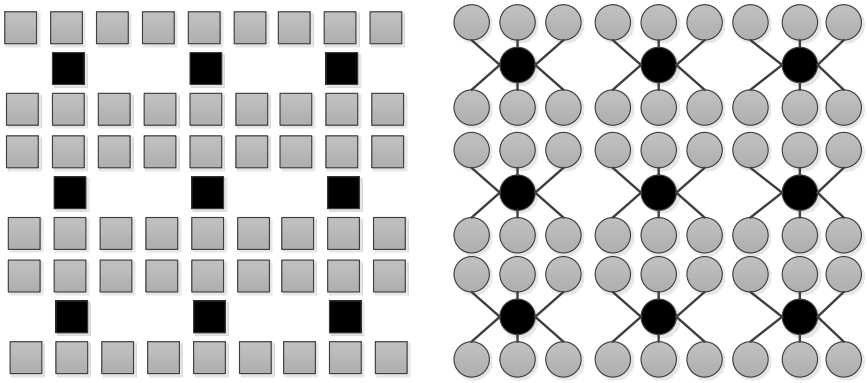


Figure 11: (a) (1, 6) IRA grid design, (b) the corresponding graph model. The gray nodes represent primary modules and the black nodes denote spare modules.

Like the (1, 4) IRA a (1, 6) IRA can be viewed as a combination of $N/6$ identical clusters where N is the number of primary modules in the system and it is an integral multiple of 6. Each cluster consists of 6 primary modules and one spare module. Reliability of each cluster is the likelihood of having at most one failed module among the seven modules in the cluster.

$$R_{cluster\,(1,6)}(t) = \sum_{i=0}^{1} \binom{7}{i} R_m^{7-i}(t) C\left(1 - R_m(t)\right)^i$$

Equation (8).

The reliability of the (1, 6) IRA scheme with N primary modules is given by:

$$R_{(1,6)}(t) = \left(\sum_{i=0}^{1} \binom{7}{i} R_m^{7-i}(t) c\left(1 - R_m(t)\right)^i \right)^{\frac{N}{6}}$$

$$= \left(R_m^7(t) + 7R_m^6(t)(1 - R_m(t)) \right)^{\frac{N}{6}}$$

Equation (9).

Figure 12 shows the reliability of (1, 6) IRA for different values of $R_m(t)$ and N, and compares with the reliability of the corresponding systems without redundancies. Once again, it can be concluded that adding interstitial redundancy has the potential to improve system reliability.

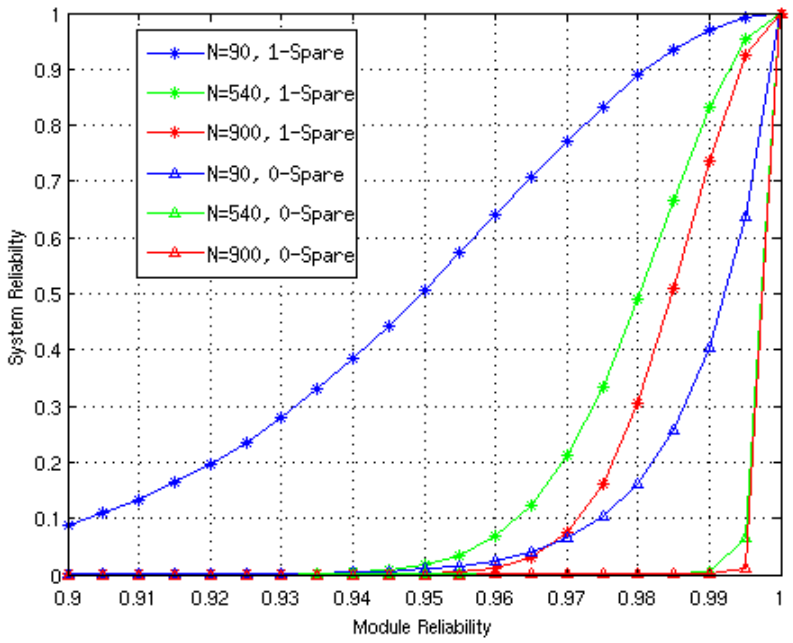
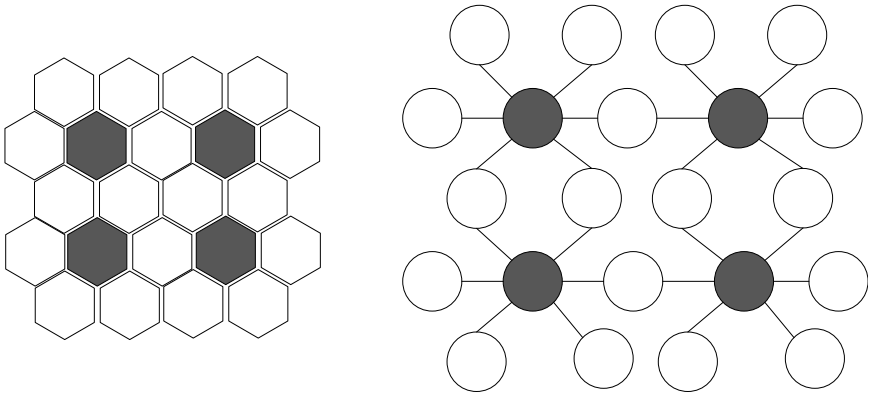


Figure 12: The reliability of (1, 6) IRA MEA with redundancy ratio of 0.1667, C = 1, and $N = mn$ = 90, 540 and 900 compared to the corresponding MEAs without redundancy.

3.5.3. Reliability Analysis of a (2, 6) IRA

Figure 13(a) represents the grid layout of a (2, 6) IRA configuration and figure 13(b) represents the corresponding graph model for the configuration. For fault-tolerant designs with higher redundancy ratio, such as the (4, 4) and (2, 6) IRAs, analytical modeling to determine the reliability of a system is not straightforward due to the complex assignment of spare modules. However, the cluster based technique used above for the (1, 4) and (1, 6) IRA designs can still be used to derive approximate expressions for MEA reliability.



(a) (b)

Figure 13: (a) (2, 6) IRA grid design, (b) the corresponding graph model. The gray nodes represent primary modules and the black nodes denote spare modules.

$$R_{cluster(2,6)}(t) = \sum_{i=0}^{2} \binom{8}{i} R_m^{8-i}(t) c\left(1 - R_m(t)\right)^i$$

Equation (10).

$$R_{cluster(2,6)}(t) = R_m^8(t) + 8R_m^7(t)(1 - R_m(t)) + 28R_m^6(t)(1 - R_m(t))^2$$

Equation (11).

Assuming that the (2, 6) IRA with N primary modules can be approximately divided into N/6 clusters, and the failures are independent, the reliability of the (2, 6) IRA system can be estimated by:

$$R_{(2,6)}(t) = \begin{pmatrix} R_m^8(t) + 8R_m^7(t)(1-R_m(t)) \\ +28R_m^6(t)(1-R_m(t))^2 \end{pmatrix}^{N/6} \quad \text{Equation (12).}$$

Figure 14 shows the reliability of (2, 6) IRA for different values of $R_m(t)$ and N, and compares with the reliability of the corresponding systems without redundancy. As expected, interstitial redundancy improves system reliability.

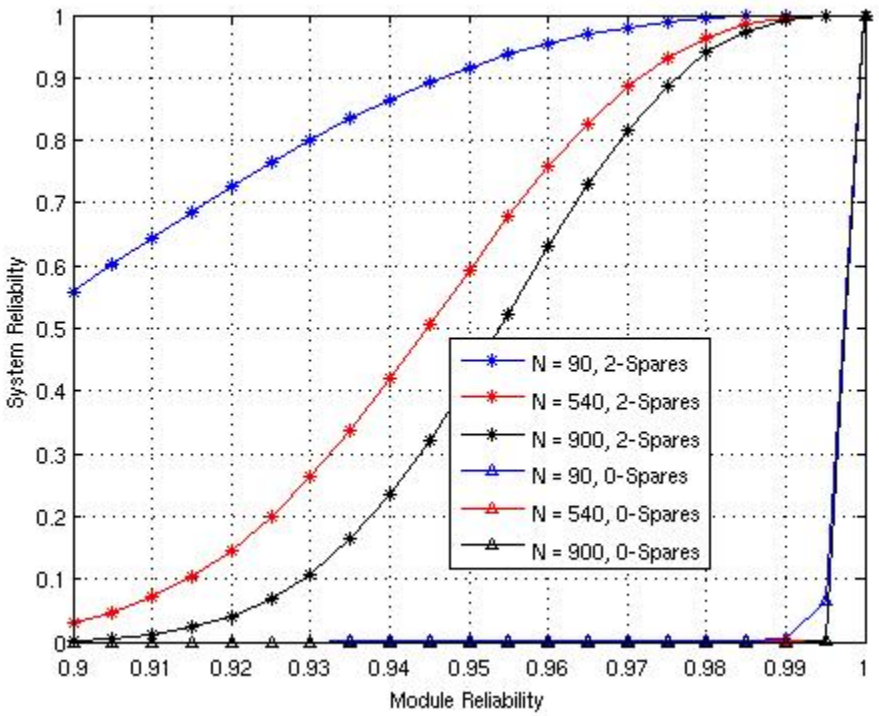


Figure 14: The reliability of (2, 6) IRA MEA with redundancy ratio of 0.33, C = 1, and N = mn = 90, 540 and 900, and the reliability of the corresponding MEAs without redundancy.

3.5.4. Reliability Analysis of a (4, 4) IRA

To analyze the reliability of a (4, 4) IRA design consider the IRA design of figure 5, where the redundancy ratio is 1.0. For a$m \times n$ (4, 4) IRA, the number of primary modules, p is mn and the number of spare modules, s is (m - 1)*(n - 1). The reliability, $R_{(4,4)}(t)$, of a (4, 4) IRA with fault coverage C can be approximated by equation (13) considering it as a *p-out-of-*(p + s) system, that is, an mn-out-of-(mn + (m-1)(n-1)) system:

$$R_{(4,4)}(t) = \sum_{i=0}^{s} \binom{s+p}{i} R_m^{s+p-i}(t) C\left(1 - R_m(t)\right)^i$$ Equation (13).

A second approximation introduced is that while four spare modules are available to replace each non-boundary primary module, each of the four corner primary modules can be replaced by only one spare module and each of the remaining primary modules on the boundary can be replaced with two spare modules. The corner modules can be considered as a 1-out-of-2 system. Thus, the reliability of the sub-system of four corner primary modules can be given by:

$$R_{corner(4,4)}(t) = \left(\sum_{i=0}^{1} \binom{2}{i} R_m^{2-i}(t) C\left(1 - R_m(t)\right)^i \right)^4$$ Equation (14).

Among the remaining boundary primary modules and their corresponding spare modules, there is one set of 2(*m* - 2) primary modules with 2(*m* - 3) spare modules and one set of 2(*n* - 2) primary modules with 2(*n* - 3) spare modules. The reliability of the sub-system consisting of these modules can be approximated by 2(*m* - 2) out-of-(4*m* - 10) and 2(*n* - 2) out-of-(4*n* - 10) systems. Thus, the reliability of such a subsystem is given by equations (15), (16) and (17):

$$R_{boundary(4,4)}(t) = R_{boundary1(4,4)}(t) R_{boundary2(4,4)}(t)$$ Equation (15).

Where,

$$R_{boundary1(4,4)}(t) = \sum_{i=0}^{2(m-3)} \binom{4m-10}{i} R_m^{4m-10-i}(t) C\left(1 - R_m(t)\right)^i$$ Equation (16).

And,

$$R_{boundary2(4,4)}(t) = \sum_{i=0}^{2(n-3)} \binom{4n-10}{i} R_m^{4n-10-i}(t) C\left(1 - R_m(t)\right)^i$$ Equation (17).

Finally, the reliability of the sub-system consisting of the remaining set of (m - 2)*(n - 2) primary modules with (m -3)*(n - 3) spare modules can be approximated as a (m - 3)*(n -3) out-of-(2mn - 5m - 5n + 13) system, given by:

$$R_{other(4,4)}(t)=\sum_{i=0}^{(m-3)(n-3)}\binom{2mn-5m-5n+13}{i}R_m^{2mn-5m-5n+13-i}(t)C\left(1-R_m(t)\right)^i$$

Equation (18).

Thus, the reliability of a (4, 4) MEA can be obtained by combining all the sub-system reliabilities, as shown in (19):

$$R_{(4,4)}(t)=R_{corner(4,4)}R_{boundary1(4,4)}R_{boundary2(4,4)}R_{other(4,4)}$$

Equation (19).

Figure 15 shows the reliability of a (4, 4) IRA for different values of R_m and N, and compares it to the reliability of the corresponding MEA without redundancy.

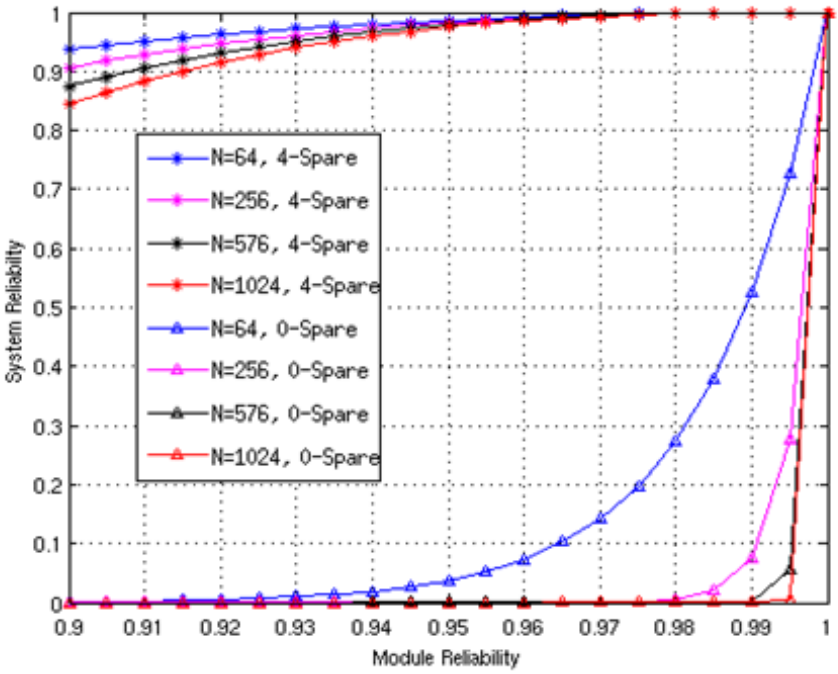


Figure 15: The reliability of (4, 4) IRA MEA with redundancy ratio of 1, C = 1, and N = mn = 64, 256, 576 and 1024 compared to the corresponding MEAs without redundancy.

3.5.5. Comparing the System Reliabilities of (1, 4), (1, 6), (2, 6) and (4, 4) IRA MEA Designs

Figure 16 shows the effect of module reliability on the system reliability of (4, 4), (2, 6), (1, 4) and (1, 6) fault-tolerant MEA designs with primary modules '*N*' = 64 and a fault coverage, *C* of 1.

From figure 16 it can be concluded that the system with a higher level of redundancy, such as the (4, 4) IRA, should be used when module reliability is low while systems with lower redundancy can be used when module reliability is high.

The IRAs considered here had redundancy ratios ranging from 0.16 to 1.0. We note that a redundancy ratio higher than one is possible (such an IRA would have more spare than primary modules), and the design and analysis developed here can be readily extended to such IRAs. Further, as indicated above, we have considered a MEA to be fault-free after reconfiguration if the number of working modules used is equal to the number of primary modules. However, a higher value of reliability can also be obtained if a smaller number of working modules suffices to achieve the desired function, that is, a graceful degradation of MEA function is acceptable.

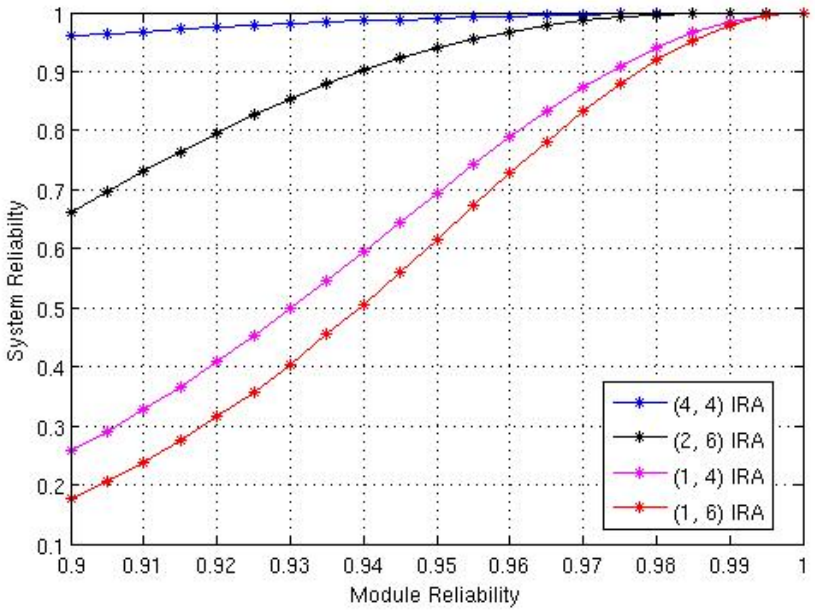


Figure 16: Reliability comparison of (4, 4), (2, 6), (1, 4), and (1, 6) IRA designs with N = 64 and C = 1 for different values of module reliability.

Further analysis suggests that, given a situation where the fault coverage, C, is less than 1, the fault-tolerant system continues to perform better than a system without redundancy. Figure 17, shows the reliability analysis of different IRA designs with 64 primary modules for C = 1, 0.90 and 0.80. It can be noted that a system with higher fault coverage factor should be used with lower sensor module reliability and a system with lower fault coverage factor could be used when the sensor module reliability is high to achieve desired level of overall reliability.

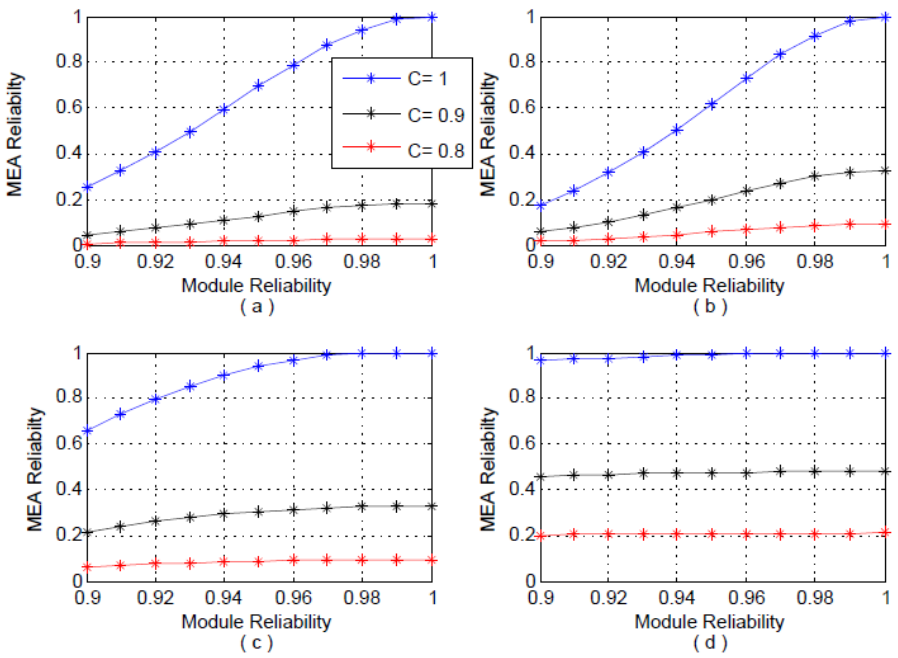


Figure 17: Reliability comparison of a different IRA design with coverage factors C =1, 0.9, and 0.8 and varying module reliability in a MEA of size N = 64. (a) (1, 4) IRA design, (b) (1, 6) IRA design, (c) (2, 6) IRA design, (d) (4, 4) IRA design.

3.5.6 Simulating a (4, 4) IRA MEA

An extended simulation of the (4, 4) IRA MEA solution is presented in Figures 18 and 19. In this simulation random faults were injected in both primary and spare modules of the MEA and using the fault-reconfiguration algorithm the MEA was reconfigured. The evaluation corresponding to each data point is repeated 15 times, and then the percentage of instances that resulted in a successful reconfiguration of the MEA was determined. A successful reconfiguration implies that each failed module could be replaced by a functioning spare. Figure 18 shows the effect of faults in primary and spare modules of a (4, 4) IRA, with MEA sizes N = 64 and 100. The percent system reconfiguration obtained is plotted as a function of percentage of faulty primary modules with the percentage of faulty spare modules varying from 0 to 65%. Faults were injected in a random pattern within the IRA, and the simulation was run to compute the percentage of fault

reconfiguration using the maximum-matching algorithm, as described in Section 3.4. Though this analysis is performed for the (4, 4) IRA, the results can be easily extended to other IRA configurations.

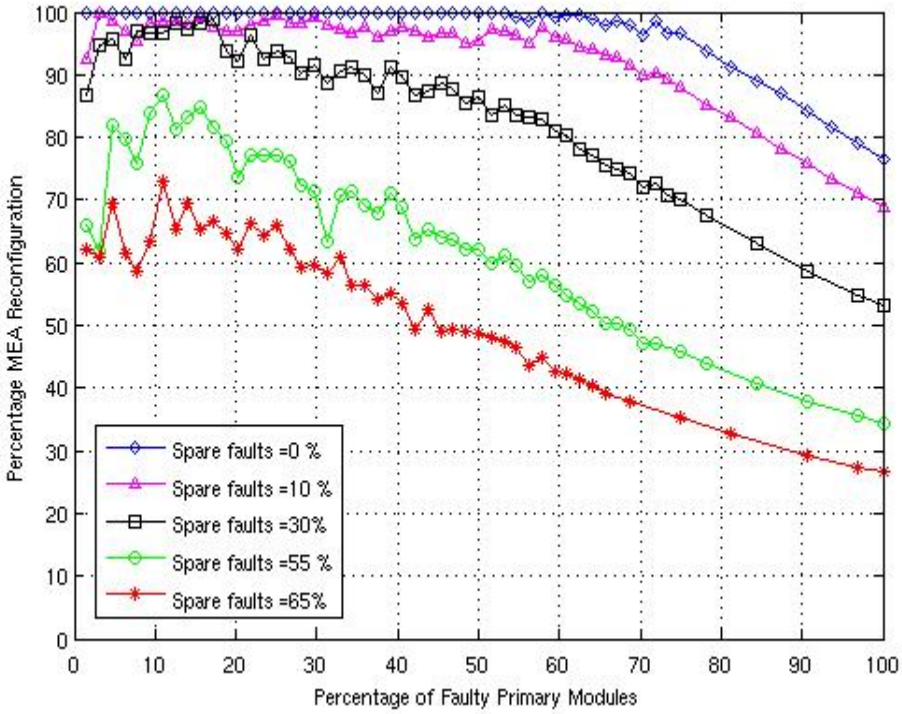


Figure 18: Simulation of fault reconfiguration for a (4, 4) IRA with for s = 64, with a fault coverage factor of C = 1

Observing Figures 18 and 19, it is evident that there is a steady decrease in percentage MEA reconfiguration with increasing percentage of primary faults. A (4, 4) IRA MEA can tolerate a large number of faults and continue to be fully functional. As the number of faults increases there is a graceful degradation in the capability of the MEA.

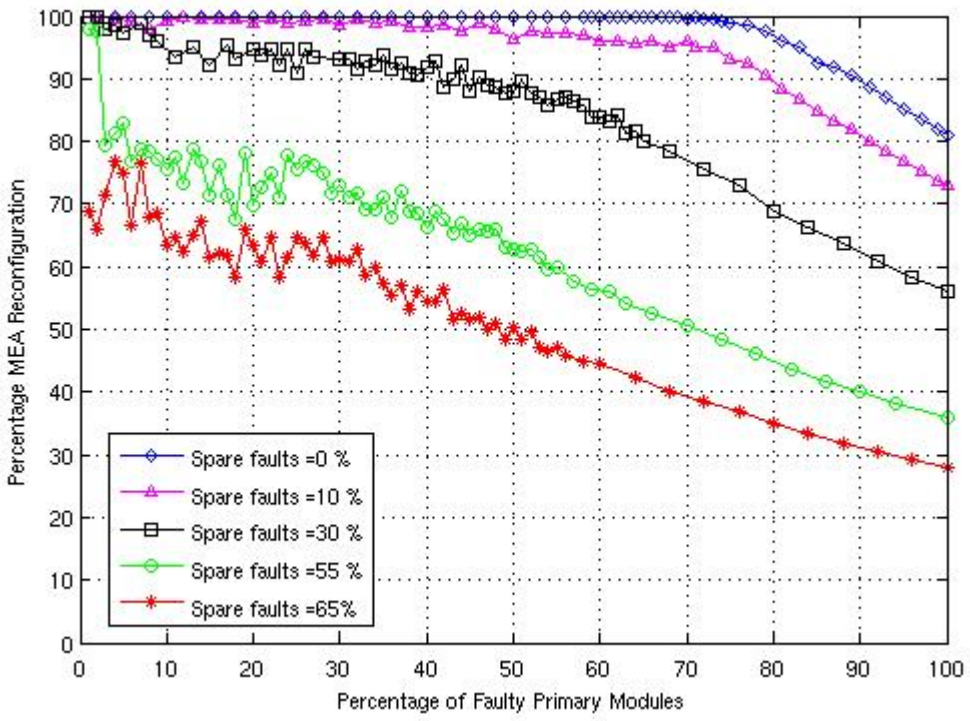


Figure 19: Simulation of fault reconfiguration for a (4, 4) IRA with for $N = 100$, with a fault coverage factor of $C = 1$

It can be noted that the percent fault reconfiguration has a higher variance when the percentage of primary faults are low and percentage of spare faults are high as compared to the case when the percentage of primary faults are high and the percentage of spare faults are low. This is because in the presence of spare faults the percentage MEA reconfiguration varies depending on the spatial relationship between primary and spare faults. If most of the faulty primary sensors are surrounded by faulty spare sensors, the MEA reconfiguration encounters a 'worst-case' scenario. In contrast if most of the faulty primary sensors are surrounded by healthy spare sensors the system reconfiguration encounters a 'best-case' scenario. Due to these two extreme cases, the variance in the average MEA reconfiguration is much higher when the percentage of spare faults is considerably greater than the percentage of primary faults. We can also observe that percentage MEA reconfiguration is

nearly 90% when spare faults are between 0-30% and primary faults are between 0 and 50%. With increasing percentage of spare faults there is a decrease in MEA reconfiguration as may be expected. When the number of primary faults is greater than 50%, we observe, in Figures 18 and 19, a decrease in the variance of the average MEA reconfiguration. This is because as increasing numbers of primary modules become faulty there is a decrease in the difference between the best-case and the worst-case scenarios. Eventually, the variance in MEA reconfiguration minimizes. However, it is important to note that the proposed MEA offers better reliability (percent system reconfiguration ≈ 30%) even with a high percentage of spare faults (≈ 65%) and very high primary faults (≈ 90%), as compared to a MEA without redundancy.

3.6. Design Summary

The two fault-tolerant solutions have different degrees of reconfiguration complexity and overhead. The reconfiguration strategy for the row or column based solution is simple. It does not require, for example, a graph based matching to obtain a result. The reconfiguration for the spare row or column solution may require replacement of fault-free modules. The reconfiguration for the interstitial redundancy array is more complex; however, it does not involve replacement of fault-free modules. A fault tolerant scheme can also be proposed where row or column based and interstitial redundancy can be used together. That is, the difference in complexity and overhead of the two solutions can be used to advantage.

The fault-tolerant strategies described in this Chapter are developed for a 2D MEA. However, these solutions can readily be extended to other form-factors. For example, the concepts described here can be extended to a linear MEA with spare sensors integrated

with primary sensors on the linear array. The concepts described here can also be extended to the inner or outer surface of a tube. To do this we consider a fault tolerant sensor array to be placed on a 2D rectangular surface as described here. This rectangular surface can then be considered to be rolled so that two opposite edges of the 2D rectangular surface touch each other. A surface rolled in this manner will form a tube. The sensing array may be placed on the inner and/or outer wall of this tube. The concepts developed here can also be extended to the surface of other 3D structures such as a sphere with primary and spare sensors placed at different latitudinal or longitudinal points on the surface of the sphere. The reconfiguration algorithm described here can readily be extended to these non-2D form factors so that there is continuity across the entire surface of sensors.

CHAPTER 4: DESIGN OF A FAULT-TOLERANT BRAIN IMPLANTABLE DEVICE

An ideal brain implantable device or a brain-machine interface should include a neural signal processing block that assists in recording and monitoring the underlying neural activity and a neuromodulator which if required, can trigger a signal to stimulate the underlying brain tissue or deliver drugs locally to intervene an undesirable neural activity such as a seizure. Therefore, a brain implantable device should include (i) electronic circuits that can assist in processing and recording the weak neural signals captured by the array of electrodes in the implanted multi-electrode array (MEA) and (ii) a logic block which can analyze the incoming signals and trigger an intervening mechanism deliver local drugs to stall the progression of harmful neural progression.

A block diagram of a typical neural signal monitoring and modulating circuit has been discussed earlier in figure 2, Chapter 2. Referring to figure 2, it is evident that the neural activity monitoring occurs in the following three blocks: (1) the neural-front-end (NFE); (2) the analog multiplexer; (3) and the analog-to-digital-converter (ADC). The NFE includes a low-noise-amplifier (LNA) to provide a first level of amplification to the weak neural signals, a band-pass filter to select the frequency band of signals that are of interest and a unity gain buffer to further amplify and strengthen the weak neural signals that are required for monitoring and hence need further processing. Figure 20 represents a block diagram of a brain implantable device that includes real-time neural signal monitoring and modulating blocks, comprising of an array of electrodes (MEA), an amplifying and

filtering unit (NFE), a digitizing unit (ADC), and a logic block that acts upon data received from the implanted device to execute neural signal intervention in order to subside a potentially harmful neural activity.

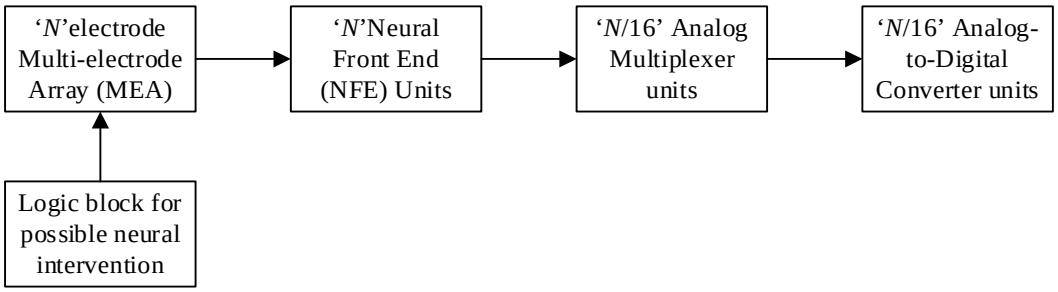


Figure 20: Block diagram of a brain implantable device with neural signal monitoring and modulating or neural intervening capability.

In this architecture, for an '*N*' electrode multi-electrode-array (MEA), where '*N*' is the number of electrodes in the MEA, the neural signal processing block consists of '*N*' neural-front-end units. According to earlier IC designs to observe brain activity [69], demonstrates that, each electrode is designed to have its own dedicated neural-front-end unit to process the weak neural signals captured by the respective electrodes instead of using an analog multiplexer to timeshare a single amplifier between multiple electrodes.

The key motivation behind allocating each electrode with its own dedicated low-noise-amplifier is that the time constants inherent in the amplifier dynamics are typically much longer than the multiplexer switching time required catching the brief neural activity across an array of many electrodes. Another piece of literature which focuses on optimizing the power and area in the design of *in vivo* integrated neural systems [60], demonstrate that irrespective of the circuit topology and process technology used in the design of such systems the optimal multiplexing ratio which makes the systems power-area product minimum is 16. Hence, to achieve an area-power optimal design, this work includes one

multiplexing unit and one ADC for every 16 electrodes the basic brain implantable system design. Figure 20 represents this for an '*N*' electrode brain implantable system, i.e. for a system with '*N*' electrodes in the multi-electrode array; the minimum area-power product in the design can be achieved with '*N*/16' analog multiplexers and '*N*/16' analog-to-digital converters.

Recent years has witnessed a growing demand for small size, low-power, and ambulatory physiological signal acquisition system. And, the rapid CMOS scaling that has been taking place in the semiconductor technology arena, has assisted in achieving such a low-power-small-size wireless neural monitoring device. However, in an era of extreme CMOS scaling, reliability issues are becoming a critical problem. Device reliability issues such as bias temperature instability, hot-carrier injection, time-dependent dielectric breakdown of gate-oxides, and interconnect reliability concerns such as electromigration pose serious concern for devices that are intend to operate continuously for long periods of time, i.e. in terms of years and decades. Being classified as critical devices, it is imperative for brain implantable systems to incorporate some form of fault-tolerance such that in case of failure in any component of the device, the system will have an option to degrade gracefully instead of an abrupt system failure leading to total loss of data/recording resulting in dire consequences such as re-surgery to replace the implanted device.

This chapter proposes three different fault-tolerant architectures for the neural signal processing block of brain implantable devices that are used to monitor real-time neural signals continuously for long periods of time. The motivation behind each of the 3 fault-tolerant architectures for the neural signal processing block is also discussed. A

hardware redundancy approach is employed in making the processor fault-tolerant, thereby enhancing the overall dependability of the implantable device. The proposed designs can be broadly divided into 2 categories: (i) 'Fault-tolerant Architecture Design 1' includes hardware redundancy in the sensing layer of the implantable device and (ii) 'Fault-tolerant Architecture Design 2' and 'Fault-tolerant Architecture Design 3' include hardware redundancy in the neural signal processing layer of the implantable device.

As discussed earlier in the motivation of this work the future brain implantable devices will aim at recording and monitoring continuous neural data instead of recording only certain events. This is important for predicting and impeding an impending seizure activity. Hence, to record the entire bandwidth of a certain type of neural signals we need to decide the number of bits that will be required by the ADC blocks and the approximate sampling rate. For example if the target signal bandwidth to record are ECoG signals which are typically between 0-500 Hz, to meet the Nyquist criteria let us assume that the sampling frequency is 1.6 KHz, which is slightly greater than the Nyquist frequency of 1 KHz. Each ADC digitizes signals from 16 electrodes i.e. each ADC has 16 input channels hence the sampling rate per channel will be 16 * 1.6 KHz, i.e. equal to 25.6kSamples/sec. Assuming the ADC resolution required is 0.1µV, with an input voltage range of +/- 50µV to +/- 100µV, i.e. implying a $200\mu V_{peak\text{-}to\text{-}peak}$ the minimum number of bits required by the ADC can be calculated by the following equation: $V_{resolution} = \frac{V_{peak-to-peak}}{2^{Number\_of\_Bits}}$. Working with the above values in the equation for $V_{resolution}$, it can be calculated that the minimum *number of bits* required to record a fairly continuous ECoG signal is 11 bits. Hence, a 12 bit ADC is considered for all further analyses that is included in this work.

The type of brain implantable device discussed here consists of two major functional blocks: (1) the neural signal processing block, a unit that is possibly housed within the cranium or on/near the brain tissue and hence has severe area and power restrictions and prone to a higher failure rate than (2) the intervening logic block, which is placed near the neural signal processing block but is located on the exterior body of the patient, and hence is excluded from the severe area-power restrictions as faced by the internally implanted neural signal processing block. Evidently, to support the implantable device in case of a fault in the neural signal processor the design needs to include fault-tolerant features, such as, logic for fault-detection and fault-diagnosis and a mechanism such as an analog switch network to disconnect a failed circuit for a possible system reconfiguration after a fault has occurred. In case of a failure in any of the major functional blocks the neural signal monitoring system will fail to operate as expected. For example, if the ADC block fails, it is likely that the entire implantable device will fail to monitor the underlying neural activity and hence it will be necessary to replace the implanted device with a new one. To overcome this inability to tolerate component failures at the functional level fault-tolerant mechanisms via hardware redundancy within the implantable device is discussed in sections 4.1., 4.2., and 4.3. Section 4.4., describes a current generation patented brain implantable design which will be used as a benchmark design to compare and analyze the 3 proposed fault-tolerant designs with respect to the benchmark design in terms of the performance parameters which are, the system reliability, the area and the active power used by the proposed fault-tolerant implantable designs versus the design described in the benchmark.

4.1. Fault-tolerant Architecture Design 1

The multi-electrode array or MEA block of the brain implantable architecture consists of arrays of sensors or electrodes that capture the underlying neural signals. The current available and proposed MEA designs do not include any techniques to make this block fault-tolerant. Faults in the MEA can occur because of sensor failure due to mechanical stress on the sensor or the connecting wires during surgery to place electrodes or due to stress from changes in the brain and the surrounding milieu thereafter. Electrode failure can also arise due to the brain tissue response to chronically implanted sensors possibly resulting in encapsulation of a sensor due to gliosis [26], which can further lead to neuronal death at the sensing. In case of sensor failure in the MEA, the neuronal activity will not be captured correctly thereby impairing the purpose of the implantable device. Hence, to enable the implanted device to function properly we introduce the idea of including spare electrodes in the multi-electrode array (MEA) to incorporate fault-tolerance in the sensing layer. Chapter 3 discusses four types of fault-tolerant MEA designs that includes four different levels of redundancy ratios. Though the (4, 4) IRA MEA with a redundancy ratio of 1 is considered in this section and in sections 4.2., and 4.3., for MEA design of the proposed fault-tolerant architectures, other IRA designs can also be adopted to design the MEA in the fault-tolerant architectures.

In this work, the ‘Fault-tolerant Architecture Design 1’ is described as a brain implantable device in which the multi-electrode array includes fault-tolerance capability, as shown in the block diagram in Figure 21. The blocks with ‘bold’ outer line are the major functional blocks of the system which either captures the neural signal or processes it for further evaluation/monitoring. The analog switch network assists in

disconnecting a faulty electrode from the rest of the system and replaces it with a healthy spare electrode. This design has no fault-tolerance capability within the neural signal processor block of the implanted device, i.e. any failure in the neural signal processing block can affect the functioning of the implanted monitoring system if the device is not replaced with a properly functioning unit. A logic block to detect and diagnose faults in the fault-tolerant MEA block is required which will send information regarding faulty electrodes if any, and information about available spare electrodes that will replace the faulty electrodes in an optimal way, to the analog switch network that will then proceed with the MEA reconfiguration. This logic block is proposed to be a part of future work in this research.

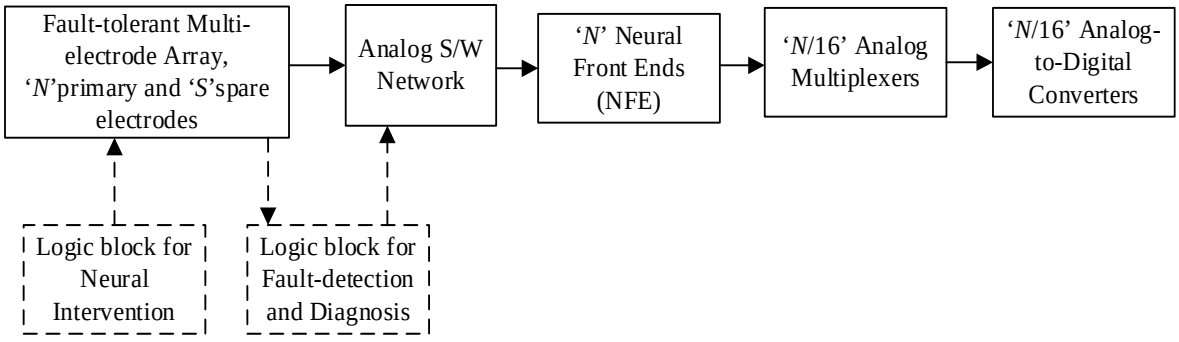


Figure 21: Block diagram for the Fault-tolerant Architecture Design 1.

The reliability of a system described by the Fault-tolerant Architecture Design 1, for a (4, 4) IRA MEA is given by the following equation:

$$R_{FT-Architecture1}(t) = R_{(4,4)\text{MEA}}(t) * R_{switch\_network}(t) * R_{NFE\_\text{block}}(t) * R_{MUX\_\text{block}}(t) * R_{ADC\_\text{block}}(t)$$

$$R_{FT-Architecture1}(t) = R_{(4,4)\text{MEA}}(t) * R_{switch\_network}(t) * R_{NFE}^{N}(t) * R_{MUX}^{N/16}(t) * R_{ADC}^{N/16}(t)$$

Equation (20)

Where,

$R_{(4,4)MEA}(t)$ is given by equation (19) in Chapter 3, for an '*N*' electrode multi-electrode array brain implantable device.

4.2. Fault-tolerant Architecture Design 2

The neural signal processing block in a brain implantable device can be broadly divided into 3 major functional units: (i) the Neural Front End, (ii) the Analog Multiplexer, and (iii) the Analog-to-Digital Converter. The abstraction layer to incorporate hardware redundancy in the processing block is at the component level where fault-diagnosis and fault recovery can be attained with least complexity as compared to cases where the entire device has to be replaced by re-surgery. The fault-tolerant architecture design 2 incorporates redundancy in the NFE unit of the neural signal processing layer in the implantable device in addition to the redundancy in the MEA or the sensing layer of the device. Figure 22 represents a block diagram of the proposed fault-tolerant design.

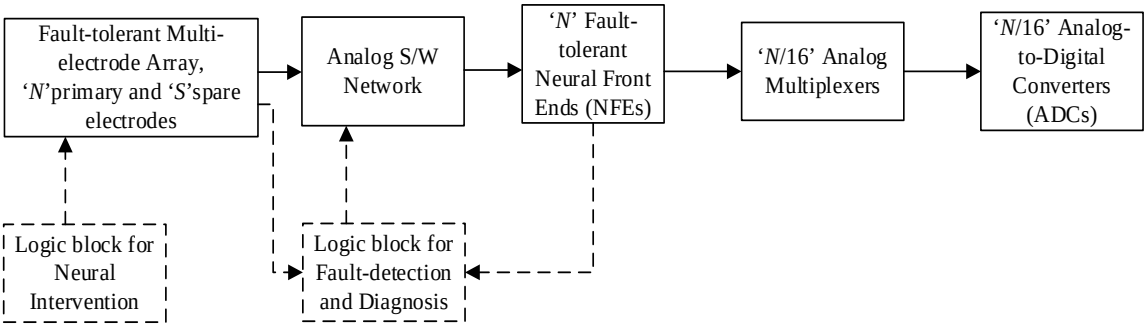


Figure 22: Block diagram for the Fault-tolerant Architecture Design 2

The neural-front-end (NFE) is responsible for amplification and filtering the weak neural signals captured by the MEA, therefore a failure in the NFE unit will eventually lead to device failure. With the presence of one or more redundant NFE units for every primary NFE unit, the fault-tolerance mechanism will trigger a reconfiguration

of the faulty NFE unit via the 'fault-detection and diagnosis' block and the analog switch network which will disconnect the faulty NFE unit and connect a 'healthy spare' of the NFE unit to the system. We can have more than one type of this architecture design by altering the degree of redundancy in the NFE unit. For example, in a 1:2 NFE redundancy design, each primary NFE unit has two spare NFE units for possible reconfiguration. A 1:1 NFE redundancy design is considered in the system reliability analysis for the Fault-tolerant Architecture Design 2, for a (4, 4) IRA MEA is represented by the following equation:

$$R_{FT-Architecture2}(\mathrm{t}) = R_{(4,4)\mathrm{MEA}}(\mathrm{t}) * R_{switch\_network}(\mathrm{t}) * R_{NFE\_\mathrm{block}}(\mathrm{t}) * R_{MUX\_\mathrm{block}}(\mathrm{t}) * R_{ADC\_\mathrm{block}}(\mathrm{t})$$

$$= R_{(4,4)\mathrm{MEA}}(\mathrm{t}) * R_{switch\_network}(\mathrm{t}) * R^{N}_{1:1\_\mathrm{Redundant\_NFE}}(\mathrm{t}) * R^{N/16}_{MUX}(\mathrm{t}) * R^{N/16}_{ADC}(\mathrm{t})$$

Equation (21)

Where,

$$R_{1:1\_\mathrm{Redundant\_NFE}}(\mathrm{t}) = \sum_{i=0}^{1} \binom{2}{i} R^{2-i}_{NFE}(\mathrm{t}) * (1 - R_{NFE}(\mathrm{t}))^{i}$$

And, $R_{(4,4)MEA}(\mathrm{t})$ is given by equation (19) in Chapter 3, for an '*N*' electrode (4, 4) IRA MEA design.

4.3. Fault-tolerant Architecture Design 3

The next major complex functional unit that processes the underlying neural signals in the neural signal processor is the analog-to-digital-converter (ADC) unit. With the increase in scaling factor in the current CMOS technology in critical applications such as brain implantable devices, complex circuits are expected to be less reliable for longer periods of time. The Fault-tolerant Architecture Design 3 in addition to redundancy in the electrode array and neural-front-end units also includes redundancy and hence fault-

tolerance capability within the analog-to-digital converter unit of the neural signals processor as shown in Figure 23, such that the fault-tolerant mechanism can recover the system from any faults that occurs in the ADC unit of the system. However the degree of redundancy included in the ADC units may vary according to the constraints in the design parameters such as the area and power of the implantable system. For instance, an '*N*' electrode fault-tolerant MEA can have 1 or 2 spare ADC units depending on the design parameter limitations. With respect to the other fault-tolerant architectures that have been proposed in sections 4.1 and 4.2 of this chapter, this architecture design has the maximum degree of hardware redundancy and hence is expected to have the highest reliability factor among the 3 proposed designs.

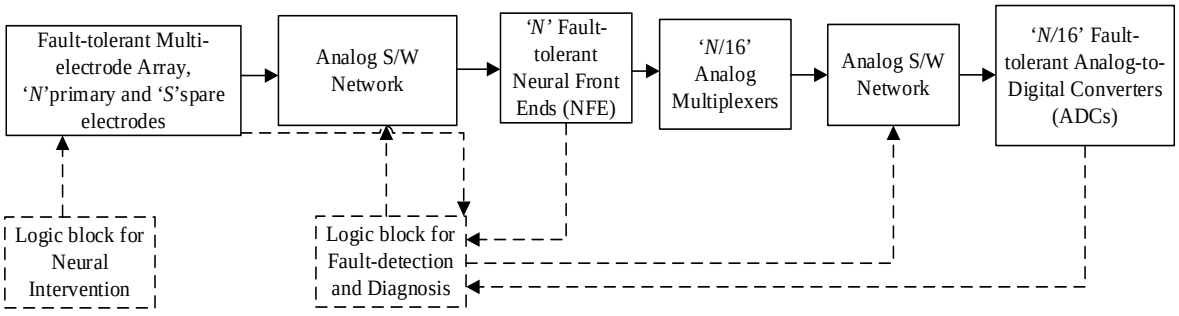


Figure 23. Block diagram for the Fault-tolerant Architecture Design 3

Note that the analog multiplexer unit does not include any hardware redundancy in any of the proposed fault-tolerant designs due to the following reasons: (1) the analog multiplexer unit is a relatively simple circuit compared to the neural-front-end and the analog-to-digital-converter units and hence expected to have a higher reliability per unit with respect to its NFE and ADC counterparts, (2) Faults in analog multiplexers may include faults in select lines and input and output lines. For an *m* X 1 multiplexing unit, failure in a single input channel will result in reconfiguring i.e. switching all '*m*' input lines in order to bring the spare multiplexing unit inline. This will involve replacing several

fault-free input lines which will cause design overkill and this will also increase the leakage power due to maximum switching being required even in the least required cases. This leakage power may in turn increase the device power requirements and the overall temperature of the implantable device which can affect the surrounding tissue (3) and, faults in a multiplexer will in most cases, lead to a graceful degradation in the overall system performance and not cause a sudden disruption of the functions of the implantable device.

We recognize that adding a spare ADC for each primary ADC unit in an '*N*' electrode implantable multi-electrode device might be expensive. Hence, the number of spare ADC units is kept flexible i.e. the degree of redundancy in this unit need not necessarily be 1, a less than 1 degree of redundancy may also contribute in increasing the reliability of the implantable device. Here, 'degree of redundancy' in a fault-tolerant architecture is the ratio of the number of spare units available per primary unit which is intended to be made fault-tolerant in the system. A 1:1 ADC redundancy design is considered in the system reliability analysis for the Fault-tolerant Architecture Design 3, for a (4, 4) IRA MEA, is represented by the following equation:

$$R_{FT-Architecture3}(\mathrm{t}) = R_{(4,4)\mathrm{MEA}}(\mathrm{t}) * R_{switch\_network}(\mathrm{t}) * R_{NFE\_\mathrm{block}}(\mathrm{t}) * R_{MUX\_\mathrm{block}}(\mathrm{t}) * R_{ADC\_\mathrm{block}}(\mathrm{t})$$

$$= R_{(4,4)\mathrm{MEA}}(\mathrm{t}) * R_{switch\_network}(\mathrm{t}) * R^{N}_{1:1\_\mathrm{Redundant\_NFE}}(\mathrm{t}) * R^{N/16}_{MUX}(\mathrm{t}) * R^{N/16}_{1:1\_\mathrm{Redundant\_ADC}}(\mathrm{t})$$

Equation (22)

Where,

$$R_{1:1\_\mathrm{Redundant\_NFE}}(\mathrm{t}) = \sum_{i=0}^{1} \binom{2}{i} R_{NFE}^{2-i}(\mathrm{t}) * (1 - R_{NFE}(\mathrm{t}))^{i}$$

$$R_{1:1\_\mathrm{Redundant\_ADC}}(\mathrm{t}) = \sum_{i=0}^{1} \binom{2}{i} R_{ADC}^{2-i}(\mathrm{t}) * (1 - R_{ADC}(\mathrm{t}))^{i}$$

And, $R_{(4,4)MEA}(t)$ is given by equation (19) in Chapter 3, for an '*N*' electrode multi-electrode array.

4.4. An Architectural Benchmark for Next Generation Brain Implantable Devices

It is important to demonstrate how the proposed fault-tolerant architectures are comparable to those that are proposed in literature. For this purpose an architectural benchmark for next generation brain implantable devices is selected to be compared in terms of the three vital design parameters for such devices, namely (1) the area of the implantable device, (2) the active power consumed by the architecture and (3) the reliability of the implantable device to faults in the implanted device. A patent filed by researchers at Yale University [70], has set itself as an architectural benchmark for next generation brain implantable devices. This piece of work has been used to compare and validate the fault-tolerant designs proposed in this dissertation.

Figure 24 represents a block diagram of the architecture described in the Yale design for a brain implantable system. The major functional blocks of the design for recording neural signals are: (1) an array of electrodes to sense the underlying neural activity, (2) an analog switch network that connects the electrodes to the array of instrumentation amplifiers and is also used for electrode impedance measurement and tissue stimulation, (3) a group of instrument amplifiers, one for each of the recording electrodes, (4) an analog-to-digital converter unit to facilitate data transition to and from a remote circuitry, and (5) a transmission and reception unit. It must be noted that the microcontroller, the stimulation pulse generator, the power circuit unit and the transmission/reception units are not implanted within the patient's body; instead they are on the external skin close to the site of the implant.

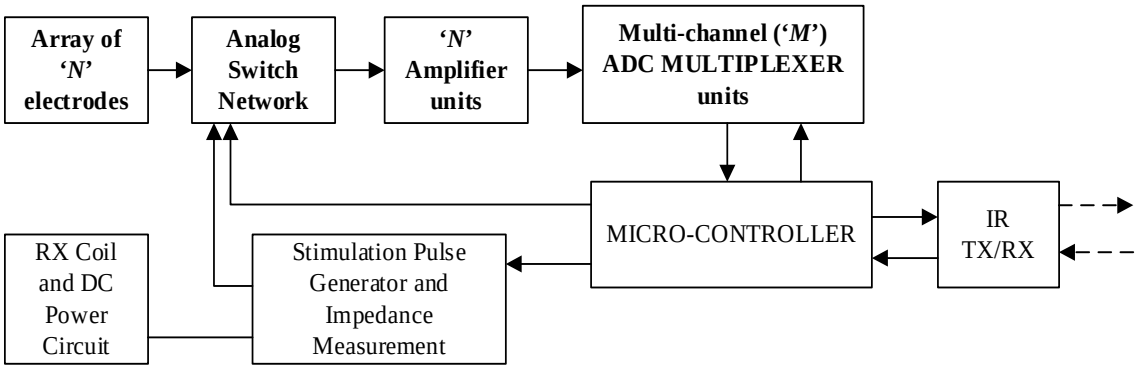


Figure 24: Block diagram of the Yale patent architecture design.

A system with an array of '*N*' electrodes has '*N*' amplifier units and the corresponding analog switch to relay the sensed neural signals from the underlying electrodes to the amplifier unit. The signals are then routed to the multichannel analog-to-digital converter via a multiplexing unit. Depending on the total number of electrodes the number of electrodes '*N*' in the system the number of ADC MUX '*M*' required can be predetermined. Figure 24 shows a block diagram of the patent design of the brain implantable architecture proposed by the Yale group of researchers. The 'implantable' portion of the design is highlighted in 'bold' text, this includes the block of '*N*' array of electrodes, the analog switch connecting the electrodes to the amplifier block, the '*N*' neural amplifiers and the multiplexed analog-to-digital converters. The number of analog multiplexers and ADC units that are used is determined depending on the value of the total number of channels '*N*'. In order to make a close comparison of the designs we assume that the architecture proposed by the patent design follows the design optimization criteria proposed in [60], for the number of multiplexers and ADCs used per '*N*' channels. The design optimization criteria dictates that each multiplexed ADC should process 16 channels, thereby making the number of ADC MUX '*M*' required totaling to '*N*/16'.

Taking into consideration the above assumptions and design criteria the reliability of this system can be expressed by the following equation:

$$R_{Benchmark\_system}(t) = R_{(0,4)\text{MEA}}(t) * R_{switch\_network}(t) * R_{\text{Amplifier\_block}}(t) * R_{MUX\_\text{block}}(t) * R_{ADC\_\text{block}}(t)$$

$$= R_{(0,4)\text{MEA}}(t) * R_{switch\_network}(t) * R^{N}_{Amplifier}(t) * R^{N/16}_{MUX}(t) * R^{N/16}_{ADC}(t)$$

Equation (23)

Where,

$$R_{(0,4)\text{MEA}}(t) = R^{N}_{electrode}(t)$$

One of the major pros of this design is the analog switch network that continuously monitors the impedance of the implanted electrodes. This information can be used to monitor which electrodes are healthy and which electrodes sense signals are inaccurate, thereby giving a false-positive or false-negative indication to use the neural stimulation mechanism to curb seizure activity in that area of the brain. This can lead to a potentially unnecessary neural stimulation or might put the patient's life in jeopardy if it was a false-negative indication and the seizure suppressant is not activated. However, this design does not include any type of fault-tolerance mechanism that can either reconfigure possible faults in the system to achieve complete system recovery from a state of total system failure or lead the system into a state of graceful degradation. This is a major drawback of the Yale design as well as in many other brain implantable architectures that has been proposed in the literature as discussed in Chapter 2.

4.5. Design Analysis of the Proposed Fault-tolerant Architectures

In this section, comparison between the three proposed fault-tolerant architectures and the benchmark architecture has been drawn in terms of three vital performance parameters namely, (1) the area of the implantable device, (2) the active

power consumed and (3) the overall system reliability of the brain implantable architecture designs. To facilitate this analysis, approximate values of the three performance parameters for the three proposed fault-tolerant architecture designs and the benchmark architecture design are derived for an '*N*' channel MEA neural-recording integrated chip in a 0.18µm CMOS technology. The proposed fault-tolerant architecture designs are evaluated for implantable devices with (1, 4) and (4, 4) interstitial redundancy array (IRA) type implantable MEA electrode designs for different values of '*N*', where '*N*' is the total number of recording channels, which is same as the total number of primary electrodes present in the MEA of the brain implantable device.

4.5.1. System Reliability Analysis:

The reliability equations of the four IRA MEA designs considered in this work, i.e. the (1, 4), (1, 6), (2, 6) and (4, 4) IRA MEAs are derived as discussed in Chapter 3 of this document. Reliability expressions for the system reliabilities of the four brain implantable architectures introduced in this Chapter are provided in sections 4.1., 4.2., 4.3., and 4.4 for a (4, 4) IRA MEA configuration. The expressions for system reliabilities of the four systems for a (1, 4), (1, 6), and (2, 6) IRA MEAs can be derived in the same lines. It is clearly evident from the block diagrams of the four brain implantable architectures shown in figures 21 – 24, that the four systems consist of major neural signal monitoring blocks arranged in either a 'series' or 'parallel' or a combination of the two, such that the systems assumed to have a constant failure rate also have sufficient combinatorial arguments to employ Combinatorial Reliability Analysis in deriving the system reliability expressions for the four implantable architecture designs [29]. It must be noted that two out of the five major blocks of the implantable device, namely the analog

switch block and the analog multiplexer block are quite similar in functionality with separate logic driving either of them. Because of the simplicity of design of these blocks, their respective reliabilities are assumed to be 1.0 to simplify the design analysis of the system. Also, in the design analysis of the proposed fault-tolerant systems we assume the coverage factor to be 1.0., by doing so we assume that a fault if present in the system, is successfully detected and diagnosed and the fault-reconfiguration process is achieved correctly by replacing the faulty components with healthy spare components present within the system. Also, the analog switch block serves as a tool to achieve fault-reconfiguration in the system, and hence is assumed to have a reliability of 1.0.

Figures 25, 27, 29 and 31 represent the system reliability trends of the four architectures with a (4, 4) IRA MEA configuration, for varying values of component reliability, for '*N*'= 64, 256, 1024 and 4096, and with a coverage factor of '*C*'=1. The system reliability of the four architectures are depicted such that a reliably working system is one in which all '*N*' channels of the implantable device is functional. An analysis of the system reliability trends indicate that the systems of the three proposed fault-tolerant architectures are more reliable than the system in the benchmark architecture. Observing the system reliability trends it is also clear that systems with a lower component reliability should adopt Fault-tolerant Architecture 3 to maintain good system reliability and Fault-tolerant Architectures 1 and 2 can be adopted for systems with higher component reliability to maintain a decent system reliability while keeping a lower hardware overhead. Similarly, the system reliabilities of the four implantable architectures with a (1, 4) IRA MEA configuration, for '*N*'= 64, 256, 1024 and 4096 is represented in Figures 26, 28, 30 and 32.

Also, the system reliability expressions for systems with (1, 6) and (2, 6) IRA MEA can be derived in the same lines as discussed for the (1, 4) and (4, 4) IRA MEA designs.

The system reliability expressions for the four architectures are derived considering an assumption that a 100% fault reconfiguration is required for normal system operation. Hence, the system reliability trends shown in figures 25 - 32 are extremely conservative as compared to what is generally expected in practice, which is only a certain percentage of channels need to remain operational for the system to function reliably. Therefore, our results clearly indicate that the system reliability will be considerably greater if a system with less-than-hundred-percent working channels i.e. a state of graceful degradation is acceptable. Figures 29 - 32 may suggest that systems become less reliable when the number of sensors in the MEA increases. This is true only when it is assumed that a system is considered to be functional when each channel (sensor and its signal conditioning circuitry) is operational, i.e., no more than the total number of available spare units in the system can fail. It should be noted, however, that the total number of faults which can be tolerated with these designs are higher for larger MEAs. Moreover, if graceful degradation in system function is acceptable, then systems with larger MEAs will have better performance.

The results in the graph in Figures 25 - 32 are intended to facilitate a comparison either between the four system architectures with the same number of electrodes (*N*) or between systems with same architecture design and different number of spares or different redundancy ratio. For example, one can compare the system reliability of Fault-tolerant Architecture 3 with (4, 4) IRA MEA for '*N*' = 64 shown in the Figure 25 with the Fault-tolerant Architecture 1 with (4, 4) IRA MEA for '*N*'= 64 shown in the same

figure. Or, the Fault-tolerant Architecture 3 with (4, 4) IRA MEA for '*N*' = 64 shown in Figure 25 can be compared to the Fault-tolerant Architecture 3 with (1, 4) IRA MEA for '*N*'= 64 shown in Figure 26. The system reliability analyses made in Figures 25 - 32 for the four implantable architectures evidently shows that the three proposed fault-tolerant designs project better system reliability as compared to a system that does not include any redundancy.

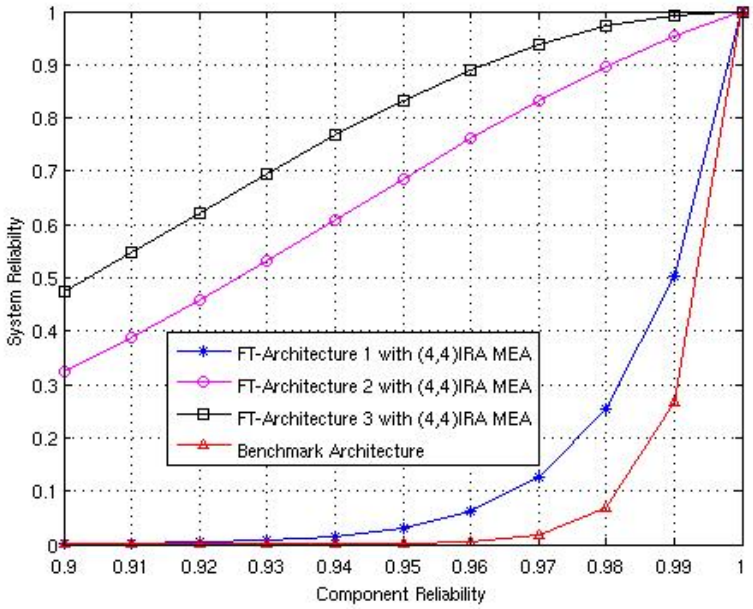


Figure 25: System reliability of the three proposed fault-tolerant architectures and the benchmark architecture in a (4, 4) IRA MEA configuration for *N* = 64 channels, for component reliability varying between 0.9 - 1.0.

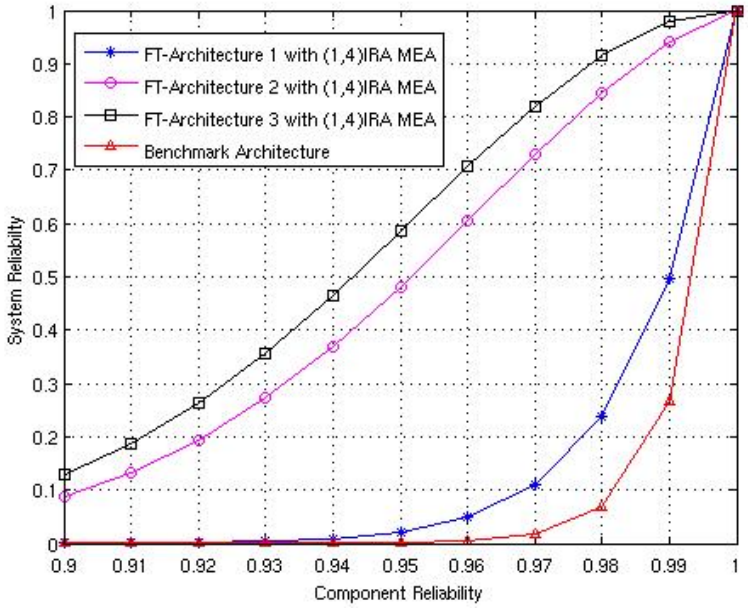


Figure 26: System reliability of the three proposed fault-tolerant architectures and the benchmark architecture in a (1, 4) IRA MEA configuration for $N = 64$ channels, for component reliability varying between 0.9 - 1.0.

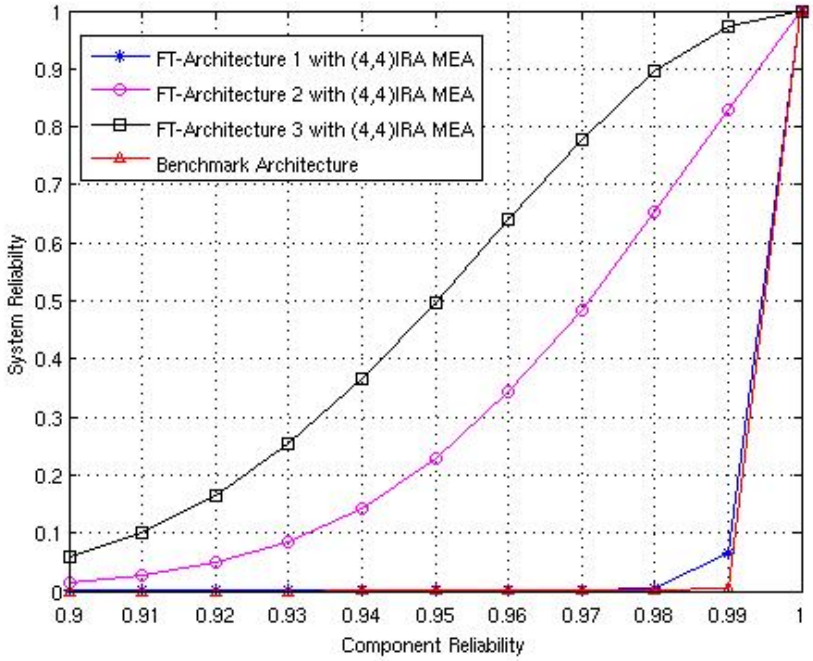


Figure 27: System reliability of the three proposed fault-tolerant architectures and the benchmark architecture in a (4, 4) IRA MEA configuration for $N = 256$ channels, for component reliability varying between 0.9 - 1.0.

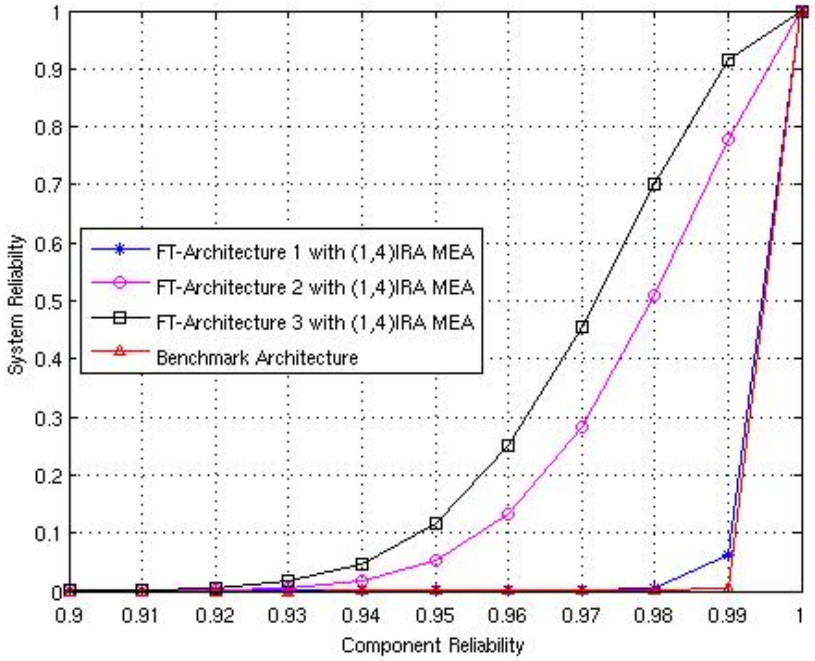


Figure 28: System reliability of the three proposed fault-tolerant architectures and the benchmark architecture in a (1, 4) IRA MEA configuration for N = 256 channels, for component reliability varying between 0.9 - 1.0.8

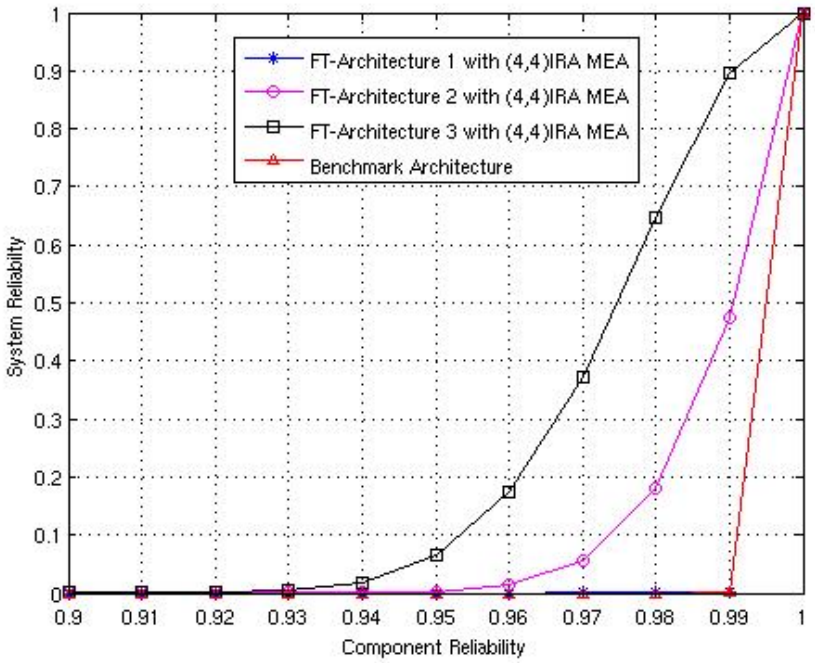


Figure 29: System reliability of the three proposed fault-tolerant architectures and the benchmark architecture in a (4, 4) IRA MEA configuration for N = 1024 channels, for component reliability varying between 0.9 - 1.0.

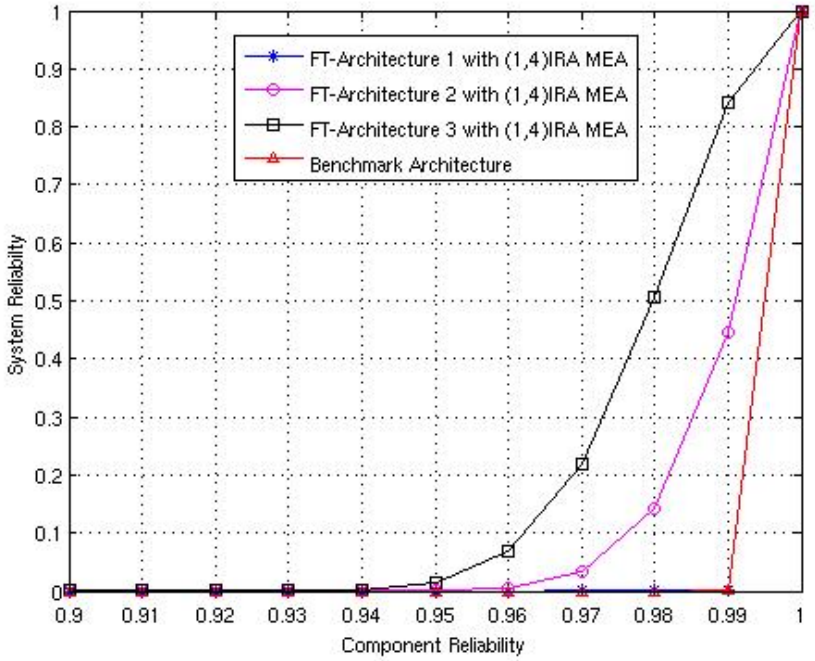


Figure 30: System reliability of the three proposed fault-tolerant architectures and the benchmark architecture in a (1, 4) IRA MEA configuration for N = 1024 channels, for component reliability varying between 0.9 - 1.0.

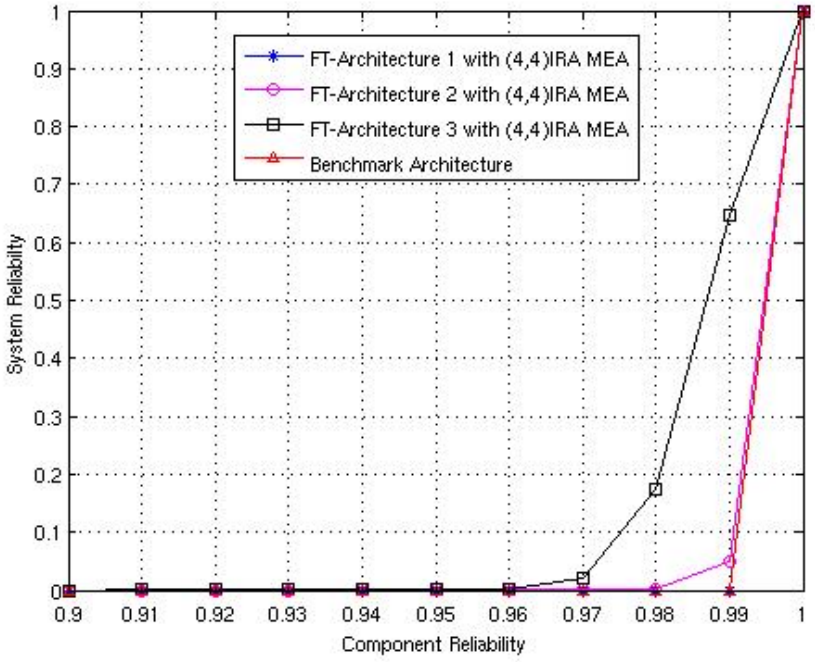


Figure 31: System reliability of the three proposed fault-tolerant architectures and the benchmark architecture in a (4, 4) IRA MEA configuration for N = 4096 channels, for component reliability varying between 0.9 - 1.0.

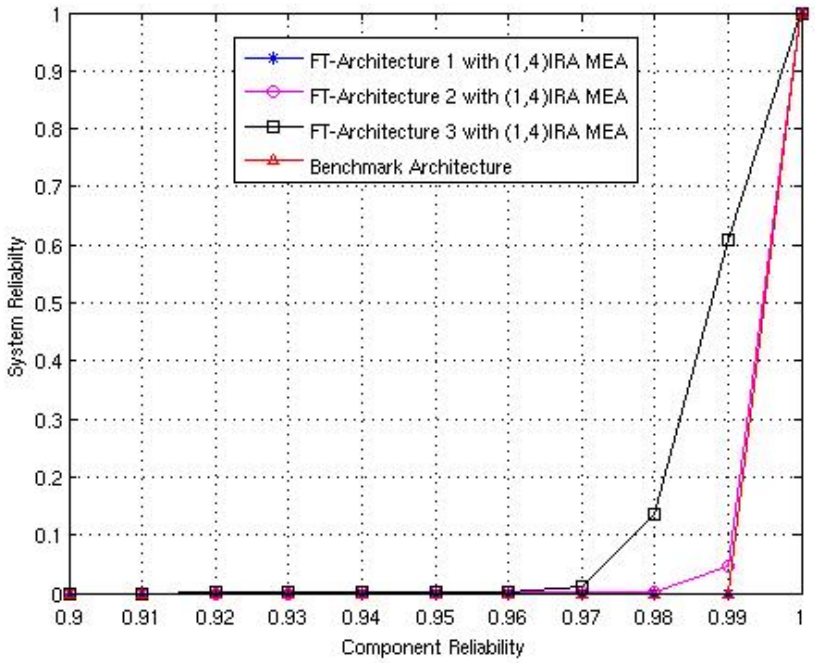


Figure 32: System reliability of the three proposed fault-tolerant architectures and the benchmark architecture in a (1, 4) IRA MEA configuration for N = 4096 channels, for component reliability varying between 0.9 - 1.0.

4.5.2. System Reliability Analysis with Graceful Degradation

It is evident from the system reliability analysis of the three proposed fault-tolerant systems in section 4.5.1., that a system is qualified to be fault-free after reconfiguration if and only if the number of working channels is equal to the total number of channels in the system. A channel is defined as a single path that starts at a sensing electrode, and continues through the major microelectronic circuit blocks of the neural microelectronics, like the neural-front-end, the analog-multiplexer and the analog-to-digital-converter circuits. The system reliabilities in such cases as shown in figures 25-32, for the three proposed fault-tolerant implantable architectures in (4, 4) IRA MEA and (1, 4) IRA MEA designs. However, a higher value of reliability can be obtained if a smaller number of working channels suffices to achieve the desired function, that is, if a graceful degradation of the system is allowed.

The system reliability if a graceful degradation is applicable will swing between two extreme cases. A best case scenario is one in which the faults in the system occur such that they are distributed in all the major blocks of the implantable system such as the MEA, the NFE and the ADC. In this case the total number of channels that will fail will be less than the number of fault sites. On the contrary a worst case scenario is one in which the faults are concentrated within a single major block of the implantable system such that it leads to maximum possible channels to fail. For example, assume a system with Fault-tolerant Architecture design 1, with N = 64 recording channels and (4, 4) IRA MEA. If a 10% graceful degradation is allowed in the system then the total number of faults allowed in the system is 6. Under the best case scenario the 6 faults are evenly distributed in all the three major blocks of the implantable device such that no more than 2 channels fail. In the worst case scenario all the 6 fault-sites will remain concentrated in one of the major blocks of the implantable device, in this case let's assume that the 6 fault-sites are localized to the MEA, indicating that 6 channels have failed. Therefore, if graceful degradation in the system function is acceptable, then systems with larger recording channels will have better performance than the ones shown Figures 28 and 32.

4.5.3. Area- Power Analysis:

The three proposed fault-tolerant brain implantable architecture designs and the benchmark architecture are distinctly different from one another in terms of the amount of redundancy and the scope of fault-tolerance available in the major functional blocks: namely the multi-electrode array (MEA), the neural-front-end (NFE) and the analog-to-digital-converter (ADC). The MEA can be a 2D or a 3D array of electrodes that are either spread across or embedded within the brain tissue that is of interest. Each neural-

front-end comprises of three distinct circuits: a front-end low-noise neural-amplifier, a band-pass filter and a unity gain buffer. And, due to its moderate speed, moderate resolution and very low-power consumption a successive-approximation-register (SAR) ADC has been selected for physiological applications such as a brain implantable device [18], [23] and [60]. From the block diagrams of the three proposed fault-tolerant architecture designs and the benchmark architecture are shown in Figures 21 - 23 and Figure 24 respectively, it is clearly evident that the total area occupied by an implantable architecture can be expressed as a sum of the areas of the signal processing blocks in the neuroelectronic circuit of the implantable architecture design. And, the total power of an implantable architecture can be approximated as the sum of the power drawn by each of the signal processing blocks in the fully implantable neuroelectronic circuit. These expressions can be represented by the following equations:

$$Area_{total} = Area_{NFE\_block} + Area_{switch\_network} + Area_{multiplexer} + Area_{ADC\_block}$$

Equation (24)

$$Power_{total} = Power_{NFE\_block} + Power_{switch\_network} + Power_{multiplexer} + Power_{ADC\_block}$$

Equation (25)

A benchtop testing of a similar neural-front-end circuit in 0.18µm CMOS [18], reveals that the area occupied and power consumed by a neural-front-end unit in the four implantable architectures discussed here is 0.03 mm^2 and 5.4µW respectively. A simulation of a similar 12-bit SAR ADC circuit, as expected to be used in the implantable architectures, is realized in 0.18µm 1P6M mixed-signal CMOS technology [23], and the results conclude that the power consumed by the 12-bit SAR ADC is 47.86µW. The same piece of literature also reveals that the ADC occupies an area of 0.39mm^2. It is evident

from the expressions for total area and power of the implantable systems represented by Equations (24) and (25), that the system with the highest redundancy and hence the reliability will consume the maximum area as compared to the systems with a lower level of redundancy. As an example, approximate values for the total system area and power consumed by the four different architecture designs with an N = 64, (4, 4) IRA MEA and component reliability of 0.98, when fabricated in a 0.18 µm CMOS process technology are presented in Table 1.

Table 1: Reliability-Area-Power comparison for the three proposed fault-tolerant architecture designs versus the benchmark architecture design for an N = 64 (4, 4) IRA MEA system, in a 0.18 µm CMOS process technology.

	System Reliability	Total System Area (in sq-mm)	Total System Power (in µWatts)
Benchmark Architecture	0.06	3.48	537.110
Fault-tolerant Architecture 1	0.25	3.48	537.300
Fault-tolerant Architecture 2	0.90	5.40	537.364
Fault-tolerant Architecture 3	0.98	6.96	537.368

The following assumptions have been made in computing the values for the total system area and power for each of the four architectures: (1) The area occupied by the switching network is assumed to be negligible with respect to the neural-front-end and analog-to-

digital converter blocks, and (2) Power used by every switch in the analog switch network is equal to 1 nW. In arriving at the values of the total system area and power for each of the four architectures in Table 1, the following points must be noted: (1) the analysis only accounts for the area and power consumed by the active components in the system, such as the analog switches, neural-front-end units and analog-to-digital units. The area occupied by the MEA (i.e. the array of passive sensor units) are not accounted for; (2) the area and power of the analog multiplexer is relatively negligible w.r.t. to the other active components in the implanted device hence is not accounted for in the total area-power analysis of the systems; and (3) the table represents only approximate values, however the exact values for the total system area and power if obtained will follow a similar trend as described by the approximate values presented in Table 1. Therefore, the relative total system area and power comparison between the four implantable architectures can be represented by the following expressions:

$$Area_{FT-Architecture3} > Area_{FT-Architecture2} > Area_{FT-Architecture1} > Area_{Benchmark\_Architecture}$$
$$Power_{FT-Architecture3} > Power_{FT-Architecture2} > Power_{FT-Architecture1} > Power_{Benchmark\_Architecture}$$

In addition to the extra redundant units that contribute to the larger area of a more redundant design, the switching network required to facilitate system reconfiguration also contributes to the extra area of the system. In addition to the leakage power in each of the four systems, the switching power required to reconfigure the system will contribute to a higher power consumption. This switching power will be greater in each of the three proposed systems with higher reliability as compared to the benchmark architecture design.

CHAPTER 5: CONCLUSIONS

This thesis presents a detailed argument for the importance of incorporating fault-tolerant solutions in chronic brain implantable systems and gives a brief overview of the existing neural monitoring and modulating techniques in Chapters 1 and 2 respectively. The proposed fault-tolerant solutions are presented in Chapters 3 and 4, and require redundant units that act as spares and replace the primary units should they fail. In Chapter 3, the reliability and simulation analysis of the two fault-tolerant solutions clearly indicate that with hardware redundancy solutions, an increase in the reliability of an MEA is possible. Where a 'module' in the MEA grid is composed of a sensor and its associated circuitry. There are, however, some limitations and additional design aspects of these solutions which must be considered. First, we note, that the reliability of both primary and spare modules is likely to be the same. Both primary and spare modules are placed in the same environment and both are equally likely to fail as they will be subjected to similar stress and will experience similar brain tissue response [26].

The reliability analyses of the three fault-tolerant brain implantable architecture designs presented in Chapter 3, clearly indicate an increase in the probability of dependable monitoring of the electrical activity of the brain. Like any other fault-tolerant approach which includes redundancy, the strategies presented in this work will increases cost and development time and may impact power consumption, heat generation, mass, and volume of an implantable device. Redundancy thus makes some implantable design issues more critical and may require the use of appropriate conservation strategies. A fault-tolerant

design thus requires a trade-off between dependability and the amount of redundancy required to achieve it. It must be noted that the fault-tolerant solutions can be designed with cold spare circuitry, where a spare unit is switched on only if it is brought online during reconfiguration. Cold spare reconfiguration helps conserve power, facilitates thermal management, and may extend the life of the spare units.

A second category of fault-tolerant design can be explored where the electrodes and signal conditioning circuitry can be considered separately and a fault-tolerance strategy can be evolved which treats the electrodes and the electronics as separate components with different redundancy ratios for each, and allows separate reconfiguration to be performed for the electrode array and their electronics. The three fault-tolerant architecture designs presented in Chapter 4 exploring the aforementioned second category of fault-tolerant design. Other additional design aspects that need to be considered while designing complete fault-tolerant implantable solutions (which have not been addressed in this work) are the other components of a brain monitoring systems such as the reference electrode, or the computation, communication and power sub-systems. Some of these components and sub-systems are relatively simple compared to the sensing component and a simple scaling of these systems with redundant spares can help improve device reliability.

Two assumptions are made in the reliability analysis of the fault-tolerant solutions that are presented in this work. The first assumption is that the module failure rate (in Chapter 3) or the unit failure rate (in Chapter 4) is constant during the lifespan of the implantable device. Second, it has been assumed in the presented fault-tolerant solutions that the module failures (in Chapter 3) or the unit failures (in Chapter 4) are independent. In the situation where the failures are not independent, for example when there are cluster

faults, the reconfiguration strategy presented in Section 3.4 is still applicable and leads to optimal reconfiguration. Depending on the size of the fault cluster, the number of spare modules available may be insufficient, leading to an MEA whose reliability is lower than when failures are independent. However, if a graceful degradation state is allowed, then the system reliability can be higher.

The solutions described here are not necessarily limited to electrophysiological sensors and its corresponding signal conditioning circuit or the brain. The solutions can be readily extended to any organ which has to be reliably sensed by an implanted array of sensors and the accompanying electronics. Other sensors, which may be considered, include glucose sensors, or biosensors to measure neurochemistry.

This dissertation presents five fault-tolerant solutions. Two solutions are proposed to improve the reliability of MEAs. The MEA may contain only sensors or include a modular structure that includes a sensor and the accompanying signal conditioning circuit. The first solution utilizes rows or columns of spare modules to replace faulty primary modules. In this approach the hardware overhead is substantial. The second solution uses space redundancy with local configuration capability where spare modules are placed in the interstitial sites of the MEA and can replace their neighboring faulty primary modules. The analytical and simulation results presented indicate a significant improvement in system reliability with redundancy. Three other novel architecture designs have been proposed that aim at enhancing the fault-tolerant capability of fully implantable brain-machine devices. Their corresponding reliability analysis indicates that fault-tolerant solutions will improve the overall system reliability and availability of chronic implantable devices. Moreover, as demonstrated in Sections 3.6., and 4.5.2., if graceful degradation in

system function is acceptable, then the systems will have better performance than estimated by the reliability analysis done in Chapters 3 and 4.

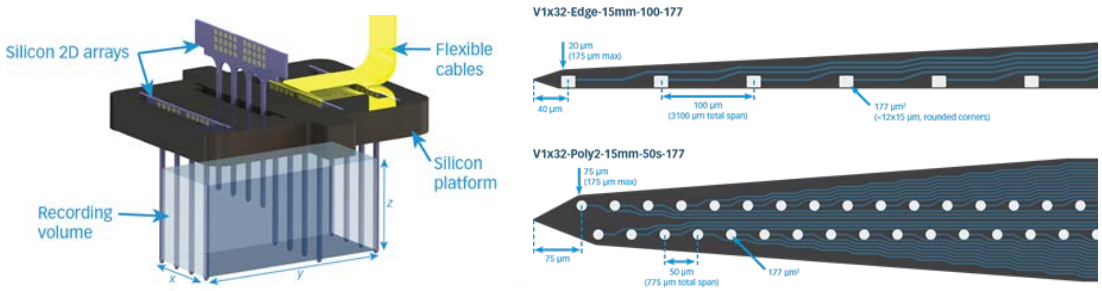
The proposed fault-tolerant architectures have been successfully compared against the benchmark architecture in terms of reliability area and power of the four architectures. An increase in reliability always involves some level of redundancy, hence it is obvious that the fault-tolerant architecture will have a greater area and power consumption. However, due to the low-power and area techniques available due to advancements in the semiconductor technology it is a very small price to pay to provide patients with reliable implants that can be implanted chronically for long periods of time.

5.1. Future Work

For the fault-tolerant solutions and concepts presented in this work to operate as intended it is essential to have a real-time fault-detection and diagnosis unit which can detect an error in the system in real-time and locate the failed unit in order to execute the necessary steps required to achieve an optimal system reconfiguration with the available spare units. The accuracy of the fault-detection and diagnosis algorithm will dictate the performance of the overall system reconfiguration from faulty conditions. Hence, in future an accurate fault-detection and diagnosis algorithm will take forward the work presented in this dissertation towards implementation and benchtop testing to investigate the performance of the implantable device.

Recently there has been several efforts to decrease the sensor size and making the sensor grids denser. Furthermore, several groups have proposed 3-D dense sensor grids so that signals from areas beneath the cortical surface can also be measured. For example, Figure 33 shows the Matrix Array [71] and the Vector Array [72] where several Vector

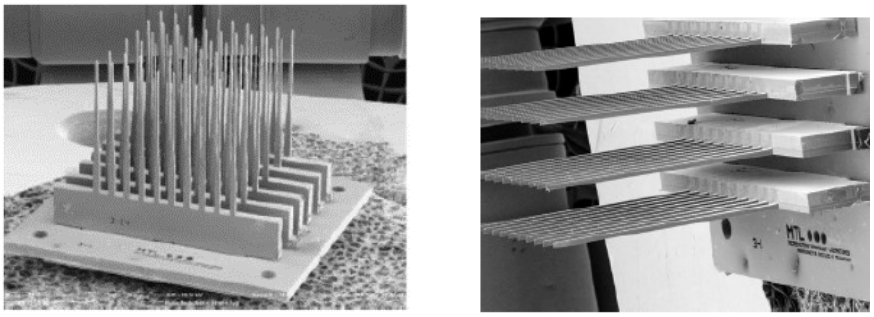
Arrays can be combined into a 3-D configuration. Similarly, Modular Bionics, a privately held company located in Santa Ana, California, that is dedicated to advancing neuro and bionic technologies has proposed N-Form, a 3-D grid of sensors.



(a) Matrix Array (b) Vector Array

Figure 33: (a) The Matrix Array consists of 2-D silicon microelectrode arrays installed into a silicon platform. (b) Vector Arrays can be combined into a 3-D configuration. (Courtesy: NeuroNexus)

More recently another interesting customizable 3-D array has been proposed [73]. Figure 34 shows the micrograph of a six ten-probe linear arrays assembled into a 6 x 10 two-dimensional array of probes. Each probe has 32 sensors. The probes in each linear array are spaced 400 µm center-to-center and the arrays are spaced 600 µm center-to-center.



(a) A micrograph of six ten-probe linear arrays.

(b) Linear arrays are spaced at 600 µm

Figure 34: Scalable 3-D microelectrode recording architectures. (Courtesy MIT)

The concept of using the interstitial redundancy in 1-D and 2-D grids can be easily extended to the 3-D grids of any shape and size to improve the reliability of the 3-D grids.

One possible strategy that could be used to determine *m* and *n* of an (*m*, *n*) system could be based on the Euclidean distance defined by the user. If the defined distance is *d*, then all the spare sensors within the distance of *d* from a primary sensor gives the value of *m* and all the primary sensors within the distance of *d* from a spare sensor gives the value of *n*. Analytical techniques used for 2-D systems can applied for 3-D systems to calculate the system reliability. A second strategy that could be used is based on functional redundancy where a clustering algorithm identifies sensors whose measurements are similar. Maximum matching algorithm can then be applied on the clusters identified to replace faulty sensors by fault-free sensors.

Furthermore, such systems with thousands of sensors will pose significant challenges in transmitting signals to the outside world due to limited bandwidth. One way to overcome this problem is to transmit only the relevant signals. Once the clustering algorithm identifies all the clusters, the sensors in each cluster are ranked according to the quality of the signals and only best measurements are transmitted. It should be noted this strategy inherently incorporates aspects of fault-tolerance, indicating the possibility to create a fault-tolerant 3D grid system of any shape or size. For example, the 3D system could take the shape of a sphere or a cylinder.

5.2. Final Thoughts

The future of brain implantable device is predicted to be dense, wireless, and fully-implantable for long periods of time (i.e. in terms of years). Unlike other critical systems brain implantable devices which are aimed at chronically used, are derived of any fault-tolerant techniques. As feature sizes continue to decrease to provide better area-power characteristics, with the continued desire to increase the recording density while attempting

to monitor neural activity for extended periods of time, the reliability of the implanted system will continue to reduce further unless intercepted by in-built fault-tolerant solutions incorporated within the device. In this thesis, I have presented novel fault-tolerant solutions which can be implanted within the implantable neural signal acquisition system thereby increasing the possibility for such devices to function chronically for years after implantation. With the appropriate amount of redundancy these fault-tolerant solutions have the ability to have good area-power performance while achieving a higher system reliability when compared to a system that is devoid of fault-tolerant features in its design.

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