POWERLINE COMMUNICATIONS THROUGH SERIES CONNECTED SWITCHED MODE POWER CONVERTERS TO BE USED IN SOLAR MICROINVERTERS

by

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ABSTRACT

DANIEL WADE EVANS. Powerline communications through series connected switched mode power converters to be used in solar microinverters. (Under the direction of DR. ROBERT COX)

Modern photovoltaic converters and energy storage modules are shifting to a cascaded or distributed module-level inverters to reduce the required voltage output of each module and thereby optimizing production costs. The switch to an AC-stacked architecture, where all modules are in series, requires a method of synchronization of the voltage and current output of each module to the grid since each module has no direct connection to the grid as to acquire such synchronization. Many different methods for communicating the zero crossing to each photovoltaic converter module are currently available but either increases plant level costs from running additional wiring for wired mediums or are susceptible to remote interference in wireless communication mediums potentially disrupting operation by either loss of synchronization or inaccurate timing of synchronization to the zero crossing of the grid.

This research develops a current-mode based methodology for powerline communication and synchronization by which the photovoltaic converter and energy storage modules may detect the zero crossing and synchronize the converter operation to the grid. Included in the methodology is the use of series connected power electronics as a communications medium for the current-mode based means of power line communications. The developed communications model, generalized for all series connected power electronics, establishes a foundation for part the physical layer in the OSI model. This model is implemented and performance analyzed in synchronization of a physical system consisting of series connected inverters used in solar power conversion. The approach has been used to allow an 8-module, $120V_{RMS}$ string to operate in the field for over six months without any synchronization or controls-related failures.

ACKNOWLEDGEMENTS

I want to acknowledge SineWatts, Incorporated (Inc.) and the chief executive officer (CEO), Shibashi Bowhmik, for opportunity to work with and help develop the technology used in the panel level optimized solar inverters deemed the SineWatts 'Molecule'. Hardware design, whether it be for research or product development, involves a significant financial cost that must be paid upfront. SineWatts, Inc. has borne those costs throughout this dissertation and has made it possible for this work to be completed.

I also want to acknowledge my advisor, Dr. Robert Cox, for all the insight he has provided over the years. His knowledge and experience in the design of electronics has been invaluable. He has also put forth a lot of effort to see the completion of the designs presented in this dissertation, even spending nights and mornings working with me in the lab.

I also want to acknowledge my coworkers Paul O'Connor, John Troxler, Deepak Somayajula, and Saurabh Trivedi as well as Hamid Jafarian, Mehrdad Biglarbegian, Iman Mazhari, Shahriar Nibir, and Dr. Babak Parkhideh at UNC Charlotte that participated on the project. They have greatly assisted in the setups and testing with the communications.

DEDICATION

This work is dedicated to my family. My father, Wade Evans, has sacrificed a lot to help put me through school. My mother, Billie Evans, has been a constant source of love and encouragement. No matter what was going on, I could always visit and enjoy a home cooked meal. I enjoyed visiting my brother and my sister-in-law, Brent and Tamara Evans, and their children. The role of crazy uncle is a blast playing with my niece and nephew. Watching them grow up, I see how quickly anyone can learn when they focus. During the later stages of research and writing, two major experiences changed my look on life. My brother had a blocked artery in his heart and had a stint put in. Afterward, I became an uncle to a second nephew. Events like this tends to put life back into perspective. I am glad to have more time to spend with my family.

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LIST OF ABBREVIATIONS

AC	alternating current
ADC	analog to digital converter
AGC	automatic gain control
ANT	Advanced and Adaptive Network Technology
AWGN	additive white Gaussian noise
BPSK	binary phase shift keying
CAN	controller area network
CSV	comma-separated values
DC	direct current
DSP	digital signal processor
FET	field effect transistor
FFT	fast Fourier transform
IC	integrated circuit
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
MLPE	module level power electronics
MOSFET	metal oxide semiconductor field effect transistor
MPPT	maximum power point tracking
NASA	National Aeronautics and Space Administration

OFDM	orthogonal frequency division multiplexing
OSI	open system interconnection
PCB	printed circuit board
PF	power factor
PLC	power line carrier
PLL	phase locked loop
PRIME	Powerline Intelligent Metering Evolution
PSD	power spectral density
PV	photovoltaic
PWM	pulse width modulation
QPSK	quadrature phase shift keying
SNR	signal to noise ratio
SPI	serial peripheral interface
THD	total harmonic distortion
TI	Texas Instruments
TTL	transistor-transistor logic
UNC	University of North Carolina
VCO	voltage controlled oscillator

CHAPTER 1: INTRODUCTION

Since the dawn of time, man has relied on the sun's energy to survive. In 1941, Ohl patented the first silicon solar cell in the United States with an efficiency of less than 1 % [1–3]. As effiency increased, the National Aeronautics and Space Administratin (NASA) became interested in using the solar cells for the purpose of powering satellites and proceeded to launch the Vanguard 1 [4]. Since then, efficiency of the silicon PV cells have increased to 26.7% [5] and commercially available silicon solar panels have now risen to 22.7% [6]. It is noted that new solar cells, such as III-V class materials and multi-junction manufacturing, are being investigated for manufacturing besides traditional silicon cells, but are not commercially available. The highest reported efficiency of these types of solar cells is 46% [5].

Once the solar panels have converted solar energy into electrical energy, the distribution and use of the electrical energy is considered in the design of a photovoltaic converter. For the purpose of generating large amounts of power into the electrical grid, switched mode converters have been employed with the first 1-megawatt power station, and ARCO Solar design, being commisioned during 1982 in Hisperia, California [4].

1.1 Progression of Switched Mode Converters Used in Photovoltaic Converters

Photovoltaic (PV) power generation is currenting expanding at a rate of 43% year-over-year in the United States [7], with total penetration expected to reach at least 178 GW by 2040 [8]. Depending on the impact of policies such as the Clean Power Plan (CPP), this growth could potentially be much larger [8]. Current growth is largely fueled by the ever-decreasing costs of PV modules and associated equipment,

with some developers claiming that installed costs on utility-scale systems will be less than \$1 per W_{DC} in 2017 [9]. This explosive growth has led to the several commercially available inverter topologies, including central, string, and module-level solutions [10–14]. These various architectures can be compared and evaluated in terms of power conversion efficiency, maximum power point tracking (MPPT) efficiency, reliability, and cost.

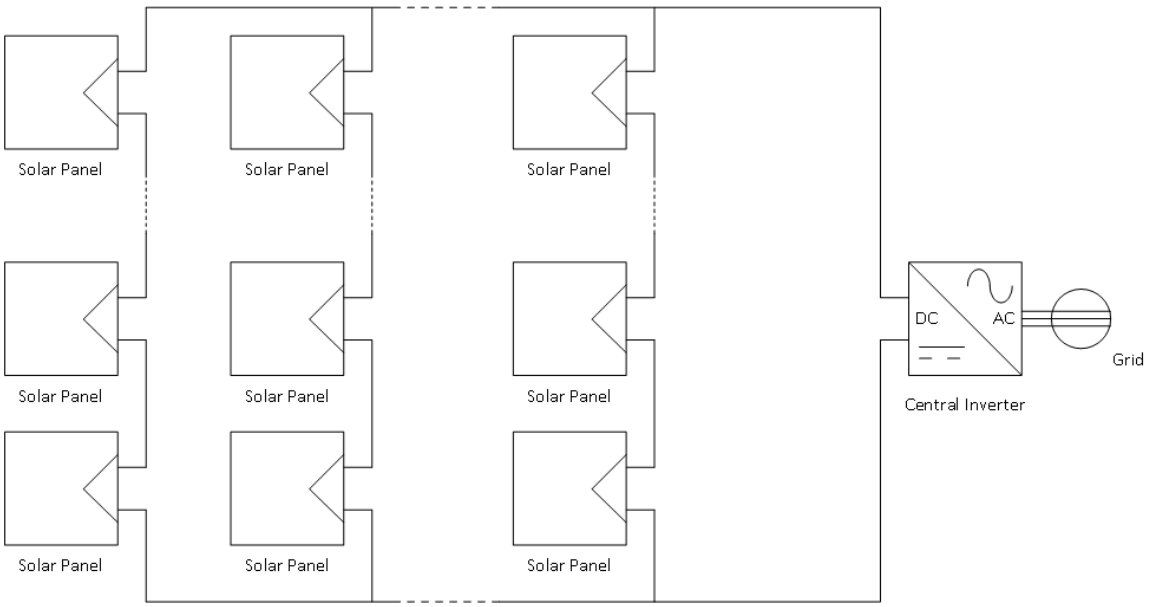

Figure 1.1: A central inverter operating at a plant level by converting power from all strings of solar panels at the grid interface only.

The first converter is a central inverter, an inverter that has multiple strings of solar panels connected together with the direct current (DC) to alternating current (AC) conversion at the grid interface [11] and can be seen in figure 1.1. This is the most common type of solar converter used by electrical utilities and has a power conversion efficiency, as high as 98.5% [15]. Such a system does not contain any type of individual panel MPPT and suffers from a single point of failure design [11] but does have very high reliability by having a minimum amount of electronics for the system. The price for the converter averages €0.05/W or \$0.058/W, the lowest of all converters [15].

The second converter is a string inverter, an inverter that has a single string of solar panels connected with the DC to AC conversion at the grid interface [11] and can be seen in figure 1.2. This is the second most common type of solar converter used by electrical utilities and has a power conversion efficiency, as high as 98% [15]. Such a system also does not contain any type of individual panel MPPT and instead will sweep for the maximum point in the entire string [11]. The plant does not suffer from a single point of failure due to having a large number of string inverters, but does have reduced reliability by having more power converters in the plant. The price for the converter averages €0.06-0.017/W or $0.069-0.20/W, the second lowest of all converters [15].

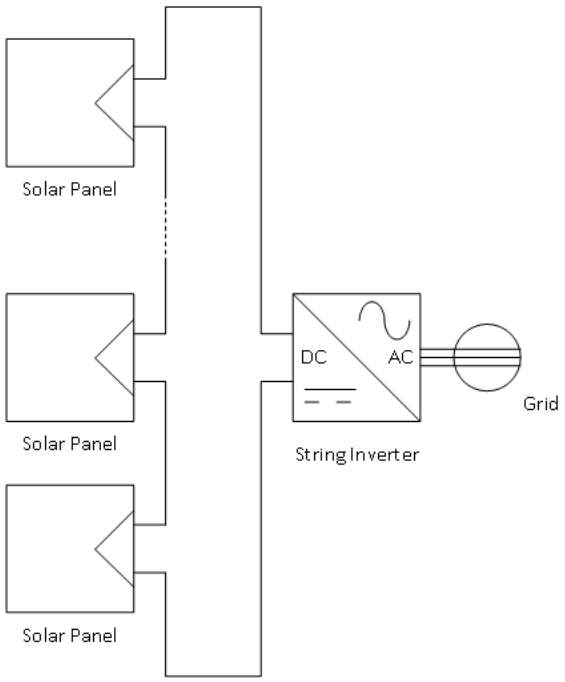

Figure 1.2: A string inverter coverts power from a single string of series connected solar panels.

The string inverter family of inverters also include multi-string inverters as seen in figure 1.3. These types of inverters include a DC/DC converter between the string of PV panels and the inverter at the grid interface. This system is designed for three phase connections but the industry is typically references these with the generic name

string inverter.

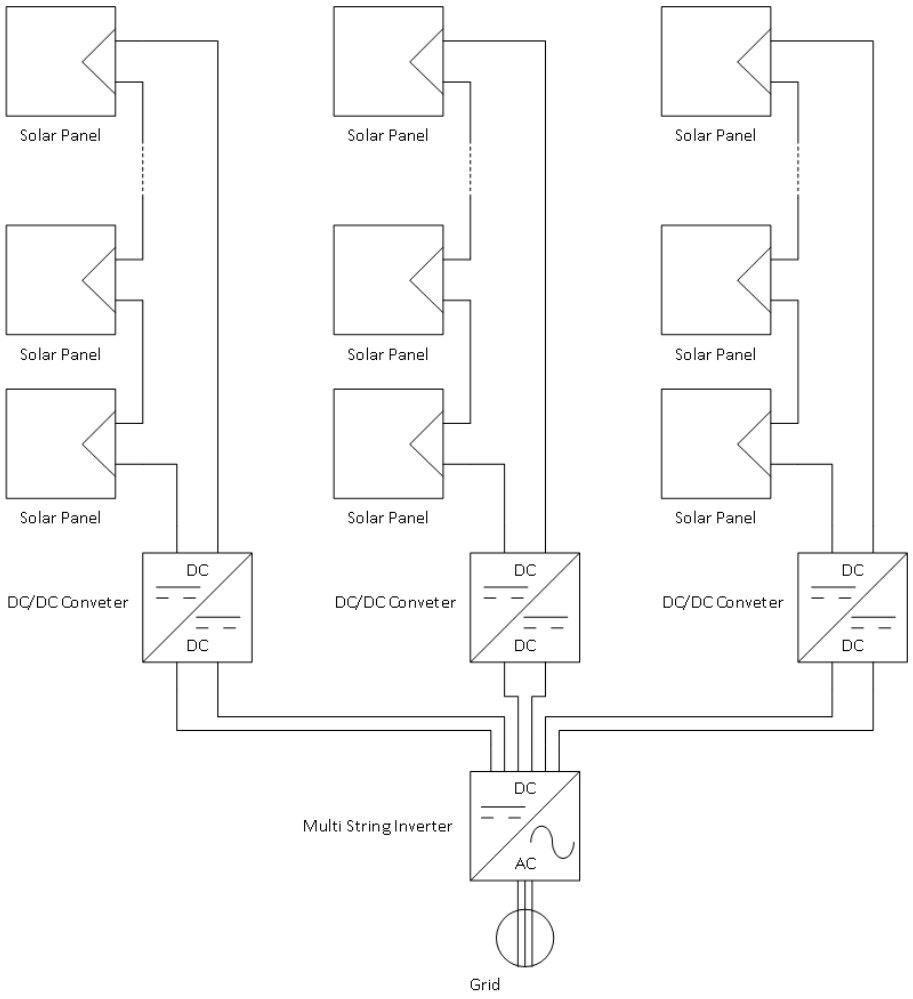

Figure 1.3: A multi-string inverter consists of two stages of power conversion, a DC/DC converter at each string of series connected solar panels and a DC/AC inverter at the grid interface.

The transition to module level power electronics (MLPEs) brought about the micro inverter, an converter that has a single solar panels connected to the grid by implementing a DC/AC power conversion that boosts the output voltage [11] and can be seen in figure 1.4. This type of solar converter has not had large adoption rate by electrical utilities primarily due to the high cost per watt. The converter has a power conversion efficiency in the range of 90% to 95% [15]. This MPLE converter implements MPPT such that each panel [11]. The plant does not suffer from a single

point of failure due to each panel having its own converter, but such a system has caused the price for the plant level system to increase significantly to approximately €0.28/W or $0.32/W, the highest of all converters [15].

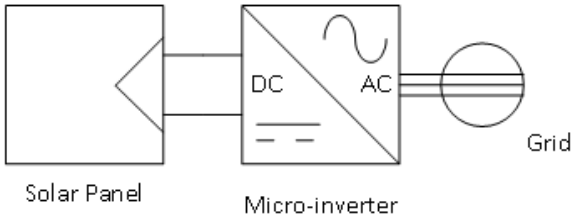

Figure 1.4: A micro inverter coverts power from a single solar panel directly to the grid.

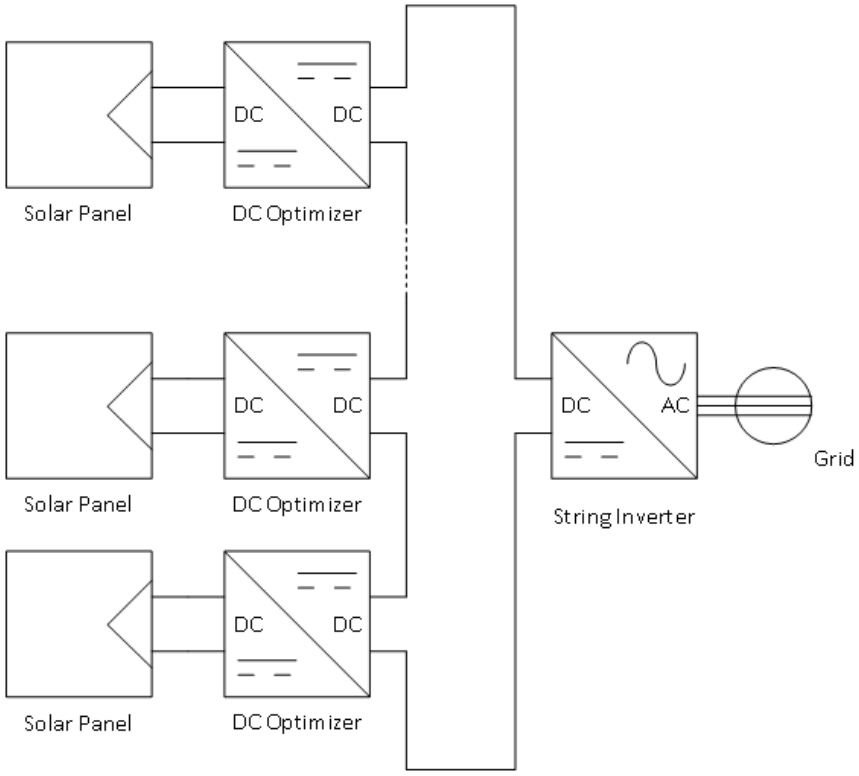

Figure 1.5: A DC optimizer is DC/DC converter at each solar panel before connecting in a string with a DC/AC inverter at the grid interface such that the maximum power can be obtained from each individual panel.

The newest commercially available MLPE is referred to as a DC optimizer, a DC/DC converter that attaches to each solar panel operating as a low voltage step down converter [11] and can be seen in figure 1.5. This type of solar converter works

in conjunction with the string inverters to obtain MPPT on each indivual panel. The converter has a power conversion efficiency up to 98.8% [15]. This MPLE converter implements MPPT such that each panel [11]. Reliablity depends on whether the DC optimizer can be bypassed in a failure or not but there are concerns with the ease of replacement of the DC optimizer module. The increased electronics in the system does cause the price for the plant level system to increase to approximately €0.09/W or \$0.10/W, but does not include the string converter at the grid interface [15].

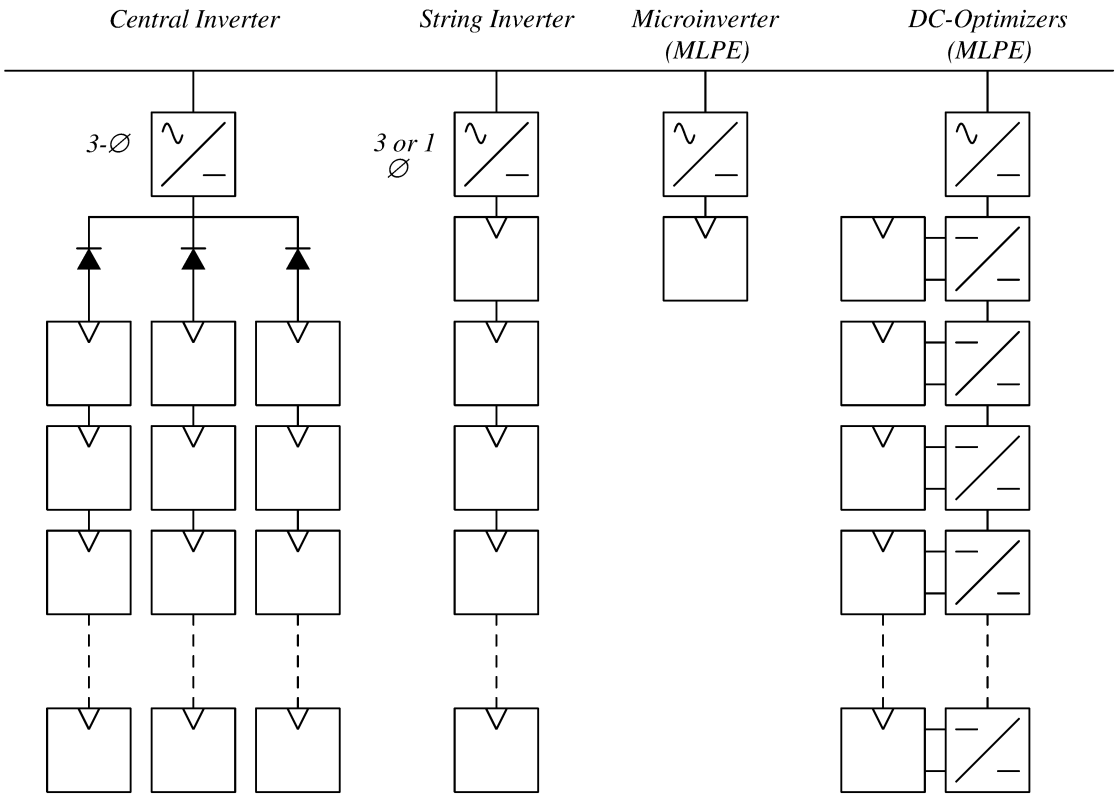

Figure 1.6: Representation of PV inverter topologies (a) The central inverter is characterized by having multiple strings of solar panels connected in parallel at a DC to AC converter with protection diodes to protect against reverse bias conditions. (b) The string inverter is characterized by having only one string of panels attached to a converter enabling it to preform string level maximum power point tracing. (c) The micro-inverter operates at the panel level interfacing each panel to the grid. (d) DC-Optimizers contain panel level converters to tract the maximum power point at each panel while leaving it up to an inverter at the end of the string to interface to the grid.

As a final recap of the PV converters, a major component of any grid-connected PV installation is the DC-to-AC inverter that conditions the DC power provided by the module such that it can be coupled into the AC grid. The two most critical functions of these inverters are to maximize energy harvest and to control the relative phase of the current injected into the grid. Figure 1.6 shows the most common inverter topologies. The least expensive and most common variety is the central inverter, which interfaces multiple strings of series-connected PV modules and can support capacities upwards of several MW. The fact that central inverters use only one power stage to interface so many modules to the grid means that they offer extremely high reliability. By the same token, however, the inverter can only extract the maximum amount of power from the combination of strings connected on its DC-side, meaning that differences between panels resulting from soiling or long-term wear can dramatically reduce the potential energy yield [16,17]. To combat this issue and to increase penetration in the commercial and residential markets, manufacturers have introduced string inverters which are essentially smaller scale central inverters that handle only a few series-connected strings.

1.2 Overview of the SineWatts Architecture

Recently, there has been significant interest in MLPE. With the ability to optimize the power flow from each panel, MLPE solutions offer the highest overall yield [17]. In addition, MLPE solutions provide an opportunity to rapidly shutdown each panel in a rooftop array during fire conditions and thus provide the best means to meet aggressive new requirements for protecting first responders during emergencies [18]. The additional flexibility provided by MLPE does not come without drawbacks in current commercially offered solutions. Most notably, efficiency is lost either because multiple power conversion stages are required or a high step-up ratio is needed [16]. Additionally, MLPE solutions have a higher cost per Watt because of the sheer number of components required in each installation [19]. That said, the cost for such

systems has dropped dramatically, and the leading manufacturers are experiencing as much as 300% annual growth in units shipped [19].

From a technical perspective, MLPE is clearly the best pathway for the PV industry. To optimize efficiency and reduce costs, the research community has explored approaches that allow inverters to be mounted to the back of individual panels so that the inverter outputs can be directly combined before interfacing to the grid. One such approach relies on the cascaded H-Bridge topology, in which individual inverters are connected to the back of individual panels whose AC-side outputs are combined in series [20,21]. Among several drawbacks of this approach is the fact that the operation of each individual inverter must be coordinated by a central controller. Essentially, each inverter must send and receive signals during each switching cycle. It is well known that communication delays can be extremely problematic in distributed control systems with many nodes communicating so frequently [22]. This practical problem has precluded the widespread adoption of such techniques.

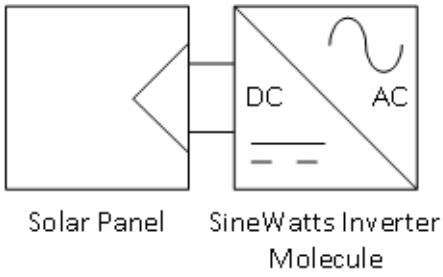

Figure 1.7: The SineWatts inverter molecule attaches individually to the solar panel like the microinverter but does not connect directly to the grid.

SineWatts, Inc. recently patented several new approaches to solve the problems associated with decentralizing of the inverter functionality [23]. Figures 1.7 and 1.8 shows the SineWatts architecture. Note that each module provides a low-voltage AC output waveform synchronized to the grid voltage. As discussed in later sections of this dissertation, this approach allows for significantly lower voltage power semiconductors that can switch at frequencies on the order of several hundred kHz. This

latter fact is important because it implies that component count and size can be reduced so that nearly the entire inverter can be placed on a single silicon die. Key to the SineWatts approach is a simple control scheme that relies only on low-bandwidth signals broadcast over the powerline.

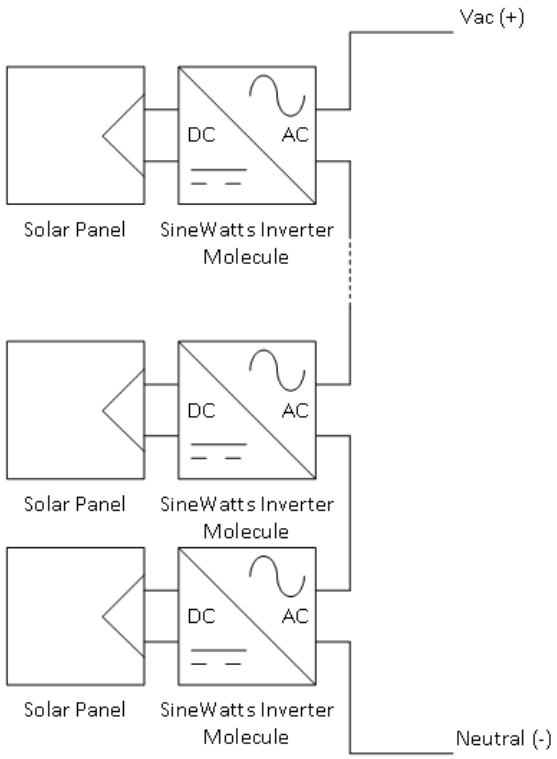

Figure 1.8: The SineWatts inverter molecule outputs an AC voltage that will add together in a string to build up to the grid voltage. This topology is referred to as an AC-stacked inverter system.

In the SineWatts architecture presented in figure 1.8, each PV module has its own low-voltage inverter. Given that the inverter functionality is distributed to individual panels, each power converter is called an Inverter Molecule$^{\mathrm{TM}}$. Although there are multiple ways to instantiate the architecture, figure 1.9 shows the most common approach, with $N-1$ of the series-connected inverters operating in a voltage-source mode. Assuming a grid voltage of the form $V_G sin(\omega t)$, then the peak voltage provided by each voltage-mode molecule (VMM) is approximately V_G/N. The remaining inverter operates in a current-controlled mode.

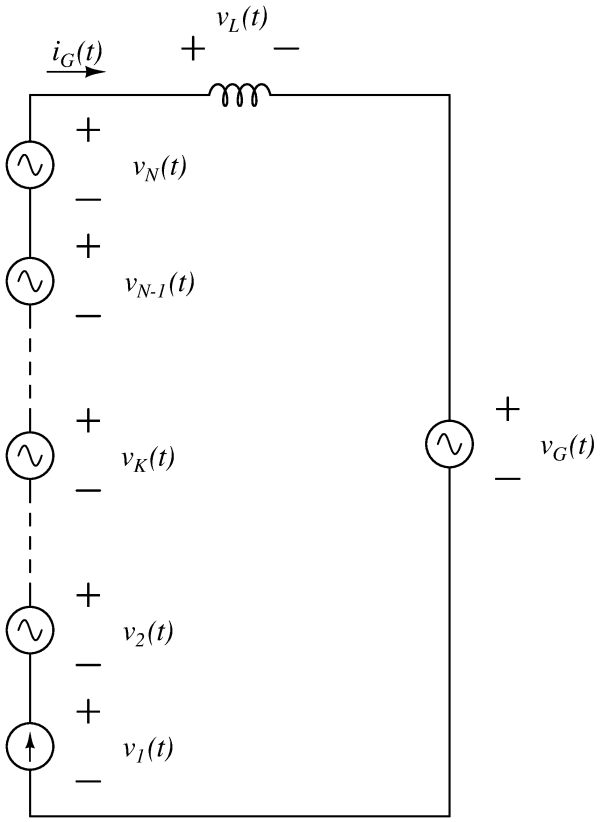

Figure 1.9: Steady state model of the SineWatts architecture.

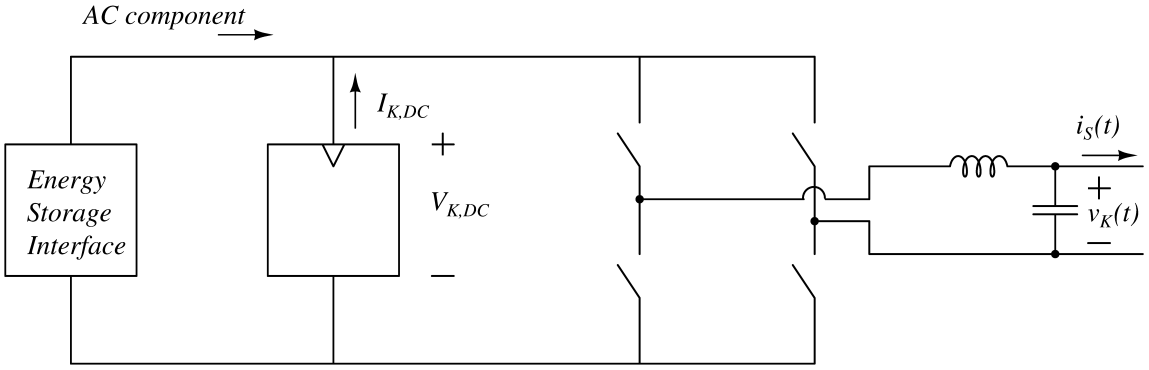

Figure 1.10: Simplified internal structure of the SineWatts Inverter Molecule™.

Figure 1.10 shows the simplified internal operation of each molecule. The full-bridge inverter utilizes pulse-width modulation (PWM) to create a sinusoidal waveform at the output of the low-pass filter. Each sinusoid is synchronized to the grid voltage such that the output of the k^{th} molecule has the form $v_K(t) = V_K sin(\omega t)$. Assuming

the AC-side current has the form $I_G sin(\omega t)$ and ignoring any higher-order switching effects, the AC-side power at the k^{th} molecule is given in equation 1.1 below.

$$p_K(t) = v_K(t) i_G(t) = \frac{V_K I_G}{2} \left[1 + \cos\left(2\omega t\right)\right] \tag{1.1}$$

Since instantaneous power balance requires the power at the DC-side of the full-bridge to match the AC-side output power, a capacitive storage element is added as shown in figure 1.10 to source the AC component in equation 1.1. The average power at the AC side matches the PV input power, and thus in terms of the variables presented in figure 1.10, the average power is described in equation 1.2 below.

$$\langle p_K(t) \rangle = \frac{V_K I_G}{2} = V_{K,DC} I_{K,DC} \tag{1.2}$$

A local controller in each Molecule continuously tracks the maximum power point of its PV module. From the perspective of the $N-1$ VMMs, the AC-side current is fixed, and thus each controller must vary the amplitude of its output voltage to maintain the module at its maximum power. To do so, it varies the modulation index of the inverter, which is defined in equation 1.3 below [24].

$$m_K = \frac{V_K}{V_{K,DC}} \tag{1.3}$$

Given that that the amplitude of the current is essentially constant from the perspective of each VMM, equation 1.2 in combination with the maximum power point tracking ensures that the steady-state amplitude of the output voltage will always be defined as seen in equation 1.4.

$$V_K = \frac{2 V_{K,DC} I_{K,DC}}{I_G} \tag{1.4}$$

If for some reason the steady-state current changes while the environmental conditions on k^{th} panel do not, the amplitude of the k^{th} output voltage will thus scale accordingly.

The behavior of the current-controlled molecule, which is known as a current-administrator/voltage compensator (CAVC), is like that of the VMMs except that it controls the AC-side current amplitude to match the maximum power point. Average power balance in the CAVC thus dictates that the AC-side current is related as seen in equation 1.5.

$$I_G = \frac{2V_{K,DC}I_{K,DC}}{V_1} \tag{1.5}$$

Given the operation of the $N-1$ VMMs, the amplitude V_1 at the CAVC output is fixed in steady-state and its value is given by summing the voltages around the loop in figure 1.9, as seen in equation 1.6.

$$v_1(t) = v_G(t) + v_L(t) - \sum_{K=2}^{N} v_K(t) \tag{1.6}$$

Note that a change in the voltage from any one of the VMMs will thus reduce V_1 and ultimately force a corresponding change in the current I_G. Note that appropriate steady-state behavior requires the number of panels to be selected per the given grid voltage. For a typical 60-cell PV module having a maximum power point voltage between 25 and 30V [25], each Molecule will provide approximately 15VAC under steady-state conditions.

While the dynamic operation and start-up characteristics of the SineWatts architecture are outside of the scope of this work, the steady-state analysis presented here is sufficient for describing the requirements of the communications system. Even though control is distributed in the SineWatts architecture, the communications requirement is vastly simplified. Information about the required power flow from each Molecule is communicated through simple circuit constraints set by Kirchhoff's Laws.

In each Molecule one of the two terminal variables is always fixed in steady-state such that other terminal variable can naturally fluctuate as needed to maintain maximum power transfer. During normal operations, the only required communications signal is a broadcast transmission that synchronizes the PWM switching clock in each molecule to the AC grid voltage. This signal must be transmitted approximately once every AC line cycle as opposed to once every switching cycle. This signal must be reasonably free of delay and have minimal error. Furthermore, an effective scheme requires a low-cost implementation.

1.3 Importance of Grid Synchronization

The generation of power from a plant into the electrical utility's grid involves the control of the amplitude and phase of the plants current relative to the utilities voltage. This relation specifies the apparent power of the system, including the real and reactive power components and can be seen in equations 1.7 to 1.9 below [26]. When examining the relation of the angle of the current to the angle of the grid voltage, it shows how as the angle difference varies between 0° and 360°, the amount of real power that is supplied to the grid changes changes from its maximum value, to zero, and then eventually to a negative value meaning that power flow has been reversed.

$$S = V_{rms}\angle\theta_v \, I_{rms}\angle -\theta_i = P + jQ \tag{1.7}$$

$$P = V_{rms} I_{rms} \cos\left(\theta_v - \theta_i\right) \tag{1.8}$$

$$Q = V_{rms} I_{rms} \sin\left(\theta_v - \theta_i\right) \tag{1.9}$$

When generating power to the grid, an impedance must be inserted between the generator and the grid to control the current flow. The difference between the generator and grid voltage is divided by the impedance of the inductor to obtain the current

that flows. Theoretically, as the inductance value is reduced approaching zero, the current magnitudes increase toward infinity. Utilizing this known inductance, the generators voltage can be controlled relative to the grid's voltage and phase to control the current and hence the power generation [27].

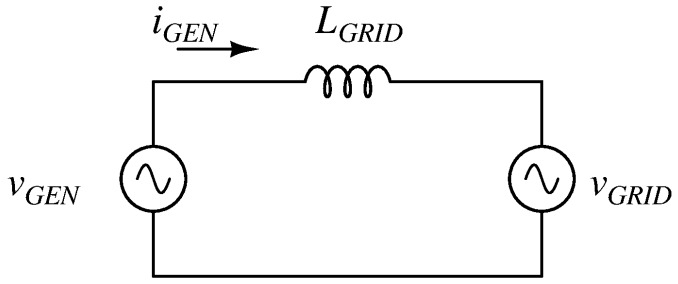

Figure 1.11: Circuit model for a generator injecting current into the grid through an inductance.

Derived from figure 1.11 is the power generation equations of the generator. Below in equations 1.10 to 1.12 are the time domain definitions of the values labeled in figure 1.11. These will be transformed to the steady state equations for the rest of the derivation.

$$v_{grid} = V_{GRID,PK} \cos(\omega t) \tag{1.10}$$

$$v_{GEN} = V_{GEN,PK} \cos(\omega t + \delta) \tag{1.11}$$

$$i_{GEN} = I_{GEN,PK} \cos(\omega t + \phi) \tag{1.12}$$

The analysis begins with the Kirchhoff's voltage law (KVL) to get a relation for the current through the inductor.

$$-v_{GEN} + v_{L,GRID} + v_{GRID} = 0 \tag{1.13}$$

$$-v_{GEN} + j\omega L_{GRID} i_{GEN} + v_{GRID} = 0 \tag{1.14}$$

$$i_{GEN} = \frac{v_{GEN} - v_{GRID}}{j\omega L_{GRID}} \tag{1.15}$$

Then looking at the apparent power equation, the relation for the inductor current can be substituted in.

$$s_{GRID} = \frac{1}{2}(v_{GRID})(-i_{GEN})^* \tag{1.16}$$

$$s_{GRID} = (v_{GRID}) \left(-\frac{v_{GEN} - v_{GRID}}{j\omega L_{GRID}} \right)^* \tag{1.17}$$

Then substituting in the frequency domain versions of the grid and generator voltage.

$$s_{GRID} = \frac{V_{GRID}}{2} \left(\frac{V_{GRID} - V_{GEN}e^{j\delta}}{j\omega L_{GRID}} \right)^* \tag{1.18}$$

$$s_{GRID} = \frac{V_{GRID}}{2} \left(j\frac{V_{GRID} - V_{GEN}e^{j\delta}}{j^2\omega L_{GRID}} \right)^* \tag{1.19}$$

$$s_{GRID} = \frac{V_{GRID}}{2} \left(\frac{jV_{GRID} - jV_{GEN}e^{j\delta}}{-\omega L_{GRID}} \right)^* \tag{1.20}$$

The derivation continues by rearranging the equation to get rid of the conjugate.

$$s_{GRID} = \frac{V_{GRID}}{2} \left(\frac{jV_{GEN}e^{j\delta}}{\omega L_{GRID}} - \frac{jV_{GRID}}{\omega L_{GRID}} \right)^* \tag{1.21}$$

$$s_{GRID} = \frac{V_{GRID}}{2} \left[\left(\frac{jV_{GEN}e^{j\delta}}{\omega L_{GRID}} \right)^* - \left(\frac{jV_{GRID}}{\omega L_{GRID}} \right)^* \right] \tag{1.22}$$

$$s_{GRID} = \frac{V_{GRID}}{2} \left[\frac{-jV_{GEN}e^{-j\delta}}{\omega L_{GRID}} + \frac{jV_{GRID}}{\omega L_{GRID}} \right] \tag{1.23}$$

Finally, applying Euler's formula to transform the exponential into sin and cos functions can the apparent power formula be completed.

$$s_{GRID} = \frac{j\left(V_{GRID}\right)^2}{2\omega L_{GRID}} - \frac{jV_{GRID}V_{GEN}\left[\cos\left(-\delta\right) - j\sin\left(-\delta\right)\right]}{2\omega L_{GRID}} \tag{1.24}$$

$$s_{GRID} = \frac{j\left(V_{GRID}\right)^2}{2\omega L_{GRID}} - \frac{V_{GRID}V_{GEN}\sin\left(\delta\right)}{2\omega L_{GRID}} - \frac{jV_{GRID}V_{GEN}\cos\left(\delta\right)}{2\omega L_{GRID}} \tag{1.25}$$

The real and reactive power can then be split from the apparent power equation.

$$s_{GRID} = P_{GRID} + jQ_{GRID} \tag{1.26}$$

$$P_{GRID} = -\frac{V_{GRID}V_{GEN}}{2X_{L,GRID}}\sin(\delta) \tag{1.27}$$

$$Q_{GRID} = \frac{(V_{GRID})^2}{2X_{L,GRID}} - \frac{V_{GRID}V_{GEN}}{2X_{L,GRID}}\cos(\delta) \tag{1.28}$$

From the final equations derived, the phase difference of the string voltage has a direct relationship to the power generated into the grid. This means that for a set power harvested from the solar panels in the AC-stacked architecture, the phase of the generated voltage must be maintained. Hence, the inverters must be synchronized to the grid.

1.4 Comparison of Synchronization Methodologies

Synchronization in remote connected power electronics is essential for proper operation as shown in the previous section. This notion is true for all modular architectures that have AC output with various examples as:

- Modular multilevel converters
- Cascaded H Bridges
- AC stacked converters

The basic structure of the synchronization is having a central unit coordinate the synchronization time and then use a communication protocol and medium to communicate the synchronization to the other power electronic modules. This concept is visualized in figure 1.12. The communications protocol and hence the medium can be selected as appropriate for the requirements. The two fundamental mediums of communication are wired and wireless communication where each has a wide range of protocols.

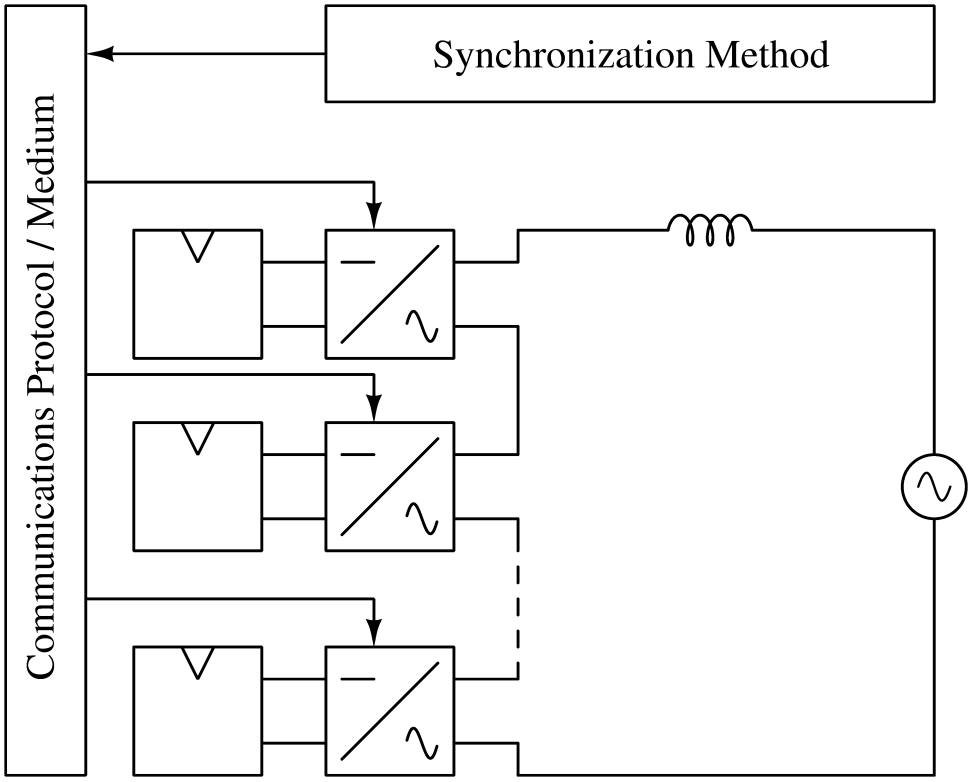

Figure 1.12: Visualization of the basic synchronization structure is series connected architectures. A synchronization method is provided by a central unit that communicates this information to the remote power electronics in the system through a selected protocol and medium. Shown is the AC-stacked inverter architecture but the concept is the same for all series connected power electronic modules.

Synchronization can be provided in several different protocols such as controller area network (CAN) and serial peripheral interface (SPI) for a wired medium or "Advanced and Adaptive Network Technology" (ANT) for a wireless medium. In the AC-stacked architecture, one needs to synchronize only at the line frequency, which greatly simplifies the synchronization process. This was shown in the architecture introduction earlier in the chapter. Utilizing this information, several examples of synchronization is found.

One CAN example shows a modular multilevel inverter being used for wind power generation in which the modules are synchronized at the switching frequency [28]. The individual inverters switching frequency is 333 Hz with a sampling frequency of

16 kHz. The CAN bus sends the synchronization signal such that the variance in synchronization is $\pm 25\,\mu s$ allowing for power operation of the system with minimal impact. In comparison with the AC-stacked inverter architecture, the synchronization frequency is higher and the variance between converters is appropriate for grid synchronization.

Another CAN protocol example shows the PWM synchronization in a cascaded H-bridge multilevel inverter where the wired medium is a fiber optic communication link [29]. The optical communication allows for the communication to occur with the reference voltage of each inverter at a different operating level. The system is a 1400 kW induction motor drive operating at 6600 V. The reported time difference in synchronization between two modules, hence the variance, is $83\,\mu s$. This is a higher variance than the first reported CAN example [28], but is still very low compared to the grid frequency in an AC-stacked inverter architecture.

There is a reported cascaded multilevel inverter with H-bridge implementation that synchronizes with an SPI protocol while using conventional wiring with optoisolators [30]. The SPI protocol is utilized in synchronizing a 4 kHz PWM reference signal for synchronization as well as the three phase line voltages. The allowable error in the system is 5% which for 4 kHz is $12.5\,\mu s$. This is comparable to the CAN latency [28].

Besides the reported use of fiber optics for the reference voltage difference of the modular inverters [29], often communications signals are provided via fiber optic cables to avoid problems from EMI [30]. EMI on wired media utilizing electrical signals are not only avoided by utilizing light in fiber optics cables but also by the use of wireless communication medium. There has been development of a synchronous medium access approach via wireless, known as the ANT protocol, to synchronize wireless sensors [31]. Reported using this protocol is a method of ranging wireless sensors based on the latency between the wireless synchronization and the latency of a sound through air from the transmitter to receiver when transmitted at the same

time. This is possible due to the variance of the wireless modules having a variance of $3\,\mu s$. Such variance is lower than the wired mediums [28,29] and would be appropriate for use in the modular multilevel converters or AC-stacked inverter architecture.

1.5 Conceptual Overview of Grid Synchronization Through the Power Line

The AC-stacked inverter architecture still utilizes an interface when connecting to the electrical utilities. This interface does not contain any power conversion hardware since the power is already conditioned by the solar inverters at the panels. Instead, the grid interface contains an electronic relay and an interface inductor enabling a higher system efficiency than the DC-optimizers as there is no power conversion. Figure 1.13 shows a representation of this grid interface. Besides the interface hardware, the grid interface contains a number of sensors to measure both the grid and string voltage and current values. The measurements from these sensors allow the grid interface to provide proper protection for the AC-stacked inverter architecture. There is anti-islanding, under and over voltage protection, over current protection, and other fault protection built in [32–34].

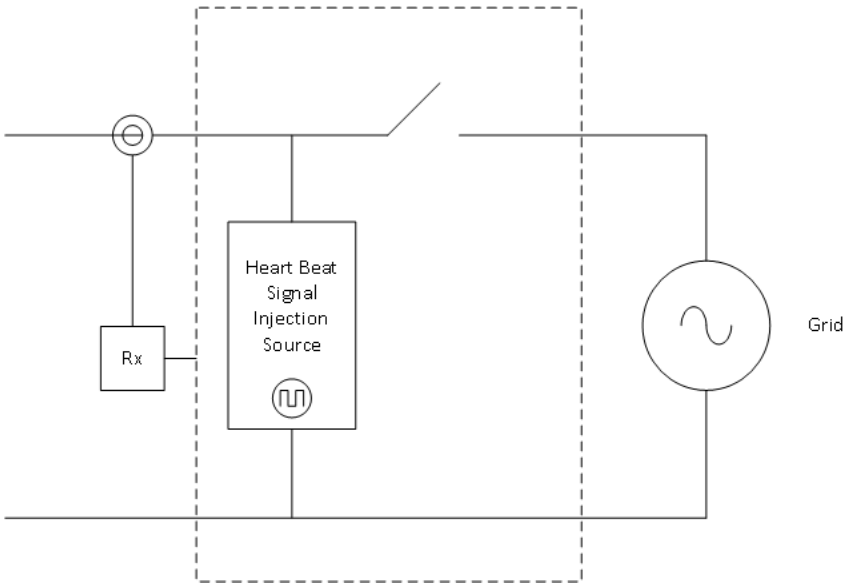

Figure 1.13: The grid connection of the AC-stacked inverters connects to the grid through a system, referred to as the termination box, consisting of a controlled electronic relay, AC filter, measurement circuitry and communication framework.

This grid interface provides all the hardware necessary for the measurement of the grid zero crossing and provides a connection point to the powerline of the string of AC-stacked inverters. The grid interface can add communication hardware to the string connection point without impacting any functional operation of the grid interface. The general idea of communicating the zero cross information of the grid is to for this communication hardware to send a pulse to represent the positive zero grid crossing. The receiver board then detects this pulse and sends it to the controller on the inverter hardware such that it then has the timing to synchronize to the grid voltage. The actual implementation details will be shown later in this dissertation.

1.6 Research Contribution

Previously reported results for the AC-stacked inverter architecture employed the use of a digital signal between the grid interface and the AC-stacked inverter modules with the use of an optoisolator for coupling between the different voltage references [32, 34–37]. This wiring does not allow the power electronic modules to be practically implemented in a commercial solution as the excessive wiring to each and every MLPE. The development of successful prototype depends on finding a new means of communicating the zero cross information to the individual inverters without requiring a change in infrastructure to existing installation methods and can operate in a reliable manner without being subject to outside interference. The current-mode powerline communications developed in this research does just that.

This research also advances the development of powerline communications in a new direction of current-based powerline communications and then uses this advancement to enable a completely decentralized AC-stacked inverter operation. No such commercial solution for a current-mode powerline communications exists which made the development quite difficult. This research shows how a current-mode powerline communications can still propagate down the communications line even though the series connected power electronics separate the wiring into sections in the system. This is

done by utilizing the series connected power electronics as a physical medium for PLC communications.

1.7 Organization of Dissertation

Chapter 2 conducts a literature review of current PLC commercially offered solutions and their relation to the current-mode PLC developed. This chapter also defines the specifications used in the design of the low latency grid synchronization signal. Chapter 3 shows the theoretical and physical implementation of the physical access layer. Empirical results are compared to the theoretical for the physical access layer before any channel modeling is performed. Chapter 4 then develops the channel model from transmitter to receiver whereby the current-mode PLC is utilizing series connected power electronic modules as a transmission medium. The chapter includes a relation for the string and grid connections in the development of the channel model. Chapter 5 examines the noise characteristics in the communication channel model as well as the hardware requirements for a signal to noise ratio (SNR). Chapter 6 presents the runtime results of the AC-stacked inverter architecture utilized by SineWatts whereby the current-mode PLC is utilized for grid synchronization. Results for the system include a six month field deployment in Birmingham, Alabama. Chapter 7 concludes the dissertation with suggestions for further work on expanding the current-mode PLC communications.

CHAPTER 2: LITERATURE REVIEW

Power line communications market has greatly expanded in recent years to a market capital of $5.47 billion dollars in 2017 with an estimated $9.43 billion dollars in 2018 [38]. Two specific areas addressed are broadband communications mainly targeted for residential customers looking to provide network capabilities inside buildings utilizing existing electrical wiring instead of installing new network cabling, and secondly narrowband communications utilized by electrical utilities to reduce communication costs and while providing long range communications solution utilizing the existing grid wiring [39]. The narrowband communications has been largely implemented by protocols such as G3-PLC and PRIME and with the regulatory bodies of the FCC in the United States and CENELEC in Europe overseeing the frequency bands availability and restrictions [39].

Even with such a large and expanding market, power line communications has not adapted to a current-mode communications means for the physical layer but instead has relied on the traditional voltage mode communications for the parallel connections found in traditional wiring. As continuous efficiency improvements in electronics has occurred, new system architectures have been explored as means of reducing converter losses in systems by utilizing a series connection of power electronics to avoid multiple power loss conversion stages. This emerging market currently consists of DC-optimizers [40, 41], stacked H-bridges [10, 42], and AC-stacked inverter architecture [23, 35–37, 43–48] in the solar market alone. Other industries are experiencing a paradigm shifts in the way to optimize power conversion for total system efficiency as well. Currently, the server industry is also looking at the use of series connected server architecture in which each server in a rack operates at ratio of the DC bus power to

the server rack to the number of servers in the rack with load balancing techniques and auxiliary power converters for load balancing when needed [49]. Other architectures based on the differential power processors may as well be utilized as a communication medium for a current based PLC communications [50, 51].

2.1 Overview of Power Line Carrier Communications

Available power line carrier communications for narrowband communication has many reference designs from various companies. Observed here is one from Texas Instruments [52] but others follow a similar design. This system is portrayed in figure 2.1. The communications utilize a unified transmitter and receiver design with grid interface by means of an isolation transformer. This isolation transformer typically includes several blocking capacitors to make sure low frequency voltage does not cause large currents through the transformer. The transmitter has the carrier and modulation generated by a microcontroller following one of the communication protocols. The transmitter then buffers the voltage signal by means of a line driver. This line driver ensures the transmitter can maintain the output signal despite loading conditions by providing large amounts of current. The signal propagates into the secondary of the isolation transformer and out of the primary into the line. The receiver obtains its signal from the isolation transformer as any signal on the line propagates through the primary and out of the secondary. The signal then passes

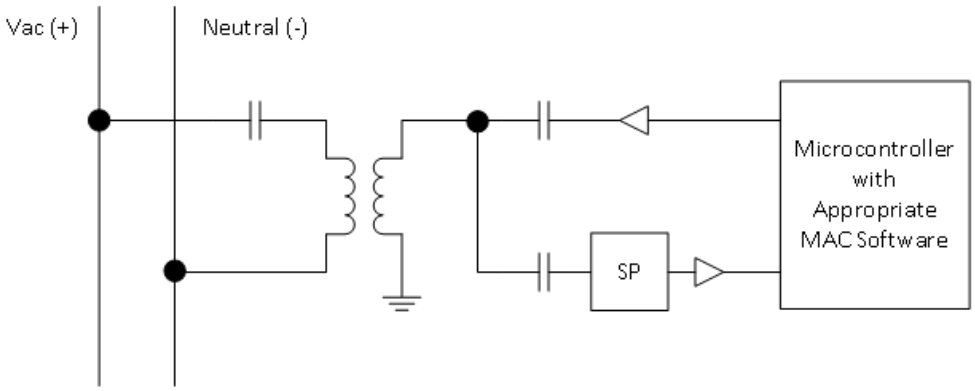

Figure 2.1: Typical PLC communications receiver and transmitter circuitry.

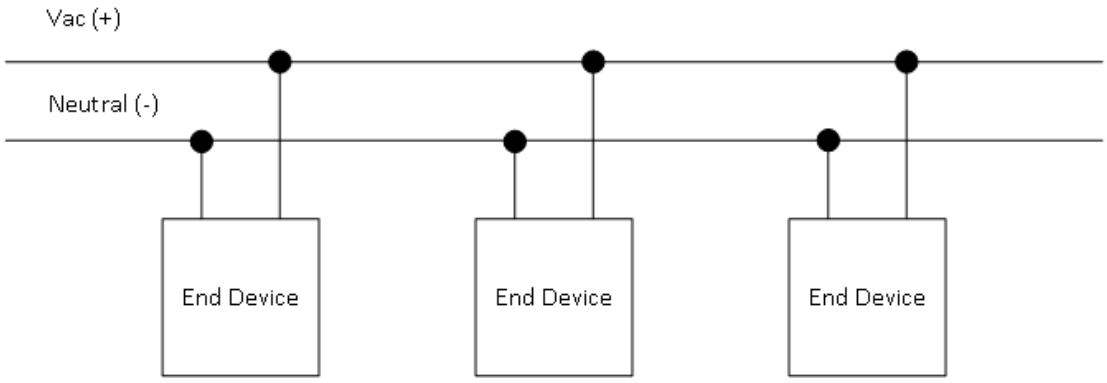

Figure 2.2: Typical PLC communications configuration where all devices are connected in parallel across the grid.

through some filtering blocks to remove noise and is amplified if needed. The same microcontroller used for the transmitter then samples the received signal and demodulates the signal and recovers the transmitted information.

The devices connected to the grid all have the same line and neutral connection. They see the same voltage. At a basic approximation, the receiving devices see the same voltage signal that is transmitted out one. This approximation is made by assuming an ideal conductor such that the devices are in parallel as seen in figure 2.2 and hence the voltage on the line is constant across all devices. Such an approximation though does not represent a real system but does display the justification for using voltage for the signal [53].

2.2 Power Line Carrier Communications Through Series Connected Switched Mode Converters Used in Solar Converters

The connection for modular power electronic converters is a series connection, not the parallel connection for the typical power line communication devices. Such a system is portrayed in figure 2.3 for comparison. For the series connection, a voltage based signal originating at the line and neutral connection would be reduced based on the number of devices in the series connection. A voltage based signal is not ideal then for a PLC communications scheme in series connected devices. Utilizing the

analysis from chapter 1 for the AC-stacked inverter architecture, it has been shown that the current through the devices is the same such that decentralized control. Since the current will be the same through the devices, why not use that current for communications as well? The development of this current-mode PLC communications and the application of this developed communications for synchronization in the AC-stacked inverter architecture is the focus of this dissertation and will presented in later chapters.

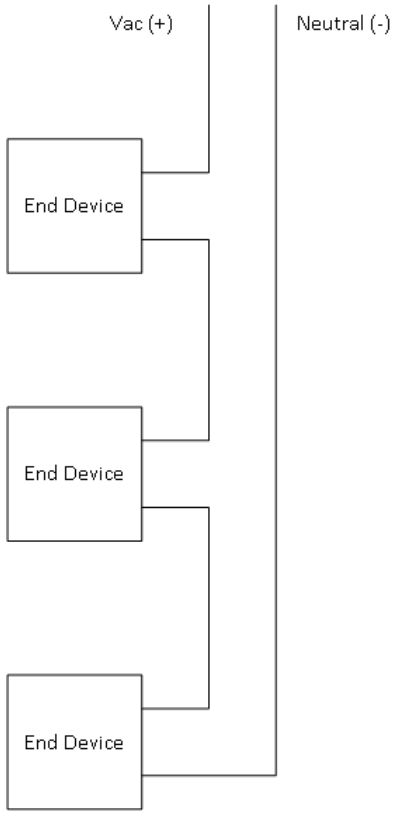

Figure 2.3: PLC communications setup in series representing the communication modules on each switched mode power converter in the string.

2.3 Specifications of Grid Synchronization Through a Power Line Carrier

Any communications scheme designed to synchronize the operation of the previously descried AC-stacked inverter module, must meet the following general specifications:

- The same signal must be broadcast to each AC-stacked inverter module.
- There must be minimal delay between the transmission and the reception at each AC-stacked inverter module.
- There must be minimal variance of the received signal at different AC-stacked inverter modules.
- The error rate should be a minimal.

These general specifications of delay and variance must have some type of ceiling though for reliable system operation even though the further reduced these become, the better it would be for the system. To quantify the ceiling, the power factor (PF) and the grid protection response time must be explored.

The desired power factor of the AC-stacked inverter architecture operating at peak power is $PF \geq 0.98$. This value means that the zero crossing of the current may be within $\pm 333 \mu s$. Since the grid interface will be measuring the zero crossing and then transmitting once the crossing is detected, this maximum delay is specified as the delay from the grid zero crossing to the reception at the AC-stacked inverter's controller. The variance is specified as being 10% of this value or $\pm 33.3 \mu s$.

CHAPTER 3: IMPLEMENTATION OF THE PHYSICAL ACCESS LAYER FOR THE RECEIVER AND TRANSMITTER WITH SIMULATED AND EMPIRICAL RESULTS

3.1 Design and Simulation of the Physical Access Layer

The first layer of a communication system in the open systems interconnection (OSI) model is the physical layer with specifies the transmitter, receiver, encoding techniques, and data rates. The physical layer here will be modeled for a simplex communication system in which the grid interface is transmitting the zero crossing information of the grid. One way to meet these goals is to transmit a current that contains information about the phase of the grid voltage as described in chapter 2. To transmit a current to each molecule, a transmitter circuit is connected at the grid interface.

This transmitter is transformer-coupled into the AC line. One can analyze the steady-state behavior of this circuit using superposition. Assuming the communications frequency ω_2 is not equal to the line frequency ω, then the string current, $i_s(t)$, and the grid current, $i_g(t)$, are

$$i_s(t) = i_{s,\omega}(t) + i_{s,\omega_2}(t) \tag{3.1}$$

$$i_g(t) = i_{g,\omega}(t) + i_{g,\omega_2}(t) \tag{3.2}$$

where the subscripts ω and ω_2 indicate the line and communication components at the two different frequencies. At line frequency, the communications current source can conceptually be shorted such that no line-frequency current flows into the transmitter. The line-frequency components of the gird and string currents are thus equal as

expressed in equation 3.3 below.

$$i_{s,\omega}(t) = i_{g,\omega}(t) \tag{3.3}$$

At the communications frequency, the analysis leaves the communications current source and the impedances of the string and grid. Figure 3.1 shows one way to represent the resulting circuit. By Kirchhoff's current law (KCL), we note that relation expressed in equation 3.4.

$$i_{s,\omega 2}(t) + i_{TX} = i_{g,\omega 2}(t) \tag{3.4}$$

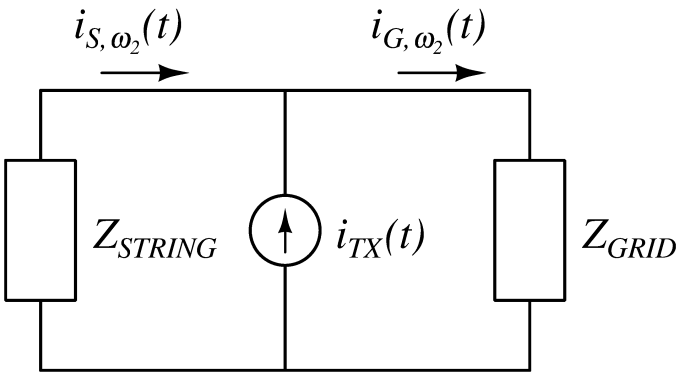

Figure 3.1: Preliminary modeling of the impedance seen by the PLC current injection by applying superposition to analyzed only the transmitted current.

To minimize power dissipation and any grid-side interference issues, we desire to have $i_{TX} = -i_{S,\omega_2}$. To ensure this, we must have $Z_{GRID} >> Z_{STRING}$ at ω_2. Each inverter module is designed to have the same output filter components and thus the impedance of each module at ω_2 is estimated as seen in equation 3.5 below. This will be assumed for the rest of the communication physical layer design and then analyzed later in the channel model of chapter 4.

$$Z_K = j\omega_2 L_{OUT} || -j/(\omega_2 C_{OUT}) \tag{3.5}$$

The overall string impedance is thus estimated quickly as $Z_{STRING} = NZ_K$ where

N is the number of inverter modules in the string. During the inverter design, the frequency ω_2 and the components L_{OUT} and C_{OUT} are selected appropriately. Given the requirements of the power stage, the values are approximately $5\mu H$ and $10\mu F$, respectively. Selecting the communications frequency to be at least 100 kHz thus assures that one is in a range where C_{OUT} dominates the assumed string impedance. Literature on classic, voltage-based powerline-carrier communications indicates that grid impedances in this frequency range are at least an order of magnitude higher than that of the series combination of $10\mu F$ capacitors [53, 54] As a result, $i_{G,\omega_2} = 0$. Note, this is only an estimate for the start of the physical layer design, the actual analysis is found in chapter 4.

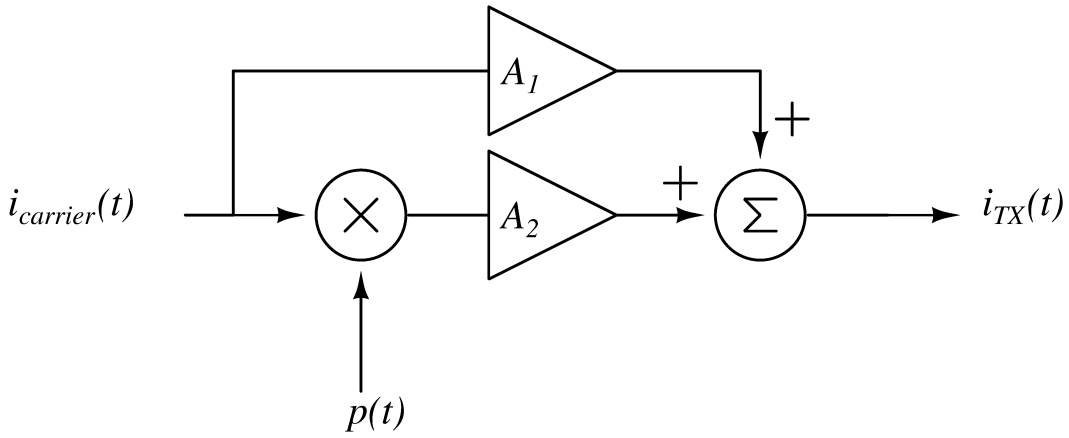

Figure 3.2: Simplified block diagram of the modulation technique for the PLC communications.

The transmitter design scheme is shown in figure 3.2. The carrier signal is a sinusoidal waveform with the frequency selected of 113 kHz. The carrier signal will be added to itself such that part of the carrier is available for the receivers phase locked loop (PLL) will be able to stay locked. The modulation occurs, the inverse of the carrier signal is added to the carrier and the summation of the two will be transmitted. The ideal carrier signal and its inverse is seen in figure 3.3. The gains applied in the transmitter simulation are $A_1 = 1$ and $A_2 = 0.7$.

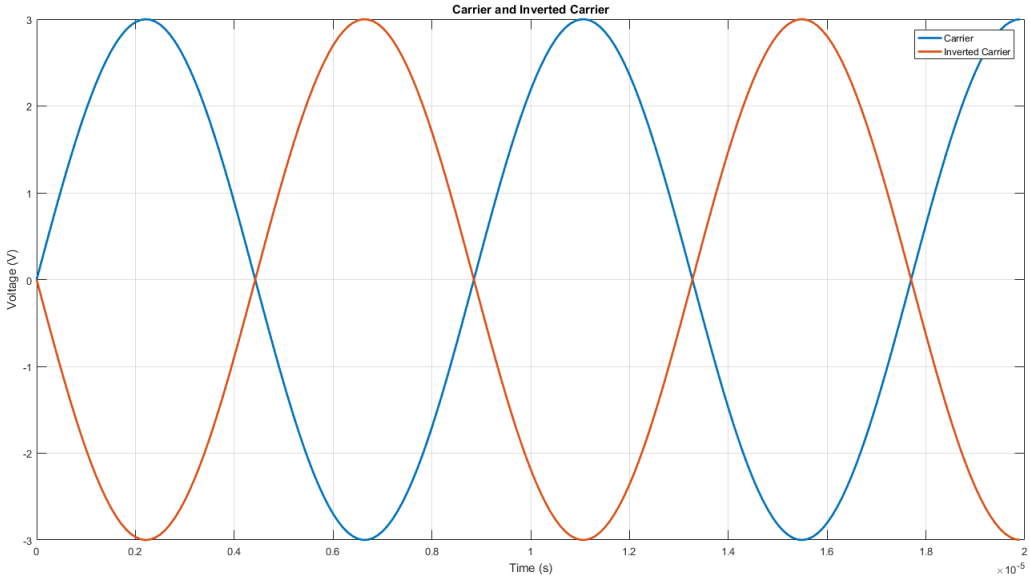

Figure 3.3: Ideal carrier waveform used for the PLC and the inverted carrier utilized for the phase shift keying.

To indicate the phase of the grid voltage, a system connected at the grid interface locates zero crossings. Specifically, a digital filtering algorithm in the microcontroller at the grid interface [11] generates a short pulse every time the grid voltage crosses from negative to positive. Figure 3.4 shows this process.

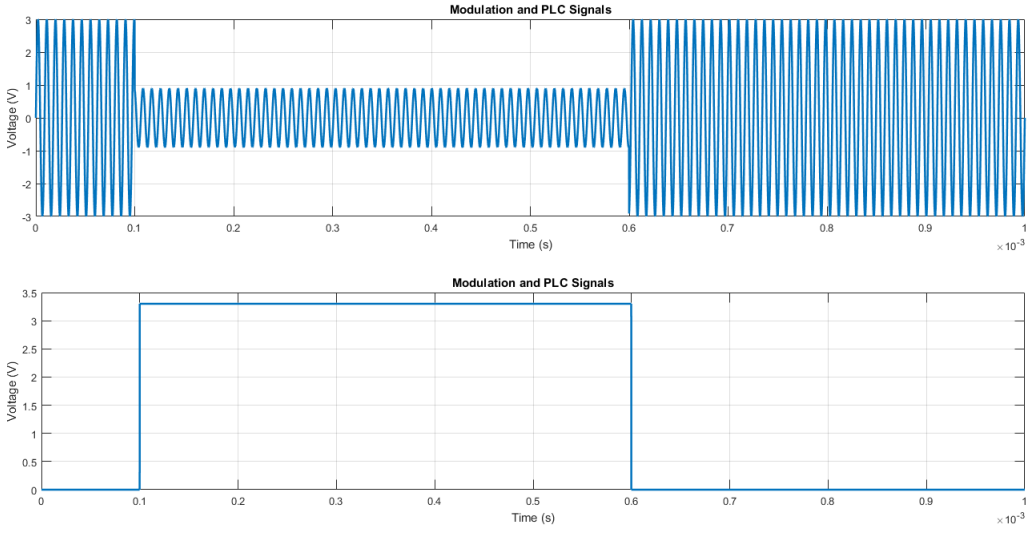

Figure 3.4: Simulation of the BPSK modulation of the PLC.

Note that the synchronization pulse changes state for a brief time Δ at the beginning of each line cycle. This signal is thus modeled as equation 3.6.

$$p(t) = \begin{cases} 1, & nT < t < n(T\Delta) \\ -1, & \text{otherwise} \end{cases} \tag{3.6}$$

where T is the period of the line voltage and n is an integer. The pulse train p(t) is then transmitted to the inverters using binary phase shift keying (BPSK) to yield a transmitted current of the form in equation 3.7 [55]. The final simulation of the transmitter with three BPSK modulations from the grid zero crossing is shown in figure 3.5. The simulations are carried out with voltage values and is expected to be implemented with an integrated circuit (IC) that converts the system voltages to a current.

$$i_{TX}(t) = I_1 p(t) \cos(\omega_s t) + I_2 \cos(\omega_s t) \tag{3.7}$$

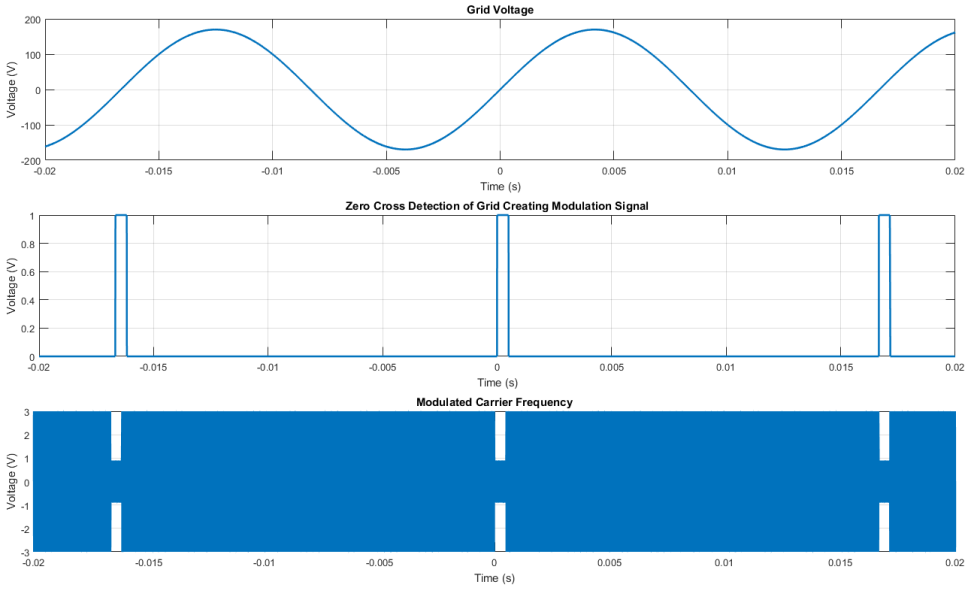

Figure 3.5: Grid zero cross detection scheme. The negative to positive zero crossing is of the grid, top plot, is detected and forms a modulation signal, middle plot, which is used to modulate the carrier frequency creating a BPSK signal for synchronization.

Figure 3.6 shows the block diagram of the prototype system designed and implemented to meet the specifications provided in the previous section. This prototype has three major subsystems, namely the front end, the demodulator, and the automatic gain controller (AGC).

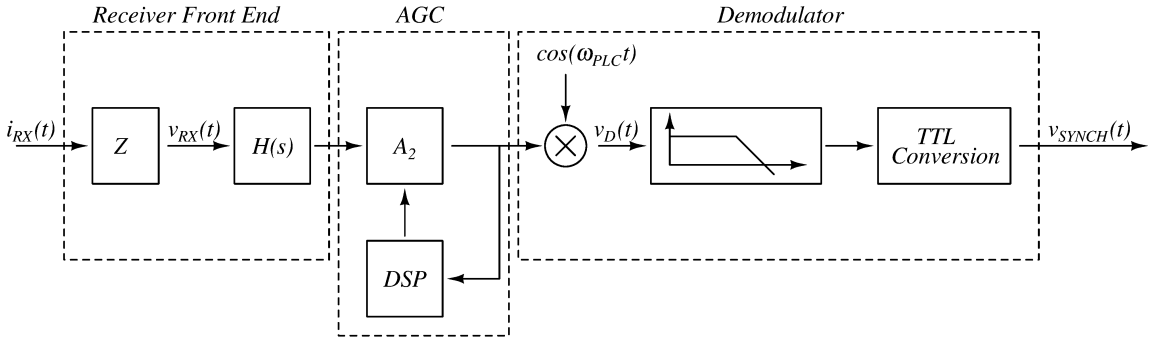

Figure 3.6: Block diagram of the physical receiver layer.

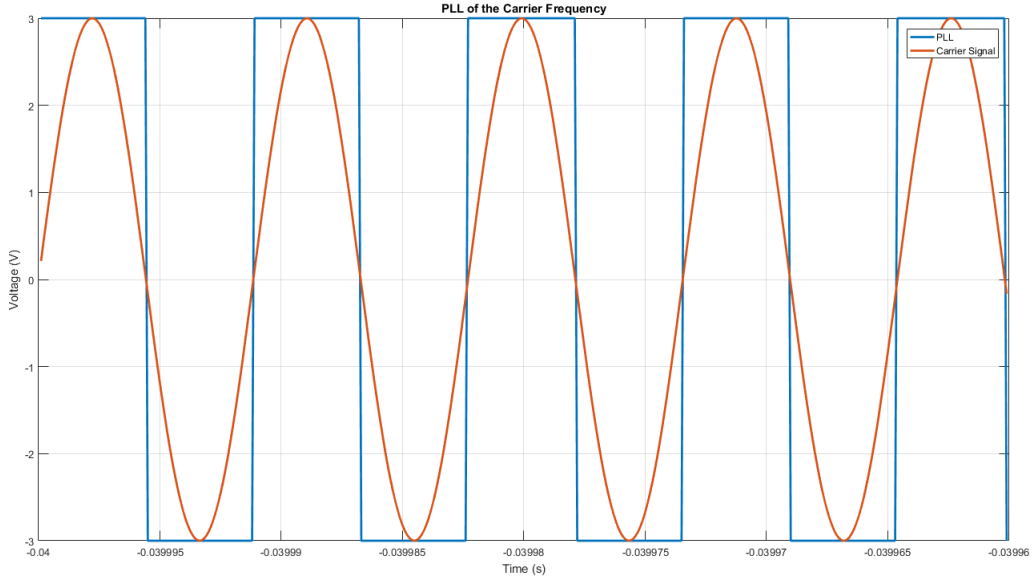

Figure 3.7: Simulation of the PLL for the demodulation circuit to detect the carrier frequency.

For the purpose of designing the demodulation scheme, on the demodulator is simulated. The PLL block is implemented by locking a square wave to the carrier frequency detected by the receiver as seen in figure 3.7. This square wave multiplication is the same as depicted in the block diagram since the square wave contains

a fundamental sinusoid of the same frequency of the carrier, but also includes higher order harmonics of the carrier frequency. This is seen by the trigonometric Fourier series of the square wave as seen in equation 3.8 where V_{PLL} is the peak voltage [56].

$$v_{PLL}(t) = V_{PLL}\frac{4}{\pi}\left(\cos(\omega_2 t) - \frac{1}{3}\cos(3\omega_2 t) + \frac{1}{5}\cos(5\omega_2 t) - \frac{1}{7}\cos(7\omega_2 t) + ...\right) \quad (3.8)$$

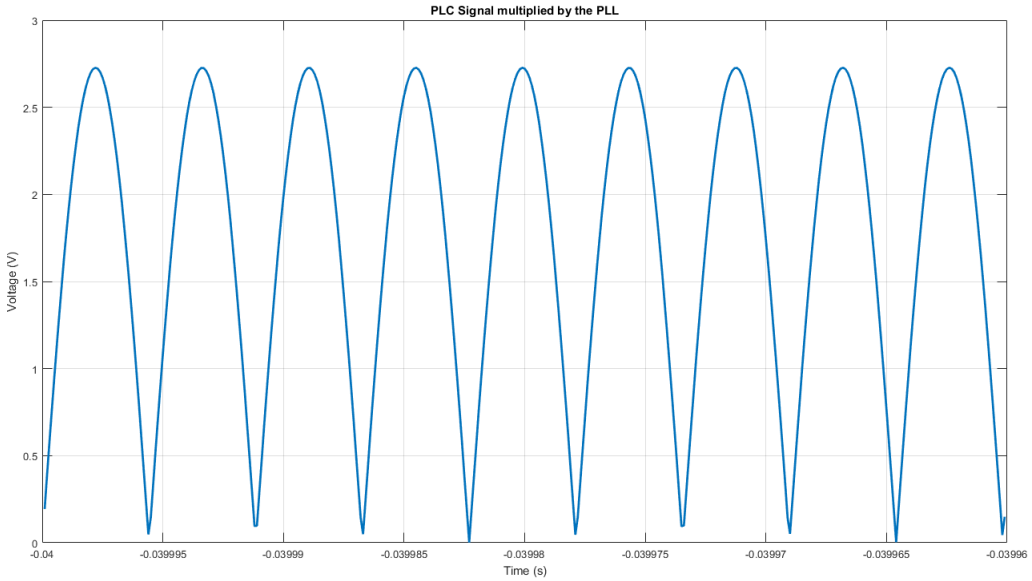

Figure 3.8: Simulation of the ideal demodulation before filtering.

The resulting multiplication of the received carrier without any BPSK modulation is shown in figure 3.8. This waveform can visually be seen to be the scaled absolute value of the carrier signal. Equation 3.9 describes this mathematically.

$$v_D(t) = V_{PLL}\,|v_{in}(t)| \quad (3.9)$$

Even though the expression as the absolute value is simplistic, it does not allow for the mathematical analysis of the low pass filter following the multiplication. To see this analysis, the multiplication must be rewritten as in equation 3.10 and then

transformed by the sum to product identity as seen in equation 3.12 [57].

$$v_D(t) = V_{in}\cos(\omega_2 t)V_{PLL}\frac{4}{\pi}\left(\cos(\omega_2 t) - \frac{1}{3}\cos(3\omega_2 t) + ...\right) \tag{3.10}$$

$$v_D(t) = \frac{4V_{in}V_{PLL}}{\pi}\left(\cos(\omega_2 t)\cos(\omega_2 t) - \frac{1}{3}\cos(\omega_2 t)\cos(3\omega_2 t) + ...\right) \tag{3.11}$$

$$v_D(t) = \frac{2V_{in}V_{PLL}}{\pi}\left(1 + \cos(2\omega_2 t) - \frac{1}{3}\cos(2\omega_2 t) - \frac{1}{3}\cos(4\omega_2 t) + ...\right) \tag{3.12}$$

Modifying the values in the product to sum transformation of equation 3.12 to terms of the of the received current transmitter, the final equation is expressed in equation 3.13.

$$v_D = ZA_2\left[\frac{I_1}{2}p(t) + \frac{I_1}{2}p(t)\cos(2\omega_S t) + \frac{I_2}{2} + \frac{I_2}{2}\cos(2\omega_S t)\right] \tag{3.13}$$

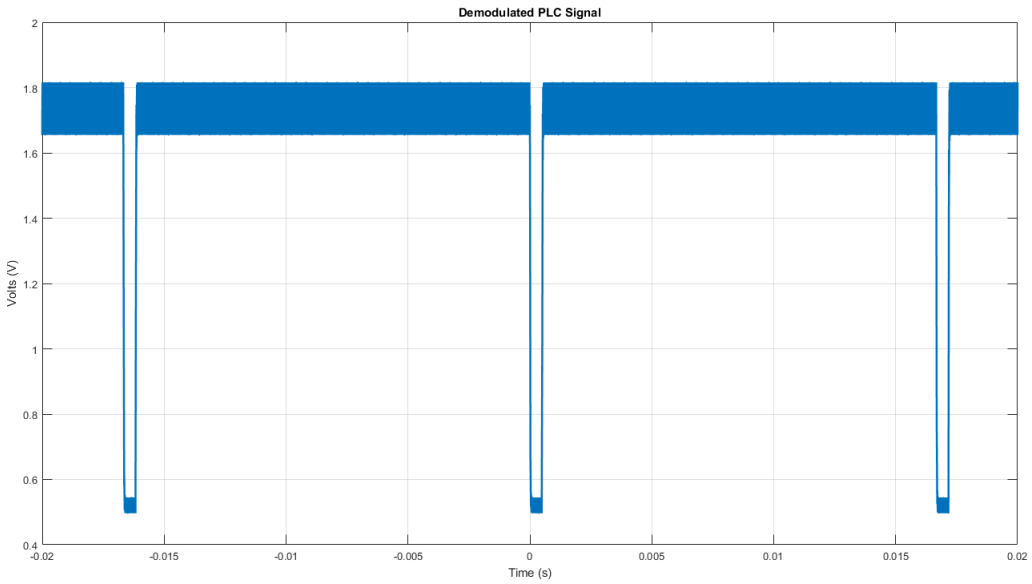

Figure 3.9: Simulation of the ideal demodulation after filtering.

Sizing the low pass filter such that the DC component of the output is allowed but the higher frequencies are attenuated will leave the necessary component to recover the BPSK modulation. The low pass filter is designed with a low pass cut off frequency

of approximately 16 kHz. The result of the low pass filter while functioning as the demodulator is seen in figure 3.9.

The final step in the demodulation process is the determination of the bit output of the filter output. This deterministic selector is simulated using a Schmitt trigger where the signal level has to drop below the determined value before the output bit is toggled, and then rise above a higher value before resetting the output bit. This keeps the output from possibly bouncing if the signal approaches the threshold values. The final output of the simulation showing the resulting demodulation is shown in figure 3.10.

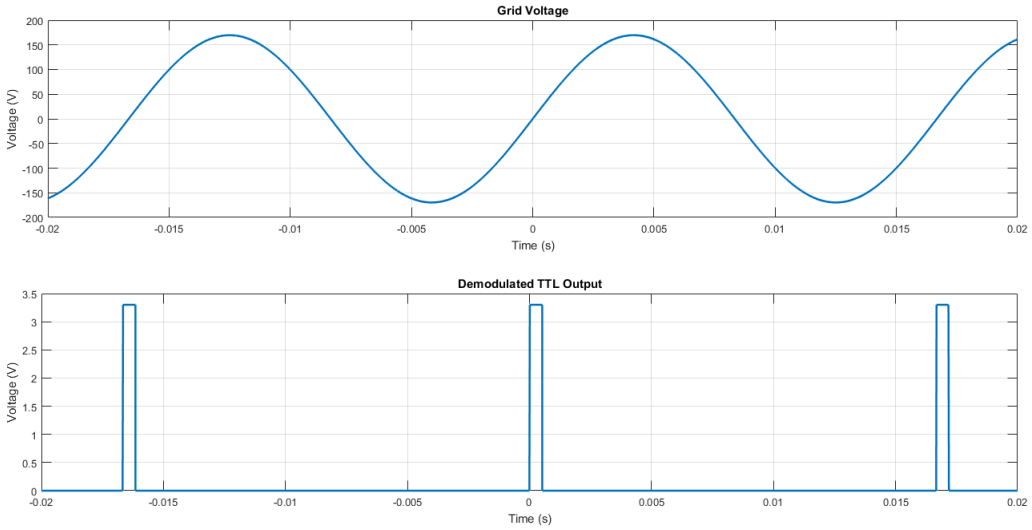

Figure 3.10: Simulation of the ideal demodulation final TTL output.

3.2 Implementation of the Physical Receiver Layer

The physical implementation of the receiver layer has quite a few more individual components comprising the blocks of figure 3.6. The full block diagram including individual components is seen in figure 3.11. This section of the dissertation will explain the implementation of each of these components.

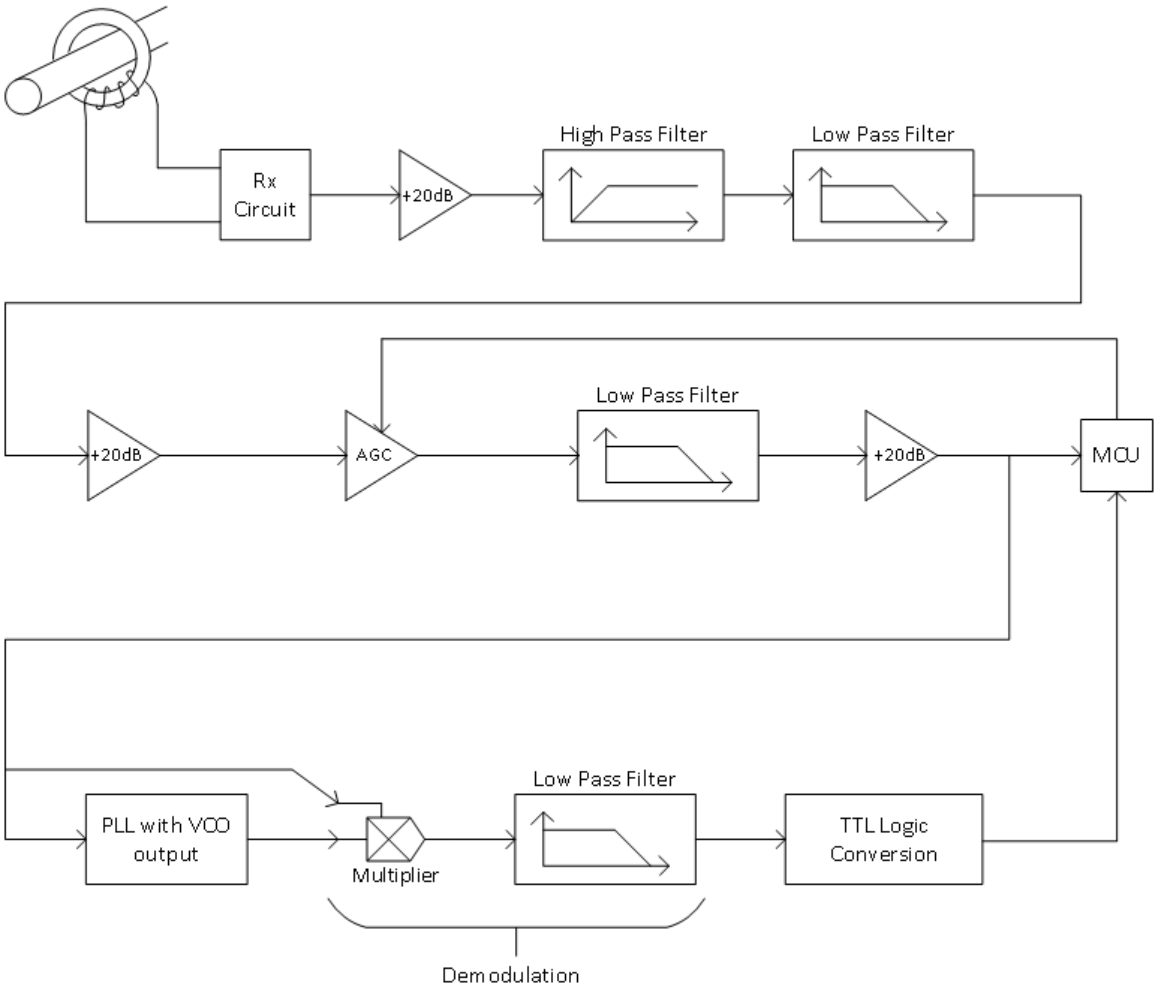

Figure 3.11: Block diagram of the full PLC receiver showing the different modules to detect and demodulate the communication signal.

The front end of each inverter's receive system consists of a current transformer and appropriate signal-conditioning circuitry as shown in figure 3.12. A highly permeable core is desirable, but the saturation flux density of most commercially available materials is such that a large and hence expensive core is needed to avoid saturation [58]. As an alternative, our coils are wound on a nylon spacer and thus have a permeability close to that of free space [58]. The nylon spacer is thus larger than the preferred solution and has an outer diameter of 1 inch. The full physical size of the nylon spacer can be found in figure 3.13. The 10AWG powerline runs through the center of each core as shown in figure 3.14. Sixty-five turns of 22AWG magnet wire are wrapped

around each spacer thereby giving a turns ratio of 1:65. This turns ratio value, N_1 to N_2 will be used in later calculations.

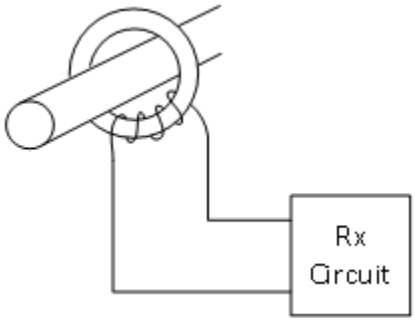

Figure 3.12: The receiver coil wraps around the power line to couple the PLC signal to the receiver circuit.

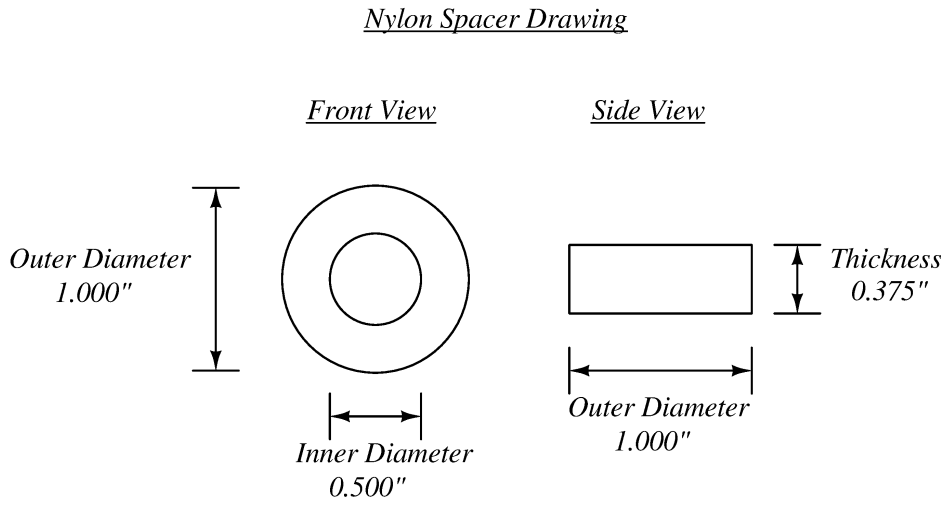

Figure 3.13: Physical drawing of the nylon spacer used for the implementation of the receiver coil.

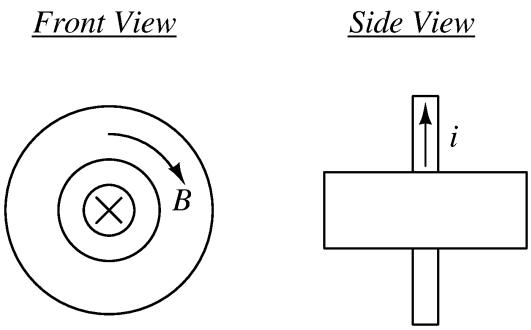

Figure 3.14: Physical drawing of the nylon spacer showing the current conduction and corresponding $\vec{B}$ field.

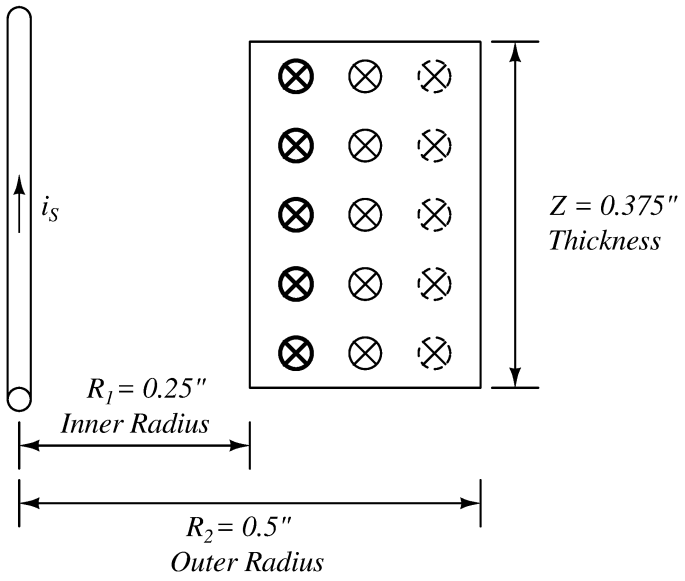

Figure 3.15: Drawing of the $\vec{B}$ field inside a cross section of the receiver coil showing the non-uniform $\vec{B}$ field in the x direction.

The current passing through the powerline induces a magnetic field around the powerline. This magnetic field has a non-uniform flux density based on the distance from the wire that flows through the cross section of the secondary winding of the current transformer and is seen in figure 3.15. Assuming the powerline passes through the exact center of the coil orthogonal to the face of the spacer as shown in figure 3.14, then the flux density $\vec{B}$ can be approximated as [59]

$$\vec{B} = B(r)\hat{\phi} \tag{3.14}$$

At a given radius r, the flux density is constant and its strength can be determined from Ampère's law. The resulting integral is [59]

$$\oint \vec{B} \cdot d\vec{s} = \mu_0 i_S \tag{3.15}$$

Using equation 3.14 and noting that $d\vec{s} = rd\phi\hat{\phi}$, equation 3.15 becomes

$$\int_0^{2\pi} B(r) = 2\pi r B(r) \tag{3.16}$$

Equating the right-hand sides of both equations 3.16 and 3.16, we find

$$\vec{B} = \frac{\mu_0 i_S}{2\pi r}\hat{\phi} \tag{3.17}$$

The total flux Φ through the coil is determined by integrating equation 3.17 over the cross-sectional area of the coil as shown in figure 3.15. We thus have [59]

$$\Phi = \int \vec{B} \cdot d\vec{a} \tag{3.18}$$

$$d\Phi = \vec{B} \cdot d\vec{a} \tag{3.19}$$

With respect to the parameters defined in figure 3.15, we see that $d\vec{a} = Zdr\hat{\phi}$, and thus equation 3.18 is derived below to equation 3.24.

$$d\Phi = \left(\frac{\mu_0 i_S}{2\pi r}\right)\hat{\phi}\,(drz) \tag{3.20}$$

$$\Phi = \int_{R_1}^{R_2} \frac{\mu_0 i_S Z}{2\pi r} dr \tag{3.21}$$

$$\Phi = \frac{\mu_0 i_S Z}{2\pi} \int_{R_1}^{R_2} \frac{1}{r} dr \tag{3.22}$$

$$\Phi = \frac{\mu_0 i_S Z}{2\pi} \left[\ln\left(R_2\right) - \ln\left(R_1\right)\right] \tag{3.23}$$

$$\Phi = \frac{\mu_0 i_S Z}{2\pi} \ln\left(\frac{R_2}{R_1}\right) \tag{3.24}$$

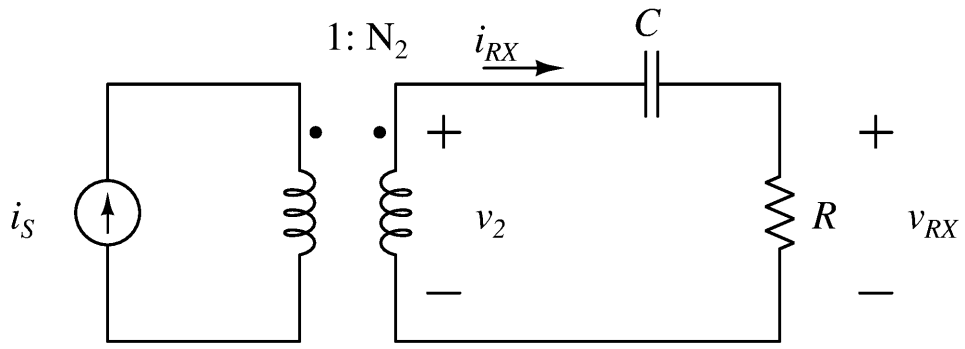

Figure 3.16: Circuit model for the actual current transformer and its interface circuit.

To determine the received signal, we model the coil as shown in figure 3.16. The powerline current $i_S(t)$ is represented as a current source driving the primary. Using the model given here, the self-inductance of the primary is

$$L_{11} = \frac{\Phi}{i_S} \tag{3.25}$$

and the mutual inductance is

$$L_{12} = L_{21} = \frac{N_2 \Phi}{i_S} \tag{3.26}$$

A similar analysis shows that

$$L_{22} = N_2 L_{12} \tag{3.27}$$

In terms of these definitions, the voltage at the secondary is

$$v_2(t) = L_{21} \frac{di_S}{dt} - L_{22} \frac{di_{RX}}{dt} \tag{3.28}$$

To attenuate low-frequency content and to convert $i_{RX}(t)$ to a voltage, a high-pass filter is connected as shown in figure 3.16. The overall transfer function is fully found in equation 3.29.

$$\frac{V_{RX}}{I_S} = \frac{-s^2 L_{21} CR}{s^2 C L_{22} + sRC + 1} \tag{3.29}$$

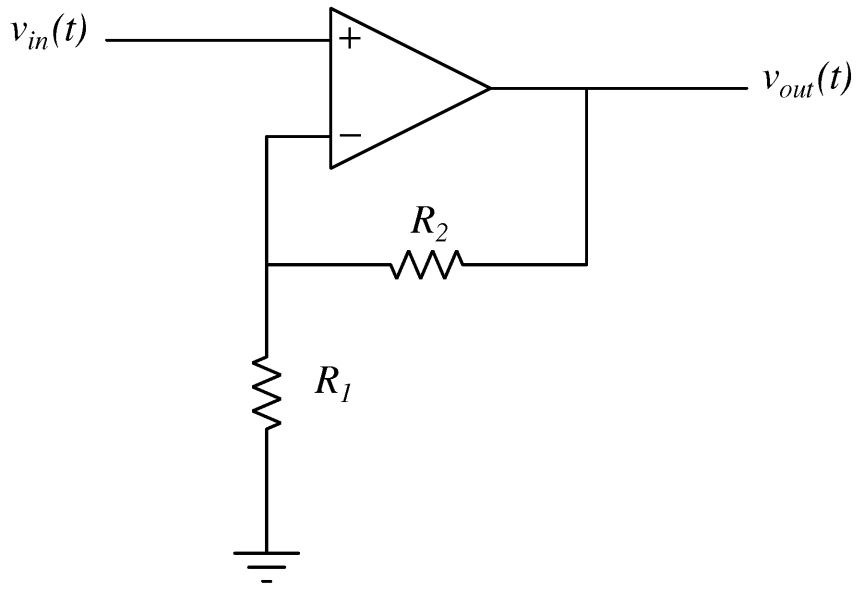

Figure 3.17: A non-inverting amplifier configuration used in the design of the gain stages.

After the receiver front end is the pre-amp to boost the gain before any active filtering is applied to remove the noise outside the communications band. This pre-amp is a single ended, non-inverting amplifier as seen in figure 3.17. The gain is determined by the ratio $-R_2/R_1$ [60] and is configured for $-10\,V/V$ or $+20\,dB$.

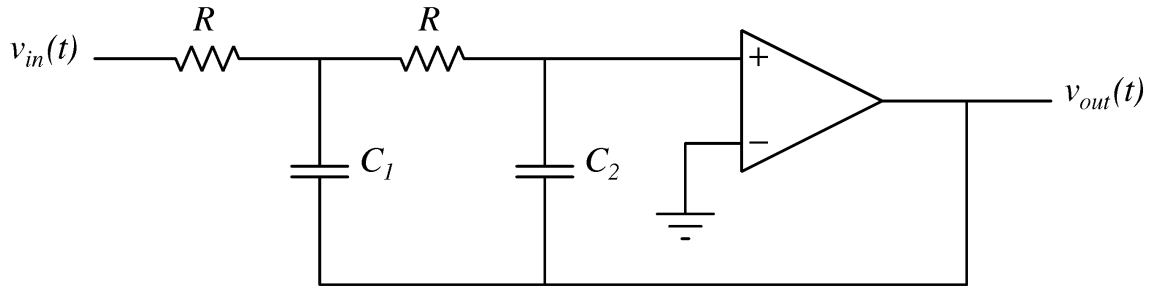

Figure 3.18: A second order Sallen-Key low pass filter used to implement the low pass filtering blocks.

After the pre-amp stage, the receiver has a filtering stage to filter out both the high and low frequencies not in the communications frequency band. Instead of implementing both the high and low frequency filtering in a band-pass stage, it is split into a separate low pass and high pass filter. The first filter analyzed here is

the low pass filter implemented with a second order, unity gain, Sallen-Key low pass filter design as seen in figure 3.18. The transfer function of the filter is defined in equation 3.30. To design with this filter, a cutoff frequency must be defined based on the RC values of the filter and a damping ratio ζ. The capacitor values used in the implementation are then evalutaed based on the C and ζ values as seen in equations 3.32 - 3.33 [61].

$$A_V = \frac{v_{out}(t)}{v_{in}(t)} = \frac{{\omega_0}^2}{s^2 + 2\zeta\omega_0 s + {\omega_0}^2} \tag{3.30}$$

$$\omega_0 = \frac{1}{RC} \tag{3.31}$$

$$C_1 = \frac{C}{\zeta} \tag{3.32}$$

$$C_2 = \zeta C \tag{3.33}$$

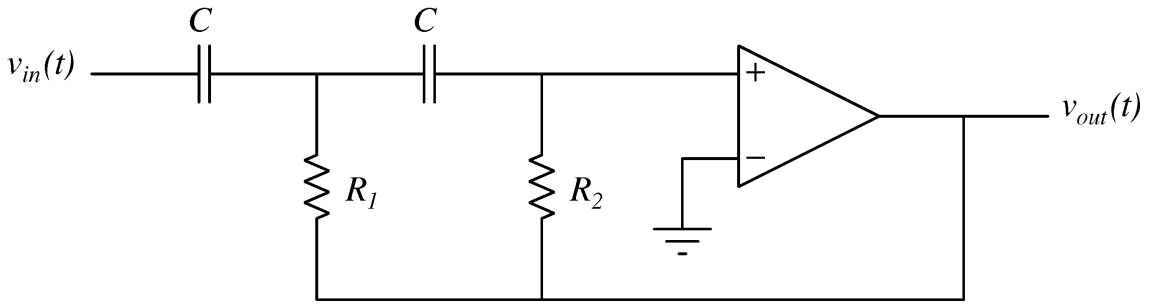

Figure 3.19: A second order Sallen-Key high pass filter used to implement the high pass filtering blocks.

The second filter analyzed is the high pass filter implemented with a second order, unity gain, Sallen-Key high pass filter design as seen in figure 3.19. This is the compliment to the Sallen-Key low pass filter previously described. The transfer function of the filter is defined in equation 3.34. To design with this filter, a cutoff frequency must be defined based on the RC values of the filter and a damping ratio ζ. The resistor values used in the implementation are then evalutaed based on the C and ζ values as seen in equations 3.32 - 3.33 [61].

$$A_V = \frac{v_{out}(t)}{v_{in}(t)} = \frac{{\omega_0}^2}{s^2 + 2\zeta\omega_0 s + {\omega_0}^2} \tag{3.34}$$

$$R_1 = \zeta R \tag{3.35}$$

$$R_2 = \frac{R}{\zeta} \tag{3.36}$$

The low and high pass, unity gain, Sallen-Key filters are utilized as the building blocks for designing the low and high pass filters in the block diagram of 3.11. These filters are implemented as a Butterworth filter and uses the design parameters from figure 3.20.

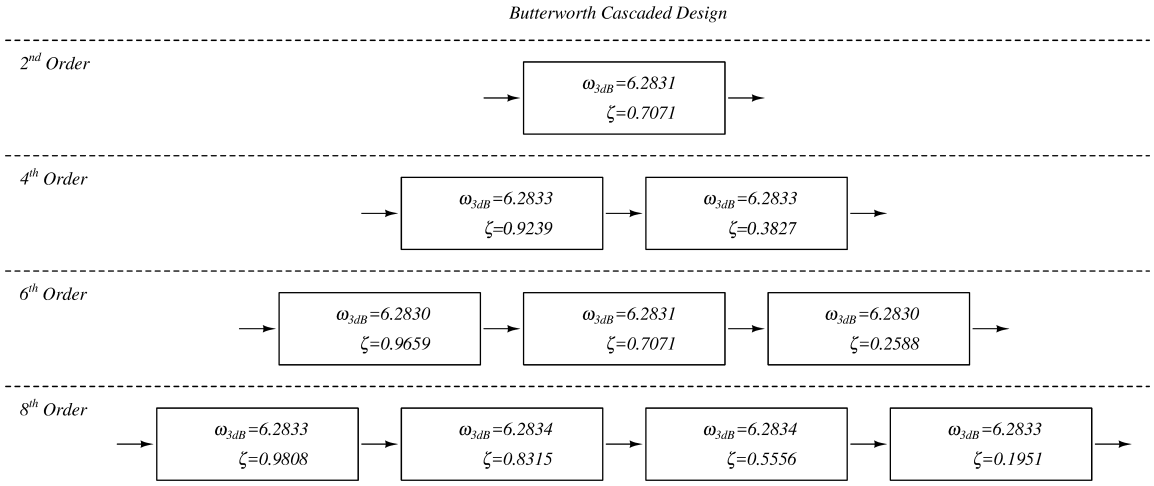

Figure 3.20: Design parameters for cascaded Butterworth filter designs utilized for the high and low pass filters.

The first filter is a 2nd order, Butterworth, high pass filter and is implemented as a with the design parameters of table 3.1. The cutoff frequency is selected at 10 kHz, a decade lower than the communications frequency of 113 kHz to ensure no attenuation. The primary interest of this filter is to ensure that the 60 Hz current component of the power line is completely attenuated from impacting the receiver as this current is many magnitudes larger than the communications frequency. The attenuation from the filter will be much larger than $-80\,dB$ for the line frequency.

Table 3.1: Design parameters and component values for the 2nd order Sallen-Key high pass filter used in the PLC receiver.

Parameter	Stage 1
f_c	10 kHz
ω_{3dB}	62.831×10^3 rad/s
ζ	0.7071
R	15.9155 kΩ
C	1000 pF, 5 %
R_1	11 kΩ, 1 %
R_2	22 kΩ, 1 %

The second filter is a 6th order, Butterworth, low pass filter and is implemented with the design parameters of table 3.2. The filter is designed with a cutoff frequency of 250 kHz, slightly more than an octave above the communications frequency and exactly one octave below the switching frequency of the power electronics of the inverter module. The filter is designed to remove the switching noise from the receiver and provides roughly $-36\,dB$ of attenuation at the switching noise frequency.

Table 3.2: Design parameters and component values for the 6th order Sallen-Key low pass filter used in the PLC receiver.

Parameter	Stage 1	Stage 2	Stage 3
f_c	250 kHz	250 kHz	250 kHz
ω_{3dB}	$1.570\,75 \times 10^6$ rad/s	$1.570\,78 \times 10^6$ rad/s	$1.570\,75 \times 10^6$ rad/s
ζ	0.9659	0.7071	0.2588
R	3.9 kΩ, 1 %	3.9 kΩ, 1 %	3.9 kΩ, 1 %
C	163.241 pF	163.238 pF	163.241 pF
C_1	180 pF, 5 %	240 pF, 5 %	620 pF, 5 %
C_2	160 pF, 5 %	120 pF, 5 %	430 pF, 5 %

Following the filtering stages to clean up the received signal is another amplifier stage, referred to as the main amplifier. This amplifier boosts the signal by $20\,dB$ and is implemented exactly the same way as the pre-amp. Reusing functional blocks simplifies the design process and reduces the design time.

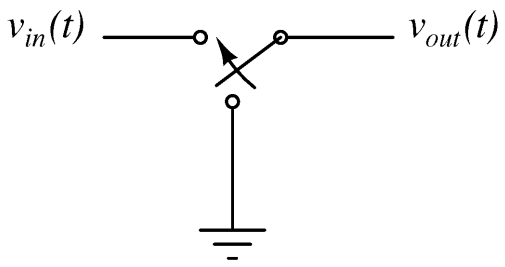

Figure 3.21: Switching strategy for gain control to produce a fundamental frequency of the input voltage with a gain reduction proportional to the duty cycle.

Following the main amplifier comes the automatic gain control (AGC) stage. This stage consists of two components, the gain reduction and the feedback path. Analyzed first is the gain reduction with the feedback path analyzed after the functional blocks before the PLL are described. The gain reduction is implemented using a PWM chopper circuit with the concept illustrated in figure 3.21. The output voltage of the PWM chopper is either the input voltage or 0 V based on the duty cycle. This is expressed below in equation 3.37 and represents a time domain solution based on the duty cycle case.

$$v_{out}(t) = \begin{cases} v_{in}(t), & nT < t < n(T\Delta) \\ 0, & \text{otherwise} \end{cases} \tag{3.37}$$

As in the case with the PLL multiplication of the demodulation, the pulse wave of the duty cycle can be converted to a Fourier series expansion with the fundamental frequency being the switching frequency of the PWM chopper. This is implemented at 500 kHz. The output voltage can then be abbreviated as in equation 3.38.

$$v_{out}(t) = Dv_{in}(t) + \text{Higher Order Terms} \tag{3.38}$$

The chopped output is then filtered to attenuate the higher frequencies and leave the scaled carrier frequency. This is accomplished by the use of a 6th order, Butterworth, low pass filter. As the name implies, it is accomplished by using the previously designed filter using the Sallen-Key amplifier. The filtered signal is then passed into the final amplifier referred to as the post-amp stage. This amplifier is a functionally the same as the last two gain stages with a $-10V/V$ or $10\,dB$ gain.

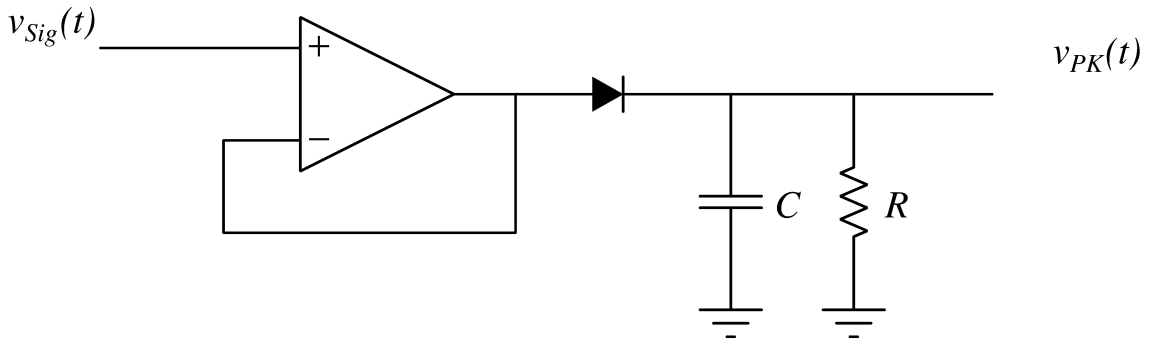

Figure 3.22: A peak rectifier circuit utilized to determine the magnitude of the signal.

The feedback path of the automatic gain control is implemented with a digital control in the microcontroller based on the peak voltage into the PLL. The signal is buffered into a peak rectifier with a large RC time constant such that the decay will not be significant between the two peaks of the carrier frequency. The peak rectifier is seen in figure 3.22. The peak voltage, $v_{pk}(t)$ is then sampled by the analog to digital converter (ADC) of the microcontroller. The microcontroller then compares the peak value to a the desired value to see the error and adjusts the duty cycle, D, accordingly. The gain control is only adjusted during startup of the system since the receiver will not know what signal strength the transmitter is transmitting at. The signal strength could be much larger than expected, or it could be much smaller. The receiver can only guess at startup and then adjust to correct the error. After the value is determined, it will not change in the system while everything is powered and operating.

A phase-locked loop (PLL) generates the carrier. This circuit is implemented using

the HEF4046 [62]. The PLL was designed to have a free-running frequency of $113\,kHz$ and a lock range of $\pm 5\,kHz$. A proportional-plus-integrator (PI) compensator is used as the loop filter to yield zero steady-state phase error [63]. The voltage controlled oscillator (VCO) within the PLL ultimately produces a square wave with a frequency ω_2. This waveform is mixed with the amplified and filtered version of the voltage $v_{RX}(t)$. Assuming these circuits are well designed, this voltage is proportional to the current presented in equation 3.7. The VCO output is represented as a Fourier Series of the form below in equation 3.39.

$$v_{vco}(t) = \sum_{n=1,\ n\ \text{odd}}^{\infty} \frac{4}{\pi n} \cos\left(n\omega_2 t\right) \tag{3.39}$$

In the exact same approach as the simulation, the received signal is multiplied with the VCO generated from the PLL. The multiplication is performed by implementing a switch, similar to the PWM chopper of figure 3.21, and is seen in figure 3.23. Here, $q(t)$ is the VCO output that is aligned to the carrier frequency. In a proof to verify the operation, assuming no modulation is occuring, the the switch selects $v_{in}(t)$ when positive based on the positive value of VCO. When $v_{in}(t)$ becomes negative, the switch selects the inverted signal and the output once again has a positive signal. Effectively happening is the output taking the absolute value of the signal as analyzed in the matlab simulation earlier. This inverse input of the receiver is formed by passing the post-amp output through an inverting amplifier, as seen in figure 3.24, with a gain of $0\,dB$ by setting R_1 equal to R_2 [60].

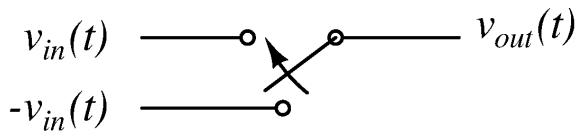

Figure 3.23: Switch-based multiplier used to mix the received signal with the carrier. The resulting process, along with a low pass filter, will recover the modulated signal.

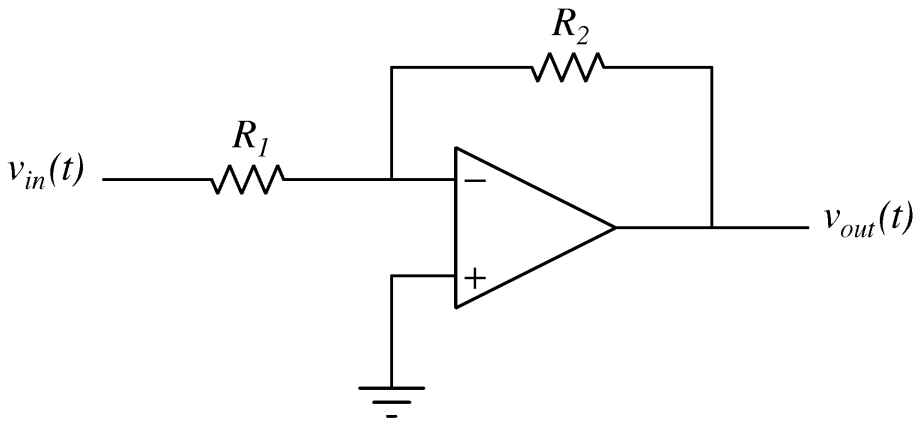

Figure 3.24: An inverting amplifier configuration used in the PLL multiplication stage of the receiver.

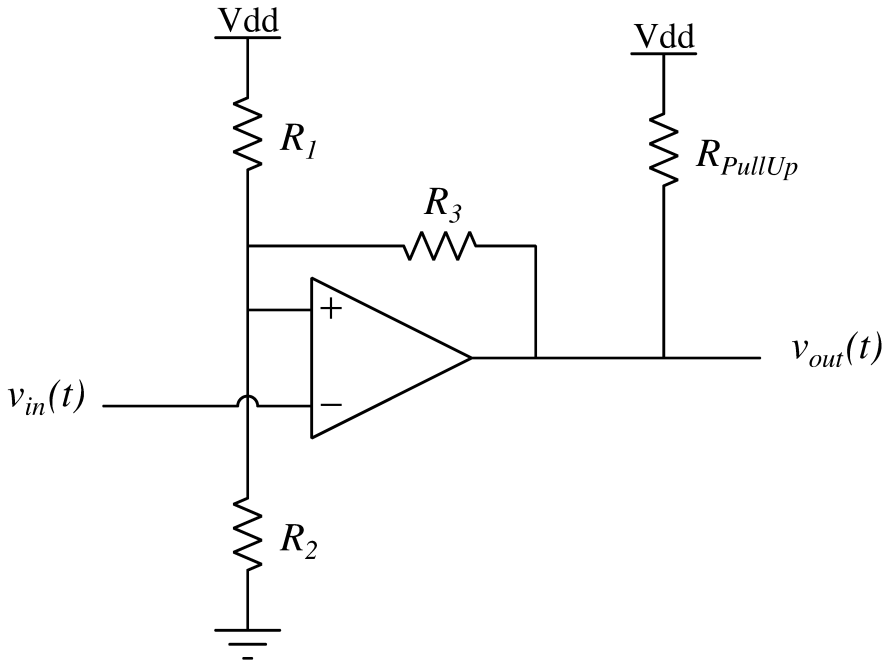

Figure 3.25: The Schmitt trigger implementation for conversion of the demodulated signal to a TTL output. The circuit operates with an open collector design such that the output voltage has a pull-up resistor to the TTL logic level.

After mixing, the voltage thus contains a baseband component proportional to $p(t)$ as well numerous harmonics of ω_2. These higher order terms are attenuated using a simple RC low pass filter with a bandwidth of approximately 10 kHz. The resulting analog waveform has an amplitude that varies slightly over time. To convert

this waveform to an appropriate logic signal, it is passed to a Schmitt trigger. The Schmitt trigger is a comparator with hysteresis and operates on the principle of positive feedback such that the input voltage will have two thresholds that will cause the output voltage to change [64]. The voltage levels selected were $0.3\,V$ and $0.7\,V$. The final waveform ultimately passes to an external interrupt pin on the digital signal processor (DSP).

3.3 Implementation of the Physical Transmitter Layer

The physical implementation of the transmitter layer much more complicated for implementation than shown in previously in figure 3.2. The full block diagram including individual components is seen in figure 3.26. This section of the dissertation will explain the implementation of each of these components. Most of the components are selected from already existing designs used in the receiver layer. Those that are not will be explained in more detail.

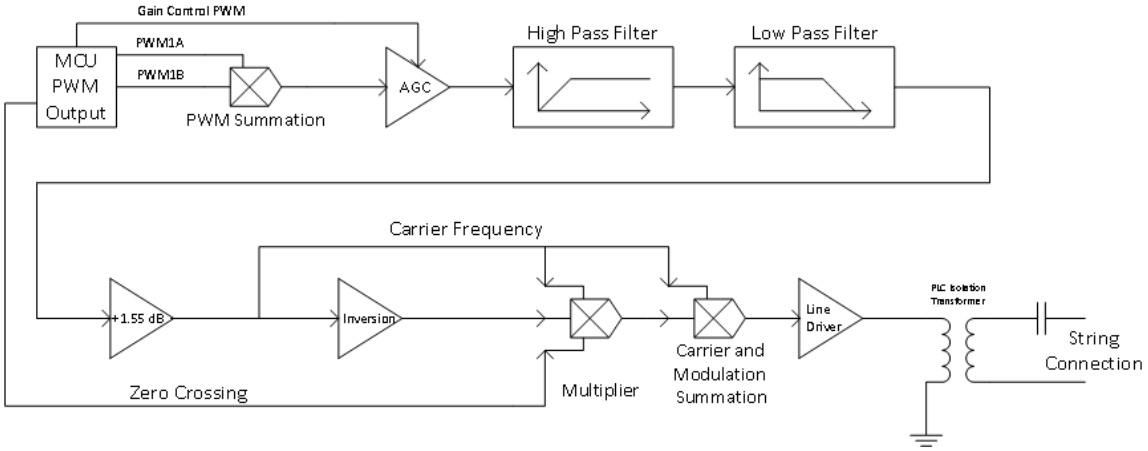

Figure 3.26: Block diagram of the full PLC transmitter showing the different modules to create the carrier and modulate the communications signal.

The first block in the transmitter is the carrier generation from the microcontroller by the use of a two PWM signals. The PWMs operate at a frequency of 113.6 kHz and output a duty cycle of 33% and 66%. THe PWMs are then summed together using a summing amplifier as seen in figure 3.27. Due to the stepping of the output

of the summed PWM signals, all even harmonics and all multiples of the 3rd order harmonics are eliminated from the Fourier Series [65]. The fundamental is much larger than the next term of the series, the 5th harmonic.

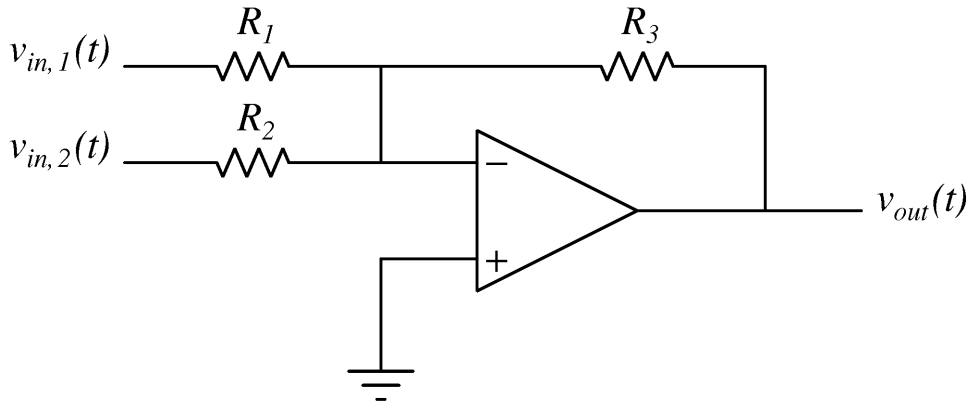

Figure 3.27: A summation amplifier configuration used in the carrier generation from the PWM signals of the microcontroller.

Following the summation is a gain reduction block, implemented with the same switch strategy as the AGC in the receiver was. This gain reduction block is controlled by the PWM output of the microcontroller at the grid interface. The gain control is set up to act as open loop or closed loop control. The feedback path for the closed loop control is the receiver board built into the grid interface.

The next two blocks are a high pass filter and a low pass filter. The high pass filter is a passive, first order filter consisting of a capacitor and resistor with a cut off frequency of 10 kHz. The purpose in this circuit is to remove any DC offset that occurs from the operational amplifiers. The low pass filter is a 6th order, Butterworth filter with a cutoff frequency of 250 kHz. This is the same low pass filter implemented with Sallen-Key stages in the receiver section. This filter attenuates the harmonics from the carrier generation and the gain control.

The fundamental frequency, the carrier frequency, at this point is not operating at the largest value it can in the electronics even if the gain control block did not reduce the gain. This is due to the fact that the fundamental component is a lower

magnitude than the summation of the two PWM signals. To operate the carrier at the maximum value, the gain is increased here with a non-inverting amplifier that has a gain of $1.55\,dB$ or about $1.2\,V/V$.

The modulation is performed based on a switch selection with the selection signal being the grid crossing pulse $p(t)$. This pulse causes a switch to select either the carrier frequency directly or the inverse of the carrier frequency when modulating. The inverse of the carrier frequency is obtained by an inverting op-amp with a gain of $0\,dB$ or $-1V/V$. This block performs exactly the same as the simulated transmitter modulation.

The modulated signal and the carrier are added back together with a summation amplifier with the gains for the two signals being $A_1 = 0.6V/V$ and $A_2 = 0.4V/V$ respectfully to the carrier and the modulated signal. Normalizing the gain A_2 to A_1, the modulated signal is found to be 0.67 the value of the carrier, a slight deviation of the simulated gain. The selection of A_1 and A_2 was done to get a signal level that would maximize the allowable voltage swing of the operational amplifiers as well as adhere to using standard value resistors. A more accurate implementation to the simulation could be performed, but the results do not deviate from the expected enough to justify such effort.

The final signal is sent to the line driver amplifier, a Texas Instruments (TI) OPA561. This amplifier is called a line driver due to the large output current it can source. It is important to mention that this amplifier acts as a buffer to the current transmitted. As such, this where the modeling of the transmitter ends in chapter 4 and the channel modeling begins even though it is not the end of the transmitter's hardware implementation. The line driver output connects to a stability network and then to the isolation transformer. The stability network and isolation transmformer is based on the TI reference design [52] with slight modifications to increase the current limitation. The capacitor at the string side is to prevent the low frequency voltage

of the string from seeing the low impedance path through the isolation transformer and is referred to as a blocking capacitor. Further examination of the transmitter hardware in the communications model will show how the transmitted string current, $i_s(t)$ is estimated from the voltage into the line driver IC, $v_{PLC}(t)$.

3.4 Empirical Results of the Physical Access Layer

The physical access layer was thoroughly tested after the design and implementation to gauge functionality. The transmitter circuit at the grid interface generates the appropriate BPSK signal using a 113kHz carrier waveform. The functionality testing was done with the communications signal transmitted on a separate wire and

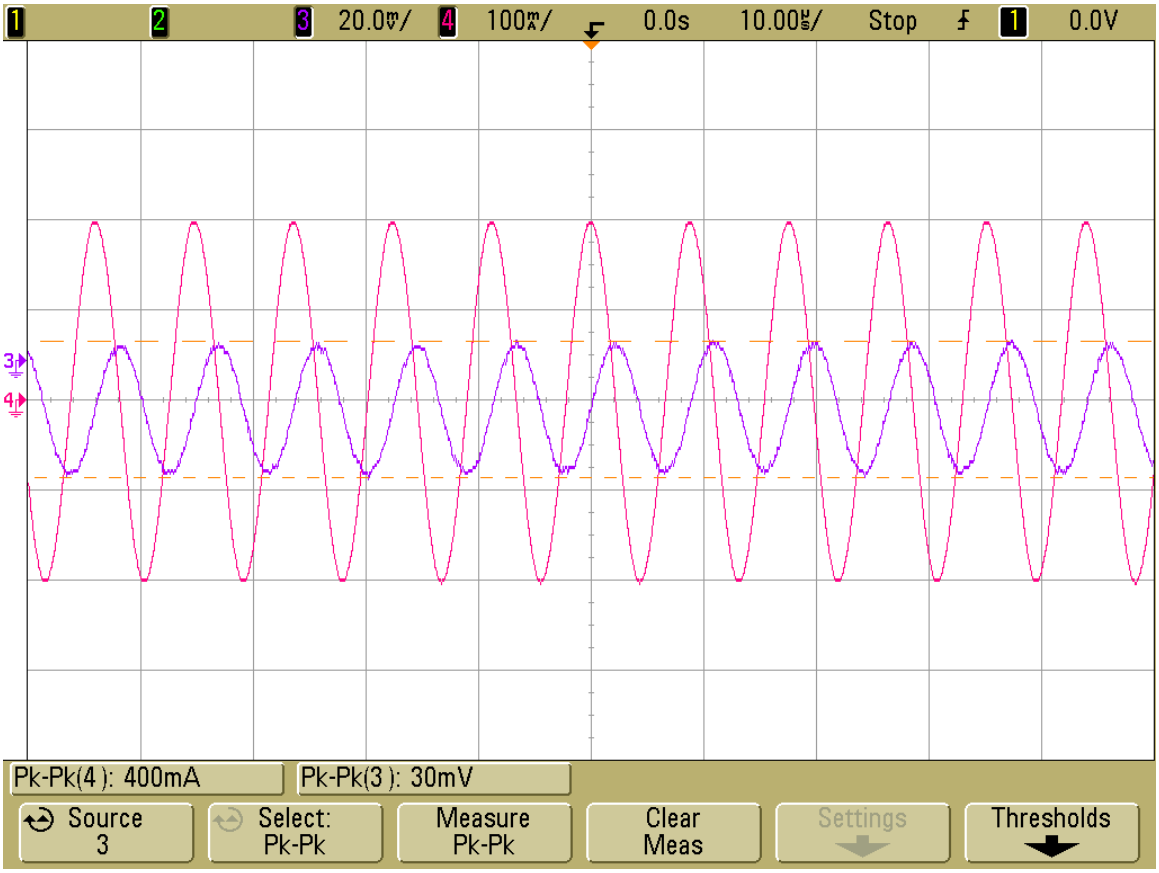

Figure 3.28: The receiver frontend detects the synchronization signal through the current transformer. The injected current, shown as trace 4 in red, is transformed into a voltage signal, shown as trace 3 in purple, based on the transfer function relation presented in equation 3.29. The magnitude of the output, 30 $mV_{pk\text{-}pk}$ for a 400 $mA_{pk\text{-}pk}$ input verifies the relation. A slight DC offset occurs due to the input bias of the op-amp and scope calibration.

not the powerline to both ease the development of the inverter and communications hardware. Results with the communications signal integrated onto the powerline will be shown in chapters 4 and 6.

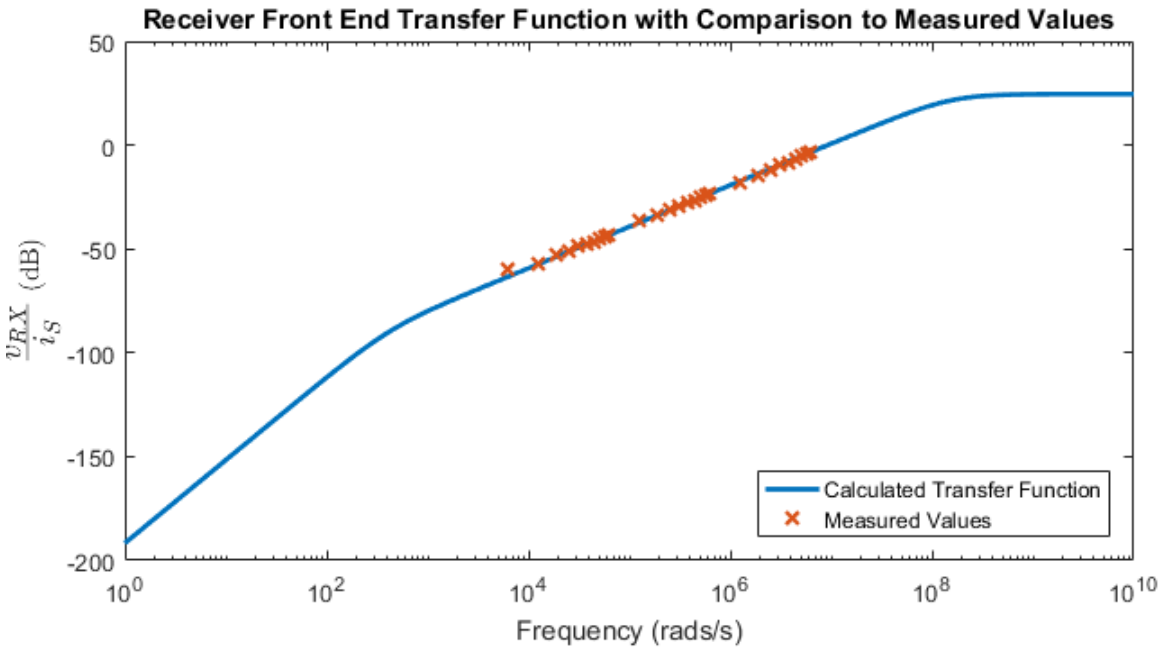

Figure 3.29: Predicted (solid line) and measured frequency response of the receiver front end over a range from 1 kHz to 1 MHz.

The first test of the receiver is examining how close to the model the current transformer and receiver front end perform. Measurements show that L_{22} is $7\mu H$ and L_{21} is $0.108\mu H$. Similarly, the resistor and capacitor from figure 3.16 are $1.1k\Omega$ and $2.2\omega F$, respectively. Figure 3.28 shows the voltage $v_{RX}(t)$ when using a $400mA_{pk\text{-}pk}$ carrier waveform and the component values provided previously. Note that the measured amplitude is approximately $30mV_{pk\text{-}pk}$. This value is extremely close to that predicted by equation 3.29. Figure 3.29 compares the measured and predicted values when performing a sweep over several potential carrier frequencies. Note the close agreement. In practice, of course, the carrier frequency is constant; it was modified in this case only for purposes of validating the predicted results [66].

Figure 3.30 illustrates the operation of the AGC. Note that the received waveform

(yellow), is mixed with the PWM waveform (green). The mixer output (red) is filtered to recover the scaled and shifted version of the input shown in purple. The amplitude of this waveform is adjusted by changing the duty ratio of the PWM output (green). In this example, the duty ratio is 15%. Note that this implementation was selected because of the relative ease of implementing it on an integrated circuit.

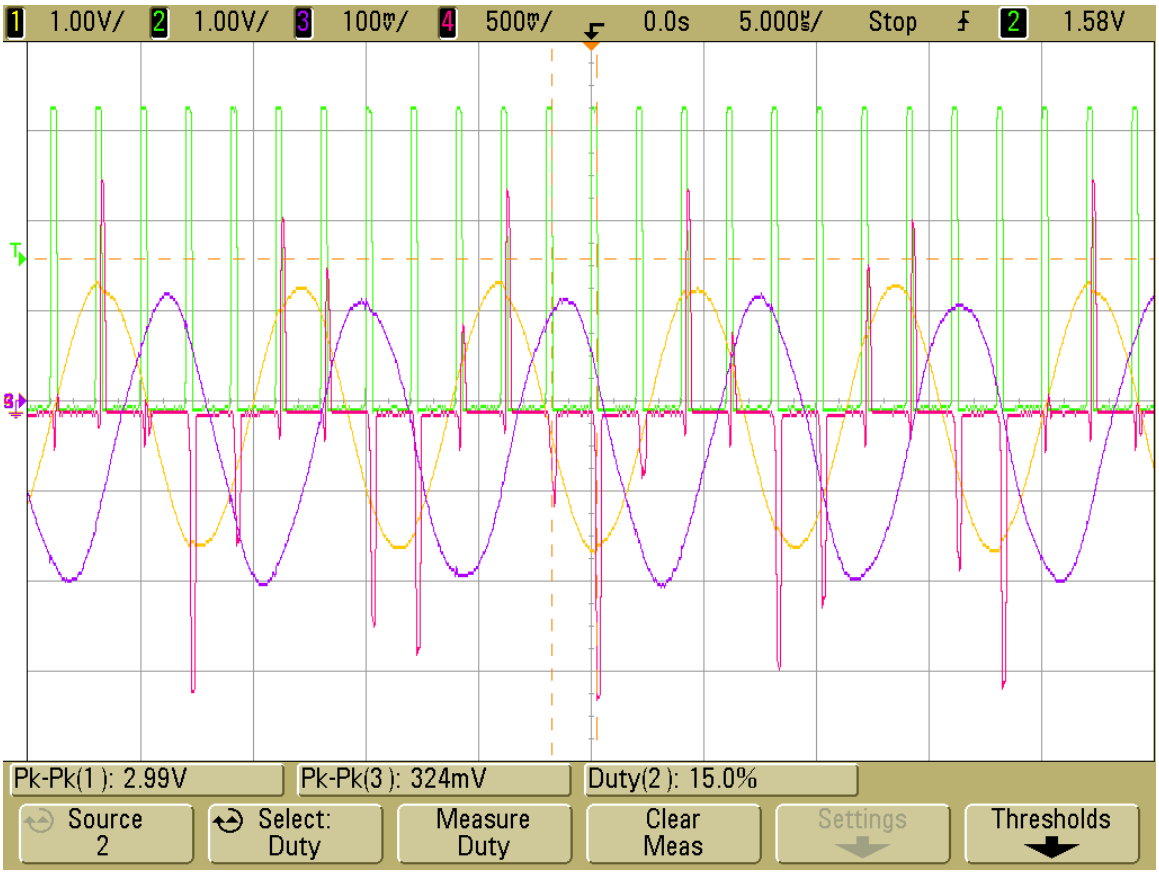

Figure 3.30: Implementation results of the automatic gain control. The automatic gain control signal input, trace 1 in yellow, is chopped by the PWM signal, trace 2 in green. The output, trace 4 in red, appears as a pulse train whose amplitude matches that of the input. The result after filtering, trace 3 in purple, is a sine wave that is a scaled version of the input.

Figure 3.31 shows the performance of the demodulator previously shown in the Matlab simulation of figures 3.8 and 3.9. The yellow trace is the output of the VCO within the PLL circuit. This waveform is phase-locked to the carrier waveform and ultimately mixed with it. The green trace is the mixer output which gives give an

absolute value waveform. The mixer output does go slightly below the zero into a negative value. This is a result of a slight phase difference between the PLL and the carrier signal as well as a small delay in the analog switch IC. This phase difference will ultimately reduce the DC component of the demodulated signal. This is not a problem for the Schmitt trigger however as the gain control block can adjust the gain and hence increase the DC component of the demodulated signal. This adjustment is built into the reference gain for the desired output of the microcontroller feedback code. This waveform is subsequently filtered to produce the analog waveform shown

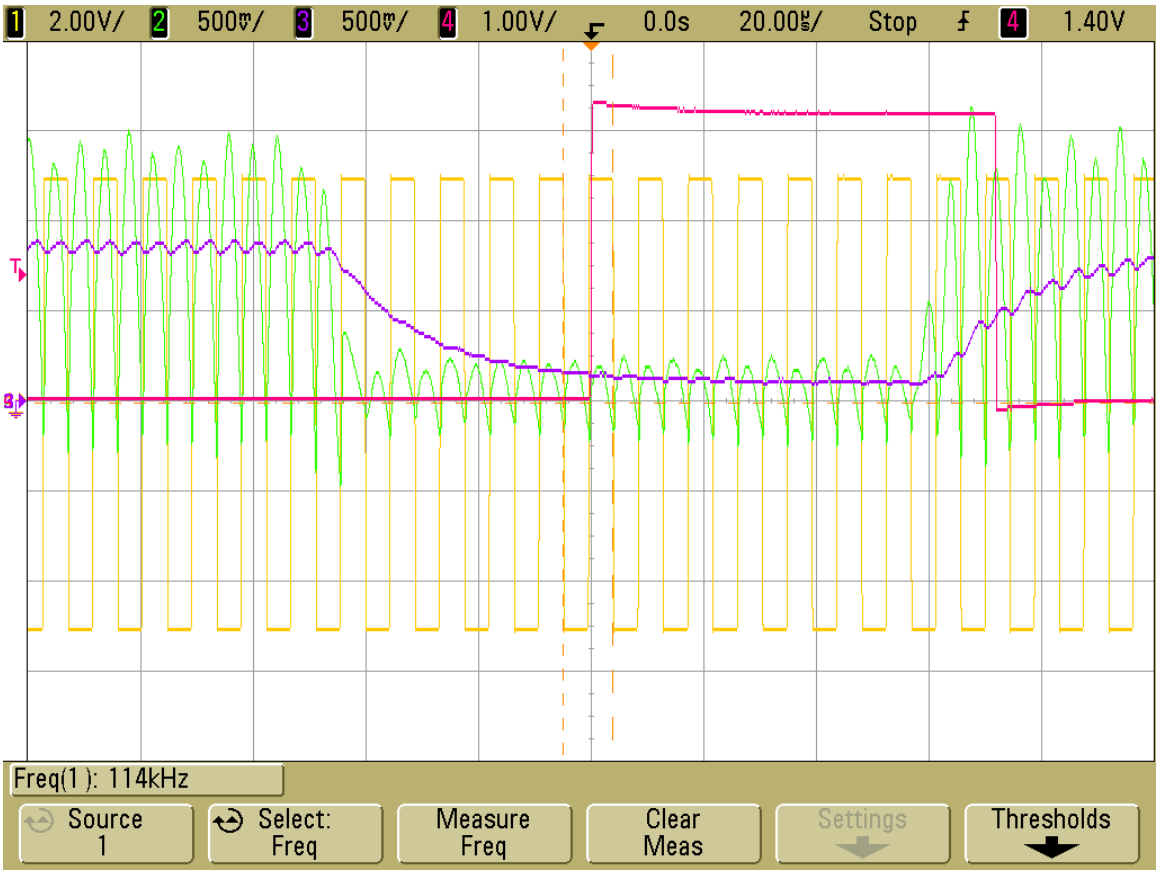

Figure 3.31: Implementation results of the receiver's demodulation block. The demodulation locks to the carrier signal by a PLL, trace 1 in yellow, and then multiplies the received PLC signal by the PLL effectively creating an absolute value, trace 2 in green. During the phase shift keying, the multiplication value drops significantly allowing the BSPK signal to be recovered after applying a low pass filter, trace 3 in purple. The recovered signal is then compared by means of a Schmitt trigger to create the TTL logic signal, trace 4 in red.

by the purple trace. This is the demodulation signal that then needs to be converted to a TTL logic signal using a deterministic selector, implemented with a Schmitt trigger. The red waveform is the final logic-level signal provided to the DSP. The final TTL logic signal is fully received by the microcontroller approximately 45 μs after the modulation is detected at the receiver.

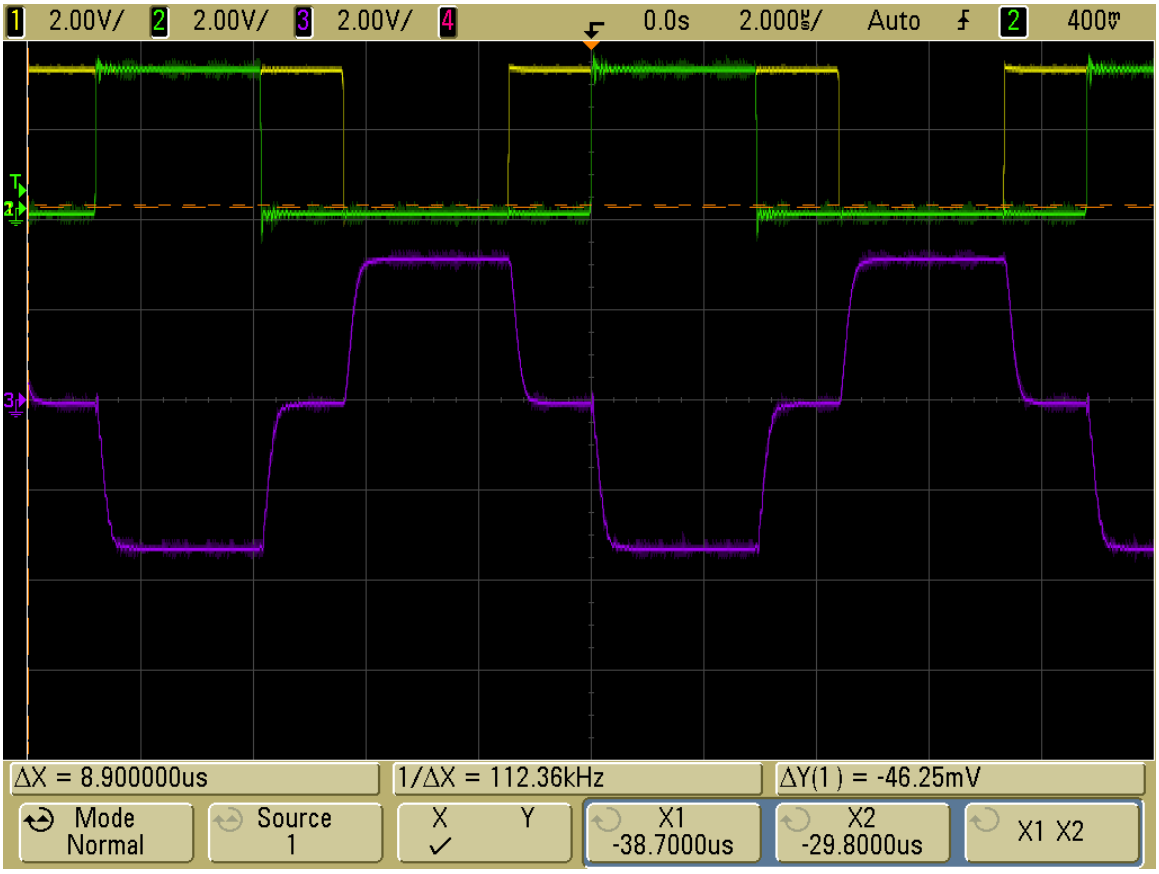

Figure 3.32: Implementation results for the communications carrier generation from the PWM channels of the DSP. The DSP generates two PWM signals at the carrier frequency with a duty cycle at 33% and 66% as captured by trace 1 in yellow and trace 2 in green. These PWM signals are summed together to get a multilevel PWM signal displayed as trace 3 in purple.

The transmitter carrier generation begins in figure 3.32. The PWMs coming out of the microcontroller are controlled properly such that the third harmonic multiples are canceled out. The resulting summation with a DC offset produces the waveform shown in purple. The real implementation does not utilize op-amps with a high

enough gain-bandwidth or slew rate and can be seen in the slant and rounding of the multilevel PWM output signal from the summing amplifier. This does not ultimately impact the carrier frequency, the fundamental of the multilevel PWM signal.

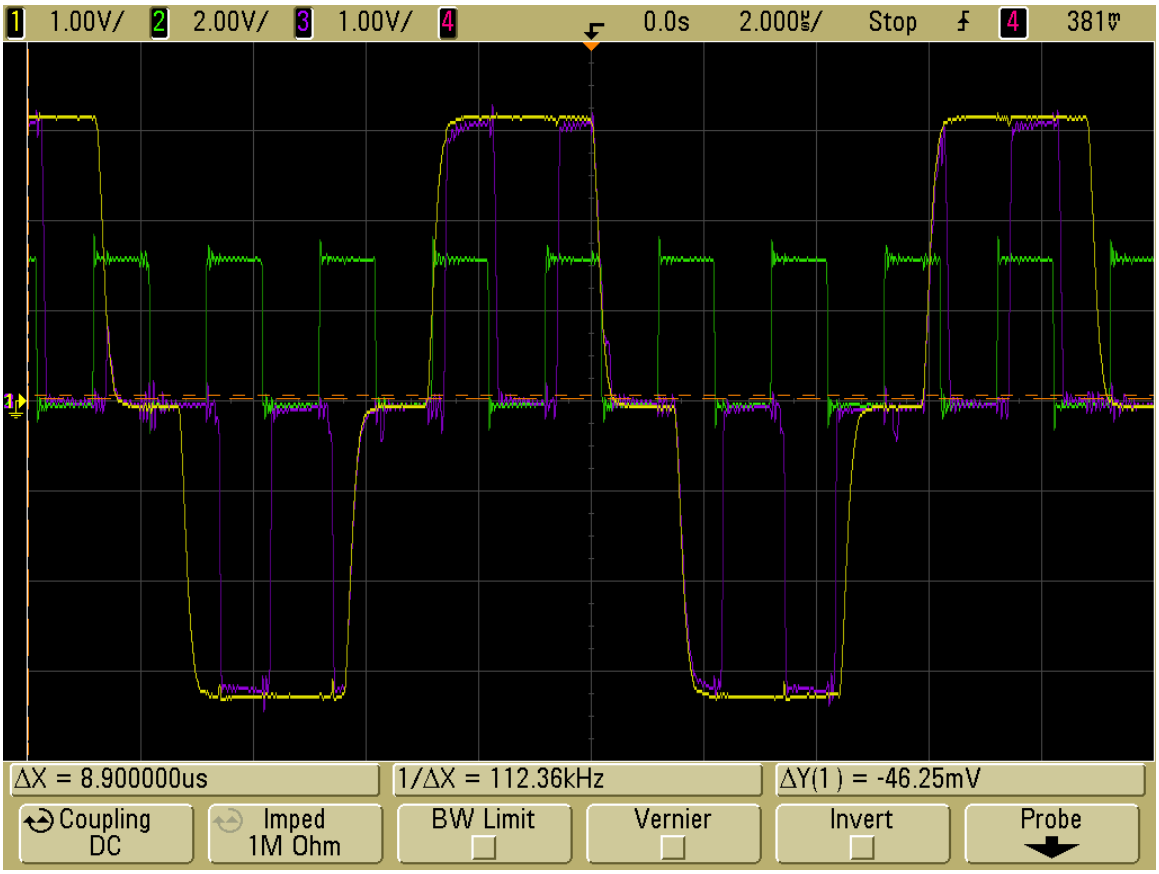

Figure 3.33: Implementation results for the transmission circuit gain control. The summed PWM signals, trace 1 in yellow, composing the carrier signal is passed through a PWM multiplier, trace 2 in green, resulting in a chopped carrier waveform, trace 3 in purple. This is effectively multiplying the fundamental signal by a duty cycle to attenuate the magnitude.

After the multilevel PWM signal is generated, it is passed to the gain reduction block implemented from an analog switch that will change between the signal and ground based on the duty cycle from the microcontroller. Featured in figure 3.33 is the circuit operation of this gain reduction on the multilevel PWM. The duty cycle is 50% and creates the chopped carrier signal that then needs to be filtered. The filtering is not shown here since it is a repeat of the receiver filtering block. The

rest of the modulation circuitry before the line driver is not shown in detail, but the modulation results will be shown shortly.

The line driver, a high power and frequency op-amp, is designed to drive high currents into the isolation transformer. As such, it is capable of becoming unstable without proper care in the design. The stability network from TI's reference design was slightly changed for allowing high current into the powerline. This required a test on the stability of the line driver and is performed with a step response, made from a square wave, as seen in figure 3.33. The line driver is stable with a $50\,mV$ overshoot for a $1\,V$ step response, a 5% overshoot.

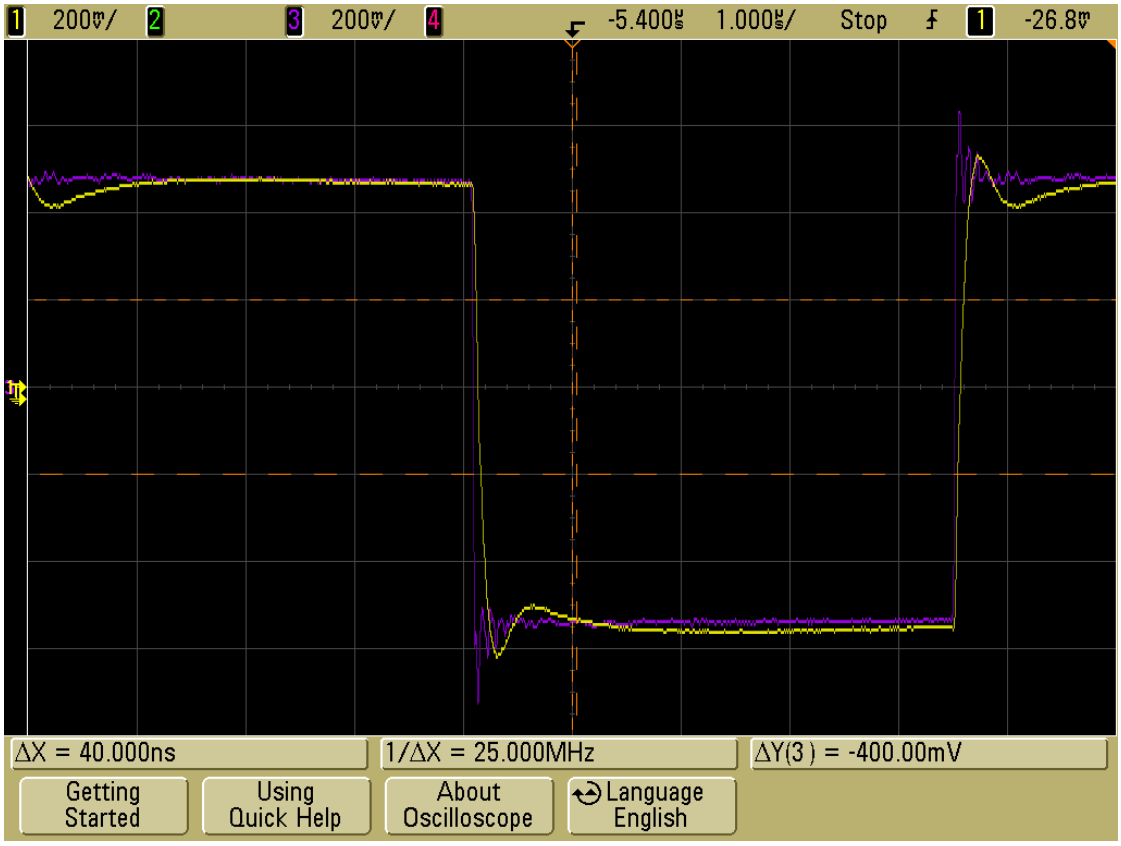

Figure 3.34: Step response of the line driver circuit with stability network. The input is a $1\,V_{pk\text{-}pk}$ square wave seen trace 3, purple. The output, trace 1 in yellow, shows a stable step response with an acceptable overshoot.

The modulation of the transmitter is shown in figure 3.35. The modulation signal from the microcontroller causes causes an immediate phase shift to occur and the

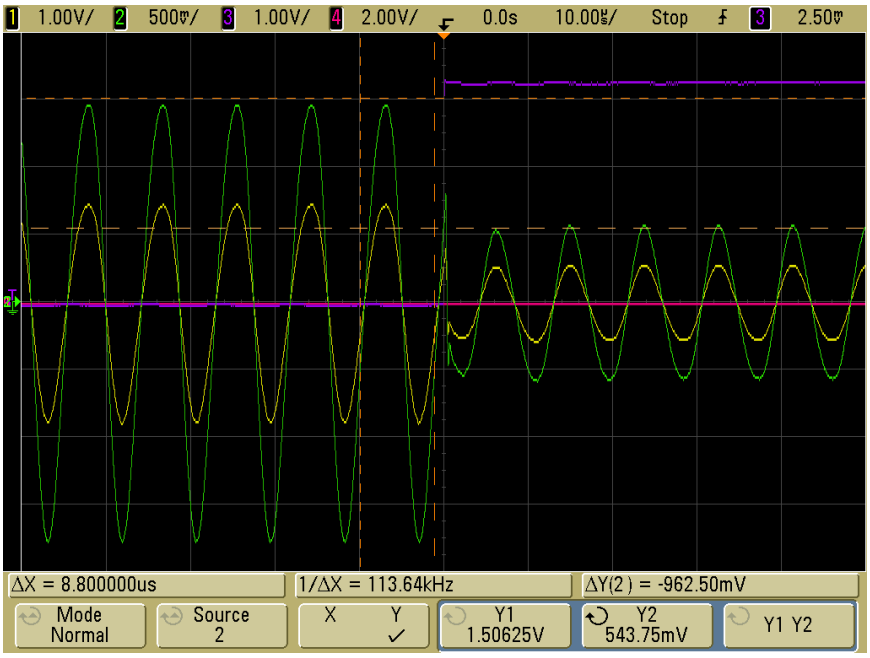

Figure 3.35: Modulation of the transmitter circuit showing the encoding of the carrier at the line driver. The modulation signal, trace 3 in purple, causes the carrier fundamental to be summated with the phase inversion of the of the carrier resulting in the modulation shown in the input, trace 1 in yellow, and output, trace 2 in green, of the line driver.

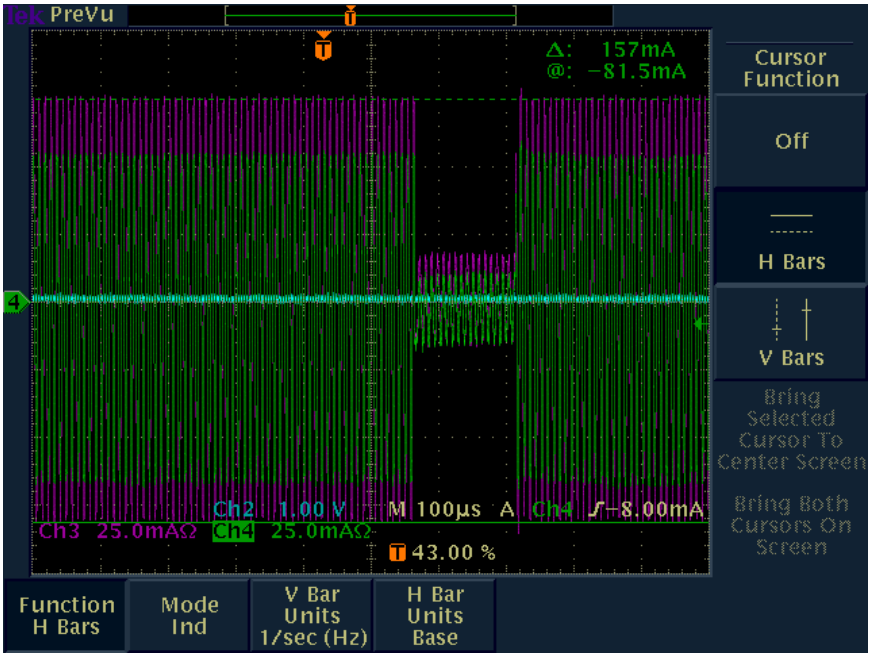

Figure 3.36: Current outputs from the line driver circuit, trace 4 in green, and the isolation transformer, trace 3 in purple, for the transmission circuit.

summated phase shift added to the carrier results modulation seen in the input and output of the line driver. The line driver shows no issues handling the modulation with the stability circuit. Figure 3.36 shows the current output during modulation. The line driver output current shows no sign of distortion either and a scaled current, due to the turns ratio of the isolation transformer, is seen at the output of the transformer and injected into the system.

CHAPTER 4: COMMUNICATIONS CHANNEL MODEL UTILIZING SERIES-CONNECTED POWER ELECTRONIC MODULES

The transmission and reception of information consists of taking a data stream, encoding the data for transmission, physically transmitting the encoded signal in the communications channel in which noise will corrupt the signal, and finally having a receiver decode the data stream and recover the encoded data. A communications model for this process is seen in figure 4.1 in which is a generic approach is defined for a single path transmission [67]. As the transmitter and receiver were previously described in chapter 3, this chapter examines the channel model formed when utilizing series-connected power electronic modules as the physical medium for communication signal [68].

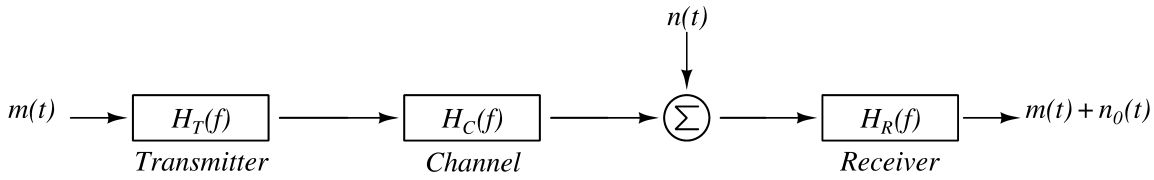

Figure 4.1: Generic communication channel model to be adapted for utilizing series connected power electronic modules.

4.1 Understanding the Physical System Propagation Effects

Traditional powerline communications utilize a multipath channel model due to the physical branching of the possible paths the communications signal can follow [69]. In the design of the current based communication methodology, it was defined that the current, $i_{Rx}(t)$, at each of the receivers to be the same transmitted current. This in turns defines that there will only be one communication path for the series connected power electronic modules. The communications channel model for the

current based power line communications system is therefore similar to that of the wire line communications model.

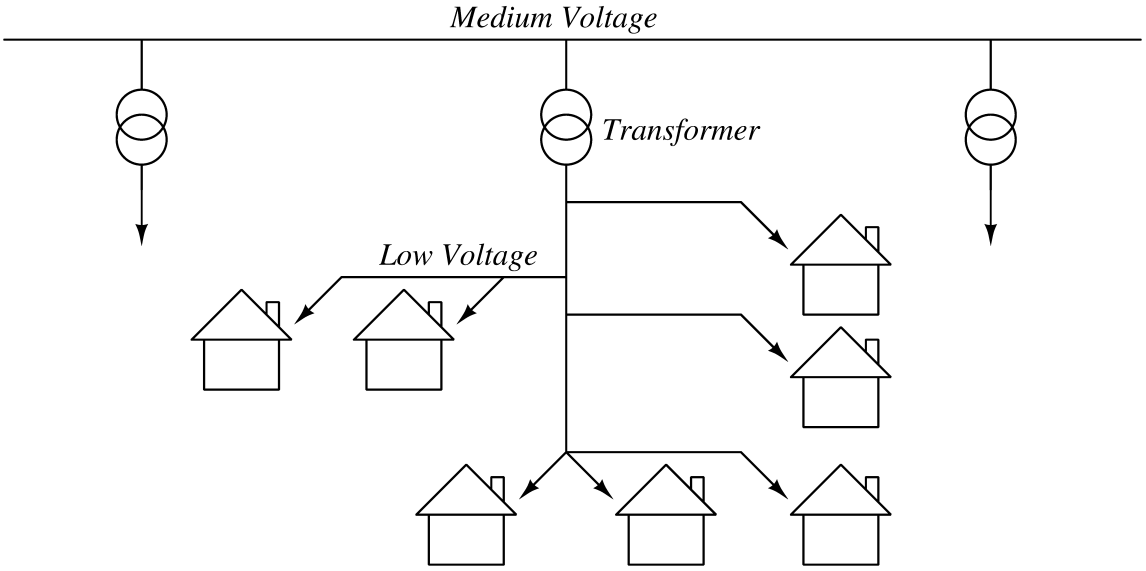

Figure 4.2: Traditional power line communications tend to have a transmission path that can branch to various locations across the distribution network requiring a multipath model for the communication system.

The wire line communications model is used in media such as traditional telephone lines that transmits a 10 kHz bandwidth signal down a pair of conductors that has a spectrum of 1 to 2 Mhz usable bandwidth over long distances, Ethernet cables that use twisted pair wires such as Cat6 with a 90 ft distance and a bandwidth of 250 Mhz, or a coaxial cable that is manufactured with a conducting wire surrounded by a conducting shield with an insulating material between such as RG6 which cable companies use and has an approximate bandwidth of 500 Mhz [70]. The current based powerline communications presented has similarities to the previous wireline media in that it is a point to point communication with low bandwidth requirements. It will be shown later in this chapter how the conductor acts like a low pass filter. The model is different though from the previously listed wireline communication mediums in that there is no twisted pair wiring in the power line neither is there any type of shielding around the conductor. The biggest change setting it apart from the

other communication mediums is the utilization of the power electronic modules as a communication medium instead of only the wiring.

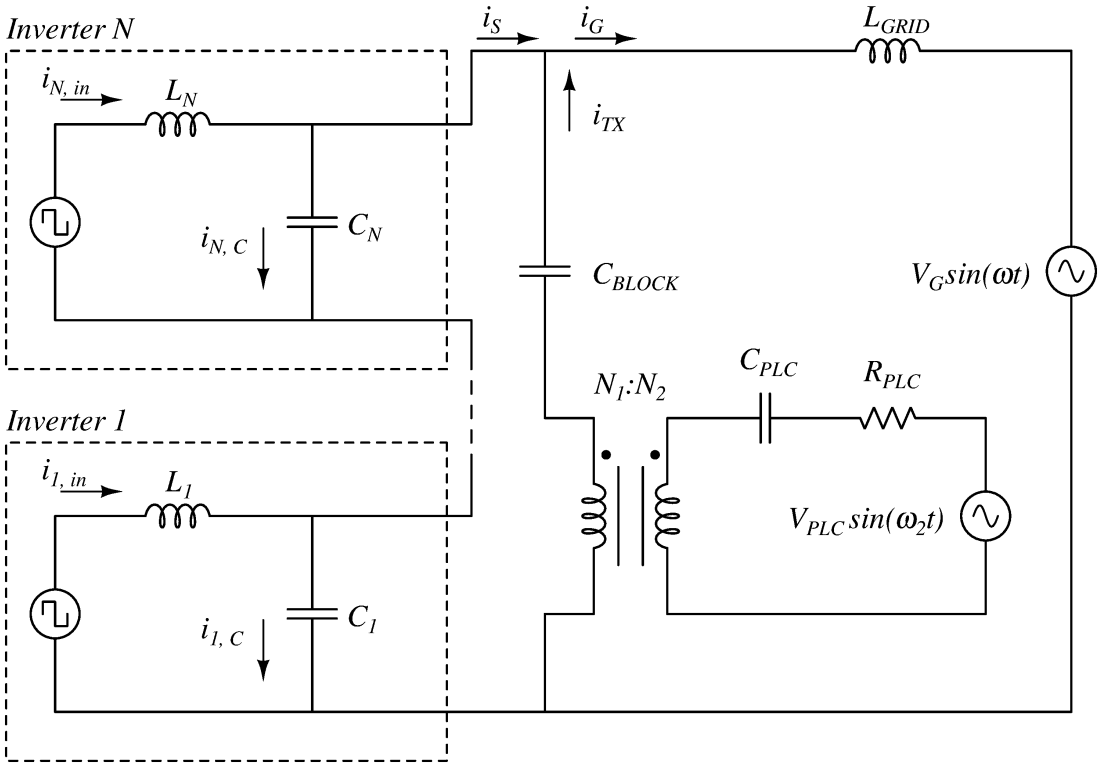

Figure 4.3: Conceptual circuit model for the AC-stacked inverter system showing the end devices connected in a string with the output filter of each inverter allowing a low impedance path for the PLC current.

The application of this current based powerline communication medium in this dissertation is series connected power converters used in solar conversion. In such a system, the wire between each solar panel is physically separated by the power converter that would be inside the junction box. The communications current flows into and out of the positive and negative terminals just like the low frequency power generation current as seen in figure 4.3 for the AC-stacked architecture. The difference between the two currents becomes apparent inside the power electronics as the high frequency communications current propagates though the electronics differently due to the impedance differences among the paths as the frequency increases. The power electronics modules in conjunction with the wiring will still yield a single path model.

Also displayed in figure 4.3 is the grid interface in which the transmitted communications current can flow. This path can be modeled as a parallel impedance to the string of power electronic modules and will not contain any receivers. All this will affect is the distribution of the current and with a properly designed grid interface, this value may be negligible. It will be shown how in the designed system it does not significantly affect the system and can be properly modeled as part of the communications system.

4.2 Modeling of the Switched Mode Power Converters

The primary communications medium inside series-connected power electronics is the impedance seen looking into the terminals of the power line connection, whether that be the input or output terminals. This impedance may consist of passive elements, such as inductors or capacitors used as filtering elements, or active elements such as diodes, field effect transistors, and other such components. Each individual power electronics system will likely be different, but should not be a reason for concern for the communications viewpoint so long as the signal can propagate through electronics in the specified frequency bands.

The secondary medium inside such a system is the wiring between the power electronics. Depending on the specifications of the wiring, hence the wire type, gauge, and length, this impedance can interact with the power electronics impedance and can therefore hamper or facilitate a desired low impedance at in the frequency channels. The modeling of both of these aspects will be examined in this section.

Power electronics generally consist of some type of passive filtering followed by active devices used in the power conversion process. This occurs at both the input and output terminals of the module. What is of interest is how the impedance looks at the terminals of the series-connection and how it may change over time. In the case of the output of a converter, there is typically a LC filter to ensure the switching ripple in both the voltage and current is attenuated to acceptable levels. In the case

of the input of a converter, there is generally a capacitor or an LC filter. Ideally, there should be a capacitor placed immediately across the input terminals to ensure a low impedance for the PLC signal.

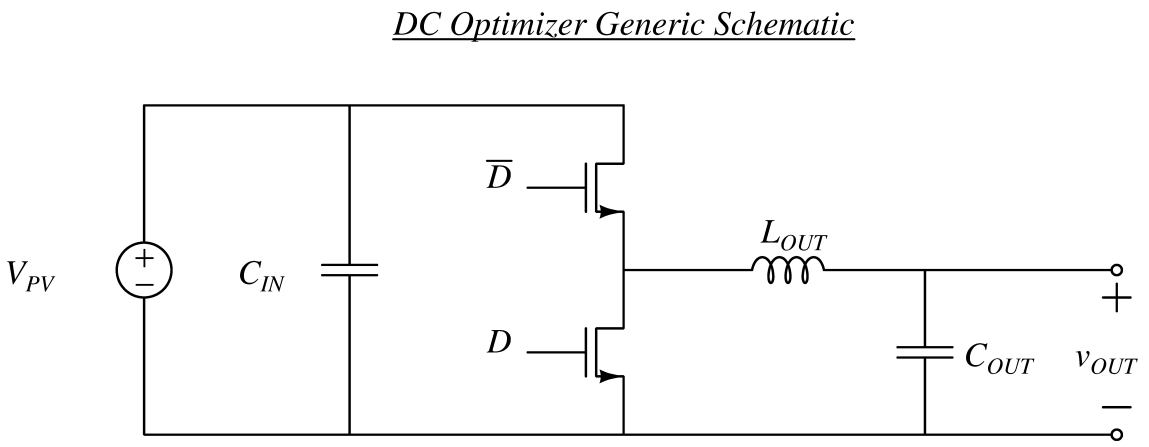

Figure 4.4: Generalized schematic for a DC-Optimizer. The output of the converter is series-connected and allows the PLC current to pass through the output filter as its medium.

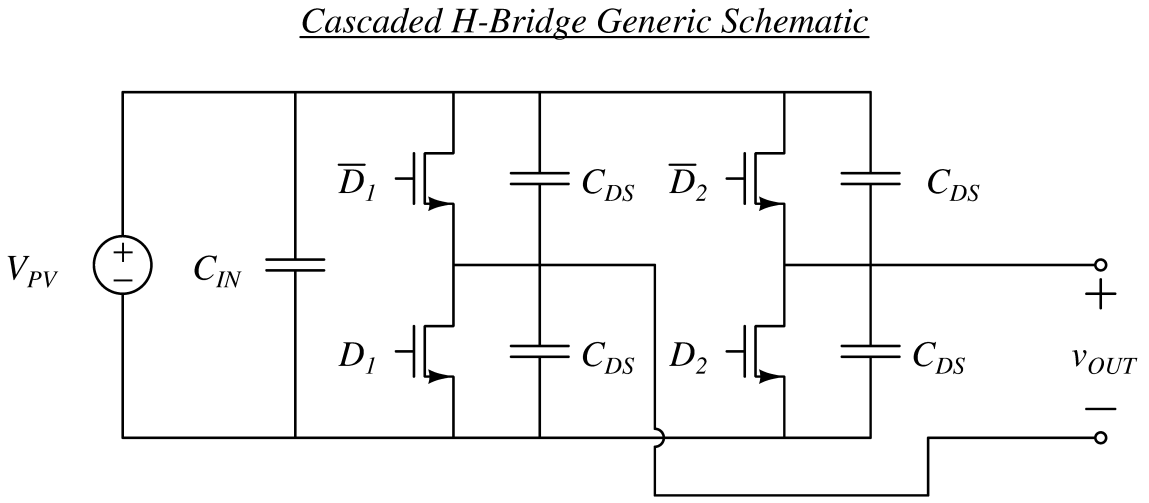

Figure 4.5: Generalized schematic for a cascaded H-bridge. The output does not contain a filter to direct the PLC current when series-connected and instead sees the impedance of the switches.

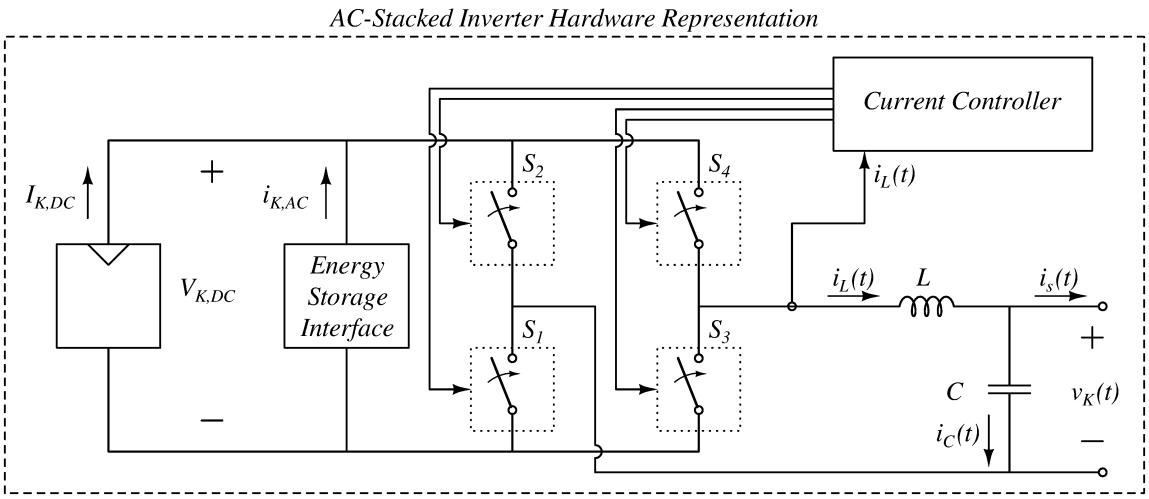

Figure 4.6: Generalized schematic for the AC-stacked inverter hardware. Like the DC-Optimizer, the inverter contains the LC filter at the output which makes the impedance modeling the same.

Generalized schematics of power electronics commonly seen in series connected configurations are found in figure 4.4 through figure 4.6. Two of the architectures that are used in series-connected power electronics, the DC-Optimizer and the AC-Stacked inverter have a similar output impedance equation as seen below in equation 4.1.

$$Z_{Output} = Z_{C,OUT} || \left(Z_{L,OUT} + Z_{Switches}\right) \tag{4.1}$$

The impedance of the switches though will change between them and will generally have little impact in that the impedance of the output is generally much greater in comparison at the communications frequency, as well as the impedance of the wiring seen later. The dominating component for a low output impedance is generally the capacitance. The switch impedance for the DC Optimizer is still defined below in equations 4.2 through 4.5. The switch state for DC Optimizer is defined as state 0 having the bottom FET on and state 1 having the top FET on for the buck configuration.

$$Z_{OFF} = R_{DS,OFF} || Z_{C,DS} \tag{4.2}$$

$$Z_{ON} = R_{DS,ON} || Z_{C,DS} \tag{4.3}$$

$$Z_{DC} = Z_{C,DC} || Z_{PowerSource} \tag{4.4}$$

$$Z_{Switches,Buck} = \begin{cases} Z_{ON} || \left(Z_{OFF} + Z_{DC}\right) & S_0 \\ Z_{OFF} || \left(Z_{ON} + Z_{DC}\right) & S_1 \end{cases} \tag{4.5}$$

The cascaded H-bridge will have the same expression for the switch impedance as the AC-stacked architecture due to the shared H-Bridge switching stage, but will differ in regard to the impedance seen at the output of the terminals as there is no LC filter. Instead, the output impedance is dominated by the impedance of the converters switches. In an H-bridge in which all the switches are the same, and neglecting all configurations that would cause a short on the DC bus or switch transitions, there are four cases the switches can be configured with at least two switches active at all times. These states are defined as state 0: both bottom switches on, state 1 and 2: one bottom switch on and one top switch on in the opposite leg, and state 3: both top switches on. Defined are impedances in equations 4.2-4.8 for components and derivation values, with a final switch state impedance in equation 4.9, with two values based on switch states of the converter. It should be noted that the derivation assumes that each pair of FETs in a leg are identical, but each leg may be optimized for switching speed and hence have a different FET pairing. This is typical in a H-Bridge that is configured for unipolar switching. The notation used to distinguish between the FETs optimized for slow switching will be a subscript 1 and the FETs optimized for fast switching will be marked with a subscript 2.

$$Z_{A,Unipolar} = \frac{Z_{ON,1} Z_{OFF,1}}{Z_{ON,1} + Z_{OFF,1} + Z_{DC}} \tag{4.6}$$

$$Z_{B,Unipolar} = \frac{Z_{OFF,1} Z_{DC}}{Z_{ON,1} + Z_{OFF,1} + Z_{DC}} \tag{4.7}$$

$$Z_{C,Unipolar} = \frac{Z_{ON,1} Z_{DC}}{Z_{ON,1} + Z_{OFF,1} + Z_{DC}} \tag{4.8}$$

$$Z_{Switches,Unipolar} = \begin{cases} Z_A + (Z_C + Z_{ON,2}) \,||\, (Z_B + Z_{OFF,2}) & S_0, S_3 \\ Z_A + (Z_C + Z_{OFF,2}) \,||\, (Z_B + Z_{ON,2}) & S_1, S_2 \end{cases} \tag{4.9}$$

If the H-Bridge is configured for bipolar switching where all four FETs are optimized for a single switching frequency and are all the same, the equation 4.9 would then be transformed into equation 4.13 as seen below.

$$Z_{A,Bipolar} = \frac{Z_{ON} Z_{OFF}}{Z_{ON} + Z_{OFF} + Z_{DC}} \tag{4.10}$$

$$Z_{B,Bipolar} = \frac{Z_{OFF} Z_{DC}}{Z_{ON} + Z_{OFF} + Z_{DC}} \tag{4.11}$$

$$Z_{C,Bipolar} = \frac{Z_{ON} Z_{DC}}{Z_{ON} + Z_{OFF} + Z_{DC}} \tag{4.12}$$

$$Z_{Switches,Bipolar} = \begin{cases} 2\,(Z_{ON} || Z_{OFF}) & S_0, S_3 \\ Z_A + (Z_C + Z_{OFF}) \,||\, (Z_B + Z_{ON}) & S_1, S_2 \end{cases} \tag{4.13}$$

Interesting observation with this type of varying impedance is now the additional communication requirements and optimizations that now must be considered in the design of power electronics that will be utilized as the communication medium. Another thing to note, the communications frequency here is not specified as being above or below the switching frequency. In modules such as the cascaded H-Bridge, the switching frequency would be much lower than the communications frequency so the transmitted carrier would be in the switch state for multiple encodes before the switch state changing. In hardware such as the AC-Stacked inverters, the switching frequency may be much higher than the communications frequency in which case, the switch states may change much more often during the encoding time. This type of hardware introduces a much more complicated time varying impedance model for the

communication system that much be considered and designed for. It will be shown that such a system can still be utilized as a communications medium so long as the encoding, transmission, reception, and demodulation scheme is immune to such a varying impedance.

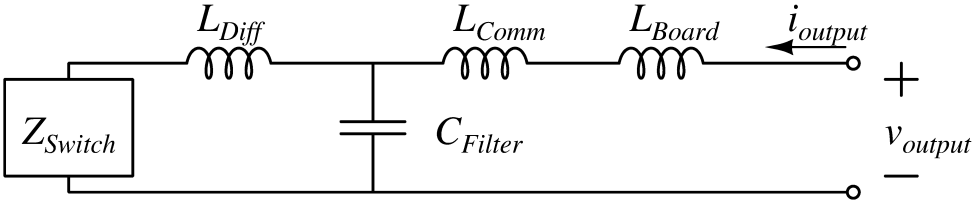

Figure 4.7: Circuit model for the inverter module output filter to determine the impedance of the converter with respect to the communications current.

The theoretical impedances of a converter typically have small errors from the actual measured impedance due to tolerances and parasitics. With the utilization of the AC-Stacked inverter hardware, the actual impedance was modeled and measured for comparison to the theoretical impedance. The inverter output filter impedance model is shown in figure 4.7 and contains a parasitic board inductance, L_{Board} from the traces of the printed circuit board (PCB) as well as an extra inductance,L_{Comm} due to mismatched winding in the common mode inductor. The extra terms yield an equation as seen in 4.14. The output impedance of the AC-Stacked inverters is a function of the inverter's design and should be optimized not only to reduce the switching noise of the converter, but to allow a low impedance path for the power line communications.

$$Z_{Output} = Z_{Board} + Z_{Comm} + Z_{Filter}||(Z_{Diff} + Z_{Switches}) \tag{4.14}$$

In the analysis of this dissertation, the board was already designed and as such, was not optimized for the communications. The output impedance of the converter as analyzed showed that it would have some slight dependency based on the switching and hence the magnitude of the output voltage of the inverter. Such a dependence led

to the measurement of the impedance in three different methods. The first method was the switching as measured at the zero crossing of the electrical cycle with a $\pm 500\mu s$ window. The measured impedance of the converter at this location in the electrical cycle was $Z_{Output} = 0.02241 - 0.11580j$. The window is then moved for the second measurement to the peak of the electrical cycle which, for a $60Hz$ grid, occurs $4.167ms$ after the zero crossing. Here the measured impedance changed to $Z_{Output} = 0.02102 - 0.14364j$. The last measurement of impedance is taken as the averaged impedance across the entire electrical cycle. The total output impedance of the inverter measured across an entire electrical cycle is $Z_{Output} = 0.02975 - 0.10346j$. All measurements are primarily capacitive in nature showing the dominance of the LC filter.

4.3 Modeling of the Powerline Impedance

In narrow band PLC communication where distance can be significant, the traditional method of modeling is to examine the medium as a transmission line [53]. In the case of series connected power electronics, the argument is made that the length of the wire is significantly shorter than the wavelength of the transmission frequency as seen in equation 4.15 [71].

$$\lambda = \frac{c}{f} = \frac{3e8}{120e3} = 2500m = 8202.1ft \tag{4.15}$$

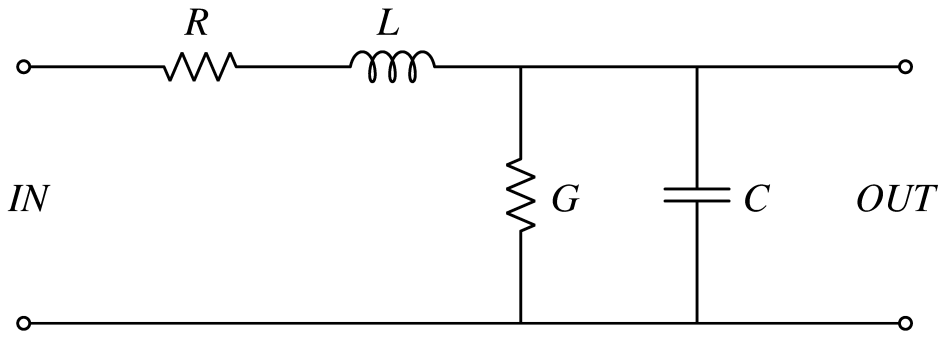

Figure 4.8: Lumped transmission line model for the wiring impedance.

With this assumption, the transmission line can be modeled as a lumped circuit model such as that in figure 4.8 and then analyzed applying Kirchoff's laws. The resistance of the wire in the system can be generalized as impedance of the gauge of the wire for use in narrowband communications assuming the wire is stranded. It is generally the length of the wire and hence the inductance that tends to dominate in the communications frequencies of interest and such the conductance and capacitance between the terminals are neglected [72]. As the inductance dominates, it is not a bad assumption to only use in the impedance estimation. The maximum inductance of a straight wire in free space is found as

$$L_{Wire} = 2l\left[ln\left(\left(\frac{2l}{d}\right)\left(1+\sqrt{1+\left(\frac{d}{2l}\right)^2}\right)\right) - \sqrt{1+\left(\frac{d}{2l}\right)^2} + \frac{\mu}{4} + \frac{d}{2l}\right] \quad (4.16)$$

where l is the length of the wire in centimeters, d is the diameter of the wire in centimeters, μ is the relative permeability of the surrounding material, and L is the inductance in nH [73]. The predicted maximum of the wiring is not necessarily obtained due to physical constraints with bends and such, but is taken as the absolute maximum that should appear. A lower impedance is preferred anyways such that a lower transmit power may occur for the current. This difference is important to note when predicting scalability in series-connected power electronic systems.

4.4 Modeling of the Grid Impedance

For series connected power electronics, it is possible that there may be a parallel connection in the application. For that of solar converters, it is the grid interface by which the power generated by the converters flows through. Examined in this section is the grid interface seen in figure 4.9. In this setup, the parallel impedance of the grid connection is primarily dominated by the impedance inherit to the grid interface

itself and described as equation 4.17.

$$Z_{Grid} = Z_{FET} + Z_L + Z_{Relay} + Z_C \tag{4.17}$$

The effective impedance, Z_C, at the X and Y capacitors may change depending on the loading conditions of the grid. Examined here is the open circuit and short circuit conditions between line to neutral connections to examine the two extreme cases that may occur at the grid interface box. As such Z_C will reach a maximum and minimum condition. The impedance of Z_C adds to that of the grid interface inductance thereby reducing the overall impedance magnitude.

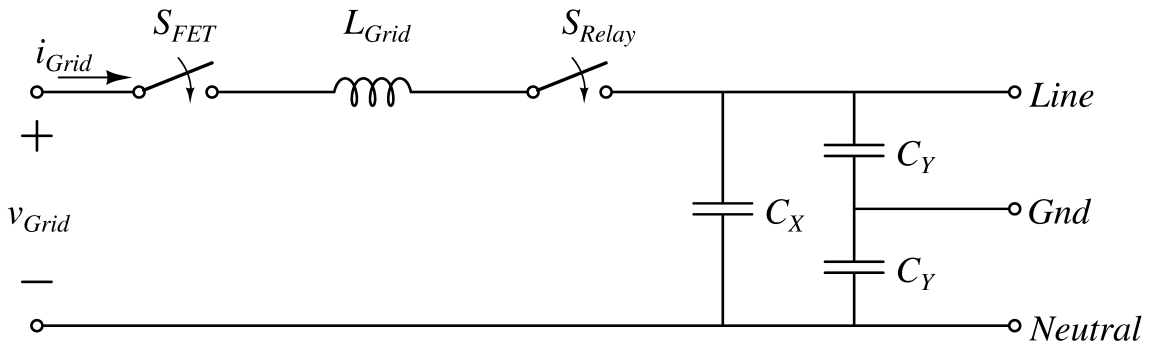

Figure 4.9: Circuit model for the grid interface hardware.

4.5 Communications Channel Model

All of the components of the channel has now been defined and can be applied to form the complete channel model. Shown again in figure 4.10 is the channel model but with the appropriate signals labeled in regards to the communication transmission and channel model. The channel is defined as starting at the output of the line driver IC. The reason for defining this as the beginning of the channel is because the signal at this point is buffered with all circuitry before it comprising the transmitter where the carrier is composed, gain control occurs, and modulation is controlled. Anything after the line driver is influenced by the impedance of the series connected power electronic modules and would change $i_S(t)$.

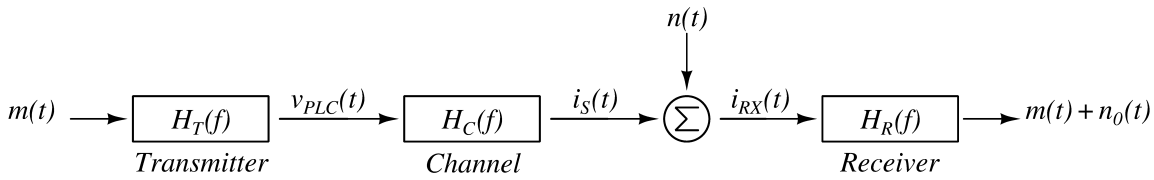

Figure 4.10: Communication channel model for utilizing the series connected power electronic modules.

The general hardware model for the transmission at the beginning of the series-connected power electronics is shown in figure 4.11. This hardware consists of a high current line driver amplifier, a transformation impedance for converting from a voltage mode to current mode communication, a stability network, isolation transformer for protecting the transmission hardware, and a high voltage blocking capacitor to keep the any DC or 60 Hz voltage from causing large currents to occur in the isolation transformer.

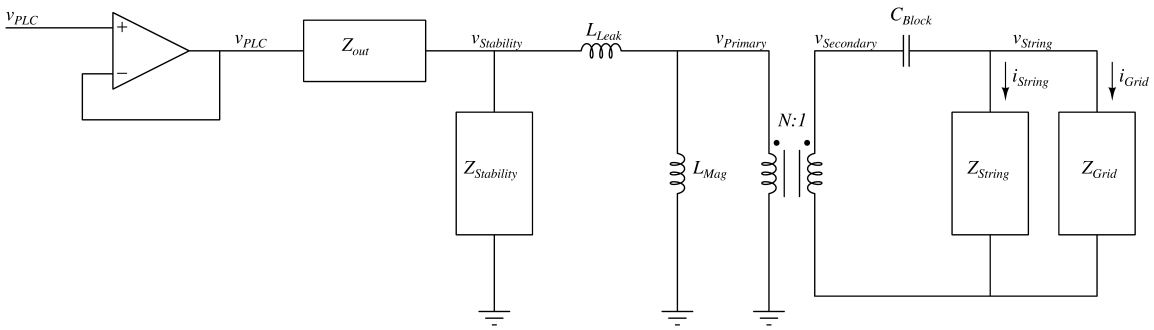

Figure 4.11: Circuit model for the transmission hardware used to develop the transfer function of the line driver voltage output to the string current.

The current transmitted from the beginning of the line driver throughout all the series-connected power electronics can be predicted by the transfer function of equation 4.18.

$$\frac{i_{String}}{v_{PLC}} = \left(\frac{i_{String}}{v_{String}}\right)\left(\frac{v_{String}}{v_{Secondary}}\right)\left(\frac{v_{Secondary}}{v_{Primary}}\right)\left(\frac{v_{Primary}}{v_{Stability}}\right)\left(\frac{v_{Stability}}{v_{PLC}}\right) \qquad (4.18)$$

Substituting in the quantities for each of the ratios in equation 4.18 from the respected

values of figure 4.11 the full equation is then given in equation 4.18 below with $Z_{eq,1}$ being the magnetizing impedance parallel to the reflected impedance of the transformers secondary load and $Z_{eq,2}$ being the stability impedance parallel to the leakage inductance and $Z_{eq,1}$ combined. Knowing the voltage output of the line driver chip, it is then possible to predict the string current for a design. All values given in the design should not change for the scaling of 2 to 32 inverter modules in the AC-stacked inverter system except for the string impedance.

$$\frac{i_{String}}{v_{PLC}} = \left(\frac{1}{Z_{String}}\right)\left(\frac{Z_{String}||Z_{Grid}}{Z_{String}||Z_{Grid}+Z_{Block}}\right)\left(\frac{1}{N}\right) \left(\frac{Z_{eq,1}}{Z_{eq,1}+Z_{Leak}}\right)\left(\frac{Z_{eq,2}}{Z_{eq,2}+Z_{Out}}\right) \tag{4.19}$$

The string impedance is a function of the output filter of each inverter module and the impedance of the wiring between the inverter modules as seen in equation 4.20 where N is the number of inverter modules in the string, and not the isolation transformer's turns ratio.

$$Z_{String} = NZ_{Output} + Z_{Wire} \tag{4.20}$$

The equivalent impedances listed in the transfer function of equation 4.19 are there for simplifying the expression. The first equivalent impedance, $Z_{eq,1}$ shown in equation 4.21, is the combination of the reflected impedance of the isolation transformer, equation 4.22, and the magnetizing inductance. The second equivalent impedance is the parallel combination of the stability network and the impedance at the primary of the isolation transformer as expressed in equation 4.23.

$$Z_{eq,1} = Z_{MAG}||Z_{REFLECTED} \tag{4.21}$$

$$Z_{REFLECTED} = N^2\left(Z_{String}||Z_{Grid}+Z_{Block}\right) \tag{4.22}$$

$$Z_{eq,2} = Z_{STBL} || \left(Z_{LEAK} + Z_{eq,1} \right) \tag{4.23}$$

4.6 Empirical Results of Communications Channel Model

Modeling the communications channel is only complimented by validation of the model. Here, each of the models are measured and compared to the theoretical and the final channel model evaluated at the end. The inverter's output impedance has already been measured and compared with the model. The total output impedance of the yielded by the inverter is $Z_{Output} = 0.02975 - 0.10346j$, primarily capacitive in nature.

The wiring impedance is a function of the resistance and inductance of the wire. In the lab setup, a 16 AWG stranded copper wire is used to carry the necessary current during operation. Such wire has minimal resistance compared to the inductance. As the inductance dominates, only it is used in the impedance estimation. The predicted maximum inductance, calculated using the straight wire inductance of equation 4.16, of the 16 AWG wiring used with 3 sections of wire totaling 154.3 cm is $2.38\,\mu H$. The predicted maximum of the wiring is not necessarily obtained due to physical constraints with bends and such, but is taken as the absolute maximum that should appear. The actual measured inductance at the communications frequency is $1.506\,\mu H$, or 62.3% less. This is important to note when predicting upwards to utility scale systems.

The string impedance consists of an accurate value from the output impedance and an estimated output from the wiring impedance. Without having accurate prediction of the wiring impedance, the best way to predict the current when designing for a minimum communications current is to assume the maximum wiring impedance. A lower impedance will then only increase the current transmitted. The final string impedance in the two inverter module setup, taken from the measured wire impedance before wiring the inverters and the output filters of the inverters, comes to be estimated as

$Z_{Estimated} = 0.0595 + 0.8680j$. The actual measured impedance measured from the transmission of the communication signal comes to be $Z_{String} = 0.0499 + 0.8280j$. It is believed the resistance part of the measurement may be improved by more accurate measurements and the inductive part of the measurement changes slightly when configuring the wiring.

The grid impedance, seen in figure 4.9, is primarily dominated by the impedance inherit to the grid interface and, as stated before, the impedance at the capacitance may change depending on the loading conditions of the grid. At the communications frequency, the grid interface inductor dominates the impedance. Therefore, the capacitance will reduce the overall impedance of the grid interface. Of the two extremes, the grid connection being shorted or opened, it is when the grid interface is shorted that the largest communications impedance occurs as the capacitance impedance will no longer be reducing the inductive impedance. The predicted impedance when the relays are closed and with a short from the line to neutral connection is $40.5\angle 90°$ with the measured impedance being $41.6\angle 90.64°$.

With the full grid and string impedance, the full transfer function of equation 4.19 yields a predicted to signal strength of $1.280A_{pk\text{-}pk}$ for a line driver output of $6.645V_{pk\text{-}pk}$. The actual measured value of the communications current through the string was $1.226A_{pk\text{-}pk}$. Such a result shows accurate prediction of the transmitted signal for a known output and ability to predict with known values of the string impedance. The accurate prediction shows the communications channel model is valid.

CHAPTER 5: CHARACTERIZATION OF NOISE IN THE COMMUNICATIONS CHANNEL MODEL AND EFFECT ON RELIABILITY

Communication systems must inherently operate in a real environment with which there is noise. For traditional voltage-mode powerline communications, there are some publications that go into great depth of the noise which impairs the communication signal [53]. The first is the reflected signal noise due to multi-path effects from other devices in the parallel connection. This type of noise should not be present in the series channel model as there is only a single path being utilized for the current to the receivers [53]. The second type of noise is described is periodic noise, or noise that occurs at regular time intervals [53]. This affects communication for only a fraction of time. The third type of noise described as cyclostationary noise, noise that occurs on a regular interval or pattern relative to the electrical cycle [53]. Cyclostationary noise is a subset of periodic noise but is examined differently as the period is defined relative to the electrical cycle where periodic noise may be of a different frequency from the line frequency. A fourth type of noise is described as impulsive noise, or noise that occurs across the entire frequency domain at one point in time. Finally there is the additive white Gaussian noise (AWGN) that occurs. The AWGN is a noise that is equally distributed to all frequency spectrums and represents what is reffered to as the noise floor [74]. These noises are all voltages detected by the receiver.

In the case for using the power-electronics as the communication medium for current-mode powerline communications, the noise is found in the current which consists of the switching noise (i_{SW}) that is generated on top of the standard AWGN (i_{AWGN}) as well as the input or output current of the power electronics (i_{Power}). This noise sets requirements on the transmission current (i_{TX}) power and the usable fre-

quencies that can be utilized when transmitting through the series-connected power electronics. These components of the total current (i_{Series}) are all detected by the receiver which means that any extra component from the transmitted current can therefore be considered as noise sources.

$$i_{Series} = i_{TX} + i_{Power} + i_{AWGN} + i_{SW} \tag{5.1}$$

WIth the application of the communications scheme for the AC-stacked inverter architecture, the literature was searched for several types of current noise found in PV inverters. The first noise reported consists of line frequency harmonics and their cancellation with controllers and filters [75]. The literature on this type of noise is very low frequency and compared to the communications frequency and is handled well by the filtering in the receiver's design. Therefore, this noise is not looked at. The second type of noise regulary reported in string inverters is that of common mode noise that flows through the converter due to a ground loop existing [76, 77]. Of particular interest is the string inverters that utilize a unipolar switching strategy where the common mode noise is particularly worse than bipolar switching [78, 79]. This is interesting as the implementation of the AC-stacked inverter architecture being utilized for the communications development does use unipolar switching. Although there is not as much literature in comparison, the ground loop noise of cascaded H-bridges is interesting as there are multiple ground loops that exist where the ground current will split between the converts and return to ground at different places and is referred to as multi-nodal common-mode noise [80, 81]. Analysis of the noise between string inverters and cascaded H-bridges differ based on the parasitic ground capacitance with the MLPE's having only a small PV panel capacitance which authors are working on modeling [82].

5.1 Noise Characterization in the AC-Stacked Inverter Architecture

The noise in the AC-stacked inverter architecture can now be characterized in terms of the already identified noises. The receiver detects all the currents shown in equation 5.1. It has already been shown what the transmitted communications current and the power looks like, so for this chapter, the noise components will be examined. Figure 5.1 shows an example time domain noise from a series-connected power electronics system. Measured are the total current of the converter leaving on one wire and the common-mode current as measured with both output wires inside the current probe while the system is configured to operate without generating power into the grid. As the receiver will include some of the common-mode noise through the single wire, it is examined as well. Visual inspection of the current waveforms yields a few interesting observations. The first is that the there is a general shape to the noise is periodic over the electrical cycle. The second is the noise spike at the zero crossing of the electrical cycle where the slow FETs change in the unipolar switching strategy of the inverter hardware. Also observed with the visual inspection of the

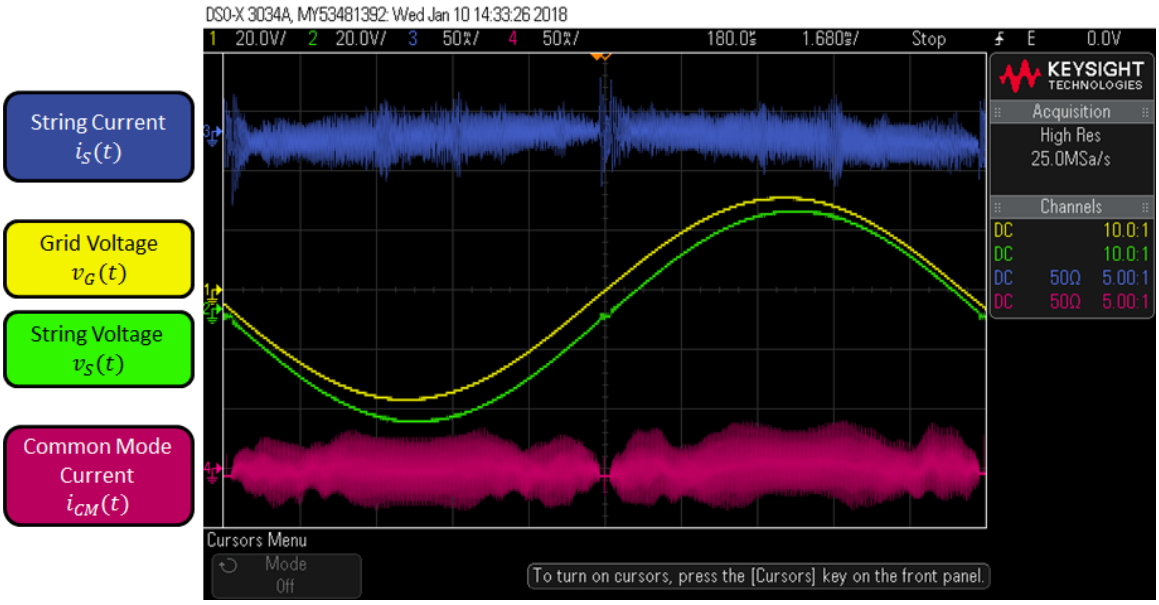

Figure 5.1: Currents under open-circuit switching in a two-inverter string: total current leaving one inverter (blue) and common-mode current (pink).

current noise, is the similar shapes seen in literatue of the common-mode noise of PV inverter systems [78–82]. This similarity in the noise pattern is encouraging as the system will be behaving as expected and allows for direct relations.

Modeling in cascaded H-bridges have shown a model for multi-nodal common-mode noise [80, 81] and with comparison to this model, an adaptation can be made for the AC-stacked inverter architecture. This simple model is portrayed in figure 5.2 where the inner and outer ground current loops are identified. The ground loop current originates at one ground point, flows through a parasitic capacitance which would be the frame capacitance in PV panels [82], through the electronics which is modeled as the sources, and at the output of the inverter module, may split two different directions to return to a ground back through another inverter module or the grid interface. The current having multiple paths to return to ground is why the noise is

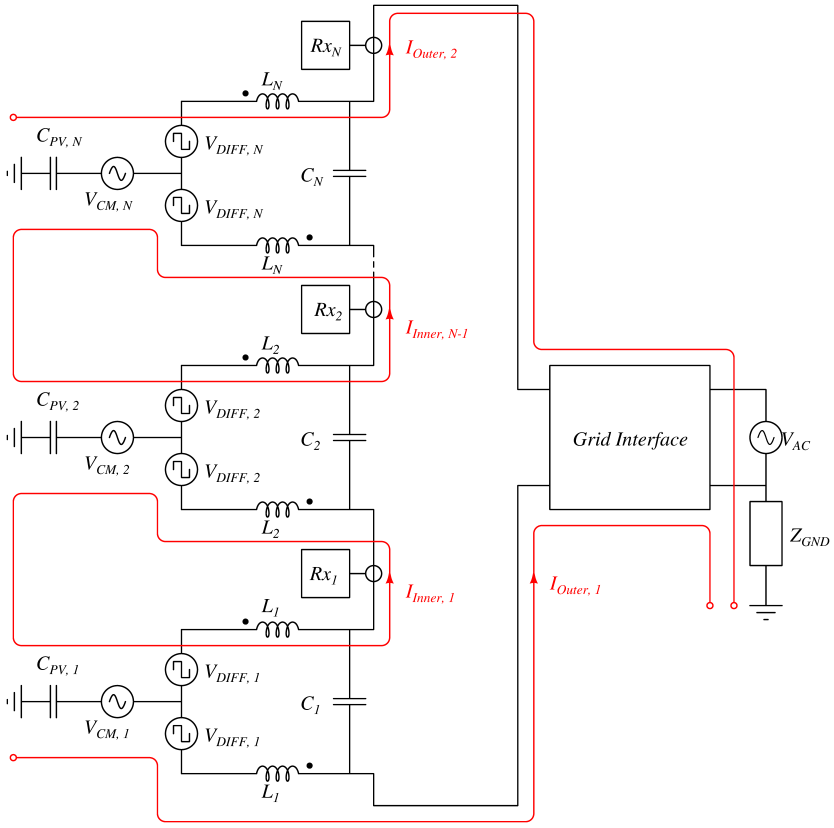

Figure 5.2: Ground current leakage paths exist in the AC-stacked architecture causing additional noise in the receiver.

referred to as multi-nodal common-mode noise. The distribution of current along the multiple paths is believed to be affected by the duty cycle alignment of the power electronics in the series connection. Figure 5.3 shows an example of the duty cycle alignment between two adjacent converters becoming offset over time and the effect in a real system is seen in figure 5.4 where the current distribution changes when synchronization causes realignment. It is seen in figure 5.5 that across one full electrical cycle that current distribution does not change, only the magnitude of noise is cyclostationary. The primary frequency of this noise is the switching frequency of the power electronics.

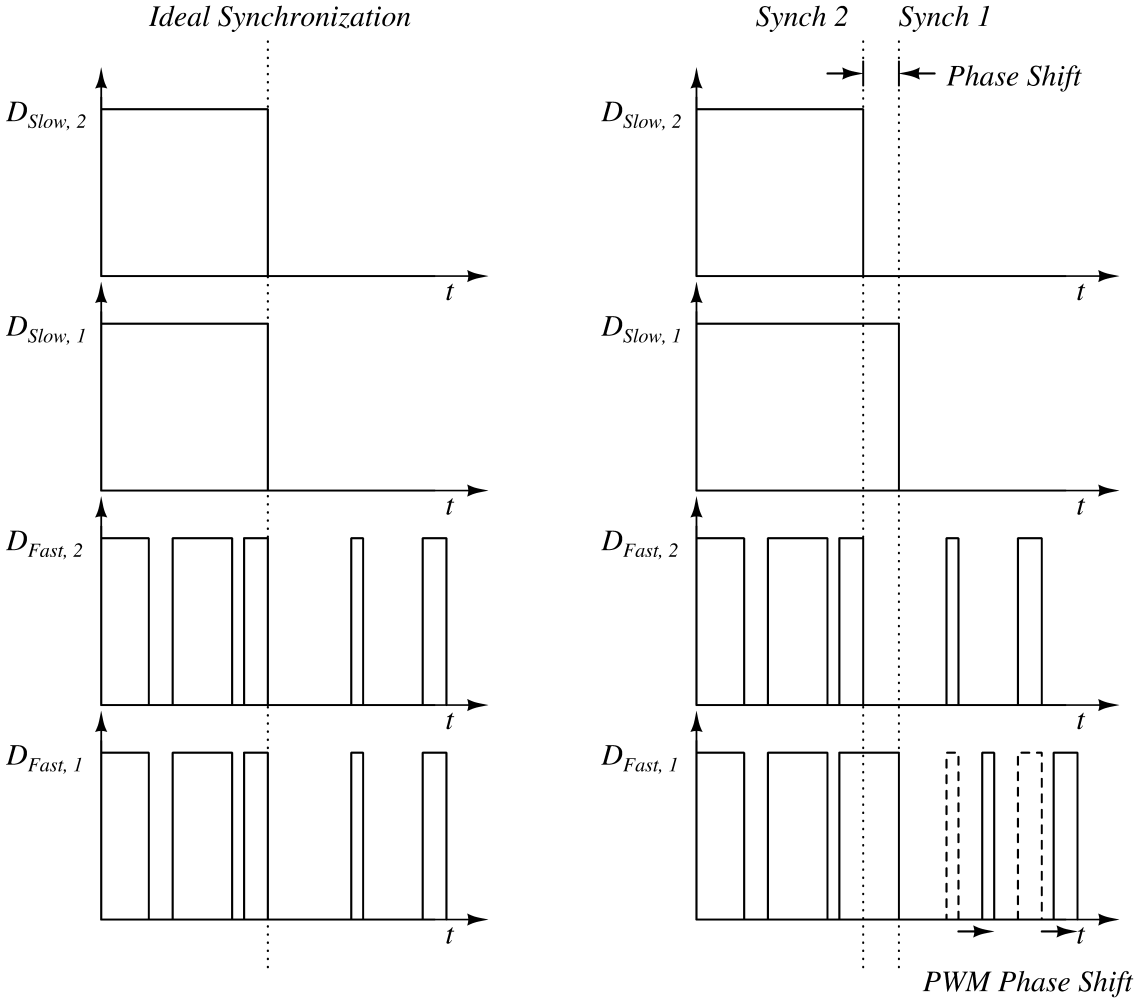

Figure 5.3: PWM alignment example showing the offset that occurs due to synchronization variance.

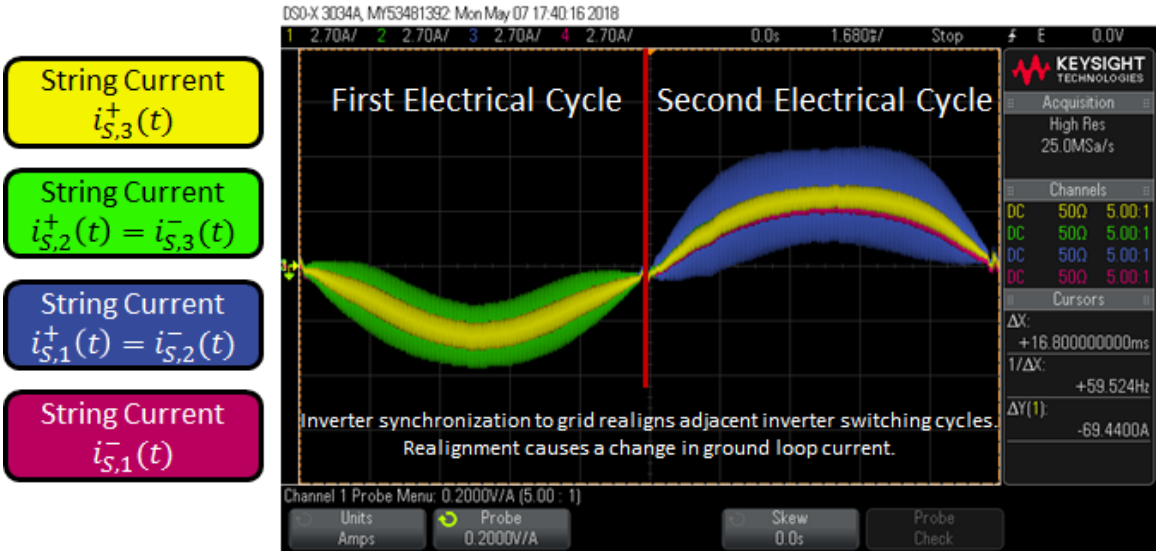

Figure 5.4: Total current measured in each wire connecting the outputs of a three module AC-stacked inverter system. During operation, the total current measured will include leakage currents that vary in magnitude as the switching of the inverters is realigned during grid synchronization.

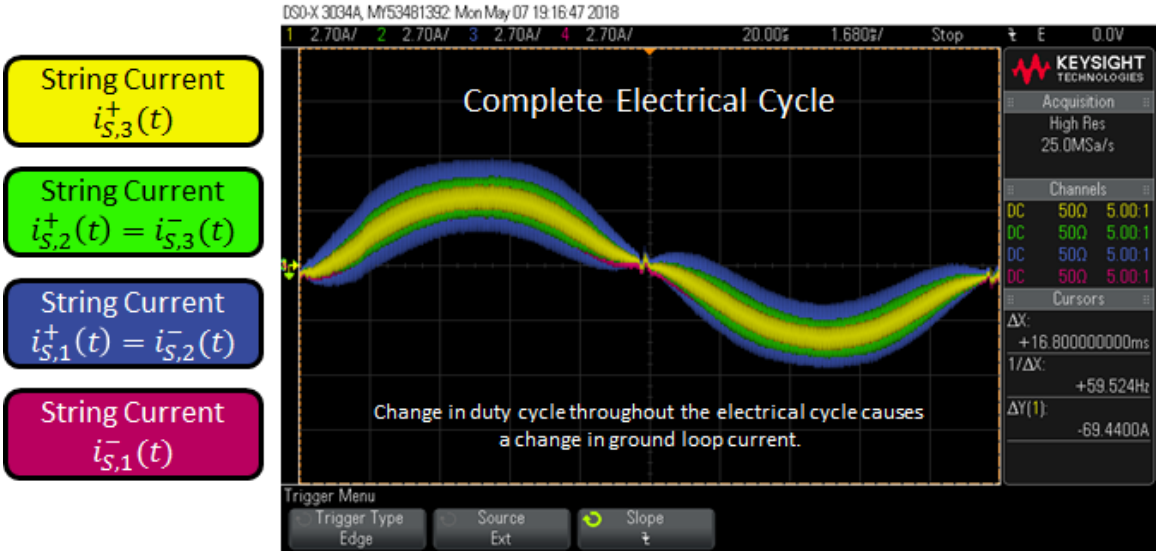

Figure 5.5: A complete electrical cycle showing the leakage currents vary in magnitude due to changing duty cycle throughout the electrical cycle causing the leakage current to be cyclostationary.

The receiver coil will detect all frequencies of noise on the single line no matter if it is differential or common-mode. Above the AWGN is the noise introduce from the switching of the inverters. That noise can be described as four components. The first

component is the 500 kHz switching noise from unipolar switching of the fast side MOSFETs and is directly proportional to the duty ratio. The magnitude of the duty ratio is the largest at the peak of the electrical cycle as portrayed in figure 5.6. Also, the duty ratio is the lowest at the zero crossing of the electrical cycle where there is even a dead band from the physical implementation just not being able to handle the small duty ratio. The time domain expression and the associated continuous time Fourier transform is found in equations 5.2 and 5.3.

$$n_{500kHz}(t) = \frac{V_{DC}}{Z_{GND}} m_a(\theta - \sigma) \sin(2\pi 500E3t) \tag{5.2}$$

$$n_{500kHz}(f) = \frac{V_{DC}}{Z_{GND}} m_a(\theta - \sigma) \left(\frac{j}{2} [\delta(500E3) - \delta(-500E3)] \right) \tag{5.3}$$

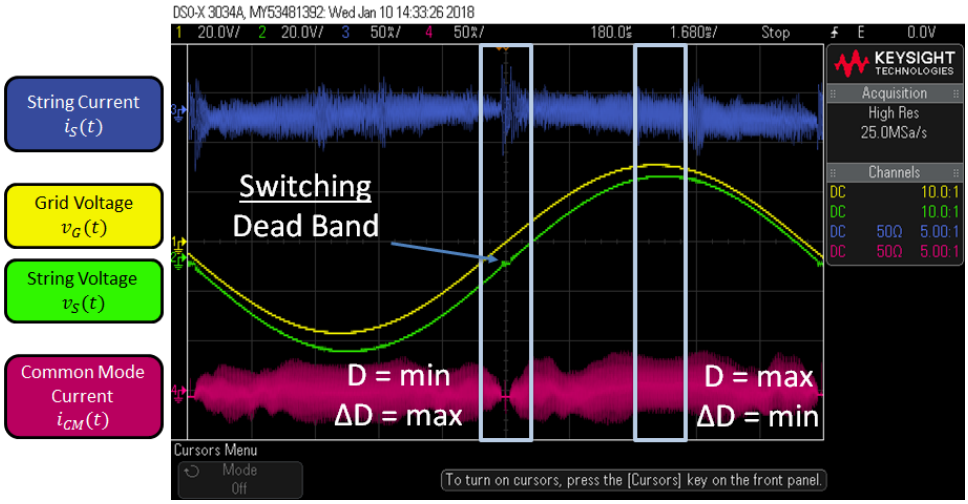

Figure 5.6: Visual portrayal of the time slices of the duty ratio control of the inverter's switches are at the upper and lower limits. At the zero crossing, the duty ratio is the lowest as seen by the output voltage being close to zero. The controller is adjusting the duty ratio at the fastest rate at the zero crossing as the output is changing the fastest. At the peak of the electrical cycle is where the duty ratio is the largest. The amount of change in the duty ratio is the lowest here.

The second component is the 100 kHz noise which is generated by the duty ratio update rate of the controller. The controller samples the voltage and current at 100 kHz and then recalculates the appropriate duty cycle. This change in the duty ratio,

the duty ratio derivative, is the largest near the zero crossing of the electrical cycle as portrayed in figure 5.6. The time domain expression and the associated continuous time Fourier transform is found in equations 5.4 and 5.5.

$$n_{100kHz}(t) = \frac{\delta\left(\frac{V_{DC}}{Z_{GND}} m_b(\theta - \sigma)\sin\left(2\pi 100E3t\right)\right)}{dt} \tag{5.4}$$

$$n_{100kHz}(f) = \frac{V_{DC}}{Z_{GND}} m_b(\theta - \sigma)\left(\frac{1}{2}\left[\delta(100E3) + \delta(-100E3)\right]\right) \tag{5.5}$$

The third component is the 20 kHz noise which is generated by the resonance of the output filter of the inverter. The LC filter has a Q factor, seen in equation 5.6 which relates to the amount of resonance and the peak value the LC filter has [83]. The inverter is designed such that the losses are the smallest possible and hence, resistance is kept to the minimum of the wiring resistance only in the LC filter. This creates a high q value and the LC filter is excited every time the inverter switches. The time domain expression and the associated continuous time Fourier transform is found in equations 5.7 and 5.8.

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{5.6}$$

$$n_{20kHz}(t) = \frac{V_{DC}}{Z_{Damp}}\sin\left(2\pi 20E3t\right) \tag{5.7}$$

$$n_{20kHz}(f) = \frac{V_{DC}}{Z_{Damp}}\left(\frac{j}{2}\left[\delta(20E3) - \delta(-20E3)\right]\right) \tag{5.8}$$

The final component is the impulsive noise which is generated by the switching of the low MOSFETs in the unipolar switching. The inverter can be thought of being in steady state which experiences a sudden step change in the DC voltage when the switch occurs. This step change in voltage happens across the inverters self capacitance which results in a current across this capacitance as described in the time domain expression of equation 5.9. Taking the continuous time Fourier transform, a

flat response is expected across all frequencies as seen in equation 5.10. This impulse response of the inverter is only seen at the zero crossing of the electrical cycle and by definition, brief in time.

$$n_{impulsive}(t) = C_{inverter}\frac{\delta\left(V_{DC}\,\mathrm{sgn}\left(\sin\left(2\pi 60t\right)\right)\right)}{dt} \tag{5.9}$$

$$n_{impulsive}(f) = C_{inverter}V_{DC} \tag{5.10}$$

5.2 Noise Measurements in the AC-Stacked Inverter Architecture

The time domain noise measurements does not give much information to the impact of the noise at the communications frequency. To better understand that, the noise measurements are transformed into the frequency domain utilizing the fast Fourier transform (FFT) and into a spectrogram which is a plot of the FFT with respect to time. Many publications analyzing the noise of solar inverters already look at the FFT to measure and model the noise. These measurements though are typically across the entire electrical cycle or multiple electrical cycles [78,79,81,82]. This is vastly different from the noise measurements of the voltage mode PLC communications where the window of the FFT is only half of the electrical cycle and the spectrograms examine the noise throughout the whole electrical cycle with a moving window [53] but do not try to model the sources of the noise as they do not know what will be connected to the grid. Here, this work utilizes the modeling of the inverters to understand and characterize the noise sources like classical inverter modeling but changes the measurement to a small window for the FFT and spectrogram to see the true impact on the communications. The FFT and the spectrograms analyzed are taken from a time window of 1 ms at the zero crossing and the peak of the electrical cycle with the idea portrayed in figure 5.7. These windows for the FFT and the time span for the spectrogram coincide with the switching noise shown in the earlier section relating to the duty cycle and the impulsive response of the inverter.

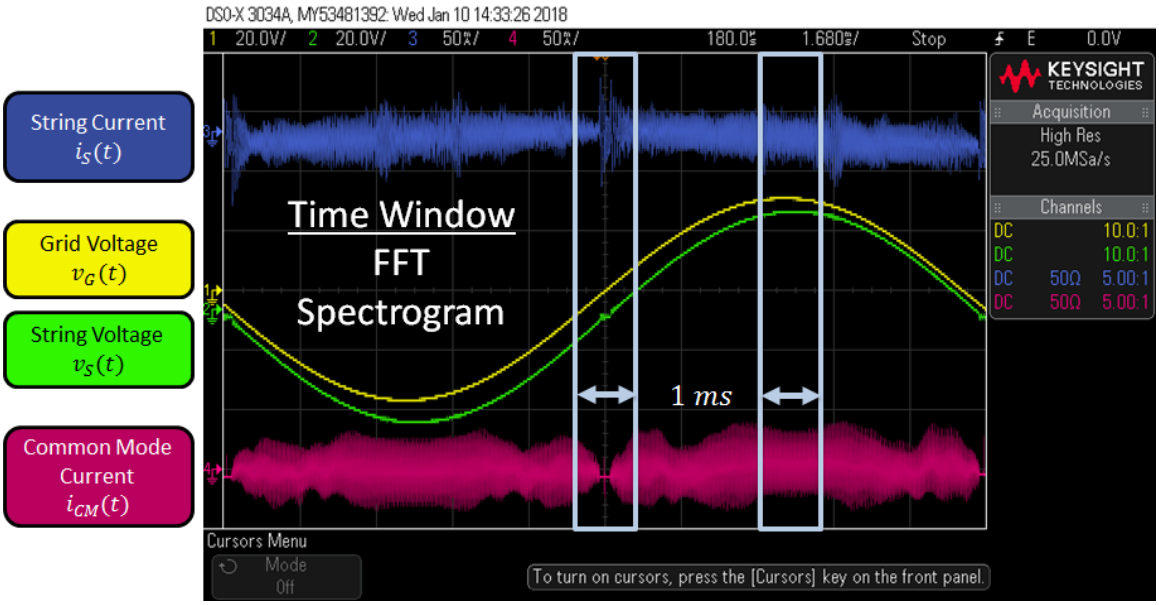

Figure 5.7: Visual portrayal of the time slices of the noise is taken for the FFT window and the spectrogram analysis. A 1 ms window is used to examine and measure the noise at the zero crossing and peak of the electrical cycle.

The system is configured for these tests in three inverter system utilizing linear power supplies with an output voltage of approximately $32\,V_{DC}$. Linear supplies were used as it was the best way to approximate the low parasitic capacitance to ground that would be in a typical PV system for the AC-stacked inverter architecture. The system was set to operate in a switching mode before the grid interface makes connection between the string and grid. As such, the system is not producing any power and has no 60 Hz current component. This condition is noted to be the worst case noise condition for the AC-stacked inverter architecture as it would have the highest PV voltage on the DC input of a solar panel. The total string current is measured between the second and third inverter and the common-mode current is measured by sum mating both the positive and negative current outputs of the third inverter. This is accomplished by setting the current probe to be clipped around both output wires of the third inverter. It is noted that in the noise analysis and measurements, radiated noise as a noise source is not considered simply due to the complexity of identifying and measuring.

The conversion of the FFTs is seen in figures 5.8 for the window around the zero crossing and figure 5.9 for the window around the peak of the electrical cycle. The first noise component examined is the AWGN which is establishing the noise floor in the plots. The AWGN is approximately -86.45 dB for the total current and -83.55 dB for the common-mode current for the zero crossing window. This changes for the peak of the electrical cycle where the noise floor is -99.45 dB for the total current and -93.03 dB for the common-mode current. The cause of this difference will be more apparent when looking at the spectrograms, but shows why the entire electrical cycle should be examined with regards to communications.

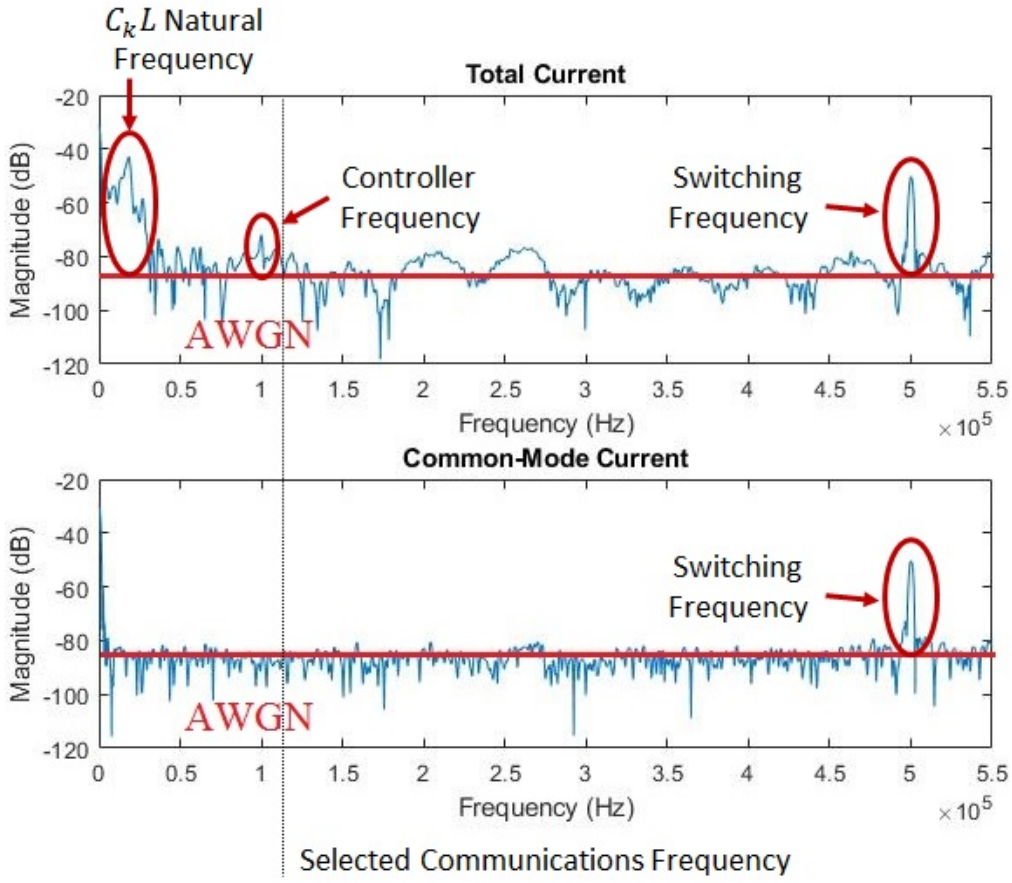

Figure 5.8: Fast Fourier transform (FFT) of the currents of figure 5.1 showing the frequency spectrum of the noise that occurs centered at the zero crossing of the electrical cycle. Highlighted in the frequency spectrum is the AWGN, switching noise, the output filter resonance, and the controller update noise.

Above the noise floor in the total current of figure 5.8 can bee seen several types of noise. The first noise is at 20 kHz and is from the C_kL resonance of the output filter. The resonance is measured as -43.45 dB. The second noise is at 100 kHz and is the PWM update from the controller. This controller noise is -72.7 dB. Finally the 500 kHz switching noise is seen with a magnitude of -51.6 dB. Looking at the common-mode components of the noise, only the 500 kHz switching noise is present with a magnitude of -50.68 dB.

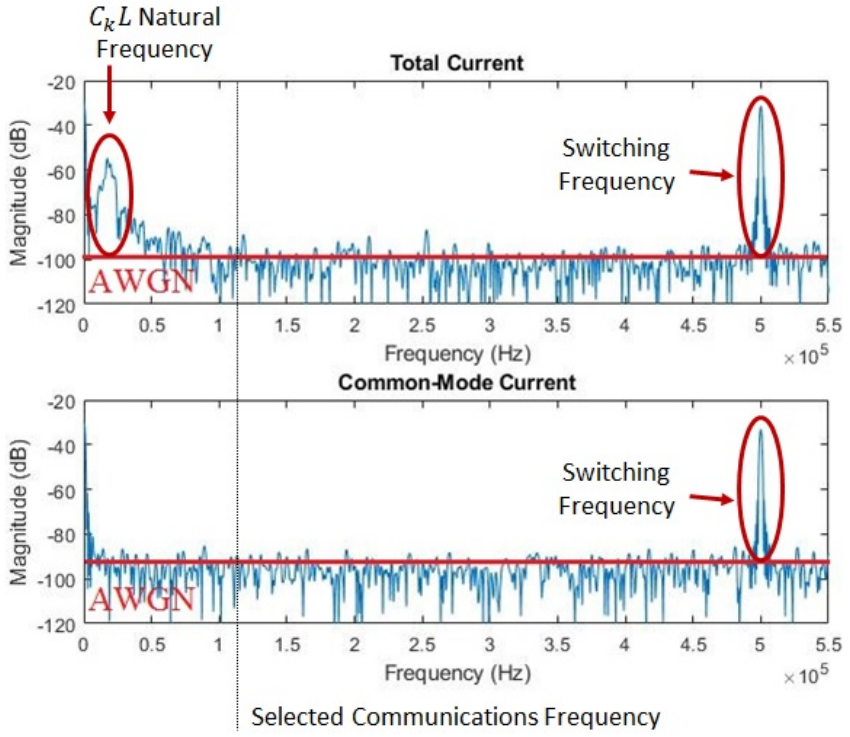

Figure 5.9: Fast Fourier transform (FFT) of the currents of figure 5.1 showing the frequency spectrum of the noise that occurs centered at the peak of the electrical cycle. Highlighted is the AWGN, switching noise, and the output filter resonance. The magnitude of the noise sources is observed to be of a different magnitude at the peak of the electrical cycle as the noise from the zero crossing of the electrical cycle.

Examining the peak of the electrical cycle, the above the noise floor in the total current of figure 5.8 only consists of the 20 kHz C_kL resonance of the output filter and the switching noise. The resonance is measured as -55.38 dB. The 500 kHz switching noise is seen with a magnitude of -32.33 dB. Looking at the common-mode

components of the noise, only the 500 kHz switching noise is present with a magnitude of -33.59 dB. The lack of the the controller noise and the increase of the switching noise relates exactly as expected for the duty ratio and rate of change of the duty ratio when the window is moved from the zero crossing to peak of the electrical cycle.

The noise in the FFTs show that only one noise is close to the communications frequency utilized in this design. If the communications channel is utilized for other frequencies such as 500 kHz, it may be necessary to reduce the noise in the channel. Reduction of the common-mode noise at 500 kHz can be accomplished with the use of a common-mode filter at the output of the converter. The sizing of this common-mode inductance is accomplished by utilizing a known measurement of the noise and parasitic capacitance to ground whereby a new impedance can be added in series such that it reduces the noise amplitude. Shown in figure 5.10 is the reduction of the switching noise by 10 dB with the use of a common-mode choke.

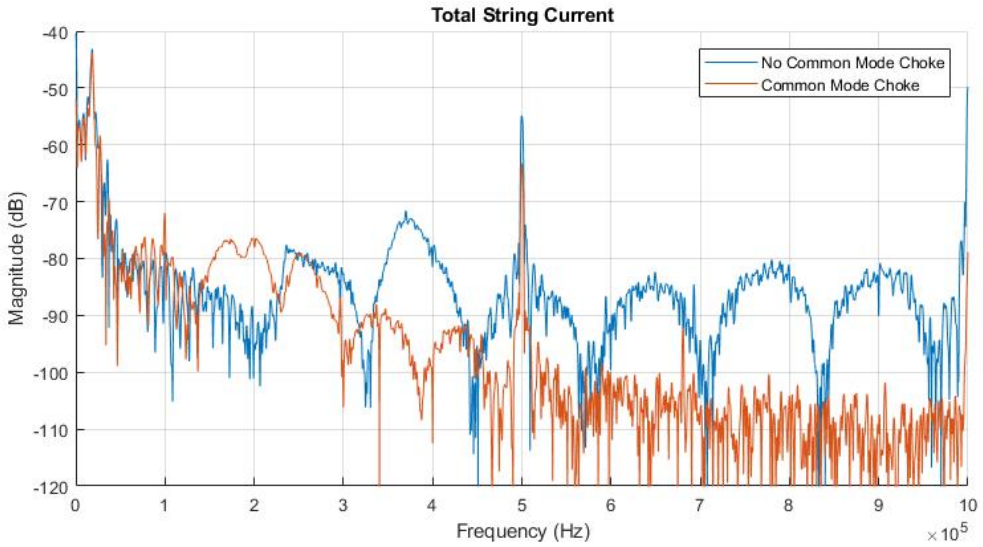

Figure 5.10: Reduction of common mode noise as seen in the total sting current with the addition of a common mode filter at the output of the inverter module.

The spectrogram is a comparison of the power spectral density (PSD) in the frequency domain of a signal as it progresses in time. Shown in figure 5.11 is the spectrogram across three electrical cycles of the system. Observed in this spectro-

gram is the cyclostationary nature of the switching noise as it progresses through the electrical cycle. The 500 kHz noise in particular is easily seen to correlate to the duty ratio of the inverter.

The scale of the spectrogram is a bit different than that of the FFT. The FFT is expressed as the current magnitude in dB while the spectrogram is expressed as the power of the signal in dB divided by the frequency. The conversion from PSD to the magnitude expressed in dB is seen in equation 5.11.

$$magnitude(dB) = 20\log\left(10^{\frac{PSD}{10}} f\right) \tag{5.11}$$

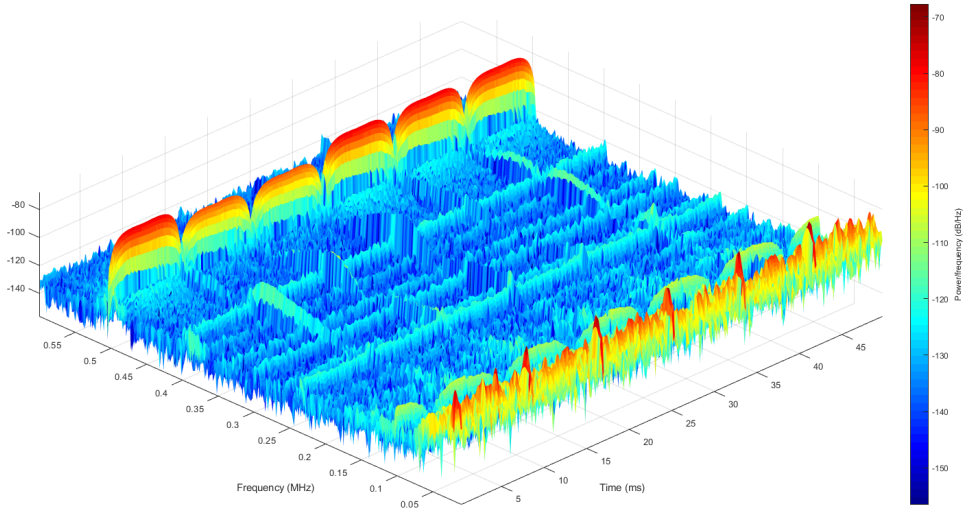

Figure 5.11: Spectrogram showing the power spectral density (PSD) of the noise across three electrical cycles of the AC-stacked inverter system during switching operation but without generating power into the electrical grid. Shown is the frequency range from 10kHz to 600kHz with the dominant noise frequencies being 20kHz and 500kHz. Seen in the spectrogram is the cyclostationary nature of the noise arising throughout the electrical cycle with a band of impulsive noise occurring across all frequencies at the zero crossing of the inverters.

Examining the spectrogram in the 1 ms window at the zero crossing reveals all noise sources clearly in figure 5.12. The noise floor is around $-125\,dB/Hz$. The switching

frequency at 500 kHz can be seen decreasing as it approaches the zero crossing with a deadband appearing for roughly $150\,\mu s$. At the very middle of the zero crossing, the slow MOSFETs switch creating the impulse response and can be seen as labeled in figure 5.12. This noise is the maximum noise observed at the communications frequency and is roughly $-100\,dB/Hz$. Also observed is the controller noise at 100 kHz and is seen decreasing the further from the zero crossing. The 20 kHz resonance is seen at all times with the noise varying with different levels of excitation.

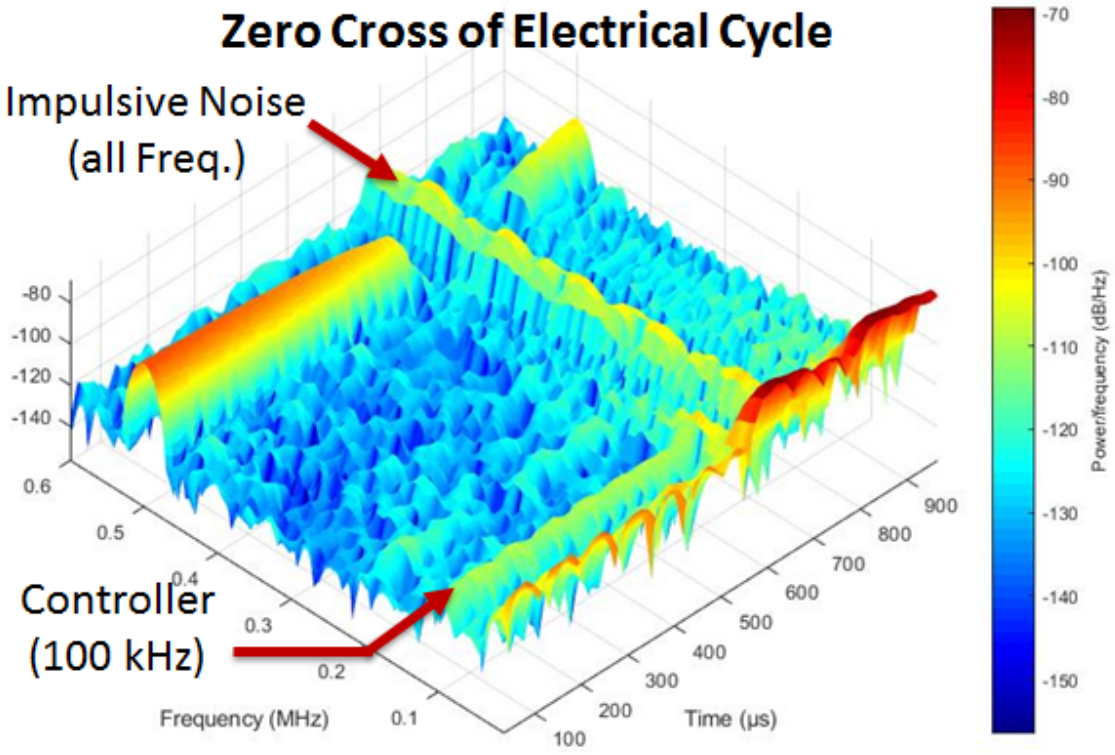

Figure 5.12: Spectrogram showing the power spectral density (PSD) of the noise zoomed in at the zero crossing of the electrical cycle. Shown here is the controller noise introduced at 100 kHz, the impulsive noise that is flat across all frequencies, the 500 kHz switching noise which reduces as the duty cycle falls, and the output filter resonance response.

Examining the spectrogram in the 1 ms window at the peak of the electrical cycle reveals only the switching noise and the resonance response as seen in figure 5.13. The noise floor is once again around $-125\,dB/Hz$. The switching frequency at 500

kHz can be seen almost constant across the peak with roughly $-75\,dB/Hz$ of noise. No observation is seen of the controller noise at 100 kHz. There is no noise observable above the noise floor at the communications frequency. The 20 kHz resonance is once again seen at all times with the noise varying with different levels of excitation.

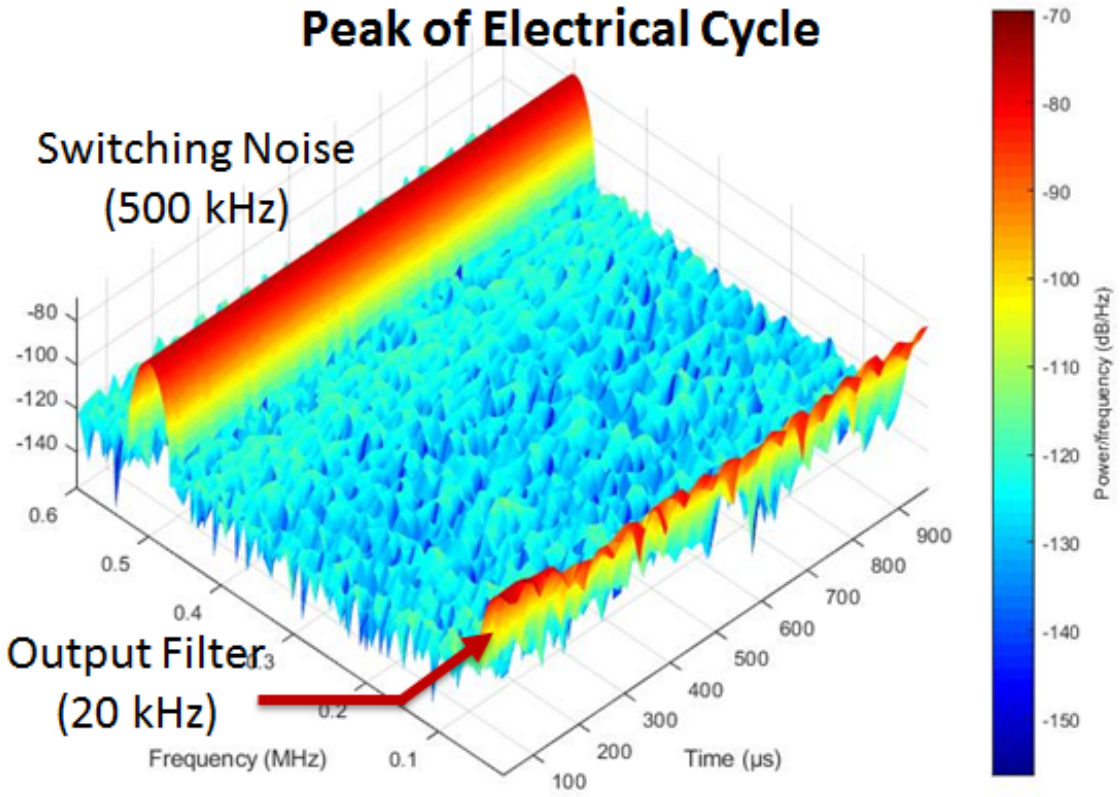

Figure 5.13: Spectrogram showing the power spectral density (PSD) of the noise zoomed in at the peak of the electrical cycle. Shown here is the 500 kHz switching noise, which appears steady since the duty cycle remains almost constant, and the output filter resonance response.

5.3 Reliability of Communications

For reliability testing, the AC-stacked inverter architecture was configured to utilize three PV inverter modules connected to the grid interface. The synchronization for these PV inverters came from the grid interface but was configured to run on a separate wire from the powerline such that operation of the inverters were not impacted while running a test that intentionally reduces the signal strength of the

PLC to create measurable errors. The grid interface was connected to an AC power supply that can deliver or absorb power, hence acting as an emulated grid. The emulated grid voltage was set to $36\,V_{RMS}$ at 60 Hz. The inverter modules connected to supply set up as a PV emulator with an open circuit voltage of $32\,V_{DC}$. The system was then ran continuously while the signal to noise ratio (SNR) was swept across a range to obtain the bit error rate of the receiver. The grid interface was set to not close the relay between the string and the grid such that the PV inverters was outputting a peak voltage, the worst case noise condition observed.

A second grid interface was utilized to inject the PLC onto the powerline. The grid interface also has a receiver board build in such that transmitted communications may be observed. The receiver coil was attached to the wiring between the second inverter's positive output and the third inverter's negative output. The inverters are numbered with respect to increasing voltage output such that the first inverter's output to ground would be $12\,V_{RMS}$ and the third inverter's positive output to ground would be $36\,V_{RMS}$. This connection point of the receiver coil ensures that the noise added in the channel model due to multi-mesh common-mode noise is included.

The software running on this second grid interface was configured to modulate the PLC at the positive going zero crossing as in real system operation and then observe the output of the receiver board for any bits received. Since the receiver's PLL chip suffers from a design defect that occasionally contains a 360° flip when modulation occurs, the software contains a lockout window to neglect such an occurrence since it is not due to noise. The software then counts any pulse from the receivers TTL output outside of this lockout window as a fake synchronization signal, or a bit error. Once a modulation occurs from this second grid interface, the software then observes if the synchronization signal is recovered from the receiver board. A successful recovery of this signal is counted as a successful transmission and no recovery as a missed transmission, or a bit error. As the system continuously runs, the software counter keeps

track of the total modulations, fake synchronizations, and missed synchronizations.

The method of detection for the bit errors using the debug mode of the DSP controller of the grid interface is shown in figure 5.14. During the initial coding of the counters used to quantify the bit error rate, manual verification was performed for a detected error. Figure 5.15 shows once such error occurring. In this bit error example, the receiver experienced enough noise at the detection coil to cause the receiver to output a bit even though there was no modulation that occurred at the transmitter since it was not the positive zero crossing of the grid voltage.

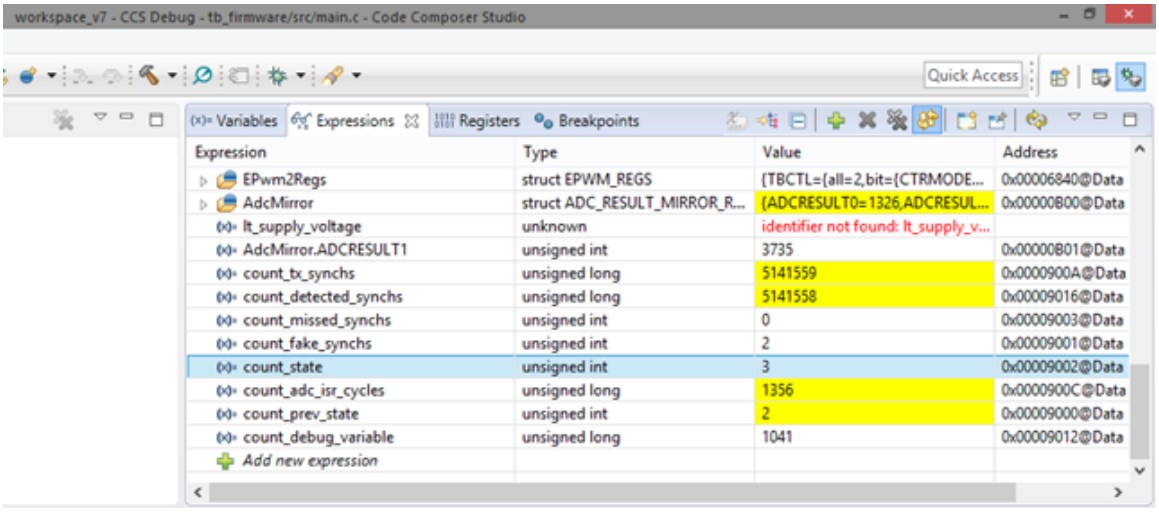

Figure 5.14: Debug mode of Texas Instruments embedded development software showing the running counters of the bit error rate test. The microcontroller tracks the number of transmitted bits, correctly received bits, missed bits, and the false bits. The bit errors, missed and false bits, is divided by the correctly received bits to determine the bit error rate.

After reviewing the proper operation of the bit error counting code in the DSP, the system was ran for an appropriate amount of time to get a calculation of the bit error rate from the data of the counters, typically in the range of 2 hours to 24 hours as the bit error rate decreased and hence took longer for an error to occur. The results were tallied and plotted in figure 5.16. The bit error rates starts high at approximately one out of a hundred. Due to the nature of the noise, the fake synchronization signals detected in this result was due to the unique noise at the zero

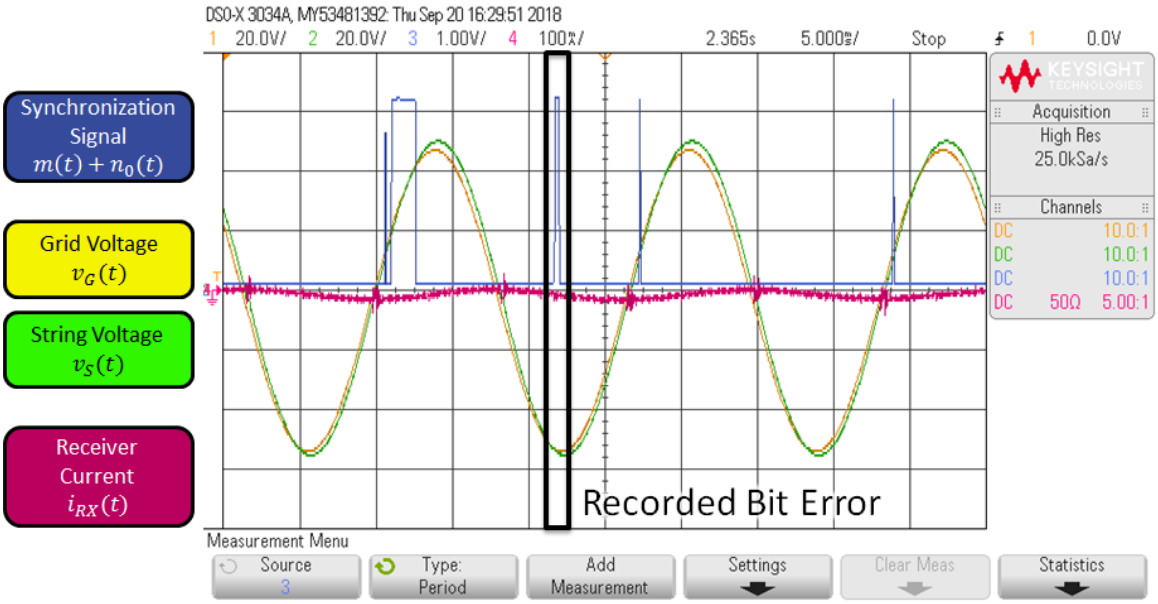

Figure 5.15: Observed bit error in the receiver during operation of the AC-stacked inverter system during switching operation but without generating power into the electrical grid. Bit error occurs slightly before the peak of the electrical cycle.

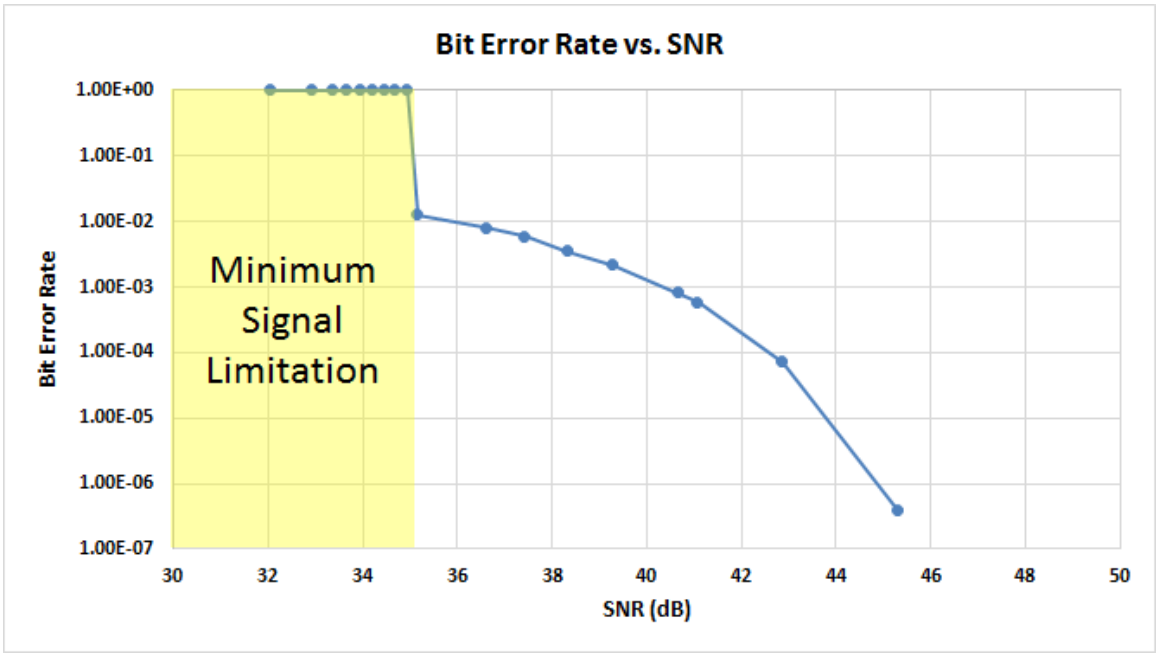

Figure 5.16: Plot of the observed bit error rate compared to the signal to noise ratio of the communications current detected by the receiver.

crossing of the inverters as it was consistently detected at the negative going zero crossing. As the signal strength increased and the error rate started dropping, the

errors appearing become much more distributed across the electrical cycle instead, a sign that the signal has become more than the noise at the zero crossing.

Depending on the control implementation in the AC-stacked inverter architecture, a bit error rate as high as 0.001 can be handled. It is unknown what utilities will specify as an acceptable error rate for commercial solutions as this work was academic in nature, but for the sake of this dissertation, it will be specified as 1E-6. It is shown that from the experimentally found bit error rate of this hardware that a SNR in the range of +45 dB would successfully reduce the probability of error to the specified rate for operation of the AC-stacked inverter architecture [84].

CHAPTER 6: RESULTS OF THE POWER LINE CARRIER WITH RUNTIME OPERATION OF SWITCHED MODE POWER CONVERTERS

The AC-stacked inverter architecture described in chapter 1 has been implemented and extensively field tested utilizing the power line communications presented. The string interfaces with a 120 V_{RMS} grid and consists of eight individual inverters. Figure 6.1 shows the complete system. Given that it currently is in a development phase, it has been designed to be easily reconfigured for different tests. Specifically, the system has the following configuration options:

- DC-Side Connections: The inverters can each be fed by either a 60-cell PV module or a PV emulator. Each PV emulator consists of a current-limited 500W DC power supply in series with a small resistor.
- AC-Side Connections: The string is interfaced to the grid through an electromechanical switch and an inductor. The grid can be either the actual utility distribution network or an emulator. This grid emulator consists of a programmable source and a programmable load connected in parallel to absorb additional power.
- PLC Connection: For testing and development purposes, the PLC signal can be transmitted either via a separate communications wire or on the power line itself.

The remainder of this chapter describes tests performed using several different system configurations. The purpose is to show the effectiveness of the proposed communications scheme and its impact on the operation of the power electronics.

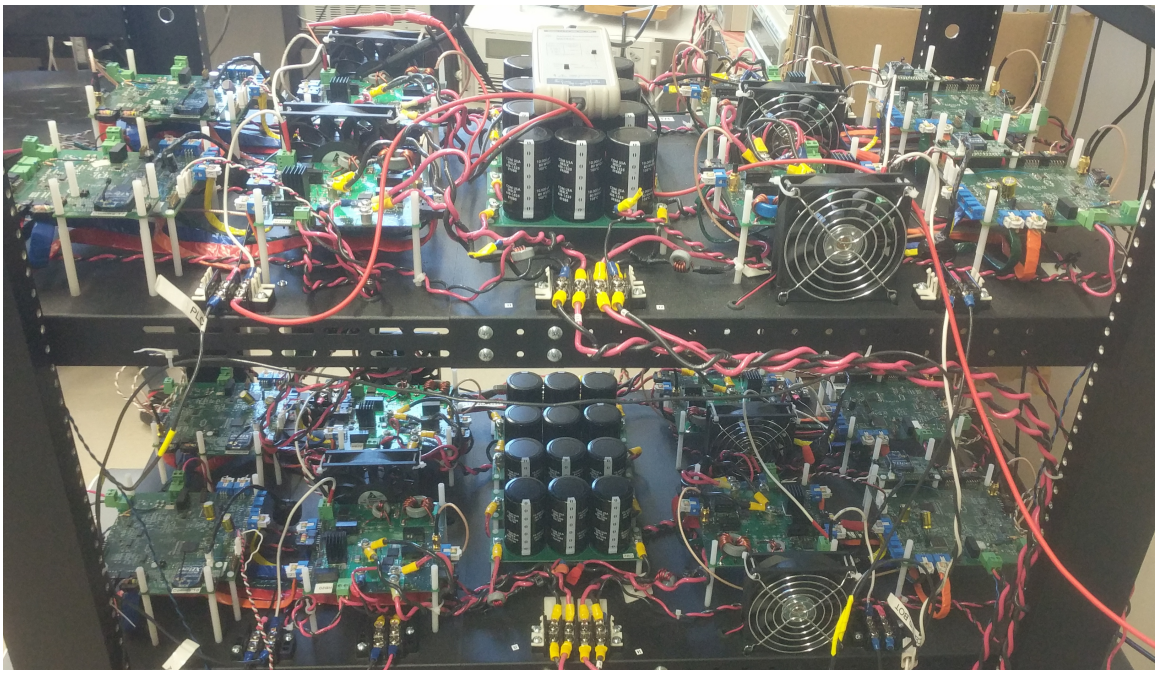

Figure 6.1: Laboratory prototype of the AC-stacked inverter architecture. This prototype system was used to verify the model for the transmission model presented for series-connected power electronics. Shown is a system comprised of eight inverters that can be configured to use 1 to 8 inverters as desired.

6.1 System Operation of the AC-Stacked Switched Mode Power Converters with the PLC on a Separate Line

The operation of the communication layer is demonstrated in figure 6.2 and shows the performance when the communications scheme utilizes the dedicated wire. The receiver coil in each inverter is placed around this separate wire, which contains only the communications current. It couples this current current into the detection circuit that then demodulates the BPSK signal and outputs the TTL zero cross information to the controller for synchronization to the grid voltage. When the grid voltage (yellow) transitions from negative to positive, the transmitter encodes this into the communications current (pink) using the BPSK technique described previously. The impact is clearly apparent in the measured communications current, which decreases its magnitude in response to the zero-cross of the voltage. The measured delay from the grid voltage crossing to the modulation is $100\,\mu s$ and the receiver's demodulation

approximately another $50\,\mu s$. This delay is below the maximum allowable delay for a power factor greater than 0.99. The green waveform shows the pulse output of the demodulator in one of the inverters.

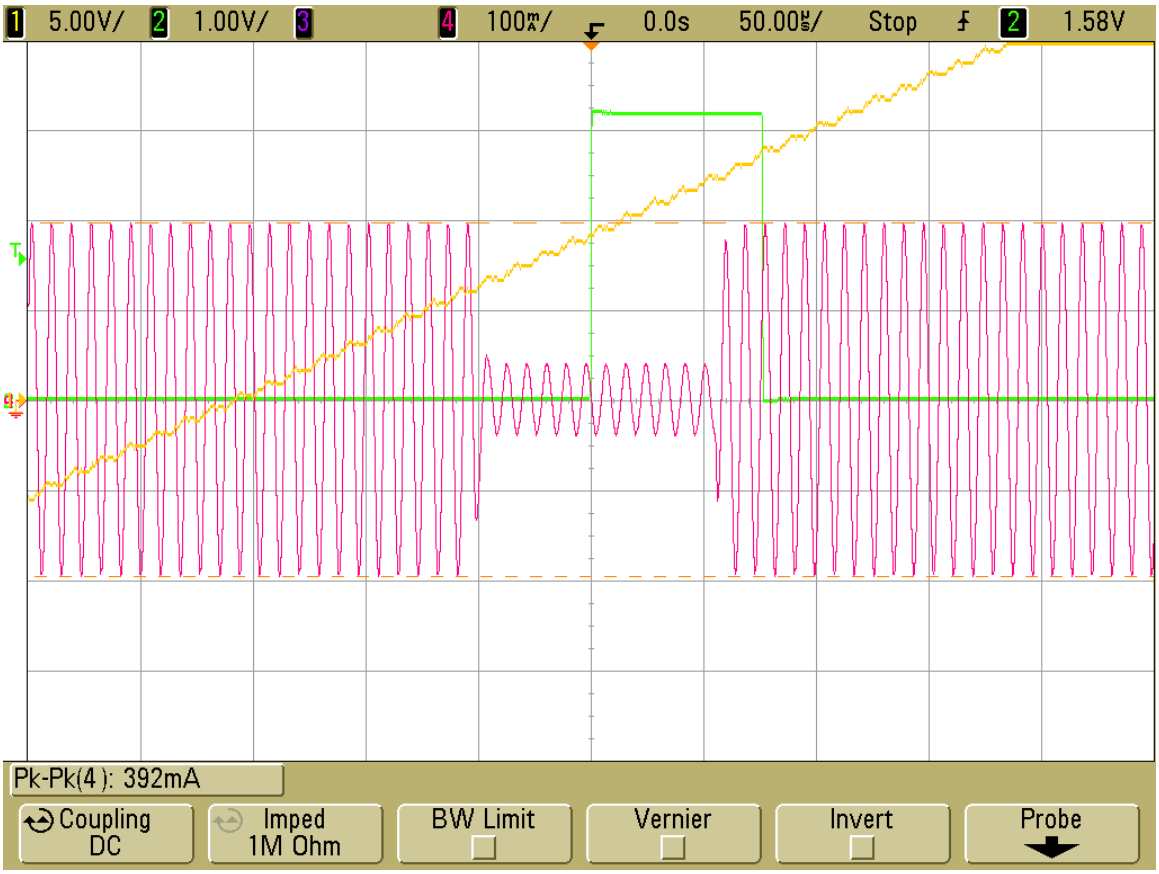

Figure 6.2: Operation of the communication system in the AC-stacked inverter architecture using a separate wire. Communications current (pink), grid voltage (yellow), and received pulse signal at one of the inverters (green) during normal operation.

Figure 6.3 demonstrates the performance of the complete system under normal operating conditions when connected to the actual $120\,V_{RMS}$ grid and providing power from 225W PV panels. The blue waveform shows the received pulse at one of the eight inverters. Note that it rises as the grid voltage (yellow) crosses through zero. In this image, the width of the received synchronization pulse at the zero-cross appears wider than the one shown in figure 6.2. This results from the fact that the PLL in the receiver circuit occasionally experiences short-term cycle slips shortly after the

synchronization pulse. A cycle slip occurs when the phase difference in the PLL's phase detector grows to be 360 degrees so that the loop ultimately remains locked. As the phase moves through the transient, however, the demodulator output responds as if a new BPSK pulse has been received. This phenomenon is not fully understood, but it occurs at a much higher frequency when the inverters are actively switching so it is believed to be caused by the higher noise in the system. This behavior is consistent with literature on the impact of noise in PLLs [63], but further analysis is required to fully understand it and mitigate it. Given that such behaviors will always be an issue of concern no matter how exceptional the hardware, the control software features a lockout window and a basic frequency filter designed to disregard any second pulse that falls too closely to the believed zero-cross to be a real synchronization event. The controls are thereby not affected by this event.

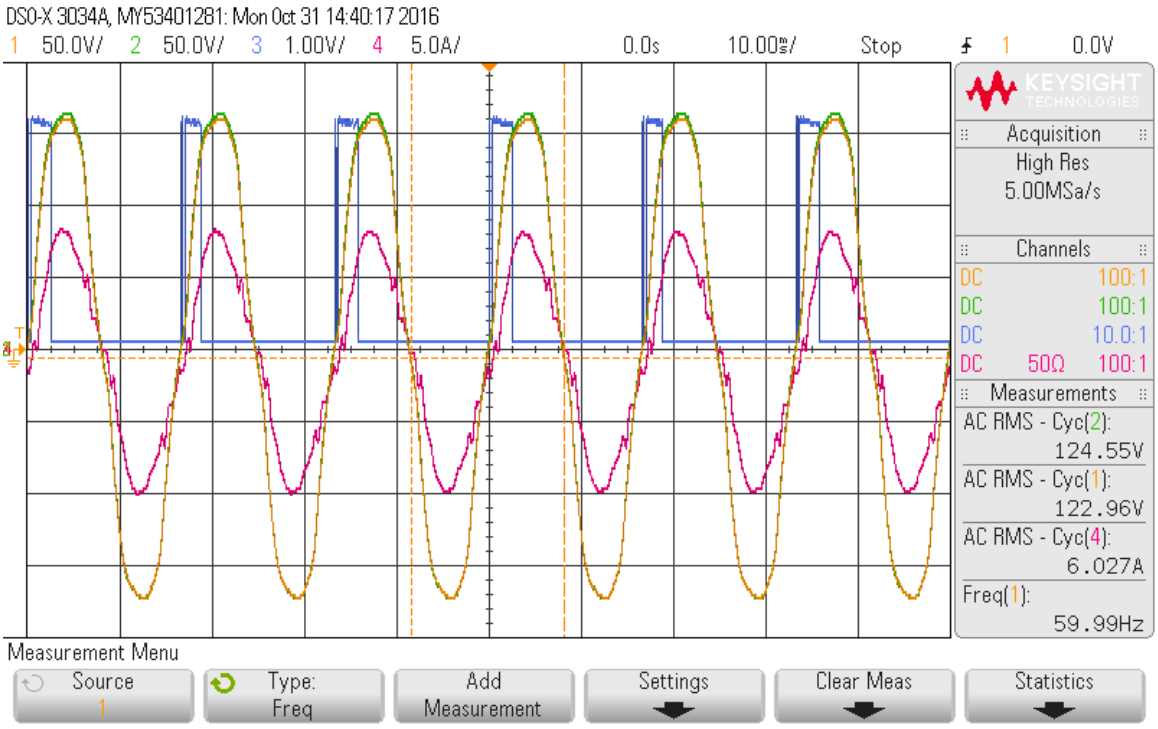

Figure 6.3: AC-Stacked inverter architecture operating utilizing current-mode powerline communications on a separate wire. Received pulse signal (blue), grid voltage (yellow), and string current (red) during normal grid-tied operation. Distortion in the string current is caused by harmonics in the grid voltage at the test site. THD remains within acceptable limits.

6.2 System operation of the AC-Stacked Switched Mode Power Converters with the PLC Integrated with the Power Line

The separate communications wire was initially introduced to allow the PLC subsystem and the power electronics to be separately developed so that any issues with one would not affect the other. The primary concern was the potential impact on the controller discussed in chapter 1. Once both had been demonstrated, appropriate integration proceeded. Testing was initially conducted with the inverters connected to the grid emulator and the PV emulators.

Figure 6.4 demonstrates the operation of the communications system when the power line was also used as the communications medium. In this image, the full

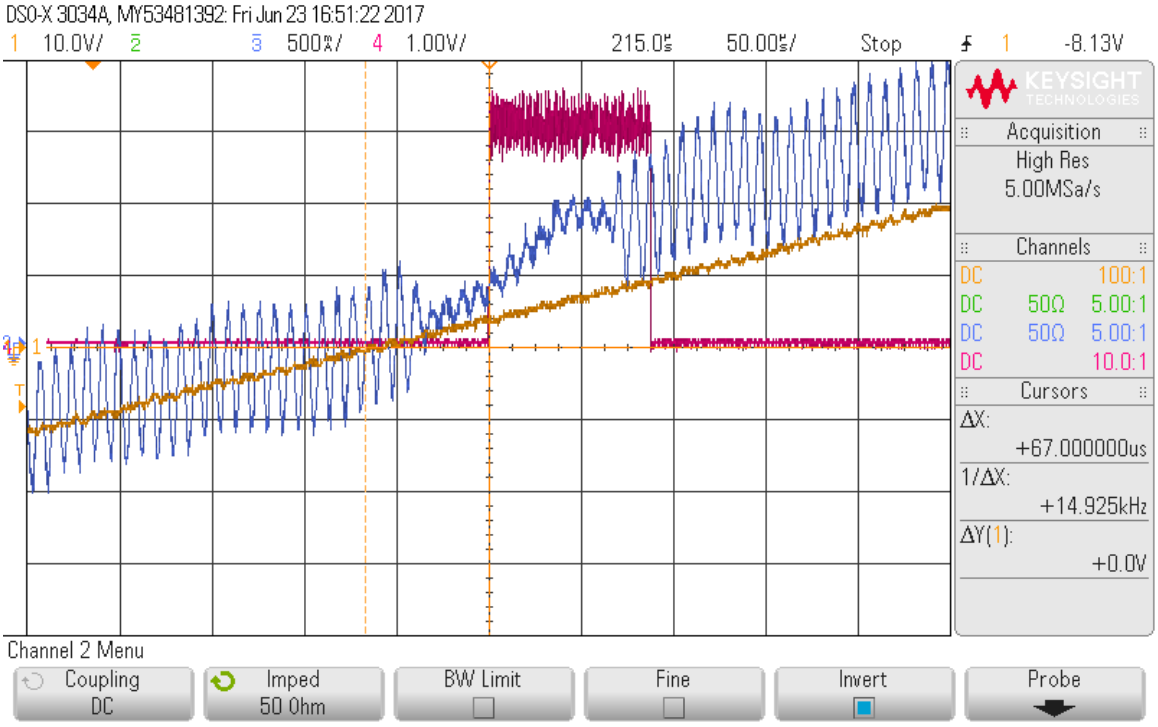

Figure 6.4: Operation of the communication system in the AC-stacked inverter architecture using the powerline. Emulated grid voltage (yellow), string voltage (green), string current (blue), and received pulse (red) during normal grid-tied operation to a grid emulator. Shown is a zoomed in version of figure 6.5 to show the string current containing both the communications signal as well the 60Hz current for power generation demonstrating the solution is a PLC. The inverters are using the received pulses of the receiver circuit for grid synchronization.

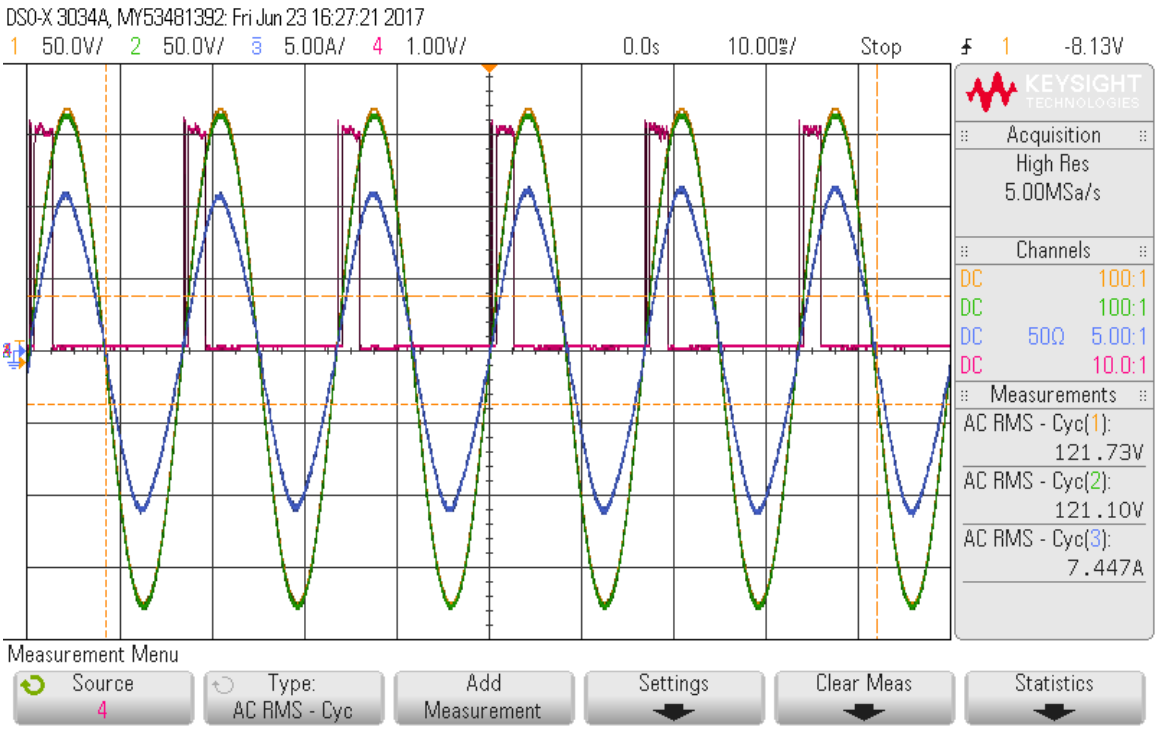

Figure 6.5: AC-Stacked inverter architecture operating utilizing current-mode power-line communications on the powerline. Emulated grid voltage (yellow), string voltage (green), string current (blue), and received pulse (red) during normal grid-tied operation to a grid emulator. Distortion in the string current is caused by harmonics introduced via the current controller in the AC-stacked inverter system. There is ongoing development in the control system that has yielded lower results, but not yet published or utilized for these results.

8-Inverter string is delivering 900 W into the grid emulator at 120 V_{RMS}. The blue waveform is the string current, which clearly shows the communications signal superimposed atop the line-frequency component. As the grid voltage (yellow) transitions from negative to positive, the communications current clearly decreases its amplitude as expected. The red waveform shows the TTL output provided to the controller for synchronization. Given the design of the receiver, it takes about 40 μs from the time it first receives the BPSK portion of the communications current until the time when the receiver's synchronization pulse transitions from low-to-high. Combined with the delay at the transmitter, the total amount of time from the zero-crossing to the rising edge of the synchronization pulse is about 67 μs. The overall variance between the

timing of this edge at the various inverters has been found to be about $10\,\mu s$, and it arises mainly from component tolerance. Note that delays on this order will have no measurable effect on the phase of the generated voltage. Any impact of dynamic variations on the harmonic output is explored below.

Figure 6.5 demonstrates the performance of the complete system when communications occurs over the power line. This image shows the emulated grid voltage (yellow) and the string current (blue). The pink waveform is the output of one of the receiver circuits. Note that the cycle slips described previously are still observed, but that the additional software filtering ensures that they do not effect system operation.

6.3 Analysis of the AC-Stacked Inverter Architecture's Total Harmonic Distortion with PLC Integration

One of the major concerns with using PLC for synchronization was its impact on the operation of the peak current controller. This behavior was assessed by measuring the total harmonic distortion (THD) in the current waveform when the full system was operating both with and without the dedicated communications wire. In the laboratory, the grid voltage has very high harmonic levels, and these harmonics can significantly increase the amount of harmonic current. Harmonic compensation has been developed to mitigate such problems, but the nature of the development cycle on a complex project of this variety is such that the necessary controller updates have not been fully integrated into the production-level firmware. Given that the basic harmonic impact is smaller when the system is connected to a purely sinusoidal AC grid, we connected the string to the grid emulator. To avoid any dynamic effects caused by variable cloud cover, PV emulators were connected at the input of each inverter.

Figure 6.6 shows the measured string current waveform both with (bottom) and without (top) the dedicated communications wire. The waveforms are qualitatively similar. Figures 6.7 and 6.8 show the frequency content of the string current over

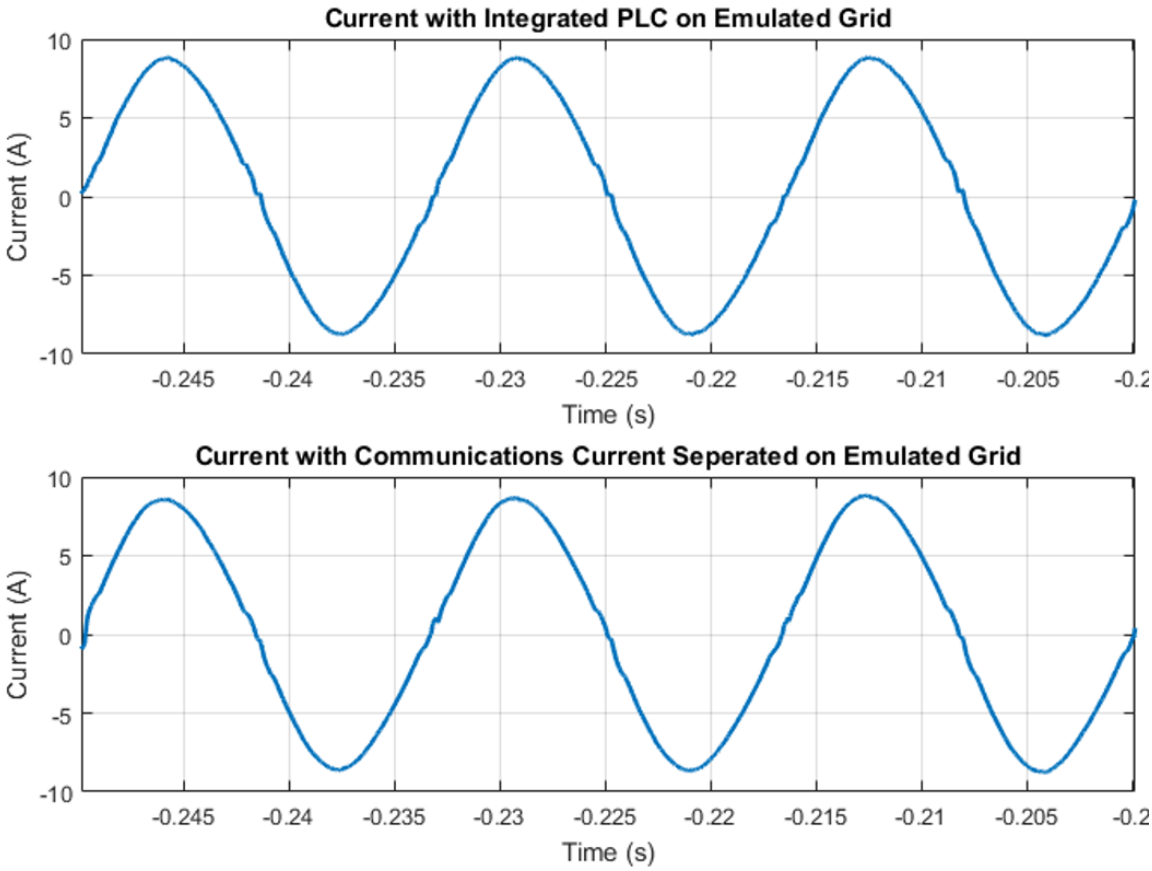

Figure 6.6: Time domain comparison of string current between figures 6.7 and 6.8 zoomed in to visually show the minimal impact of the communications current on the current controller. The current is visually the same. The plots are made from comma-separated values (CSV) data from the scope.

a 2kHz span beginning at DC. Once again, the results appear qualitatively similar. Table 1 shows the measured THD at steady-state current levels between $3\,A_{RMS}$ and $10\,A_{RMS}$. Note that the THD is slightly lower in most cases when the PLC is injected onto the power line, although the values are clearly comparable in all cases. The results make clear that the PLC has no measurable impact on the operation of the controller. As described previously, however, the THD is somewhat high in all cases. This results from the fact that no harmonic compensation is currently included in the system, and proper compensation can clearly reduce this. The bottom line is that no additional harmonic content is generated by integrating the communications onto the power line.

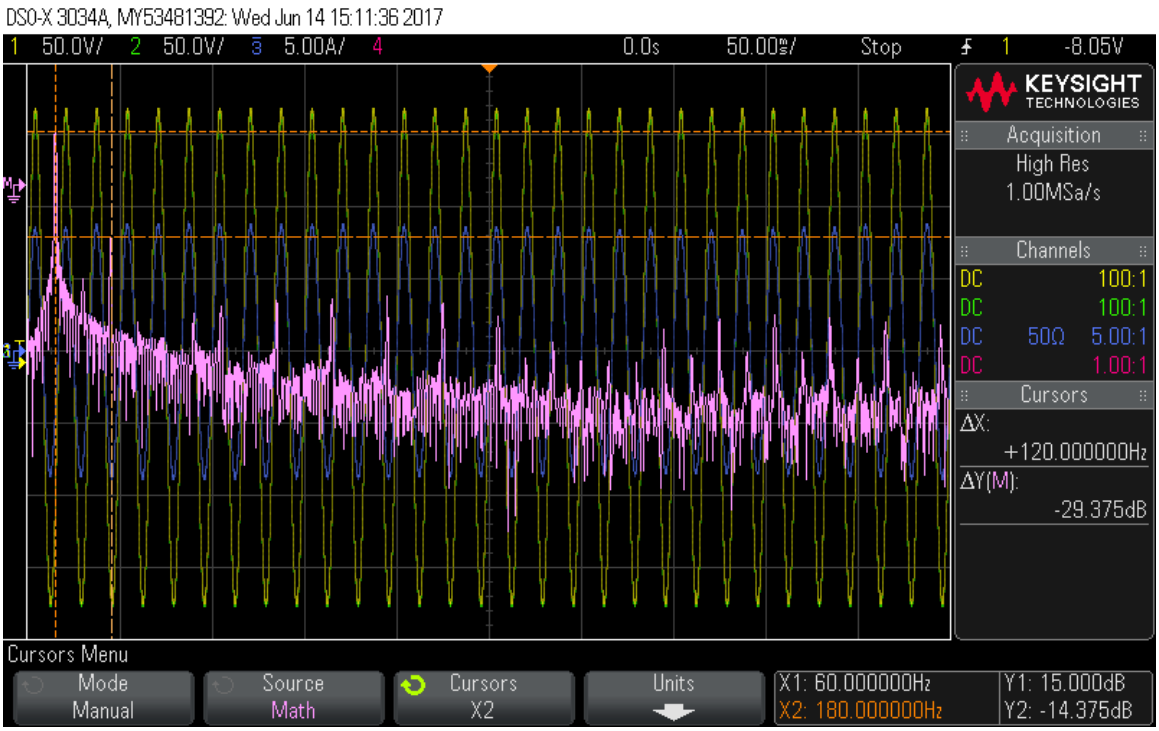

Figure 6.7: FFT of the string current during operation with powerline communications on a separate wire. Emulated grid voltage (yellow), string voltage (green), string current (blue), and FFT (pink) during normal grid-tied operation to a grid emulator. Grid emulator used to isolate PLC impact on THD from varying noise in real grid. THD calculated from converting a CSV file of the FFT in dB to RMS values and then examining the fundamental frequency magnitude with all harmonic magnitudes up to 2kHz.

Table 6.1: Comparison of the string current THD to see any impact of the communications integration to the powerline.

Current (A_{RMS})	3	4	5	6	7	8	9	10
Current THD PLC Separated	5.11%	4.17%	3.48%	3.61%	4.41%	5.84%	7.39%	8.85%
Current THD PLC Integrated	5.33%	3.74%	3.07%	3.46%	4.19%	5.69%	7.74%	8.81%

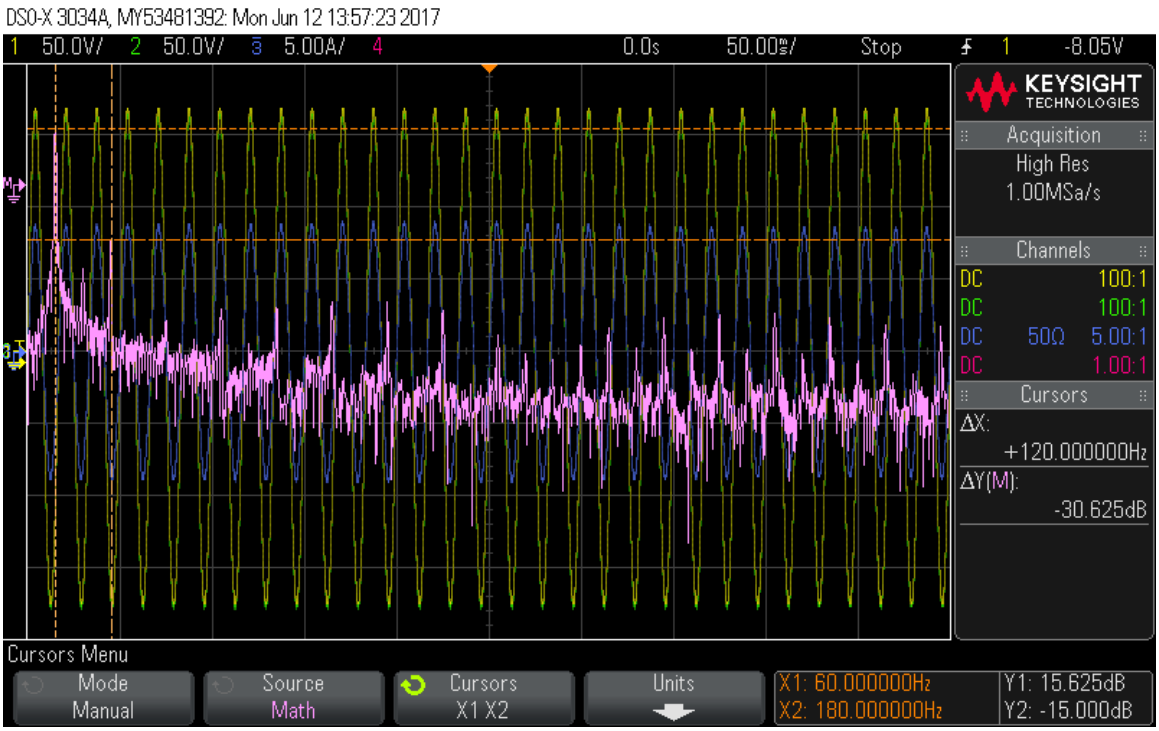

Figure 6.8: FFT of the string current during operation with powerline communications on the powerline. Emulated grid voltage (yellow), string voltage (green), string current (blue), and FFT (pink) during normal grid-tied operation to a grid emulator. The string current THD, shown here with the current communication integrated onto the power line, is similar to the results with a separate communications wire as shown in figure 6.7.

6.4 Field Test Results

The system was extensively field tested over a four-month period. During that trial, an eight-inverter array was installed at the Southeastern Solar Research Center in Birmingham, Alabama. Each inverter was connected to a 60-cell, 225 W monocrystalline panel, and the entire system was interfaced to the $120\,V_{RMS}$ distribution network at the site. Once again, challenges imposed by the complexity of the project required the team to use a dedicated communications wire. Figure 6.9 shows the performance of the eight-module system over a typical day. During the four-month evaluation period, no synchronization or communications-related failures were observed [85]. This result further validates the fact that the cycle-slip behavior discussed previously is not a major concern.

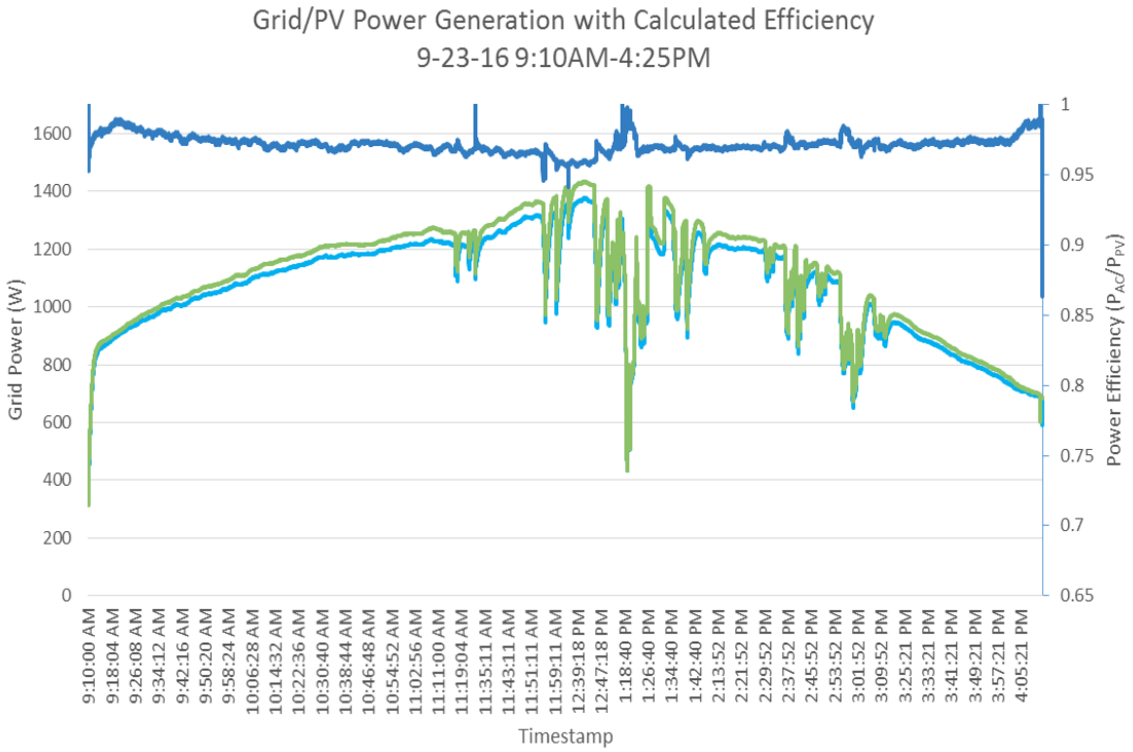

Figure 6.9: Field test results of the AC-stacked inverter architecture deployed in Alamabama. Shown is the total DC side power (green), grid power (light blue), and calculated efficiency (dark blue) over one day at the field site.

CHAPTER 7: SUMMARY, CONCLUSION AND FUTURE WORK

Presented in this research is a novel current-based powerline communications framework by which series connected power electronics are utilized as a physical medium for PLC communications. Sound electrical engineering principles are utilized for theoretical concepts of injecting a current signal through the series connected power electronic modules which is then built upon by simulations of the communication framework for the current-mode PLC. Unlike a lot of theoretical dissertations, this research moves beyond simulations and is actually implemented as real system for proof of work, comparison to theoretical, and observations for future improvements and applications. The developed current-mode powerline communications was utilized for a synchronization method that enables completely decentralized AC-stacked inverter operation. The successful operation of the solar converter system with the AC-stacked inverters shows practical realization of the theoretical design. The results will be generalized for any series-connected power-electronics architecture. A patent has been filed on the proposed approach [86]. Even though the application utilized was an AC-stacked inverter architecture, the results are generalized for any series-connected power-electronics architecture.

The results included demonstrate the scope of the issues that must be addressed when balancing the requirements of the communications system with the functionality of the power electronics. The AC-stacked architecture is attractive because it easily scales to match any AC system voltage and allows significant reduction of the passive filter elements. As the number of inverters increases, however, more noise is injected into the system and thus more common-mode filtering is needed. The fact that string size and parasitic capacitances are unknown when a given inverter is manufactured

make it difficult to optimally design the output filter which has a clear impact on the performance of the current-mode PLC communications. A set of boundaries must be imposed by the current-mode PLC communications on the power electronics design and vice versa before any optimization occurs such that the performance of either is not neglected.

As series-connected devices become more prevalent, market demand for a powerline communications system will eventually bring forth a retail sales solution for these communication systems. There is no reason that prevents standard voltage-mode communication protocols, such as G3-PLC or Prime, being utilized for upper protocol layers for current-mode powerline communication so long as the underlying physical layer was adapted for the current-mode design. With a cost effective physical layer implementation, utilizing the existing infrastructure for communications will simplify the design for such installations and hence costs. Pushing the adaption of a powerline solution series-connected devices is the security of such devices in sensitive areas of infrastructure. Any type of eavesdropping or disruption of communication would then require direct access whereby the system would already be compromised.

The innovative modeling in this dissertation lays the foundation for the first layer of a communications protocol that can be used in these current based PLC communication systems. The results show a narrow band channel being utilized to reliably deliver an ultra-low latency signal via a BPSK encoding scheme. The current being transmitted though the power electronics matches the expected values and is capable of being optimized for transmission power.

Future research for this communications scheme involve establishing bidirectional communications at the physical layer. The current realization of this research is limited to simplex communications at this time from the grid interface to the AC-stacked inverters. Such an implementation requires changes to current physical access layer, but would not impact upper protocol layers. The bidirectional communications

would be a requirement before any commercial solution would become available.

A second advancement would involve advanced signal detection and filtering in the receiver. The receiver requires a high SNR for a bit error rate, much higher than theoretical SNR requirements for BPSK communications. The receiver was implemented with a very basic PLL chip which should be upgraded to a much more reliable solution and should work to reduce the SNR requirements. The filtering was designed such that switching frequency would be eliminated from the receiver, but higher harmonics may not be properly filtered with the gain-bandwidth of the current operational amplifiers. New filtering designed with proper high frequency bandwidth may aid in the locking ability of the PLL if it is subject to unlocking at those high frequencies.

A final area for future research would explore the application and functional testing of a variety of encoding schemes such as quadrature phase shift keying (QPSK) and orthogonal frequency division multiplexing (OFDM). The BPSK utilized is not the best encoding scheme for the transmission and reception of high bandwidth data. Adaptation of these encoding schemes would increase the data rates of the current-mode powerline communications as well as increase compatibility with the available standards mentioned before, G3-PLC and PRIME. It may also increase the power efficiency of the communications by reducing the time utilization of the communication channel for a given amount of data.

REFERENCES

[1] M. A. Green, "The path to 25% silicon solar cell efficiency: History of silicon cell evolution," *Progress in Photovoltaics: Research and Applications*, vol. 17, no. 3, pp. 183–189. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pip.892

[2] R. Ohl, "Light-sensitive electric device," May 27 1941, US Patent 2,402,662. [Online]. Available: https://patents.google.com/patent/US2402662A/en

[3] ——, "Light-sensitive electric device including silicon," May 27 1941, US Patent 2,443,542. [Online]. Available: https://patents.google.com/patent/US2443542A/en

[4] O. of Energy Efficiency and U. D. o. E. Renewable Energy. The history of solar. [Online]. Available: https://www1.eere.energy.gov/solar/pdfs/solar_timeline.pdf

[5] M. A. Green, Y. Hishikawa, E. D. Dunlop, D. H. Levi, J. Hohl-Ebinger, and A. W. Ho-Baillie, "Solar cell efficiency tables (version 52)," *Progress in Photovoltaics: Research and Applications*, vol. 26, no. 7, pp. 427–436. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pip.3040

[6] M. DeBono, "New sunpower panels are our most powerful ye," SunPower, March 2018. [Online]. Available: https://us.sunpower.com/blog/2018/03/26/sunpower-announces-370w-home-solar-panel/

[7] S. Kahn and et al, "U.s. solar market insight executive summary q3 2016," GTM Research and the Solar Energy Industries Association, 2016.

[8] U. E. I. Administration, "Annual energy outlook 2016 with projections to 2040," Aug 2016, dOE/EIA-0383(2016).

[9] E. Wesoff, "First solar ceo: 'by 2017, we'll be under $1.00 per watt fully installed," GTM, June 2015. [Online]. Available: https://www.greentechmedia.com/articles/read/First-Solar-CEO-By-2017-Well-be-Under-1.00-Per-Watt-Fully-Installed

[10] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded h-bridge multilevel pv inverter with distributed mppt for grid-connected applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1722–1731, March 2015.

[11] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1292–1306, Sept 2005.

[12] L. Hassaine, E. OLias, J. Quintero, and V. Salas, "Overview of power inverter topologies and control structures for grid connected photovoltaic systems," *Renewable and Sustainable Energy Reviews*, vol. 30, pp. 796 – 807, 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1364032113007545

[13] S. Kouro, B. Wu, Ã. Moya, E. Villanueva, P. Correa, and J. RodrÃguez, "Control of a cascaded h-bridge multilevel converter for grid connection of photovoltaic systems," in *2009 35th Annual Conference of IEEE Industrial Electronics*, Nov 2009, pp. 3976–3982.

[14] M. H. Balali, N. Nouri, A. Nasiri, and H. Seifoddini, "Development of an economical model for a hybrid system of grid, pv and energy storage systems," in *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, Nov 2015, pp. 1108–1113.

[15] I. Fraunhofer Institute for Solar Energy Systems. (2018, August) Photovoltaics report. [Online]. Available: https://www.ise.fraunhofer.de/en/publications/studies/photovoltaics-report.html

[16] C. Deline, B. Marion, J. Granata, and S. Gonzalez, "A performance and economic analysis of distributed power electronics in photovoltaic systems," Tech. Rep., Nat. Renewable Energy Lab, Jan 2011, NREL/TP-5200-50003.

[17] C. Deline, J. Meydbray, M. Donovan, and J. Forrest, "Photovoltaic shading testbed for module-level power electronics," Tech. Rep., Nat. Renewable Energy Lab, 2012, nREL/TP-5200-54876.

[18] S. Moskowitz, "Will the US mandate module-level power electronics in 2017?" GTM Research, Nov. 19, 2015. [Online]. Available: https://www.greentechmedia.com/articles/read/will-the-us-mandate-module-level-power-electronics-in-2017

[19] D. Feldman, R. Margolis, and D. Boff, "Q1/Q2 2015 solar industry update," Presentation, Nat. Renewable Energy Lab, July 2015.

[20] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a single-phase cascaded h-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4399–4406, Nov 2009.

[21] A. Dell'Aquila, M. Liserre, V. G. Monopoli, and P. Rotondo, "Overview of pi-based solutions for the control of dc buses of a single-phase h-bridge multilevel active rectifier," *IEEE Transactions on Industry Applications*, vol. 44, no. 3, pp. 857–866, May 2008.

[22] J. K. Yook, D. M. Tilbury, and N. R. Soparkar, "Trading computation for bandwidth: reducing communication in distributed control systems using state estimators," *IEEE Transactions on Control Systems Technology*, vol. 10, no. 4, pp. 503–518, Jul 2002.

[23] S. Bhowmik, "Systems and methods for solar photovoltaic energy collection and conversion," Dec. 27 2016, uS Patent 9,531,293. [Online]. Available: https://www.google.com/patents/US9531293

[24] N. Mohan, T. M. Undeland, and W. P. Robbins, "Switch-mode dc-ac inverters: dc $\leftrightarrow$ sinusoidal ac," in *Power Electronics: Converters, Applications, and Design*, 3rd ed. Hoboken, NJ: John Wiley & Sons, Inc., 2003, ch. 8, sec. 1-2, pp. 200–210.

[25] C. Honsberg and S. Bowden. Modules and arrays. [Online]. Available: http://pveducation.org

[26] J. D. Irwin and R. M. Nelms, "Steady-state power analysis," in *Basic Engineering Circuit Analysis*, 8th ed. Hoboken, NJ: John Wiley & Sons, Inc., 2005, ch. 9, sec. 1-11, pp. 419–470.

[27] A. E. Fitzgerald, C. Kingsley Jr., and S. D. Umans, "Synchronous machines," in *Electric Machinery*, 6th ed. New York, NY: McGraw-Hill Companies, Inc., 2003, ch. 5, sec. 4-5, pp. 266–281.

[28] M. A. Parker, L. Ran, and S. J. Finney, "Distributed control of a fault-tolerant modular multilevel inverter for direct-drive wind turbine grid interfacing," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 2, pp. 509–522, Feb 2013.

[29] Y. Park, J. Yoo, and S. Lee, "Practical implementation of pwm synchronization and phase-shift method for cascaded h-bridge multilevel inverters based on a standard serial communication protocol," *IEEE Transactions on Industry Applications*, vol. 44, no. 2, pp. 634–643, March 2008.

[30] P. C. Loh, D. G. Holmes, and T. A. Lipo, "Implementation and control of distributed pwm cascaded multilevel inverters with minimal harmonic distortion and common-mode voltage," *IEEE Transactions on Power Electronics*, vol. 20, no. 1, pp. 90–99, Jan 2005.

[31] R. Carotenuto, M. Merenda, D. Iero, and F. G. D. Corte, "Using ant communications for node synchronization and timing in a wireless ultrasonic ranging system," *IEEE Sensors Letters*, vol. 1, no. 6, pp. 1–4, Dec 2017.

[32] I. Mazhari, H. Jafarian, J. Enslin, S. Bhowmik, and B. Parkhideh, "Locking frequency band detection method for islanding protection of distribution generation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[33] I. Mazhari, L. Beghou, J. Enslin, B. Parkhideh, and S. Bhowmik, "Locking frequency band exposure method for islanding detection and prevention in distributed generation," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 4361–4366.

[34] I. Mazhari, H. Jafarian, B. Parkhideh, S. Trivedi, and S. Bhowmik, "Locking frequency band detection method for grid-tied pv inverter islanding protection," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 1976–1981.

[35] H. Jafarian, R. Cox, J. H. Enslin, S. Bhowmik, and B. Parkhideh, "Decentralized active and reactive power control for an ac-stacked pv inverter with single member phase compensation," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 345–355, Jan 2018.

[36] H. Jafarian, S. Bhowmik, and B. Parkhideh, "Hybrid current-/voltage-mode control scheme for distributed ac-stacked pv inverter with low-bandwidth communication requirements," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 321–330, Jan 2018.

[37] H. Jafarian, I. Mazhari, B. Parkhideh, S. Trivedi, D. Somayajula, R. Cox, and S. Bhowmik, "Design and implementation of distributed control architecture of an ac-stacked pv inverter," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 1130–1135.

[38] S. E. International. (2018, Jan) Revenue set to grow in power line communication market. [Online]. Available: https://www.smart-energy.com/regional-news/north-america/revenue-power-line-communication-market/

[39] C. Semiconductor. (2011, Aug) What is power line communication? [Online]. Available: https://www.eetimes.com/document.asp?doc_id=1279014

[40] M. Kasper, D. Bortis, and J. W. Kolar, "Classification and comparative evaluation of pv panel-integrated dc-dc converter concepts," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2511–2526, May 2014.

[41] C. Olalla, C. Deline, and D. Maksimovic, "Performance of mismatched pv systems with submodule integrated converters," *IEEE Journal of Photovoltaics*, vol. 4, no. 1, pp. 396–404, Jan 2014.

[42] O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo, "Cascaded h-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, vol. 2, June 2003, pp. 731–735 vol.2.

[43] H. Jafarian, B. Parkhideh, J. Enslin, R. Cox, and S. Bhowmik, "On reactive power injection control of distributed grid-tied ac-stacked pv inverter architecture," in

2016 IEEE Energy Conversion Congress and Exposition (ECCE), Sept 2016, pp. 1–6.

[44] H. Jafarian, M. Biglarbegian, and B. Parkhideh, "Controller robustness analysis of grid-tied ac-stacked pv inverter system considering manufacturing inaccuracies," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 2349–2354.

[45] H. Jafarian, N. Kim, B. Parkhideh, and J. Enslin, "Analysis of smart inverter functions of decentralized grid-connected ac-stacked pv inverter architecture," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 3594–3600.

[46] H. Jafarian, N. Kim, and B. Parkhideh, "A distributed active and reactive power control strategy for balancing grid-tied cascaded h-bridge pv inverter system," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 1667–1672.

[47] J. O. Troxler and R. W. Cox, "An adaptive framework for mitigating current harmonics caused by distributed energy resources," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2018, pp. 505–512.

[48] N. Kim, H. Jafarian, B. Parkhideh, and J. Enslin, "Performance and mitigation strategy of distributed ac-stacked pv inverter architecture under grid background harmonics," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 2291–2295.

[49] E. Candan, D. Heeger, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Hot-swapping analysis and implementation of series-stacked server power delivery architectures," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 8071–8088, Oct 2017.

[50] P. S. Shenoy and P. T. Krein, "Differential power processing for dc systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1795–1806, April 2013.

[51] S. Qin and R. C. N. Pilawa-Podgurski, "Sub-module differential power processing for photovoltaic applications," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 101–108.

[52] T. Instruments. (2005, August) Tms320c2000^{TM} digital signal controller power line communication user's guide. [Online]. Available: www.ti.com/lit/ug/spru714/spru714.pdf

[53] M. Nassar, J. Lin, Y. Mortazavi, A. Dabak, I. H. Kim, and B. L. Evans, "Local utility power line communications in the 3-500 khz band: Channel impairments, noise, and standards," *IEEE Signal Processing Magazine*, vol. 29, no. 5, pp. 116–127, Sept 2012.

[54] I. H. Cavdar and E. Karadeniz, "Measurements of impedance and attenuation at cenelec bands for power line communications systems," *Sensors*, vol. 8, no. 12, pp. 8027–8036, 2008. [Online]. Available: http://www.mdpi.com/1424-8220/8/12/8027

[55] B. P. Lathi and Z. Ding, "Angle modulation and demodulation," in *Modern Digital and Analog Communication Systems*, 4th ed. New York, NY: Oxford University Press, 2003, ch. 5, sec. 1-8, pp. 252–301.

[56] ——, "Signals and signal space," in *Modern Digital and Analog Communication Systems*, 4th ed. New York, NY: Oxford University Press, 2003, ch. 2, sec. 1-10, pp. 20–90.

[57] ——, "Amplitude modulations and demodulations," in *Modern Digital and Analog Communication Systems*, 4th ed. New York, NY: Oxford University Press, 2003, ch. 4, sec. 1-10, pp. 178–251.

[58] W. T. McLyman, "Transformer and inductor design handbook." New York, NY: Marcel Kekker, 2004.

[59] M. Zahn, "Electromagnetic field theory: A problem solving approach." Malabar, FL: Krieger, 1979.

[60] A. S. Sedra and K. C. Smith, "Operational amplifiers," in *Microelectronic Circuits*, 6th ed. New York, NY: Oxford University Press, 2010, ch. 2, sec. 1-8, pp. 52–123.

[61] D. Binkley, "Lecture 11: Cascaded design of 2nd, 4th, 6th, and 8th order filters," Course Notes, Elect. and Comp. Eng., UNC Charlotte, Oct 2011.

[62] N. Semiconductor. (2018, October) Hef4046b msi phase-locked loop. [Online]. Available: https://www.nxp.com/documents/data_sheet/HEF4046B_CNV.pdf

[63] T. H. Lee, "Phase-locked loops," in *The Design of CMOS Radio-Frequency Integrated Circuits*, 1st ed. New York, NY: Cambridge University Press, 1998, ch. 15, sec. 1-9, pp. 438–478.

[64] A. S. Sedra and K. C. Smith, "Signal generators and waveform-shaping circuits," in *Microelectronic Circuits*, 6th ed. New York, NY: Oxford University Press, 2010, ch. 17, sec. 1-9, pp. 1334–1395.

[65] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, "Variablefrequency dc/ac converters," in *Principles of Power Electronics*, 1st ed. Reading, MA: Addison-Wesley Publishing Company, Inc., 1992, ch. 8, sec. 2, pp. 173–179.

[66] D. Evans and R. Cox, "Powerline communications strategy enabling fully decentralized control of ac-stacked pv inverters," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 2277–2284.

[67] B. P. Lathi and Z. Ding, "Performance analysis of modulated communication systems under noise," in *Modern Digital and Analog Communication Systems*, 4th ed. New York, NY: Oxford University Press, 2003, ch. 10, sec. 1-4, pp. 564–600.

[68] D. Evans and R. Cox, "Series-connected power electronics as a communication medium," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2018, preceedings to be published.

[69] M. Zimmermann and K. Dostert, "A multipath model for the powerline channel," *IEEE Transactions on Communications*, vol. 50, no. 4, pp. 553–559, April 2002.

[70] D. Tse, "Lecture 9: Modeling the wireline channel: Intersymbol interference," Online, Elect. Eng. and Comp. Sci., UC Berkeley, Feb 2008. [Online]. Available: http://inst.eecs.berkeley.edu/ ee121/sp08/handouts/lecture9_ece461.pdf

[71] T. H. Lee, "Phase-locked loops," in *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. New York, NY: Cambridge University Press, 2003, ch. 6, sec. 1, pp. 202–204.

[72] D. Evans and R. Cox, "Channel modeling for powerline communications in series-connected pv inverters," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2018, pp. 1–7.

[73] F. W. Grover, in *Inductance Calculations*. New York, NY: Dover Publications, 2009, first published by D. Van Nostrand Co., New York, 1946.

[74] B. P. Lathi and Z. Ding, "Performance analysis of digital communication systems," in *Modern Digital and Analog Communication Systems*, 4th ed. New York, NY: Oxford University Press, 2003, ch. 11, sec. 1-12, pp. 605–702.

[75] R. Teodorescu, F. Blaabjerg, U. Borup, and M. Liserre, "A new control structure for grid-connected lcl pv inverters with zero steady-state error and selective harmonic compensation," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, vol. 1, Feb 2004, pp. 580–586 Vol.1.

[76] J. C. Giacomini, L. Michels, L. Schuch, H. Pinheiro, and C. Rech, "Design of a lcl filter for leakage current reduction in transformerless pv grid-connected three-level inverter," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 239–245.

[77] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 4, pp. 902–913, Nov 2010.

[78] Ó. López, F. D. Freijedo, A. G. Yepes, P. Fernández-Comesaña, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Transactions on Energy Conversion*, vol. 25, no. 1, pp. 140–147, March 2010.

[79] D. Dong, X. Zhang, F. Luo, D. Boroyevich, and P. Mattavelli, "Common-mode emi noise reduction for grid-interface converter in low-voltage dc distribution system," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2012, pp. 451–457.

[80] R. Lai, M. H. Todorovic, and J. Sabate, "Analysis and suppression of a common mode resonance in the cascaded h-bridge multilevel inverter," in *2010 IEEE Energy Conversion Congress and Exposition*, Sept 2010, pp. 4564–4568.

[81] Y. Zhou and H. Li, "Analysis and suppression of leakage current in cascaded-multilevel-inverter-based pv systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5265–5277, Oct 2014.

[82] W. Chen, X. Yang, W. Zhang, and X. Song, "Leakage current calculation for pv inverter system based on a parasitic capacitor model," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8205–8217, Dec 2016.

[83] J. D. Irwin and R. M. Nelms, "Variable-frequency network performance," in *Basic Engineering Circuit Analysis*, 8th ed. Hoboken, NJ: John Wiley & Sons, Inc., 2005, ch. 12, sec. 3, pp. 567–588.

[84] D. Evans and R. Cox, "Channel modeling for powerline communications in series-connected pv inverters," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Oct 2018, preceedings to be published.

[85] B. York, "Investigation of a series-connected solar inverter architecture," Jun 2017, ePRI Report 3002011366. [Online]. Available: http://www.epri.com/abstracts/Pages/ProductAbstract.aspx?ProductId=000000003002011366

[86] R. COX and D. EVANS, "Systems and methods for synchronizing converter modules," Jun. 23 2016, wO Patent App. PCT/US2015/066,773. [Online]. Available: https://www.google.com/patents/WO2016100865A1?cl=en

APPENDIX A: SOURCE CODE FOR MATLAB SIMULATION OF THE COMMUNICATIONS PHYSICAL LAYER

Matlab code for simulation of the current receiver coil of the receiver physical layer.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Rogowski Coil Simulation - Simulates the Transfer
    Function
% Daniel Evans
% 10/19/2016
% SineWatts (C) in conjunction with the
% University of North Carolina at Charlotte
% Department of Electrical and Computer Engineering
%
% This script file simulates the transfer function of the
% receiver coil known as a rogowski coil.

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Clear out Octave Console/Workspace and set format long

clc;
clear all;
close all;
format long;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Enable code profiling

% profile on;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Load Octave packages needed to run.
% Comment out if in Matlab.

% pkg load signal;
% pkg load control;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Create the variables to access the data.

time_step = 1E-7;
time_vector = 0:time_step:0.08;  % Time vector for grid (s
    )
f_plc = 60;
```

```
%f_plc = 113E3;
i_plc = 18.4*sin(2*pi*f_plc*time_vector);
%i_plc = 0.2*sin(2*pi*f_plc*time_vector);
R = 1100;
C = 2.2E-6;
id = 0.5;
od = 1.0;
width = 0.375;
L22 = 7.03E-6;
L21 = L22/65;
W = logspace(0,10,400);
f_measured = [1E3,2E3,3E3,4E3,5E3,6E3,7E3,8E3,9E3,1E4,2E4,
      3E4,4E4,5E4,6E4,7E4,8E4,9E4,1E5,2E5,3E5,4E5,5E5,6E5
    ,7E5,  8E5,9E5,1E6];
w_measured = f_measured*2*pi;
i_measured =
    [1.28,1.22,1.22,1.22,1.22,1.22,1.22,1.22,1.21,
    1.21,1.2,1.18,1.17,1.15,1.12,1.09,1.06,0.86,0.84,0.519,
     0.398,0.308,0.249,0.211,0.183,0.161,0.141,0.127];
v_measured =
    [0.0013,0.00175,0.00265,0.0034,0.004375,0.0051,
    0.005775,0.006725,0.0078,0.008425,0.0175,0.02475,
    0.0318,0.03875,0.0454,0.0515,0.057,0.051,0.055,
    0.065625,0.0744,0.079,0.08,0.082,0.084,
    0.086,0.086,0.086];
dB_measured = 20*log10(v_measured./i_measured);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Generate the transfer functions for the coil.

num = [-L21*C*R,0,0];
denum = [C*L22, R*C, 1];
sys = tf(num,denum);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Plot the bode plot and save data points

bode(sys, {1,10000000000});
[MAG,PHASE]=bode(sys, W);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Plot the time domain signal to verify operation in
    circuit

[v2,t_out,x_out] = lsim(sys,i_plc,time_vector);
```

```
figure;
plot(t_out,v2);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Plot the bode plot with comparison to measured data points

figure('position', [21, 61, 640, 360]);
semilogx(W,20*log10(MAG(1,:)),w_measured,dB_measured,'x','LineWidth', 2);
legend('Calculated Transfer Function', 'Measured Values','location','southeast');
title('Receiver Front End Transfer Function with Comparison to Measured Values');
xlabel('Frequency (rads/s)')
ylabel('\fontsize{18}{0}$\frac{v_{RX}}{i_S}$ (dB)', 'Interpreter', 'latex')
set(gca, 'LooseInset', get(gca, 'TightInset'));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Unload Octave packages.  Comment out if in Matlab.

% pkg unload signal;
% pkg unload control;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Conclude profiling and print results.

% profile_data = profile("info");
% profile_data = profile("info");
% profshow(profile_data,20);
% profile off;
```

APPENDIX B: SOURCE CODE FOR MATLAB SIMULATION OF THE ENCODING SCHEME

Matlab code for simulation of the modulation and demodulation technique of the physical layer.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% PLC Simulation - Simulates the Modulation and Demodulation Techniques
% Daniel Evans
% 9/22/2016
% SineWatts (C) in conjunction with the
% University of North Carolina at Charlotte
% Department of Electrical and Computer Engineering
%
% This script file simulates the modulation and demodulation techniques
% for the power line carrier (PLC) used in the communication system
% in the SineWatts Project.  This file is to be used in my writing
% of my dissertation.  This file models the ideal PLC.  A seperate
% file models the actual circuit with the look at noise.


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Clear out Octave Console/Workspace and set format long

clc;
clear all;
close all;
format long;


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Create the variables to access the data.

V_carrier = 3;                                  % Magnitude of the carrier voltage (V)
V_grid = 120*sqrt(2);                           % Magnitude of the grid voltage (V)
f_carrier = 113000;                             % Frequency of the carrier (Hz)
```

```
31 f_grid = 60;                                  % Frequency of
       the grid (Hz)
32 time_step = 0.0000001;                        % Time step for
        waveforms (s)
33 modulation_width = 0.0005;                    % Modulation
       duration of carrier (s)
34 time_vector_carrier = 0:time_step:.001;       % Time vector
       for carrier (s)
35 time_vector_grid = -0.04:time_step:0.04;      % Time vector
       for grid (s)
36
37 graph_start = (numel(time_vector_grid)-1)/4 +1;
38 graph_stop = (numel(time_vector_grid)-1)/4*3 +1;
39
40 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
41 % Create the simulated data.
42
43 v_c = V_carrier*sin(2*pi*f_carrier*time_vector_carrier);
44 v_c_inv = -v_c;
45 modulation = zeros(1,numel(time_vector_carrier));
46 PLC_signal = zeros(1,numel(time_vector_carrier));
47
48 for i=1:1:numel(time_vector_carrier)
49  if((i>1000)&&(i<(modulation_width/time_step+1000)))
50   modulation(i) = 3.3;
51  end;
52 end;
53
54 for i=1:1:numel(time_vector_carrier)
55  if(modulation(i)==3.3)
56   %PLC_signal(i) = carrier_inverted(i);
57   PLC_signal(i) = v_c(i)+0.7*v_c_inv(i);
58  else
59   PLC_signal(i) = v_c(i);
60  end;
61 end;
62
63 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
64 % Plot the figures for clarity.
65
66 figure('position', [21, 61, 1280, 720]);
67 plot(time_vector_carrier(1:200), v_c(1:200),
       time_vector_carrier(1:200), v_c_inv(1:200), 'LineWidth
       ', 2);
68 title('Carrier and Inverted Carrier');
```

```
xlabel('Time (s)');
ylabel('Voltage (V)');
legend('Carrier','Inverted Carrier')
grid on;
set(gca, 'LooseInset', get(gca, 'TightInset'));

figure('position', [21, 61, 1280, 720]);
subplot(2,1,1);
plot(time_vector_carrier, PLC_signal, 'LineWidth', 2);
title('Modulation and PLC Signals');
xlabel('Time (s)');
ylabel('Voltage (V)');
grid on;
ax = gca;
outerpos = ax.OuterPosition;
ti = ax.TightInset;
left = outerpos(1) + ti(1);
bottom = outerpos(2) + ti(2);
ax_width = outerpos(3) - ti(1) - ti(3);
ax_height = outerpos(4) - ti(2) - ti(4);
ax.Position = [left bottom ax_width ax_height];
subplot(2,1,2);
plot(time_vector_carrier, modulation, 'LineWidth', 2);
title('Modulation and PLC Signals');
xlabel('Time (s)');
ylabel('Voltage (V)');
grid on;
ax = gca;
outerpos = ax.OuterPosition;
ti = ax.TightInset;
left = outerpos(1) + ti(1);
bottom = outerpos(2) + ti(2);
ax_width = outerpos(3) - ti(1) - ti(3);
ax_height = outerpos(4) - ti(2) - ti(4);
ax.Position = [left bottom ax_width ax_height];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Move the modulation from a fixed point to the zero
    crossing.

modulation(1:numel(time_vector_grid)) = 0;
PLC_signal(1:numel(time_vector_grid)) = 0;

v_c = V_carrier*sin(2*pi*f_carrier*time_vector_grid);
v_c_inv = -v_c;
```

```
113 v_g = V_grid*sin(2*pi*f_grid*time_vector_grid);
114
115 for i=1:1:(numel(time_vector_grid)-1)
116  if((v_g(i)<0) && (v_g(i+1)>=0))
117   modulation((i+1):(i+(modulation_width/time_step)+1))=1;
118  end;
119 end;
120
121 for i=1:1:numel(time_vector_grid)
122  if(modulation(i))
123   %PLC_signal(i) = carrier_inverted(i);
124   PLC_signal(i) = v_c(i)+0.7*v_c_inv(i);
125  else
126   PLC_signal(i) = v_c(i);
127  end;
128 end;
129
130 figure('position', [21, 61, 1280, 720]);
131 plot(time_vector_grid(graph_start:graph_stop), v_g(
      graph_start:graph_stop), 'LineWidth', 2);
132 title('Grid Voltage')
133 xlabel('Time (s)');
134 ylabel('Voltage (V)');
135 grid on;
136 set(gca, 'LooseInset', get(gca, 'TightInset'));
137
138 figure('position', [21, 61, 1280, 870])
139 subplot(3,1,1)
140 plot(time_vector_grid(graph_start:graph_stop), v_g(
      graph_start:graph_stop), 'LineWidth', 2)
141 title('Grid Voltage')
142 xlabel('Time (s)')
143 ylabel('Voltage (V)')
144 grid on
145 ax = gca
146 outerpos = ax.OuterPosition
147 ti = ax.TightInset
148 left = outerpos(1) + ti(1)
149 bottom = outerpos(2) + ti(2)
150 ax_width = outerpos(3) - ti(1) - ti(3)
151 ax_height = outerpos(4) - ti(2) - ti(4)
152 ax.Position = [left bottom ax_width ax_height]
153 subplot(3,1,2)
154 plot(time_vector_grid(graph_start:graph_stop), modulation
      (graph_start:graph_stop), 'LineWidth', 2)
```

```
title('Zero Cross Detection of Grid Creating Modulation Signal')
xlabel('Time (s)')
ylabel('Voltage (V)')
grid on
ax = gca
outerpos = ax.OuterPosition
ti = ax.TightInset
left = outerpos(1) + ti(1)
bottom = outerpos(2) + ti(2)
ax_width = outerpos(3) - ti(1) - ti(3)
ax_height = outerpos(4) - ti(2) - ti(4)
ax.Position = [left bottom ax_width ax_height]
subplot(3,1,3)
plot(time_vector_grid(graph_start:graph_stop), PLC_signal(graph_start:graph_stop), 'LineWidth', 2)
title('Modulated Carrier Frequency')
xlabel('Time (s)')
ylabel('Voltage (V)')
grid on
ax = gca
outerpos = ax.OuterPosition
ti = ax.TightInset
left = outerpos(1) + ti(1)
bottom = outerpos(2) + ti(2)
ax_width = outerpos(3) - ti(1) - ti(3)
ax_height = outerpos(4) - ti(2) - ti(4)
ax.Position = [left bottom ax_width ax_height]

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Demodulate the PLC Signal by multiplying by the carrier frequency (PLL) and
% then sending the output through a low pass filter and comparator.

for i=1:1:numel(time_vector_grid)
  if(v_c(i)>=0)
    pll(i) = 3;
   else
    pll(i) = -3;
  end;
end;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Plot the modulated signal and the PLL
```

```

start_point = 2;
end_point = 400;
figure('position', [21, 61, 1280, 720]);
plot(time_vector_grid(start_point:end_point),pll(start_point:end_point), time_vector_grid(start_point:end_point),v_c(start_point:end_point), 'LineWidth', 2);
title('PLL of the Carrier Frequency');
xlabel('Time (s)');
ylabel('Voltage (V)');
legend('PLL', 'Carrier Signal');
grid on;
set(gca, 'LooseInset', get(gca, 'TightInset'));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Multiply the PLC signal with the PLL for the start of the demodulation

v_unfiltered = PLC_signal.*pll/3.3;

start_point = 2;
end_point = 400;
figure('position', [21, 61, 1280, 720]);
plot(time_vector_grid(start_point:end_point),v_unfiltered(start_point:end_point), 'LineWidth', 2)
title('PLC Signal multiplied by the PLL');
xlabel('Time (s)');
ylabel('Voltage (V)');
grid on;
set(gca, 'LooseInset', get(gca, 'TightInset'));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Construct the TC, first order, low pass filter transfer function.

R = 10000;
C = 1E-9;

num = [1];
denum = [C*R,1];
tf_lowpass_demod = tf(num,denum);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Obtain the output of the low pass filter.
```

```
235
236 [v_out,t_out,x_out] = lsim(tf_lowpass_demod,v_unfiltered,
       time_vector_grid);
237
238 figure('position', [21, 61, 1280, 720]);
239 plot(t_out(graph_start:graph_stop),v_out(graph_start:
       graph_stop), 'LineWidth', 2);
240 title('Demodulated PLC Signal');
241 xlabel('Time (s)');
242 xlim([time_vector_grid(graph_start),time_vector_grid(
       graph_stop)]);
243 ylabel('Volts (V)');
244 grid on;
245 set(gca, 'LooseInset', get(gca, 'TightInset'));
246
247 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
248 % Simulate the schmitt trigger used to convert the
       demodulated signal to TTL logic.
249
250 V_upper = 1.6;
251 V_lower = 0.9;
252 V_comparison = V_lower; % initial value for schmitt
       trigger
253
254 for(i=1:1:numel(t_out))
255   if(V_comparison == V_lower)
256     if(v_out(i) < V_lower)
257       TTL(i) = 3.3;
258       V_comparison = V_upper;
259     else
260       TTL(i) = 0;
261     end;
262   else
263     if(v_out(i) > V_upper)
264       TTL(i) = 0;
265       V_comparison = V_lower;
266     else
267       TTL(i) = 3.3;
268     end;
269   end;
270 end;
271
272 figure('position', [21, 61, 1280, 720]);
273 subplot(2,1,1);
```

```
274 plot(time_vector_grid(graph_start:graph_stop), v_g(
       graph_start:graph_stop), 'LineWidth', 2);
275 title('Grid Voltage');
276 xlabel('Time (s)');
277 xlim([time_vector_grid(graph_start),time_vector_grid(
       graph_stop)]);
278 ylabel('Voltage (V)');
279 grid on;
280 ax = gca;
281 outerpos = ax.OuterPosition;
282 ti = ax.TightInset;
283 left = outerpos(1) + ti(1);
284 bottom = outerpos(2) + ti(2);
285 ax_width = outerpos(3) - ti(1) - ti(3);
286 ax_height = outerpos(4) - ti(2) - ti(4);
287 ax.Position = [left bottom ax_width ax_height];
288 subplot(2,1,2);
289 plot(t_out(graph_start:graph_stop),TTL(graph_start:
       graph_stop), 'LineWidth', 2);
290 title('Demodulated TTL Output');
291 xlabel('Time (s)');
292 xlim([time_vector_grid(graph_start),time_vector_grid(
       graph_stop)]);
293 ylabel('Voltage (V)');
294 grid on;
295 ax = gca;
296 outerpos = ax.OuterPosition;
297 ti = ax.TightInset;
298 left = outerpos(1) + ti(1);
299 bottom = outerpos(2) + ti(2);
300 ax_width = outerpos(3) - ti(1) - ti(3);
301 ax_height = outerpos(4) - ti(2) - ti(4);
302 ax.Position = [left bottom ax_width ax_height];
```

APPENDIX C: SOURCE CODE FOR THE MATLAB SIMULATION OF THE PLL IN THE RECEIVER

Matlab code for the design of the PI Controller of the communications receiver PLL utilizing the CD4046.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% CD4046 PLL for use in Demodulation Circuit
% Daniel Evans
% 04/29/2015
% Sinewatts (C)
% University of North Carolina at Charlotte
% Department of Electrical and Computer Engineering
%
% This script file looks at the closed loop response for the CD4046 PLL
% designed for the demodulation circuit used by SineWatts. This circuit
% is set for differential 5 V rails for the Alpha Proto.

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Clear out Matlab Console/Workspace and set format long

clc;
clear all;
close all;
format long;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Create the variables that describe the system.

C = 330E-12        % Capacitance (F)
C1 = 1E-6     % Capacitance (F)
R1 = 360E3        % Resistance (Ohms)
R2 = 53.6E3         % Resistance (Ohms)
R3 = 160E3         % Resistance (Ohms)
R4 = 8E3         % Resistance (Ohms)
%R3 = 180E3         % Resistance (Ohms)
%R4 = 6.2E3         % Resistance (Ohms)
Vdd = 10           % Supply Voltage (V)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Calculate parameters for the Loop

```

```
37 Kd = Vdd / (4*pi);
38 Vc = Vdd/2;
39 Vc_min = 1.2;
40 Vc_max = Vdd-1.2;
41
42 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
43 % Create the specifications of the system.
44
45 spec_Fosc = 110E3;
46 spec_Wosc = spec_Fosc*2*pi;
47 spec_PM = 70;
48 spec_Fcross = 100;
49 spec_Wcross = spec_Fcross*2*pi;
50 spec_Flock = 10E3;
51
52 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
53 % Create the PM values of the system. PM is based on R4
       and C1
54
55 time_constant = 1/(0.1*spec_Wcross);
56 R4_cal = time_constant/C1
57
58 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
59 % Create the Loop Gain for the lock frequencies
60
61 Ko = 2*pi*(spec_Flock)/(Vc-Vc_min)
62 % Ko = 2/(R1*C)
63 R1_calc = 2/(C*Ko)
64 R2_calc = 4/(C/2*spec_Wosc-(Vc-1)/R1)
65
66 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
67 % Create the Crossover frequency with R3
68
69 R3_calc = ((Kd*Ko/(spec_Wcross^2))*(2^0.5))/C1
70 % R3 = 23567;
71 % R3 = 470000;
72
73 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
74 % Create the Closed Loop Transfer Function and plot the
       results
75
76 Open_Loop = tf([Kd*Ko*R4*C1, Kd*Ko],[R3*C1,0,0]);
77 Closed_Loop = tf([R4*C1*Kd*Ko,Ko*Kd],[R3*C1, R4*C1*Kd*Ko,
       Kd*Ko]);
78 w = [1,1E12];
```

```
79 bode(Open_Loop);
80 figure;
81 pzplot(Open_Loop);
82 figure
83 step(Closed_Loop)
84
85 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
86 % Calculate the lock range for the PLL
87
88 Wosc_min = 2*((Vc_min-1)/R1 + 4/R2)/C;
89 Fosc_min = Wosc_min / (2*pi)
90 Vc_max = Vdd;
91 Wosc_max = 2*((Vc_max-1)/R1 + 4/R2)/C;
92 Fosc_max = Wosc_max / (2*pi)
93 Wosc = 2*((Vc-1)/R1 + 4/R2)/C;
94 Fosc = Wosc / (2*pi)
```

VITA

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From 2006 to 2014, he was a teacher assistant at the University of North Carolina at Charlotte. He also participated in two summer internships with General Electric in Salem, VA, in 2008 and 2009 working with the distributed control systems group and the signal electronics, power electronics and controls group. From 2014 to 2016, he was a communications and firmware engineer at SineWatts Inc. He is currently a research assistant with the University of North Carolina at Charlotte. His area of interests include communications, control systems, embedded firmware, integrated circuit design, power converters, power electronics and signal processing.