INVESTIGATION OF DISTRIBUTED CONTROLS AND COMMUNICATIONS IN CASCADED MULTI-LEVEL INVERTER

by

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A thesis submitted to the faculty of
The University of North Carolina at Charlotte
in partial fulfillment of the requirements
for the degree of Master of Science in
Electrical Engineering

Charlotte

2018

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ABSTRACT

NISHA RAVINDRANATH MISHRA. Investigation of distributed controls and communications in cascaded multi-level inverter. (Under the direction of DR. MADHAV MANJREKAR)

This thesis investigates a cascaded H-bridge multi-level inverter topology (CHB-MLI). It utilizes a unique methodology that converts the conventional DC voltage output of a solar photo-voltaic (PV) panel to generate switched quasi-square wave AC voltages. When aggregated, the CHB-MLI realizes a superior quality multi-level waveform. This alternative approach offers advantages, such as, extracting maximum power at panel level and realizing system-level cost benefits. Sorted Stair Case Modulation is the control technique implemented on CHB-MLI. This control scheme is evaluated against two different sorting cycle scenarios: half-cycle and quarter-cycle. The simulation model is run for these scenarios (on developed case studies) with variety of solar irradiance, coefficient of variation and mean irradiance levels, when CHB-MLI is integrated with the load. The resultant percentage yields and the voltage and current ripple at panel level are documented for each scenario. It is noted that increasing the sorting frequency improves the yield and reduces the ripple when irradiance conditions are uniform; however, under non-uniform irradiance conditions, negligible improvement is observed. The benefits of distributed controller over a single master controller are analyzed. Also, the required parameters for the execution of distributed controls are identified. Multiple communication protocols are reviewed, keeping the focus on simple implementation and reducing wire requirements. Three protocols —Universal Asynchronous Receiver Transmitter (UART), Serial Peripheral Interface (SPI), and Inter-Integrated Circuit (I2C)— are studied considering various attributes. I2C protocol is implemented on the developed laboratory prototype of seven-level CHB-MLI, integrated with resistive load.

ACKNOWLEDGEMENTS

Foremost, I would like to express my sincere gratitude towards my parents, my sister, my brother, and my supporter, for believing in me and making it possible for me to follow my dream of pursuing higher education.

I would like to thank my advisor, Dr. Madhav Manjrekar for his throughout support, guidance and encouragement, this accomplishment would not have been possible without him. The door to his office was always open whenever I ran into a trouble spot. He steered me in the right the direction whenever he thought I needed it.

It would be my duty to extend my gratitude to the committee members Dr. Tiefu Zhao and Dr. Valentina Cecchi for spending time to assess my work and participating in my thesis.

I am thankful to EPIC (Energy Production and Infrastructure Center) and UNC Charlotte for their generous support throughout my studies.

I am obligated to my lab mate, Prasanth Kumar Sahu, for endless discussions, support, and advice that aided me to focus on my work. I would also like to acknowledge my friend, Surya Prateek Sureka, for his support and editorial comments. I would like to extend my gratitude towards embedded system guides, Dr. Ehab Shoubaki, Vinayak, and Karim H. Erian.

Lastly, I appreciate support of my roommates —Monika, Nidhi, and Raka—, and would also like to thank my friends and well-wishers.

DEDICATION

This thesis is dedicated to my parents, Ravindranath Mishra and Sheela Mishra, my sister, Asha Mishra, my brother, Ritesh Mishra, my supporter, Anand Bhandary, and my friend, Gangotri Goswami.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AC Alternating Current

DC Direct Current

Gbps Gigabit per second

Hz Hertz

I2C Inter-Integrated Circuit

Kbps Kilobit per second

m meter

Mbps Megabit per second

MOSFET Metal Oxide Semiconductor field Effect Transistor

MSO Mixed Signal Oscilloscope

Photo-voltaic PV

s seconds

SPI Serial Peripheral Interface

SSCM Sorted Staircase Modulation

UART Universal Asynchronous Receiver Transmitter

W Watt

CHAPTER 1: INTRODUCTION

1.1 Overview

This chapter starts by highlighting the importance of renewable energy in section 1.2. Section 1.3 presents rise in the generation and the usage of solar power technology globally. Section 1.4 displays the motivation behind this thesis, and section 1.5 familiarizes with the organization of thesis.

1.2 Renewable Energy

In past few decades, electricity consumption comprises of an increasing share of global energy demand. Figure 1.1 shows the percentage share of renewables demand in electricity, heat, and transport sector [1]. Due to the absence of risk and disasters, renewable energy is now considered a more desirable source of fuel than nuclear power. Also, the increasing cost of fossil fuels have accelerated the interest in the growth of alternative energy resources. The concerns about environmental consequences of greenhouse gas emissions arise to need for an alternative approach. The effective solutions to this problem comprises of replacing fossil fuels with renewable energy sources as much as possible; enhancing renewable energy deployment and encouraging technological innovations [2].

A large amount of investment has been made during recent years and the advancement of technology has enabled countries to produce renewable energy more cost effectively. The International Energy Agency (IEA) expects renewable electricity generation to expand by a more than one-third by 2022, with its share increasing from 24 percent in 2016 to 33 percent in 2022. Figure 1.2 demonstrates graphically closing the gap with coal and renewables.

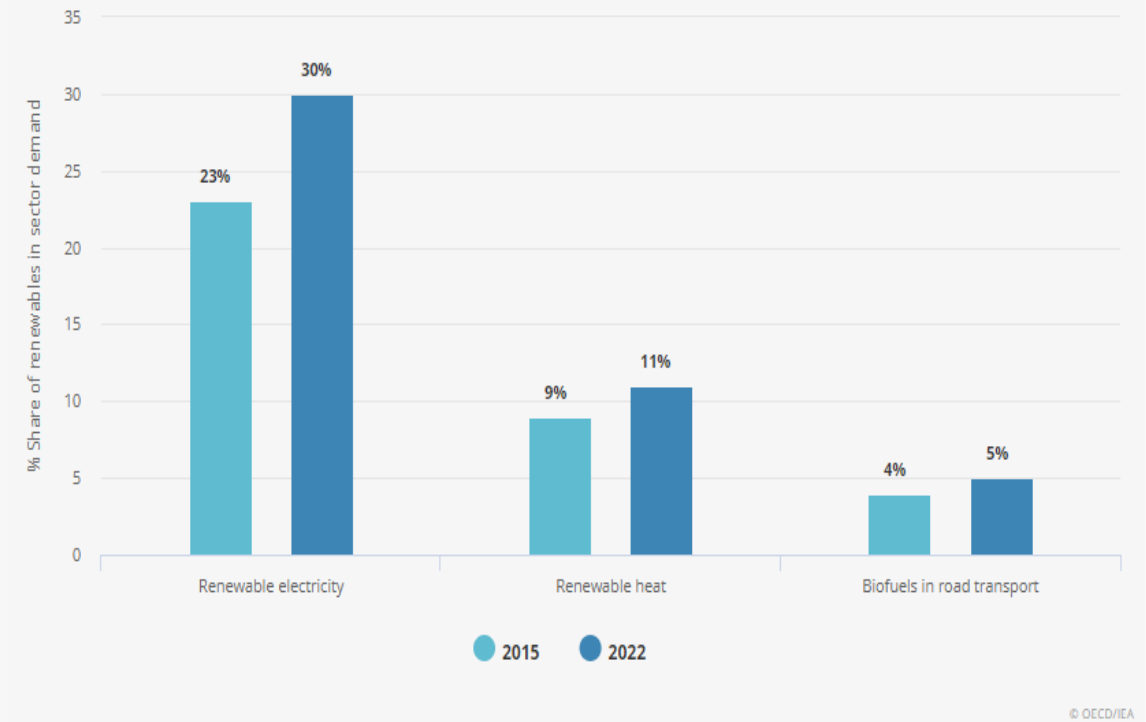


Figure 1.1: Percentile demand of renewable energy in various sector. Source [1].

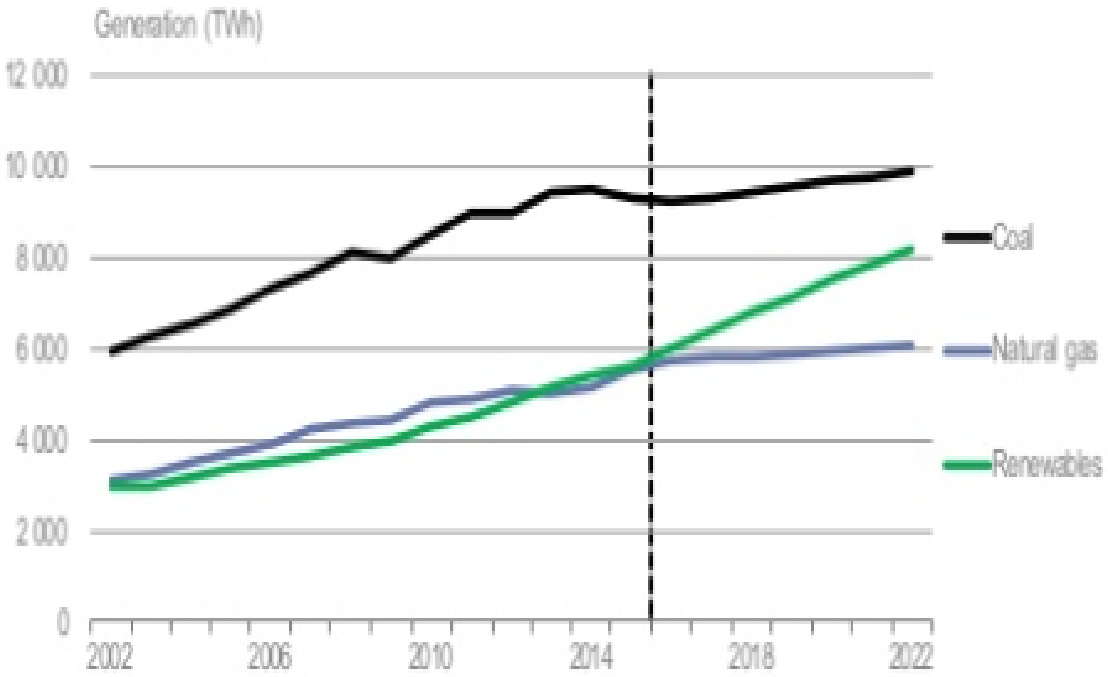


Figure 1.2: Renewable energy closing the gap with coal. Source [1].

1.3 Solar Power

The economic usefulness of solar power for residential, commercial, and industrial consumption has been investigated by researchers in multiple publications. Also, limited availability of natural primary energy sources and significance of renewable energy have encouraged industrial countries to search for alternative sources of energy such as solar power. In early 1990s, Japan started to take advantage of large-scale electricity generation by solar photo-voltaic (PV) technology, and was soon followed by Germany. Gevorkian et al. presented that the low cost power generation through solar PV technologies, increase in efficiency, and the advancement of concentrated solar power technologies in the United States has reduced the cost of electricity in the solar power industry [6]. The solar PV market has experienced remarkable growth, where the market has raised from 9,564 MW in 2007 to 69,371 MW in 2011 as displayed in figure 1.3.

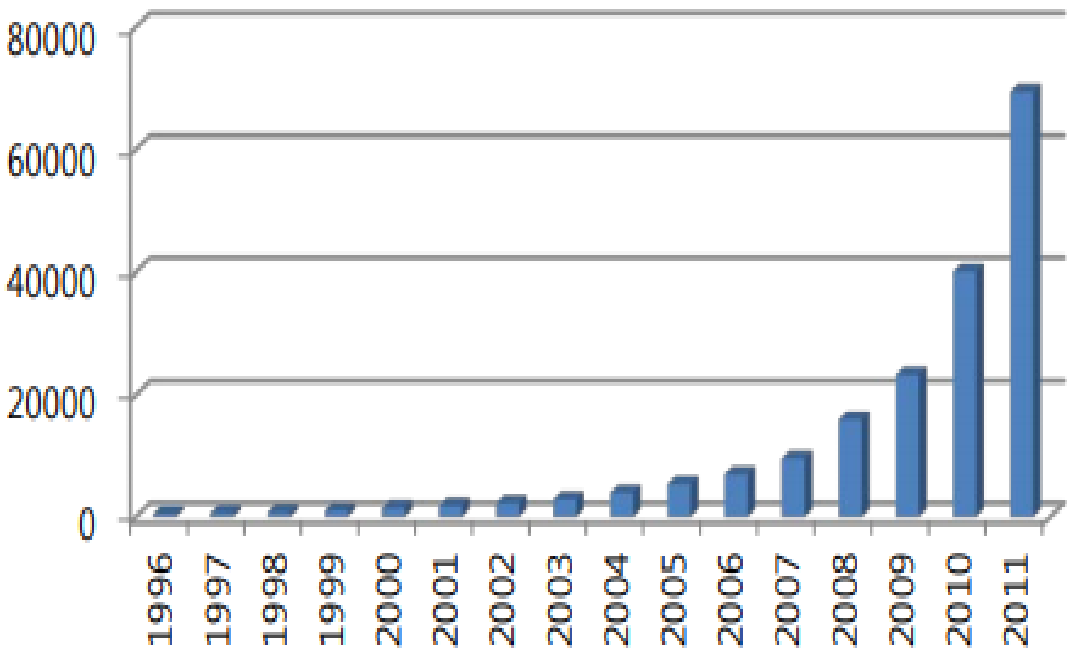


Figure 1.3: Trend in solar PV market from 1966 to 2011. Source [2].

Solar power is entering a new era, which is elevated by a strong solar PV market. Renewables accounted for almost two-thirds of global net power capacity additions, with almost 165 gigawatts (GW) was accessible in 2016 as presented in figure 1.4. Also, solar power is becoming the leader in the net capacity growth for the first time. Figure 1.5 presents the largest annual capacity additions for renewables by solar power, considerably, larger than wind and hydro [1].

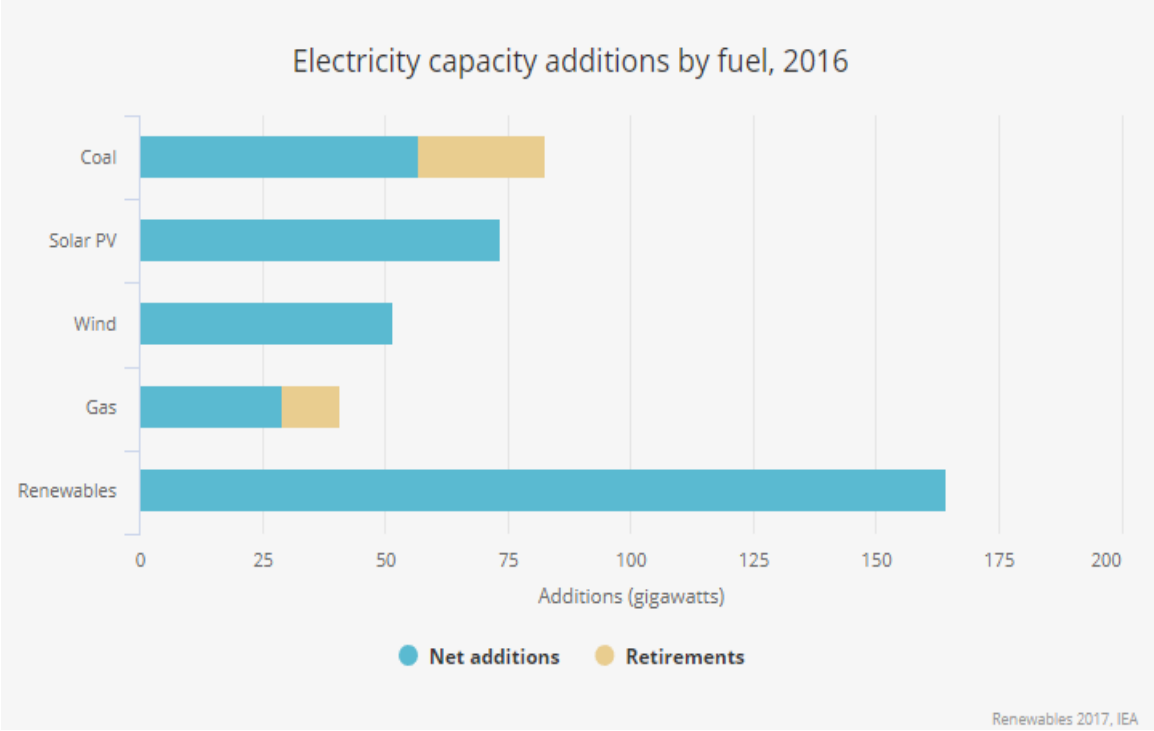


Figure 1.4: Power capacity additions and net capacity growth. Source [1]

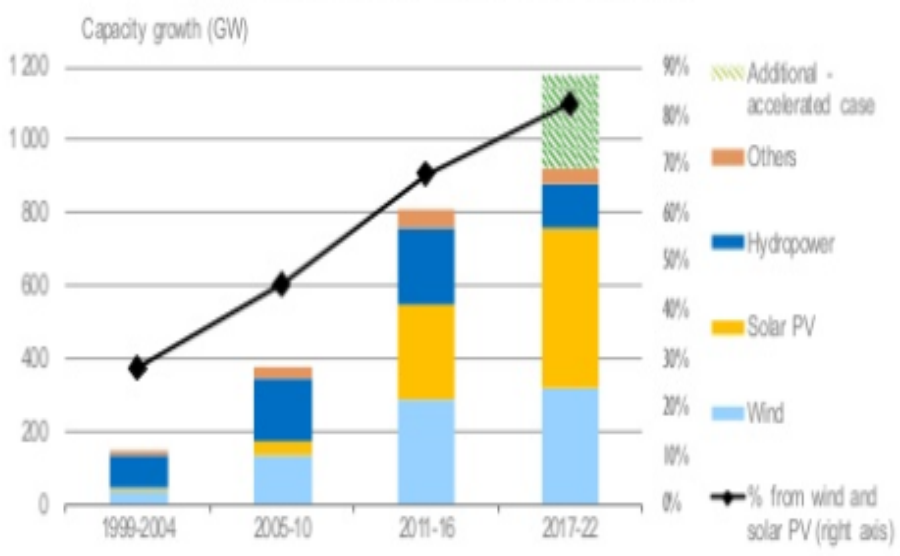


Figure 1.5: Effective growth of solar power technology in renewable electricity capacity. Source [1].

The solar PV panels, directly converts the energy from incident light into the electrical energy. In solar power generation, solar cells are employed to generate electricity. A solar cell is a p-n junction diode, when exposed to sun-light produces charge carriers. There is a flow of current when the solar cell is short circuited. The output voltage of each solar cell is approximately 0.6 to 0.7 V DC, to obtain larger DC voltages, a number of such solar cells are connected in series to form a PV module. Solar PV panels include one or more PV modules assembled together as a complete installable unit. Energy obtained from the solar PV panel serves as a low voltage DC source and has comparatively low conversion efficiency. The output power of the PV panel is DC, and as major utilization of electric power is AC. In order to enhance the efficiency and convert available low voltage DC source into required AC source, the output of the solar PV panels are connected to power converters for transformation of power from DC to AC [7].

1.4 Thesis Motivation

Power converters are required to transform DC power into usable AC power from PV panels, which can be either DC/DC converters, or DC/AC converters, or a combination of both DC/DC converters and DC/AC converters. Conventional inverter topologies such as voltage source inverter (VSI) and the current source inverter (CSI) are regularly utilized to convert generated solar electrical power into the utility grid. As these topologies require additional DC/DC converter stage, this two stage power conversion increases the circuit complexity, the cost, and the space requirements [7]. Therefore, multilevel converters acts as a reliable solution for eliminating intermediate DC-DC converters. Multi-level converters can also achieve high power using medium-power semiconductor technology making the system more cost effective [5]. This thesis investigates cascaded H-bridge Multi-level inverter topology, utilizing unique methodology that converts the conventional DC voltage output of a solar PV panel to switched quasi-square wave voltage with variable pulse width. When aggregated, realizes a superior quality multilevel waveform. Number of H-bridge power cells to be cascaded increases as the value of the AC voltage output to be synthesized increases. The rise in H-bridge power cells will make the controls more complex and clutter the circuit connections, increasing the number of wires throughout the system. Motivation of the thesis is to find a methodical approach in order to decrease the circuit connections complexity and to transmit the data required by the controllers.

1.5 Organization of Thesis

This section presents an overview of the organization of thesis -

Chapter 1 : Introduction

This chapter starts by highlighting the importance of renewable energy in section 1.2. Section 1.3 presents rise in the generation and the usage of solar power technology globally. Section 1.4 displays the motivation behind this thesis, and Section 1.5

familiarizes with the organization of thesis.

Chapter 2 : Literature Survey of Multi-Level Inverters & Communication Protocols

This chapter provides a survey of scholarly publications of various multi-level inverter topologies. In section 2.2, a review of diode clamped multi-level inverter, capacitor clamped multi-level inverter, and cascaded H-bridge multi-level inverter topologies are presented. Also, various modulation strategies are described alongwith a subsection, where comparative analysis is provided. Section 2.3 gives the brief review of various wired and wireless communication protocols.

Chapter 3 : Cascaded H-bridge Multi-Level Inverter

This chapter introduces the topology, the modulation strategy and the detailed circuit schematic of proposed cascaded H-bridge multi-level inverter (CHB-MLI). In section 3.2 topology and working principle of single H-bridge and cascaded H-bridge are presented. Section 3.3 offers detailed circuit schematic with design characteristics of each component. In Section 3.4 detailed description of sorted staircase modulation control strategy to synthesize two terminal AC output voltage is delivered.

Chapter 4 : Architecture of Distributed Controls and Communication Protocols

This chapter presents the importance of distributed controls and highlights economical benefits of distributed solution, when implemented with CHB-MLI topology. Section 4.2 gives insight of single master controller, its limitations and its necessity of distributed controls. Section 4.3 discusses various connected communication protocols namely: Universal Asynchronous Receiver Transmitter, Serial Peripheral Interface, and Inter-Integrated circuit. Simplified architectural schematic of these protocols when implemented with CHB-MLI are clearly shown with two comparisons in section 4.4. The chapter concludes with the section 4.5, where in-depth analysis on the available features of the micro-controller utilized for distributed controls are performed.

Chapter 5 : Modeling and Simulation of Cascaded H-bridge Multi-Level Inverter

This chapter describes the model of a load connected CHB-MLI companioned with PV panels developed in MATLAB/Simulink and displays performed simulation results. Section 5.2 explains a block diagram of load connected CHB-MLI with distributed controls, which is further subdivided into model of solar PV module and control strategy. In section 5.3 simulation results of load connected CHB-MLI are presented. Also, discussion for two sorting frequencies in both the case studies are exhibited.

Chapter 6 : Experimental Results

This chapter displays experimental results obtained from the laboratory prototype verifying the practical realization of CHB-MLI. In section 6.2, the description of hardware prototype developed in power electronics laboratory is provided. Section 6.3 shows operational experimental result recorded in oscilloscope for cascading and synchronizing inverter H-bridge power cells, implementation of SSCM strategy, and successfully establishing I2C communication with PIC32MX micro-controller. Further, section concludes with the recorded voltage and current waveforms obtained from prototyped CHB-MLI connected with resistive load.

Chapter 7 : Conclusion

This chapter presents the conclusions drawn from the simulation results presented in chapter 5, and experimentation performed in chapter 6. Future scope and the recommendations are also presented.

CHAPTER 2: LITERATURE SURVEY OF MULTI-LEVEL INVERTERS & COMMUNICATION PROTOCOLS

2.1 Overview

This chapter provides a survey of scholarly publications of various multi-level inverter topologies. In section 2.2, a review of diode clamped multi-level inverter, capacitor clamped multi-level inverter, and cascaded H-bridge multi-level inverter topologies are presented. Also, various modulation strategies are described alongwith a subsection, where comparative analysis is provided. Section 2.3 gives the brief review of various wired and wireless communication protocols.

2.2 Multi-level Inverter Topologies

Over the past decade, most researchers have emphasized on the use of high-power and medium voltage energy control devices. Multilevel converters, not only attain high power ratings, but also avail the advantages of renewable energy resources. Collectively, these studies outline advantages of multi-level inverter topology over traditional two-level topology, such as: the voltages across switches are half of the DC source voltage, for same switching losses switching frequency can be reduced, and reduced current harmonics. There is a large volume of published studies describing plentiful multilevel converter topologies. However, three major multi-level inverter architecture reported are known as —diode clamped inverter, capacitor clamped inverter, and cascaded H-bridge multilevel inverter— [8].

2.2.1 Diode Clamped Inverter

In 1981, Nabae, Takashi, and Akagi proposed diode clamped multi-level inverter (DC-MLI), which is also known as neutral point clamped (NPC) converter, and

worked essentially as a three-level diode clamped inverter [9]. Figure 2.1 presents the simplified circuit schematic of three-level diode clamped inverter, where leg A consist of four switches, labelled: S_1,S_2, S_3, and S_4 connected with four anti parallel diodes, labelled: D_1, D_2, D_3, and D_4, respectively. The DC side of inverter has two capacitors connected through a neutral point Z. Also, clamping diodes D_{Z1} and D_{Z2} are connected to neutral point. E is the voltage across each DC capacitor, which is normally half of the total DC voltage (V_d). Table 2.1 shows the device switching states of DC-MLI. Switching state 1 indicates switches are turned ON (close), and 0 indicates switches are turned OFF(open). For instance, when switch S_2 and switch S_3 are ON, the inverter output terminal A is connected to neutral point Z through one of the clamping diodes and produces voltage level 0 [3].

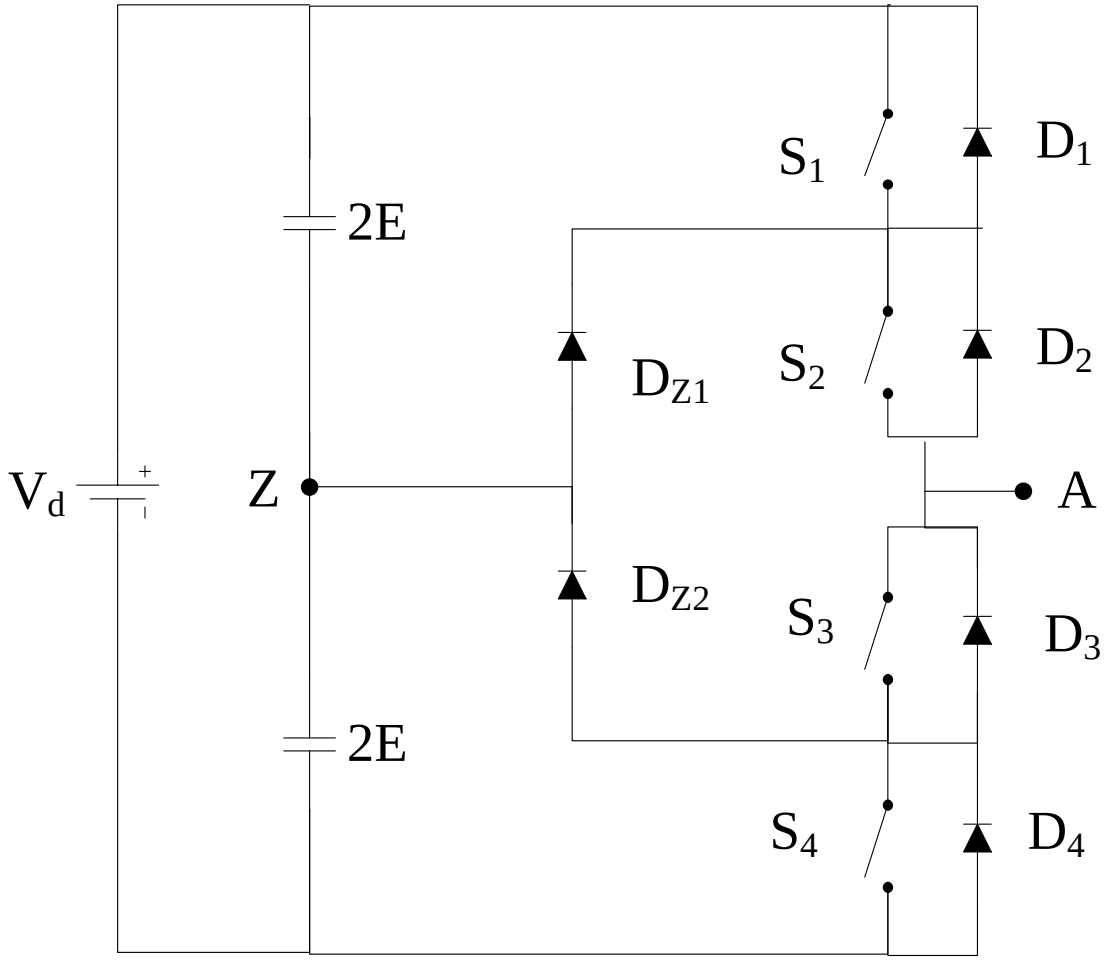


Figure 2.1: Simplified circuit schematic of three-level diode clamped inverter. Source [3].

Table 2.1: Switching states of DC-MLI in figure 2.1 generating three-level output. Source [3].

State	S_1	S_2	S_3	S_4	Inverter Voltage V_{AZ}
1	1	1	0	0	E
2	0	1	1	0	0
3	0	0	1	1	-E

Xiaoming et al. published paper proposing a new diode clamping inverter, working without series association of the clamping diodes, where the problem of distributed unequal blocking voltage is likely to be reduced by adding an auxiliary clamping network [10]. G.P. Adam et al. introduced diode-clamped inverter operating in two-level mode, facilitating voltage sharing with reduced size of DC link capacitance and developed the dwell time balancing technique, which drives the average current at DC-link node to zero [11]. Busquets-Monge et al. examined a control and pulse-width modulation technique, where set of solar PV arrays are connected to conventional diode clamped inverter, which is capable of controlling operating voltage of each array. Thereby, extracts maximum power, reduces distortion in output voltage, and increases the system efficiency [12]. In this paper, various strategies named as —total balancing strategy, commutation strategy, and minimum-commutation strategy— are investigated by M. Marchesoni et al, achieving capacitor voltages balance with multi point clamped topologies [13]. A. Nami et al. have conducted comparative study on two different arrangements (asymmetrical and symmetrical) of a four-level diode clamped inverter, and reported that asymmetric arrangement aids in getting more levels at output voltage and reducing the harmonic content [14].

2.2.2 Capacitor Clamped Inverter

In 1992, T. A. Meynard and H. Foch. has introduced capacitor clamped inverter, as an alternative topology to DC-MLI, also known as flying capacitor multi-level inverter (FC-MLI) [15]. Figure 2.2 shows a simplified circuit schematic of a five-level FC-MLI. The inverter leg have three flying capacitors with voltages E, 2E, and 3E, respectively (E is one fourth of the DC bus voltage). There are four complementary pair of switches: (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4'). Thereby, limits the number of gate signals requirement to four, for eight switches. Table 2.2 shows operating states of switches and voltage levels of FC-MLI. For example, at switching state 2, when switches S_1, S_2, and S_3 conduct, voltage at inverter output terminal(A) with respect

to the neutral point (Z) is E [3].

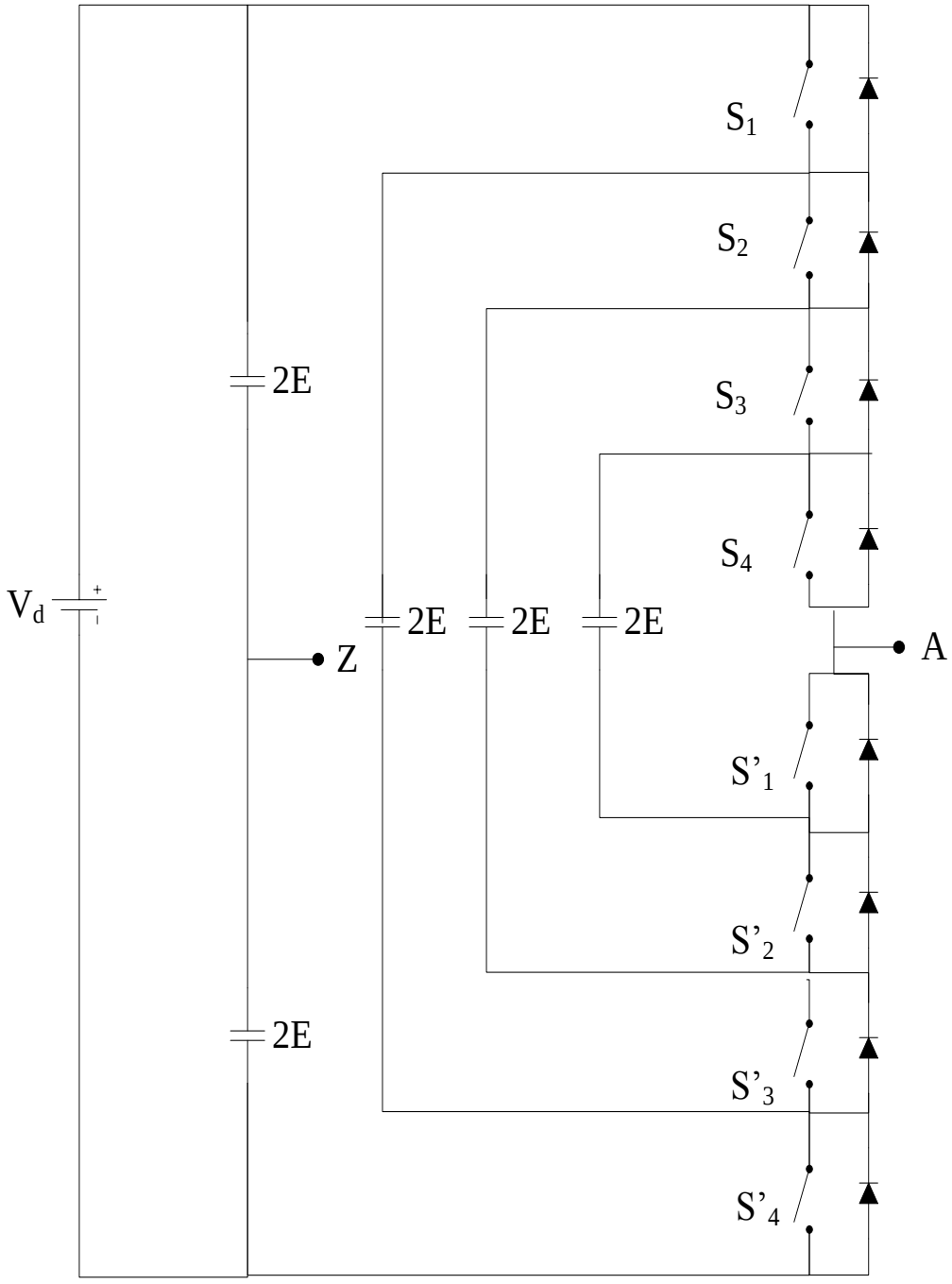


Figure 2.2: Simplified circuit schematic of flying capacitor multi-level inverter. Source [3].

Table 2.2: Switching states of FC-MLI in figure 2.2 generating five-level output. Source [3].

State	S_{11}	S_{13}	S_{21}	S_{23}	Inverter Voltage V_{AZ}
1	1	1	1	1	2E
2	1	1	1	0	E
3	0	1	1	1	E
4	1	0	1	1	E
5	1	1	0	1	E
6	1	1	0	0	0
7	0	0	1	1	0
8	1	0	0	1	0
9	0	1	1	0	0
10	1	0	1	0	0
11	0	1	0	1	0
12	1	0	0	0	-E
13	0	1	0	0	-E
14	0	0	1	0	-E
15	0	0	0	1	-E
16	0	0	0	0	-2E

Ren Lin et al. proposed three-level PWM control scheme for capacitor clamped configuration, reducing the AC side voltage harmonics and voltage stress of power semiconductor[16]. M. F. Escalante et al. introduced direct torque control (DTC) strategy, which maintains the flying capacitors voltage, and also provides the voltage levels required by control loop. Thereby, drawing attention to the advantages of using flying capacitor multi-level topology and DTC strategy, such as, flux and torque

quality improvement [17]. Kang et al. presents a modification in carrier redistribution pulse width modulation (CRPWM) technique, to overcome the drawback of the strategy at the transition of voltage level [18]. Anshuman Shukla et al. developed a time based approach, controlling the capacitor voltage, and maintaining the current profile with the help of multi-level hysteresis current regulation technique [19]. Jing Huang et al. proposed two joint-phase redundant state selection algorithms, demonstrating flying capacitor inverter that typically operates in the four-level mode can be extended to five-level operation, and three-cell inverter can achieve eight-level operation for applications involving reactive power compensation [20]. Sang-Gil Lee et al. investigated major problem, i.e., unbalance of capacitor voltage of flying capacitor multi-level inverters and proposed a new solution using a carrier based PWM method [21].

2.2.3 Cascaded Multilevel Inverter

In high-power medium voltage drives, cascaded H-bridge multi-level inverter (CHB-MLI) is one of the most popular topologies among converters. CHB-MLI is configured by connecting multiple units of single phase H-bridge power cell in series through their AC terminal. Simplified circuit diagram of three-, five-, and seven-level CHB-MLI are presented in chapter 3. Also, the operating stages of switches in three- and five-level inverter are shown in tabular form.

Malinowski et al. performed a survey of different topologies, control strategies, and modulation techniques utilized by cascaded multi-level inverters, including discussion on regenerative and advanced topologies [22]. Ebrahim et al. introduced a new configuration of cascaded multilevel inverter, with fewer switches and gate driver circuits, reducing installation area and cost [23]. Mohammad Farhadi et al. have performed analysis for symmetric and asymmetric conditions on proposed sub-multilevel inverter topology [24]. Pablo Lezana et al. demonstrated a configuration with single phase active rectifier at input and H-bridge inverter at the output, eliminates

low frequency input current harmonics effectively, and functions without difficulties in regenerative mode [25]. Sung G. Song et al. proposed a circuit configuration comprising of isolated cascaded multilevel inverter, low-frequency three-phase transformers, and a single DC input power source, with a control strategy that reduces harmonic components of the output voltage and switching losses considerably [26].

Prasanth Kumar Sahu et al. performed analysis on multiple parameters in this paper, implementing multiple control strategies on a topology identical to cascaded H-bridge multilevel inverter termed as solar panel companion inverter(SPCI) [4]. Detailed descriptions of various control strategies such as: unsorted pulse width modulation (UPWM), sorted stair case modulation (SSCM), and sorted pulse width modulation (SPWM) are provided. Figure 2.4 , figure 2.5, and figure 2.3 shows the flow chart diagram of UPWM, SSCM, and SSCM, respectively, for six SPCI modules generating thirteen-level voltage output. In UPWM, a comparison is made between sinusoidal reference wave and a high frequency carrier wave, and a pulse width modulated alternating voltage is produced. In SSCM strategy, quasi square wave sinusoidal AC voltage is synthesized through generating staircase output from each SPCI module, here the voltages are sorted in descending order. SPWM is a combination of both SSCM and UPWM strategies.

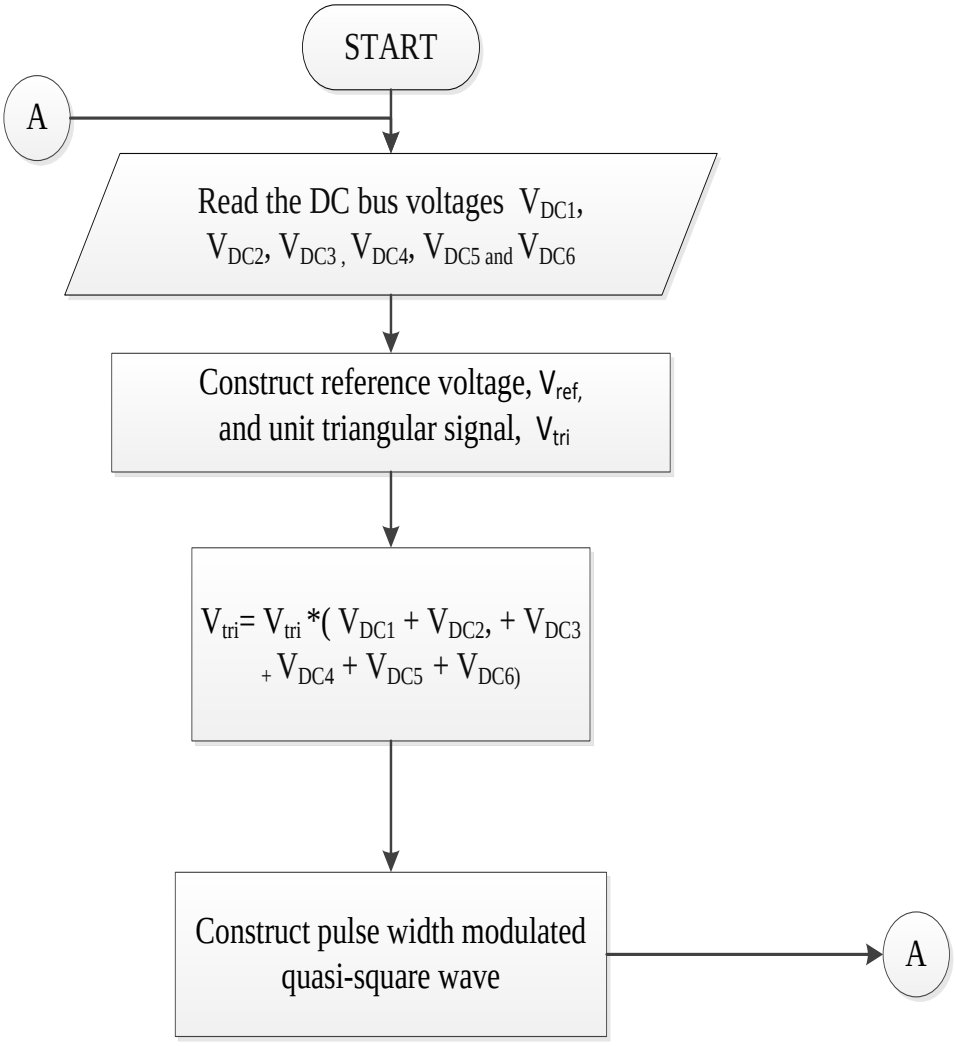


Figure 2.3: Flowchart representation implementing unsorted pulse width modulation. Source [4].

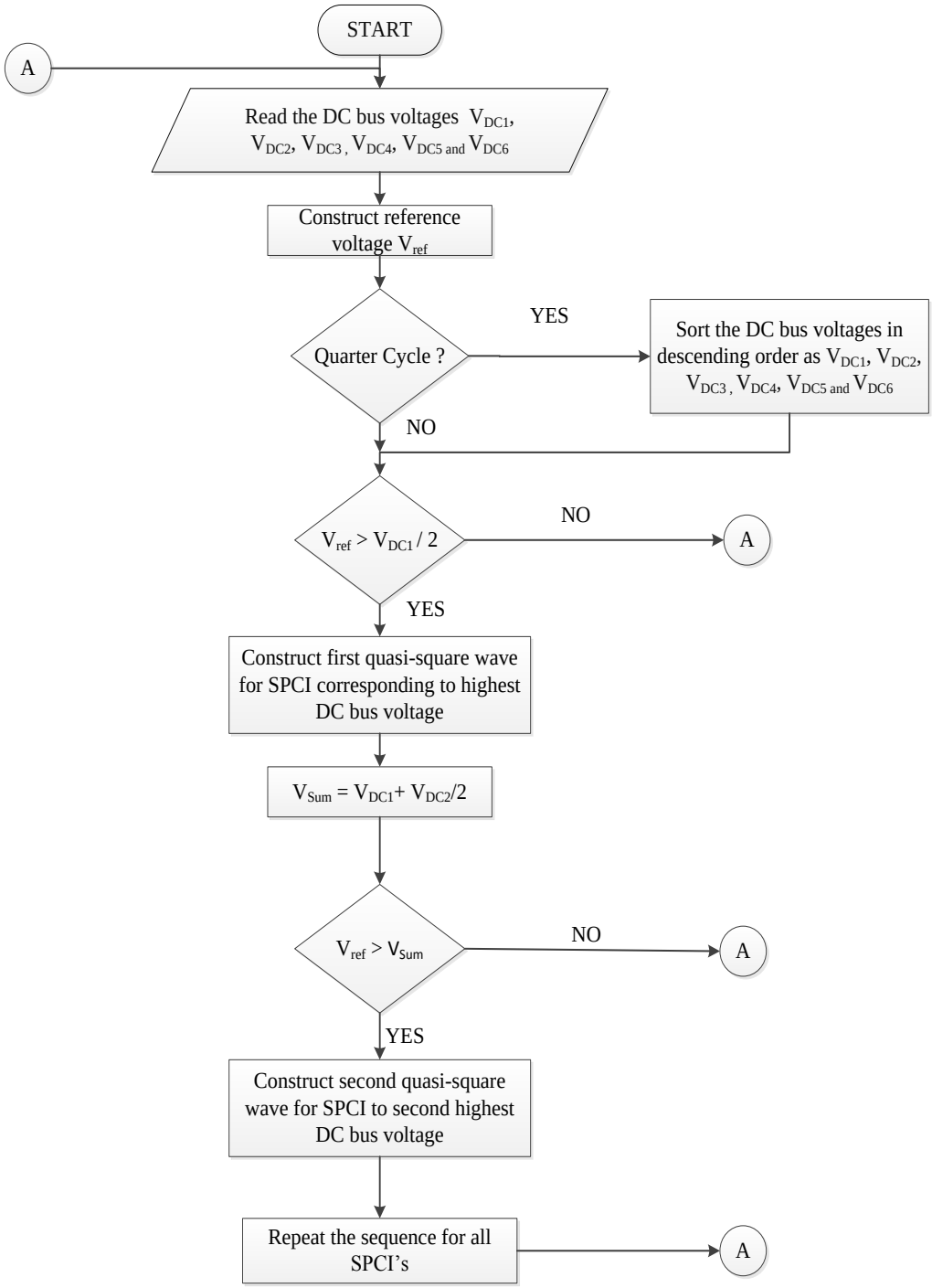


Figure 2.4: Flowchart representation implementing sorted stair case modulation. Source [4].

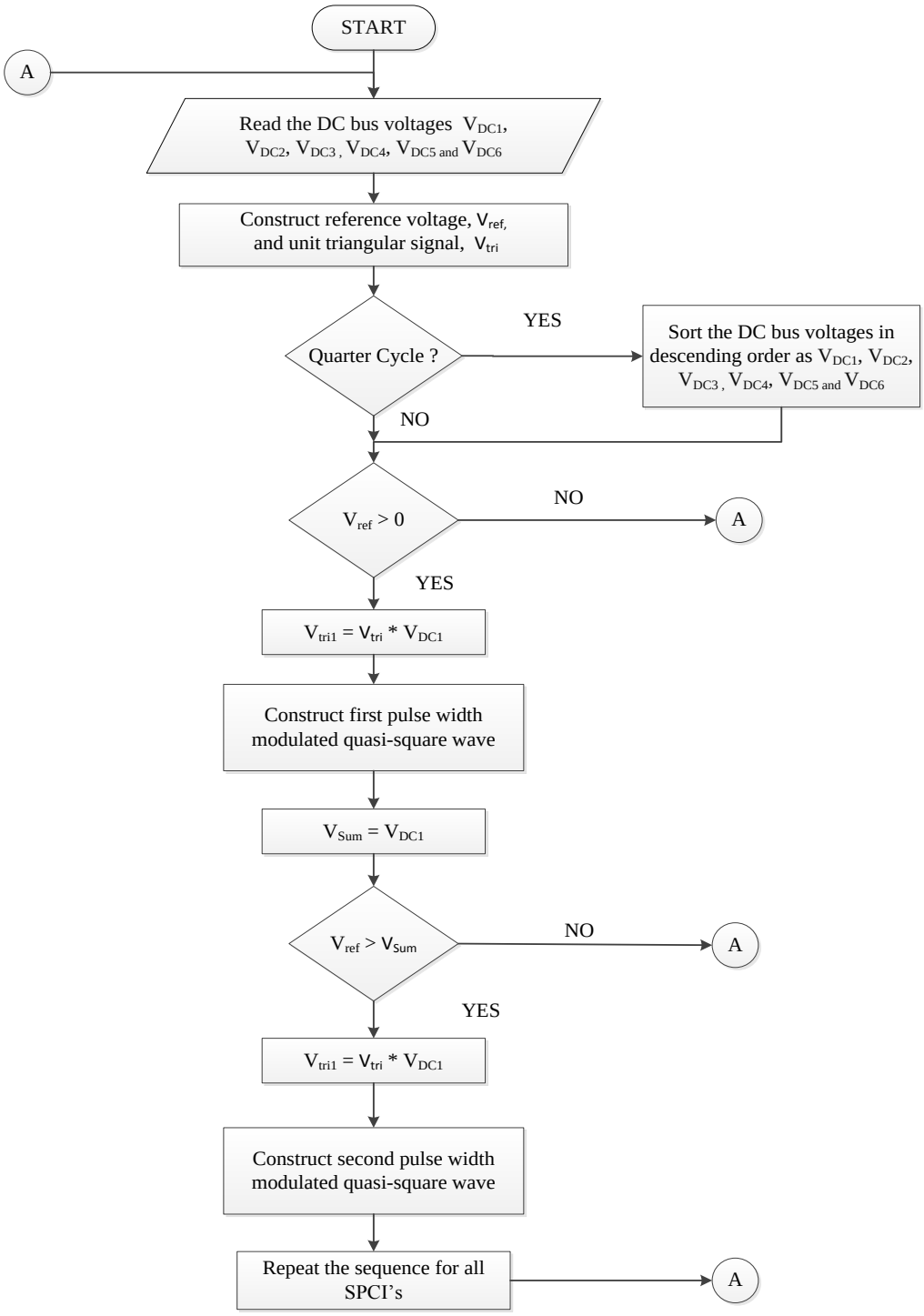


Figure 2.5: Flowchart representation implementing sorted pulse width modulation. Source [4].

2.2.4 Modulation and Control Methods

Over the last decade, multilevel converter modulation and control methods have drawn much research and development attention. Franquelo et. al. [5], performed a very useful survey about multi-level inverters, classification, and multiple control strategies. A classification of the modulation methods for multilevel inverters is presented in figure2.6. The modulation algorithms are divided into two main groups: the state-space vector based algorithm and voltage level based algorithm.The different methods are labelled with colors green, yellow, and red, relative to the switching frequencies low, mixed, and high, respectively. Space Vector based algorithms are subdivided into two techniques: space vector modulation (SVM) and space vector control (SVC). Voltage level algorithms are subdivided into four techniques: hybrid modulation (HM), selective harmonic elimination (SHE), nearest level control(NLC), and multi-carrier pulse width modulation (MC-PWM). MC- PWM is further classified into level shifted pulse width modulation (LS-PWM) and phase shifted pulse width modulation (PS-PWM)

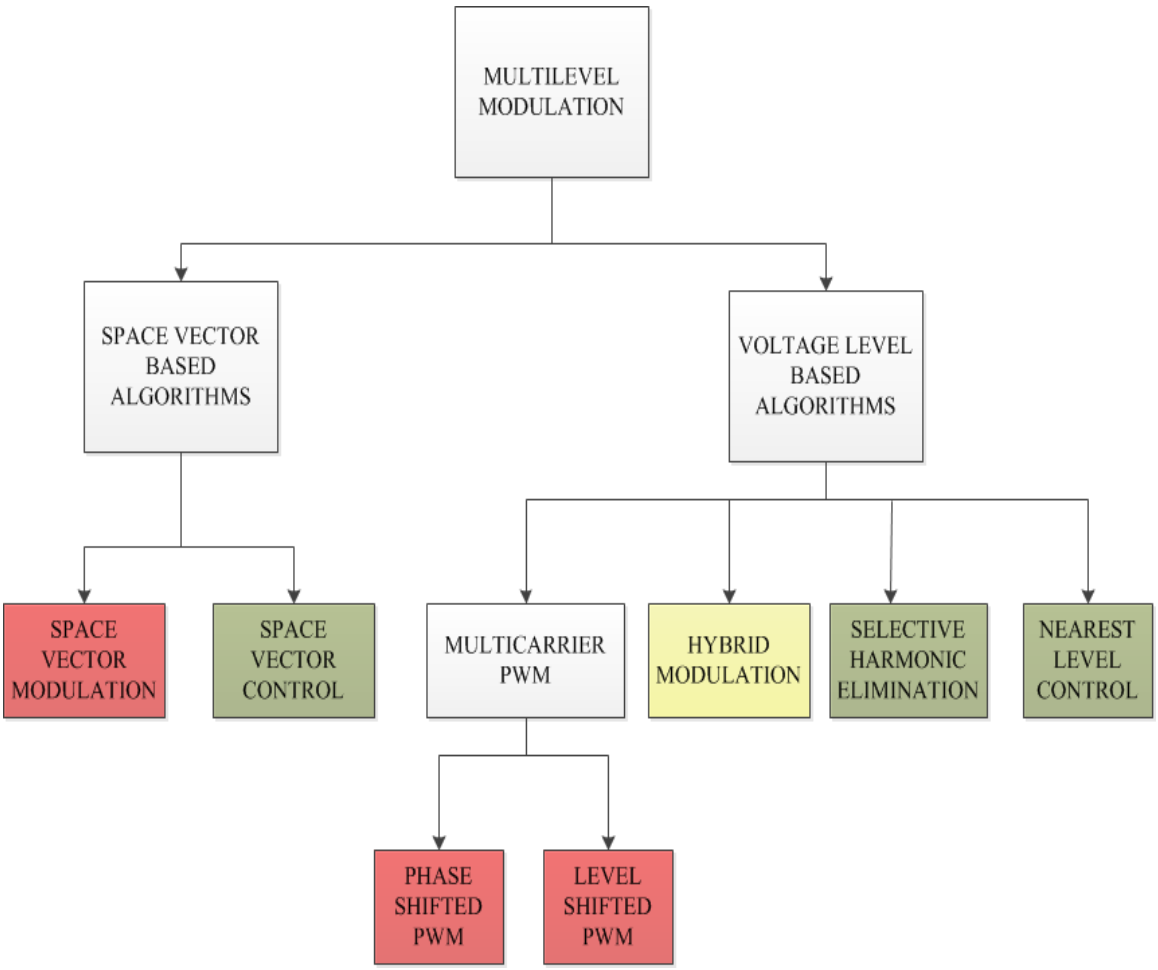


Figure 2.6: Block diagram representation of modulation strategies for multi-level inverters. Source [5].

SVM is a method, where the reference voltage is indicated as a reference vector to be constructed by the power converter. It constructs the voltage reference vector as a linear combination of the state vectors, acquiring an averaged output voltage equal to the reference over one switching period. SVC acquires benefit of the high number of voltage vectors generated by a converter with a high number of levels. It approximates the reference to the closest generable vector and functions in a natural fundamental switching frequency with reduced switching losses.

HM is in part a PWM-based technique, specially designed for the CHB with unequal DC sources. The general idea is to take advantage of the different rated power among the modules of the converters, controlling the high-power modules at a fundamental

switching frequency. Whereas, the low-power cell is being controlled using unipolar PWM. SHE method has been extended to the multilevel scenarios for high-power applications. Its algorithms are limited to open loop or low-bandwidth applications. The switching angles are computed offline and stored in tables, which are then inserted according to the operating conditions. NLC works on the same principle as SVC; here, the closest voltage level that can be generated by the inverter is considered instead of the closest vector. In PS-PWM, carriers can be arranged with shifts in phase, which assists in generating the stepped multilevel output waveform with low distortion phase. Whereas in LS-PWM, carriers can be arranged with shifts in amplitude, relating each carrier with each possible output voltage level generated by the inverter.

2.2.5 Comparison of Multi-level Inverter

Table 2.3 provides the comparison of multi-level inverter topologies depending on the implementation factors.All of the modulation schemes mentioned in previous subsection are not suitable for each topology; additionally, some algorithms are not applicable to some converters.

Table 2.3: Comparison of multi-level inverter topologies depending on implementation factors.

Factors	DC-MLI	FC-MLI	CHB-MLI
Distinct requirements	Clamping diodes	Additional capacitors	Isolated DC sources
Modularity	Low	High	High
Design complexity	Low	High (Capacitors)	High (input transformer)
Control concerns	Voltage balancing	Voltage setup	Power sharing
Fault tolerance	Difficult	Easy	Easy

Table 2.4 provides summary of the compatibility between the modulation techniques and the multilevel topologies, where $\surd$ denotes applicable and recommended, X denotes not applicable, and $\sim$ denotes applicable but not recommended.

Table 2.4: Compatibility between the modulation techniques and the multilevel topologies.

Modulation Methods	DC-MLI	FC-MLI	CHB-MLI
SVM	$\surd$	$\surd$	$\surd$
SVC	$\sim$	$\surd$	$\surd$
HM	X	X	$\surd$
SHE	$\surd$	$\surd$	$\surd$
NLC	$\sim$	$\surd$	$\surd$
LS-PWM	$\surd$	$\surd$	$\sim$
PS-PWM	X	$\surd$	$\surd$

2.3 Communication Protocols

Single master controller produces a great stress on control requirements. The number of required analog-to-digital converters and pulse generation peripherals increases as the number of voltages required to be sensed for controls and switches need to be operated increases. Therefore, study of distributed controls and communication methods is demanded; henceforth, communication protocols are investigated in this section.

2.3.1 Wired Communication Protocols

2.3.1.1 Controller Area Network

Controller Area Network (CAN) bus is a serial bus protocol designed to allow micro-controllers and devices to communicate with each other. It is a message based protocol, devised originally for multiplex electrical wiring within automobiles to save

on copper. CAN is a multi-master serial bus protocol utilized for connecting Electronic Control Units (ECUs), also recognized as nodes. CAN network requires two or more nodes for communication. All nodes are connected to each other through a two-wire bus. The wires are twisted pair with 120 Ω impedance. Each node requires:

1. Central processing unit, microprocessor, or host processor: It determines meaning of received messages and messages it needs to transmit. Sensors, actuators and control devices can be connected to the host processor.

2. CAN controller: CAN controller stores the received data bits from the bus until complete message is arrived, which can be retrieved later by microprocessor. Further CAN controller transmits the bits of the messages (received from the microprocessor) serially on the bus, as the bus becomes free.

3. CAN transceiver: CAN transceiver has two functionalities —receiving and transmitting—. While receiving, it converts the stream of data from CAN bus levels to levels that the CAN controller operates, and while transmitting, it converts the data stream from the CAN controller to CAN bus levels. CAN transceiver usually includes protective circuitry to protect the CAN controller.

A.A.Salunkhe et al. implemented CAN bus protocol using Raspberry Pi for accessing internal ECU parameters and established controls connecting two or modes node from remote place [27]. Xiaoming Li et al. proposed a CAN-BUS communication module, which can be utilized as an interface by embedded system. This module ease the communication in CAN networks by receiving and sending data through pipes, making the communication easier and more efficient [28]. Kristian et al. examined CAN bus multi-master design protocol for research applications purpose on hybrid electric vehicle using arm micro-controller. This research concludes that CAN bus automatically decrease the number of line on system, it can be built from serial UART, and synchronize data and transmute the data level to CAN + and CAN - mode [29].

Shuqing Guo performed comparative analysis on traditional vehicle circuit and CAN-bus circuit, concluding CAN-bus not only improves reliability but also reduces the cost and car failure rate [30].

2.3.1.2 Universal Serial Bus

Universal Serial Bus (USB) is an ordinary interface that allows communication between devices and a host controller. It is used to connect multiple peripheral devices. For example, printer and scanners to external hard drives and flash drives. Its wide variety of application and support for electrical power assists USB in replacing a wide range of interfaces, like, parallel and serial port. USB is designed to advance plug-and-play and enable hot swapping. Plug-and-play permits the operating system (OS) to extemporaneously configure and detect a new peripheral device without having to restart the system, and hot swapping authorizes ejection and replacement of a new peripheral without having to reboot the system. The major USB standards are: USB 3.1, USB 3.0, USB2.0, and USB 1.1.

The speed description are as follow:

- USB 3.1: USB 3.1 compliant devices are able to transfer data at speed of 10 Gbps (10,240 Mbps)
- USB 3.0: USB 3.0 compliant devices are able to transfer data at speed of 5 Gbps (5,120 Mbps)
- USB 2.0: USB 2.0 compliant devices are able to transfer data at speed of 480 Mbps
- USB 1.1: USB 1.1 compliant devices are able to transfer data at speed of 12 Mbps.

Daniel Noyes et al. analyzed the USB protocol concerning vulnerabilities and developed a holistic approach to secure USB protocol. Thereby, including the encryption

as well as authentication of data on the USB line[31]. USB communication has become the most popular tool for storing digital data in external storage devices. In the paper, Suratose et al. propose a two-factor authentication technique in order to solve problems, like, unavailability of built-in function to authenticate user, as well as limiting the software usage such that users can run it inside that assigned device only [32].Table 2.5 presents the comparison of CAN and USB communication protocols.

Table 2.5: Comparison of CAN bus and USB protocol.

Attributes	CAN	USB
Data rate	50 kb/s to 1 Mb/s	1.5 Mb/s to 10 Gb/s
Nominal range	40-1000 m	2-5 m
Number of devices	112	127
Advantages	High data transfer rate for small number of nodes	High data transfer rate depending on the mode used
Disadvantages	Wired, transfer varies with the size of network, and used to transfer small amount of data	wired and short range of length

2.3.1.3 Universal Asynchronous Receiver Transmitter

Universal asynchronous receiver transmitter(UART) allows two device to communicate with each other. The data format and transmission speeds are configurable. It uses two lines for communication of data: Tx for sending the data and Rx for receiving the data. Ground of two devices should be made common. UART takes

byte of data while transmitting, it send data bit by bit and at receiving end all bits are assembled into complete byte.

2.3.1.4 Serial Peripheral Interface

Serial Peripheral Interface(SPI) is a synchronous serial communication interface and runs on master-slave architecture with single master. It works in full-duplex mode; i.e., both master and slave can transmit data simultaneously. SPI works on four lines, also known as four wire serial bus.

2.3.1.5 Inter-Integrated Circuit

Inter-Integrated Circuit stands for I2C and can be pronounced "I squared C". This communication protocol requires two data bus lines: a serial clock line (SCL) and a serial data line(SDA). These data bus lines are bi-directional, and this configuration requires external pull up resistor. SCL contains clock signal and clock signal is always generated by the master. Peripheral address and all the data are transferred by SDA

2.3.2 Wireless Communication Protocols

2.3.2.1 Bluetooth

Bluetooth is an approach for data communication that uses short-range radio waves, replacing cords between computers and their connected units. Bluetooth shows substantial advantages for wireless network operators, end workers, and content developers of new applications. It was invented by telecom vendor Ericsson in 1994. It is a wireless technology utilized for data transfer over short distances, using ultra high frequency (UHF) radio waves in the industrial, scientific, and medical (ISM) radio band (from 2.400 to 2.485 GHz).

Shih-Jie Chou et al. presented that using Bluetooth low energy sensors to perform signal strength fingerprinting identification can increase the accuracy of positioning.This study, also incorporates an IPS design, and introduces an indoor positioning algorithm that calculates location-based information to achieve effective indoor po-

sitioning [33]. K.S. Savita discusses about bluetooth drawer lock system solution using Bluetooth technology, which assists the students for safe keeping their valuable items. The system functions on bluetooth activation function, and lock and unlock commands are communicated over bluetooth devices using Arduino UNO and Android studio [34]. Ali Nikoukar et al. addresses the effect of environment and interference on noise floor and signal propagation, and presents a model, which can be used in simulation tools for modeling Bluetooth low energy applications [35].

2.3.2.2 Wi-Fi

It is a wireless technology for local area networking. Devices based on the IEEE 802.11 standards operates with this wireless technology. Wi-Fi compatible devices can connect to Internet through a WLAN network and a wireless access point. Such access points have a range of about 20 meters indoors and a greater range outdoors. Coverage distance can be as small as a single room with walls that block radio waves, or as large as many square kilometers attained by using multiple overlapping access points [36]. A device sending information cordlessly to another device, both connected to the local network without any physical connections, such devices are more vulnerable to attack than wired connections. Haishen Peng performed analysis in terms of user access and data transmission security for Wi-Fi networks, and proposed measures to resolve Wi-Fi network security threat by creating series of security programs —basic security configuration Program, intermediate security configuration Program, and advanced security configuration program— [37]. Leeuwen et al. understands the rise in usage of wireless networking and communications leads to demand of advanced protocols with high data throughput. Issues related to security of data transported, research about several emulation tools, and custom extensions that enable an analysis platform to perform cyber security analysis of lower-layer wireless networks are presented in this paper [38].

2.3.2.3 Zigbee

Zigbee is an IEEE 802.15.4-based specification for a set of high-level communication protocols. It is employed to create personal area networks with small and low-power digital radios, such as, for home automation, medical device data collection, and other low-power low-bandwidth needs. Also, serves small scale projects which need cordless connection. The technology determined with ZigBee is intended to be simpler and economical in comparison with other wireless personal area networks (WPANs), like: Bluetooth or Wi-Fi. It has wide variety of applications and has low power consumption.

Transmission distance is limited to 10-100 meters line-of-sight, depending on power output and environmental characteristics. ZigBee devices can transmit data over long distances, through passing data, by forming a mesh network of intermediate devices to reach more distant ones. ZigBee is ordinarily used in low data rate applications that require long battery life and safe networking. ZigBee has a data transfer rate of 250 kbit/s, best fit for intermittent data transmissions from a sensor or input device.

Ramya et al. presents a detailed review of Zigbee protocol, types of device, the protocol stack architecture and its applications [39]. Qi Xia et al. proposed routing algorithms and networking based on ZigBee wireless meter reading system. Further, in-depth discussion on the problems and improvement of, for the ZigBee standard in the meter reading system are performed [40]

Table 2.6 presents the comparison of wireless communication protocols

Table 2.6: Comparison of wireless communication protocols

Attributes	Bluetooth	Wi-Fi	Zigbee
Data rate	1 Mb/s	600 Mb/s	250kb/s
Frequency	2400 MHz	2400 MHz, 5000 MHz	2400 MHz
Nominal range	10 m	100 m	10-100 m
Channel Bandwidth	1 MHz	22 MHz	0.3/0.6 MHz, 2 MHz
Number of devices	8	2000	65000+
Advantages	wireless, simple	wireless, long range, and high data transfer rate	wireless and fixed data rate set initially
Disadvantages	short range, limited number of devices	Energy inefficient	low data transfer rate

CHAPTER 3: CASCADED H-BRIDGE MULTI-LEVEL INVERTER

3.1 Overview

This chapter introduces the topology, the modulation strategy and the detailed circuit schematic of proposed cascaded H-bridge multi-level inverter (CHB-MLI). In section 3.2 topology and working principle of single H-bridge and cascaded H-bridge are presented. Section 3.3 offers detailed circuit schematic with design characteristics of each component. In Section 3.4 detailed description of sorted staircase modulation control strategy to synthesize two terminal AC output voltage is delivered.

3.2 Cascaded Multi-Level Inverter Topology

This section deals with schematic drawing of single H-bridge power cell, cascaded H-bridge power cells, operation of switches in tabular form, and inverter output obtained from simulations performed in MATLAB/Simulink.

3.2.1 Single H-bridge inverter

A single H-bridge (SHB) inverter consist of two legs. Each leg incorporates two switches, preferably metal oxide semiconductor field effect transistor (MOSFET). These switches are labeled as S_{11}, S_{12}, S_{13} and S_{14}. Each H-bridge can be powered from DC source or companioned with photo-voltaic (PV) panel itself. When PV panel is used as a source of power supply, DC-link capacitor will also be connected with the panel. A micro-controller is needed to synthesize AC output from this inverter by operating the switches in appropriate sequence. The connection of single H-bridge inverter powered with DC source at voltage (V_{DC}) can be seen in figure 3.1, where synthesized inverter output voltage (V_{out}) is measured across a rectangular load block connected between two legs forming the H-bridge.

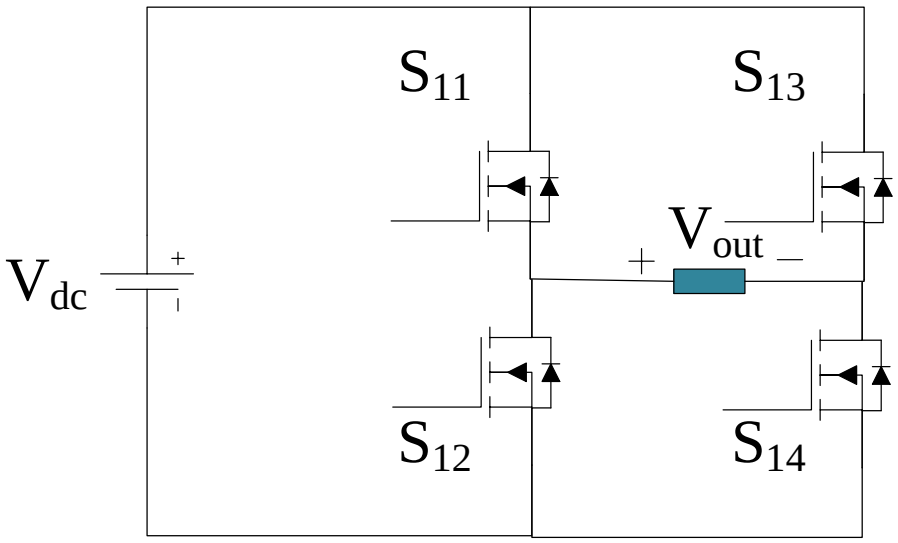
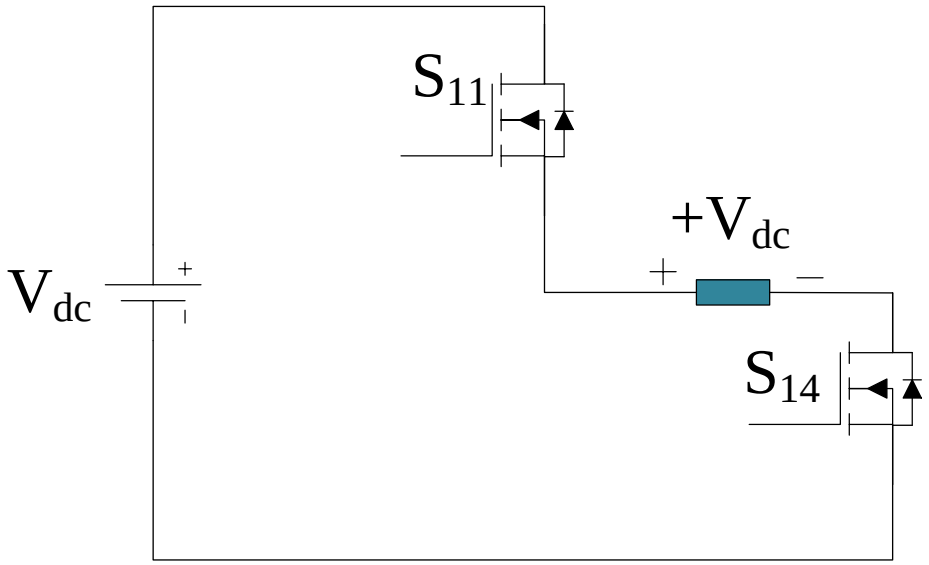
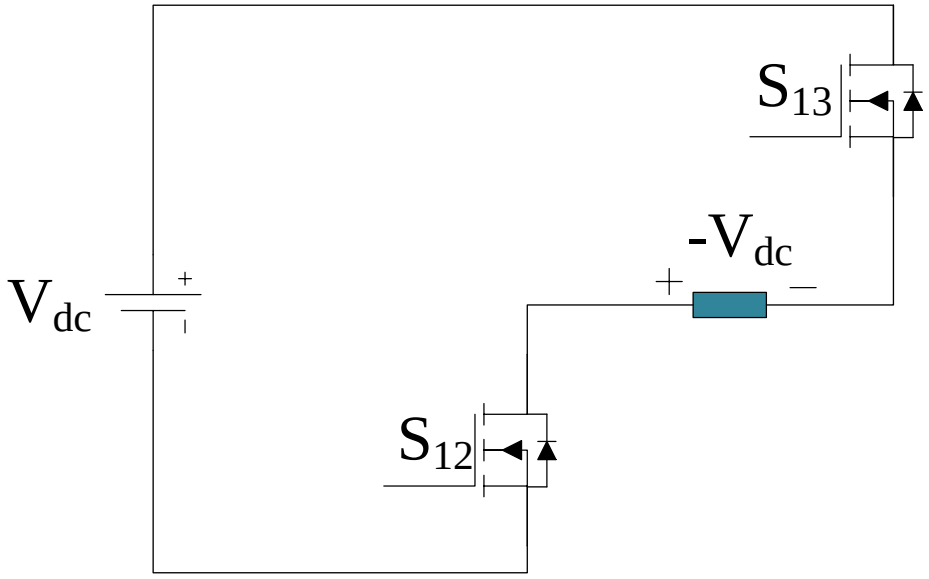


Figure 3.1: Simplified diagram of single H-bridge inverter.

In figure 3.2 equivalent circuit of voltage output at different switching combination are displayed. figure 3.2 (a), (b), (c) and (d) illustrate the combination of operating switches producing three different levels of voltage output $+V_{dc}$, $-V_{dc}$ and 0.

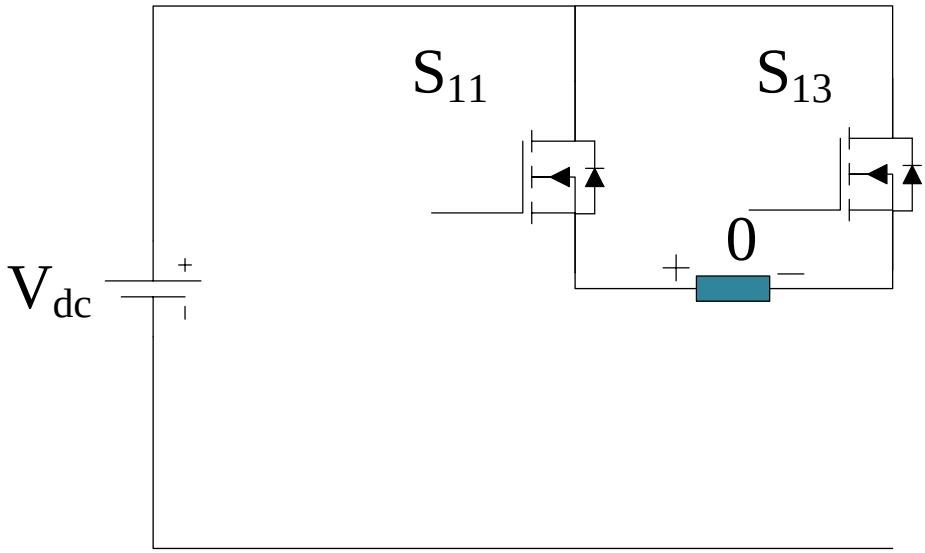


(a) Switch S_{11} and Switch S_{14} closed.

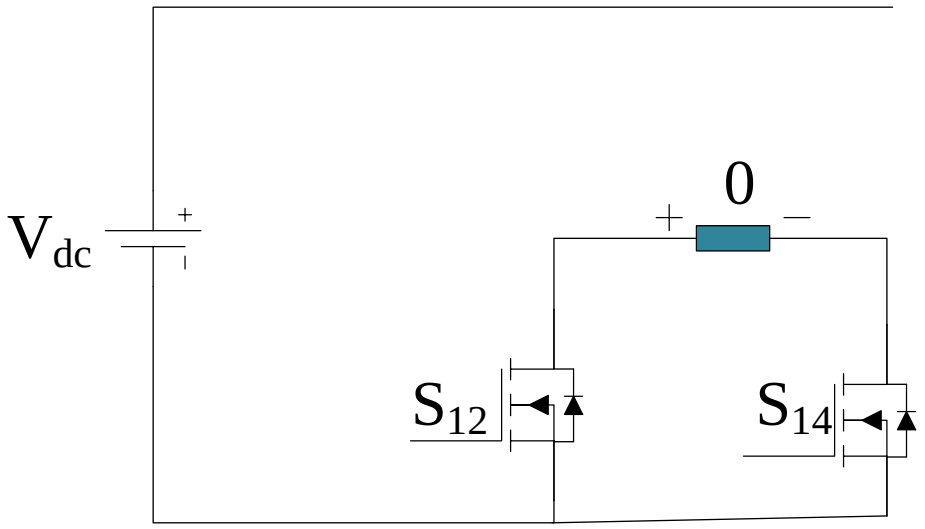


(b) Switch S_{12} and Switch S_{13} closed.

Figure 3.2: Equivalent circuits for different combination of operating switches to produce $+V_{dc}$, $-V_{dc}$ and 0 levels of output in single H-bridge inverter.



(c) Switch S_{11} and Switch S_{13} closed.



(d) Switch S_{12} and Switch S_{14} closed.

Figure 3.2: Equivalent circuits for different combination of operating switches to produce $+V_{dc}$, $-V_{dc}$ and 0 levels of output in single H-bridge inverter (contd.).

It is appropriate to begin the analysis of cascaded topology with two levels. Note that at this point switches in same leg should not be closed at the same time, i.e.

S_{11} and S_{12} cannot be closed simultaneously nor can S_{13} and S_{14}. Otherwise, a short circuit would occur across the source. In order to decrease the complexity of tables, for the operating condition of switches it is assumed that $S_{12} = \overline{S_{11}}$ and $S_{14} = \overline{S_{13}}$; i.e., when S_{11} is closed S_{12} will be open and when S_{13} is closed S_{14} will be open and vice versa. Additionally, in all tables 0 indicates the switch is open and 1 indicates the switch is closed.

Figure 3.3 displays simulation of SHB inverter performed to generate two-level output. In the legend the voltage output, signal of S_{11} and signal of S_{13} are indicated by green, blue, and red colors, respectively. Table 3.1 presents operating states of switches and voltage levels for two different switching states. Examine figure 3.3 and table 3.1, where operating states of figure and table shows that, state 1: V_{out} is $-V_{DC}$ and state 2: V_{out} is $+V_{DC}$. State 2 represents the equivalent switching operation of figure 3.2 (a) whereas state 1 illustrates figure 3.2 (b).

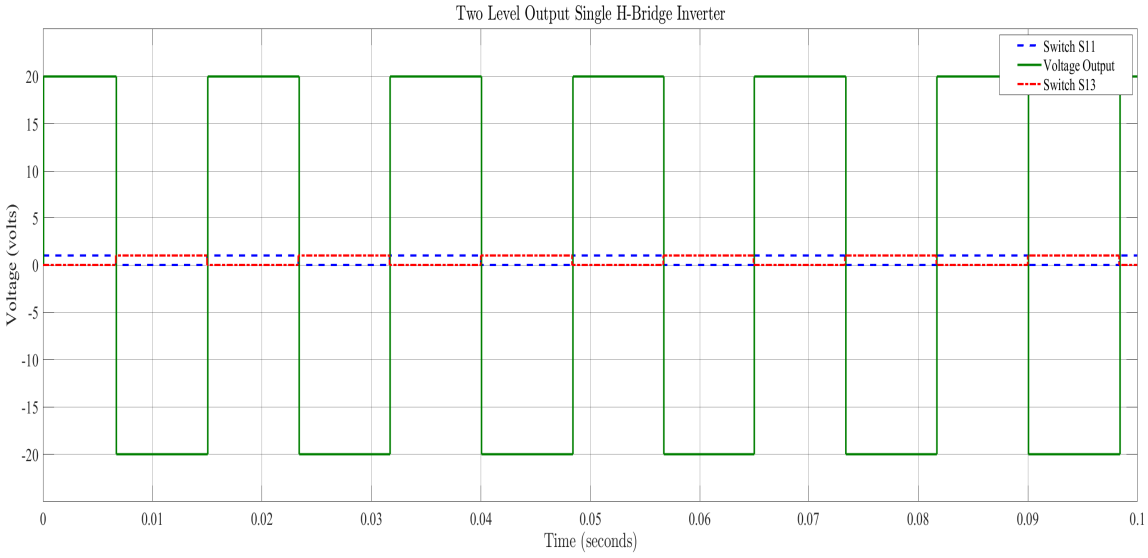


Figure 3.3: Simulation output of single H-bridge as two-level inverter.

Table 3.1: Operation of switches in figure 3.1 generating two-level output.

State	S_{11}	S_{13}	V_{out}
1	0	1	$-V_{DC}$
2	1	0	$+V_{DC}$

Figure 3.4 displays simulation of SHB inverter performed to generate three-level output. Table 3.2 presents operating states of switches and voltage levels for four switching states. Performance of switches from table 3.2 are validated in figure 3.4 drawing attention to synthesized three-level voltage output. Schematic diagram representation of state 3 and state 2 of table 3.2 are represented in figure 3.2 (a) and 3.2 (b), respectively; state 4 and 1 are depicted in figure 3.2 (c) and 3.2 (d), respectively.

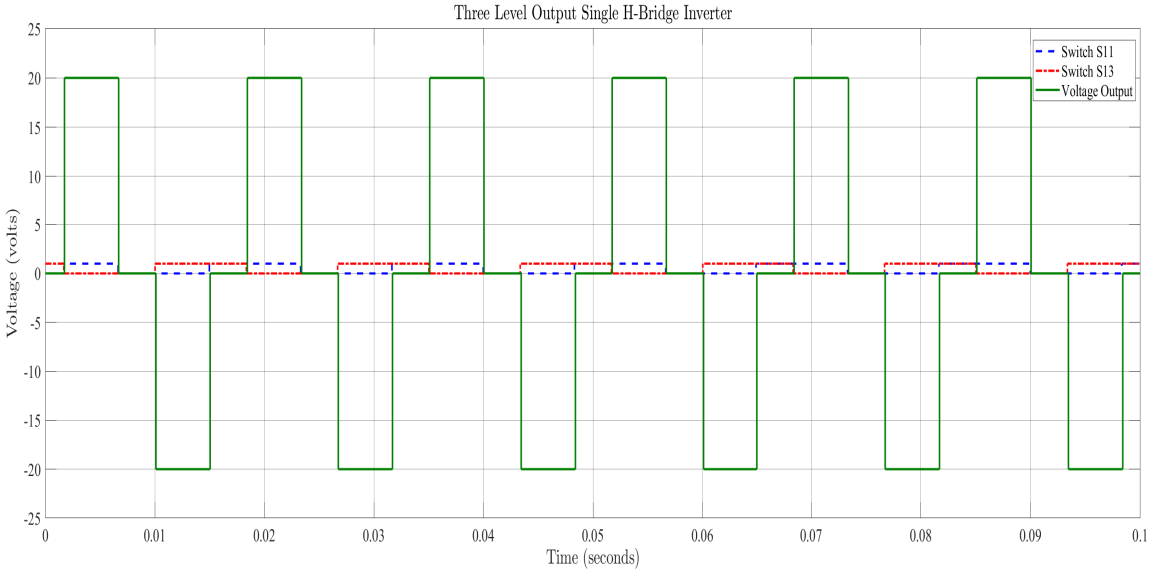


Figure 3.4: Simulation output of single H-bridge as three-level inverter.

Table 3.2: Operation of switches in figure 3.1 generating three-level output.

State	S_{11}	S_{13}	V_{out}
1	0	0	0
2	0	1	$-V_{DC}$
3	1	0	$+V_{DC}$
4	1	1	0

3.2.2 Cascaded Two H-bridge inverter

In order to study cascaded multilevel topology, two H-bridges are cascaded in this subsection. Common node of first H-bridge from switch S_{13}, S_{14} leg is connected to common node of second H-bridge switch S_{21}, S_{22} leg. Load is connected between switch S_{11}, S_{12} leg and switch S_{23}, S_{24} leg. Simplified architecture of the two cascaded modules are shown in figure 3.5. When two H-bridge inverters are connected in series, they generate five level voltage at output. Cascaded inverters using such modulation strategy are also known as symmetric cascade multilevel inverter. A seven-level or nine-level output can be generated using asymmetric cascaded modulation strategy, where each phase is supplied with unequal voltages. Thereby, this strategy limits the applications of inverter.

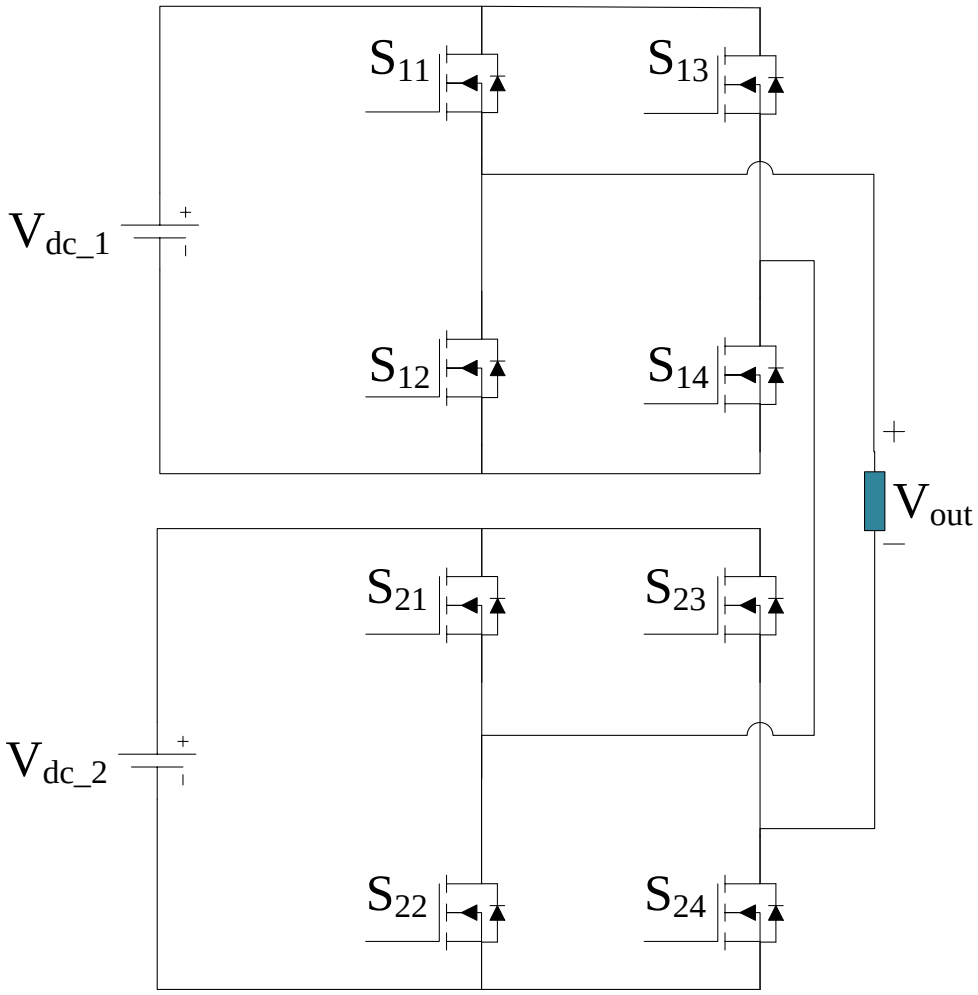


Figure 3.5: Simplified architecture of two cascaded H-bridge inverter.

Considering the importance of symmetric modulation strategy at this stage, table 3.3 includes the switching states of five-level inverter output. Table 3.3 shows sixteen different switching configurations for cascaded two H-bridge inverters. The five levels of voltages are $+V_{dc1}$, $-V_{dc1}$, $+V_{dc1}+V_{dc2}$, $-V_{dc1}-V_{dc2}$, and 0. Figure 3.6 represents simulation output of cascaded two H-bridge five-level inverter, where color of switching signals and voltage output are present in legend box. S_{11}, S_{13}, S_{21}, S_{23} are represented by blue, red, pink, and cyan, respectively.

Voltage output of symmetrically modulating switches can be validated by comparing the stages from table 3.3 and switching waveform obtained from simulation results

illustrated in figure 3.6. For instance, stage 16 can be verified when voltage level is at -20 V in the end of time cycle, where V_{dc1} = 10 V and V_{dc2} = 10 V; therefore, -V_{dc1}-V_{dc2} = -20 V. The graphics in figure 3.6 clearly shows that S_{13} and S_{23} are closed at the instance when output is -V_{dc1} -V_{dc2}.

Table 3.3: Operation of cascaded two H-Bridges in figure 3.5 as a five-Level inverter.

State	S_{11}	S_{13}	S_{21}	S_{23}	V_{out}
1	1	0	1	0	+V_{dc1}+V_{dc2}
2	1	0	1	1	+V_{dc1}
3	1	0	0	0	+V_{dc1}
4	1	1	1	0	+V_{dc1}
5	0	0	1	0	+V_{dc1}
6	0	0	0	0	0
7	0	0	1	1	0
8	1	1	0	0	0
9	1	1	1	1	0
10	1	0	0	1	0
11	0	1	1	0	0
12	0	1	1	1	-V_{dc1}
13	0	1	0	0	-V_{dc1}
14	1	1	0	1	-V_{dc1}
15	0	0	0	1	-V_{dc1}
16	0	1	0	1	-V_{dc1}-V_{dc2}

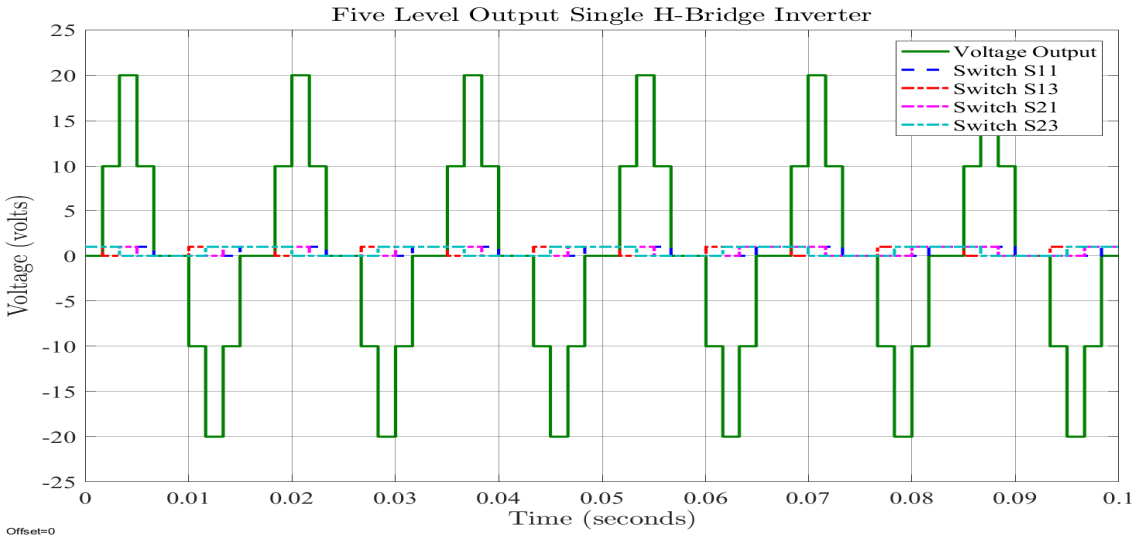


Figure 3.6: Simulation of cascaded two H-bridge inverter generating five-level output.

3.3 Design of Cascaded H-bridge Multi-level Inverter

Cascaded multilevel topology can be designed by connecting n number of H-bridges in series. For this thesis, three H-bridge modules are cascaded in order to synthesize quasi square wave AC output voltage, which is called cascaded multilevel inverter (CHB-MLI). In this section, inverter modules are described at component level, and design parameters are studied. Component name, description, and number of components required for development of each H-bridge module are listed in table 3.4

Table 3.4: Number of components required in a H-bridge.

Component	Single H-bridge
Power Supply	1
DC-DC Converter	4
MOSFET	4
Gate Driver	4
Voltage Sensor	1

Detailed circuit schematic of single H-bridge is shown in figure 3.7, including all the components needed,but circuit diagram does not include micro-controller and its connection as it will complicate the schematic. Therefore, go-to and from blocks showing the measurements sent and signal received from the micro-controller are included in the diagram. All the gate pulses utilized to trigger on the switches are indicated using from blocks. DC voltage needed to generate these gate pulses are sent to controller, using go-to block is labeled V_{sdc}, and from blocks are labeled G_{11}, G_{12}, G_{13}, and G_{14}.

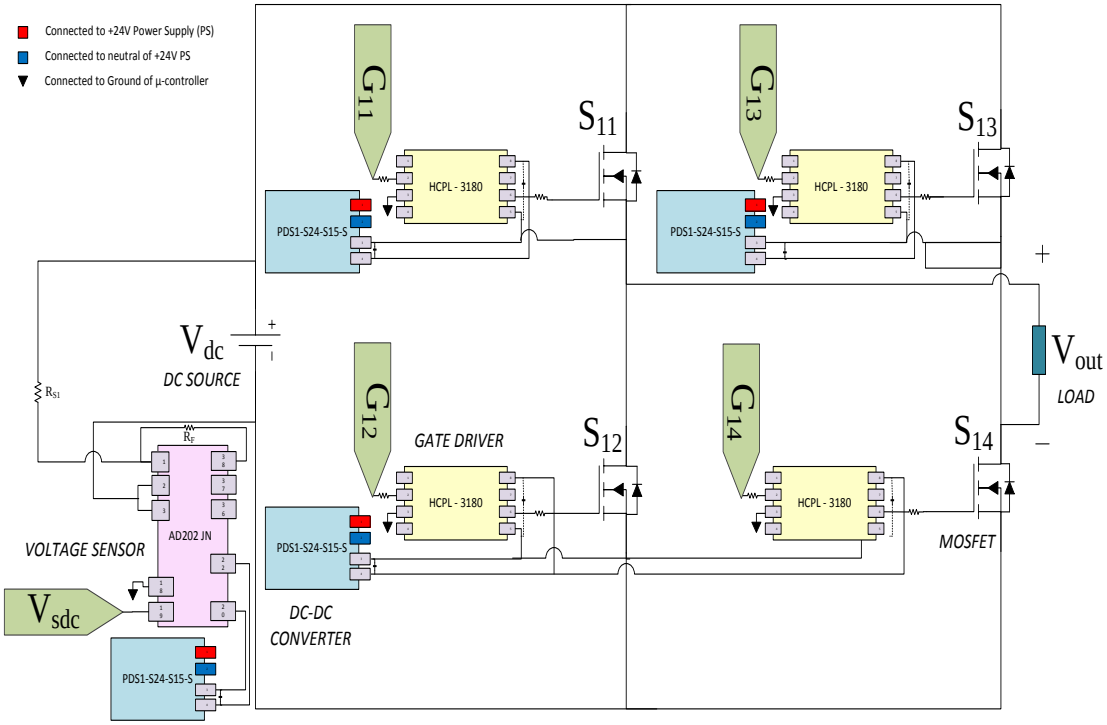


Figure 3.7: Detailed circuit schematic of single H-bridge inverter module.

All the components mentioned in table 3.4 are individually described with their functional diagrams in the following subsections.

3.3.1 DC-DC converter

A small package, DC-DC converter of PS1-S series, was used to power up gate drivers and a voltage sensor. Gate drivers triggering upper MOSFETs of both legs

were each powered from different converters, whereas bottom gate drivers of both legs receive power from same converter. Converter has four pins, as shown in figure 3.8 pin 1 and pin 2 are connected to ground (GND) and input voltage of source, respectively, and pin 3 serves at 0 potential for gate drivers connected with 15 V output at pin 4. DC supply of 24 V was necessary, and all the converters were supplied input voltage from same DC source. Pins connected to positive potential of 24 V source are represented by red square box, and neutral is shown by blue square box (figure3.7).

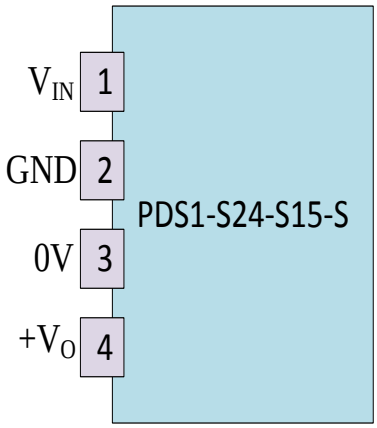


Figure 3.8: Functional Diagram of PDS1-S24-S15-S series DC-DC converter.

3.3.2 MOSFET

Four TK72E12N1, silicon N-channel MOSFETs of Toshiba, are utilized to construct each H- Bridge of CHB-MLI. The simplified drawing of MOSFET with pin 1, pin 2, and pin 3, represented as gate (G), drain (D), and source (S), respectively, are displayed in figure 3.9. The ratings of MOSFET are: Drain-Source voltage V_{DSS} = 120 V, Gate-Source voltage $V_{DSS} = \pm 20V$, and Drain Current I_D = 72 A.

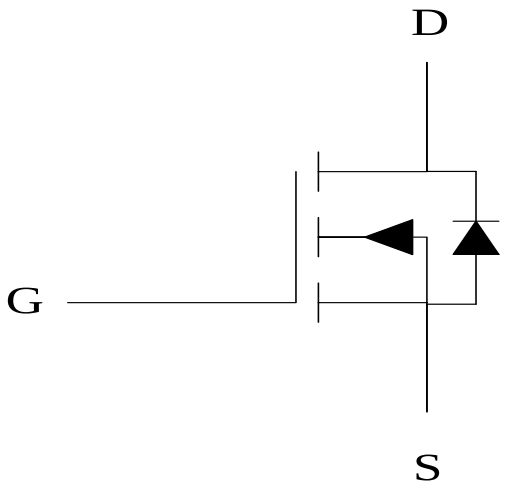


Figure 3.9: Simplified drawing of MOSFET.

3.3.3 Gate Driver

High speed 2.5 A gate drive optocoupler of HCPL-3180 series, from Avago Technologies, are utilized as a gate driver. The gate driver has 8 pins, and the functional diagram is shown in figure 3.10. As seen from the data-sheet, gate pulses from the micro-controller supplied to pin 2 (Anode) is interfaced via small resistance 300 ohms in this study, the ground of controller attaches into pin 3. Fifteen volts obtained from PS1-S series DC-DC converter is applied between pin 8 (+15 V) and pin 5 (0 V) also known as V_{CC} voltage. Gate driver output can be drawn from pin 6 or pin 7, which is connected via gate Resistance R_g to the gate terminal of MOSFET, and can be calculated from equation 3.1. Pin 5 is connected to source terminal of MOSFET, providing 0 potential for gate pulse output.

$$R_g \geq \frac{V_{CC} - V_{OL}}{I_{OLpeak}} \tag{3.1}$$

where V_{CC} = 15 V, $V_{OL} = 3V$,I_{OLpeak}= 2A, $R_g \geq 6ohms$

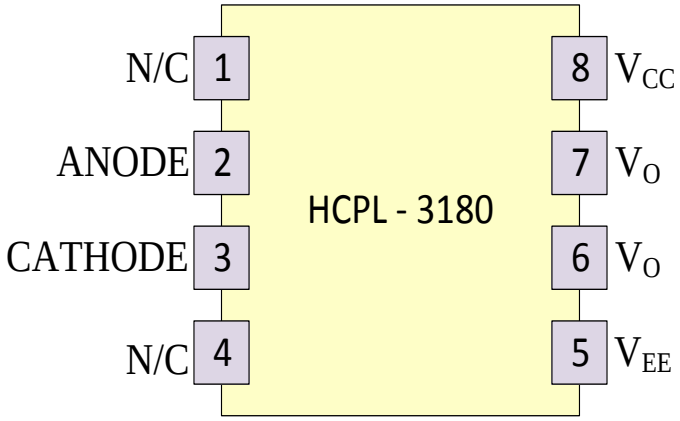


Figure 3.10: Functional diagram of gate driver.

3.3.4 Voltage Sensor

AD202JN belongs to general purpose, transformer-coupled isolation amplifier, of series AD202. They are used in multiple applications which requires measuring, processing and transmitting input signals. DC supply of 15 V is needed to power it. Pin 1 and pin 3 are connected to + Input signal and - Input signal, respectively, whereas pin 38 is connected to give Input feedback. Pin 18 and pin 19 give Output Low and Output High, respectively, as presented in figure 3.11. Power input of 15 V is connected to pin 20 and 15V power common is connected to pin 22. This amplifier is used for sensing input voltage at DC-link of H-bridge, ranging from 0-50 V. The operational amplifier circuit is designed using equation 3.2, which helps in scaling down input DC voltage in the range of 0-3.5 V for micro-controller, to process this analog signal.

$$V_O = -V_{S1} * \frac{R_F}{R_{S1}} \tag{3.2}$$

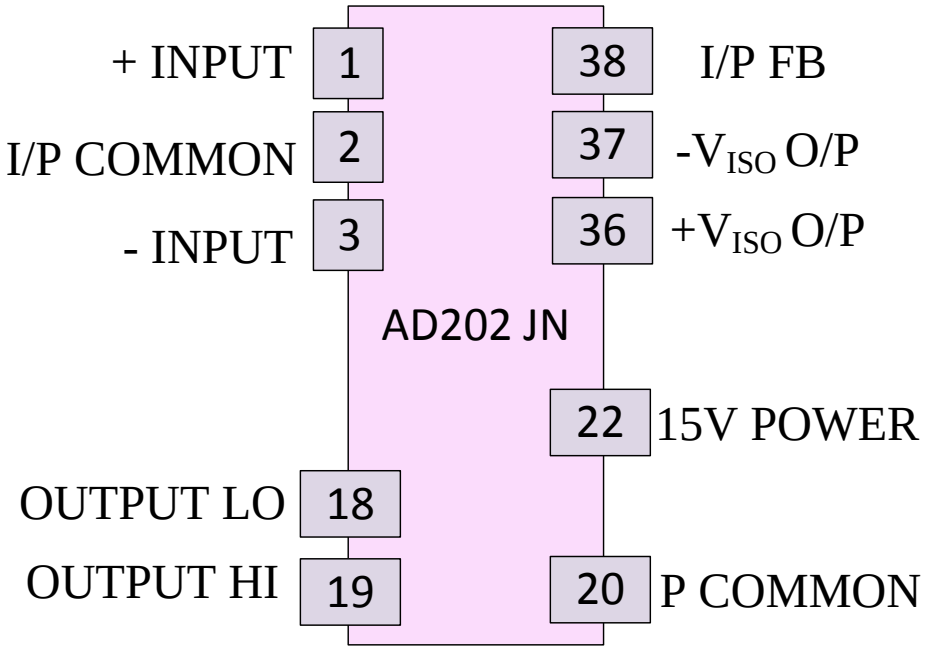


Figure 3.11: Functional diagram of voltage sensor.

CHB-MLI's detailed circuit diagram includes all the components on each board, connects three H-bridges to the DC power supply individually, and integrates two-terminal AC to load as shown in figure 3.12. Throughout this thesis, each H-bridge power cell is referenced as boxes. Inverter H-bridge power cells are being numbered as Box 1, Box 2, and Box 3. Also, the controllers go-to and from blocks are color coded as green, orange, and violet that correspond to Box 1, Box 2, and Box 3, respectively.

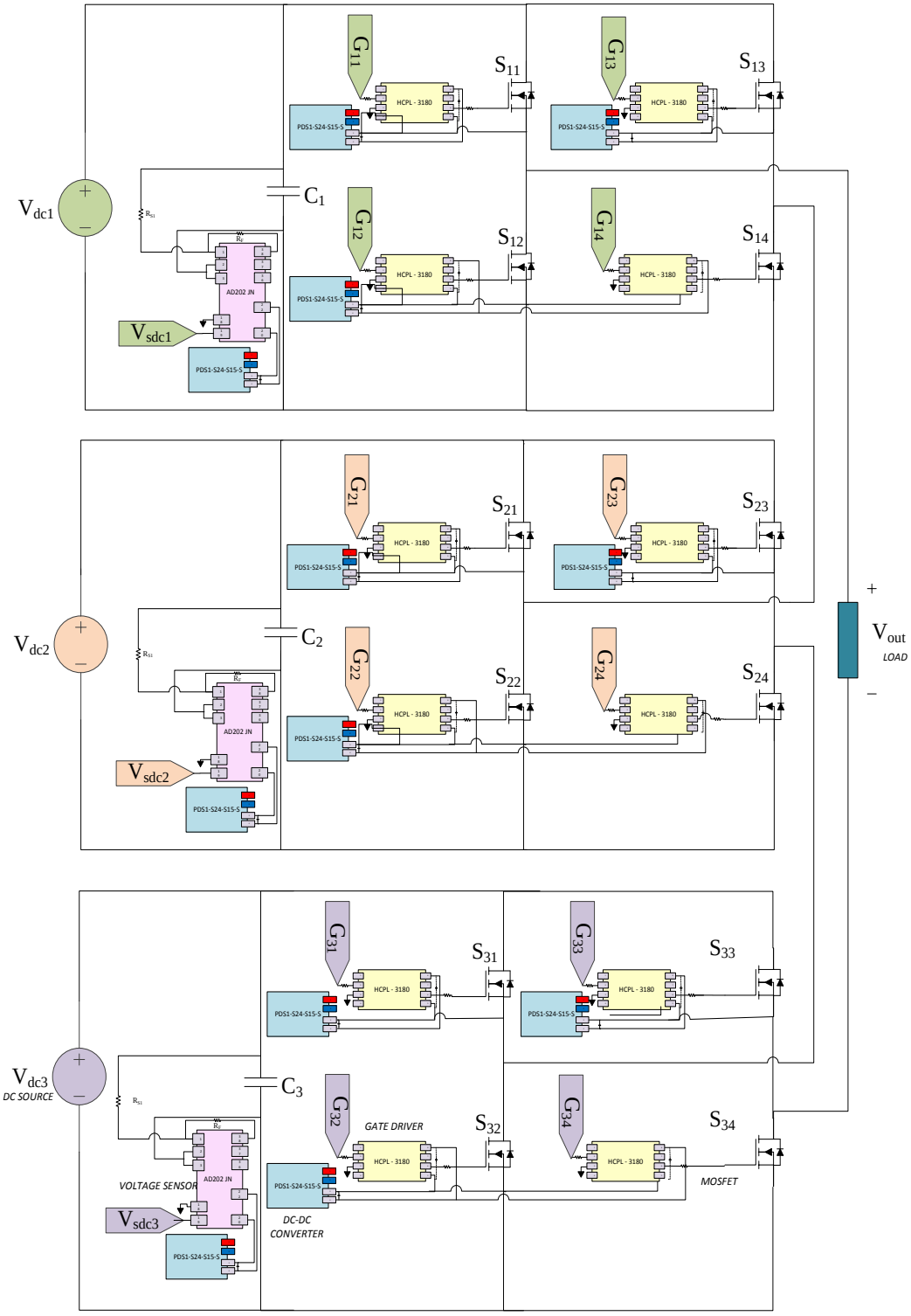


Figure 3.12: Detailed circuit schematic representation of three H-bridge cascaded multi-level inverter.

3.4 Modulation Strategy

In chapter 2, various topologies of multi-level inverters have been surveyed, and multiple modulation strategies implemented on CHB-MLI have been described. For this thesis, focus remains on a particular technique of Sorted Staircase Modulation. This strategy has been utilized for simulation and experimental verification of distributed controls on CHB-MLI, where importance is given to extract the maximum power from the each panel in order to harvest energy from renewable resource at its maximum potential. For simulation, PV panels are utilized as DC source for each module of inverter, whereas for experimental purposes DC power supplies were put to use. The DC voltages measured from all the panels are sorted in descending order, and the panel with highest voltage is designated to synthesize the first square wave output of the staircase waveform. As the width of the bottom step in the staircase is maximum, the current drawn from that particular panel will be highest. Therefore, it helps in serving the purpose of drawing the maximum available power. For the next step of the output voltage waveform, the panel with the second largest voltage is selected. The switching instance is selected at the point when the reference voltage is greater than sum of all the previous step voltages and half of the existing step voltage. This series of synthesizing output staircase waveform is repeated for all the available power cells in CHB-MLI. Figure 3.13 presents the flowchart, which describes the sorted staircase modulation strategy implemented in this thesis.

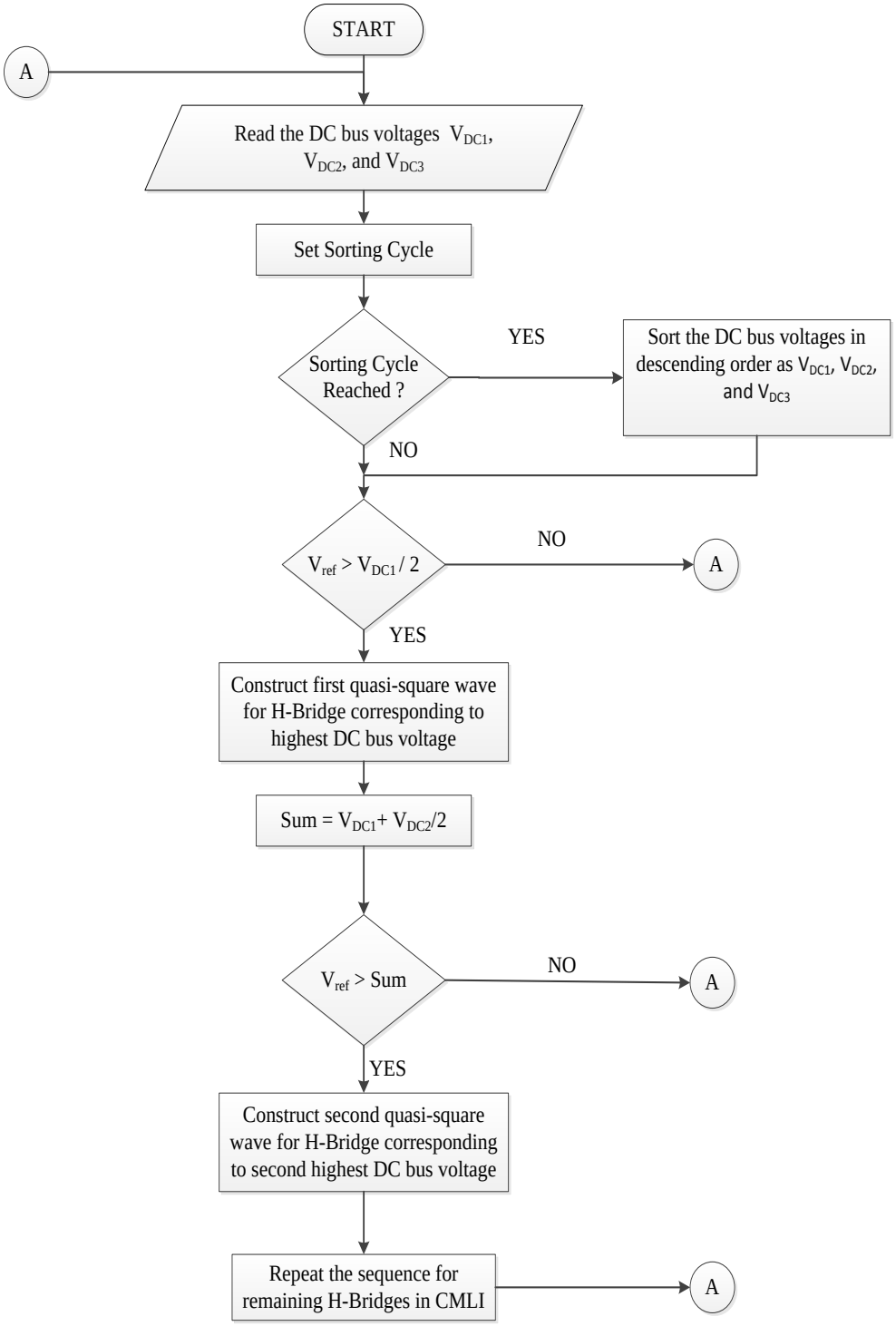


Figure 3.13: Flowchart of sorted staircase modulation strategy implemented on three H-bridge cascaded multilevel inverter.

CHAPTER 4: ARCHITECTURE OF DISTRIBUTED CONTROLS AND COMMUNICATION PROTOCOLS

4.1 Overview

This chapter presents the importance of distributed controls and highlights economical benefits of distributed solution, when implemented with CHB-MLI topology. Section 4.2 gives insight of single master controller, its limitations and its necessity of distributed controls. Section 4.3 discusses various connected communication protocols namely: Universal Asynchronous Receiver Transmitter, Serial Peripheral Interface, and Inter-Integrated circuit. Simplified architectural schematic of these protocols when implemented with CHB-MLI are clearly shown with two comparisons in section 4.4. The chapter concludes with the section 4.5, where in-depth analysis on the available features of the micro-controller utilized for distributed controls are performed.

4.2 Master Controller and Distributed Controls

As discussed in Chapter 3, each H-bridge power cell requires four gate pulses in order to operate. In CHB-MLI topology in order to cascade more modules, the gate pulses required will increase simultaneously. If the number of inverters to be cascaded is n the gate pulses required will be 4 times n. Also, each bridge is required to sense DC voltage of solar panel connected to it, which leads to rise in number of analog to digital converters (ADC) for sensing DC voltage of inverter modules. Thereby, extending the number of inverters with respect to voltage output needed to synthesize at the ac terminals of inverters expands the hardware dependency on single micro-controller. The graphical representation of such a requirement in shown

in figure 4.1

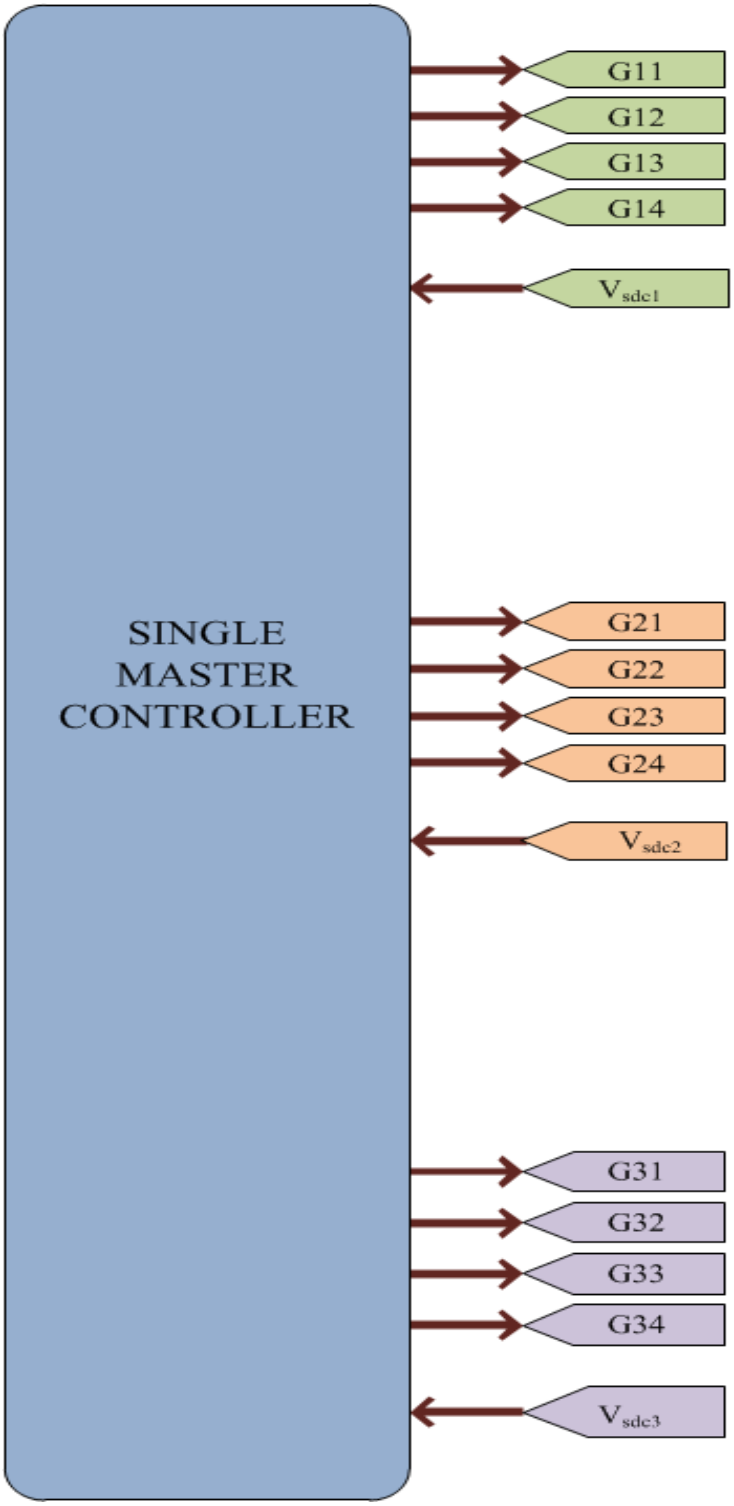


Figure 4.1: Demonstrating number of peripherals required by single micro-controller to operate three power cell CHB-MLI

Using a single micro-controller will increase the complexity in circuit connections. Number of available ADC inputs and PWM peripherals limit the number of H-bridge inverter modules that can be used. Demonstrating distributed controls will bound the requirement of pulse generator to four PWM peripherals in single controller, as presented in figure 4.2, and establishing communication for transmitting voltage of each module will confine the need of ADC to one input, as presented in figure 4.3. Therefore, it reduces the cost of controller and each inverter module. Understanding the hardware peripheral specifications and scrutinizing various communication protocols from the study in Chapter 2, 28 pin DIP package controller from Microchip PIC32MX series has been shortlisted for the implementation of distributed controls and communication.

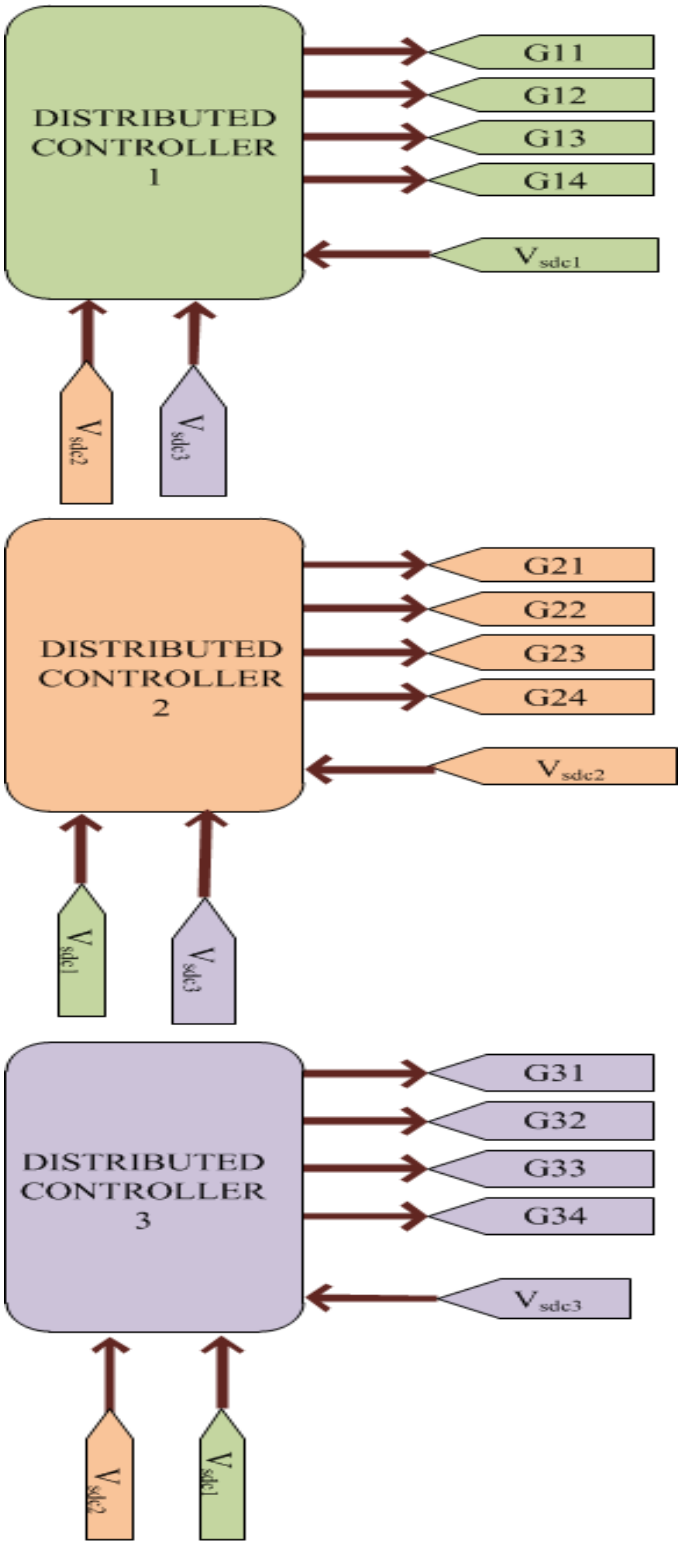


Figure 4.2: Demonstrating number of peripherals required for distributed controls to operate three power cell CHB-MLI.

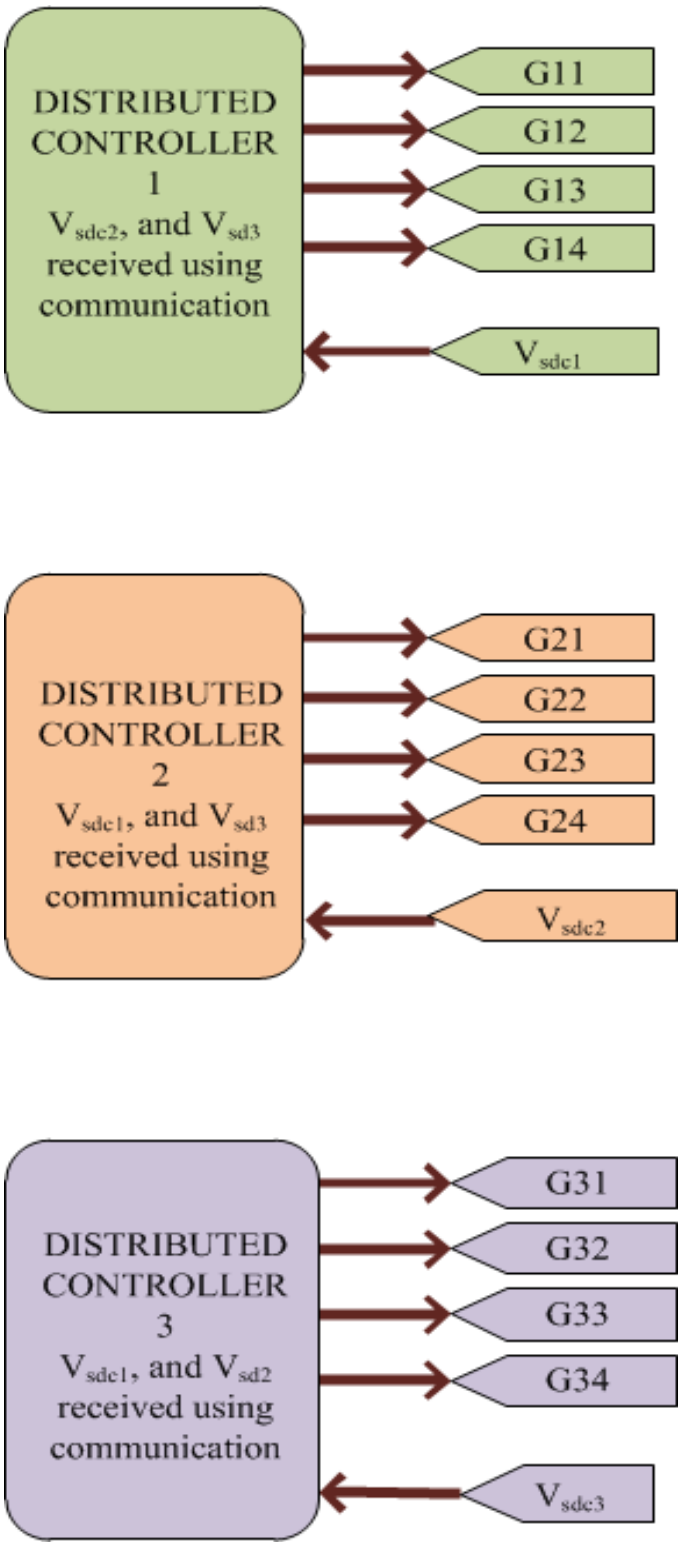


Figure 4.3: Demonstrating number of peripherals required for distributed controls along-with communication protocol to operate three power cell CHB-MLI.

4.3 Description of Connected Communication Protocols

This section looks into connected communications classified into three different protocols: universal asynchronous receiver transmitter, serial peripheral interface and inter integrated circuit.

4.3.1 Universal Asynchronous Receiver Transmitter

Universal asynchronous receiver transmitter(UART) allows two device to communicate with each other. The data format and transmission speeds are configurable. It uses two lines for communication of data: Tx for sending the data and Rx for receiving the data. Ground of two devices should be made common. UART takes byte of data while transmitting, it send data bit by bit and at receiving end all bits are assembled into complete byte [41]. Figure 4.4 presents distinct archetype of UART protocol. UART works on the principle of asynchronous transmission, where clock signal is not needed. Data can be transferred in both half-duplex and full-duplex mode.

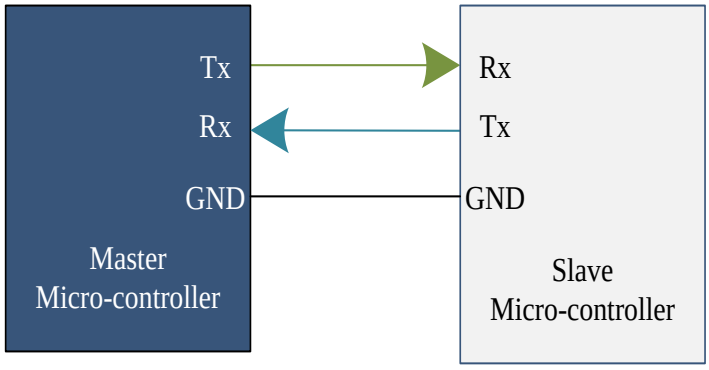


Figure 4.4: Archetype of UART protocol.

In UART transmission, Tx line remains high when not transmitting. UART initiates transmission by lowering the start bit of Tx for one period. Start bit indicates transmission has been initiated, letting receiver start its baud clock and receive the bits. After start bit, data bits are sent, and it is optional to send a parity bit there-

after. In data, least significant bit is sent first. At the end holding the line high one or two stop bits are sent, and another transmission can began. Start bit, parity bits and stop bits are control bits. As they do not contain data, baud does not correspond directly to data rate. Figure 4.5 shows typical UART 8-bit data transmission of 0b10110010 with start and stop bits but no parity. After UART receives data, it sends each bit into register. When full byte is received, the data is transferred into UART's Rx first-in-first-out queue (FIFO). Similarly, Tx FIFO is loaded while transmitting data. From FIFO, hardware data is transferred into shift register, sending it further over the wire[42].

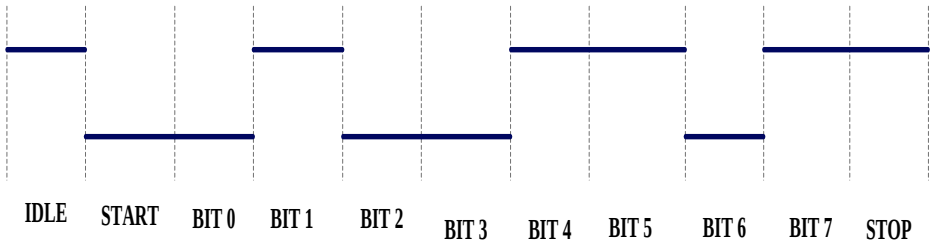


Figure 4.5: UART transmission of 8-bit data with start, stop, and no parity bit.

4.3.2 Serial Peripheral Interface

Serial Peripheral Interface(SPI) is a synchronous serial communication interface and runs on master-slave architecture with single master. It works in full-duplex mode; i.e., both master and slave can transmit data simultaneously. SPI works on four lines, also known as four wire serial bus [43]. The four lines are SCLK, MOSI/SIMO, MISO/SOMI, SS. Where, SCLK is serial clock line output from master, MOSI/SIMO is master output slave input line, MISO/SOMI is master input slave output line, and SS is slave select line output from master, active when low, and function is to select the slave. Figure 4.6 shows the archetype of SPI protocol, where each slave needs a separate SS line in order to connect multiple slaves with master micro-controller.

Master keeps the SS line low for distinct slave it wants to communicate with, and for rest of them SS line is kept high. It is essential to note that multiple slave can be selected but not recommended. As they both may try to send data on same MISO, which may produce a garbage data. Direction of data flow with respect to individual lines are depicted through arrows in the figure 4.6.

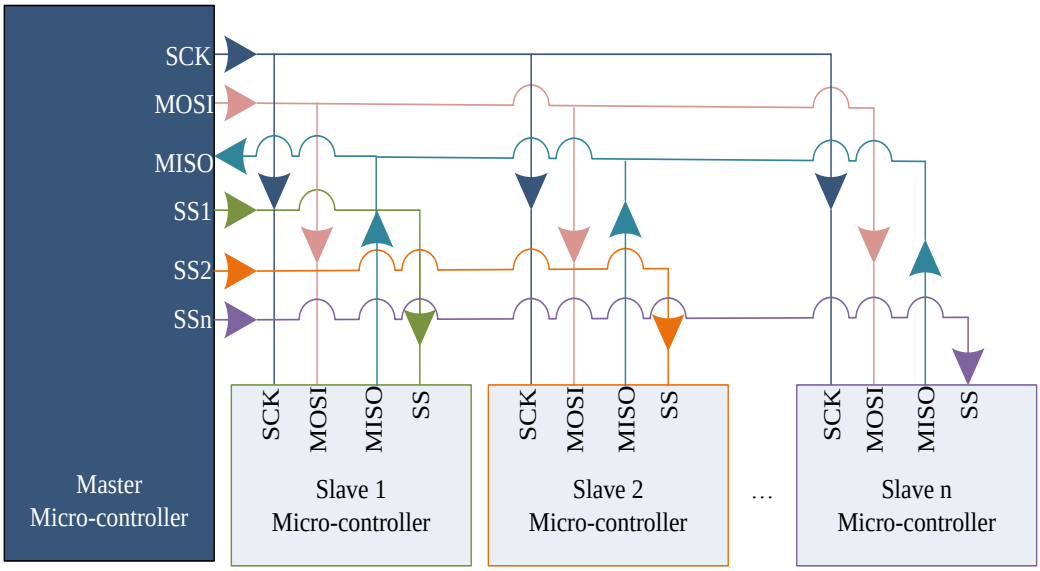


Figure 4.6: Archetype of SPI protocol.

In SPI, master initiates all the communication generating a square wave on SCK line. Reading from slave and writing to slave, both the features can work simultaneously. The slave is selected when SS is driven low. Transition to next bit of signal occurs at the falling edge of master's SCK. The devices read the data on the rising edge of SCK. In the example shown in figure 4.7 master sends 8 bits, first bit of which determines whether it will be read or write operation. The address of the slave register to be accessed is determined from AD0 to AD5. At the end if the operation is read from slave, slave will send data D0 to D7 on MISO line, otherwise master sends data on MOSI line to write on slave.

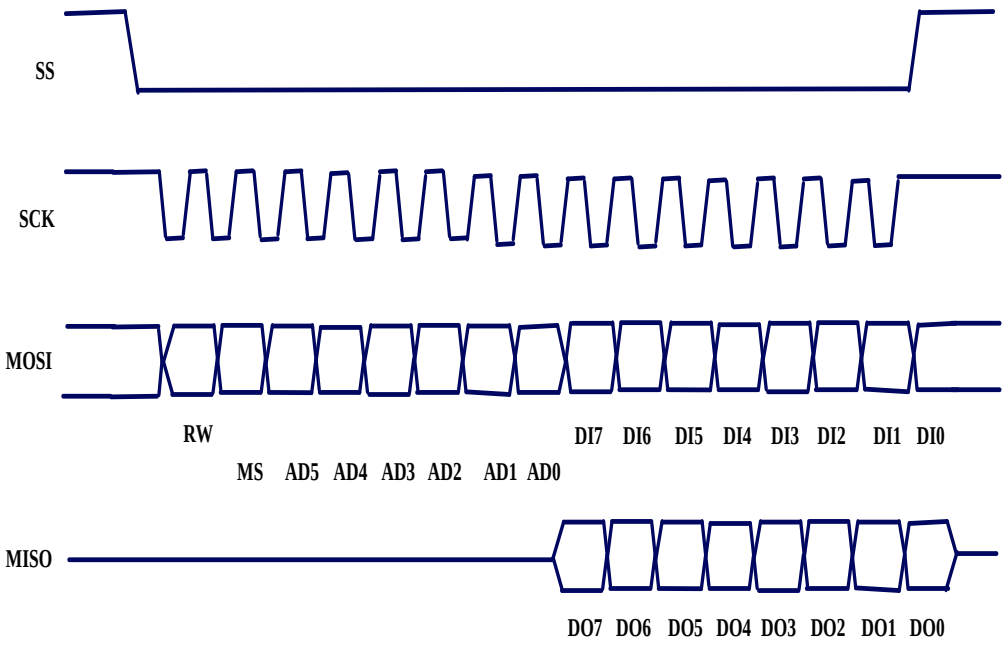


Figure 4.7: Transmission of data in SPI protocol.

4.3.3 Inter-Integrated Circuit

Inter-Integrated Circuit stands for I2C and can be pronounced "I squared C". This communication protocol requires two data bus lines: a serial clock line (SCL) and a serial data line(SDA). These data bus lines are bi-directional. Figure 4.8 represents archetype requirement of I2C protocol and highlights the need of external pull up resistor in this configuration. SCL contains clock signal, and clock signal is always generated by the master. Depending on the devices connected to bus, each device can have unique software recognizable address (7-bit or 10-bit). Peripheral address and all the data are transferred by SDA. Maximum number of slaves that can communicate on same bus is 112 [44]. I2C protocol works on simple master-slave relationship. It is possible to have multiple masters on the same I2C bus. It also has features, such as, bus collision and arbitration, to prevent data error or loss of data. 8-bit data transfer can be made, achieving baud rate of 100 kbit/s in standard mode and baud rate of

400 kbit/s in fast mode. Recent revisions of I2C can run at 1 Mbit/s in Fast mode plus and 3.4 Mbit/s in High Speed mode. It has low current consumption, immunity to noise is high, and supply voltage range is wide; however, typical voltages used are +5V and +3.3 V. Simple two-wire serial I2C bus minimizes interconnection, leading to fewer pins and reducing copper traces in PCB tracks.

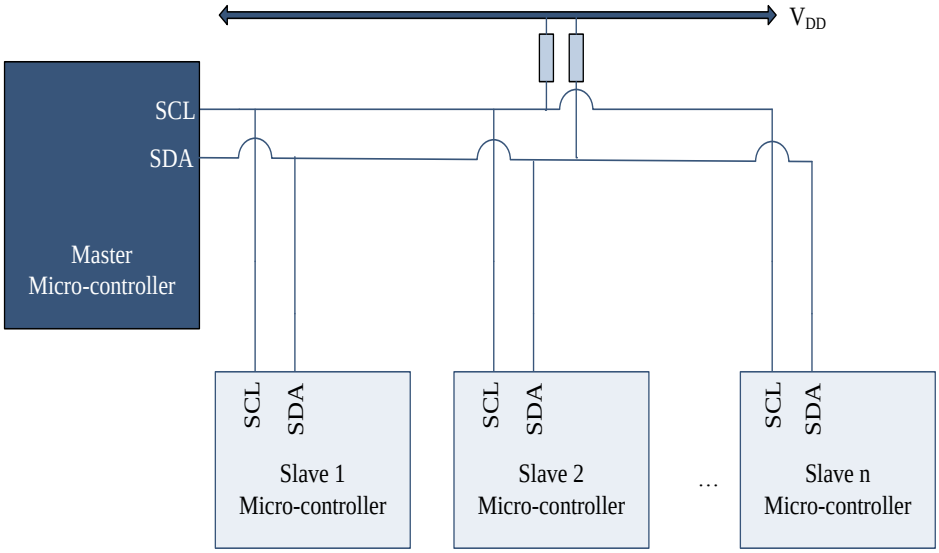


Figure 4.8: Archetype of I2C protocol.

The device that assumes the role of master in I2C protocol initiates the transmission by pulling SDA line low and leaving SCL line high. This resembles start bit, which informs other devices that the bus is entitled to this master, and cannot be claimed until the transmission is completed. While master controls the clock SCL, transmission of data is performed over SDA line. Data is read from SDA on rising edge of SCL and is loaded on SDA at falling edge of SCL. SDA line can be controlled either by master or by slave, depending on who wants to send or receive the data. 8-bit data bytes are transferred (most significant bits being the first), and the stop bit is sent with the release of SDA, allowing it to go high while SCL was high. In figure 4.9 transmission begins with 0b110..., which are the highest three bits of selected

slave address.

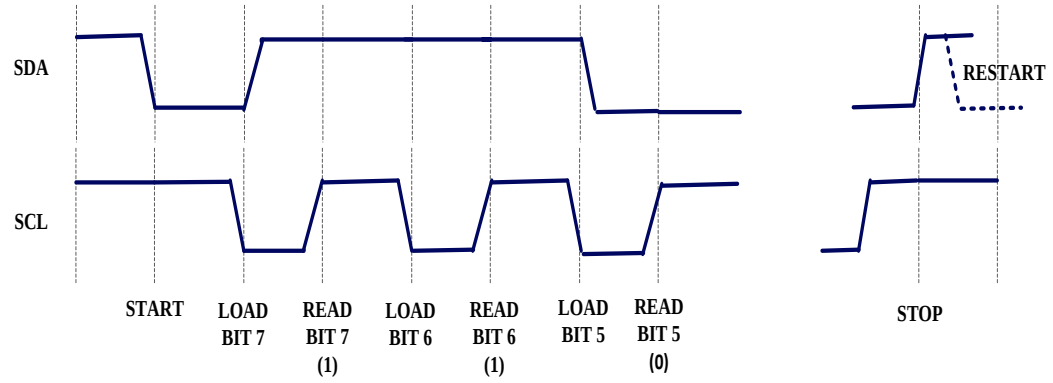


Figure 4.9: I2C protocol data transmission begins with 0b110...

4.4 Architecture and Comparison

All the protocols mentioned in previous passages are illustrated, emphasizing on wire requirements from one PIC micro-controller of a box to another. PIC 1, PIC 2, and PIC3 are embedded with H-bridge inverter named as, BOX 1, BOX 2, and BOX 3, respectively. From and go to blocks stores sensed DC voltage and gate pulses. Arrows indicates the direction of data received from analog voltage sensor and pulses sent to gate drivers of H-bridge.

Figure 4.10 provides the schematic architecture of UART protocol with PIC32MX peripheral device. Here, the image provides information of three boxes communicating the sensed DC voltages of each H-bridge. Similarly, figure 4.11 and figure 4.12 exhibit the structural connection of SPI and I2C protocol. In all the protocols, wire connections for synchronizing (SYNC) signal and ground (GND) are present. SYNC signal is needed to synchronize gate pulses for H-bridge power cells of all the micro-controllers at 60 Hz frequency.

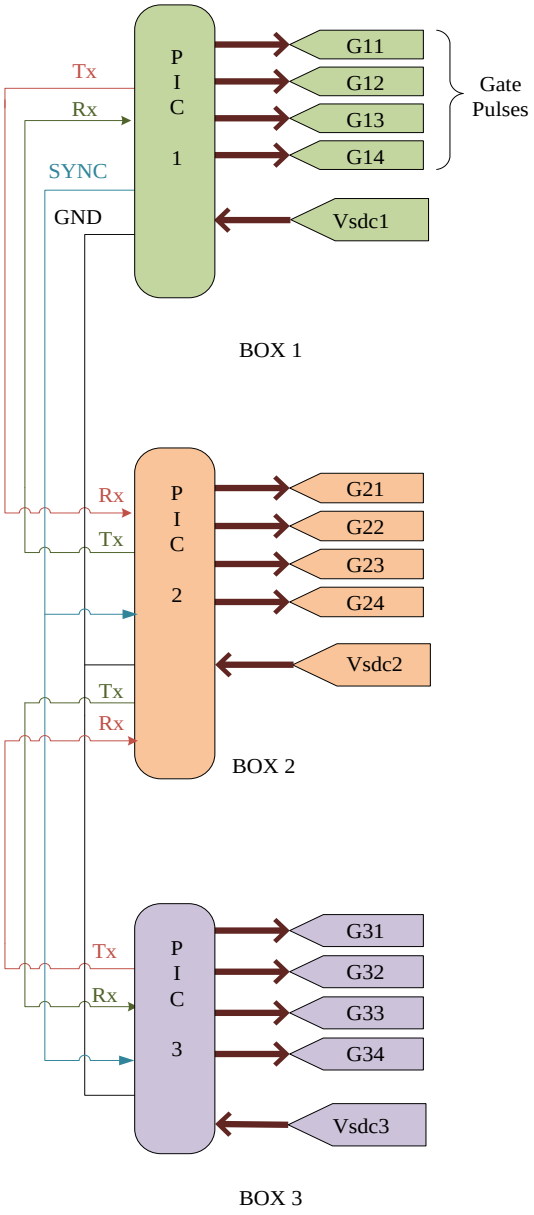


Figure 4.10: UART protocol connections with PIC micro-controller.

In the UART architecture as the number of inverter modules increases, each controller requires to have two Tx and Rx peripherals, each for transmitting and receiving data to adjacent controllers. It is demonstrated in the figure 4.10 with PIC 2 controller of an inverter module (Box 2). For three set of inverters connected in series the circuit connections appear clear, yet with increase in the number of modules the

connection complications will increase.

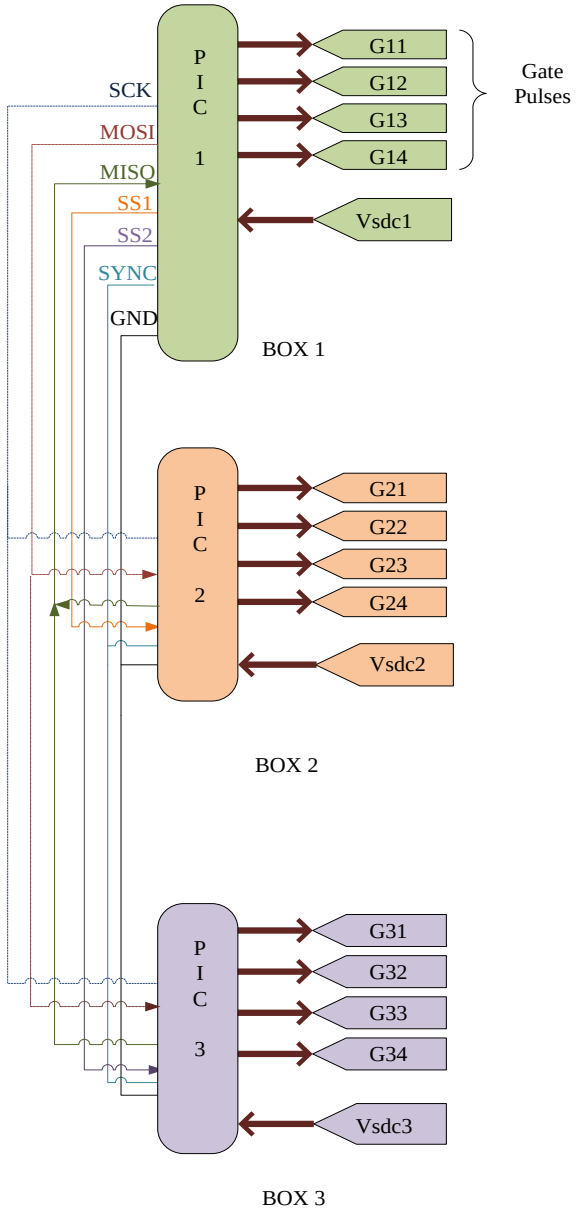


Figure 4.11: SPI protocol connections with PIC micro-controller.

The simplified schematic in the figure 4.11, exhibits the detailed master-slave relationship of SPI protocol. As the number of modules increased to synthesize higher AC voltage output, the number of wires required to connect multiple slave modules with master controller will also increase. As SPI structure has complicated four-wire

system, extension in cascaded inverter modules heightens circuit connection complexities.

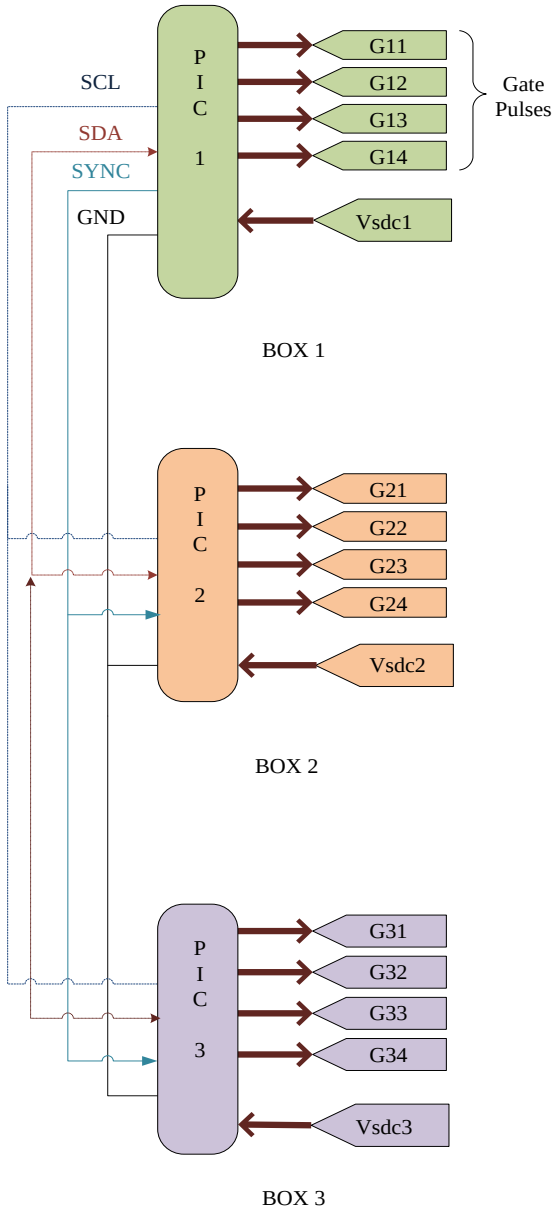


Figure 4.12: I2C protocol connections with PIC micro-controller.

I2C protocol is the simplest in terms of implementation and wiring requirements. Figure 4.12, shows the picture of two-wire multi-master system. Even with the increase in series connected inverter modules the wired connection stays same. Hence,

the protocol is clear to understand and apply.

In the table 4.1 comparative details about data rate, distance, type of communication, master-slave relation, advantages and disadvantage of three communication methods are provided. Further, an investigation in terms of physical connection necessity in relevance to number of inverter modules is shown in table 4.2.

Table 4.1: Comparison of connected communication protocols.

Attribute	UART	SPI	I2C
Data rate	from 230 Kbps to 460 Kbps	from 10 Mbps to 20 Mbps	100 Kbps, 400 Kbps, 3.4 Mbps
Distance	Low	Highest	Higher
Type	Asynchronous	Synchronous	Synchronous
Number of masters	N/A	One	One or more than one
Advantages	Simple protocol	Full duplex communication, push-pull mechanism	Multi-master system, simple addressing, bus voltage flexibility, uses flow control
Disadvantages	Communication between two devices only, fixed data rate set initially	Hardware complexity, no flow control, master and slave reltationship cannot be changed	Half-duplex interface

Table 4.2: Wire requirements for n number of inverter modules to communicate DC voltage.

Connection Protocol	Two module	Three module	n module
UART	two	four	n+(n-2)
SPI	four	five	3+(n-1)
I2C	two	two	2

4.5 Micro-controller and its Application

PIC32MX series 32-bit micro-controller of twenty-eight pin DIP package type is utilized for control purpose. The controller is coded in MPLABX integrated development environment with the basic code language (C). In the following subsections features of PIC32MX170F256B utilized for the generation of output gate pulses are discussed. PDS1-S24-S3-S DC-DC converters are used to supply V_{DD} voltage to the micro-controllers.

4.5.1 Analog-to-Digital Converter

Analog-to-Digital converter (ADC) converts analog signal to digital signal. In field of electronics it is used to provide measurements of analog signals, such as, voltage and current, into a digital number for control purposes. In PIC32 series, ADC used is of 10-bit resolution, there are 16 analog channels from AN0 to AN15.

Analog sampling comprises of two stages: acquisition and conversion. In the course of acquisition, the analog input channel is latched to the Sample and Hold Amplifier (SHA). As the sample voltage is equal to the input voltage, channel detaches itself from the SHA, to supply a steady input voltage for the conversion process. When the conversion is accomplished, conversion procedure converts the analog sample voltage to a binary depiction, and the result is stored in one of the buffer registers (from ADC1BUF0 to ADC1BUFF).

For reading the value of ADC, ReadADC10(BUF) command can be used. BOX1,

BOX2, and BOX3, utilizes channel AN0 i.e., pin 2, channel AN1 i.e., pin3, and channel AN4 i.e., pin 6, respectively, for sensing analog voltages. Measured analog voltage can be calculated from the equation 4.1

$$AnalogVoltageMesured = \frac{Voltageofsystem * ADCreading}{ResolutionoftheADC} \tag{4.1}$$

4.5.2 Output Compare

From various peripherals available in PIC32 micro-controller, output compare (OC) module is one, and it requires timer as well as compare values to operate. Either 32-bit timer or 16-bit timer can be used for this purpose, depending on the experimental requirement. There are five timers and five output compare pins in PIC32MX170F256B micro-controller. The timer is programmed to count up-to desired frequency and period value, where TMRy is timery count register and PRy is Timery period register.

The OC module has four modes of operation-

1. Single compare set high or low modes.
2. Single compare toggle mode.
3. Dual compare single or continuous pulse modes
4. Pulse width modulation mode.

Depending on the chosen operating mode, OC module matches the value of the timer with the compare values and output pulse is generated at OC pin. In this experiment dual compare continuous pulse mode is selected, where two compare values are required to put in OCxR (primary compare register) and OCxRS (secondary compare register). During match of the timer and the primary compare value in OCxR register, output pulse at OCx pin is driven to high state, whereas, negative edge of output pulse is generated when the timer and the secondary compare value

in OCxRS register are equal. TMR_y continues to count and eventually resets to 0 at period match (i.e., $PR_y = TMR_y$).

$$SwitchingFrequency = \frac{1}{SwitchingPeriod} \tag{4.2}$$

$$SwitchingPeriod = (PR_y + 1) * T_{PB} * (TMR_yPrescaleValue) \tag{4.3}$$

In our experimental set-up Timer 2 is utilized for the operation of OC module. The period register value is calculated from the equation 4.3, where T_{PB} stands for Peripheral Bus clock period. The values of following parameters are — $T_{PB} = \frac{1}{40MHz}$, $SwitchingFrequency = 60Hz$, $TMR_2PrescaleValue = 16$—.

$$\frac{1}{60} = (PR_2 + 1) * \frac{1}{40 * 10^6} * 16$$

$$0.016666 = (PR_2 + 1) * 2.5 * 10^{-8} * 16$$

$$PR_2 = 41665$$

Therefore, at every 60Hz period match Timer 2 resets. This enables Timer 2 interrupt, and in Timer Interrupt Service Routine (ISR) calculated value of time at which high state and low state of output pulses should be generated are stored.

4.5.3 Inter-Integrated Circuit (I2C) Communication

This handshaking protocol, for data transmission between master and slave, consists of following element in sequence– START, ADDRESS, ACKNOWLEDGEMENT (ACK/NACK), WRITE OR RECEIVE, ACKNOWLEDGEMENT(ACK/NACK), STOP or RESTART [42].

START: Master gives a start bit by dropping SDA line from high state to low state, it is important that SCL stays at high state when SDA issues this bit.

ADDRESS: Master issues a byte comprising of 7-bit address and a read-write (RW)

bit —least significant bit—. Address indicates towards the slave master wants to communicate with, each slave on the bus has unique 7-bit address. If RW bit is 0 master writes, and if it is 1 master reads.

ACKNOWLEDGEMENT(ACK/NACK): As slave recognizes its address, will respond by issuing acknowledge(ACK) bit of 0. Also, holds SDA line low for next clock period. Whenever SDA remains high, it signifies no acknowledgement also known as NACK, signaling master that error has occured.

WRITE OR RECEIVE: Master transfers a byte over SDA when RW = 0, and slave takes charge over SDA line and sends data when RW = 1.

ACKNOWLEDGEMENT(ACK/NACK): When slave receives write bit, it is essential to send ACK bit, otherwise, master considers an error have occurred. Master sends an ACK at read bit if it wants another byte or NACK if no more data is required.

STOP or RESTART: Master sends a stop bit by rising SDA line to high state while SCL is high, to terminate the transmission. This allows other devices to take control over the bus. Master can issue a restart bit if it wants to keep control over bus, which is a signal where stop is followed quickly by another start.

CHAPTER 5: MODELING AND SIMULATION OF CASCADED H-BRIDGE MULTI-LEVEL INVERTER

5.1 Overview

This chapter describes the model of a load connected CHB-MLI companioned with PV panels developed in MATLAB/Simulink and displays performed simulation results. Section 5.2 explains a block diagram of load connected CHB-MLI with distributed controls, which is further subdivided into model of solar PV module and control strategy. In section 5.3 simulation results of load connected CHB-MLI are presented. Also, discussion for two sorting frequencies in both the case studies are exhibited.

5.2 Model of Load connected Cascaded H-bridge Multi-level Inverter

A simplified diagram of cascaded H-bridge multi-level inverter (CHB-MLI) model developed in MATLAB/Simulink is shown in figure 5.1. As discussed in Chapter 3, three PV panels of similar rating are selected from simulink library. Figure 5.2 gives distinct view of CHB-MLI, where each H-bridge power cell is connected with a PV panel, and AC terminals of the three H-bridges are connected in series, forming a two terminal AC output. These output terminals are connected with resistive load, demanding active power of 750 W, and voltage is set at 60 V rms with 60 Hz frequency. Therefore, requirement of reference voltage to be synthesized must have a peak of 84.84 V. The distributed control blocks are the color coded subsystems, subtitled as, controller1 (green), controller2 (orange), and controller 3(purple), as shown in figure 5.1. All the measured DC voltages at DC link of each panel are sent to this control blocks, where this information is processed and utilized by SSCM

strategy to generate gate pulse signals.

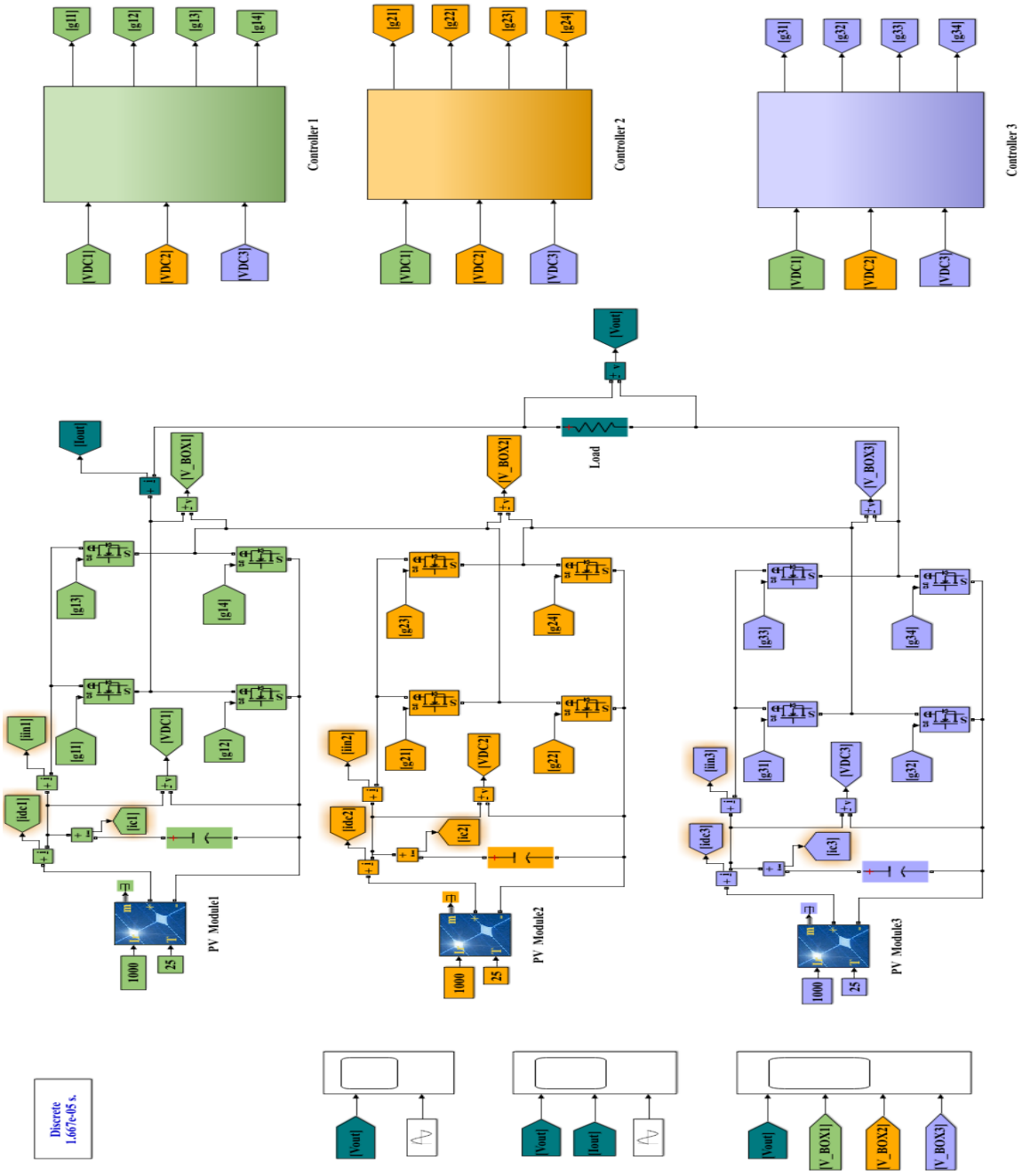


Figure 5.1: Block diagram of CHB-MLI model developed in MATLAB/Simulink.

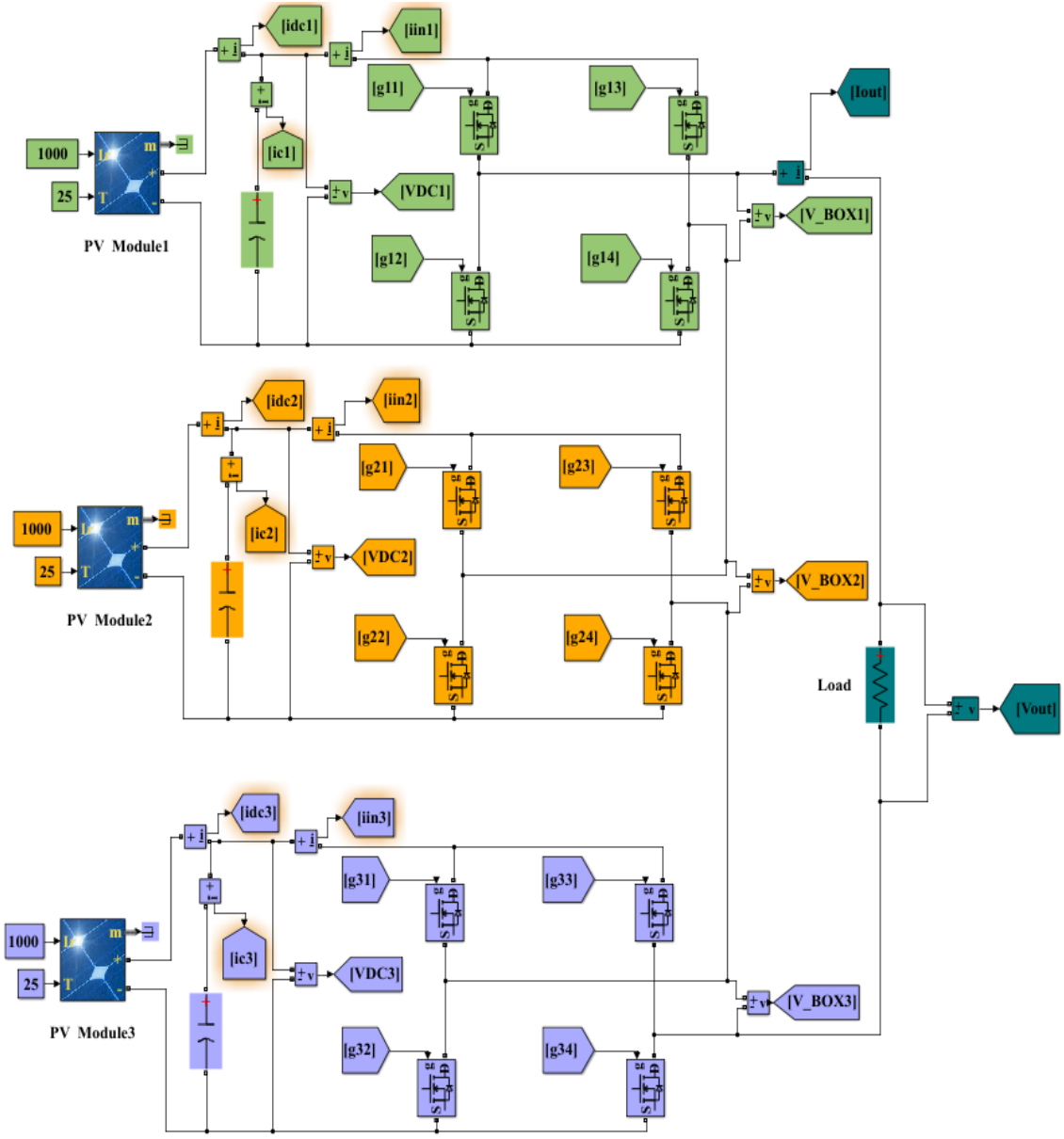


Figure 5.2: Block diagram of Cascaded Multilevel Inveter with PV modules as source developed in MATLAB/Simulink.

5.2.1 Model of PV array

In MATLAB Simulink a block named PV array represents an array of PV modules. This block allows modeling of predetermined modules accessible from NREL system advisor model and also user-defined modules. First input is irradiance of Sun, which has been provide by a constant block of 1000, in W/m^2. Second input is temperature

of cell, in deg.C kept to be 25 degrees. For this simulation Bosch Solar Energy c-Si M60 NA42117 250W PV array is selected. The goal is to extract maximum power from each panel, therefore, each H-bridge is connected with single PV , and in array data, parallel strings and series-connected module per string is to be put one.

The PV panel data specified in the block parameters image (figure 5.3) are — Maximum Power (W) 250, Cells per module (Ncell) 60, Open Circuit Voltage (Voc) 37.9, Short Circuit Current (Isc) 8.82 A, Maximum power Point Voltage (Vmp) 30.1 V, and Maximum power Point Current (Imp) 8.25 A. The operating point at which panel can provide maximum power, with Vmp and Imp is displayed in figure 5.4. It is important to note that the plot in figure is true for irradiation 1000 W/m^2.

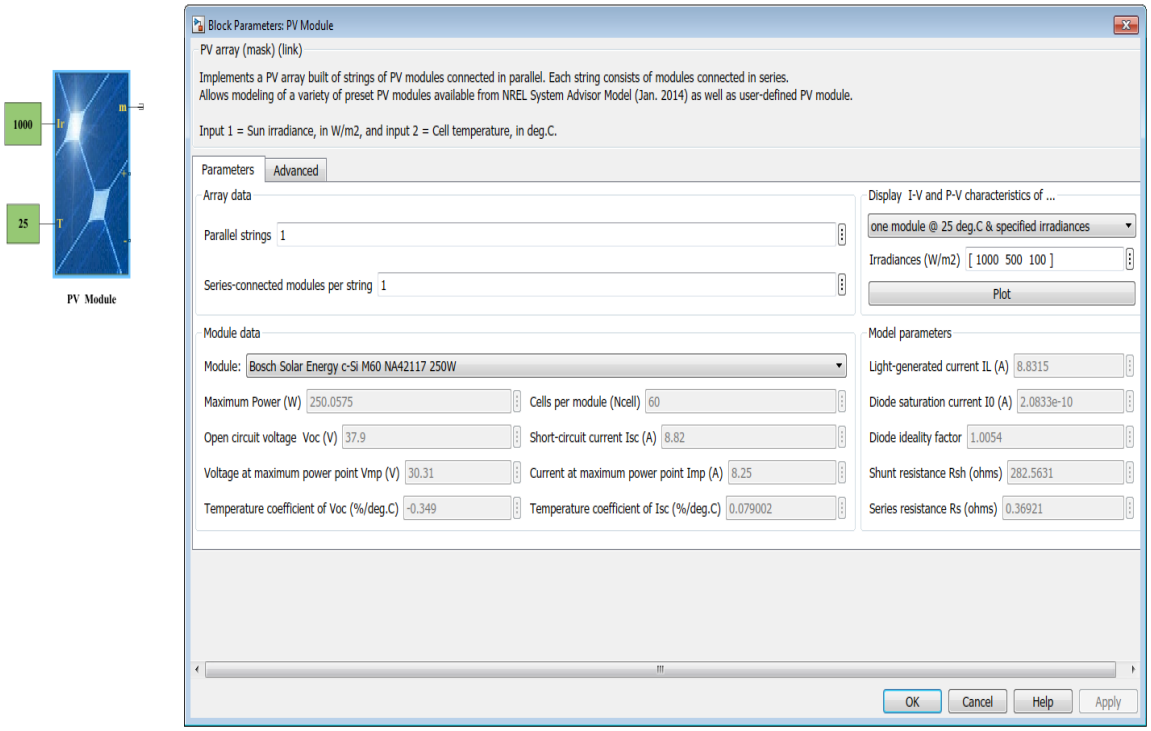


Figure 5.3: Picture showing PV array block and it parameters.

The maximum power that can be produced by a PV Module depends on the solar irradiance. To perform analysis on the simulation model two case studies are considered, which includes following terms-

1. Percentage Yield (η): Percentage yield is defined as the ratio of actual DC power output of the PV module to the available DC power output for the same case study multiplied by 100.

$$\eta = \frac{PowerExtracted}{PowerAvailable} * 100 \tag{5.1}$$

2. Mean Irradiance (μ): Mean Irradiance is expressed as the average irradiance incident on all the PV modules. For instance, a system consisting of n PV modules with irradiation Ir1, Ir2,..., Irn on PV modules, respectively. Mean irradiance of the solar system can be written in the form of equation 5.2

$$\mu = \frac{\sum_{i=1}^{n} Iri}{n} \tag{5.2}$$

3. Coefficient of Variation (λ): Coefficient of variation is described as the ratio of standard deviation of irradiance to the mean of irradiance, where σ stands for standard deviation. This parameter quantifies the divergence of irradiance from the mean value. Coefficient of variation is given by equation5.3 and standard deviation is given by equation 5.4.

$$\lambda = \frac{\sigma}{\mu} \tag{5.3}$$

$$\sigma = \frac{\sqrt{\sum_{i=1}^{n}(Iri - \mu)^2}}{n} \tag{5.4}$$

4. Uniform Irradiance: The system is said to be working in uniform irradiance,if the incident light on all the PV panels have the same irradiance. Coefficient of variation for uniform irradiance is 0 as σ becomes zero when value of μ for uniform irradiation is same as Iri. The coefficient of variation is zero for uniform irradiance.

5. Non-Uniform Irradiance: The system is said to be functioning in non-uniform irradiance, when the irradiance of the light incident on the all the PV panels vary. Coefficient of variation for nonuniform irradiance is any value between 0 and 1.

Figure 5.4 and figure 5.5 represent I-V and P-V graphs, for uniform and non - uniform irradiance case studies, respectively. It is visible from I-V curves that higher the value of irradiance, greater is the value of the corresponding short circuit current. From the P-V curves it can be seen that higher the value of irradiance larger is the maximum power, that can be extracted.

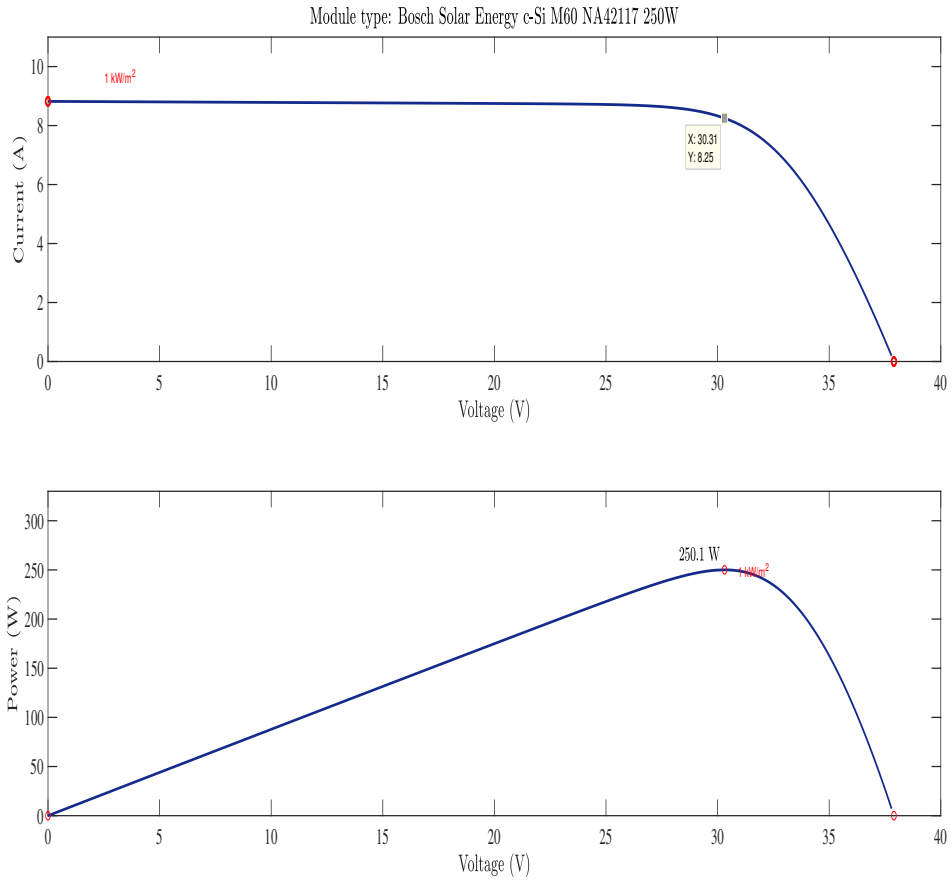


Figure 5.4: PV and IV characteristics of solar panel utilized in simulation showing the maximum power point tracking plot for 1KW/m^2.

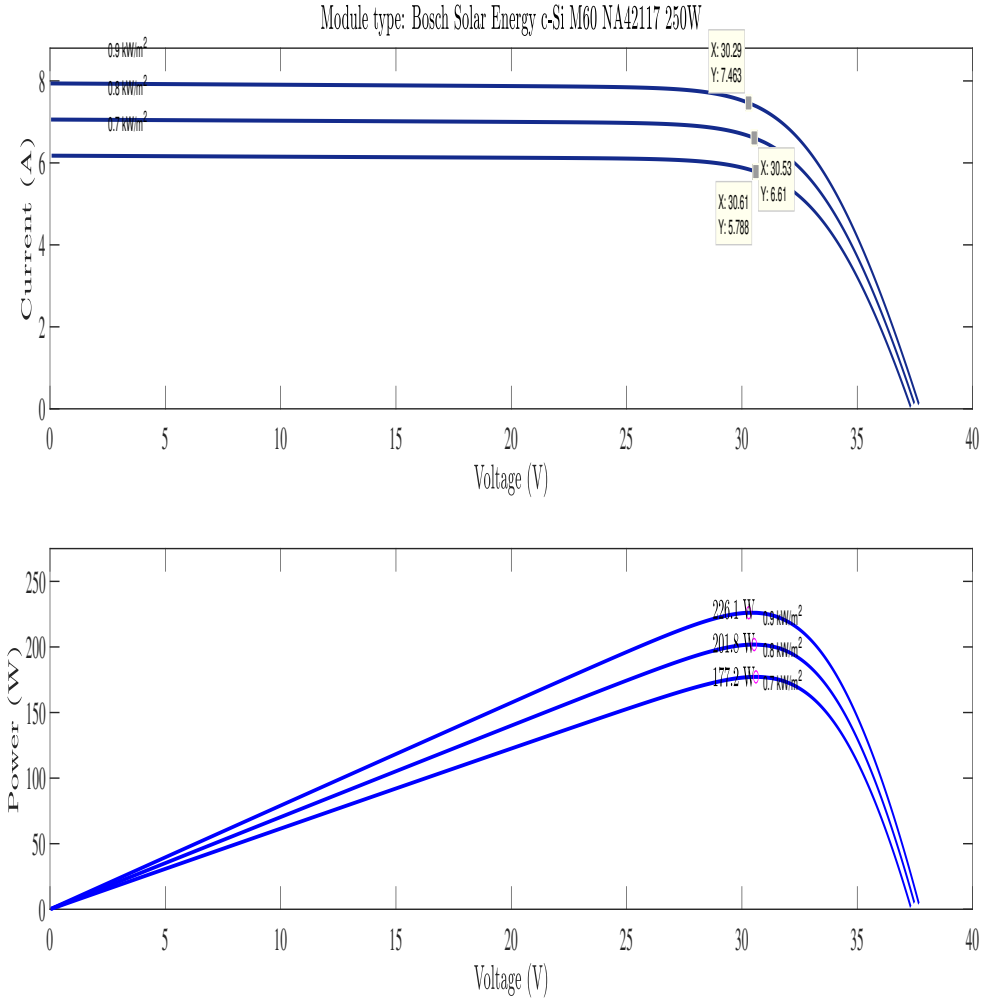


Figure 5.5: PV and IV characteristic of solar panel utilized in simulation with irradiance of incident light on PV module 1, PV module 2,and PV module 3 are 0.9KW/m^2, 0.8KW/m^2, and 0.7KW/m^2.

Table 5.1 shows change in the maximum power point voltage, current, and extracted maximum power, from PV panels with the change in irradiance of the incident light on all the PV panels

Table 5.1: Maximum power point voltage, current, and extracted maximum power from PV Modules for different irradiance.

Irradiation (W/m^2)	V_{MPP} (V)	I_{MPP} (A)	P_{MPP} (W)
1000	30.31	8.25	250.1
900	30.29	7.46	226.1
800	30.53	6.61	201.8
700	30.61	5.78	177.2

All the PV panels are provided with uniform irradiance of 1000 W/m_2 for case study 1, I-V and P-V graphs are same for all the panels as shown in figure 5.4. Case study 2 is based on non-uniform irradiation, irradiance of 900, 800, and 700 are provided to PV panel 1, 2,and 3, respectively. I-V and P-V characteristics of all the panels are distinct in this case study as shown in figure5.5. Mean irradiance and coefficient values are calculated using equation 5.2 and equation 5.3, and the parameters for two case studies are included in table 5.2.

Table 5.2: Case Studies to perform simulation for different sorting scenarios.

Case Study	Coefficient	Mean Irradiance	Standard deviation	Total Available Power
1	0	1000	0	750
2	0.1	800	81.65	605

5.2.2 Distributed Control Modulation Strategy

Distributed controls is implemented in simulations by developing three subsystems, where sorted staircase logic is processed. Figure 5.6 shows three subsystems titled as controller 1, controller 2, and controller 3. Voltages VDC1, VDC2, and VDC3 are transmitted to all the controllers, and sorted staircase strategy as explained in section 3.4 has been redesigned in this controller blocks. Each controller block generates four

gate pulses for their respective H-bridge power cells, triggering the MOSFETs ON at appropriate switching angle.

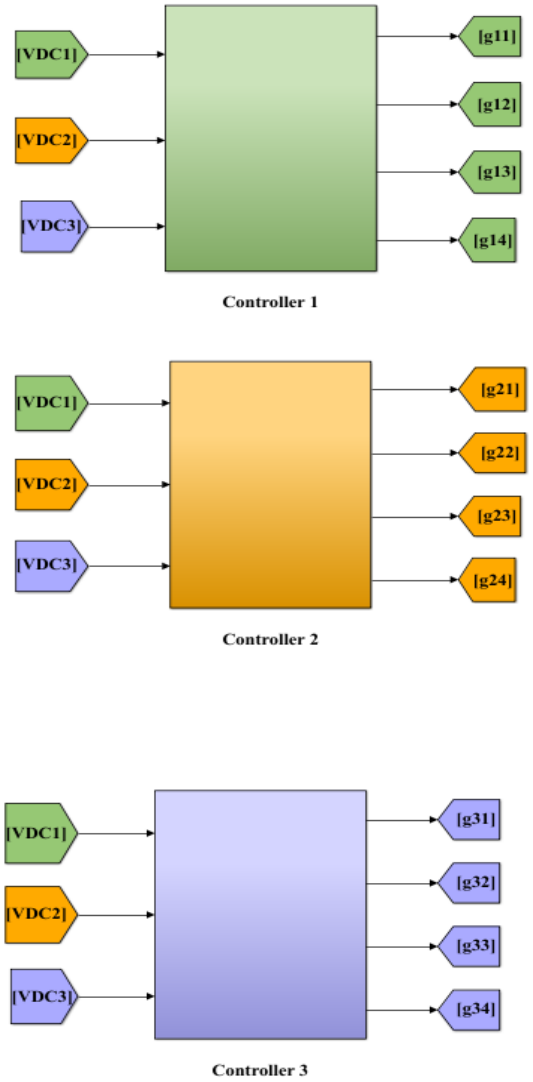


Figure 5.6: Distributed controller blocks for sorted staircase strategy in simulation.

Internal view of each controller subsystem is similar; however, theta issued in each controllers' pulse generator block is of respective H-bridge power cell (Box n). For instance, as can be seen from the figure 5.7, which is a subsystem of controller 1, theta1 serves as an input for pulse generator of H-bridge power cell (Box 1). Similarly, theta2 in controller 2 and theta3 in controller 3. Controllers also included following blocks, labeled — trigger the sorting, sorting DC voltages in descending order, switching

angle calculation, and pulse generator—. Trigger the sorting is utilized basically as a block where triggering pulse can be set for various sorting. In this developed model trigger for sorting was performed at three different cycles named as, full cycle (60Hz), half cycle (120Hz), and quarter cycle (240Hz). Sorting DC voltage block receives all the measured DC voltages, and sorting can be performed as per characteristic set (i.e., sort in ascending or descending order). In this case, it has been set to descending order with value and index as outputs of the block. Thereby, block gives the sorted DC voltages and also index of respective H-bridge power cell. An example of sorting values are displayed in scope of figure 5.7 vdcunsorted voltage panel wise are 30.1 V, 29.9 V, and 35.15 V, corresponding to VDC1, VDC2, and VDC3, respectively. After sorting, the values are in descending order 35.15 V, 30.1 V,and 29.9 V, along-with respective H-bridge power cells index 3, 1, and 2. The sorted DC voltage values and index are supplied to MATLAB function block, where calculation of switching angle is performed. The code of function block is presented in figure 5.8. The outputs of this angle calculation block are instant values at which switching of inverter power cells must be performed.

The pulse generator block for all controllers function on same logic, as explained in Chapter4, subsection 4.5.2 about output compare. In figure 5.9, the simplified schematic of logic utilized to generate gate pulses for first inverter module is displayed. The input one is saw-tooth waveform of period 60Hz making the saw-tooth rise from 0 s to 0.01666 s. The input two is angle in degrees which is required to be converted into time. The full cycle is of 360 degrees, hence, to convert into time theta must be divided by 360 and multiplied by 0.01666sec (60 Hz). Pulse is started when the angle converted in time value is equal to that of saw-tooth time value, duration of each pulse is 0.00833 second. This pulse is labeled, G11 and not of it is labelled, G12. gFurther, gate pulse labeled, G13 is 180-theta1, and not of it is labelled, G14. Similarly, gate pulses of all the controller blocks are generated.

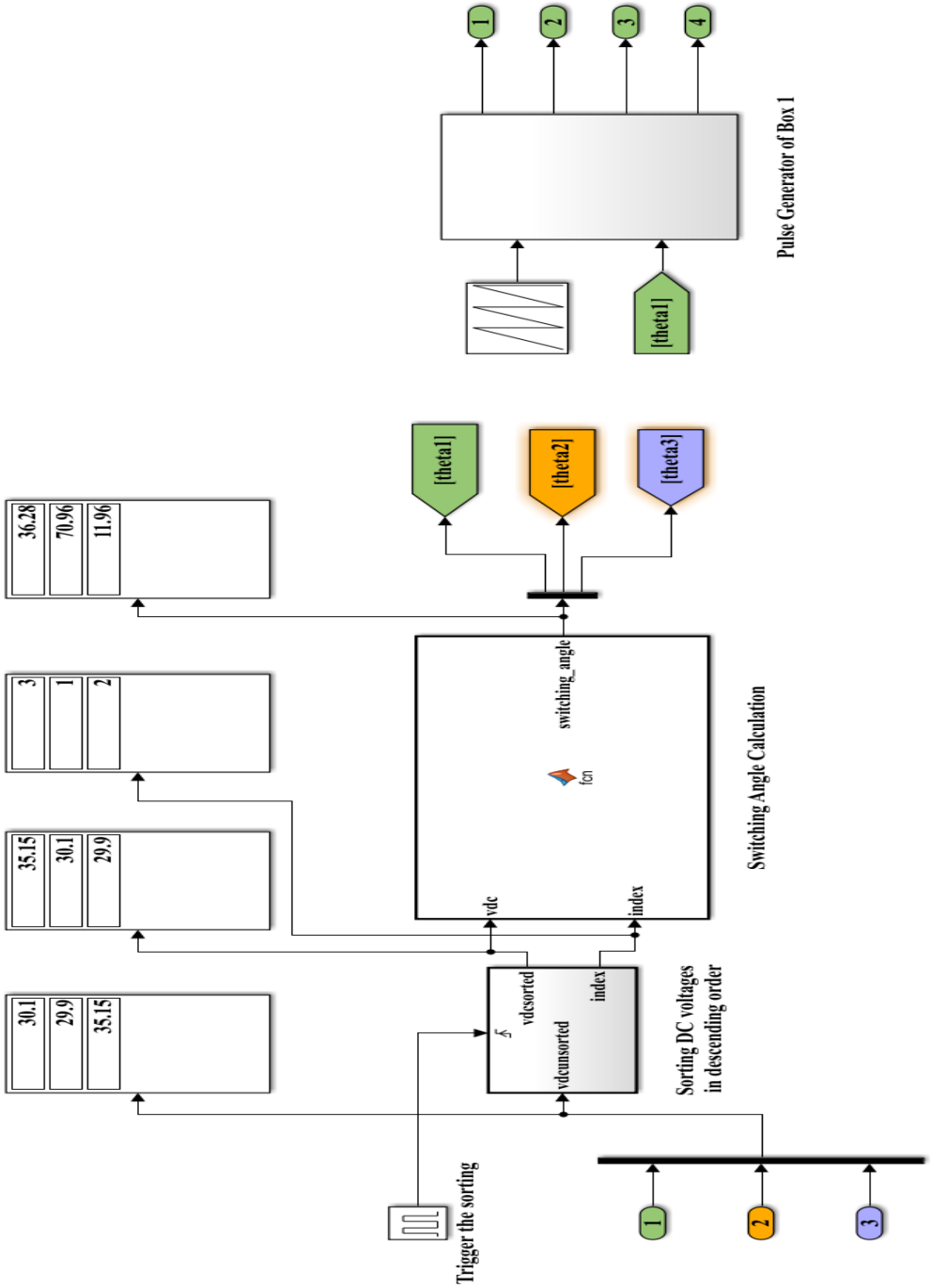


Figure 5.7: A picture describing the controls implemented in subsystem of each distributed controller.

Controller 1/Switching Angle Calculation*

```
function switching_angle  = fcn (vdc,index)
voltage = zeros(1,3)';
voltage = vdc;
temp = zeros(1,3)';
sum=0;
Vpk=60*sqrt(2);
if any(index) == 0
    ij = cast(ones(1,3)', 'like', index);
else
    ij = index;
end
theta=temp;

 for i=1:1:3
            theta(ij(i))=asin((sum+(voltage(i)/2))/Vpk)*180/3.14159;
            sum=sum+vdc(i);
 end
switching_angle=theta

```

Figure 5.8: A picture of the code inside MATLAB function block.

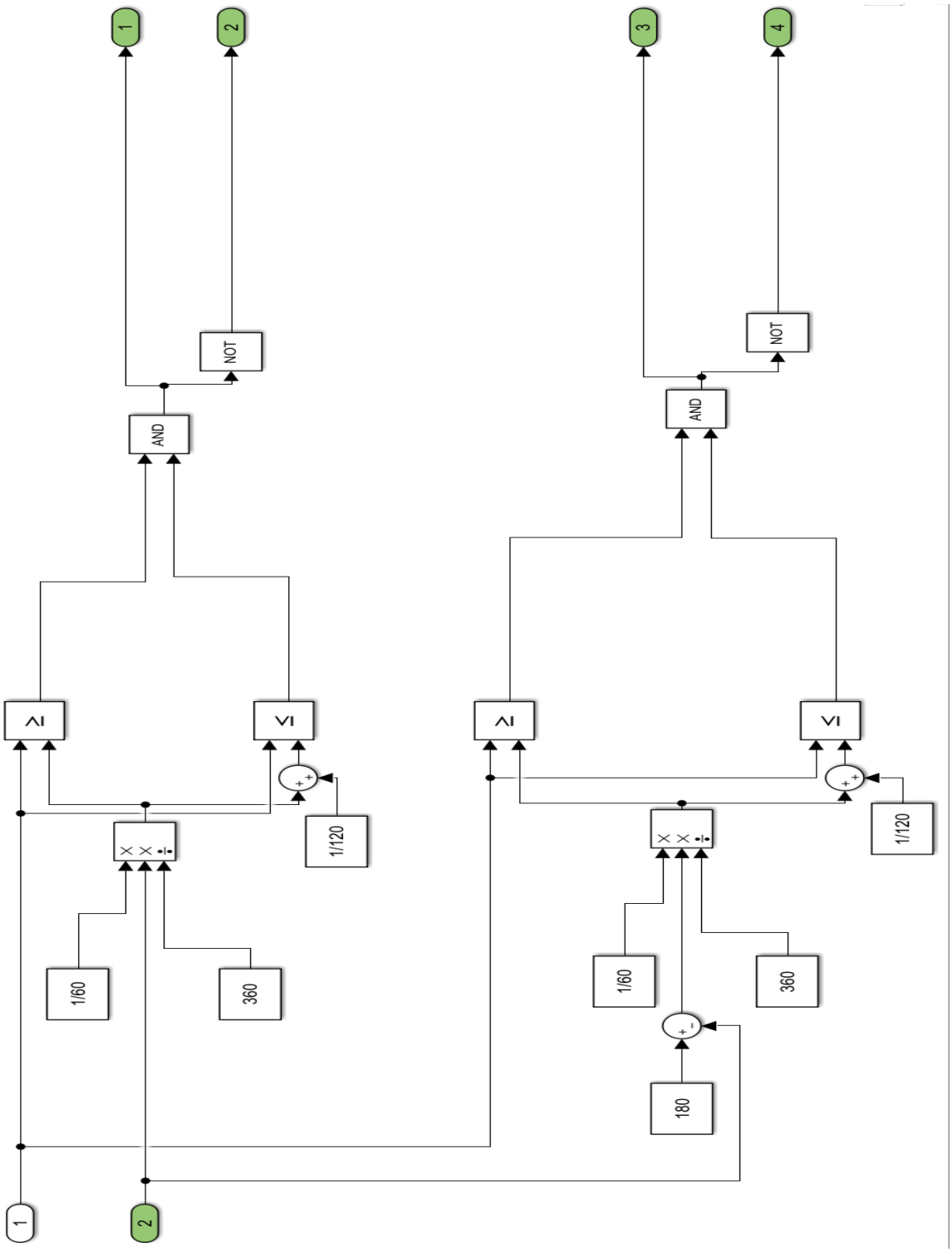


Figure 5.9: Simplified block schematic showing subsystem of pulse generator and its logic inside each controller.

5.3 Simulation Results

As presented with the help of flowchart diagram (figure 3.13) in Chapter 3, the switching angle is calculated and triggered by comparing V_{ref} and V_{DC} value. From the plot in figure 5.10 triggering points can be distinguished, the voltage crossing the reference sinusoidal voltage in following order VDC1, VDC2, and VDC3. Intersecting point of Vref and calculated switching points are marked in the picture. Green for first H-bridge box with DC voltage VDC1, orange represents second H-bridge box with DC voltage VDC2, and violet represents third H-bridge box with DC voltage VDC3. The reference sinusoidal voltage is of 60 V rms, and as it is clearly indicated the output voltage peak and reference voltage peak are at same value 84.84 volts. CHB-MLI inverter is connected with load of 750 W in case study 1 and load of 605 W in case study 2. Figure 5.11 shows CHB-MLI seven-level voltage and current output waveforms.

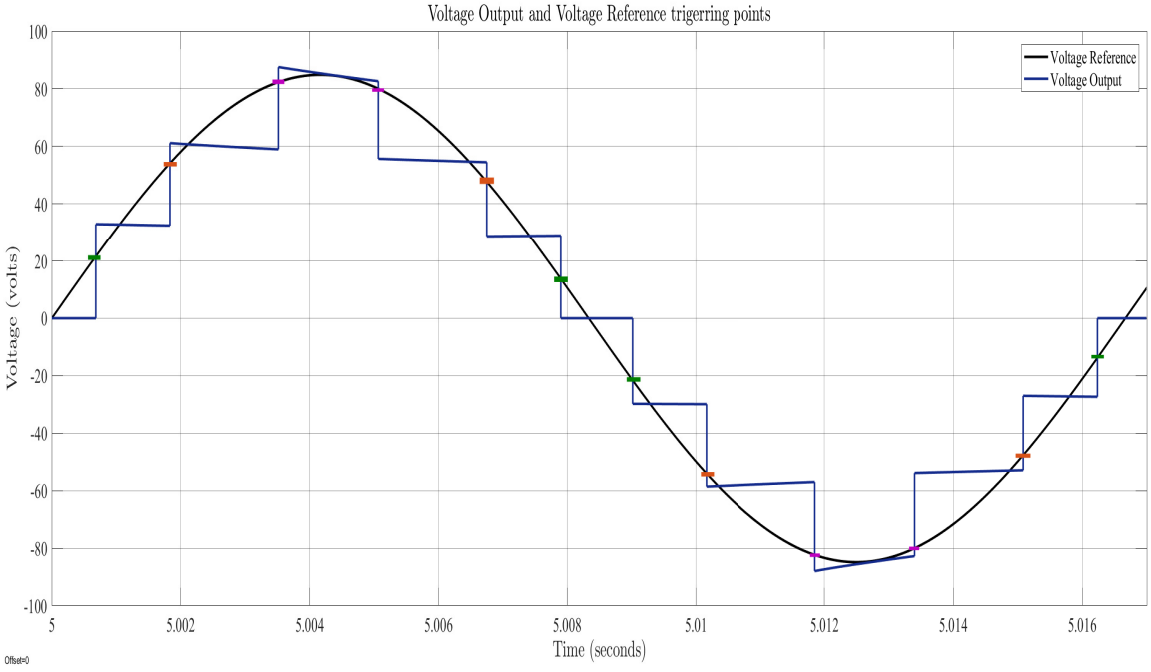


Figure 5.10: Plot of reference voltage and synthesized quasi square wave with sorted staircase modulation strategy.

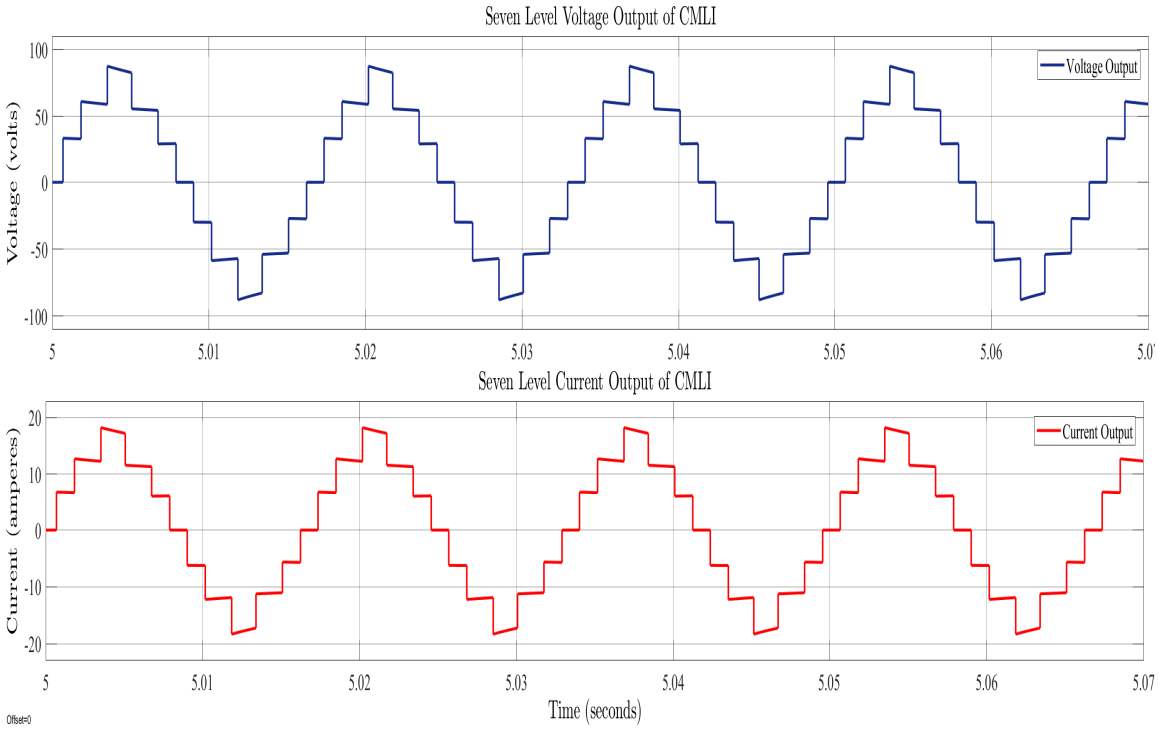


Figure 5.11: Seven-level quasi square wave voltage and current output of cascaded H-bridge multilevel inverter connected with a load of 750 W.

As explained in Chapter 3, about various switching states and operating principle of series connected H-bridge, using similar approach the output in figure 5.12 is synthesized. All the boxes are color coded and colors are resembled in legend box of the waveforms. The simulation is run for 10 s but for consistency in analysis all the outputs are plotted in time scale of 5.0 s to 5.07 s. As from the image it can be clearly understood in the time span of 5.0 s to 5.017 s VDC3 $>$ VDC1$>$ VDC2. Thereby, the two terminal AC output, where first stair is of Box 3, second of Box 1 and third of Box 2.

The H-bridge power cell with highest voltage generates first quasi square wave, PV panel connected to H-bridge generating quasi square wave output at the bottom of staircase will also supply maximum current to the system, delivering maximum power for that particular sorting cycle. It can be observed from the figure 5.13 that the current flow corresponding to highest voltage module exists for seven levels, second

highest has five levels, and lowest one has three levels. As the current measured at DC terminal, the plot of BOX1, BOX2, and BOX3, current waveforms are DC. Whereas the current waveform at the AC output terminal of CHB-MLI is synthesized square wave AC current.

The waveforms in figure 5.12 and figure 5.13 are combined in the figure 5.14 to get a distinct view of each H-bridge inverter, voltage and current, respectively. Also, their operation in each cycle while tracking the reference voltage and extracting maximum power.

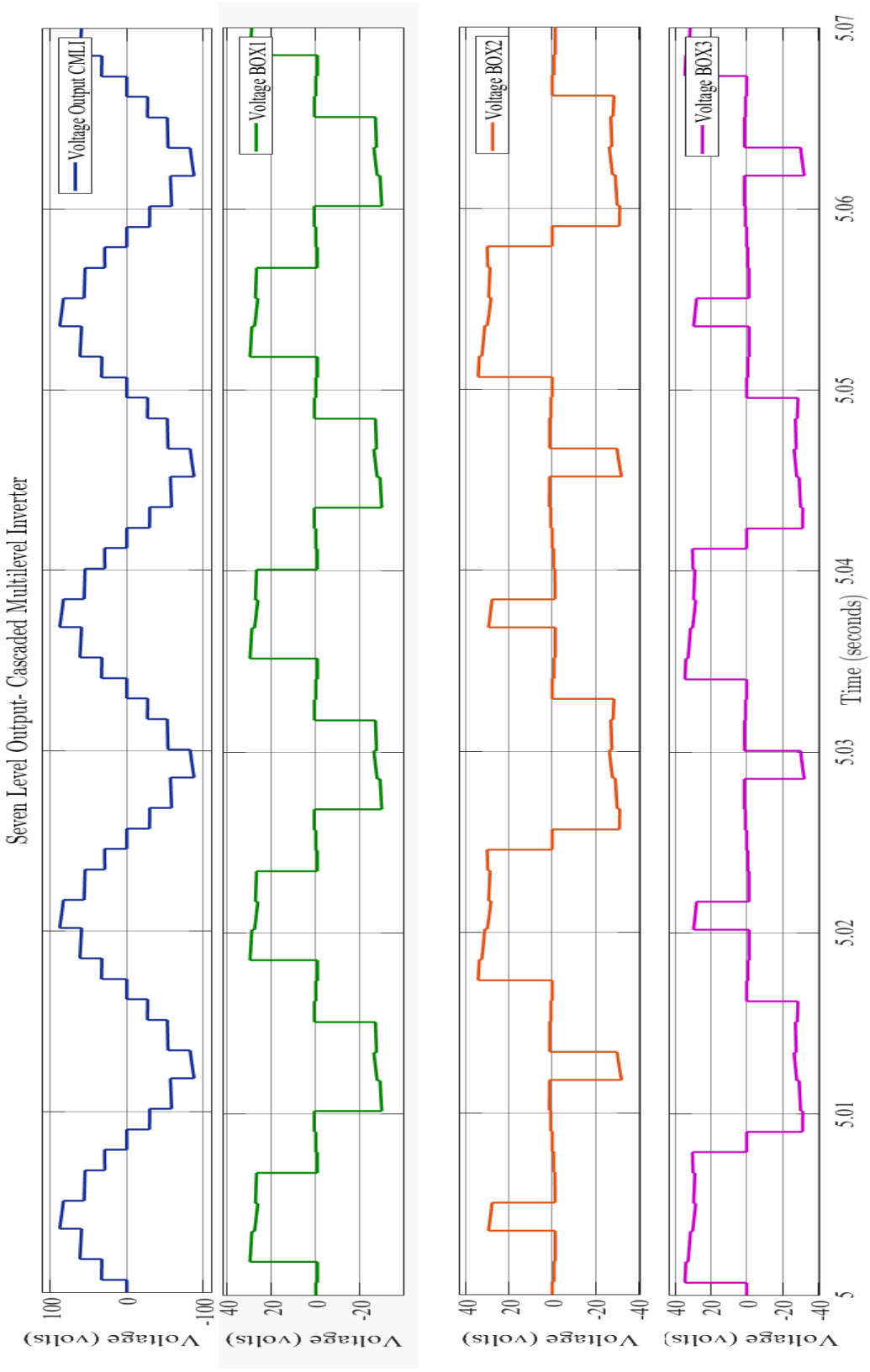


Figure 5.12: Voltage output of each inverter and cascaded H-bridge multi-level voltage output waveform.

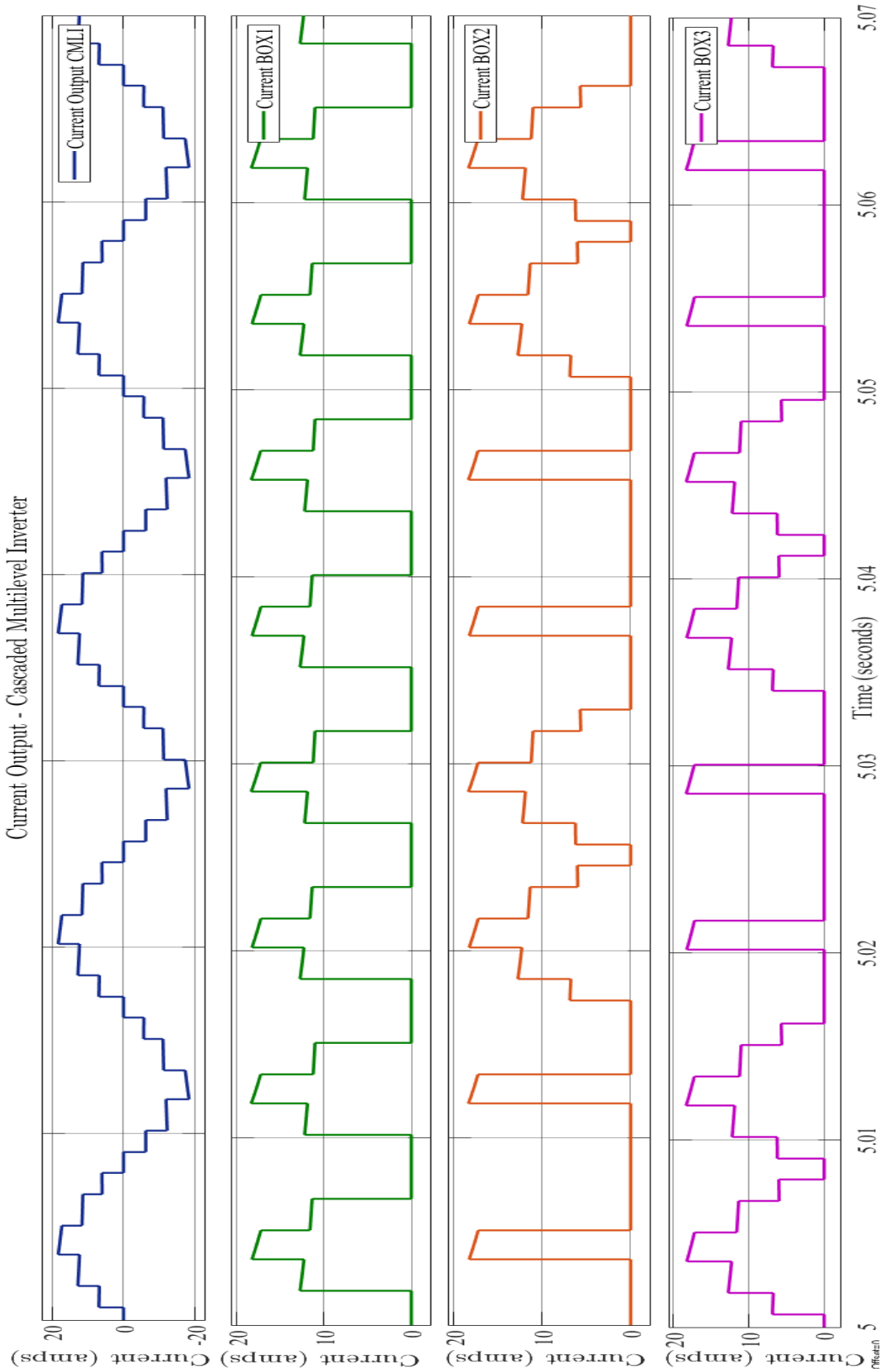


Figure 5.13: Current output of each inverter and cascaded H-bridge multi-level current output waveform.

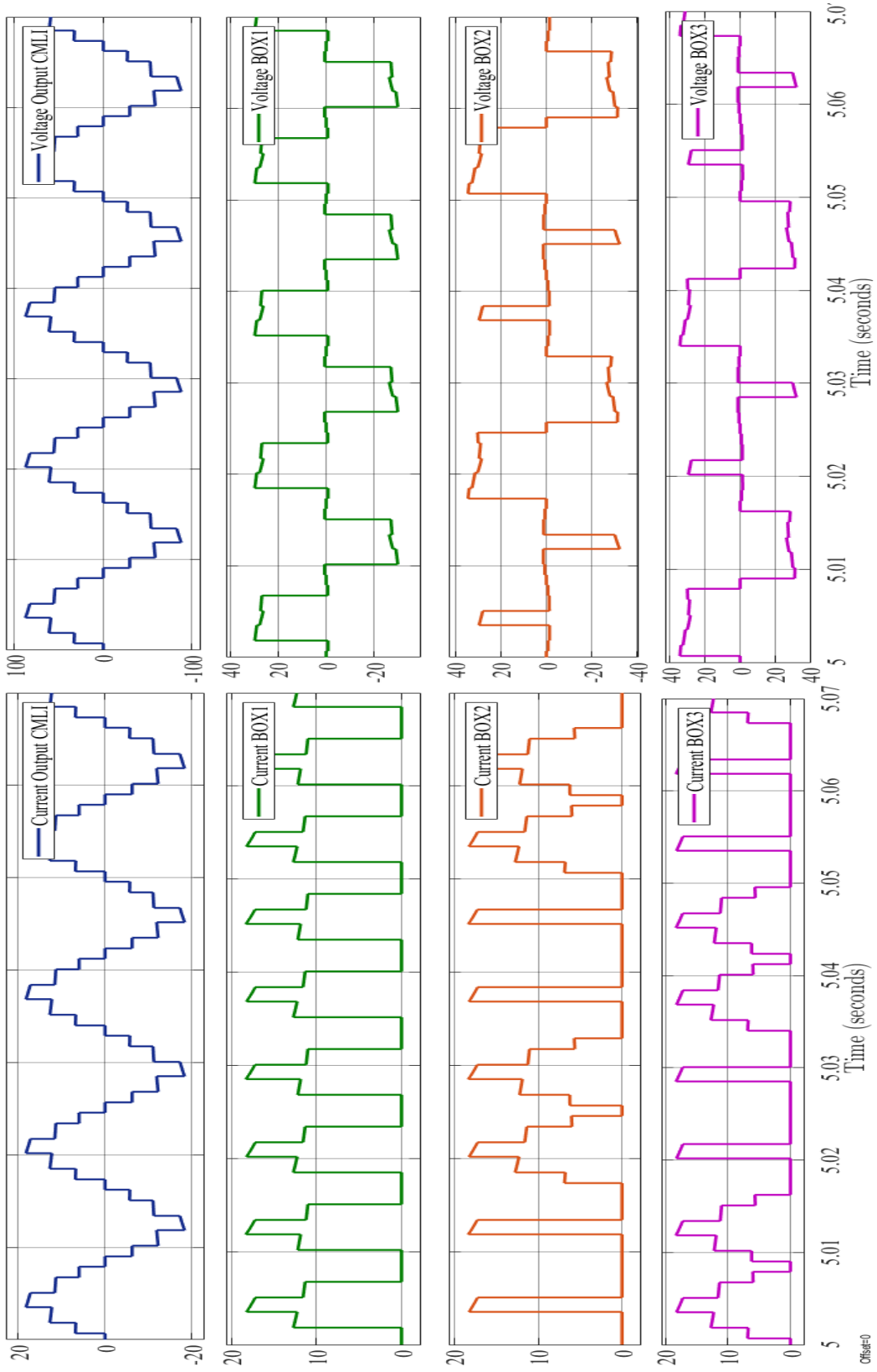


Figure 5.14: Combining the four cycle voltage and current waveforms of seven level CHB-MLI.

In figure 5.15, 5.16, and 5.17, simulation waveforms of each inverter box's voltage at 60 Hz, 120 Hz, and 240 Hz sorting frequency are displayed. The image in which sorting performed after every full cycle clearly depicts that each box operates symmetrically for complete cycle. For instance, from 5.01 sec to 5.018 sec in figure 5.15, Box 3 contributes to the bottom of staircase, Box1 contributes to the second stair and Box 3 contributes to third. Figure 5.16 remarks sorting of voltages after every half cycle, where starting 5.0 sec in first half cycle order of voltages is VDC2 > VDC1 > VDC3, and in the next half cycle order is VDC3 > VDC2 > VDC1. Figure 5.17 follows the same principal of extracting maximum available power for greatest duration, updates the sorting frequency after every quarter cycle. Similar observation for the sorting frequencies of 60 Hz, 120 Hz, and 240 Hz are portrayed with recorded current waveforms in figure 5.18, 5.19, and 5.20.

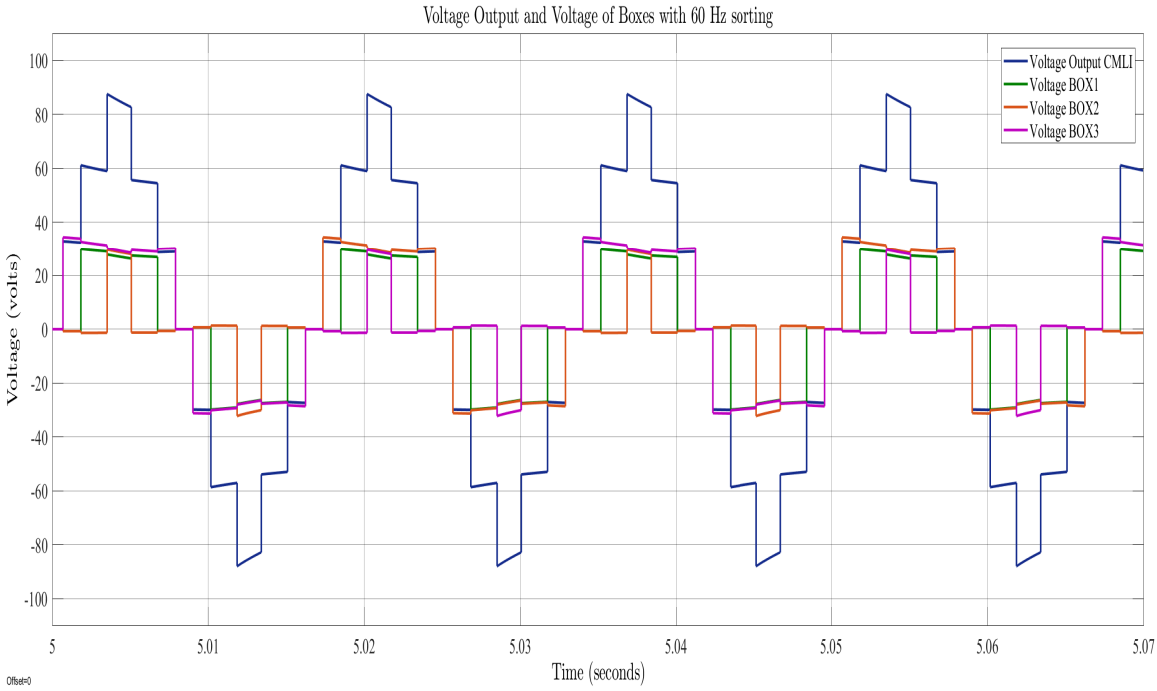


Figure 5.15: Simulation waveform of voltage output of each module and cascaded H-bridge inverter at 60 Hz sorting with irradiance 1000 W/m^2.

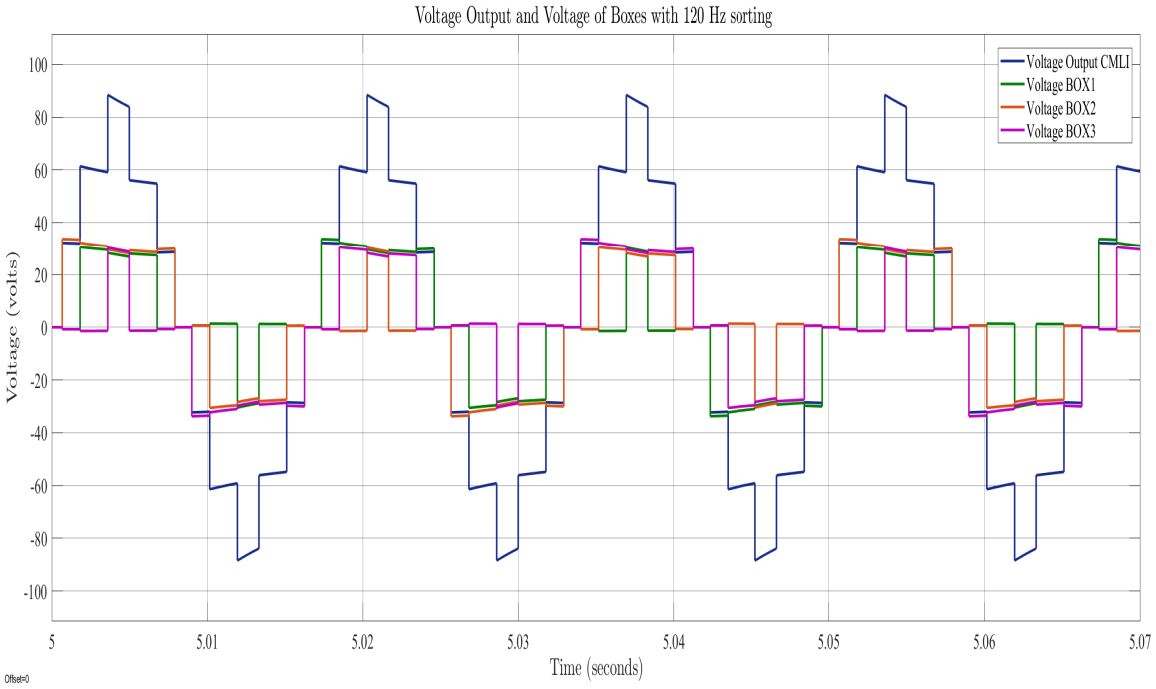


Figure 5.16: Simulation waveform of voltage output of each module and cascaded H-bridge inverter at 120 Hz sorting with irradiance 1000 W/m^2.

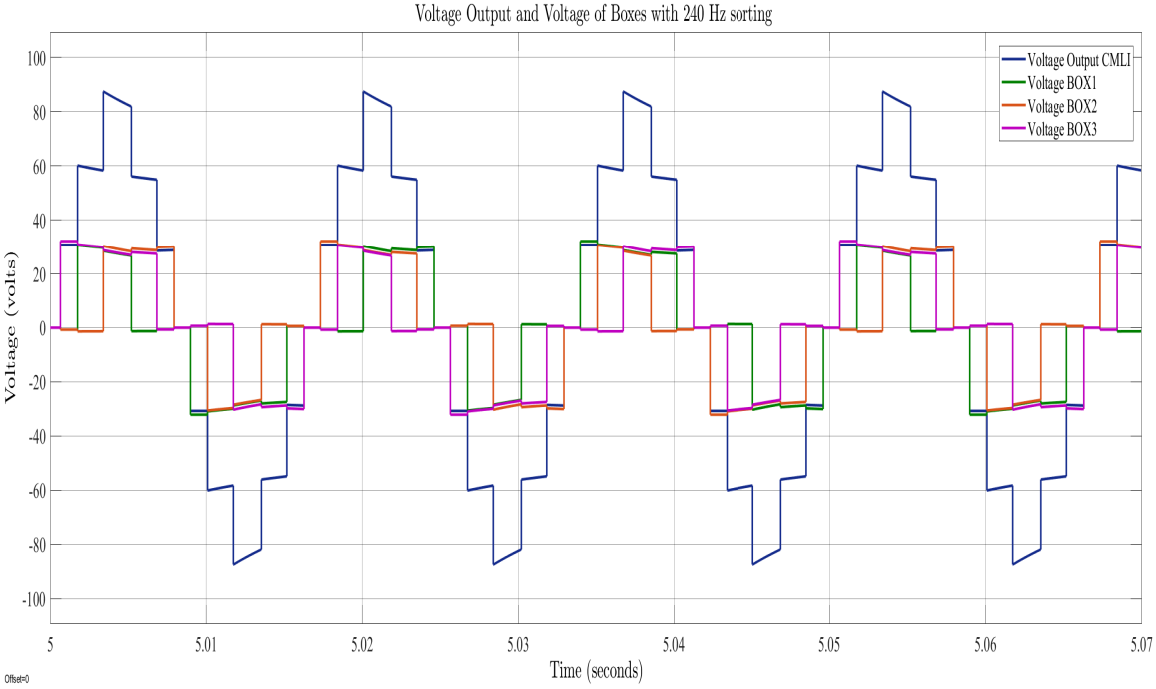


Figure 5.17: Simulation waveform of voltage output of each module and cascaded H-bridge inverter at 240 Hz sorting with irradiance 1000 W/m^2

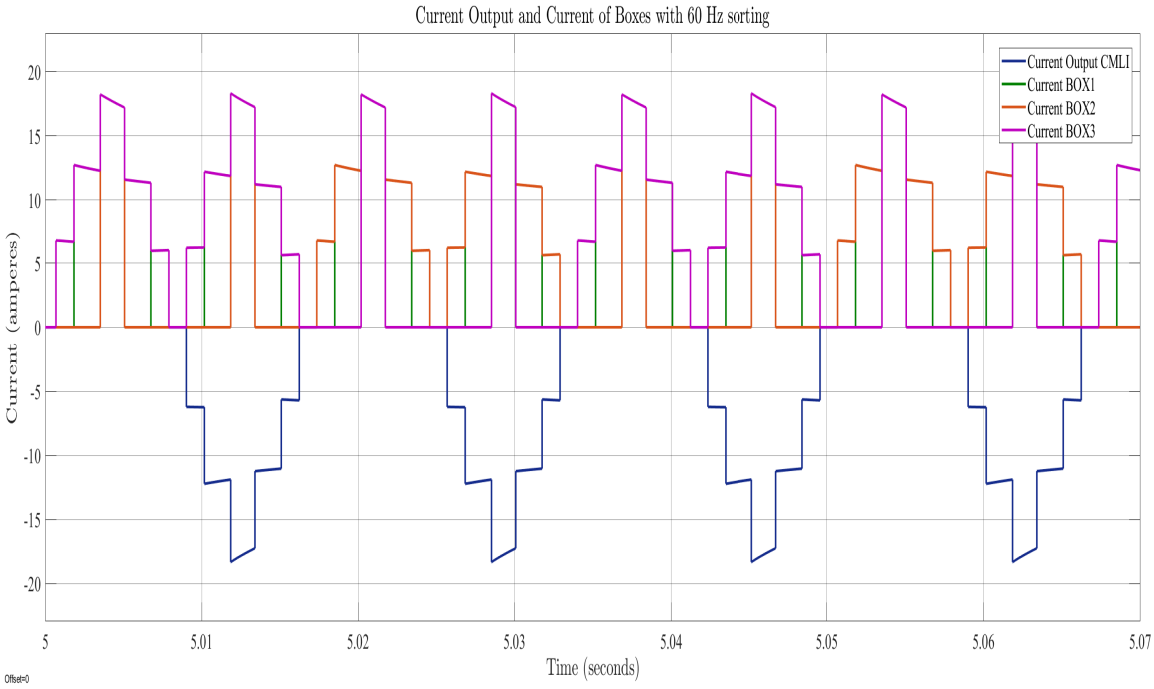


Figure 5.18: Simulation waveform of current output of each module and cascaded H-bridge inverter at 60 Hz sorting with irradiance 1000 W/m^2.

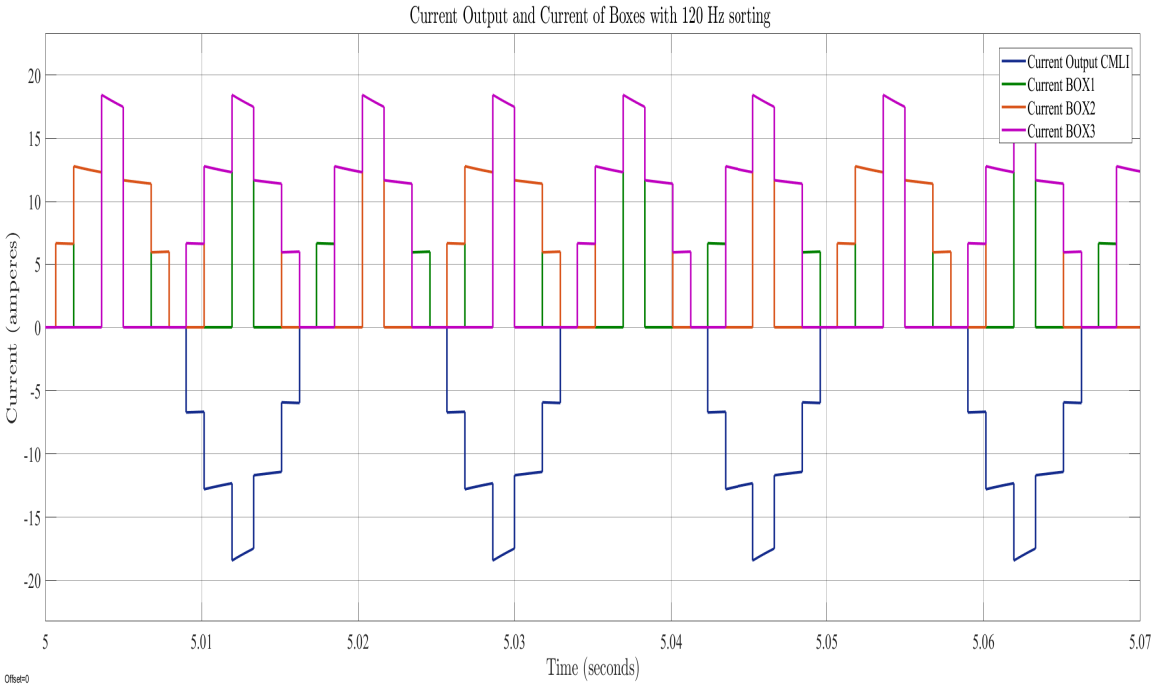


Figure 5.19: Simulation waveform of current output of each module and cascaded H-bridge inverter at 120 Hz sorting with irradiance 1000 W/m^2.

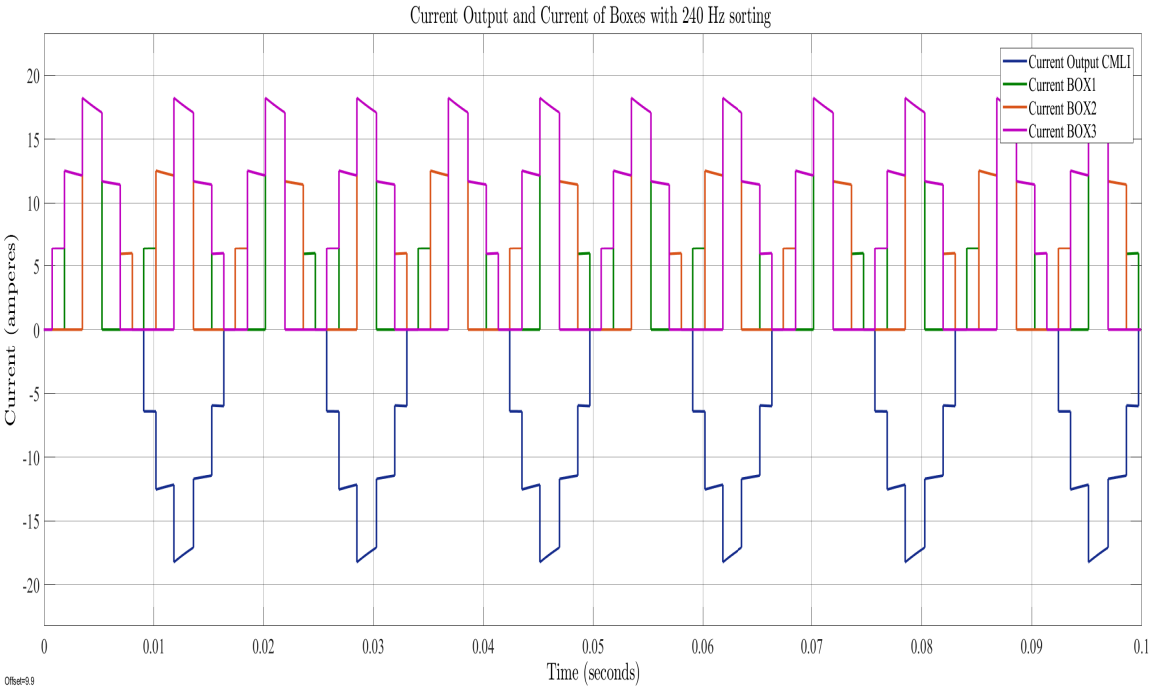


Figure 5.20: Simulation waveform of current output of each module and cascaded H-bridge inverter at 240 Hz sorting with irradiance 1000 W/m^2.

Simulations have been performed for case studies mentioned in table 5.2 for two operating scenarios (sorting DC voltages at half cycle and quarter cycle). Load Connected is of rating 750 W in case study 1 and 605 W in case study 2, which are the maximum available power in respective cases. Figure 5.21 and 5.22 display DC voltage and DC current waveform of all the PV modules. Also, the waveform of extracted power from CHB-MLI and each PV module along with inverter voltage and current output are presented. Figure 5.21 all the modules voltage sorted at 120 Hz and the ripple of all the PV panels are observed to be approximately 5.3 V, performing sort at every quarter cycle reduced the DC voltage ripple approximately to 4 volts as seen in figure 5.22.It is important to note that faster the voltages are sorted the ripple in current is also observed to be decreasing in case study 1. The sorting triggered at half cycle current ripple is 3.7 amps and at quarter cycle current ripple is 2.35 amps. In figure 5.21 the power output is 590 watts at 120 Hz sorting and power extracted from PV panels fluctuate between 240–220 watts, whereas, in figure 5.22, sorting at quar-

ter cycle extracts the maximum power of 625 watt compared to other sorting cycles. Also, the power extracted from PV panels fluctuate between 240.5–236.0 watts.

For case study 2, figure 5.23 and figure5.24, display DC voltage and DC current waveforms of all the PV panels. Also, the waveform of extracted power from CHB-MLI and each PV panel along with inverter voltage and current output are presented. In case study 2, the variation in sorting cycle does not produce any effective changes.

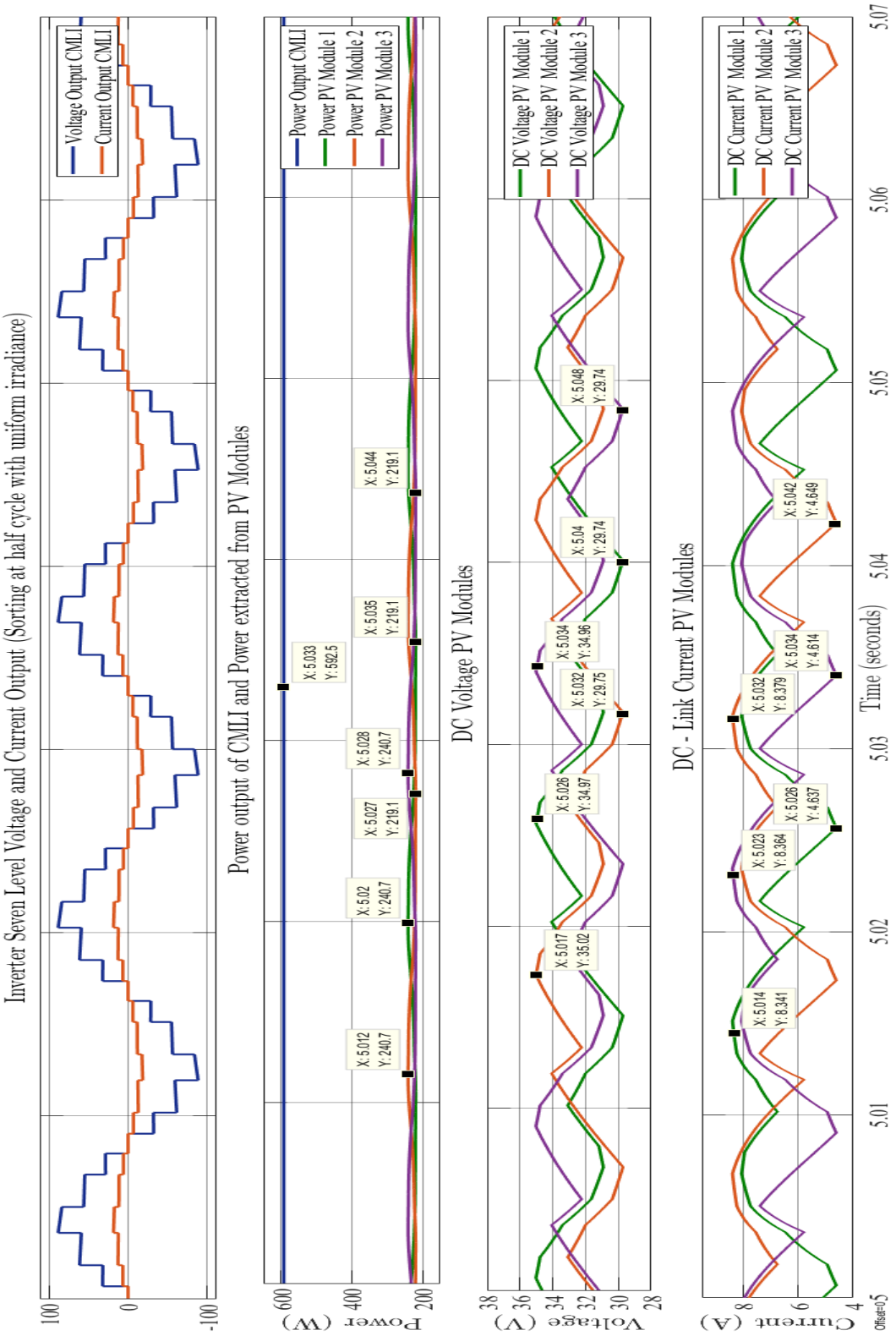


Figure 5.21: Simulation waveforms of Voltage, Current, and Power from PV Panel 1, 2, and 3. Sorting cycle set at 120 Hz (half cycle) under case study 1 with uniform irradiance of 1000 W/m^2.

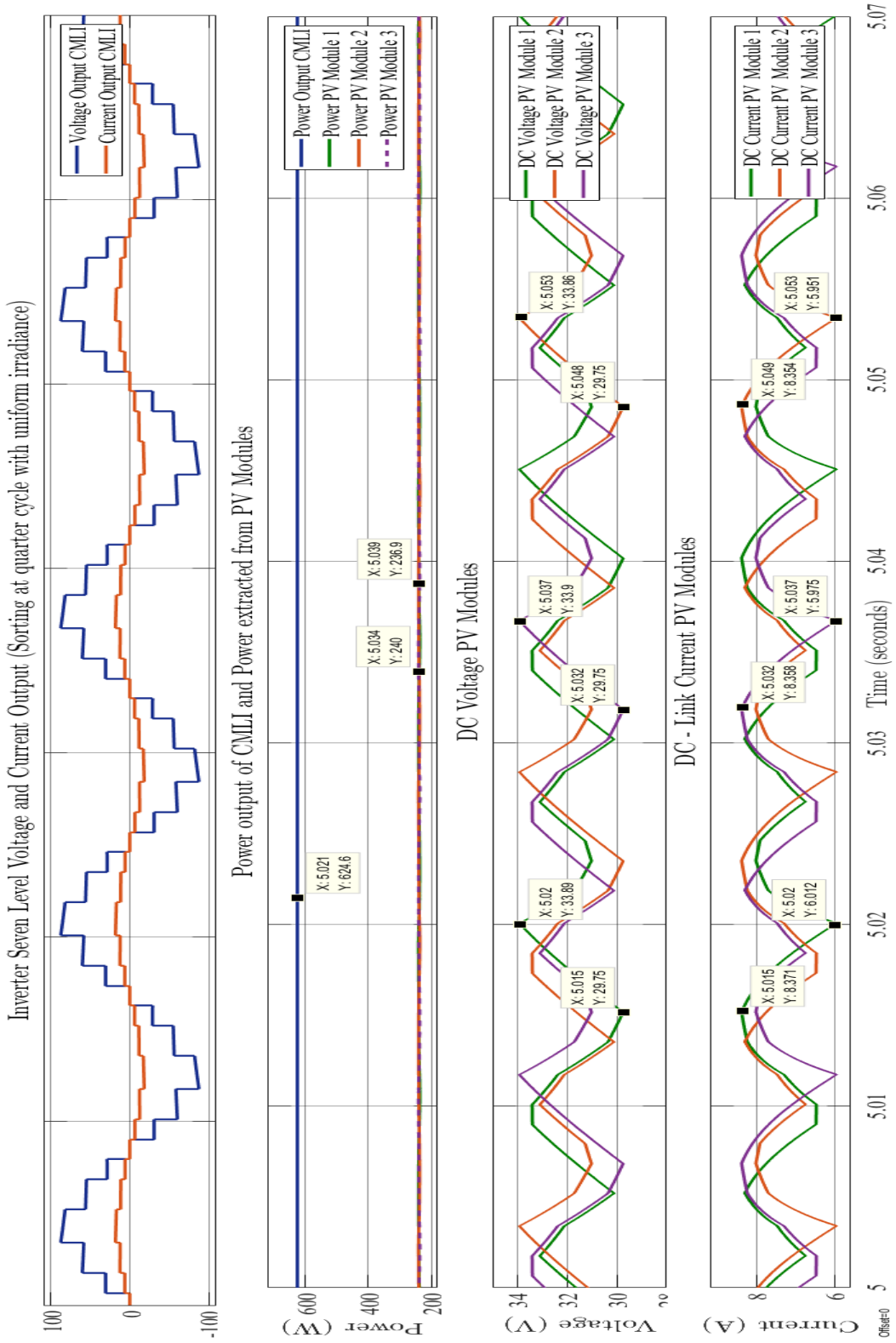


Figure 5.22: Simulation waveforms of Voltage, Current, and Power from PV Panel 1, 2, and 3. Sorting cycle set at 240 Hz (quarter cycle) under case study 1 with uniform irradiance of 1000 W/m^2.

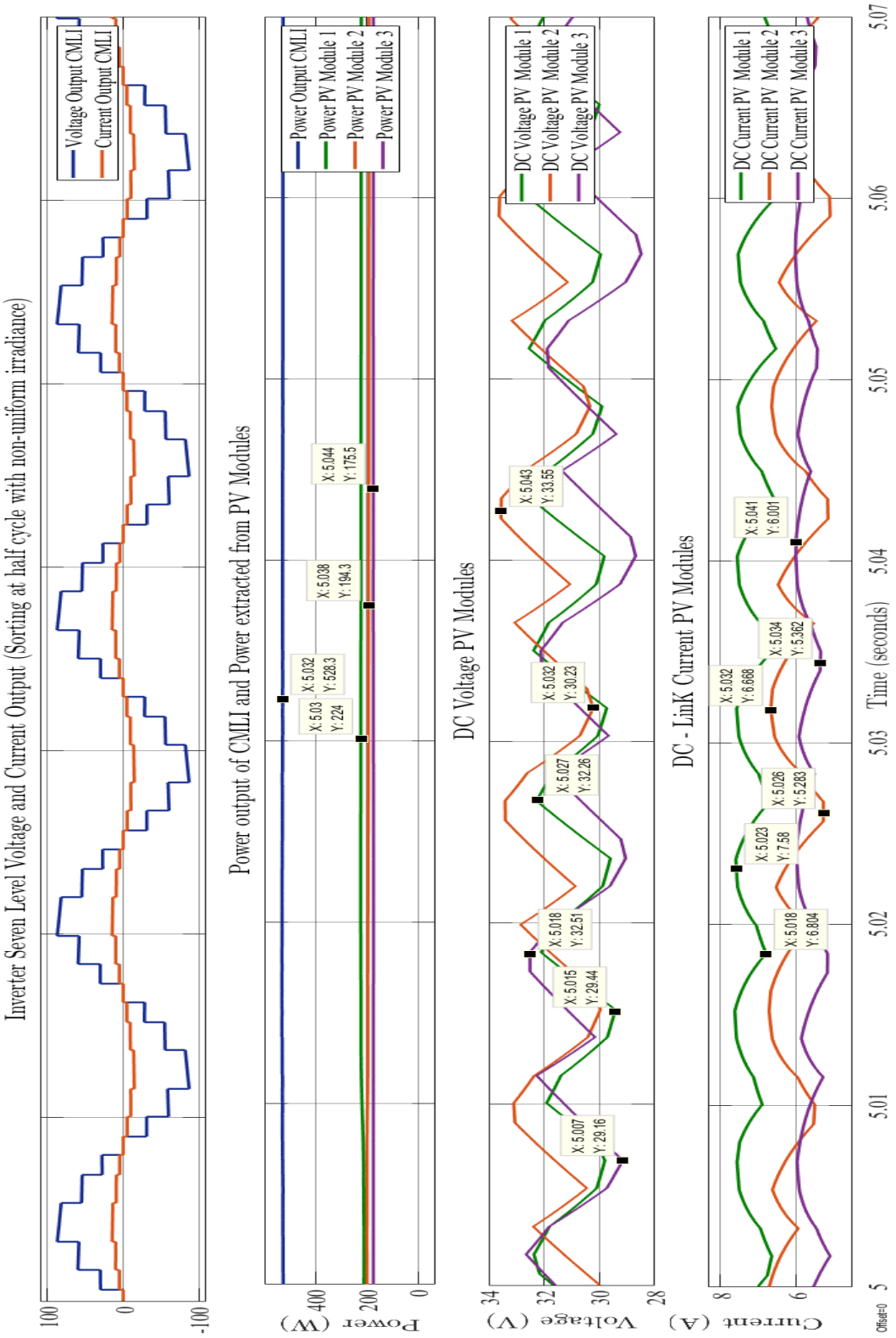


Figure 5.23: Simulation waveforms of Voltage, Current, and Power from PV Panel 1, 2, and 3. Sorting cycle set at 120 Hz (half cycle) under case study 2 with non-uniform mean irradiance of 800 W/m^2.

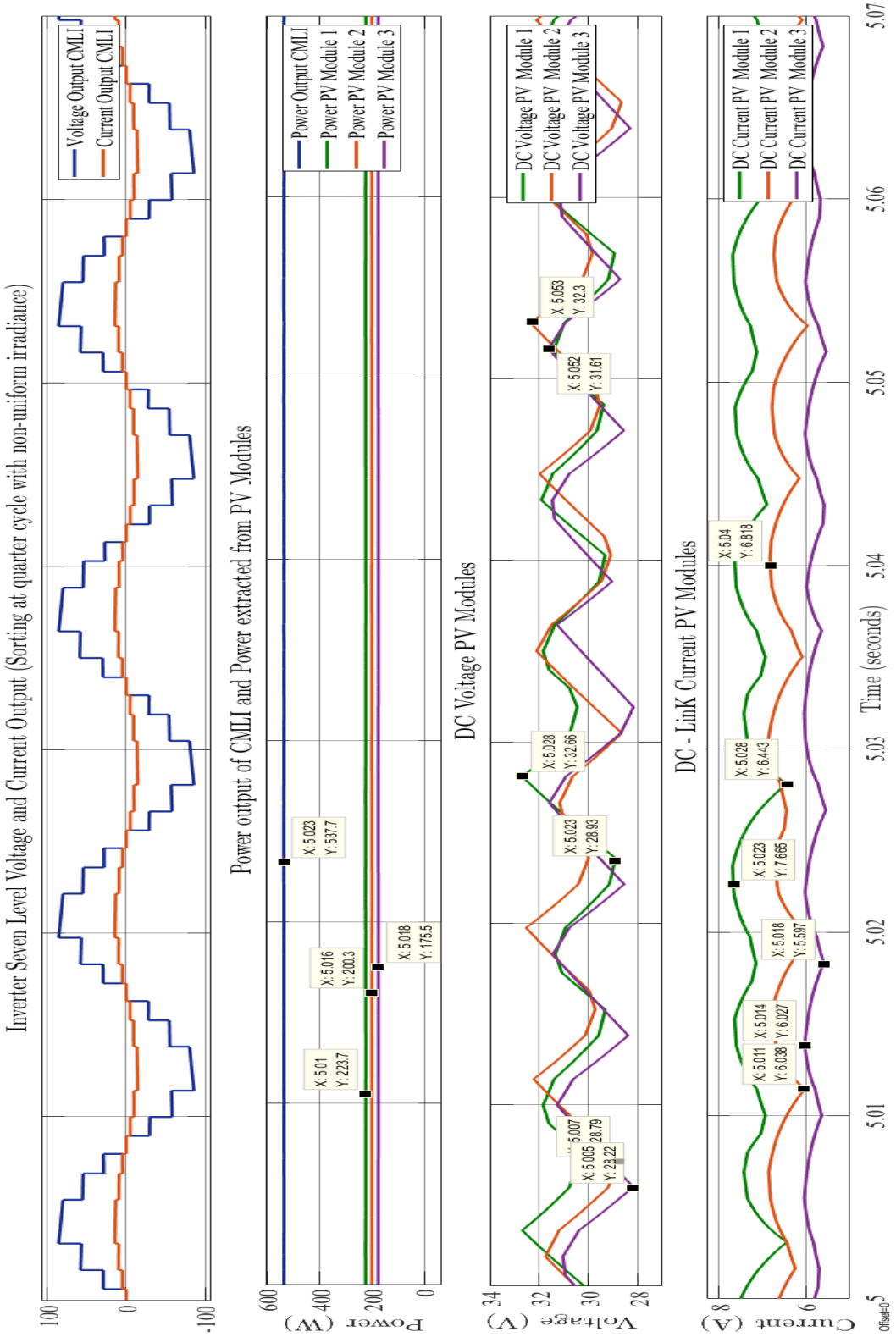


Figure 5.24: Simulation waveforms of Voltage, Current, and Power from PV Panel 1, 2, and 3. Sorting cycle set at 240 Hz (quarter cycle) under case study 2 with non-uniform mean irradiance of 800 W/m^2.

Table 5.3, 5.4, and 5.5, consolidates the observations made from the results obtained through simulation performed on the CHB-MLI model developed in MATLAB, under case study 1

Table 5.3: Extracted Power and Percentage Yield in Case Study 1 for 120 Hz, and 240 Hz sorting scenarios.

Sorting Frequency	Extracted Power	Avaliable Power	Percentage Yield
Half Cycle	592.5	750	79.00
Quarter Cycle	624.6	750	83.28

Table 5.4: DC Voltage Ripple for all PV Modules in Case Study 1 for 120 Hz, and 240 Hz sorting scenarios.

Sorting Frequency	PV Module 1 ΔV1	PV Module 2 ΔV2	PV Module 3 ΔV3
Half Cycle	5.23	5.27	5.22
Quarter Cycle	4.14	4.11	4.15

Table 5.5: DC Current Ripple for all PV Modules in Case Study 1 for 120 Hz, and 240 Hz sorting scenarios.

Sorting Frequency	PV Module 1 ΔI1	PV Module 2 ΔI2	PV Module 3 ΔI3
Half Cycle	3.704	3.73	3.75
Quarter Cycle	2.359	2.403	2.381

Table 5.6, 5.7, and 5.8, puts together observations made from the results obtained through simulation performed on the CHB-MLI model developed in MATLAB, under case study 2.

Table 5.6: Extracted Power and Percentage Yield in Case Study 2 for 120 Hz, and 240 Hz sorting scenarios.

Sorting Cycle	Extracted Power	Avaliable Power	Yield
Half Cycle	528.3	605	87.32
Quarter Cycle	537.7	605	88.88

Table 5.7: DC Voltage Ripple for all PV Modules in Case Study 2 for 120 Hz, and 240 Hz sorting scenarios.

Sorting Frequency	PV Module 1 ΔV1	PV Module 2 ΔV2	PV Module 3 ΔV3
Half Cycle	2.82	3.3	3.35
Quarter Cycle	3.73	3.51	3.39

Table 5.8: DC Current Ripple for all PV Modules in Case Study 1 for 120 Hz, and 240 Hz sorting scenarios.

Sorting Frequency	PV Module 1 ΔI1	PV Module 2 ΔI2	PV Module 3 ΔI3
Half Cycle	0.897	1.432	0.781
Quarter Cycle	1.222	0.78	0.43

CHAPTER 6: EXPERIMENTAL RESULTS

6.1 Overview

This chapter displays experimental results obtained from the laboratory prototype verifying the practical realization of CHB-MLI. In section 6.2, the description of hardware prototype developed in power electronics laboratory is provided. Section 6.3 shows operational experimental result recorded in oscilloscope for cascading and synchronizing inverter H-bridge power cells, implementation of SSCM strategy, and successfully establishing I2C communication with PIC32MX micro-controller. Further, section concludes with the recorded voltage and current waveforms obtained from prototyped CHB-MLI connected with resistive load.

6.2 Experimental Prototype Description

An experimental hardware prototype has been built in laboratory demonstrating distributed controls and communication with multi-level inverter topology. The proposed multi-level inverter has rms voltage of 60 V, and application of 70 W has been constructed and tested. The experimental parameters are displayed in table 6.1.

Table 6.1: Experimental Parameters of Seven Level CHB-MLI.

Voltage	60 V rms
Current	1.2 A rms
Power	70 watt
Resistive Load	50 ohms

A simplified schematic of the experimental prototype is presented in figure 6.1. The system consists of three cascaded H-bridge inverter, which generates seven level out-

put. Each H-bridge comprises of four MOSFETs. The silicon N-channel TK72E12N1 MOSFET has been used in the system, which is rated at 120 V drain-source voltage, and 72 A drain current. Individually, MOSFETs are driven by high speed gate drive optocoupler (HCPL-3180), rated at 2.5 A current.

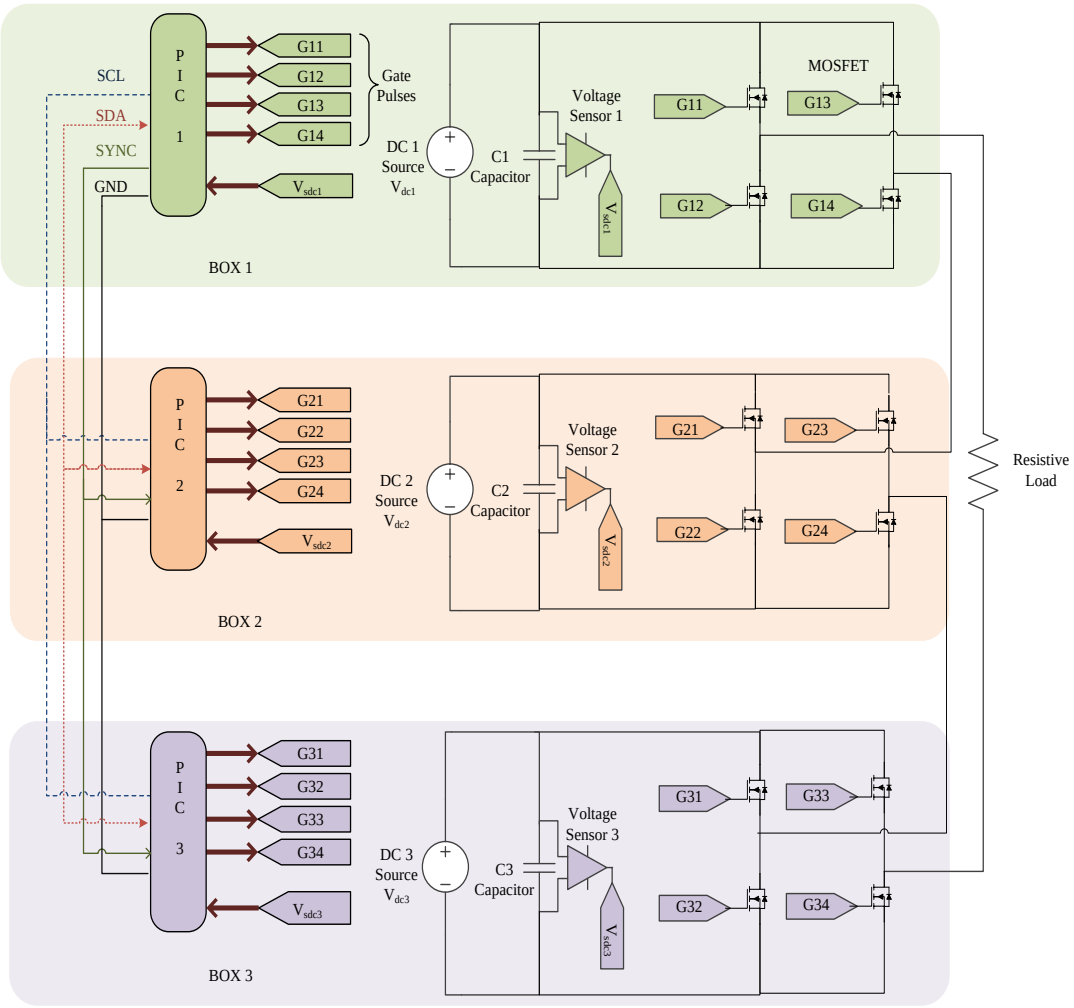


Figure 6.1: Simplified schematic of Cascaded H-bridge Multilevel Inverter with distributed controls and I2C communication protocol.

Microchip's 28 pin DIP package micro-controller (PIC32MX170F256B) is used for analog-to- digital conversion, gate pulse generation, and I2C communication. The operational amplifier circuit has been designed to sense input DC voltage, ranging from

0 V to 50 V, using analog devices AD202JN isolation amplifier with a gain of 17.42. PDS1-S series DC-DC converter are used for supplying power and housekeeping. Gate driver and isolation amplifier are powered with 24-15 V DC-Dc converter, whereas micro-controllers are powered with 24-3.5 V DC-DC converter. The detailed circuit schematic with component description is presented in Chapter 3. The laboratory hardware setup of CHB-MLI connected with load is shown in figure 6.2.

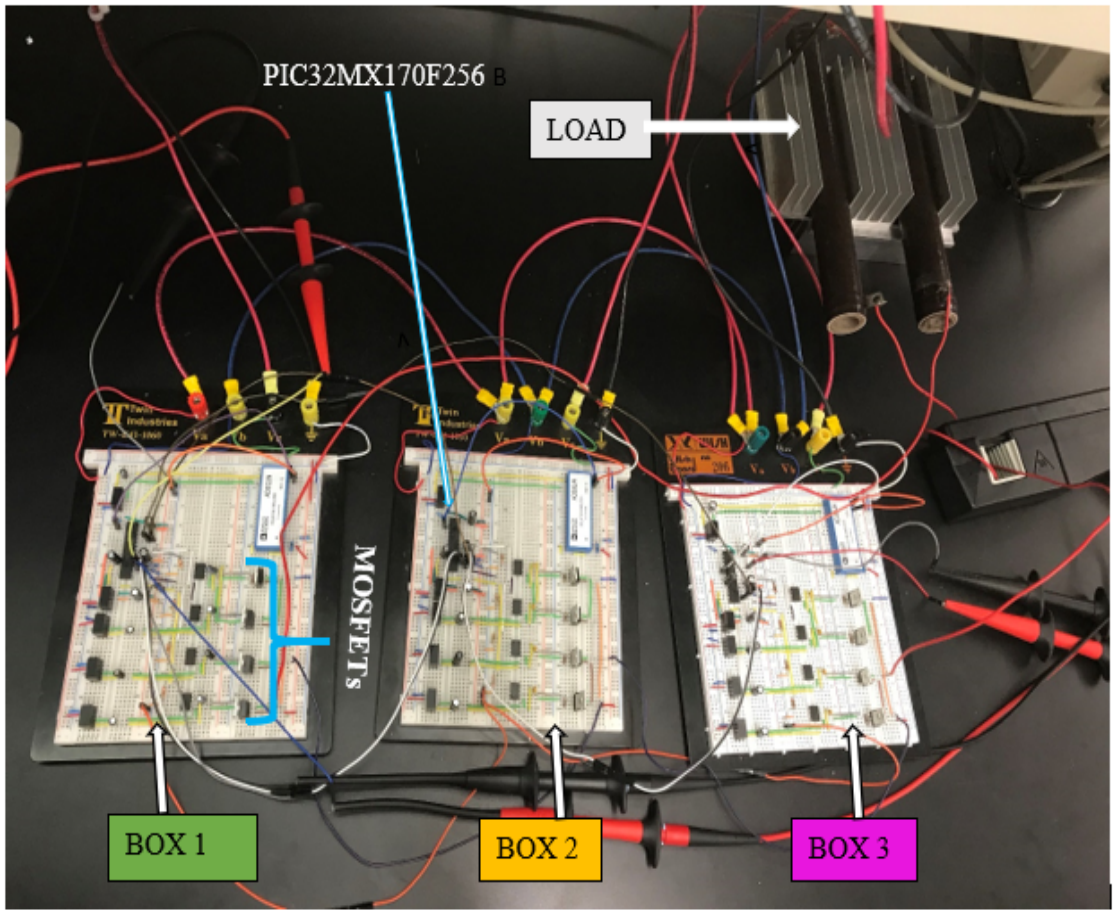


Figure 6.2: Hardware prototype of Cascaded H-bridge Multilevel Invertewith distributed controls and I2C communication protocol.

6.3 Operational Experimental Results

6.3.1 Cascading and synchronizing H-bridge modules

The basic three-level output AC waveform was synthesized, executing output compare dual mode pulse generation of pic micro-controller. Thereby, giving head start to the project. In figure 6.3, the experimental waveform validates all the four states of table 3.2, analyzing states of each switching signal and voltage output level.

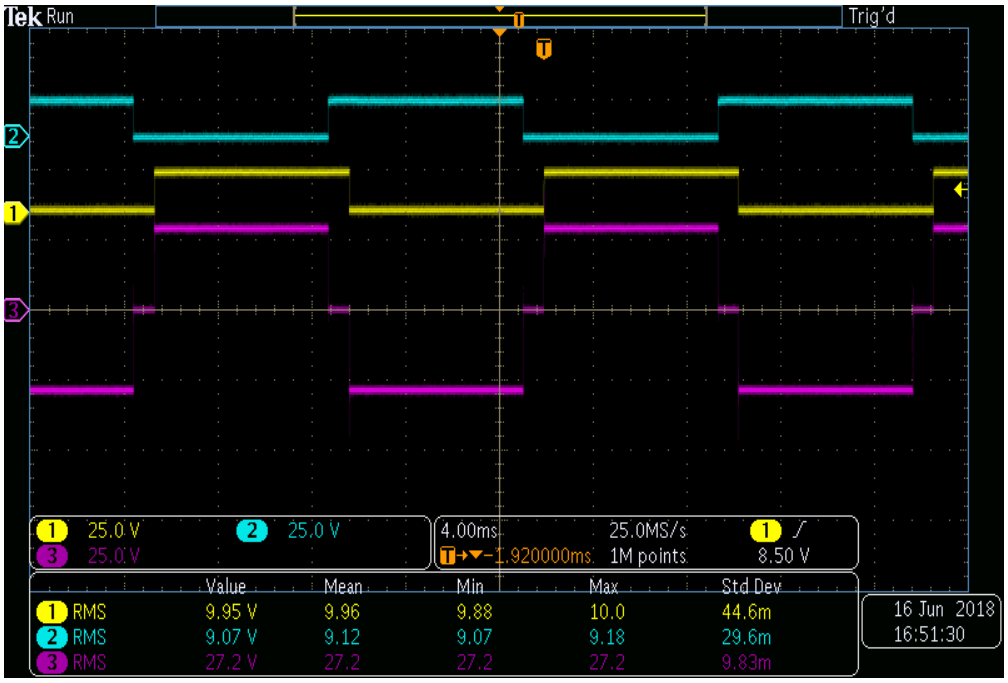


Figure 6.3: Experimental waveform of single H-bridge inverter output (magenta) with gate signals for S_{11} (yellow) and S_{13} (blue).

Micro-controllers' have specific system clock, PIC32MX170F256B has max speed of 50 MHz. Each micro-controller, belonging to same series also have different start time, unless they are operating with same crystal oscillator. Therefore, it is necessary to synchronize all the micro-controllers, so that gate pulses are generated at 60Hz cycle. In this set up Timer 2 has been utilized for pulse generation. Master controller box is set to generate a rising pulse, at output compare module 5, whenever PR_2 value is 0 and stay high until PR_2 value is 2000 as shown in figure 6.4. This pulse is given to

external interrupt pin of the slave micro-controller, where external interrupt is set for highest priority , which calls external interrupt service routine (ISR) when receives rising pulse at external interrupt pin. In figure 6.5 external ISR is presented, where Timer2 of the controller is set to count 0 and all the other output compare module pulses are set at calculated triggering pwm time (to generate gate pulse signals for switches). In master controller, Timer 2 interrupt has highest priority and the ISR of Timer 2 contains the code to set outcumpare modules at calaculated triggering time (to generate gate pulse signals for switches) as shown in figure 6.6.

```
235   // Config timer set up timer2 to generate the wave period//
236      OpenTimer2(T2_ON | T2_SOURCE_INT | T2_PS_1_16, generate_period); // genrate period is PR2 value set at 0xa2c1
237      ConfigIntTimer2(T2_INT_ON | T2_INT_PRIOR_7);                    // Setting timer interrupt at highest priority in Master
238      mT2ClearIntFlag();                                              // clear the interrupt flag
239
240   // Configure peripheral pin for Output Compare//
241      PPSOutput(1,RPB4, OC1);          // OC1 is PPS group 1, map to RPB4  (pin 11-connect to leg A)
242      PPSOutput(2, RPB11, OC2);        // OC2 is PPS group 2, map to RPB11 (pin 22-connect to not of leg A)
243      PPSOutput(4, RPB10, OC3);        // OC3 is PPS group 4, map to RPB10 (pin 21-connect to leg B)
244      PPSOutput(3, RPB6, OC4);         // OC4 is PPS group 3, map to RPB6  (pin 15- connect to not of leg B)
245      PPSOutput(3, RPB13, OC5);        // OC5 is PPS group 4, map to RPB13 (pin 24 to send sync signal (master),
246                                       //to validate synchronization (slave) )
247
248
249   // Configure Output Compare to generate pulses//
250      // OpenOCx( config, value1, value2) ( OC1RS = (value1), OC1R = (value2), OC1CON = (config) )//
251      OpenOC1(OC_ON | OC_TIMER2_SRC | OC_CONTINUE_PULSE,time_pwm1A+20831.5 ,time_pwm1A); // pulse for Switch 11
252      OpenOC2(OC_ON | OC_TIMER2_SRC | OC_CONTINUE_PULSE,time_pwm1A ,time_pwm1A+20831.5); // pulse for Switch 12
253      OpenOC3(OC_ON | OC_TIMER2_SRC | OC_CONTINUE_PULSE,time_pwm1B+20831.5 ,time_pwm1B); // pulse for Switch 13
254      OpenOC4(OC_ON | OC_TIMER2_SRC | OC_CONTINUE_PULSE,time_pwm1B ,time_pwm1B+20831.5); // pulse for Switch 13
255      OpenOC5(OC_ON | OC_TIMER2_SRC | OC_CONTINUE_PULSE,2000,0);                        // to generate sync signal for slaves in master,
256                                                                                        //in slave to validate  synchronization
257
```

Figure 6.4: Code for configuring Timer 2 and Output Compare peripheral in PIC.

```
86  void __ISR(_EXTERNAL_0_VECTOR, IPL7AUTO)  ADS_DRDY_Interrupt(void)
87  {
88  WriteTimer2(0);  //External interrupt sync signal to reset timer2
89
90  // Setting Output Compare at the calculated switching angle after every 60 Hz cycle//
91  SetPulseOC1(time_pwm2A,time_pwm2A+20831.5);     // Gate pulse for switch S21
92
93  SetPulseOC2(time_pwm2A+20831.5+1,time_pwm2A-1); // Gate pulse for switch S22
94
95  SetPulseOC3(time_pwm2B,time_pwm2B+20831.5);     // Gate pulse for switch S23
96
97  SetPulseOC4(time_pwm2B+20831.5+1,time_pwm2B-1); // Gate pulse for switch S24
98
```

Figure 6.5: External Interrupt service routine in Slave for resetting Timer2 clock (synchronization) and issue gate pulses at OC1, OC2, OC3 and OC4 pin.

```
62  void __ISR(_TIMER_2_VECTOR, IPL7AUTO) Timer2Handler(void)
63  {
64  // Setting Output Compare at the calculated switching angle after every 60 Hz cycle//
65  SetPulseOC1(time_pwm1A,time_pwm1A+20831.5);     // Gate pulse for switch S11
66
67  SetPulseOC2(time_pwm1A+20831.5+1,time_pwm1A-1); // Gate pulse for switch S12
68
69  SetPulseOC3(time_pwm1B,time_pwm1B+20831.5);     // Gate pulse for switch S13
70
71  SetPulseOC4(time_pwm1B+20831.5+1,time_pwm1B-1); // Gate pulse for switch S14
72
```

Figure 6.6: Timer 2 Interrupt Service in Master every 60Hz cycle called to issue gate pulses at OC1, OC2, OC3 and OC4 pin.

Figure 6.7 shows the external interrupt signal sent by master (green) and the output compare module five signals: slave1 (yellow) and slave2 (magenta). This picture exhibits synchronization of the three micro-controllers, validating controllers pulse generating output compare modules are synchronized. From graphics (figure 6.7) recorded using MSO, negligible delay of 970.5 ns and 937.5 ns are observed.

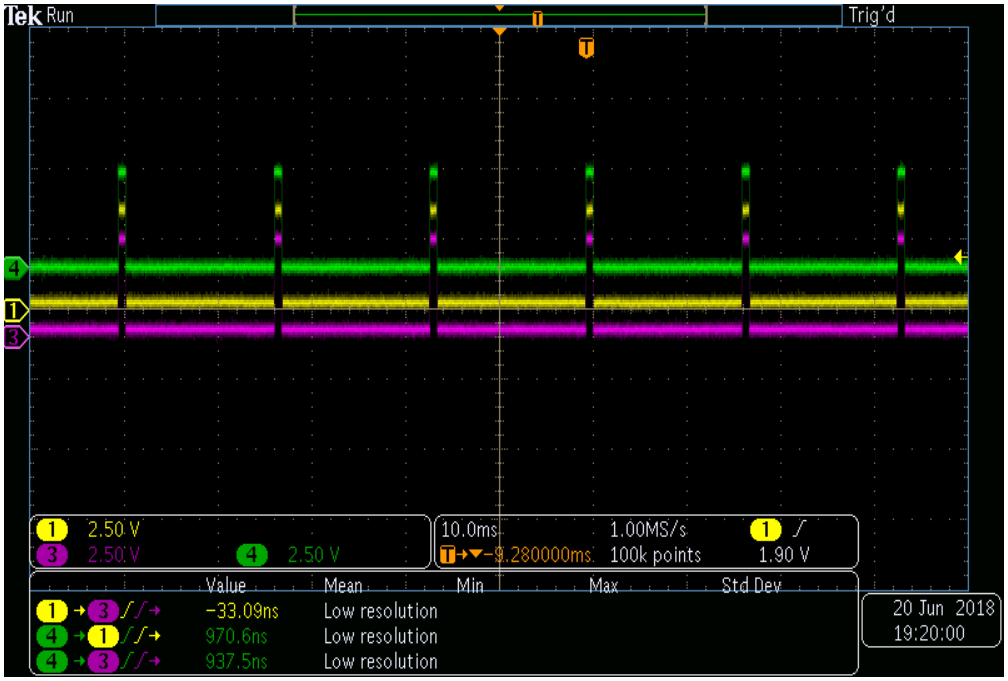


Figure 6.7: Synchronizing signal of master, slave 1 and slave 2 controller.

After synchronizing micro-controllers, two H-bridges are connected in series, establishing cascaded two H-bridge five-level AC output synthesis in experimental prototype as presented in figure 6.8. First box contributes to bottom of the staircase and second box adds at the top. Furthermore, three H-bridge modules are connected in series. Developed CHB-MLI produces seven-level AC output as shown in figure 6.9. Here, it is important to notice that each controller sense the DC voltages of all the H-bridge power cells. Also, generated gate pulses at this instance are hard coded, i.e., without any sorting algorithm.

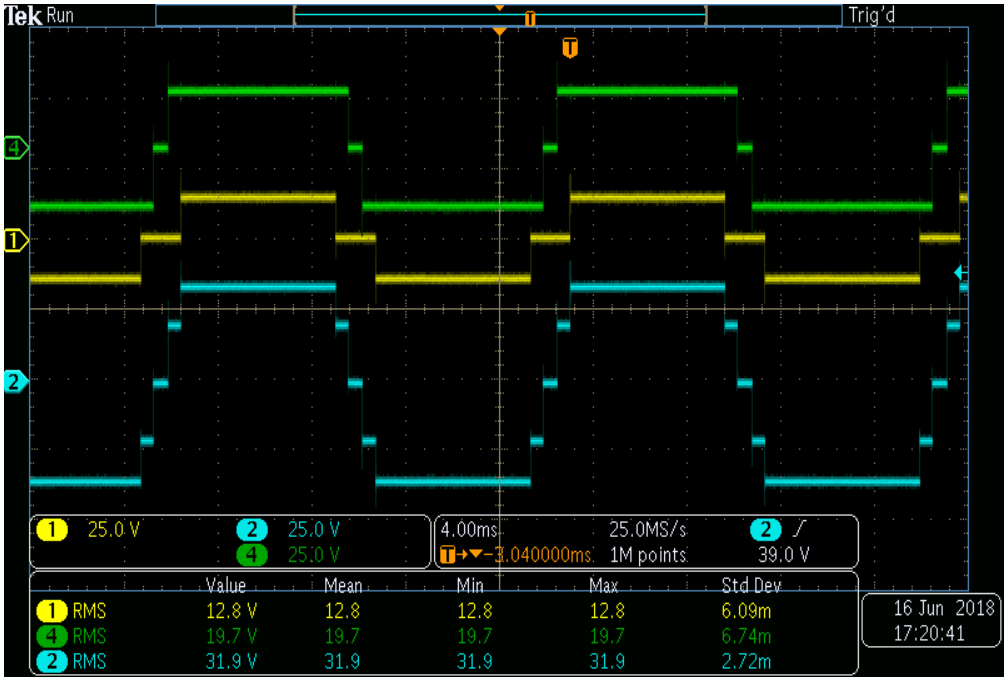


Figure 6.8: Experimental waveform demonstrating five level output of cascaded two H-bridge inverter.

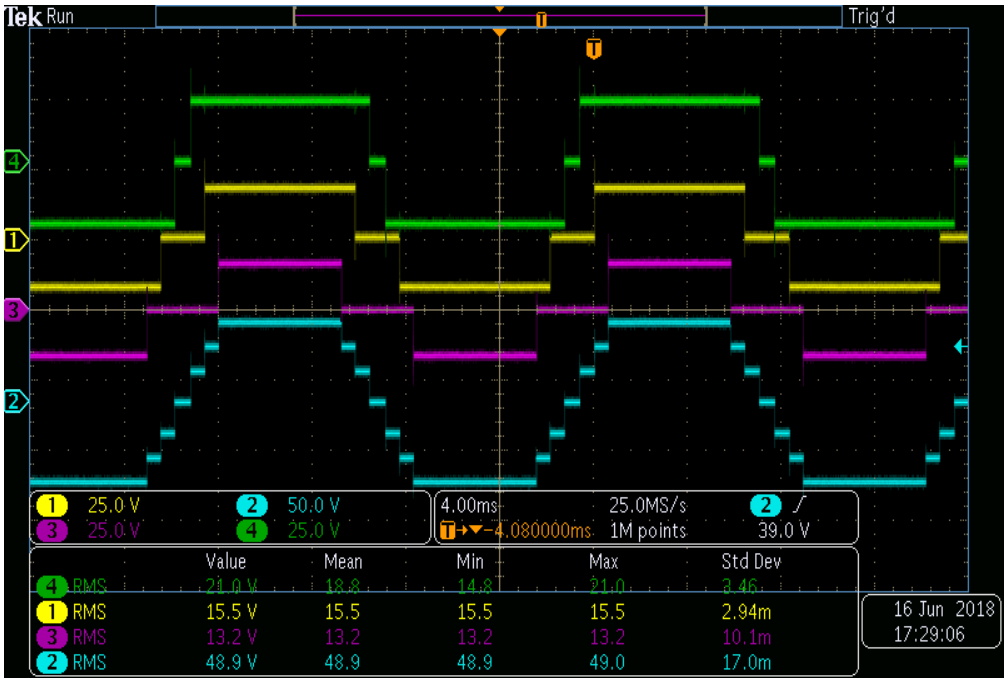


Figure 6.9: Experimental waveform demonstrating seven level output of cascaded three H-bridge inverter.

6.3.2 Sorted Staircase Single Phase Seven-Level Inverter

The controllers sense analog DC voltage of inverter power cells, converts it into ADC, and multiply with the gain value (converting back to original DC voltage) as explained in Chapter 4, under the sub-section titled as micro-controller and it working principle, and presented in figure 6.10. After putting sort algorithm, few waveforms are recorded, where the voltages of the DC supplies integrated with inverter at DC-link of H-bridge power cells are manually varied. The voltage are sorted in descending order as explained by the flowchart process in figure 3.13; further, contributing to generate quasi square wave at the calculated switching instance of respective box. The code of algorithm with time calculation for pulses are shown in figure 6.11. In figure 6.12, voltage value of Box 3 was set at 27 V, Box 2 at 23 V and Box 1 at 13 V , and color representation of the waveforms are — Box3 (magenta), Box2 (yellow), and Box1(green)—. Therefore, VDC3 $>$ VDC2 $>$ VDC1. In figure 6.13, Box 1 is fixed at 13.4 V, Box 2 at 29.6 V and Box 3 at 20.5; therefore, VDC2 $>$ VDC3 $>$ VDC1. Similarly, voltages are manually varied in figure6.14, and fixed to 29.5V, 23.7 V, and 16.4 V for BOX 1, Box 2, and Box 3, respectively; thereby, the sorting order would be VDC1 $>$ VDC2 $>$ VDC3. This section briefly demonstrated implementation of sorting algorithm.

```
109      //Putting the values read in channel order as per boxes//
110       channel2 = master_write3;              //box2
111       channel3 = master_write1;              //box3
112       Vpk=60*1.4142135;                      // Peak value of reference voltage
113       sum=0;
114       // Divide the channel value by 100 to go back to original analog values read from adc//
115          anal_VDC1=channel1/100;
116          anal_VDC2=channel2/100;
117          anal_VDC3=channel3/100;
118       // Multiply by the gain to get the original DC voltages
119          Vdc[0]=anal_VDC1*17.41648;
120          Vdc[1]=anal_VDC2*17.41648;
121          Vdc[2]=anal_VDC3*17.41648;
```

Figure 6.10: ADC value converted back to DC voltage value needed for switching angle calculation.

```
122        /*Sorting Algorithm for sorting DC voltages in descending order*/
123          for(k=0;k<3;k++)
124          {
125              ind[k]=k;
126          }
127
128          for(i=0;i<3-1;i++)
129          {
130              for(j=0;j<3-i-1;j++)
131              {
132                  if(Vdc[j]<Vdc[j+1])
133                  {
134                      tempVdc=Vdc[j];
135                      Vdc[j]=Vdc[j+1];
136                      Vdc[j+1]=tempVdc;
137                      tempind=ind[j];
138                      ind[j]=ind[j+1];
139                      ind[j+1]=tempind;
140                  }
141              }
142          }
143         /*Switching angle calculation*/
144          for(i=0;i<3;i++)
145          {
146              temptheta = (asin((sum+(Vdc[i]/2))/Vpk))*180/3.14159;//arcsin(sum(vdci-1+vdci/2)/vpeak) in radians
147                                                                   //& radians to degrees conversion
148              theta[ind[i]]= temptheta;
149              sum=sum+Vdc[i];
150          }
151
152              timetheta1A=(theta[0]*(0.016666))/360;
153              timetheta1B=((180-theta[0])*(0.016666))/360;
154              time_pwm1A=(timetheta1A*40000000/16)-1;
155              time_pwm1B=(timetheta1B*40000000/16)-1;
156
157              timetheta2A=(theta[1]*(0.016666))/360;
158              timetheta2B=((180-theta[1])*(0.016666))/360;
159              time_pwm2A=(timetheta2A*40000000/16)-1;
160              time_pwm2B=(timetheta2B*40000000/16)-1;
161
162              timetheta3A=(theta[2]*(0.016666))/360;
163              timetheta3B=((180-theta[2])*(0.016666))/360;
164              time_pwm3A=(timetheta3A*40000000/16)-1;
165              time_pwm3B=(timetheta3B*40000000/16)-1;
166
167
```

Figure 6.11: Sorting DC voltages in descending order and calculating switching angle.

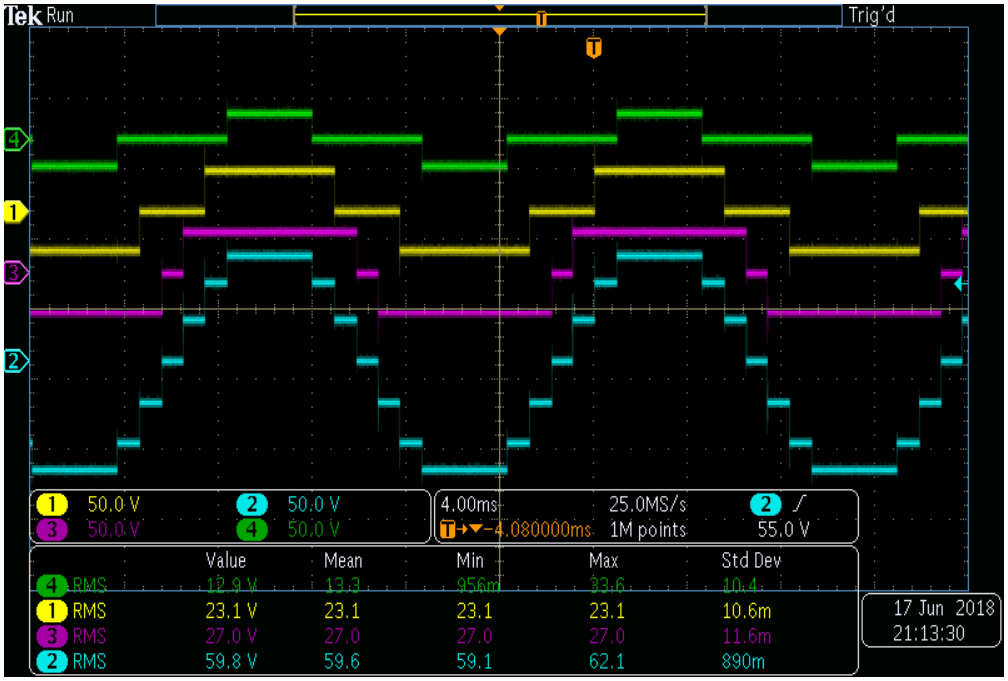


Figure 6.12: Waveform for AC output and H-bridge modules with sorting algorithm implemented and voltages are in order VDC3 > VDC2 > VDC1.

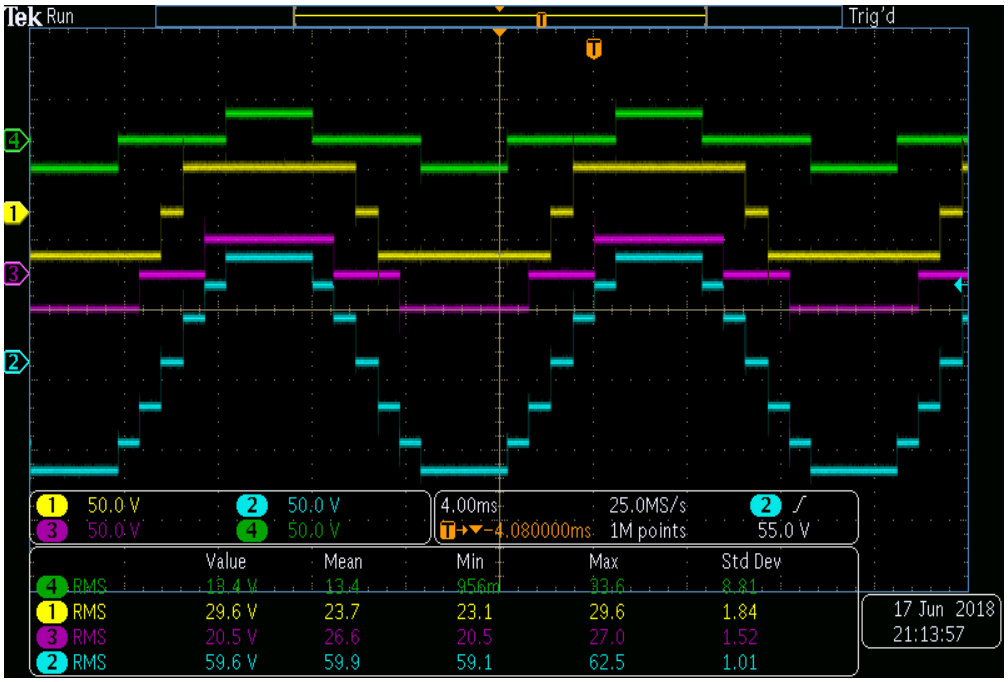


Figure 6.13: Waveform for AC output and H-bridge modules with sorting algorithm implemented and voltages are in order VDC2 > VDC3> VDC1.

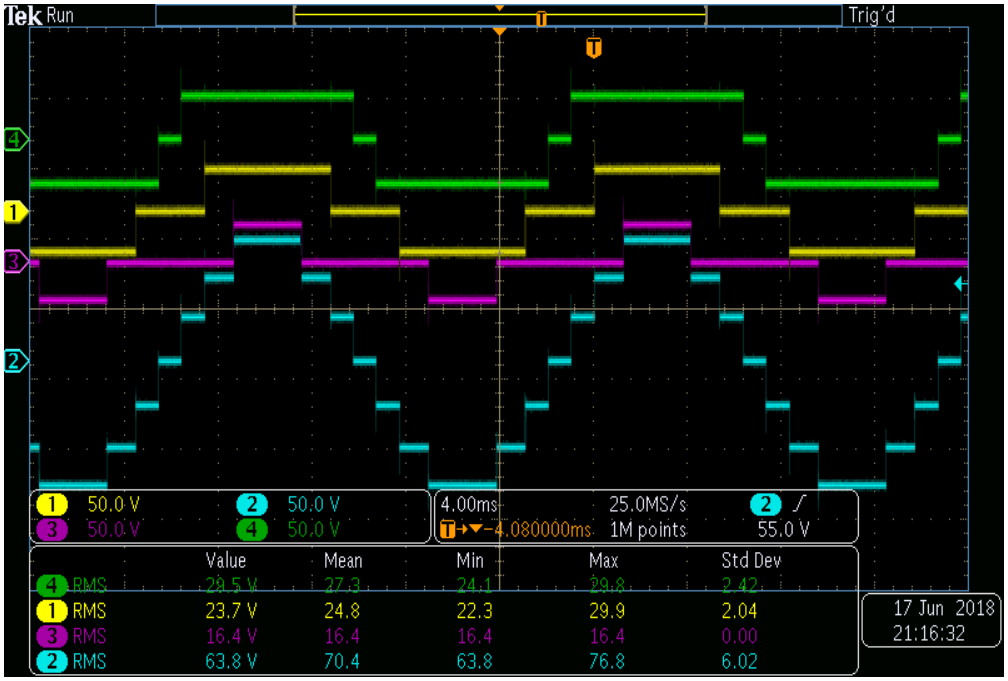


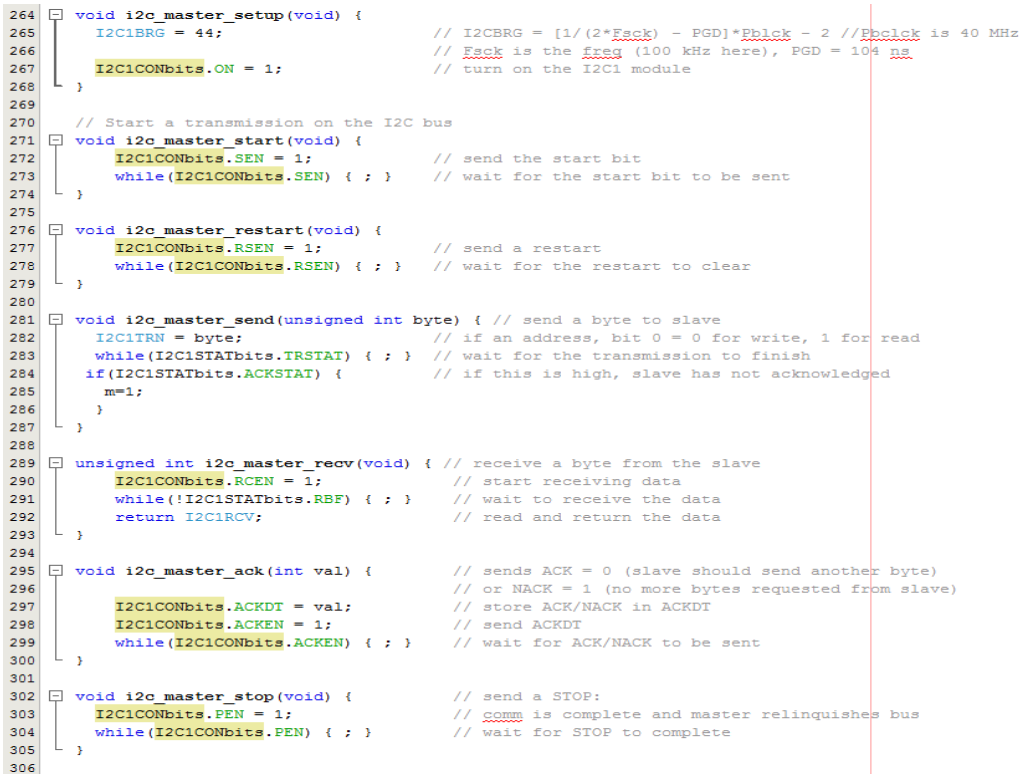
Figure 6.14: Waveform for AC output and H-bridge modules with sorting algorithm implemented and voltages are in order VDC1> VDC2> VDC3.

6.3.3 Implementation of Distributed Controls and Communication

In this subsection, each controller implements I2C communication protocol as explained in chapter 4. All the controllers are synchronized with a negligible time delay as shown in the figure 6.7 previously. As soon as Timer ISR is called in master micro-controller, it initiates communication by sending start bit. Further, sending slave address left shifted by one; and when digit in LSb it indicates read, otherwise, write. ADC value of DC voltages at DC-link of H-Bridges read from the buffer of ADC converter and stored in variables. Slaves' stores updated data in variables: slave1dc and slave2dc, whereas, master stores it in variable: masterdc. As master sends the address of slave over SDA line after taking control over SCL line, whichever slave is addressed the interrupt flag of that particular slave rise and slave ISR is executied. The detailed step-wise process of communication is described in chapter 4. Also, a section of master and slave micr0-controllers code are provided in figure 6.15 and figure 6.17 respectively.

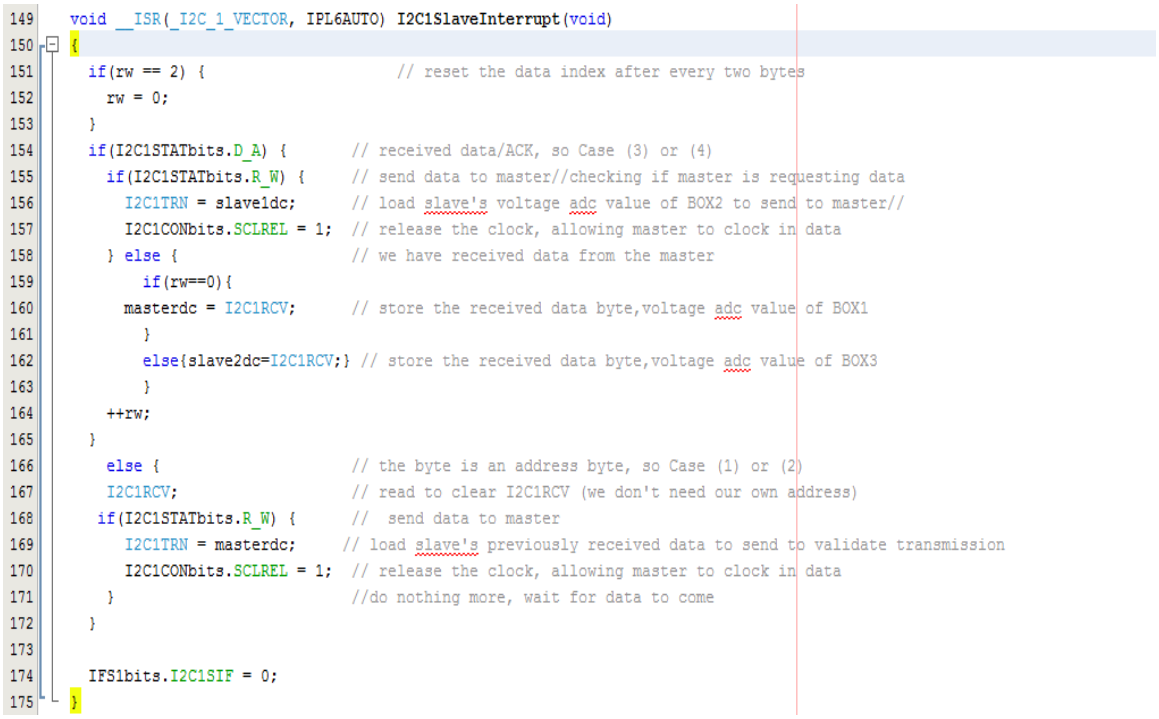
```
// I2C Protocol code for the Master controller to send and receive data from slave 1 and slave 2//
int buf[100] = {};                      // buffer for sending messages to the user
i2c_master_start();                     // Begin the start sequence
i2c_master_send((SLAVE_1_ADD<< 1) | 1); // send slave 1 address, left shifted by 1,
                                        // and then a 1 in LSB, indicating read
master_read0 = i2c_master_recv();       // receive a byte from the bus for the verification of transmitted data
i2c_master_ack(0);                      // send ACK (0): master wants another byte!
master_read1 = i2c_master_recv();       // receive another byte from the bus
i2c_master_ack(1);                      // send NACK (1):  master needs no more bytes
i2c_master_restart();                   // Issue a restart signal
i2c_master_send((SLAVE_2_ADD<< 1) | 1); // send slave 1 address, left shifted by 1,
                                        // and then a 1 in LSB, indicating read
master_read2 = i2c_master_recv();       // receive a byte from the bus for the verification of transmitted data
i2c_master_ack(0);                      // send ACK (0): master wants another byte!
master_read3 = i2c_master_recv();       // receive another byte from the bus voltage of box 3
i2c_master_ack(1);                      // send NACK (1):  master needs no more bytes

 anal_VDC=(3.3/1023)*ReadADC10(0);      // Read the adc value from the buffer
                                        // of the H-bridge box connected
 channel1 =anal_VDC*100;                //store in variable channel1 multiplying by 100
masterdc=channel1;                      // adc value of voltage  from BOX1
slave2dc=master_read3;                  // adc value of voltage from BOX3
slave1dc=master_read1;                  // adc value of voltage from BOX2
 i2c_master_restart();                  // send a RESTART so we can begin reading
i2c_master_send(SLAVE_1_ADD << 1);      // send the slave 1 address (BOX 2), left shifted by 1,
                                        // which clears bit 0, indicating a write
i2c_master_send(masterdc);              // send a byte to the slave (Value of BOX 1)
i2c_master_send(slave2dc);              // send another byte to the slave (Value of BOX 3)
i2c_master_restart();                   // send a RESTART so we can begin reading
i2c_master_send(SLAVE_2_ADD << 1);      // send the slave 2 address (BOX 3), left shifted by 1,
                                        // which clears bit 0, indicating a write
i2c_master_send(masterdc);              // send a byte to the slave (Value of BOX 1)
i2c_master_send(slave1dc);              // send another byte to the slave (Value of BOX 2)
i2c_master_stop();                      // send STOP:  end transmission, give up bus
```

Figure 6.15: I2C protocol implementation in Master controller.



```
void i2c_master_setup(void) {
  I2C1BRG = 44;                     // I2CBRG = [1/(2*Fsck) - PGD]*Pblck - 2 //Pbclck is 40 MHz
                                    // Fsck is the freq (100 kHz here), PGD = 104 ns
  I2C1CONbits.ON = 1;               // turn on the I2C1 module
}

// Start a transmission on the I2C bus
void i2c_master_start(void) {
    I2C1CONbits.SEN = 1;            // send the start bit
    while(I2C1CONbits.SEN) { ; }    // wait for the start bit to be sent
}

void i2c_master_restart(void) {
    I2C1CONbits.RSEN = 1;           // send a restart
    while(I2C1CONbits.RSEN) { ; }   // wait for the restart to clear
}

void i2c_master_send(unsigned int byte) { // send a byte to slave
  I2C1TRN = byte;                   // if an address, bit 0 = 0 for write, 1 for read
  while(I2C1STATbits.TRSTAT) { ; }  // wait for the transmission to finish
 if(I2C1STATbits.ACKSTAT) {         // if this is high, slave has not acknowledged
   m=1;
  }
}

unsigned int i2c_master_recv(void) { // receive a byte from the slave
    I2C1CONbits.RCEN = 1;             // start receiving data
    while(!I2C1STATbits.RBF) { ; }    // wait to receive the data
    return I2C1RCV;                   // read and return the data
}

void i2c_master_ack(int val) {        // sends ACK = 0 (slave should send another byte)
                                      // or NACK = 1 (no more bytes requested from slave)
    I2C1CONbits.ACKDT = val;          // store ACK/NACK in ACKDT
    I2C1CONbits.ACKEN = 1;            // send ACKDT
    while(I2C1CONbits.ACKEN) { ; }    // wait for ACK/NACK to be sent
}

void i2c_master_stop(void) {          // send a STOP:
  I2C1CONbits.PEN = 1;                // comm is complete and master relinquishes bus
  while(I2C1CONbits.PEN) { ; }        // wait for STOP to complete
}
```

Figure 6.16: Function call for Master code.



```
void __ISR(_I2C_1_VECTOR, IPL6AUTO) I2C1SlaveInterrupt(void)
{
  if(rw == 2) {                     // reset the data index after every two bytes
    rw = 0;
  }
  if(I2C1STATbits.D_A) {       // received data/ACK, so Case (3) or (4)
    if(I2C1STATbits.R_W) {     // send data to master//checking if master is requesting data
      I2C1TRN = slave1dc;      // load slave's voltage adc value of BOX2 to send to master//
      I2C1CONbits.SCLREL = 1;  // release the clock, allowing master to clock in data
    } else {                   // we have received data from the master
        if(rw==0){
      masterdc = I2C1RCV;      // store the received data byte,voltage adc value of BOX1
        }
        else{slave2dc=I2C1RCV;} // store the received data byte,voltage adc value of BOX3
        }
    ++rw;
  }
    else {                     // the byte is an address byte, so Case (1) or (2)
    I2C1RCV;                   // read to clear I2C1RCV (we don't need our own address)
   if(I2C1STATbits.R_W) {      //  send data to master
      I2C1TRN = masterdc;     // load slave's previously received data to send to validate transmission
      I2C1CONbits.SCLREL = 1;  // release the clock, allowing master to clock in data
    }                          //do nothing more, wait for data to come
  }

  IFS1bits.I2C1SIF = 0;
}
```

Figure 6.17: I2C protocol implementation in Slave controller calling Slave ISR.

Figure 6.18 shows the sync signal (magenta), SCL bus signal (blue), and SDA bus signal (yellow). The white outputs are digital probes output for clock and data buses. As sync signal is initiated and timer 2 in master started counting, master I2C protocol also gets activated. The pulse width of sync signal is 0.000804 sec and the data transmission through I2C gets completed well in advance, prior to the falling of sync signal. This displays the high speed of I2C protocol communication. The figure 6.19 consist few graphics to display the recorded waveforms of clock and data signal implemented with I2C communication protocol.

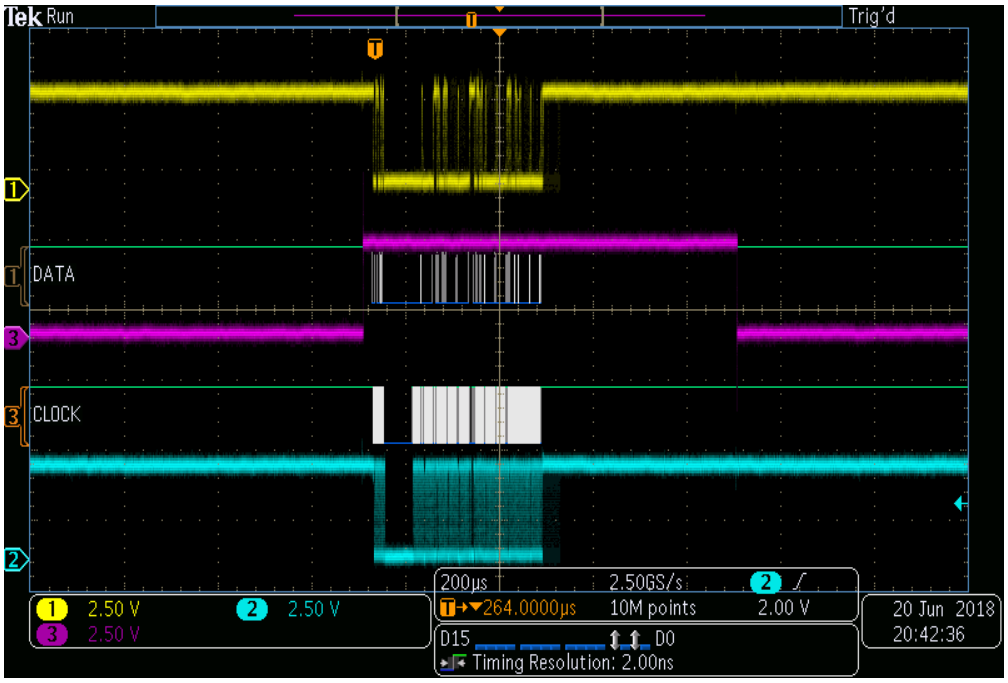


Figure 6.18: Recorded synchronizing signal, Data signal and Clock signal from PIC micro-conroller.

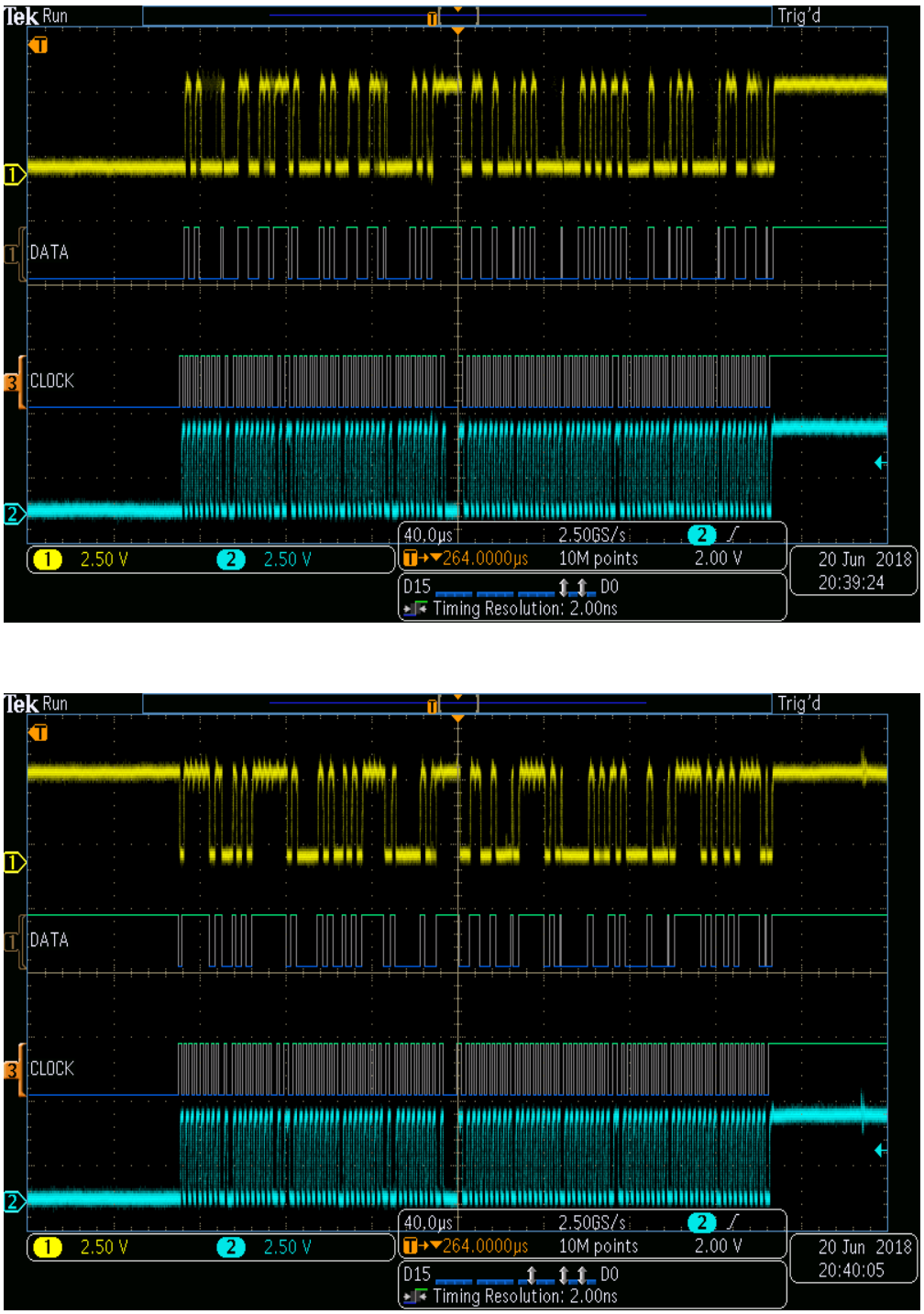


Figure 6.19: Waveform showing I2C data transfer over SDA line.

After, inserting the master program in PIC 1, slave1 program in PIC 2, and slave2 program in PIC 3; accuracy in transmission of data is validated by varying DC voltages of each H-bridge power cell. Further, system reliability in terms of data trans-

mission is cross-verified, utilizing MPLABX IDE terminal for debugging. The codes are updated with the sorting staircase modulation strategy program, and few tests are demonstrated to establish communication of data and sorting together. In figure 6.20, VDC1, VDC2, and VDC3 are set at 22.7 V, 29.6 V, and 16 V respectively. Henceforth, the sort order would be VDC2 > VDC1 > VDC3 which can be clearly seen in the staircase modulation. Figure 6.21 shows that VDC1 is set at 20.4 V, VDC2 is set at 10.8 V, and VDC3 is set at 28.9 V. Therefore, the order VDC3 > VDC1> VDC2. Both figures validate the implementation of I2C communication protocol. Thereby, transmitting the data accurately for execution of sorted staircase modulation strategy on CHB-MLI.

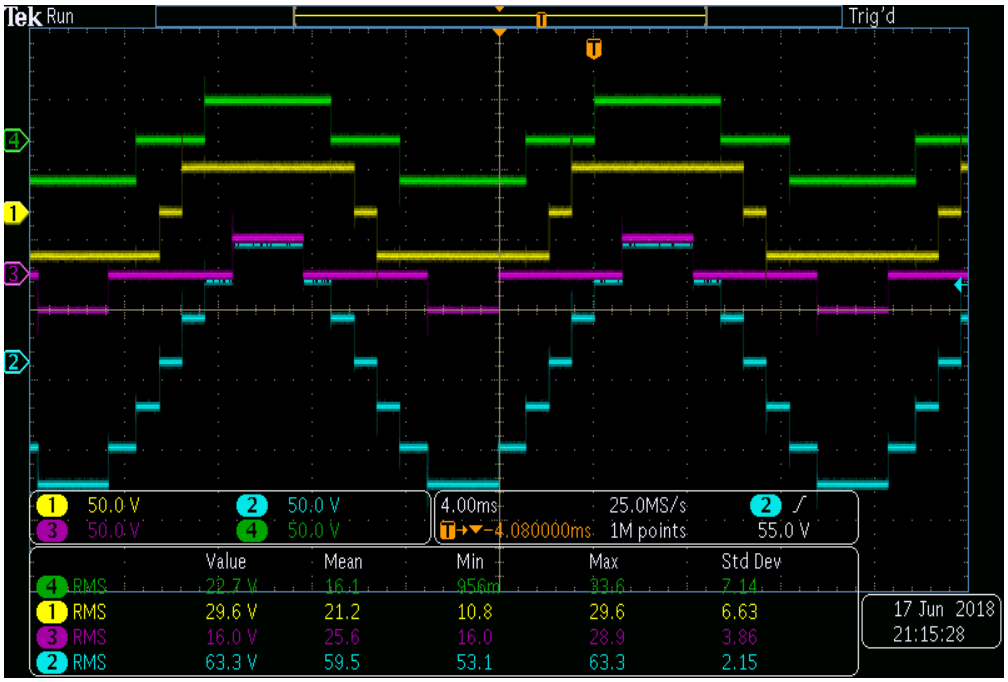


Figure 6.20: Waveform showing implementation of I2C protocol by transmitting voltage and sorting in the order VDC2> VDC1> VDC3 constructing seven level output.

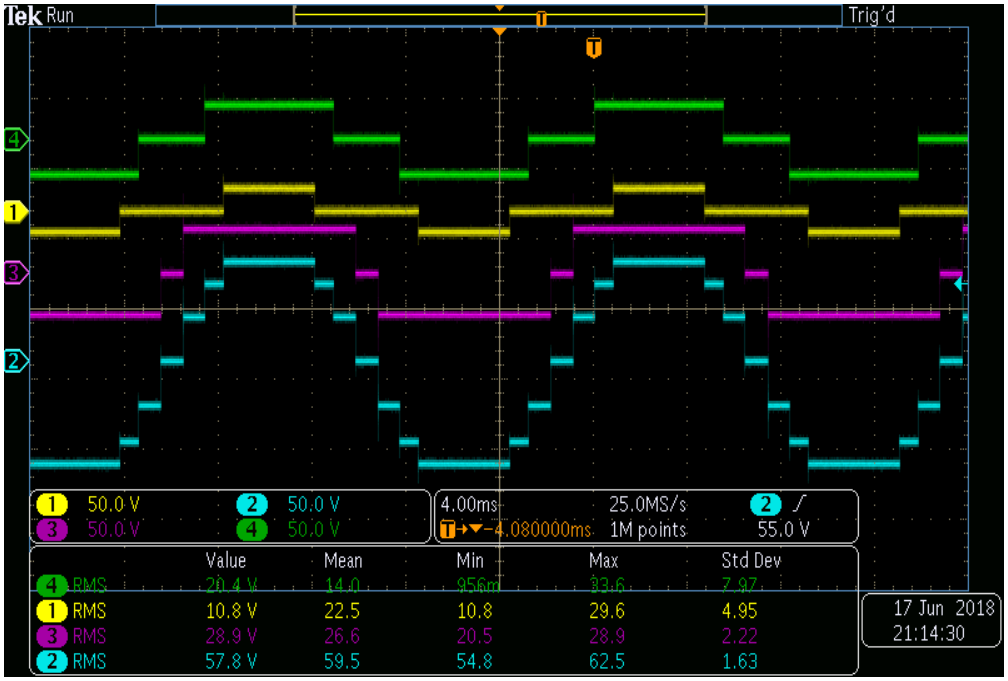


Figure 6.21: Waveform showing implementation of I2C protocol by transmitting voltage and sorting in the order VDC3> VDC1> VDC2 constructing seven level output.

6.3.4 CHB-MLI Interfaced with Load

After, I2C protocol is implemented on CHB-MLI, a load of 70 Watt is connected between the two AC terminal of cascaded three H-bridges. A current probe is assembled with the set up to record current waveform. The PIC 1 of Box 1 executes master program, PIC 2 of Box 2 executes slave1 program, and PIC 3 of BOX 3 executes slave2 program. A housekeeping power supply of 24 V is first set on. Further, DC Voltages of all the inverter H-bridge power cells are increased manually. A quasi square wave AC output voltage with 60 V rms is synthesized pushing a current of 1.18 rms, synthesizing seven level current output waveform. Henceforth, extracting power of 70 Watt in total from the three DC supplies as shown in figure 6.22.

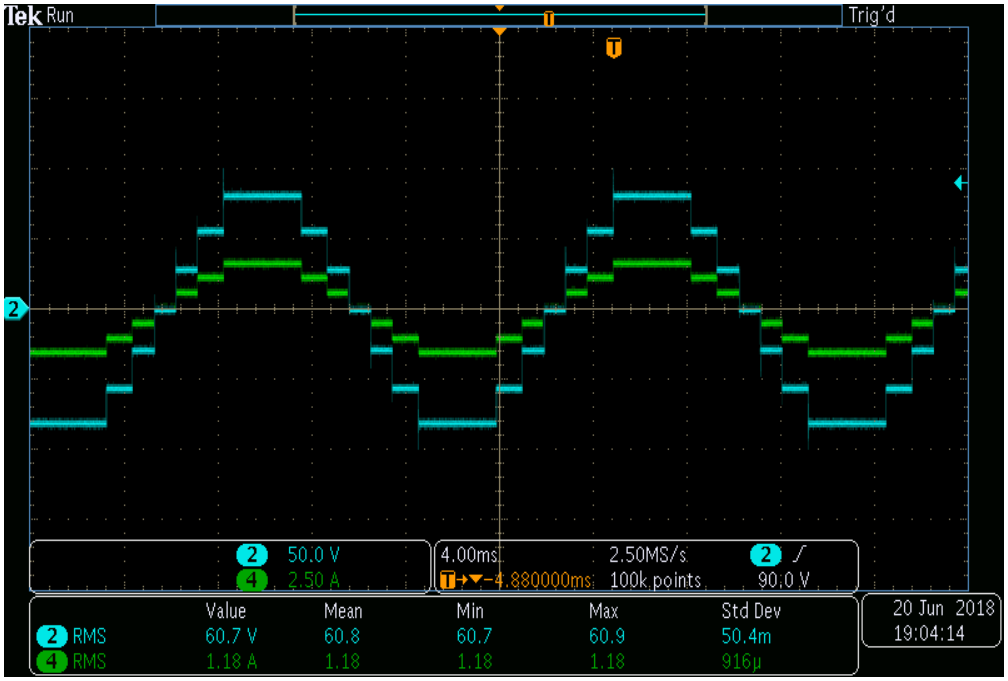


Figure 6.22: Experimental seven level AC output waveform of 60 V rms Voltage and 1.18 A rms current.

CHAPTER 7: CONCLUSION

7.1 Overview

A cascaded H-bridge multi-level inverter toplogy (CHB-MLI) utilizing a unique methodology that converts the conventional dc voltage output of a solar PV panel to quasi-square wave ac voltage. When aggregated, realizes a superior quality multilevel waveform that is directly interfaced with the load has been investigated.This alternative approach offers advantages such as extracting maximum power at panel level and realization of system-level cost benefits. The control technique of Sorted Stair Case Modulation (SSCM) has been discussed.The benefits of distributed controller over a single master controller are analyzed, and parameters needed for execution of distributed controls are listed.

Matlab/Simulink model of solar PV panel has been presented, and three PV panels are companioned individually with single phase H-bridge power cell developing CHB-MLI. Further, this inverter is integrated with single phase resistive load. Distributed controller blocks implementing SSCM strategy has been presented in MATLAB model. Simulations are performed for two different sorting scenarios corresponding to operating condition of two case studies, with uniform and non-uniform irradiance. The observations made from simulation results were demonstrated in tabular form.It is noted that increasing the sorting frequency improves the yield and reduces the ripple when irradiance conditions are uniform; however, under non-uniform irradiance conditions,negligible improvement is observed

Three protocols, Universal Asynchronous Receiver Transmitter (UART), Serial Peripheral Interface (SPI) and Inter Integrated Circuit (I2C) are discussed in detail. Architectural overview of these protocols in refernce with sven-level CHB-MLI are

displayed, consisting of three H-bridge modules with three PIC micro-controllers. I2C protocol is implemented on the developed laboratory prototype of seven-level CHB-MLI, integrated with resistive load of 50 Watts, synthesizing 60 Volt AC rms output.

7.2 Future Scope and Recommendation

The evaluation of the control strategy performed in this thesis can be tested with the grid interfacing. Also, system can be modified for closed loop current control studies. Implementation of Maximum Power Point algorithm is recommended for efficient power throughput. The hardware prototype can be built with printed circuit board design and can be tested by integrating H-bridge power cells with solar panel at DC-link. A Fourier analysis to study the Total Harmonic Distortion (THD) for the control strategy can be performed, and the controller design can be checked with IEEE 1547 standard for interconnecting distributed resources with electrical power systems. Active power decoupling solutions can be surveyed for reducing DC-link ripple. Wireless communication method discussed in the thesis can also be investigated for implementation.

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