DESIGN, MODELING, FABRICATION & CHARACTERIZATION OF INDUSTRIAL Si SOLAR CELLS

By

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A dissertation submitted to the faculty of
The University of North Carolina at Charlotte
in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in
Electrical Engineering

Charlotte

2017

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ABSTRACT

AHRAR AHMED CHOWDHURY. Design, Modeling, Fabrication & Characterization of Industrial Si Solar Cells. (Under the direction of DR. ABASIFREKE EBONG)

Photovoltaic is a viable solution towards meeting the energy demand in an ecofriendly environment. To ensure the mass access in photovoltaic electricity, cost effective approach needs to be adapted. This thesis aims towards substrate independent fabrication process in order to achieve high efficiency cost effective industrial Silicon (Si) solar cells. Most cost-effective structures, such as, Al-BSF (Aluminum Back Surface Field), FSF (Front Surface Field) and bifacial cells are investigated in detail to exploit the efficiency potentials. First off, we introduced two-dimensional simulation model to design and modeling of most commonly used Si solar cells in today's PV arena. Best modelled results of high efficiency Al-BSF, FSF and bifacial cells are 20.50%, 22% and 21.68% respectively. Special attentions are given on the metallization design on all the structures in order to reduce the Ag cost. Furthermore, detail design and modeling were performed on FSF and bifacial cells. The FSF cells has potentials to gain $0.42\%_{abs}$ efficiency by combining the emitter design and front surface passivation. The prospects of bifacial cells can be revealed with the optimization of gridline widths and gridline numbers. Since, bifacial cells have metallization on both sides, a double fold cost saving is possible via innovative metallization design.

Following modeling an effort is undertaken to reach the modelled result in fabrication the process. We proposed substrate independent fabrication process aiming towards establishing simultaneous processing sequences for both monofacial and bifacial cells. Subsequently, for the contact formation cost effective screen-printed technology is utilized throughout this thesis. The best Al-BSF cell attained efficiency ~19.40%. Detail characterization was carried out to find a roadmap of achieving >20.50% efficiency Al-BSF

cell. Since, n-type cell is free from Light Induced degradation (LID), recently there is a growing interest on FSF cell. Our best fabricated result of FSF cell achieved ~18.40% efficiency. Characterizations on such cells provide that, cell performance can be further improved by utilizing high lifetime base wafer. We showed a step by step improvement on the device parameters to achieve ~22% efficiency FSF cell.

Finally, bifacial cells were fabricated with 13.32% front and 9.65% rear efficiency. The efficiency limitation is due to the quality of base wafer. Detail resistance breakdown was conducted on these cells to analyze parasitic resistance losses. It was found that base and gridline resistances dominated the FF loss. However, very low contact resistance of 20 mΩ-cm^2 at front side and 2 mΩ-cm^2 at the rear side was observed by utilizing same Ag paste for front and rear contact formation. This might provide a pathway towards the search of an optimized Ag paste to attain high efficiency screen-printed bifacial cell. Detail investigations needs to be carried out to unveil the property of this Ag paste.

In future work, more focus will be given on the metallization design to incorporate further reduction in Ag cost. Al_2O_3 passivation layer will be incorporated as a means to attain ~23% screen-printed bifacial cell.

ACKNOWLEDGEMENTS

I want to thank first and foremost to Almighty Allah (The God) on giving me the opportunity in obtaining PhD in the focus of photovoltaics. It is a great blessing from Him to serve the humanity through my research expertise. Secondly, I want to give thanks to my mother, Lutfa Chowhdhury and father, Abdul Kahir Chowdhury on providing supports and means in this journey. My mother wanted to pursue higher education, however due to the challenging circumstances she could not accomplish her goal. Truly through this accomplishment her ultimate dream is fulfilled. Overall, my parents' unselfish love, affection and generosity was the cornerstone of being persistent and motivational towards my research work. I am immensely proud to see their smiles and happy faces through this achievement.

From academic perspective, I humbly want to express my gratitude to Dr. Paul Basore, without whom I could not have come so far. He helped me a lot in understanding the device physics and modeling in two-dimensional structure. I am ever grateful to Him for this contribution and teaching me details of simulation and modeling. I also want to thank my supervisor Dr. Abasifreke Ebong for instilling self-belief, confidence and positive attitude as a researcher. My great appreciation is due to my committee members Dr. Yasin Raja and Dr. Yong Zhang, for their discussion and support towards this work. Nevertheless, I want to recall the contribution of my undergraduate supervisor Dr. Sharif Mohammad Mominuzzaman who inspired me immensely to pursue higher education in my final year of bachelor degree.

Being in a research group, I was blessed to work with my fellow members, Veysel Unsur, Nian Chen, Babar Hossain and Yu-Chen Hsu from whom I learned most how to be a good researcher. Their friendly and cozy attitude in our research group made this journey easier for me. Moreover, numerous people helped me in my difficult times while staying at Charlotte. Firstly, I am gratified and thankful to Jehad Sinjer for bestowing brotherly love and mercy. I want to thank also Mahbub Ali Sarker and Aslam Tawhid for their immense support in odd times. While starting my life in Charlotte Mohammad Ashiqur Rahman and Mainuddin Mohammad helped me a lot to cope up with the new environment. I am very much humbled for their contribution in my life. I also want to thank Stephanie LeClair for her motherly love throughout my journey during the course of PhD program. She is the first person to whom I rushed for any kind of help knowing that she is the problem solver. I also want to thank Mark Clayton for his support while obtaining my masters' degree in Optical Science and Engineering.

Finally, I am thankful to my family members; Numer, Jesper and Liza who were instrumental in providing me inspirations and motivations for higher study. Finally, I am extremely blessed to have the support of my aunt, Jabu Chowdhury who taught me the aspect of perseverance and patience in life. The support that I received from all family members are truly significant towards my achievement.

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CHAPTER 01: INTRODUCTION

1.1. Statement of the Problem

Electricity is one of the key needs for economic, education and social advancements. However, today there are more than 1.2 billion people -17% of global population [1] in the world without access to electricity, partly because of cost or lack of natural/human resources. The cost of generating, transmitting and distributing electricity can be high, irrespective of the source. There are two sources of electricity generation: (i) renewable and (ii) non-renewable. The renewable sources include wind, photovoltaic, hydro, geothermal etc. Non-renewable include fossil (oil), coal, natural gas and nuclear. The key advantage of fossil fuel energy source lies on the cost-effectiveness, but the carbon foot print is a major concern. Renewable energy on the other hand, is free from carbon emission, provides an alternative solution towards clean and environmental friendly energy. That is why total electricity generation with renewable energy is desired, and its growth is rapidly increasing in recent years as illustrated in Fig. 1. 1. World Net electricity generation prediction.. More so, the projection growth of future renewable energy since 2015 is high in contrast to the shrinkage of non-renewable energy consumption as shown in Fig. 1.2. In particular, solar PV and wind have the highest growth compared to other renewable energy sources. Internationally, China and Taiwan lead in the PV growth in recent years as shown in Fig.1. 3. This growth has greatly influenced the CO_2 emission reduction. Locally, in United States the amount of CO_2 emission avoided due to the introduction of solar PV from the year 2010 to 2014 is shown in Fig. 1.4. This is an exponential rate of reduction in CO_2 emission compared to the early 2000s.

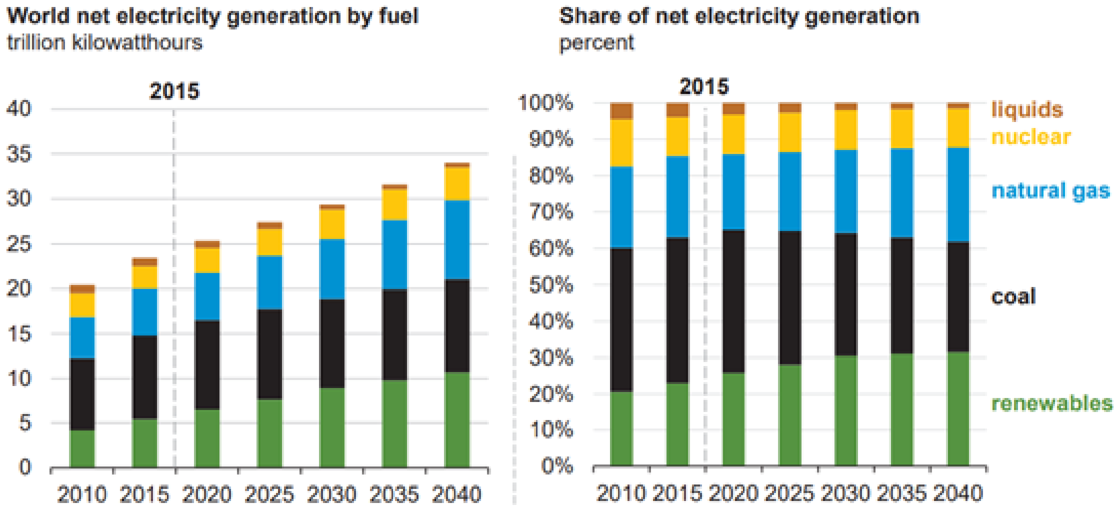


Fig. 1. 1. World Net electricity generation prediction. [2]

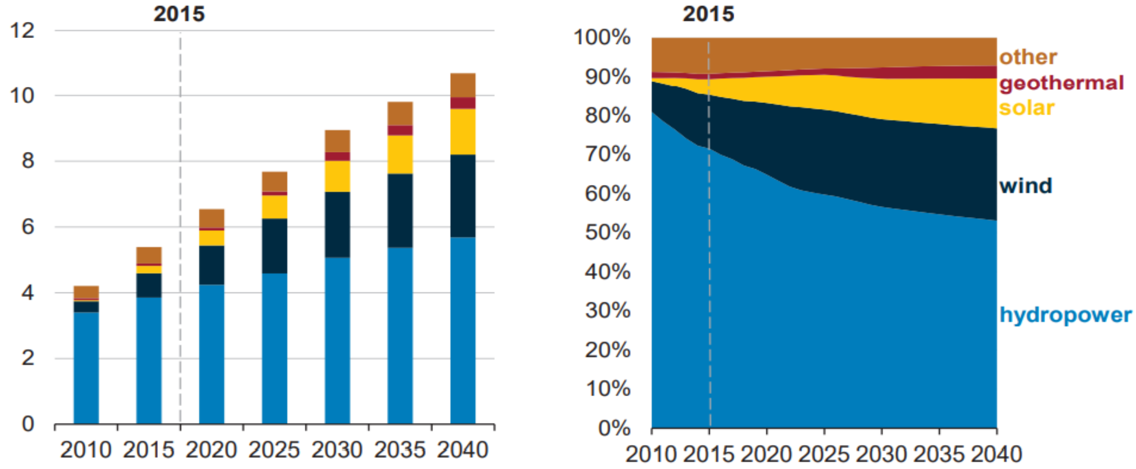


Fig. 1. 2. Growth Prediction of Renewable energy resources in the future decade.[2]

Further prediction in Fig. 1.5 shows that solar will outperform the coal energy resource in the coming decade. The key reason for solar PV becoming the major energy resource can be understood by the rapid decrease in levelized cost of electricity (LCOE) as shown in Fig. 1.6. The average cost of solar since 2016 is 0.131 USD/KWh, which is in the cost range of fossil fuel. This is a major stride given that over a decade ago, it was more than three times. In spite of this cost reduction, the levelized cost of electricity from solar needs to meet the DOE

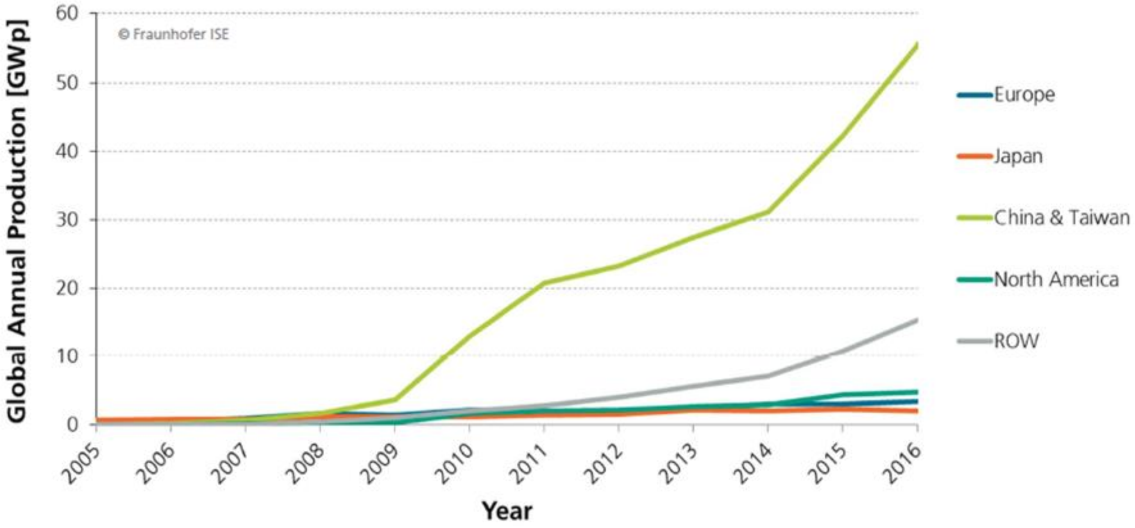


Fig. 1. 3. Global annual production of PV industry since 2005. [3]

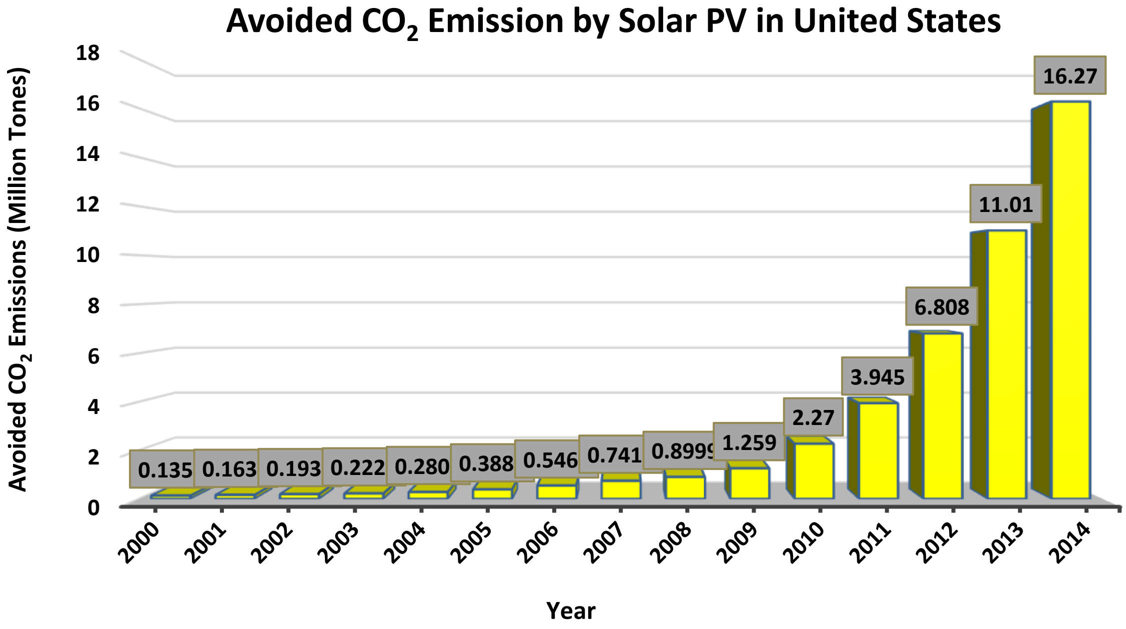


Fig. 1. 4. Utilization of solar PV has reduced the CO2 emission in recent years.[4]

Sunshot goal of 3 cent/kWh in 2030. Thus, it is prudent to design, model, fabricate, characterize and analyze simple solar cell structures with low-cost processes but achieve higher efficiencies.

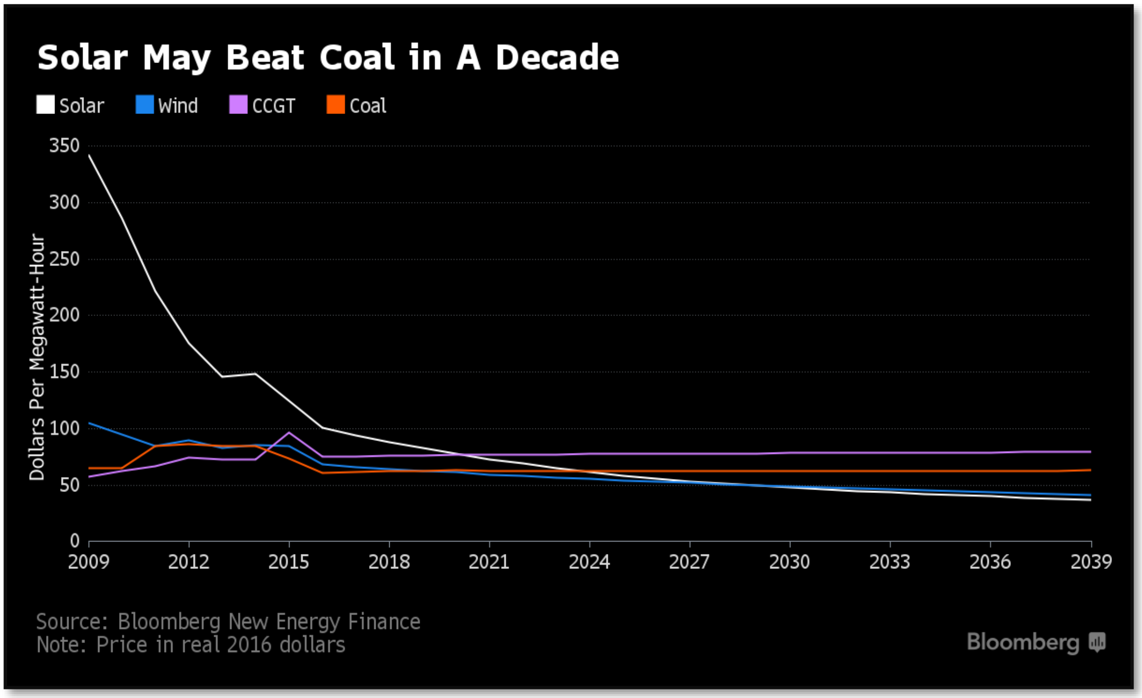


Fig. 1. 5. Solar Energy will dominate and compete in comparison with energy resources.[5]

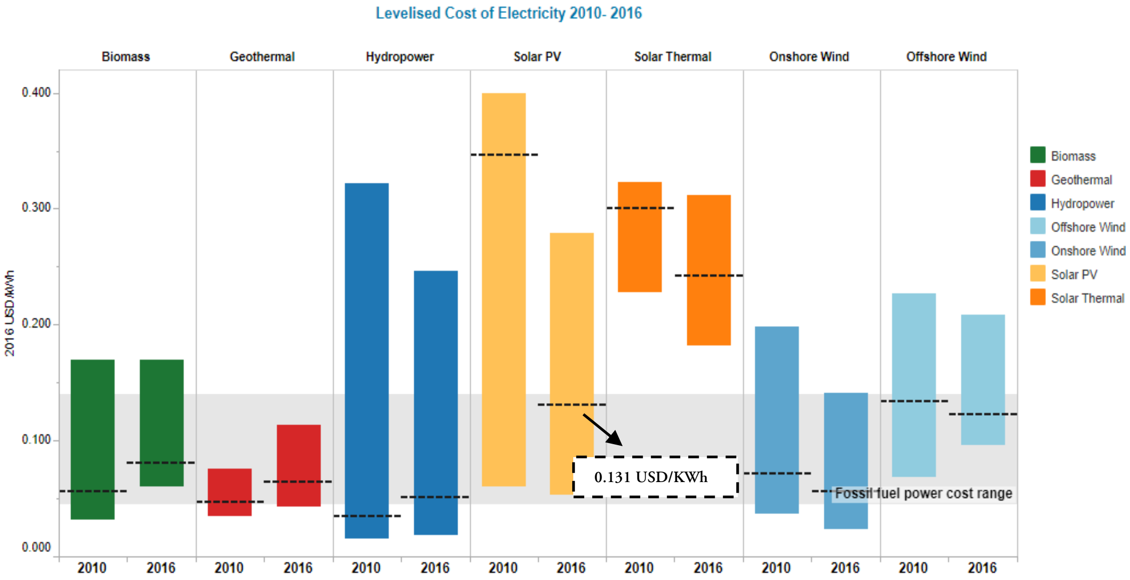


Fig. 1. 6. Levelized cost of electricity of different energy resources pinpoints that solar PV increasingly become more affordable from year 2010 to 2016. [6]

1.2. Thesis Objectives and Outlines

Since silicon is still the main substrate for commercial solar cells, and the Al-BSF has 70% market share, most of the work was focused on understanding the steps to improve the efficiencies at both cell and module levels without increasing the cost.[7] Thus The objectives of this thesis work include the cost effective solar electricity through

(i) design and modeling of simple Al-based solar cells which can be fabricated using the same processing steps, irrespective of substrates,

(ii) use a two-dimensional computer model (PC2D – personal computer two-dimensional) [8] to account for lateral current and voltages to avoid losses and improve the efficiency,

(iii) understand the losses associated with both substrates types; (p and n type) in particular front and rear recombination, shading, and the emitter total area, and

(iv) use this information to design and fabricate bifacial solar cells and then characterize to understand the efficiency limitation.

To decrease the cost without compromising the cell efficiency has been the desire of the PV community. Therefore, this work highlights simple processing sequences to achieve high efficiency, irrespective of substrate type. Both p and n type wafers can have the same Al print and dry on the rear surface, before rapid thermal firing to form either a high-low (BSF) or p-n junction for p-type and n-type substrates, respectively. However, while the p-type high-low junction reduces recombination, the n-type p-n junction forms the emitter but requires high minority carrier life time to achieve high efficiency. Substrate independence process is shown in Fig. 1.7.

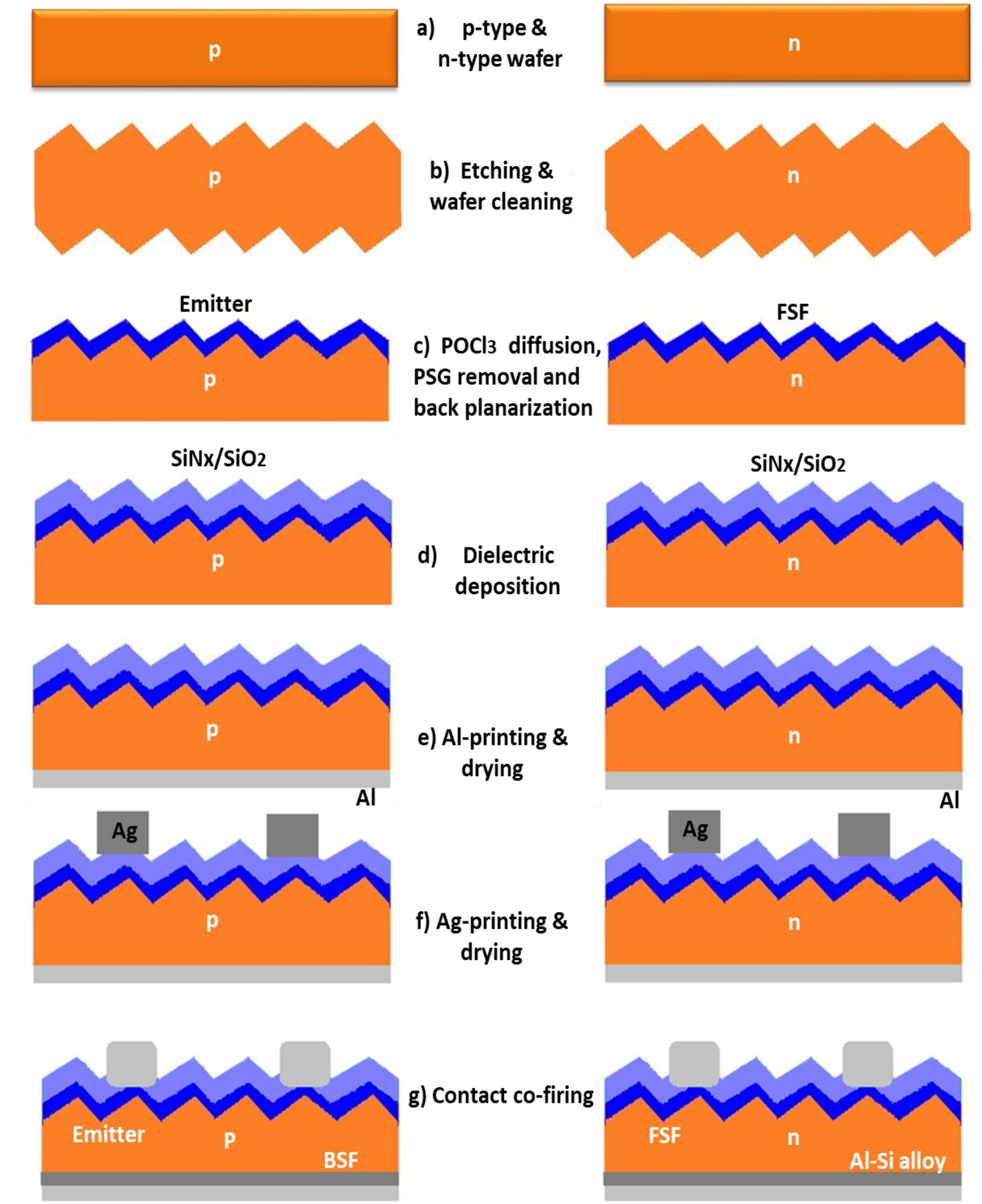


Fig. 1. 7. Identical processing sequences for substrate independent fabrication technique.

Fig. 1.8. shows the current and future prediction of industrial size large area solar cells according to ITRPV [ref]. With advancement of process technologies, the p-type BSF cells can reach ~20% efficiency while the n-type cells can achieve much higher efficiency ~23.5% with slight variation in the design such as in the n type IBC [ref]. Thus, the proposed processing technique - substrate independent has enormous advantage since both n and p type cells can be produced simultaneously. This can also lead to simpler and efficiency matching of cell to module levels. This is demonstrated in Fig. 1.9.

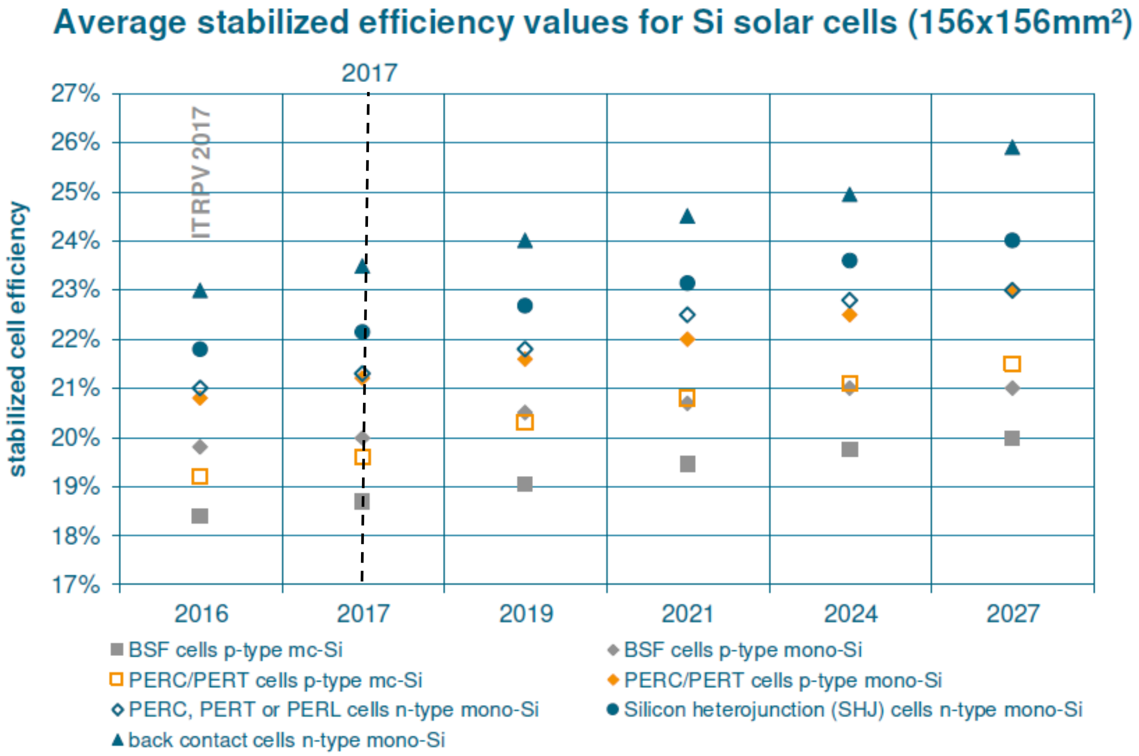


Fig. 1. 8. Average Stabilized efficiency in large area industrial solar cells.[7]

Typically, solar cell efficiency further deteriorates when it is integrated into modules because of the associated series resistance due to ribbon connectors. The efficiency loss is a strong function of mismatch primarily due to the interconnect between the cells in series configuration. [9] The interconnect for same type cells (either p or n type) is usually high

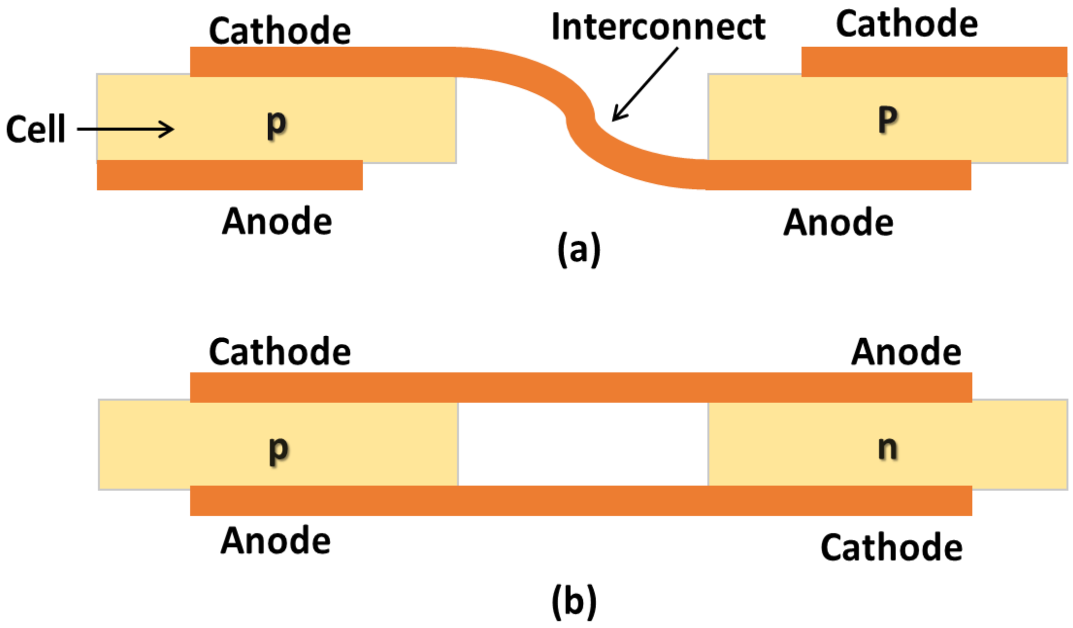


Fig. 1. 9. Interconnection between solar cells connected in series for module fabrication. (a) represents interconnect when same type wafers are connected while (b) represents simpler interconnection thus reducing the mismatch loss.

because of the series connection of anode and cathodes in the adjacent cells. In a module composed of a combination of n and p type cells interconnection can be made quite easily since all anodes and cathodes can be made on the same sides for all cells as shown in Fig. 1.9. This potential advantage further mitigates the loss in the module level and thus could be significant in attaining high module efficiency. [10] One concern in implementing the substrate independent fabrication is the current mismatch in adjacent wafers. To address this, we propose a) to use multiple streamlines to achieve different current output wafers and then, b) opting wafers with same current output to be utilized in the module fabrication.

Finally, by using the understanding from both n and p type cells the bifacial cell structure was investigated to further increase the efficiency through double sided illumination. The prospect of bifacial cell is growing more interest as predicted by ITRV-2017 roadmap in Fig.1.10. The trend behind shifting the interest towards bifacial structure is due to the more output power generation utilizing both front and rear sides of the cell. It can be observed that in the next decade percentage of bifacial cells will increase to 30% in the world market share. Hence, simple screen-printed and cost effective bifacial solar cell is explored in this thesis. By adapting the concept of substrate independent fabrication process, additional boron diffusion can be implemented in order to manufacture the bifacial cell as illustrated in Fig. 1.11. This fabrication process will reduce the complexity in the module fabrication and hence mismatch loss can be further reduced. In ref. it is discussed that by using alternate p and n type wafers in the module the interconnect can be much simpler. For this purpose, asymmetric (p or n) cells are needed to be flipped in the module connection. Thus, substrate independent fabrication process has the potentials of establishing simultaneous manufacturing process in the industrial production line.

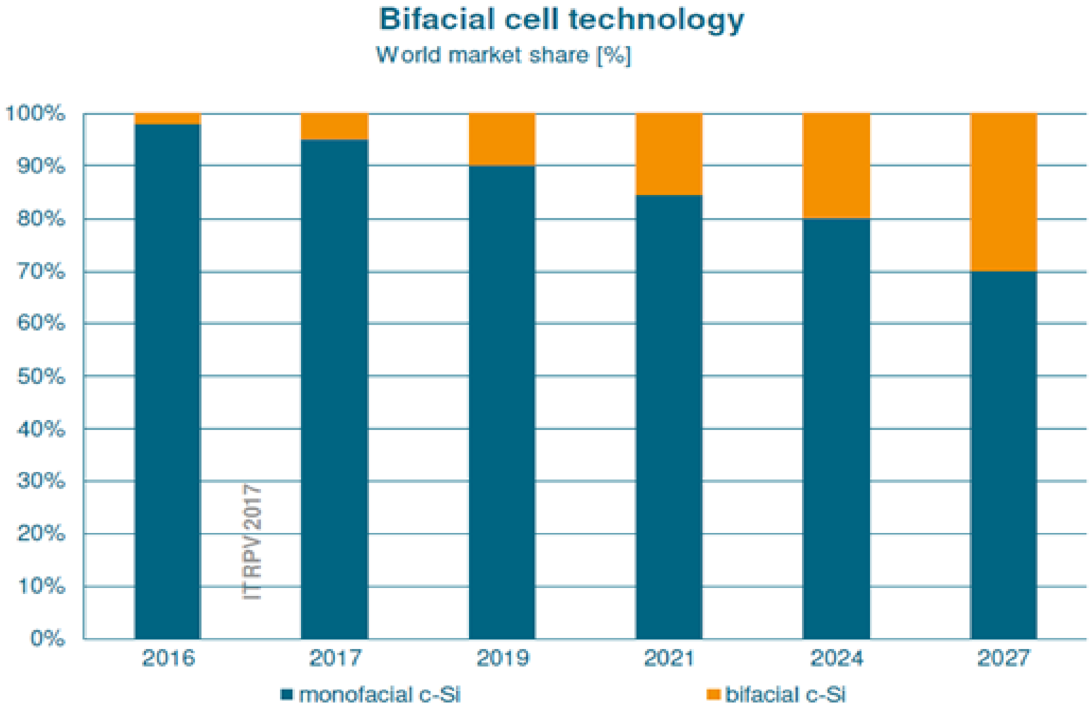


Fig. 1. 10. Prospective of bifacial cell technology in the future Si production line. [7]

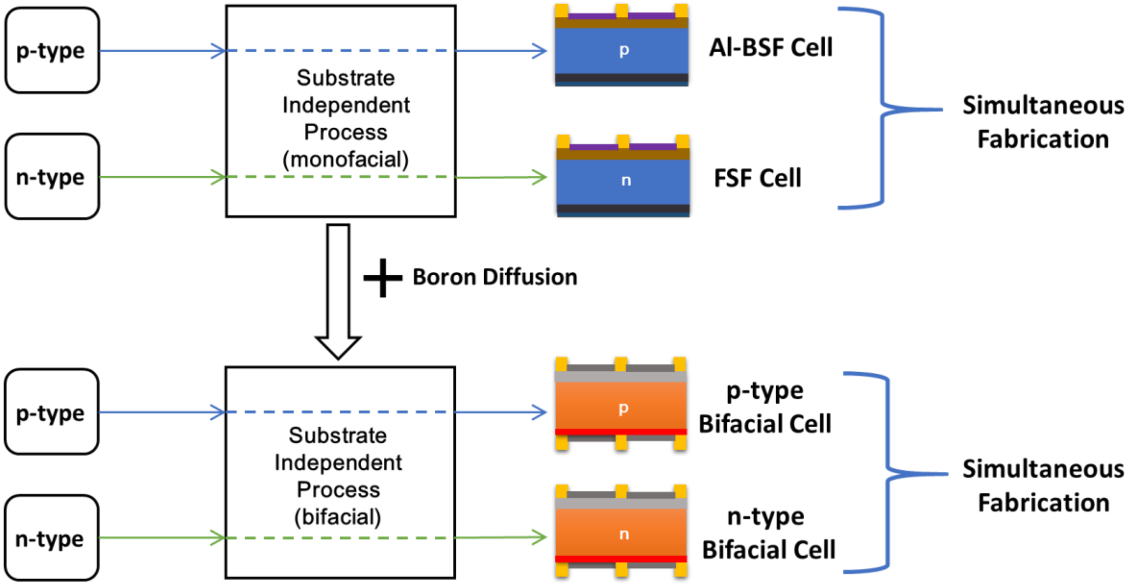


Fig. 1. 11. Substrate Independent Process for both monofacial and bifacial cells.

The thesis is organized in the four clusters; a) first off, basic solar cell working principles of a solar cell, b) Investigation of Al-BSF solar cells through modeling, fabrication and characterization, c) Analysis of FSF cells and d) Exploring the potentials of bifacial. The summary of chapter based discussion are as followed.

Chapter 01 discusses the motivation, statement of the problem and thesis outlines.

Chapter 02 discusses basic working principles of a solar cell. The mechanisms of absorption, generation and transportation is discussed. The equivalent circuit and corresponding electrical output parameters are presented. The loss analysis is explained to understand the specific performance limitation of a solar cell. Finally, characterization tools are discussed in order to interpret the experimental cell results accordingly.

Chapter 03 discusses the modeling, fabrication and characterization of n-type FSF cell. Modeling is performed in the light of PC2D to account the two-dimensional characteristics of device. Specific attention is paid to the front contact metallization design in order to reduce the Ag cost. The electrical characterization includes I-V characteristics, Suns-V_{OC} lifetime measurement, contact resistance measurement and the spectral response of the cell. Finally, a roadmap towards attaining cost effective and high efficiency ~20.50% Al-BSF solar cell is presented.

Chapter 04 encompasses the FSF solar cells modeling, fabrication and characterization. FSF cells are modelled to adapt the concept of extended rear emitter. Lateral characteristics are discussed in detail which is important for carrier conduction in n-type solar cell devices. The prospects of extended emitter are modelled to access the electrical output parameters. Following the modeling, identical substrate independent fabrication process is followed as utilized in the processing of Al-BSF cells. Finally, a blueprint for the attaining ~22% FSF cells is modeled and recommended.

Chapter 05 demonstrates modeling, fabrication and characterization of Bifacial Solar cells. Due to the bifaciality characteristics the cell was experimentally measured from both sides of the cell. The difference between from the front and rear side electrical output parameters are discussed subsequently. The loss analysis is discussed to further improve the cell performance. Finally, a roadmap to achieve cost effective and high efficiency ~21.68% bifacial solar cell is presented.

Chapter 06 enlists the future work including novel metallization design and Al_2O_3 rear passivation of bifacial solar cells.

CHAPTER 02: BASIC WORKING PRINCIPLE OF A SOLAR CELL AND GENERAL MEASUREMENT TECHNIQUES

2.1. Introduction

In this chapter, the basic working principles of a solar cell, electrical and optical losses, and the measurements techniques are discussed. Understanding of every layer with the associated losses is critical to design and modelling of solar cell. Measurement techniques such as the light-voltage measurements, Suns_V_{OC}, Lifetime, internal quantum efficiency etc. provide the electrical and optical output parameters for a given solar cell structure.

2.2. Basic Working Principles of a Solar Cell

A solar cell is an optoelectronic device that converts the optical energy to electrical energy without any polluting bye product. The illumination sunlight is the primary source of energy consumption. The working of a solar cell relies on three basic principles: a) Absorption, b) Generation and c) Collection.

2.2.1. Absorption

When a solar cell is exposed to sunlight, the total energy absorbed depends on the optical properties of the device such as the metal coverage, absorber surface, anti-reflection (AR) coating thickness and refractive index, and the surface area. The absorption also depends on the thickness and bandgap of the semiconductor material – direct or indirect. When incident sunlight has a certain energy greater than the bandgap, the electron and hole pairs are generated as shown in Fig 2.1. However, if the incident sunlight energy is less than the bandgap of the absorber, there will be no absorption, thus heat generation, which is unwanted. The incident sunlight energy required to generate the electron hole pairs can be expressed in the following relationship:

$$E = \frac{hc}{\lambda} \tag{2.1}$$

Where h is the Boltzmann constant~ 1.38×10^{23} k, c is the speed of light and λ is the wavelength of the incident sunlight. For instance, in silicon material, the incident sunlight energy should be greater than >1.12 eV, which the bandgap of Si.

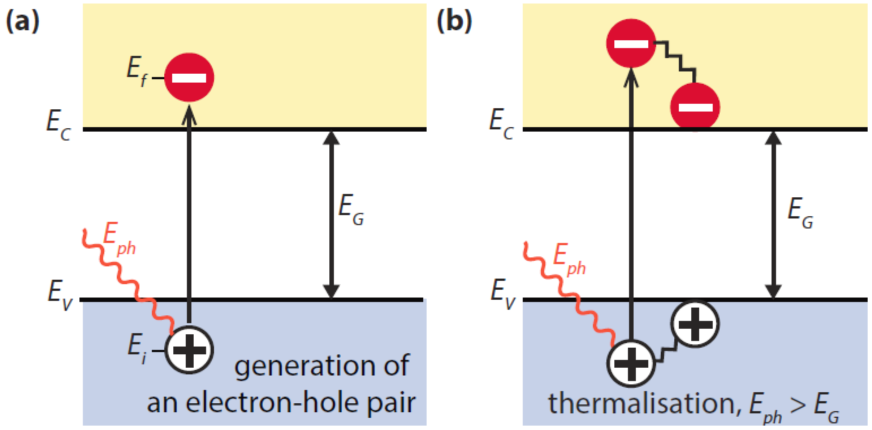


Fig. 2. 1. Absorption mechanism when (a) incident sunlight has energy greater than the bandgap (b) Rest of the energy is transferred to heat energy. The image is taken from ref. [11]

2.2.2. Generation

A solar cell is a p-n junction, which carriers on each side of the junction leads to the creation of an electric field. Generated electron hole pairs created after the absorption mechanism is impacted by this internal electric field. The minority carrier electrons in the p side in vicinity of the junction is transferred to the n side. Same happens to the minority carrier holes in the n side which is transferred to the p side. This phenomenon is further explained in Fig. 2.2. Electron-hole pairs created relatively far from the junction thus need to be involved in this process. Therefore, it is important to maintain a high bulk lifetime which causes diffusion length to be long enough such that electrons and holes located far from the junction can be collected without recombining themselves. Typically, for a solar cell operation diffusion length should be three times larger than the device length.

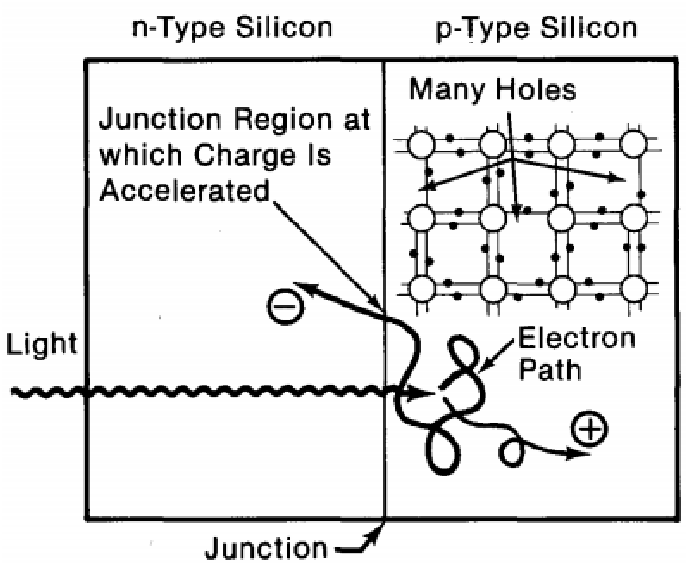


Fig. 2. 2. Charge carriers swept to the n side (electrons) by the internal electrical field at the p-n junction. The image is taken from ref. [12]

2.2.3. Collection

After generating electron-hole pairs, electrons at the n side (which essentially a majority carrier) and holes at the p side (majority carrier) accumulate therefore a charge imbalance is created. These free charge carriers cannot cross the junction due to the potential barrier created by junction. In this condition, if an external load is connected the electrons at the n side travel through the load and spend energy before it recombines at the p side contact with a hole. This spent energy is the source of electricity. A pictorial illustration of absorption, generation and collection is shown in Fig. 2.3.

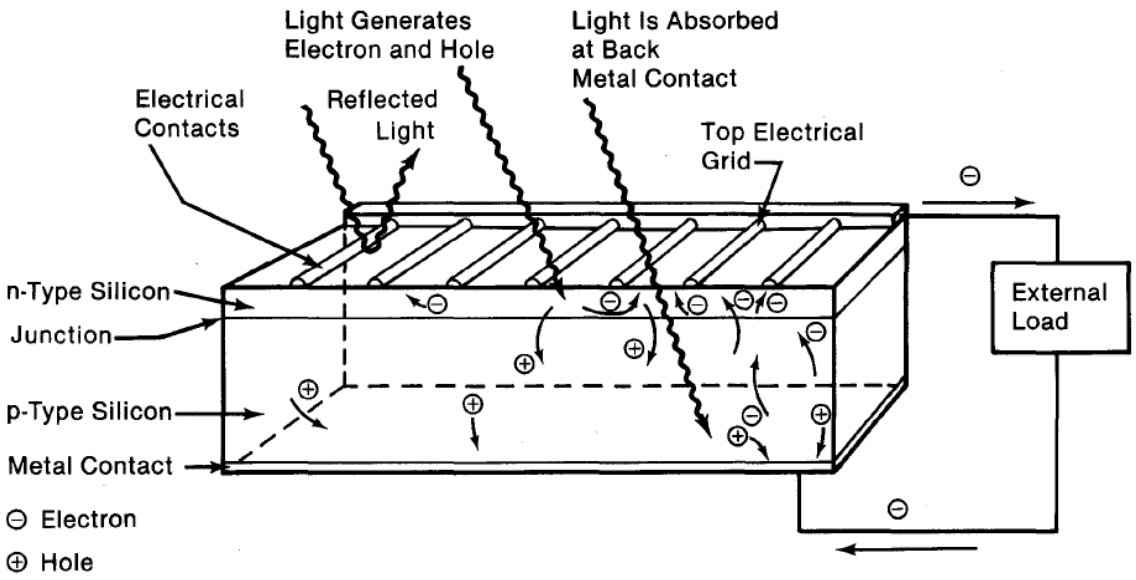


Fig. 2. 3. Basic working principle of a solar cell. The image is taken from ref. [12]

2.3. Electrical Equivalent Circuit

The electrical equivalent circuit of a typical solar cell is presented in the one-diode model as shown in Fig. 2.4. The current-voltage relationship can be written as,

$$\boldsymbol{I} = \boldsymbol{I_L} - \boldsymbol{I_O}\left[\exp\left(\frac{\boldsymbol{qV}}{\boldsymbol{nkT}}\right) - \boldsymbol{1}\right] \tag{2.1}$$

Here, I_L is the light generated current, I_0 is the recombination current inside the diode, v is the voltage across the solar cell, n is the ideality factor, k is the Boltzmann constant, and T is the temperature. In standard test condition, T=298 K (25 ^{0}C).

In the short circuit condition, voltage across the terminal is zero and the current represents the maximum current that can be collected from the solar cell. From the above relation when V=0,

$$\boldsymbol{I_{sc}} = \boldsymbol{I_L} \tag{2.2}$$

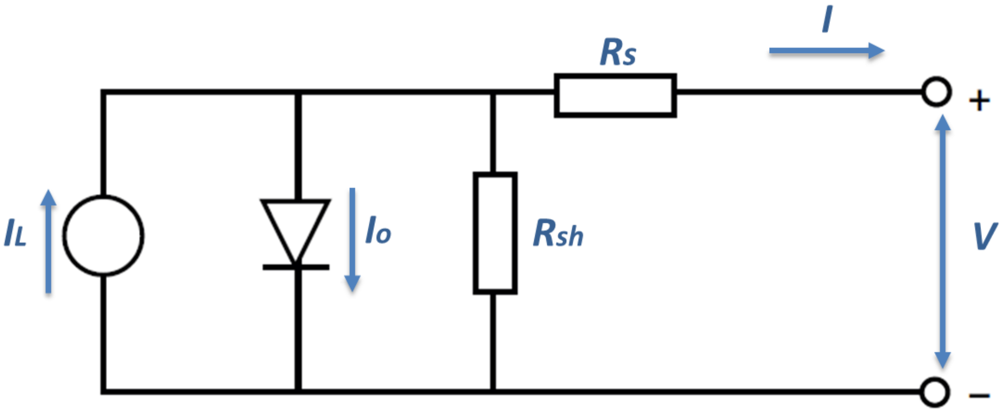


Fig. 2. 4. Electrical equivalent circuit of a solar cell.

The Isc is called the short circuit current which is a function of total generation, hole diffusion and electron diffusion lengths,

$$I_{sc} = qG(L_n + L_p) \tag{2.3}$$

In the open circuit condition, current inside the solar cell is zero and the maximum attainable voltage across the solar cell terminal is called as open circuit voltage, Voc. From equation (2.1), if I=0 then V=Voc

$$0 = I_L - I_O\left[\exp\left(\frac{qV_{OC}}{nkT}\right) - 1\right]$$

$$V_{OC} = \frac{nkT}{q}\ln\left(\frac{I_L}{I_0} + 1\right)$$

$$V_{OC} = V_T \ln\left(\frac{I_L}{I_0} + 1\right) \tag{2.4}$$

Here, V_T is called the thermal voltage, in STC, $V_T = 25mV$. It should be noted that, ideality factor (n) is ~1 in the simplified relationship (2.4). However, practically n might deviate from 1. For a good solar cell, n~1-1.10.

2.4. Loss Analysis

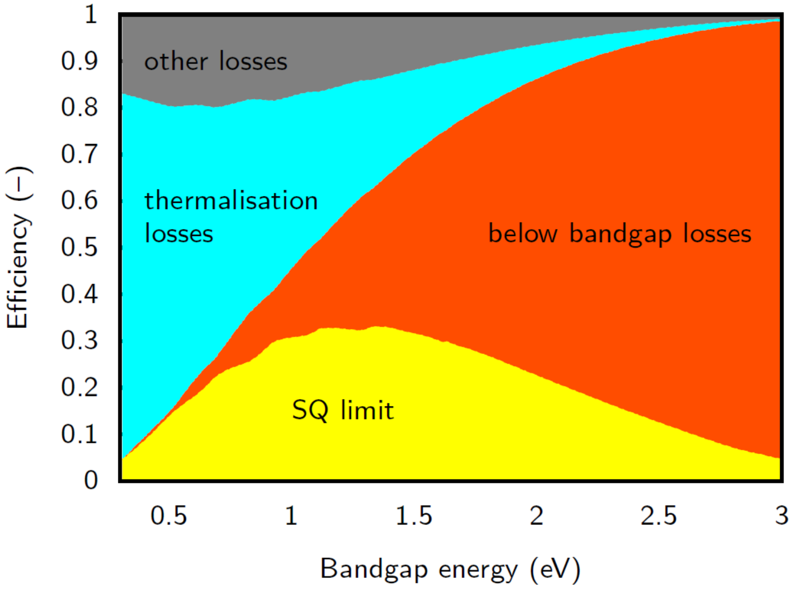


Fig. 2. 5. Schockley Quessier Limit and related efficiency loss in a p-n junction. The image is taken from ref. [11]

The Schockley Quessier limit determines maximum efficiency attained by a p-n junction device as shown in Fig. 2.5. However, this assumption only considers the direct bandgap materials. Hence, indirect bandgap material such as Si is limited to only ~30% efficiency. Recently. Ritcher et al [13] calculated highest efficiency that can be attained by a Si solar cell device as ~29.43%. In a practical solar cell, both electrical and optical loss contribute to the performance degradation. A brief discussion of most dominant electrical and optical loss is presented here.

2.4.1. Optical Loss

Optical loss directly impacts the current generation in a solar cell. In order to obtain maximum short circuit current, optical loss must be curbed considerably. Optical loss primarily consists of (i) absorption, (ii) reflection, and (iii) shading.

2.4.1.1. Absorption Loss

When light is incident on the solar cell, the intensity of light decreases as it travels through the device. This is known as Lambert-Beer law that can be formulated as,

$$I(d) = I_O \exp(-\alpha d) \tag{2.5}$$

Where IO is the incident lights intensity and d is specific distrance that light travels inside the cell. Since, incident light also transmits through the device, therefore the total absorption can be quantified by substracting the transmitted from abosrbed light.

$$I^{abs}(d) = I_O - I_O \exp(-\alpha d) \tag{2.6}$$

Fig. 2.6. shows aborption coefficeints of some common semiconductor materials. It can be observed that materials that have lower bandgap have absorption at higher wavelengths. For example GaAs has absorption at higher wavelengths. Also absorption coefficient depends on the type of bandgap. For example GaAs and InP are direct bandgap materials, hence have better absorption compared to Si at visible wavelengths (400-700 nm). For Si, blue has the highest absorption coefficient and thus most of the blue wavelength lights are absorbed within a few nanonmeter at the front side of the cell. At the same time, the red light is abosbed well in the optical path length of ~60 µm. Beyond the optical path length ~100µm infrared light is hardly absorbed and almost 90% of the light is transmitted.

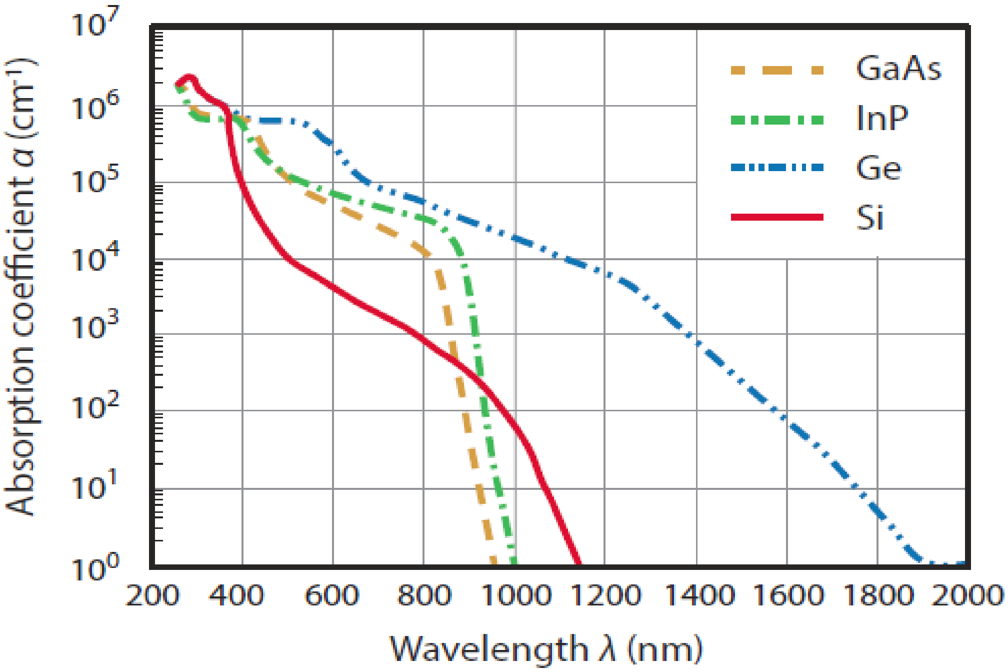


Fig. 2. 6. Absorption coefficients of common semiconductors. The image is taken from ref. [11]

In a solar cell, since all light is absorbed in all layers of the cell, absorption loss in every layer needs to be considered which is known as parasitic absorption. This can be quantified as internal quantum efficiency, IQE_{OP}.

2.4.1.2. Shading Loss

Due to the contact metallization, the incident light sees an obstruction at the front side. This causes total irradiance reduction and thus lower current generation. The shading loss can be interpreted as metallization factor which quantifies total metal fraction (A_M) to front surface area (A_{Total}),

$$F_M = \frac{A_M}{A_{Total}} \tag{2.7}$$

One approach to reduce the shading loss is to utilize finer gridlines at the front metallization. However, this in turn increases the series resistance and lowers FF. Thus, an optimization is needed to achieve maximum current generation without compromising the FF.

2.4.1.3. Reflection Loss

Incident sunlight is not absorbed completely due to the reflectance loss. Reflection in a solar cell can be categorized as:

a) Front surface reflection and
b) Rear surface reflection

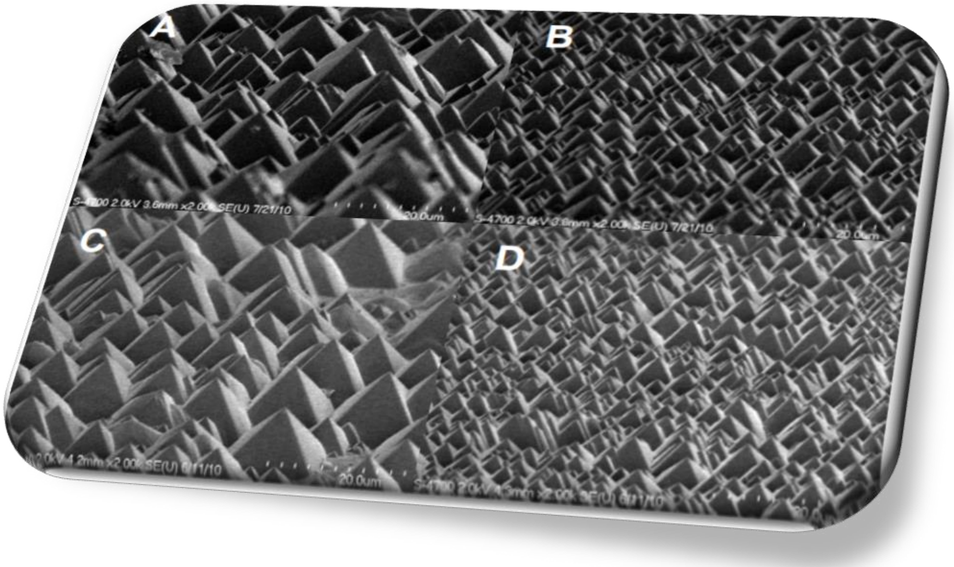


Fig. 2. 7. Textured surface with different clean chemistry.The image is taken from ref [15]

To minimize the reflection at the front surface two techniques are applied usually, a) texturing and b) antireflection coating (ARC) deposition. Texturing front surface allows more absorption by increasing optical path length. A typical texturing technique is the random pyramid structure as illustrated in Fig.2.7. Another commonly textured technique is the inverted pyramid.

Commonly used antireflection coating layer for the screen printed solar cell is SiN_X. The thickness of anti-reflection coating is chosen such that dielectric material is one quarter of the wavelength of incoming to ensure minimum reflection.

$$d_{ARC} = \frac{\lambda_O}{4n_{ARC}} \tag{2.8}$$

Where, λ_0 is the wavelength of the incident light, n_{ARC} is the refractive index of dielectric material and d_{ARC} is the thickness of the ARC layer.

2.4.2. Electrical Loss

2.4.2.1. Resistive Loss

Resistance loss impact cell performance severely, especially the FF. The FF decreases due to high series and low shunt resistances.

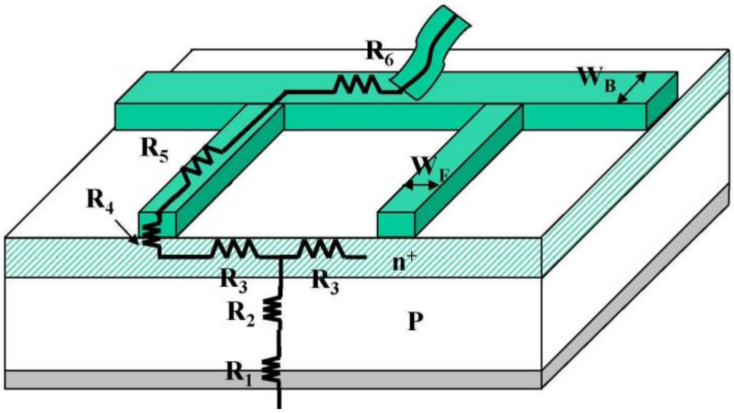


Fig. 2. 8. Components of series resistance (RS) in Al-BSF cell.

For a solar cell. series resistance has six components which is shown in Fig. 2.8. Here,

a) R_1= Resistance in the rear back Al contact.

b) R_2= Base resistance,

c) R_3= Emitter Resistance.

d) R_4= Contact Resistance between metal and Si.

e) R_5= Gridline resistance.

f) R_6= Busbar resistance.

The shunt resistance however originated from the shunting of rear Al to the front metal Ag. Another shunting path is in the Si/gridline interface due to over-firing of the front metal contact. The leakage current via shunt resistance affects the cell performance drastically and reduces FF.

2.4.2.2. Recombination Loss

The recombination loss governs V_{OC} directly in the cell performance. Recombination naturally represents the phenomenon of electrons falling on to the holes and thus creates nonexistence of minority carriers in the device. Considering the device perspective, with a moderate lifetime, there is less chance of recombination in the base. On the flipside, recombination at the surfaces are very predominant due to the surface non-regularity characteristics. Both front and rear surface thus need to be well passivated to minimize the recombination. Moreover, from the material perspective recombination can be classified as:

a) Radiative

b) Auger, and

c) Shockley-Read-Hall.

To consider the effect of all recombination in the device, following relationship can be written [14],

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{SRH}} \quad (2.9)$$

The minority carrier lifetime τ reduces as the recombination occurs. Therefore, to achieve a high minority carrier lifetime recombination needs to be minimized.

2.5. General Measurement Techniques of Solar Cell

This section outlines the detail measurement and characterization techniques that is used in solar cell process. The electrical characterization includes I-V measurement, Suns-V_{OC} measurement, WCT-120 photoconductance lifetime measurement, Internal quantum efficiency measurement and 4 point-probe contact resistance measurement.

The I-V measurement extracts the electrical output parameters of a solar cell by utilizing flash lights mimicking one sun intensity. The Suns-V_{OC} measurement gives the cell V_{OC}, Pseudo efficiency and FF without series resistance, while WCT-120 lifetime tester is measures the minority carrier life time of the cell. Spectral response and quantum efficiency measurement traces the recombination at various locations in the device, such as bulk, front and rear surfaces. Finally, contact resistance measurement with 4-point probe was utilized to measure the contact resistance of a solar cell.

2.5.1. I-V Measurement

The I-V measurement of solar cell is a key tool to determine the electrical output parameters of a solar cell. The I-V graph extracts comprehensive device parameters: R_S, FF, V_{OC}, J_{SC}, n and η. Additionally, pseudo FF data is seemingly important to attain the maximum squareness from a solar cell. In Fig. 2.9. I-V curve of solar cell is shown in dark and illuminated conditions. The most important feature is the maximum power point condition which indicates highest FF achievable from a sample solar cell. The series resistance recorded at this point is the total series resistance of a solar cell. For a finished cell, n factor should be around ~1. A high ideality factor >1 is an indication of over fired contact or/and shunt resistance. Thus, to optimize the contact firing, an n factor of close to 1 along with low R_S is expected.

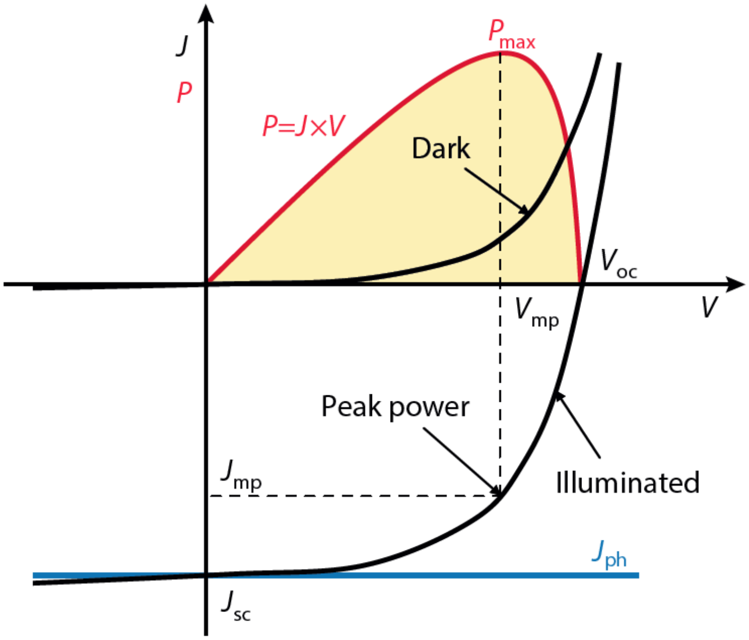


Fig. 2. 9. Solar Cell I-V curve in dark and under illumination. Image is taken from ref. [11]

2.4.2. Suns-V_{OC} measurement

The Suns-V_{OC} measurement is a key technique to interpret the material characteristic of the solar cell device. The effect of series resistance is not taken into account during this measurement, thereby material property and shunting can be realizable from the measurements. In Fig. 2.10 Suns-V_{OC} measurement is shown in contrast to the light IV measurement. The pseudo FF measurement gives the opportunity to gauge highest FF that can be achievable in this technique. Other notable features are V_{OC} at 0.1 sun and V_{OC} at 1 sun where first measurement signifies V_{max} at the maximum power point condition and later measurement represents the implied voltage free from series resistance. Voc independent of series resistance is also called implied voltage. This can be shown as,[15]

$$V_{OC} = \frac{kT}{q}\ln\left(\frac{(N_A + \Delta n)\Delta n}{n_i^2}\right) \tag{2.10}$$

Finally, output shunt resistance is considered to measure the shunt resistance which might be rooted in the material property or overfired contact during the belt furnace contact formation. Even though, Jo1 and Jo2 are two other parameters that need to be low enough for a good solar cell performance, however these are the fit parameters rather than the correct representation of recombination currents in the quasi-neutral regions and space -charge regions.

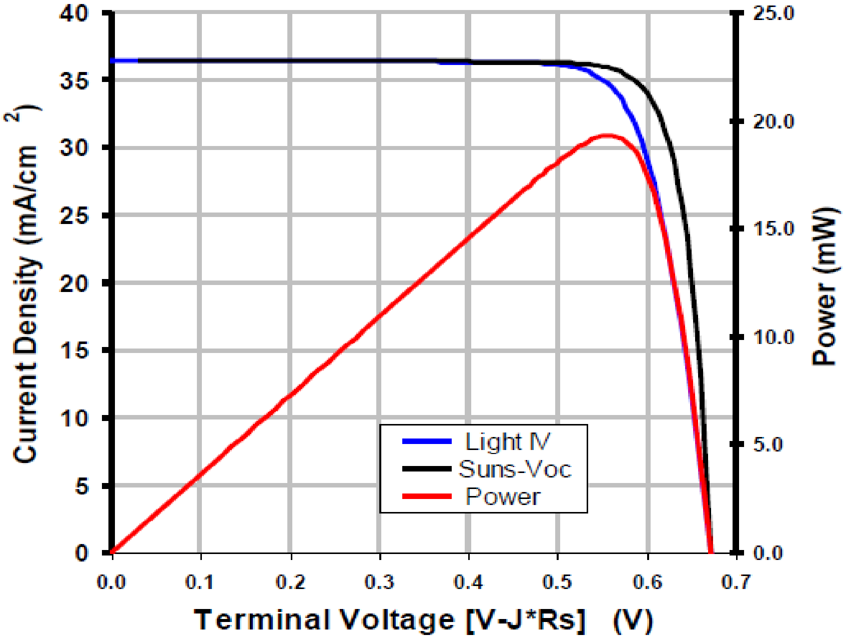


Fig. 2. 10. Deviation of Suns-Voc I-V curve from light I-V curve due to independence of series resistance effect. The image is taken from ref. [14]

2.4.3. Photoconductance Lifetime Measurement

The photoconductance lifetime tester is a crucial tool for determining device characteristics at different development stages of the solar cell. The contactless measurement is illumination dependent and creates minority carrier lifetime graph and inverse lifetime graph which is independent of Auger recombination. The effective lifetime of a solar cell is the combination of bulk lifetime, front surface passivation, S_{front} and rear surface passivation, S_{rear}, [16]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S_{front}}{W} + \frac{S_{rear}}{W} \tag{2.11}$$

Where, W is the thickness of the test wafer. In lifetime measurement technique, both front and rear surface passivation are dependent on excess carrier concentration. Therefore, (2.11) can be modified as,

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{J_{0f}(N_d + \Delta n)}{qn_i^2 W} + \frac{J_{0b}(N_d + \Delta n)}{qn_i^2 W} \tag{2.12}$$

Where, J_{0f} and J_{0b} represent recombination current at front and rear surfaces, respectively; Δn is the excess minority carrier and N_d is the dopant concentration.

2.4.4. Contact Resistance Measurement

The 4-point probe quantifies the contact resistance and emitter sheet resistance via transmission length method. The concept was first proposed by Wenner in 1916 with the aim of measuring earth resistivity. [17]Later Valdes utilized this method for the application in semiconductors.[18] In 1964 Shockley first proposed to use this technique in metal-semiconductor interface. [19]The strip width needs to be maintained at 2mm for this measurement technique. The current is injected into the probes and corresponding voltage is measured in both directions. With a varying length between the probes, contact resistance can be calculated for several positions. And finally, the average of the multiple points of the contact resistance can be calculated accordingly.

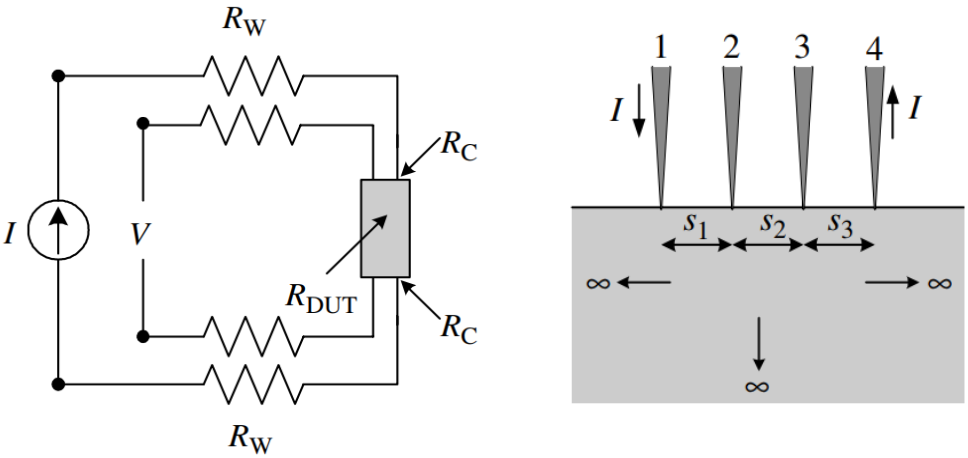


Fig. 2. 11. Four-point probe contact resistance measurement technique. The image is taken from ref. [18]

2.4.5. External Quantum Efficiency

The external quantum efficiency quantifies the fraction of the number of carriers collected to the number of photons incident on the device. If each photon contributes a carrier to the electrical conduction then quantum efficiency is 1, which is an ideal case. As shown in Fig. 2.12 the quantum efficiency of a solar cell however varies on the photon wavelengths. External quantum efficiency can be written in following expression:

$$EQE = \frac{Collected\ Carriers}{Incident\ Photon}$$

$$= \frac{I_{ph}(\lambda_o)}{e\varphi_{ph}(\lambda_o)} \tag{2.13}$$

The deviation to the ideal case generally caused by the recombination in the device. The front surface recombination dominates at the blue wavelength response. Since in a typical p type solar cell the emitter is very narrowly formed at the front side, the emitter diffusion length also influences the external quantum efficiency. The middle range represents recombination at the bulk and diffusion length. Since, recombination at the base is quite low, the resultant external quantum efficiency is close to 1. Rear recombination and base lifetime governs the quantum efficiency for long wavelength photons.

In the measurement technique, a xenon gas discharge lamp was used along with filters and monochromator to provide the wavelength range required for this purpose. With a photodetector, the incident photon flux was quantified, and an ampere meter measures the minority carrier collection.

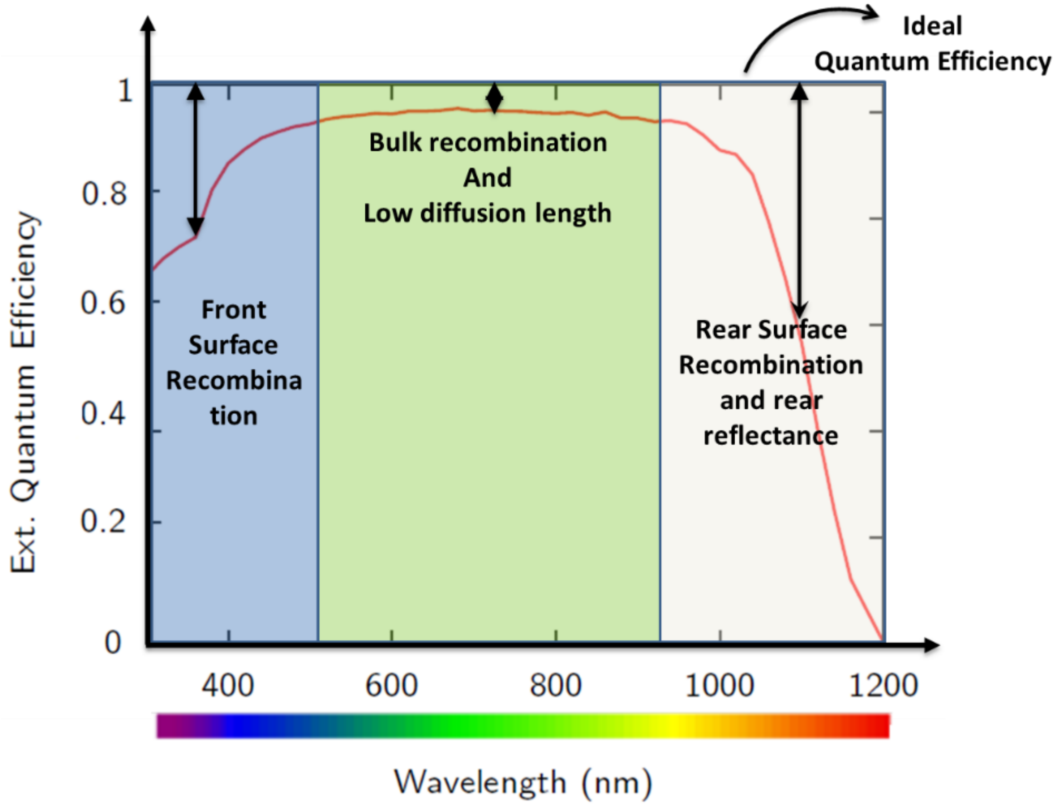


Fig. 2. 12. External Quantum Efficiency and various recombination in a solar cell.

2.5. Summary

Basic solar cell principle along with common measurement techniques are discussed in this chapter. These measurement techniques are applied directly during the characterization of the fabricated solar cells. Additionally, detail loss analysis reveals major optical and electrical loss pertinent to the performance degradation of a solar cell. In order to improve the cell performance both optical and electrical design must be considered simultaneously.

CHAPTER 03: DESIGN, MODELING, FABRICATION AND CHARACTERIZAION OF Al-BSF SOLAR CELLS

3.1. Introduction

The most simple solar cell structure in today's PV arena is the full Al-BSF structure. In this chapter design, modeling and characterization of Al-BSF structure is carreid out. PC2D computer software, was employed which accounts for lateral and longitudual currents in the device. Following the modeling technique simple substrate independent fabrication process is implemented. Since, Ag metallization cost is a concern behind high cost of Al-BSF cells, special attentions were give in the front contact design. Finally, a roadmap for attaining high efficiency cost effective Al-BSF cells is presented in commerical screen-printing technique.

3.2. Design Approach of Solar Cell

Fig. 3.1. illustrates a typical thought process that goes into the design of a solar cell. Since a solar cell is an opto-electronic device, both optical and electrical considerations must be made to overcome efficiency losses. Reflections, absorptions and transmissions associated with a) ARC layer, b) metal contact and c) passivation layers of front and rear side are solely responsible for optical performance of a solar cell. On the flipside, a) recombinations at front surface, bulk area and rear surface, and b) resistive characterisitcs at metal contacts, emitter, FSF layer and BSF layer are the contributors to electrical output performance. In this section, we layoout the layer by layer design approach to attain high efficiency industrial size cell.

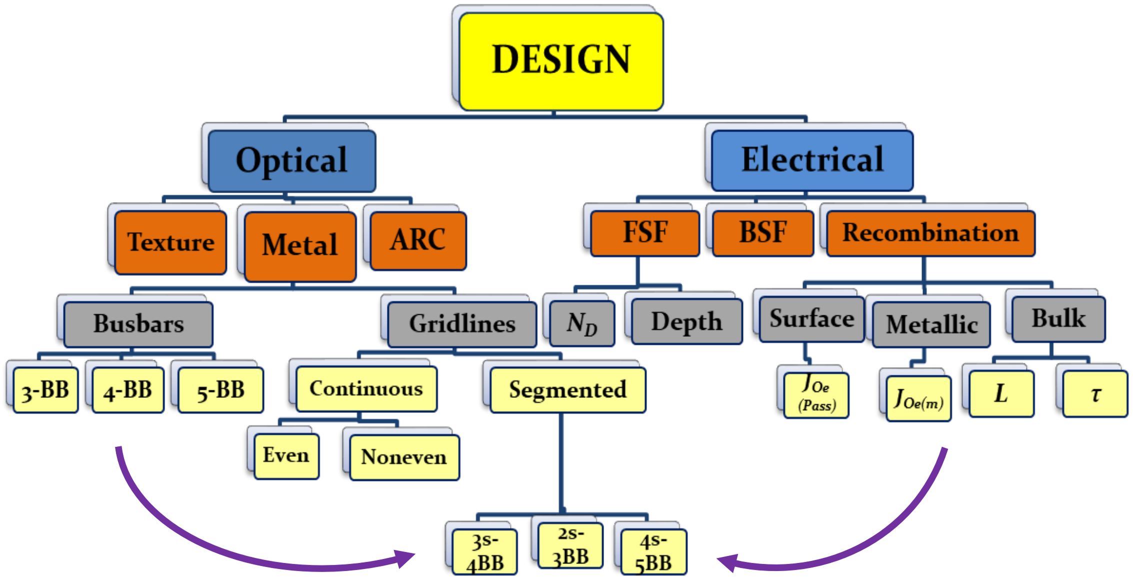


Fig. 3. 1. Flow Diagram for the simulation algorithm in PC2D.

3.2.1. Metal Contact Design

Metal Contact is an important aspect that influences both electrical and optical performance of a solar cell. As shown in Fig. 3.1, designing metal contacts can vary the cell performance significantly. In a typical solar cell, metals contacts can be breakdown to gridlines and busbare primarily. These metal contacts influences shading loss, gridline resistance and recomboniation current underneath the metals. Moreover, highly expensive silver paste consupmtion also depends on the metal gridline design and metallization technologies. [27] For instance, the front metal coverage of a conventional screen-printed silicon solar cell is about 5-8%. Therefore to achieve <5% shading loss with the gridline width of <50 μm is a goal with current current screen-printed technology. However, total series resistance increases as the contact area shrinks with decrease in gridline width. To maintain high FF while improving the gridline geometry street concept was introduced in our earlier paper in ref. [12]. The schematic of steet concpet in metallization design is shown in Fig. 3.2. with the conventional 3BB no street design. Furthermore, in ref. [28] it is shown that with 5-BB design FF can be increased campered to the 3-BB design. A 5-BB design combining with streeet design is shown in Fig. 3.3. To exploit both electrical and optical performance we predominantly used 4s-5BB design throughout this thesis.

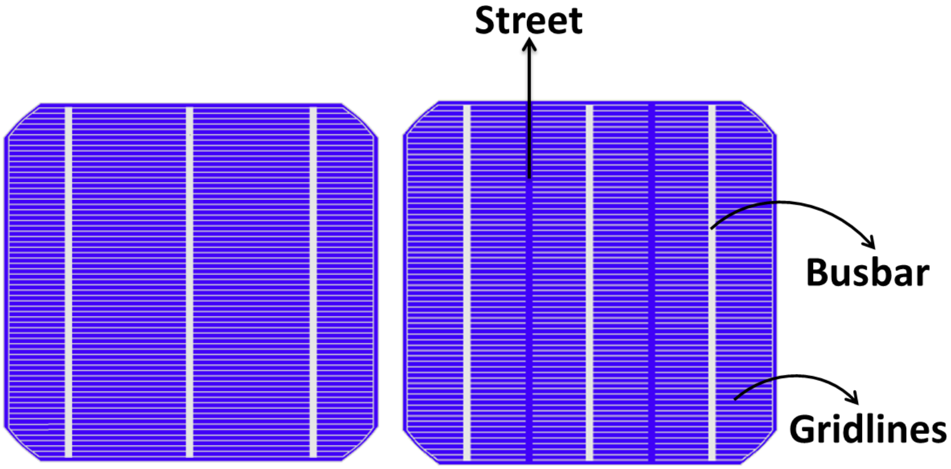


Fig. 3. 2. Street concept in 3 BB (left) design results 2s-3BB (right) design.

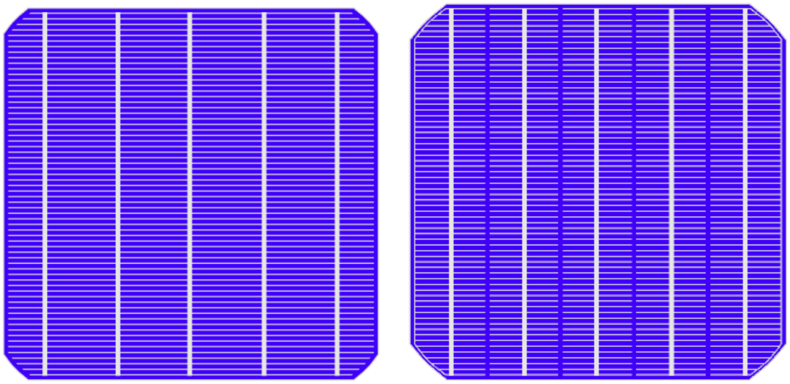


Fig. 3. 3. Street concept in 5BB (left) design results 4s-5BB (right) design.

3.2.2. Front Surface Design

To ensure the maximum absorption, we used conventional SiNx layer as an ARC layer on the top of front surface along with front metal contacts in the rest of the area. Since, this layer also provides sufficient passivation, experimentally extracted surface recombination velocity (SRV) was used. The ARC layer thickness was optimized using the PVlighthouse

OPAL 2 and Wafer Ray tracer. [20, 21] Since, J_{SC} is limited by the front absorption in ARC layer, we also used double stack SiN_x/SiO_2 layer to imrpove the J_{SC}.

3.2.3. Emitter/FSF Design

The emitter in p-type cell (or, FSF in n-type cell) design influences electrical performance of a solar cell. Current trend of high sheet resistance >80 Ω/sq. approach is adopted during the cell design. The low doping concentration associated with high sheet resistance reduces recombination in the emitter and also passivation is better in a high sheet resistance emitter. [28-31] However, the contact resistance is effected due to high sheet resistance emitter which can be shown in following relationship, [22]

$$\rho_c \propto \frac{1}{N_d} \tag{3.1}$$

Here, ρ_c is contact resistivity and N_d is emitter doping concentration. To ensure the low contact resistance, therefore Ag paste needs to be developed such that contact resistance becomes independent of doping level. One such approach is to use tellurium based glass in the Ag thick paste which has the potential to reduce contact resistance. [32-35] In our design, we maintained 80-100 Ω/sq. sheet resistance with optimized Ag paste to reduce the contact resistance accordingly. Another approach is the selective emitter approach which allows high doping concentration underneath the metal contact and thus reducing the contact resistance. However, this is an additional process to the existing streamline process and we utilized this approach only during the modelling of PERC structure. Practically, with the secondary ion mass spectrometry (SIMS) technique the doping concentration was determined and during the modelling we used extracted data obtained from experiment. The emitter depth of ~0.35 μm was maintained with this high sheet resistance.

3.2.4. Base Design

During the base design, it is important to note the effect of diffusion length on the cell performance. A high diffustion length allows minority carrier to contribute in the carrier collection prior to recombination. It also depends on the type of the material, wafer processing technique and doping concentration of wafer. Even though, a highly doped base is desired to ensure better electrical property in the device, however it reduces the diffusion length and thus lowers V_{OC}. Moreover, diffusion length is a function of minority carrier lifetime. Therefore, an optimization of diffusion length, doping concentration and minority carrier lifetime is need for opting a particular base doping concentration. In our study, we used 2 ohm-cm base for the p-type cells with minority carrier lifetime varying from 50 µs to 200 µs. For n-type materials we used high base resistvity >10 ohm-cm material to account the high injection with a minority carrier lifetime in the range of ~1000 µs to 10000 µs. In the n-type cell since junction is on the rear side, thereby a relatively high lifetime base was utlilzed to ensure maximum collection.

3.2.5. BSF Design

The premise of BSF formation is to reduce recombination in the rear surface of a p-type cell. A high-low junction (n^{++}/n^{+}) in the rear surface repels minority carrier electrons from the base side to recombine at the rear surface and hence imroves V_{OC}. The BSF has high significance specially on the cells where rear side fully Al printed. In our design, BSF in p-type cell (or emitter in n-type) was chosen based on the Al-Si alloy formed by the rear surface screen pinted Al contact. Such standard BSF is around ~0.4 µm with 3×10^{18} cm^{-3} doping concentration.

3.2.6. Rear Surface Design

Since Al-BSF and FSF cells have fully screen-printed Al in the rear side, the rear transmission is set zero for these structures. For the bifacial cell, the rear side was made mostly transparent along with the local metal contacts.

3.3. Modeling of Solar Cell in PC2D

Based on the design four different structures of solar cells are modelled in this section. The input parameters for the modelling are industrially compatible or extracted from theoretical calculation. The PC2D modelling software is used for this purpose. Since, the solution mechanism considers both lateal and longitudinal currents, important lateral properties such as, current crowding and lateral voltages are encompassed during the modelling. During the modeling in PC2D, other simulation softwares such as, PC1D, OPAL2 and Wafer Ray Tracyer are also employed to deliver the optimum input parameters. Detail algorithm for the PC2D simulation softwars is presented in Fig. 3.4.

The PC2D solves the simulation region based on 20 by 20 metrices. The simulation region based on a unit area that is compatible for the entire area of a cell. In unit rows generally represents the lateral length or surface area and colums represent the length towards the depth or thicckness of the device. By providing input parameters based on the contact and noncontact area the metrices can be designed. For an instance, while simulating Al-BSF cell, the left most colum is kept 1 and the other areas are gives 0 for ARC/ passivated layer. The simulation input parameters furhter require information on optical and electrical device parameters. The optical parameters include tansmission, haze, diffuse reflectance and spectral refleceance for both front and rear sides. Typically these values are opted from the experimental reflectance and quantum efficiency data to match entire spectrum. It is important to note that, front metallization design also plays a critical role in the optical input parameters. Since gridlines obscures the front illumination, transmission under the gridline column needs to be designed to represent the correct metallization factor (F_M). For an example, if a 5% F_M is designed, the contact column transmission is set 0% and the rest of the area is 100% for the passivated region. The calculation of F_M accounts the contribution of gridlines and busbars. More so, if the rear side is fully opaque (Al-BSF, FSF, etc.) then rear transmission is set 0 for the all columns. For accounting rear illumination in case of bifacial cells, 20 columns on the rear side is given input accordingly based on the metallization design.

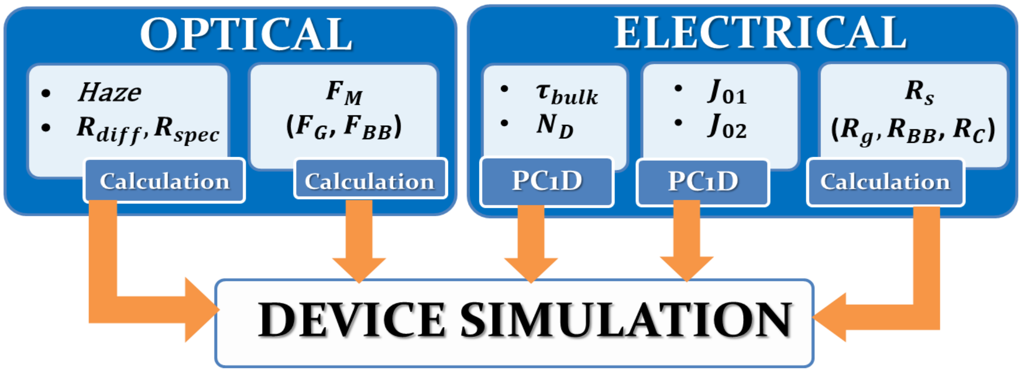


Fig. 3. 4. Flow Diagram for the simulation algorithm in PC2D.

For setting electrical input parameters, F_M is the most important to provide correct contact in the modelling. Moreover, since emitter doping profile effectively determines the surface passivation in the front and rear surfaces, thus recombination current (J_{O1}) were parameterized accordingly based on the variation on sheet resistances. To find J_{O1} for a specific surface, the PC1D is setup with that specific surface layer (texture, doping profile and surface recombination velocity). The base life time was setup very high and rear surface recombination was made nominal. This ensures all the recombination occurring in the front surface. By applying a forward bias of 0.5 volts across the junction, the dark current was calculated with following relation.

$$J_{01} = \left(\frac{I_{dark}}{A}\right) * \exp\left(\frac{V}{V_T}\right) \tag{3.2}$$

Here, V_T here represents the thermal voltage of 25 mV for T=300K. While modelling the J_{O1} it was made sure that all other external circuit elements (series resistance, shunt resistance, etc.) were excluded. The two components of J_{O1} are assigned as J_{OM} and J_{OSiN}. The J_{OM} and J_{OSiN} represents recombination currents beneath the metal contacts and SiN passivated regions respectively.

Finally, an extrinsic series resistance is set for input series resistances which encompasses gridlines, busbar and contact resistances. PC2D internally accounts other series factor such as, base and emitter resistances.

3.4. Modeling of Al-BSF Solar Cell

The modelling of Al-BSF structure maintained the 5BB concept is becoming the mainstream market in PV industry. For the gridline design we adopted the segmented street concept which has the potential of cost reduction while retaining almost same efficiency. The designed cell has industrial size cell area ~156×156 cm^2 area on 2 ohm-cm p-type CZ based wafer. The schematic of the PC2D Al-BSF structure is shown in Fig.3.5. The dotted area is the simulated unit area which is compatible to the entire cell area. As the energy band diagram illustrates in Fig. 3.4., the electrons moved by the electric field go to the front contact and holes go towards the back contact in opposite direction. The BSF helps to reduced recombination at the rear surface by creating high-low junction.

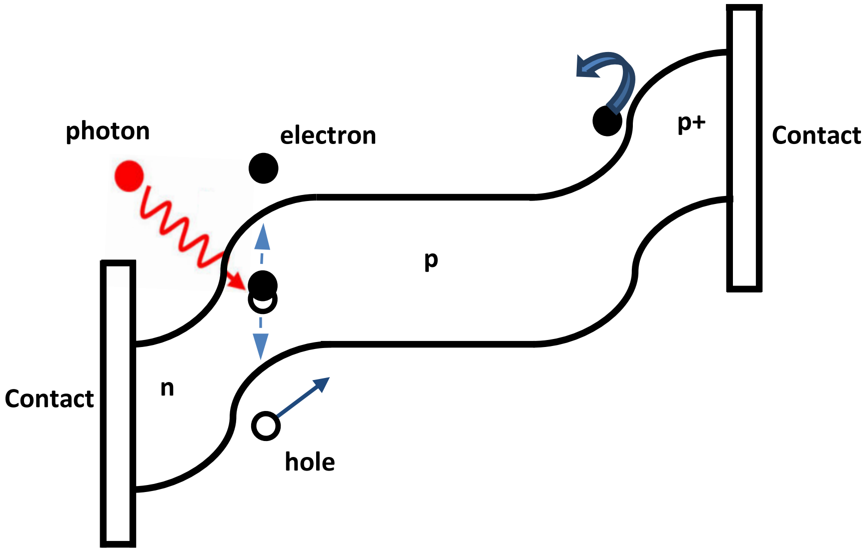


Fig. 3. 5. Energy band diagram of Al-BSF cell.

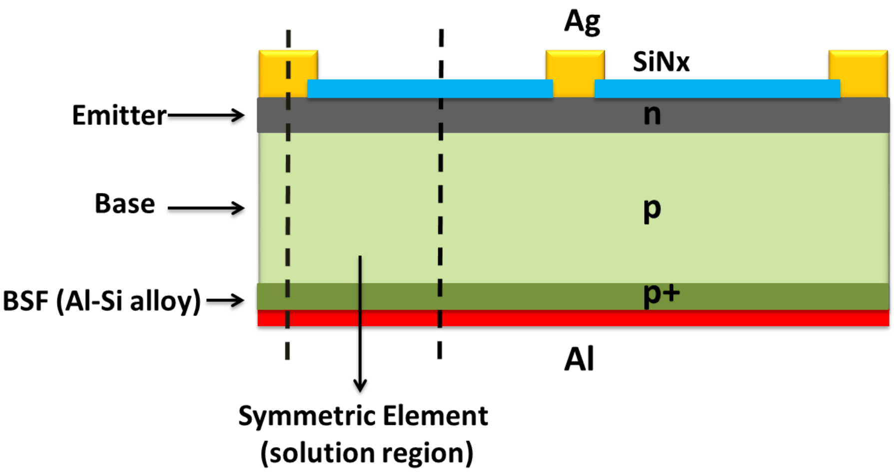


Fig. 3. 6. Device schematic of Al-BSF solar cell in PC2D. the dotted area is the representation of the unit symmetric area repeatable for the entire region of the cell.

3.4.1. Input Parameters

Table 3.1 demonstrates detail input parameters for the modelling of Al-BSF structure. The parameters are extracted either by analytical calculated or from empirical data.

Table 3. 1. Electrical Input parameters for the simulation of Al-BSF Cell

Parameter	**Value**	**Source**
Minority Carrier Bulk Lifetime	1000 μs	Experimental Data
Wafer resistivity	10 Ω-cm	Experimental Data
FSF sheet Resistance	Varied 60-100 Ω/sq	Standard Doping profile
FSF depth	0.35-0.48 μm	Standard Doping Profile
Back-junction emitter sheet Resistance	20 Ohm/sq.	Fabrication Standard
Back-junction emitter depth	10 μm	Fabrication Standard
Gridline Width	55 μm	Screen printed Fabrication Standard
Busbar Width	0.9 mm major, 0.45 mm minor	Uneven Busbar Design
FSF Passivation	100-50000 cm/s	Standard passivation Standard
Metallization Factor (F_M)	3%-5%	Analytical Calculation

3.4.2. Results and Discussion

Table 3.2 demonstrates the electrical output parameters of the modelled cell. The attained efficiency ~20.54% is the best reported efficiency for Al-BSF structure. The major improvement in the cell performance is rooted on the improved FF which can be attainable with optimization of IR belt furnace firing in the contact formation. To attain the Jsc ~39.73 mA/cm^2 emphasize should be given on the optimization of front ARC layer. We propose double ARC layer of SiN/SiO$_2$ which can attain 1.2%$_{abs}$ gain of our previous reported result using only single layer SiN as ARC layer. It should be noted that, we maintained same V_{OC} ~645mV compared to best reported cell which indicates that the wafer lifetime was maintained exactly same. Furthermore, utilizing even a higher life time wafer ~21% Al-BSF is achievable.

Table 3. 2. Simulation Result for Al-BSF Cell

Sample	**Metallization Design**	**Voc (mV)**	**Jsc (mA/cm^2)**	**FF (%)**	**η (%)**
Simulation Cell	4s-5BB	644.96	39.73	80.25	20.54
Best Cell [31]	Continuous-4BB	647.00	38.76	80.92	20.29

3.5. Fabrication of Al-BSF Cell

An Industrial size Al-BSF solar cell is fabricated and characterized in this section. Since Al-BSF cell growth has been almost saturated, special emphasize was given on the cost effectiveness of such structure. We adopted 4s-5BB metallization design as an effort to minimize the Ag cost in a high efficiency cell. The cells were fabricated based on ~156×156 cm^2 area on 2 ohm-cm p-type CZ wafer. The emitter sheet resistance ~80 Ω/sq. was maintained with gridline width ~50 μm in screen printed metallization technique. Fig. 3.7. shows the commercial process flow of detail manufacturing process. At UNC Charlotte Photovoltaic Research Laboratory (UNCC PVRL) we conducted a) back and front screen-printing, b) drying and c) belt furnace co-firing steps. Initial steps were developed by MOTECH in industrial production line.

3.5.1. Screen Printing Technique

In 1970 screen printed technology was first developed. [23] In PV arena, screen-printed metallization technique is mostly commonly used due to its' high throughput and cost-effective nature. In screen printed technique it is critical to a) maintain continuous gridline without any breakage, b) achieve high aspect ratio and c) finer gridline width. To achieve these goals screen-printing was conducted precisely. A schematic of screen-printing process is illustrated in Fig. 3.8.

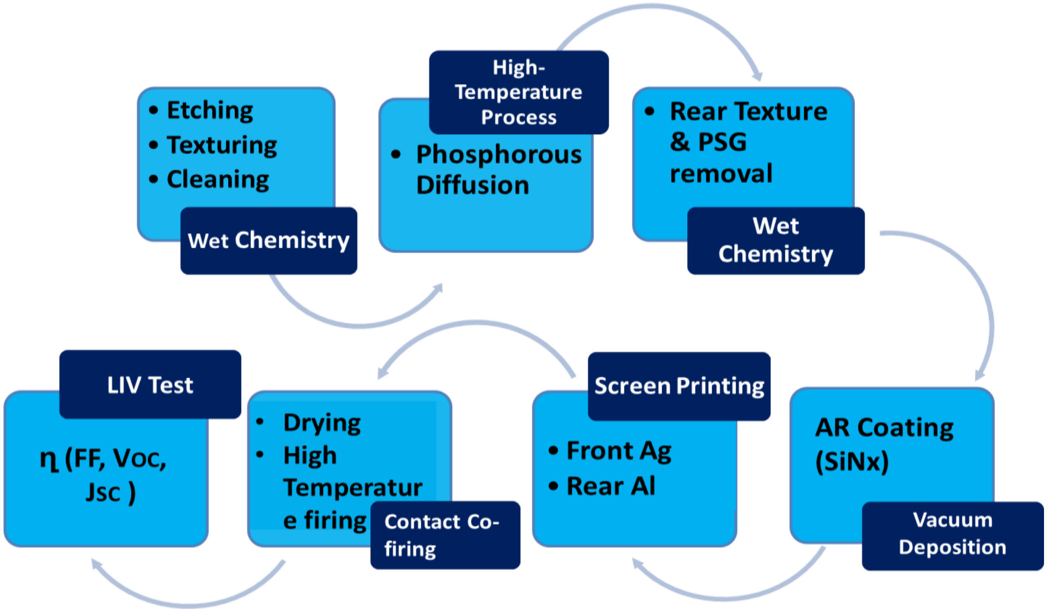


Fig. 3. 7. Standard commercial processing sequence of Al-BSF solar cell.

After placing the wafer on the stage and screen on the holder, pastes are placed on the top of the screen. The printing process has two steps,

a) Printing by front squeegee and push paste towards the back edge and,

b) Spreading paste by front squeegee and push towards the front edge.

The front squeegee is rubber made and tilted with a certain angle which is optimum for printing. In the first step, front squeegee pushes paste through the screen and based on design of the screen the same replica is printed on the wafer. The screen consists of mesh which has wires and emulsion. Paste travels through the opening, thus it is critical to have low viscosity when squeegee pushes the paste. It helps paste to completely go through the screen. However, when paste is placed on the wafer following the first printing step it is important to have viscosity which reduces the chance of spreading. These dual characteristics of paste based on the sheer pressure is called the pseudoplasticity behavior. Moreover, a good printing thus depends on a) snap off (distance between wafer and screen) and b) pressure. High pressure and low snap off is desired for completion of transportation of paste through the screen. However, high pressure and low snap off concurrently increases the chance of spreading and thus wide gridline. Thus, to maintain a fine gridline both snap off and pressure was monitored precisely.

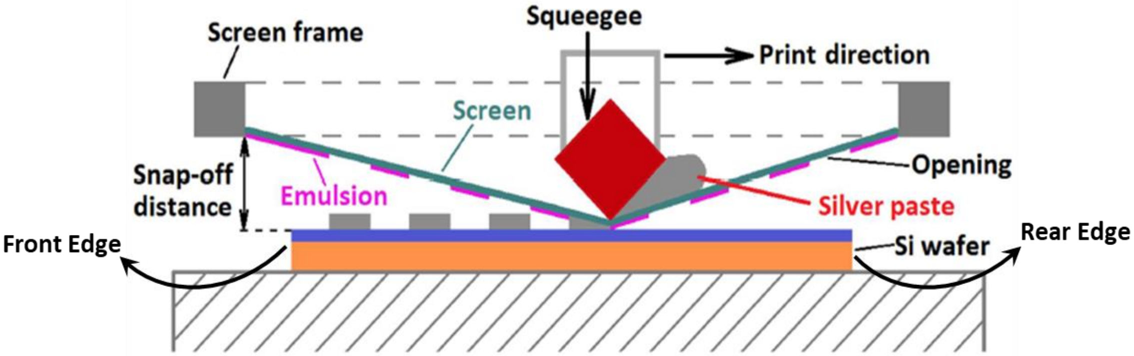


Fig. 3. 8. Standard screen-printing mechanism.

In the second step, the back squeegee spreads paste throughout the screen uniformly and goes to its basic position. The back squeegee is made of stainless steel which has flat polished edge. It is critical to maintain uniform spreading of paste which helps the next wafer to be printed with same precision. Thus, for a batch printing, the back squeegee is critical to maintain uniform printing from wafer to wafer.

Since, Al is fully screen printed at rear side, full area Al printing was conducted accordingly. The only concern with the rear Al printing is maintaining distance from the wafer edge to prevent shunting between front and rear contact. Therefore, precision alignment was maintained during the rear side printing.

3.5.2. Metallization Ag Paste

Metallization paste determines a) printability b) conductivity c) contact resistance, d) solderability and d) adhesivity of printed gridlines. Ag paste is the most widely used in PV to provide these characteristics. Three cluster components; 1) Ag powder, 2) glass frits and 3) organic binder generally form a Ag paste as shown in Fig. 3.9. The metal powder is the main component that shares ~80-90% of the paste. [24, 25] The glass frits assist to etch the dielectric layer and sintering during contact formation. 1-5% glass frits, such as, SiO_2, Al_2O_3, PbO, TiO_2, Te_2O_3, etc. are used for this purpose. The organic binders contribute 1-15% of the paste which influences the paste properties such as, adhesiveness, pseudoplasticity and wettability.

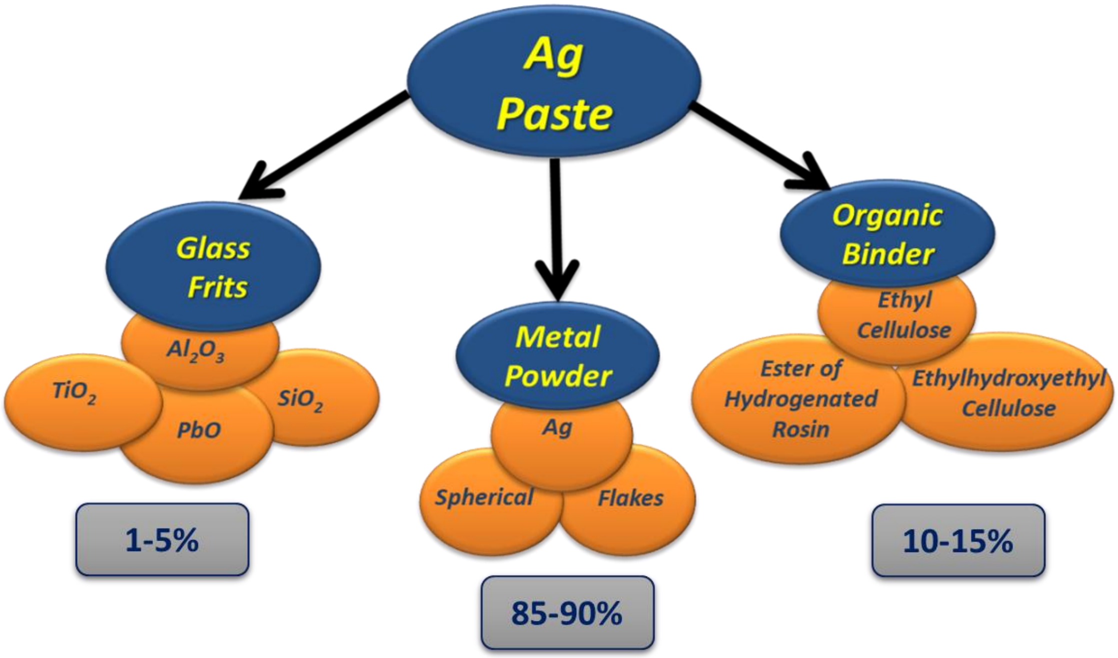


Fig. 3. 9. Major components of commercial Ag Paste.

For the rear side, Al paste was used in this fabrication process. The Al paste is relatively simpler since the full rear area is covered. The rear Al impacts the BSF formation in the cell.

For this purpose, Al contact thickness >10 µm is desired. In our printing, we maintained ~20-30 µm rear Al.

3.5.3. Drying and Contact Co-firing

After printing, both front and rear side was dried ~200 ^{0}C in a belt furnace. Following drying the cells were processed in the IR belt furnace. The IR belt Furnace is the key tool to achieve a high efficiency cell. During contact cofiring a) front contact is formed, b) sintering process occurs, and c) BSF is formed through real Al-Si alloy. Fig. 3.10. shows the firing profile of commercial I-R belt furnace established in the UNCC PVRL laboratory.

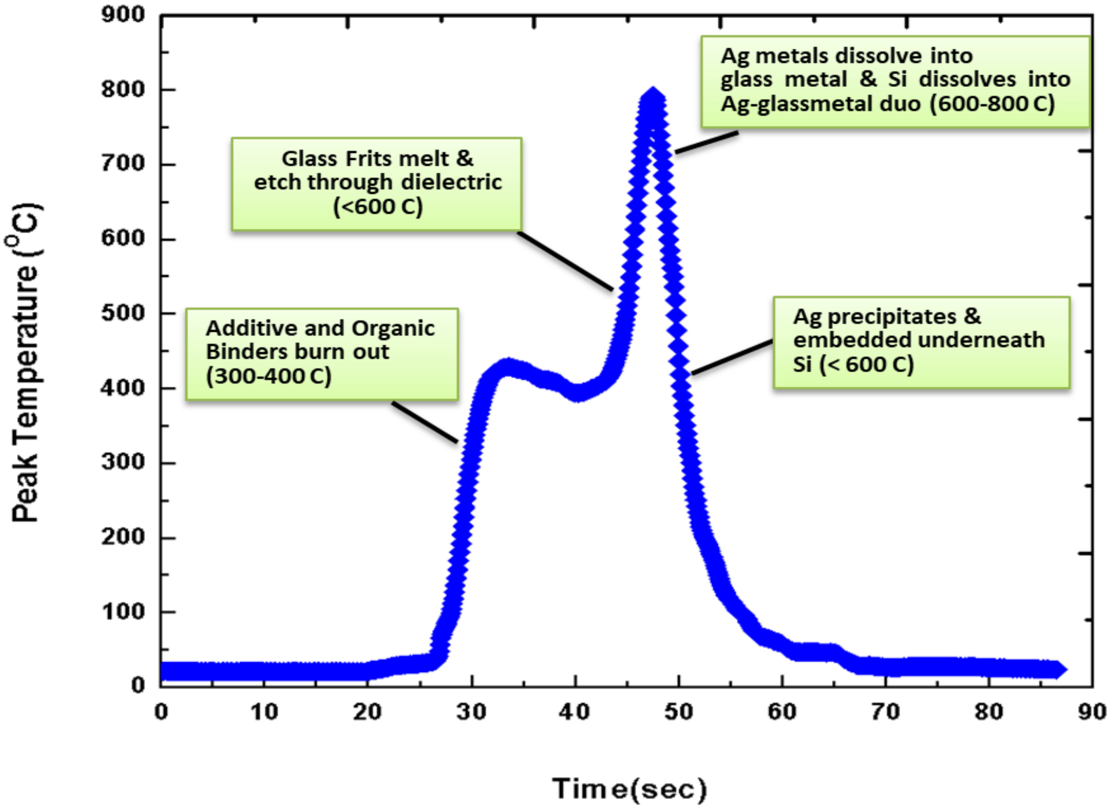


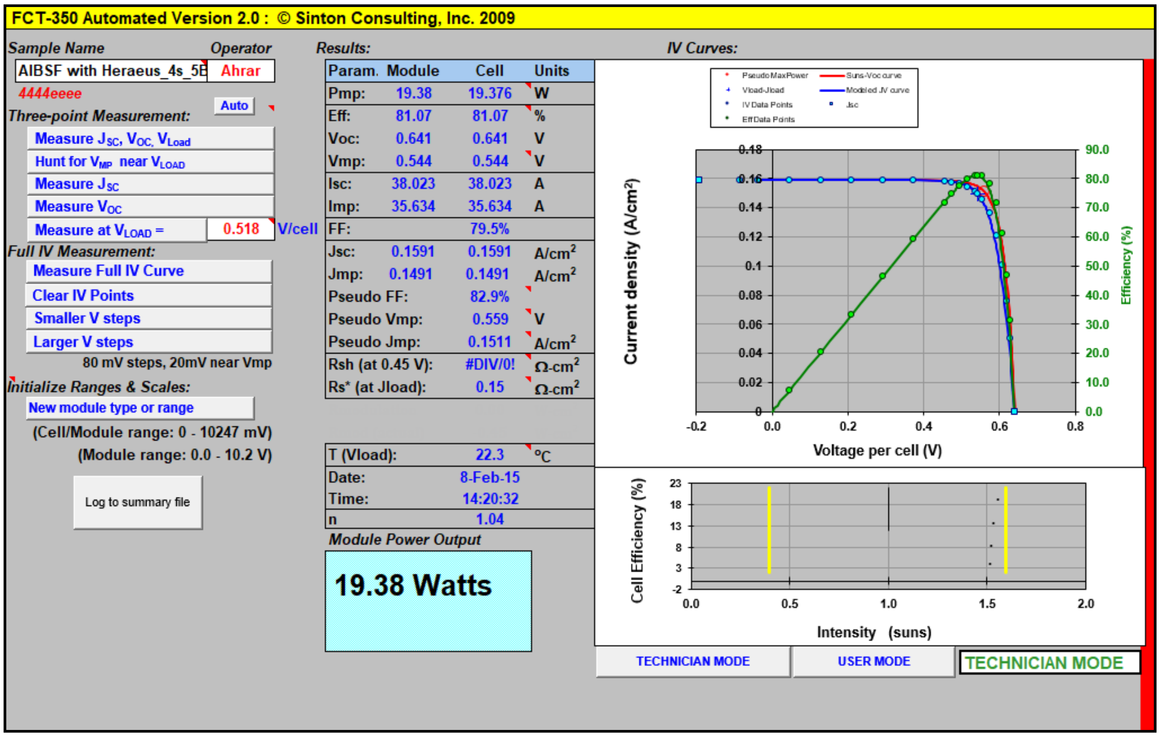
Fig. 3. 10. Firing profile of IR inline belt furnace and front contact formation.

Contact co-firing has six zones with distinct set of temperatures. Zone 01-05 (0-600^{o}C) dries out the rasins and organic binder. And zone 06 is responsible for sintering, contact formation and cool down. The complete mechanism of contact formation depends on the temperatures from the zones. With increase of temperature (i) the organic binders burn out at 300-400°C, (ii) Then glass frits start to metal, etch through the dielectric layer and reduced to its metal, <600°C (iii) Ag metal starts to dissolve into the melted glass frit metals, (such as Te, Pb, etc.) and Si dissolves to these solution, (600-800°C) and (iv) finally during cool down (after 600°C) Ag precipitates and embedded underneath the Si surface. These Ag precipitates are in the crystallite form which provides the pathway for current transportation.

3.6. Characterization of Al-BSF cell

3.6.1. Light I-V Measurement

Fig.3.11. shows the electric output results of fabricated cells. The best cell had efficiency ~ 19.4%. The light IV data for the best cell is shown in Fig.4.5. The V_{OC}~641 mV, J_{SC}~38.03 mA/cm^2 and ideality factor of ~1.04 was achieved. This high V_{OC} is an indication good wafer quality. However, further improvements in V_{OC} can be possible by detail monitoring the contact formation in IR belt furnace. The J_{SC} is in good agreement with the SiN ARC coating. However, J_{SC} can be further improved by optimization the layer thickness. The ideality factor in proximity to 1 represents that contact did not extent close to the junction thus forming an optimized contact. After firing, a high ideality factor generally caused by the overfired contact. In this case, since FF was while maintaining a low n thus reveals a good contact is formed. To further unfold the wafer characteristics, we further proceeded on the characterization in Suns-V_{OC}.



Sample Name: AlBSF with Heraeus_4s_5B

Operator: Ahrar

4444eeee

Measure at V_{LOAD} = 0.518 V/cell

80 mV steps, 20mV near Vmp

(Cell/Module range: 0 - 10247 mV)

(Module range: 0.0 - 10.2 V)

Results:

Param.	Module	Cell	Units
Pmp:	19.38	19.376	W
Eff:	81.07	81.07	%
Voc:	0.641	0.641	V
Vmp:	0.544	0.544	V
Isc:	38.023	38.023	A
Imp:	35.634	35.634	A
FF:		79.5%	
Jsc:	0.1591	0.1591	A/cm^2
Jmp:	0.1491	0.1491	A/cm^2
Pseudo FF:		82.9%	
Pseudo Vmp:		0.559	V
Pseudo Jmp:		0.1511	A/cm^2
Rsh (at 0.45 V):		#DIV/0!	Ω-cm^2
Rs* (at Jload):		0.15	Ω-cm^2
T (Vload):		22.3	°C
Date:		8-Feb-15	
Time:		14:20:32	
n		1.04	

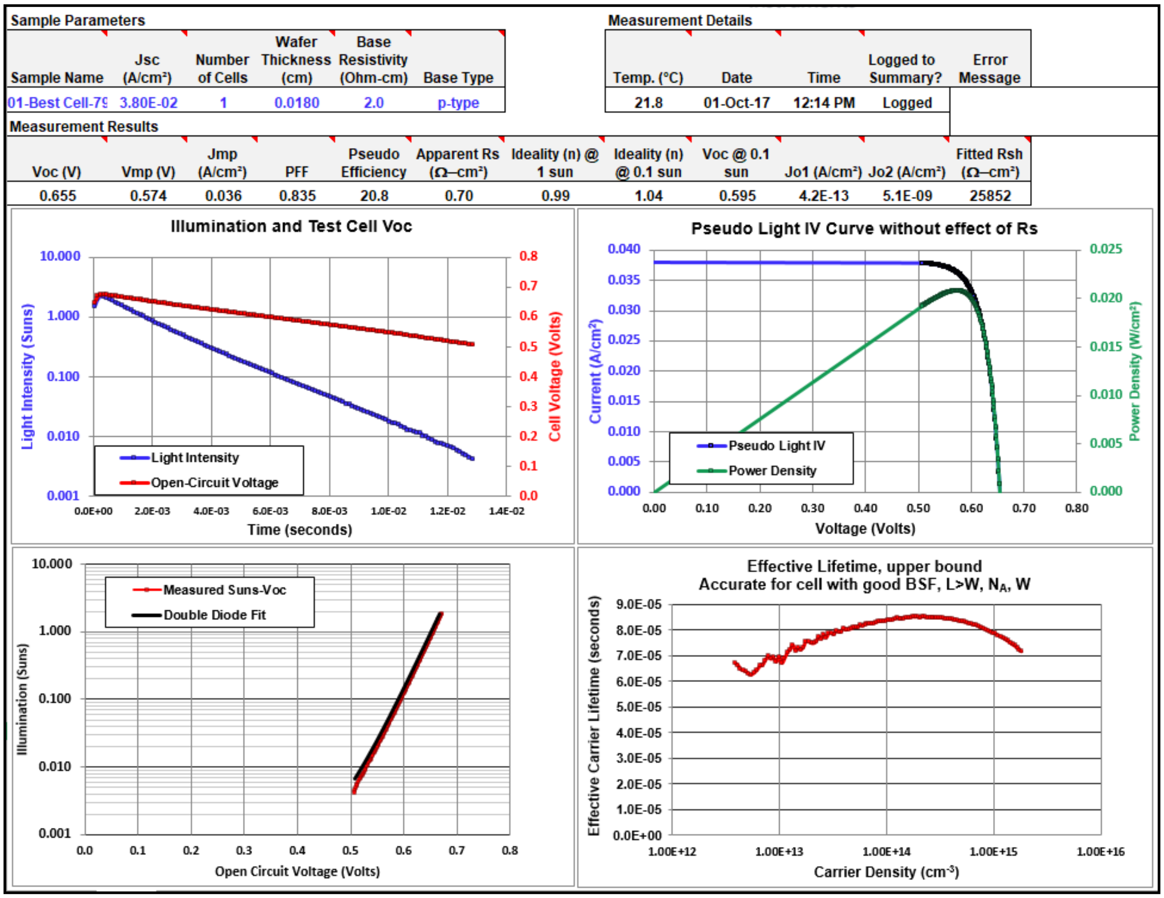
Module Power Output

19.38 Watts

Fig. 3. 11. Light I-V measurement of best Al-BSF cell obtained from Sinton FCT-350 IV.

3.6.2. Suns-Voc Measurement

The Suns-Voc measurement was conducted in SinTon Suns-Voc characterization tool. The pseudo characteristics extracted from Suns-Voc measurement is independent of the series resistance effect. Thus, it shows the maximum implied data can be achievable from such wafer. The Fig.3.12. illustrates the Suns-Voc measurement data for the best cell. The implied Voc of ~ 655mV is an indication of very good wafer quality. However, Voc at 0.1 sun ~595 mV, which eventually became low ~544 mV for the finished cell. This ~50mV is an indication that series resistance related voltage loss is a concern for this cell. To validate this, we further observed n factor at 1 sun and 0.1 sun. The respectively result shows 0.99 and 1.04, which are in good agreement with light IV data. Hence, contact did not affect Voc. Furthermore, low Jo1, Jo2 and Rshunt of 4.2e-13 A/cm2, 5.1e-9A/cm^2 and ~25000 Ω-cm^2 reveals that there is no shunting occurring in this cell. Therefore, we assume that emitter might not be uniform throughout the entire area. Since, Suns-VOC measurement is based on point where probe is placed on the wafer, to get the idea of emitter uniformity we did SunsVOC measurement for multiple points. We found that VOC at 0.1 sun is reduced to 574 mV for some measurements. Thus, based on our observations on the SunsVOC and light IV data we can conclude that a uniform can improve the cell performance significantly.



Sample Parameters

Sample Name	Jsc (A/cm²)	Number of Cells	Wafer Thickness (cm)	Base Resistivity (Ohm-cm)	Base Type
01-Best Cell-7	3.80E-02	1	0.0180	2.0	p-type

Measurement Details

Temp. (°C)	Date	Time	Logged to Summary?	Error Message
21.8	01-Oct-17	12:14 PM	Logged	

Measurement Results

Voc (V)	Vmp (V)	Jmp (A/cm²)	PFF	Pseudo Efficiency	Apparent Rs (Ω–cm²)	Ideality (n) @ 1 sun	Ideality (n) @ 0.1 sun	Voc @ 0.1 sun	Jo1 (A/cm²)	Jo2 (A/cm²)	Fitted Rsh (Ω–cm²)
0.655	0.574	0.036	0.835	20.8	0.70	0.99	1.04	0.595	4.2E-13	5.1E-09	25852

Fig. 3. 12. Suns-VOC measurement of best Al-BSF cell.

3.6.3. Pathway towards achieving high FF in Screen-printing technique

Screen-printing metallization technique became mainstream for the solar cells fabrication in early 1980s. However, the FF was limited when low sheet resistance and high gridline width was used. With the advancement of Ag paste and firing conditions, recently high FF> 81.5 is achieved for the Al-BSF cell fabrication. The evolution of FF is shown in Fig. 3.13.

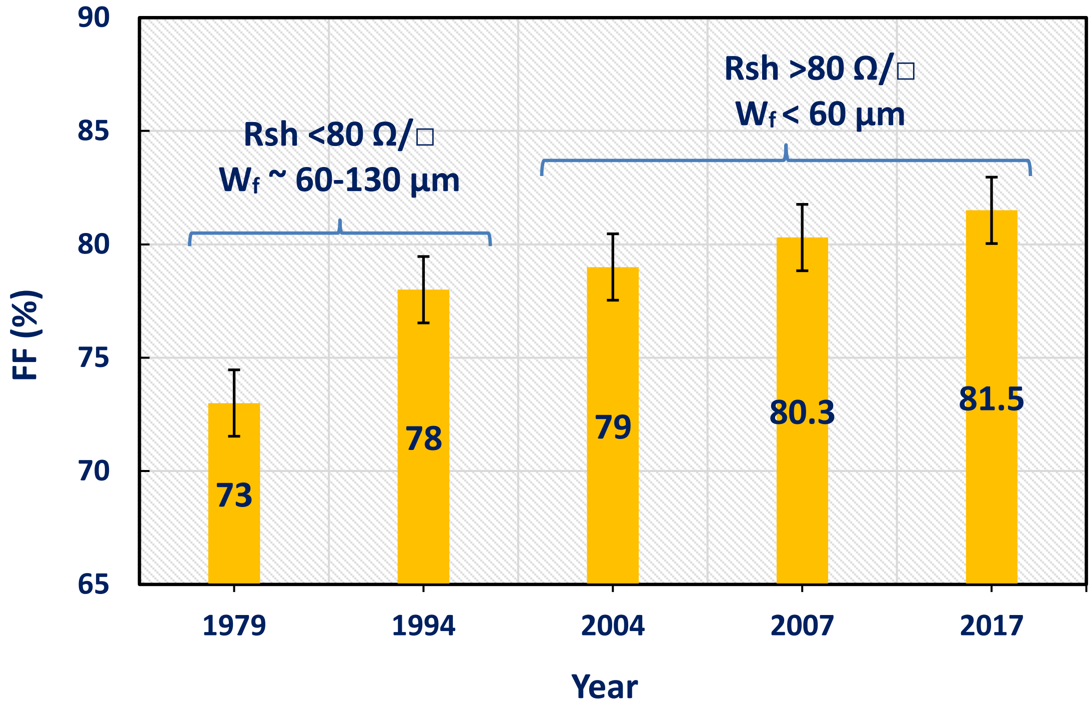


Fig. 3. 13. Evolution of FF reported in the literature. [26-31]

Fig. 3.14. Illustrates various parameters impacting the FF. During the contact co-firing optimization, it was observed that a smaller dwell time (time above >600 C) essentially improved the contact formation. This is due to the fact that a short dwell time improves ramp up rate and ramp up rate. Ramp up rate facilitates to achieve uniform BSF and thus results high V_{OC}. The ramp down rate however, does not allow any oxygen to grow at the front contact which results a low contact resistance. Depending on the paste rheology, glass characteristics the peak firing temperature also need to be optimized such that no over-fire or under-fire contacts are formed. Among the various constituents inside the Ag paste, Ag particle and glass frits mostly determine the contact resistance property. Glass frits needs to etch the dielectric layer, Moreover, the glass frits metal need to be conductive which improves the conductivity between bulk Ag metal and Si. Besides maintaining contact resistance gridlines also need to be continuous and void free which helps to maintain a low

gridline resistance. To achieve a low gridline resistance, paste properties such as, viscosity, pseudoplasticity, wettability and slumping need to set optimum. In this context, the printing parameters such as, printing pressure, printing speed and snap off also play a critical role to maintain good gridline resistance while not losing aspect ratio.

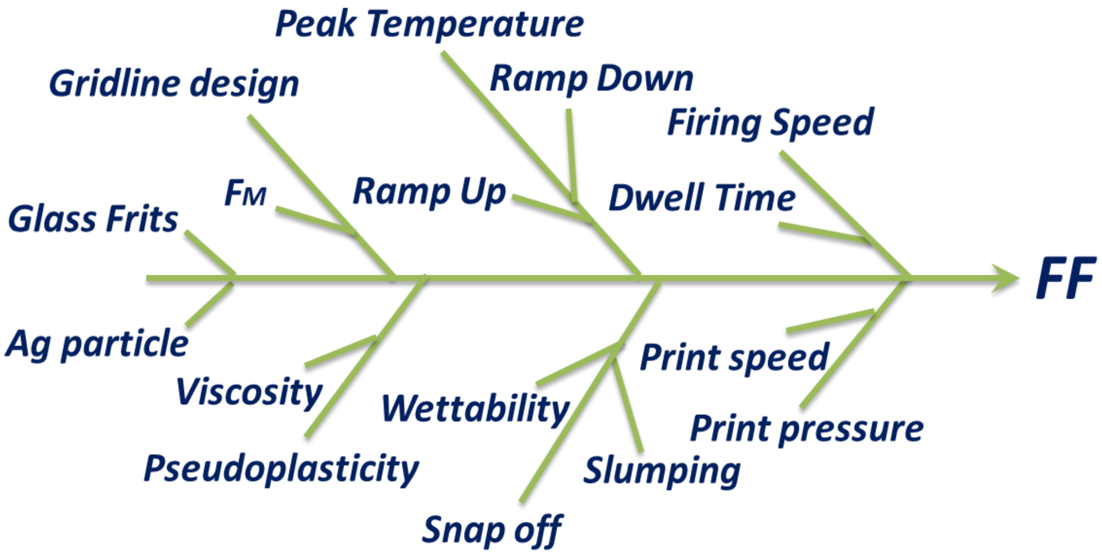


Fig. 3. 14. Effect of various design and experimental parameters on FF.

3.6.4. Optimizing BSF to achieve high V_{OC}

The BSF thickness needs to be optimized to maintain a high Voc. The relationship between firing profile temperature and BSF thickness can be expressed as,

$$W_{BSF} = \frac{t_{Al} * \rho_{Al}}{\rho_{Si}} \left(\frac{F(T)}{1 - F(T)} - \frac{F(T_o)}{1 - F(T_o)} \right) \tag{3.3}$$

Where, t_{Al} is the Al thickness, ρ_{Si} and ρ_{Al} are density of Al and Si and F(T) is the Si atomic weighted percentage of the molten phase at peak temperature and $F(T_O)$ is the Si atomic weighted percentage at the eutectic temperature. These parameters ate generally determined from Al-Si phase diagram. In the fabricated cells the Al thickness were measure 20-30 μm while alloyed at the peak temperature in the range of 750-850°C. The plotted Fig.3.15. shows that BSF thickness of 6.54-10.09 μm were maintained throughout the fabrication process.

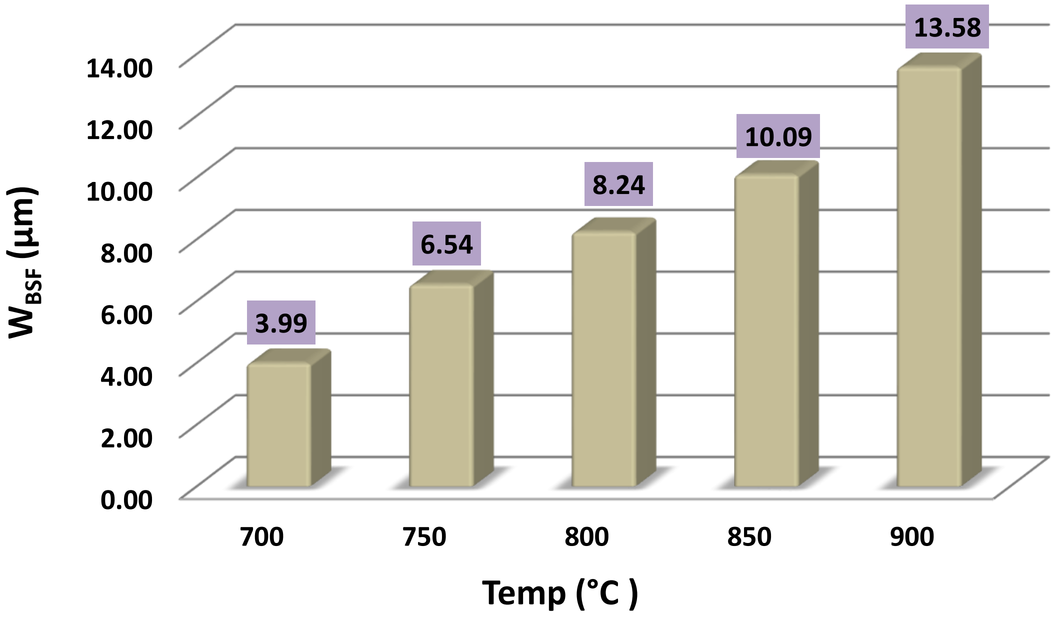


Fig. 3. 15. Modelled BSF thickness at varying peak temperatures.

3.7. The Impact of Rapid Thermal Processing (RTP) on Cell performance

From our observed data it was clear that rapid thermal processing IR belt furnace impacts the cell performance significantly. Since, contact formation results a high FF, therefore we explored into the rapid thermal processing on varying belt speed.

3.7.1. Background of Rapid Thermal Processing

Rapid thermal processing (RTP) has been deployed in the field of PY for more than two decades for (i) p-n junction formation (ii) contact anneals and (iii) forming gas anneals [32-41]. The RTP is beneficial, especially the low thermal budget because the burst of energy from the IR lamp can be used to heat only the desired region of the sample. Thus, the p-n junction formation is carried out for a much shorter time than the usual conventional furnace. The contact firing benefits from the fast ramp rates. A 30 second forming gas anneal (FGA) is as effective as the 20 minutes anneal in the conventional tube furnace [41]. RTP started with single tube, one wafer system, which showed so much promise for contact firing. In 2005, the belt furnace utilizing the infrared (IR) lamps with the fast ramps to implement the RTP concept on the production floor [42]. The thin film silicon on glass solar cell benefited from the RTP as well because of the short dwell time that resulted in effective hydrogenation of the bulk material [43, 44]. The multicrystalline solar cells benefited the most from RTP short dwell times because there is not enough time for the distribution of impurities to degrade the lifetime [45-47]. Screen-printed contacted cells became more efficient because of (i) uniform BSF formation that accompanies fast ramp up, [48] (ii) low contact resistance due to fast ramp down. Because of fast ramp down rates there is not enough time to grow oxide underneath the front grid lines, which would increase the contact resistance. Excellent hydrogenation is an added benefit of contact firing with RTP, which is observed at peak temperature -750°C for 1 second. [49-51] The short dwell time is beneficial to low quality silicon because metal impurities such as nickel and copper cannot There have been several RTP belt furnaces in the production lines for commercial solar cells. However, there has not been any commercial machine that can mimic RTP single tube furnace so that the ramp up rate is 100°C as reported by Meemongkolkiat [48] et al, which resulted in excellent open circuit voltage and high quality front contact. By mimicking the fast ramp rates of 2: 100°C, it is possible to improve the reliability of a solar cell, especially the light induced degradation (LID). The suppression of LID using RTP belt firing was first reported by Schmidt and Cuevas. [52] But their annealing time was such that the hydrogen in the

SiN will completely effuse out of the cell. Their experiment was based on evaporated contact which is not affected by redox reaction of hydrogen rather it is beneficial in removing the Schottky barrier to improve the contact resistance. However, for screen printed cells, such long time anneal in forming gas will compromise the adhesion of the gridline to silicon.

3.7.2. Cell Processing

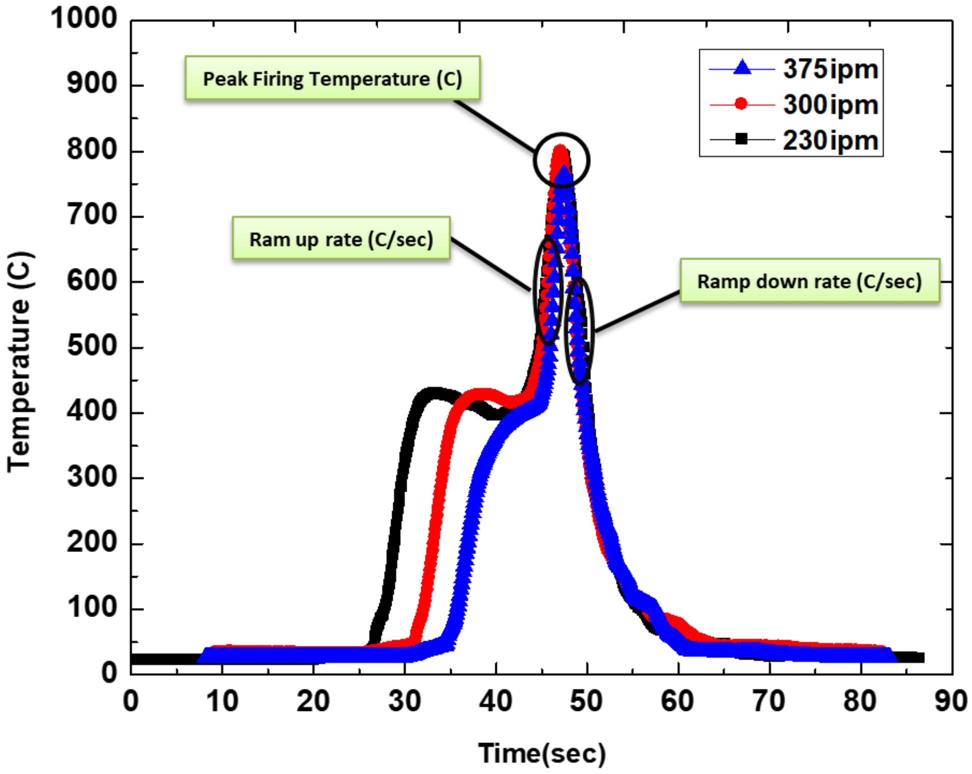


Fig. 3. 16. Firing profiles with varying belt speed obtained from IR belt furnace.

The cells were printed using 40 µm opening screens to 6 µm gridline widths, and then fired at 750-850°C peak temperature at varying belt speed of 200-400 IPM. The peak contact firing profiles with varying belt speeds are shown in Fig. 3.16. This impacted ramp up, ramp down rates, and dwell times as illustrated in Fig. 3.17., Fig 3.18. and Fig.3.19. respectively. The cells were then tested for the electrical parameters at standard test conditions.

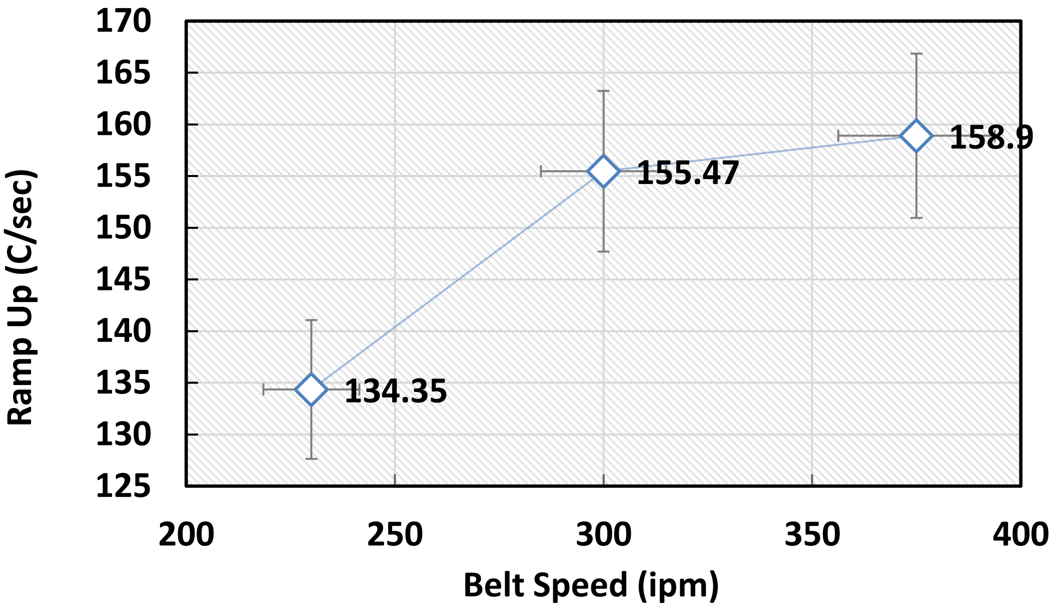


Fig. 3. 17. Ramp up rate in °C/s as a function of belt speed.

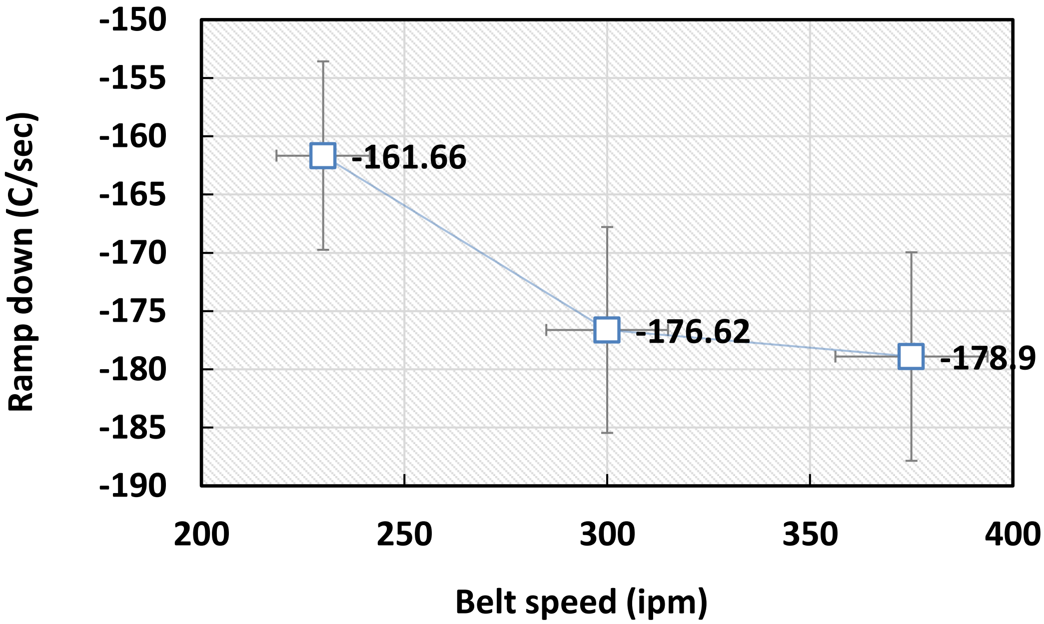


Fig. 3. 18. Ramp down rate as a function of belt speed.

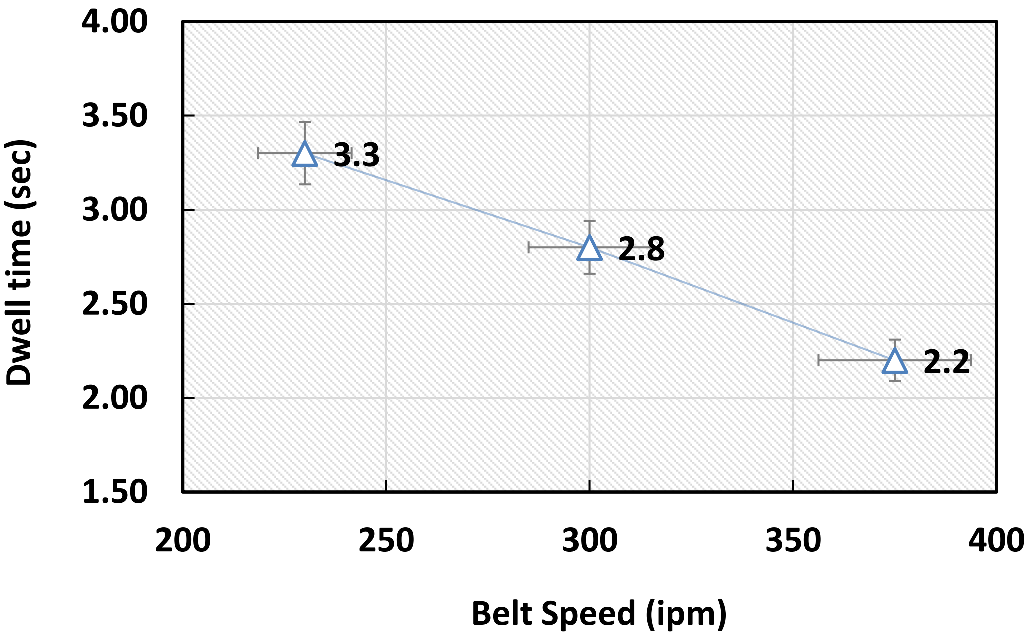


Fig. 3. 19. Dwell time as a function of belt speed.

3.7.3. Results and Discussion

The efficiency of fast belt-speed Al-BSF is plotted in Fig.3.20. The best efficiency of ~19.44% is reported at 350 ipm. As the belt speed increases ramp up, ramp down and dwell time is reduced. This effectively impacted the cell performance. The ramp up rate >100 C/sec ensured uniform BSF and thus high V_{OC}. In contrast, ramp down rate reduced the contact resistance, since oxygen did not have enough time to grow for a high belts speed. This ensured absence of void between contact and semiconductor. Thus, FF was improved for the high belt speed. Therefore, fast belt speed RTP process has the potential of increasing efficiency which can be instrumental for attaining high throughput. With the advancement of front-end fabrication throughput, improvement in the back-end metallization will allow synchronization in both front and back ends.

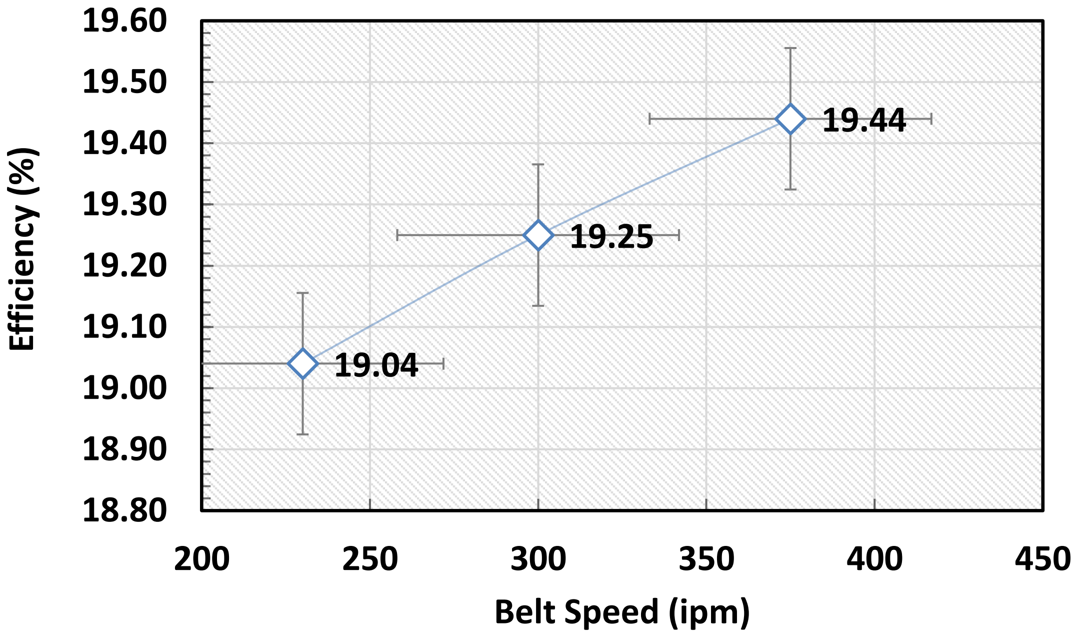


Fig. 3. 20. Efficiency of Al-BSF cells as a function of belt speed.

3.8. Roadmap to achieve >20.5% Efficiency Al-BSF Solar Cell

Fig. 3.21. shows a step by step improvement of cell performance aiming towards >20.50% Al-BSF cell. To accomplish this goal certain device modifications, need to be carried out. By utilizing a double layer SiN/SiO_2 layer, the gain in J_{SC} can improve the cell efficiency of 0.22%$_{abs}$. Secondly, the bulk lifetime and surface passivation needs to be further improved which can result an efficiency gain of 0.38%$_{abs}$. However, the most important to attain a high efficiency Al-BSF cell, the FF needs to be further improved. Our modelled result shows that with 80.5 FF finally 20.50% efficiency Al-BSF is achievable. The FF improvement can be realizable with better Ag paste combining with more precise optimization in the IR rapid thermal cofiring.

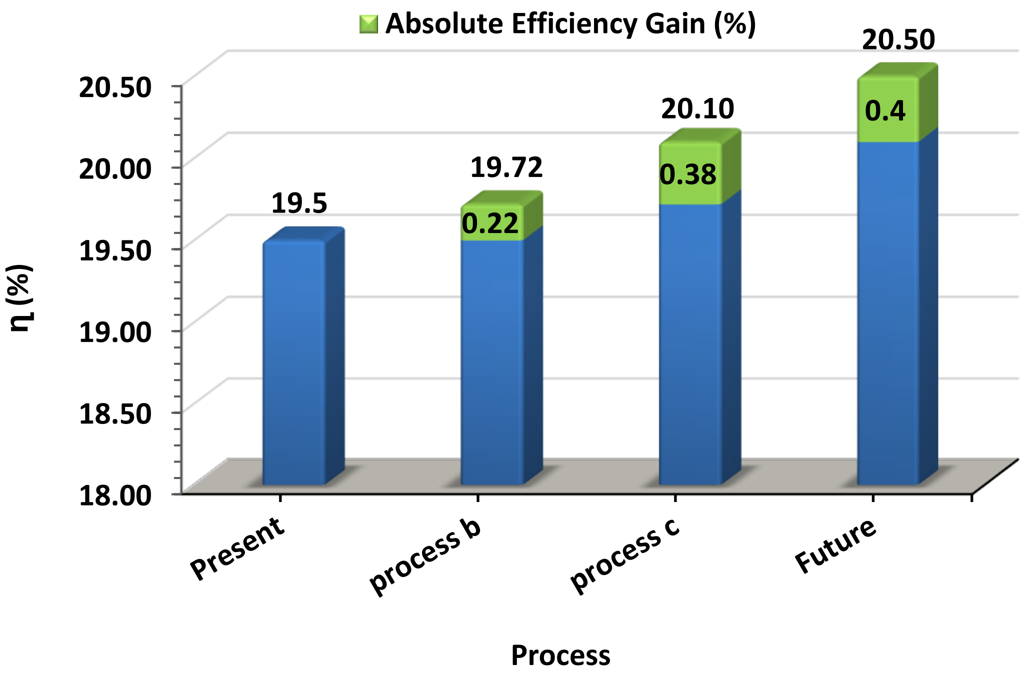


Fig. 3. 21. Step by step improvement towards >20.5% efficiency Al-BSF cell.

3.9. Summary & Conclusion

Al-BSF cell are designed and modelled in this chapter. During design, special measures were taken to introduce cost effective and simple processing sequences. One such approach is to utilize the metal contacts design that retains same performance while reduces the Ag metallization cost. This design resulted Ag consumption of ~56 mg as compared to ~80 mg in a typical cell. Subsequently, optical and electrical parameters are employed in the PC2D simulation software for each structure. The modeled results are aimed to achieve high efficiency cells compatible with industrial streamline production. The best modeled efficiencies for Al-BSF is 20.50% which is gain of ~0.2%$_{\text{absolute}}$ compared to the best reported results. Following the modeling, ~19.40% industrial size Al-BSF cell is fabricated and characterized with commercial screen-printed technique. Fabrication process was investigated in detail to unfold the aspects of efficient contact formation. The attained FF~79.50 can be further improved by optimizing IR belt furnace cofiring. Characterization results reveals that, the cell has prospect of improving performance provided with a uniform emitter. We also investigated the rapid thermal IR belt furnace firing on the cell performance. It was revealed IR belt furnace has enabled the realization of fast ramps> 100°C as obtained with the single tube RTP. This has been used to validate V_{OC} of >640 mV in this work for Al-BSF solar cell. The fast ramp up enables the uniformity of the AI-BSF formation, while fast ramp down enables the low contact resistance and hence high fill factor. Subsequently. Finally, a roadmap is given to attain >20.5% efficiency by implementing a) double layer SiN/SiO_2 dielectric material, b) improved metallization design and c) higher lifetime base material.

CHATPER 04: MODELING, FABRICATION AND CHARACTERIZATION OF N-TYPE FSF SOLAR CELL

4.1. Introduction

The conventional high efficiency p type solar cell suffers from light induced degradation (LID), which is dictated by boron-oxygen recombination centers. However, the density of the recombination is a function of substrate resistivity. Thus, the lowly doped substrate suffers the most LID [53] due to high density of defects and hence lower efficiency. Apart from LID, metal impurities such as Fe [54, 55] and physical impurities (dislocations) [56]can also impact the performance of a p-type substrate. To reduce the impact of LID and Fe metal impurities in a p-type substrate, gallium dopant was used. [57]However, the resistivity of the gallium doped silicon varies because of the very small equilibrium segregation coefficient of Ga (k_o=0.008).[58] The cost of gallium doped wafers is also a concern because of the stringent specification of limited resistivity required by cell producers.

To mitigate LID the n-type substrates, which does not have the oxygen-boron recombination centers, can readily substitute the p-type. There has been a growing research effort in the PV community to fully explore and exploit the n-type silicon. For instance, the International Technology Roadmap for Photovoltaic (ITRPV 2016)[59] has predicted that the n type wafers will dominate the market share after 2020 However, the cost of n-type substrate remains an issue because of lower production volume compared to the p-type counterpart. Also, the fabrication of an n-type cell can be expensive because of the boron diffusion to form the p-n junction (emitter). Typically, there are two major processes involved in the formation of rear junction: (a) Al-Si alloy emitter, and (b) Boron implant emitter. In case of Al-Si alloy emitter, the rear side is screen printed with full Al to facilitate the formation of emitter. This fabrication process requires only one high temperature phosphorous implant or conventional tube furnace diffusion for the FSF formation. However, for the rear junction using boron implant, two high temperature processes are required to form (i) FSF and (ii) boron implant emitter. To reduce cost of production and maintain high efficiency, the additional high temperature step can be eliminated. Thus, by using screen printed Al and emitter formation simultaneously during metal contact co-firing step is key to maintaining high yield in manufacturing.

This chapter we presented simple Al-Si alloyed formed FSF cell which can be easily fabricated with the conventional production line. Modeling is investigated in detail to understand lateral characteristics of such cell. After following the substrate independent fabrication process, the cells were characterized accordingly. Finally, A step by step improvement of such structure is modeled to attain a high efficiency FSF cell.

4.2. Literature Review

N-type cell structure, “PhosTop”, which consists front surface field (FSF), n type base and rear alloyed Al as back p-n junction was first investigated by Meier et al [60] . The premise of this structure is rooted in the utilization of rear junction coupled with high minority carrier lifetime in n-type wafer. There are two major processes involved in the formation of rear junction cell; (a) Al-Si alloy emitter on the back side, and (b) Boron implant emitter. In case of Al-Si alloy emitter, the rear side is screen printed with full Al back, which facilitates the emitter formation. This fabrication process requires only one high temperature phosphorous diffusion of the FSF before the Al print and alloy. This one high temperature was necessary for low quality silicon wafers such as the dendritic web, which the first PhosTop, 14.2% efficiency, was demonstrated.[61]

Since then there have been several reports on high efficiency n-type screen-printed silicon solar cell including Kopecek et al [62] 16% commercial size cell. Schmiga et al [63]reported 19% in 2006 and 19.3% in 2010 [64]. Meier et al in 2011 [65] reported 19.1% efficiency using implanted phosphorus for FSF and boron for the p-n junction. The key development in their work was the extension of the emitter area, which limits the Al-alloyed rear junction cell, to increase short circuit current and improve the efficiency. However, two high temperature steps are required with the implant process: one for (i) FSF and (ii) boron implant emitter.

The best reported commercial size FSF solar cell efficiency is 18.5% [66], which has emitter region bound by ~1 mm edge around the full Al back. Other recent n-type efficiencies are 19.4% [67] and 19.7% [68]. The fabrication of these cells either include selective FSF or full coverage rear emitter, which is complex and expensive to manufacture. Thus, there is a need to establish a simple and cost effective high efficiency FSF cell process.

4.3. Modeling of FSF Cell

The schematic of FSF cell is presented in Fig. 4.1. This only difference with the Al-BSF structure is the FSF instead of emitter, while emitter in the FSF cell is at the rear side, thus forming the rear junction cell. In the follwing section, we first evaluate the FSF cell performance by optimizing the emitter and base area based on the lateral current and lateral voltages. Sequentially, we drew a road map for improving the cell performance based on the emitter coverage. Finally, passivation scheme is applied to extract the further potential of a FSF cell.

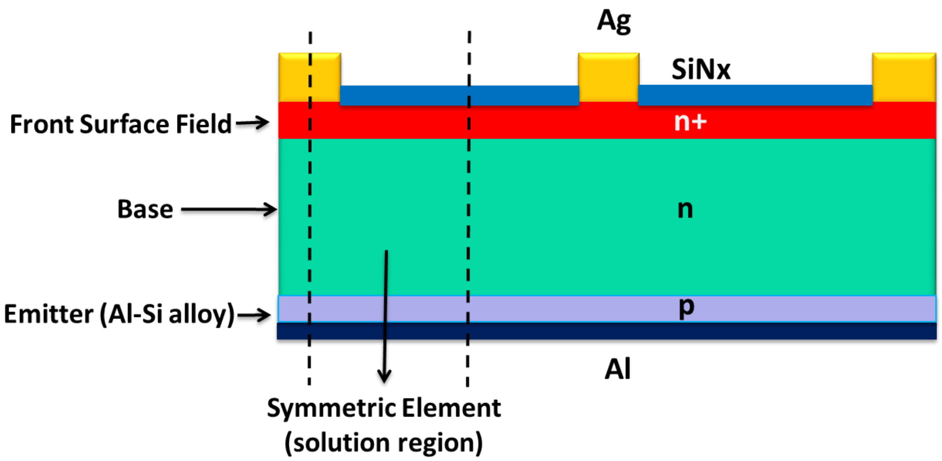


Fig. 4. 1. Device schematic of FSF solar cell.

4.3.1. Front Surface Field Design

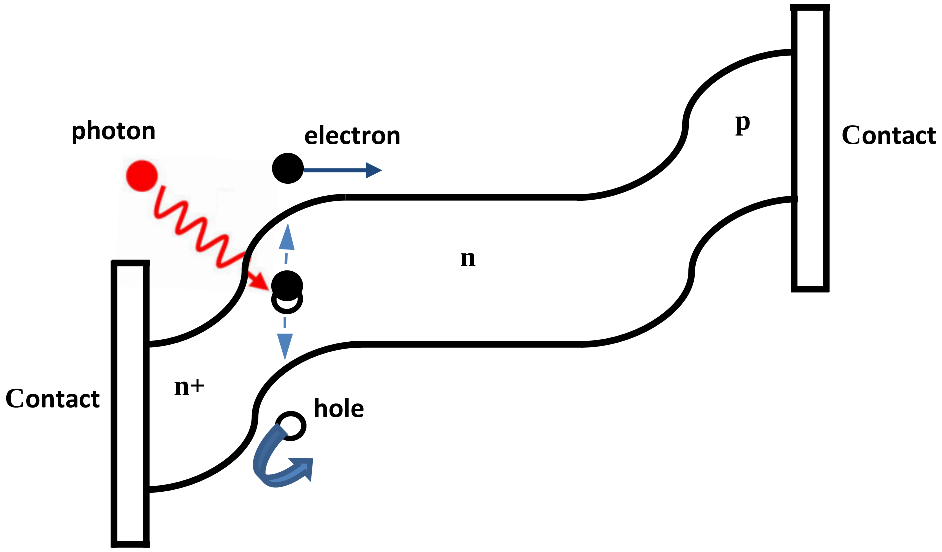


Fig. 4. 2. Energy band diagram of n+-n-p FSF solar cell (the sketch is not scaled).

As sketched in Fig. 4.2., the FSF in the n-type cell creates a high-low junction which effectively repels the minority carrier holes to recombine in the front surface. This electric field created by FSF thus improves the front surface passivation. For a high base resistivity n-type material, the FSF contributes also to uniform lateral conductivity. Thus, the lower the peak surface doping concentration the more uniform the lateral voltage drop. This is shown in Fig. 4.3. for FSF sheet resistance values of 60, 80 and 100 Ω/sq., respectively. The minute difference between 80 Ω/sq. and 100 Ω/sq. sheet resistances suggests that at-least >80 Ω/sq. FSF sheet resistance is required to attain uniform lateral voltage drop. Moreover, lower lateral voltage drops associated with high FSF sheet resistance would be beneficial towards the current trend of increasing sheet resistance in ensuring more transparent FSF.

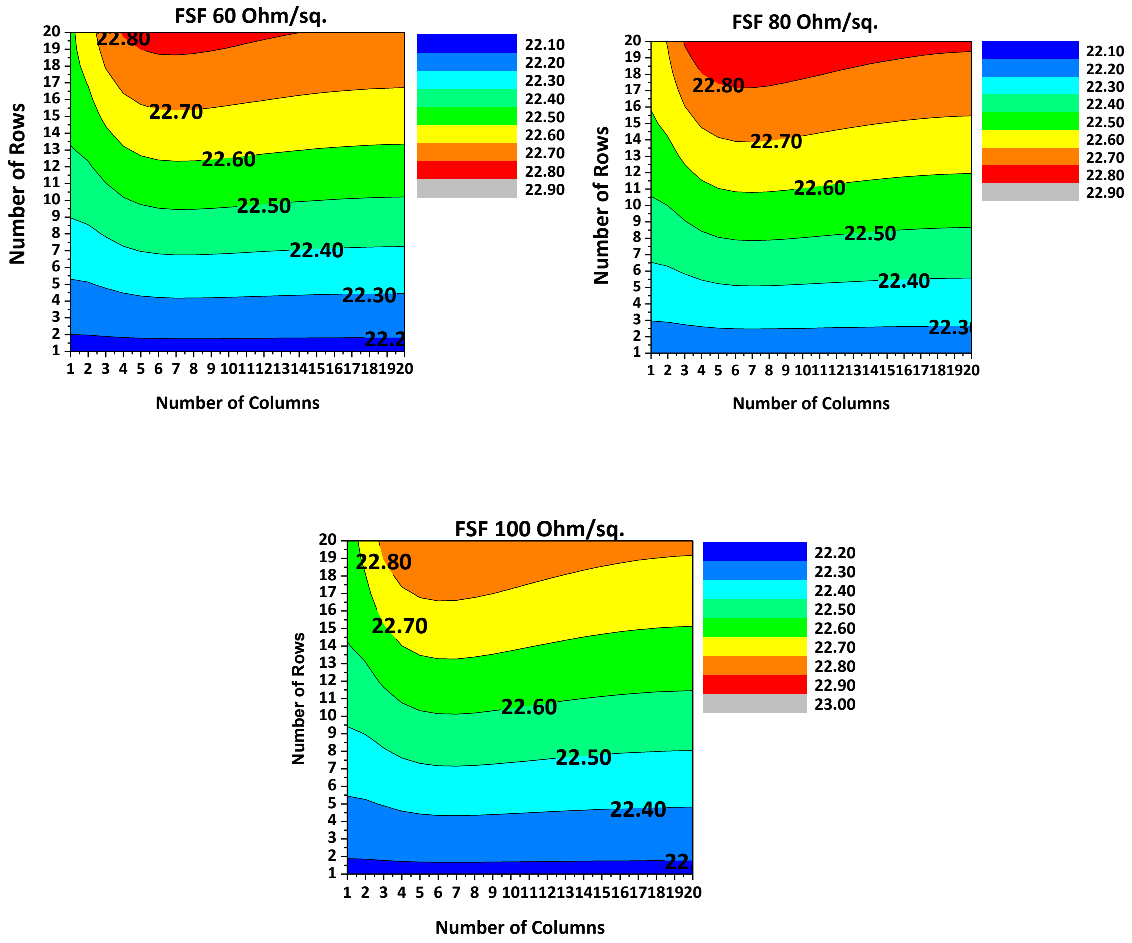


Fig. 4. 3. Contour map for hole quasi-fermi potentials for 60 Ω/sq, 80 Ω/sq. And 100 Ω/sq.

4.3.2. Base Resistivity

For the n-type wafers the base resistance significantly impacts the cell performance. PC2D is used to confirm this dependence as shown in the contour plot of Fig. 4.4.

The contour plots are generated for different base resistivity to understand the injection-level dependence of the base at the maximum power point. Unlike the p-type base, the n-type base is sensitive to lateral conductivity which impacts the overall cell performance. Three base resistivity; 1 Ω-cm and 5 Ω-cm-cm and 10 Ω-cm-cm were considered. The contour plots represent quasi fermi potentials of minority carrier holes at maximum power points. The gradient of these potentials is essentially the flow of holes in the symmetric element of the device. It can be observed from the contour plots that, as the base resistivity

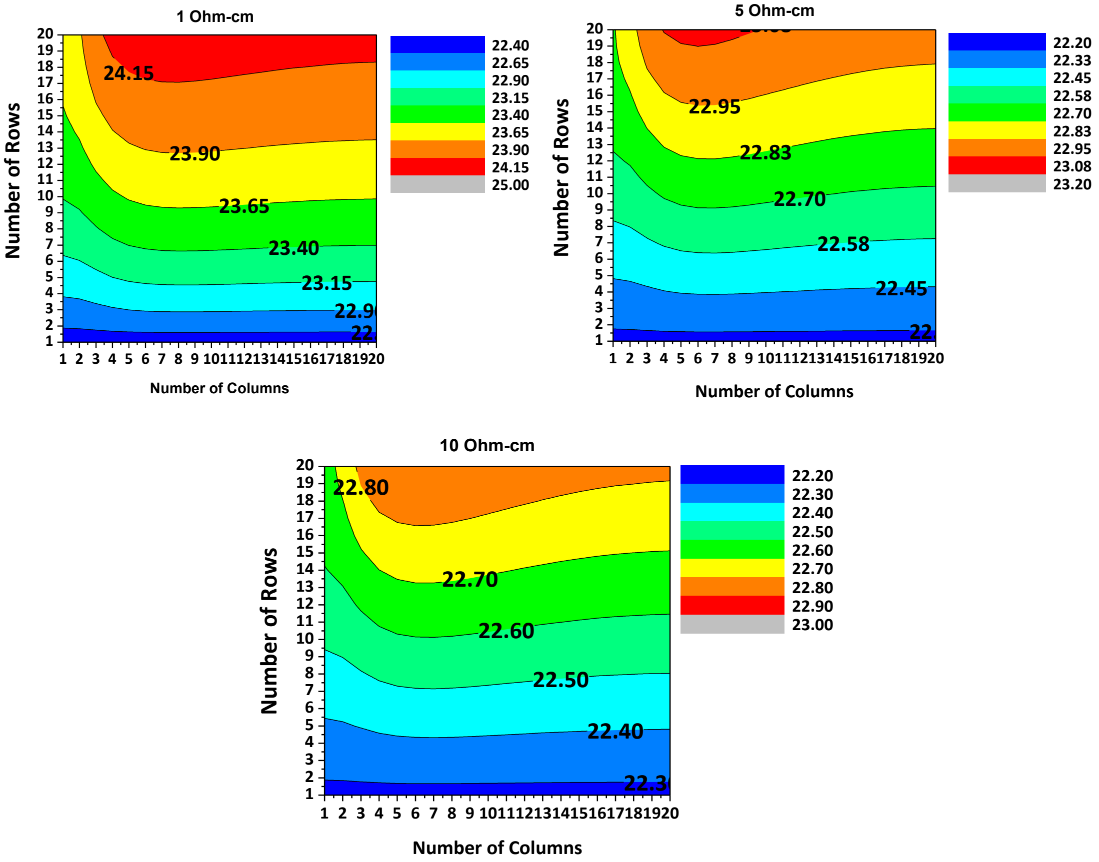


Fig. 4. 4. Contour map of hole quasi-fermi potentials for 1 Ω-cm, 5 Ω-cm and 10 Ω-cm base resistivity.

increases from 1 Ω-cm to 10 Ω-cm, the lateral fermi potentials decrease adjacent to the column 01. For instance, 50 (24.15-23.65=50) mV difference in the lateral direction is observed in the contour plot of 1 Ω-cm base on its counterpart of 25 mV (23.08-22.83=25) and 20 mV (22.80-22.60=20) at 5 Ω-cm and 10 Ω-cm base resistivity. Thus, holes flow is increases incrementally from 1 Ω-cm to 10 Ω-cm base resistivity.

4.3.3. Rear Junction collection efficiency

The Al-Si alloy at the rear surface creates the p-n junction, hence a back junction solar cell. Therefore, high quality material is needed with high minority carrier lifetime for high collection efficiency. Simulation collection efficiency of the structure is as shown in Fig. 4.5. The maximum collection efficiency of ~97% is observed at 1010 nm, which is close to the rear p-n junction. But at 350 nm, a collection efficiency of ~ 96% is exhibited. Note that the minority carrier lifetime of ~1 ms was used in the simulation.

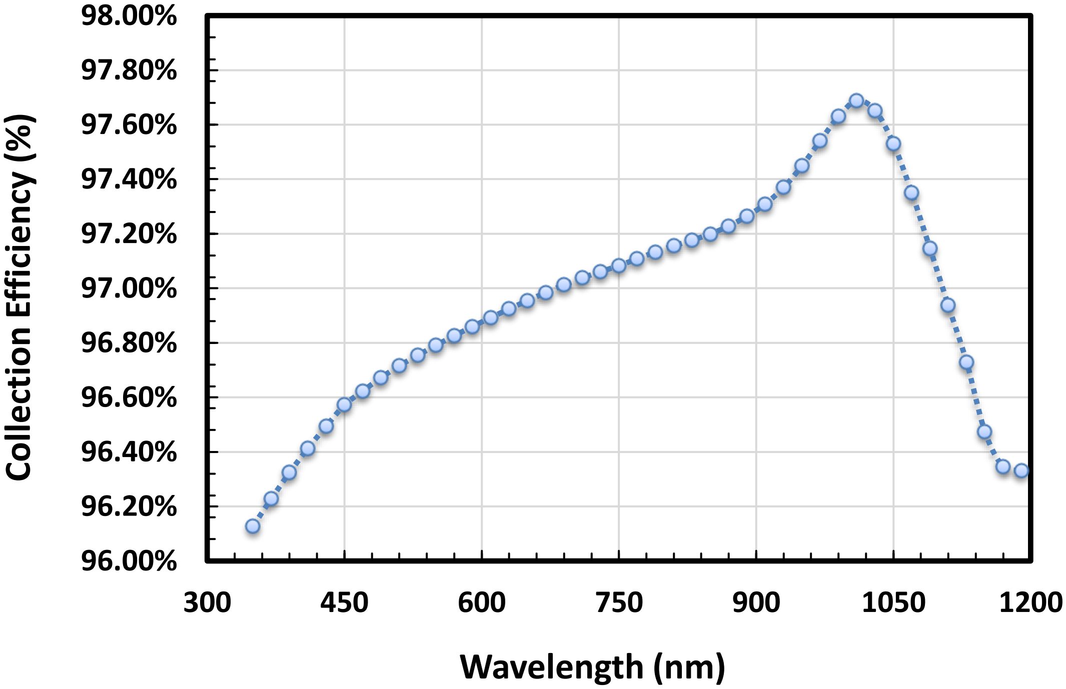


Fig. 4. 5. Collection Efficiency of n+-n-p FSF solar cell.

4.3.4. Emitter Design

The conventional rear side design of n-type FSF cell is shown Fig. 4.6. The 0.5 mm strip around the Al edge is maintained in this design. However, a gradual increase of 0.1, 0.2, 03, 0.4 and 0.5 mm Al edge is further modeled to examine the output parameters. In Table II, Al coverage along with different extension lengths are represented in different areas. For instance, Area A represent the base point with no extension and Area F represents the full emitter with 0.5 mm extension.

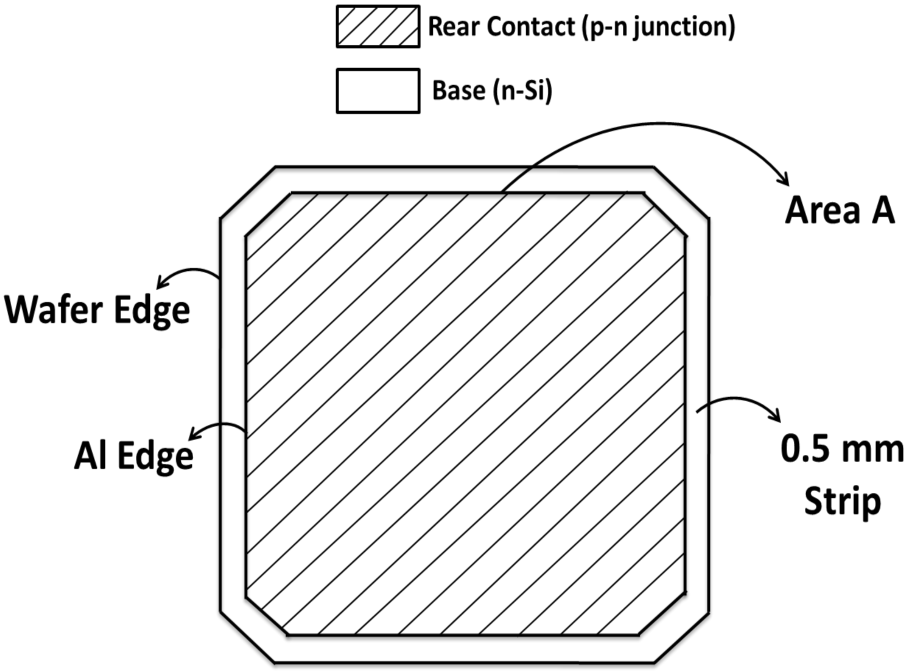


Fig. 4. 6. The rear side sketch of a conventional n-type FSF cell. The 0.5 mm strip is maintained between the Al edge and wafer edge. The Al-Si alloyed emitter and junction is thus formed underneath the Al metal coverage. In this design, there is no extension of emitter and hence it is a base position.

Table 4. 1. Name Convention of Emitter Coverages

Al Edge Extension (mm)	**Emitter Coverage**
0	Area A
0.1	Area B
0.2	Area C
0.3	Area D
0.4	Area E
0.5	Area F

4.3.5. Lateral Current

Quasi-fermi potential of minority carrier is shown in the Fig. 4.7. The contour area of quasi-fermi potential consists of 20 by 20 matrices, which represents the unit cell that is solved in the simulation design. The gradient of quasi-fermi potential represents the flow of minority carrier holes in the lateral direction. The uniform voltage distribution in the lateral direction is required for a uniform current flow, thus lower current crowding. As the emitter area coverage is from Area B to Area F, distribution of lateral voltage improved. For example, 22.60 mV contour area extends gradually along the lateral direction with more emitter coverage. Following this trend, the best lateral distribution of voltage is observed in the Area F emitter coverage.

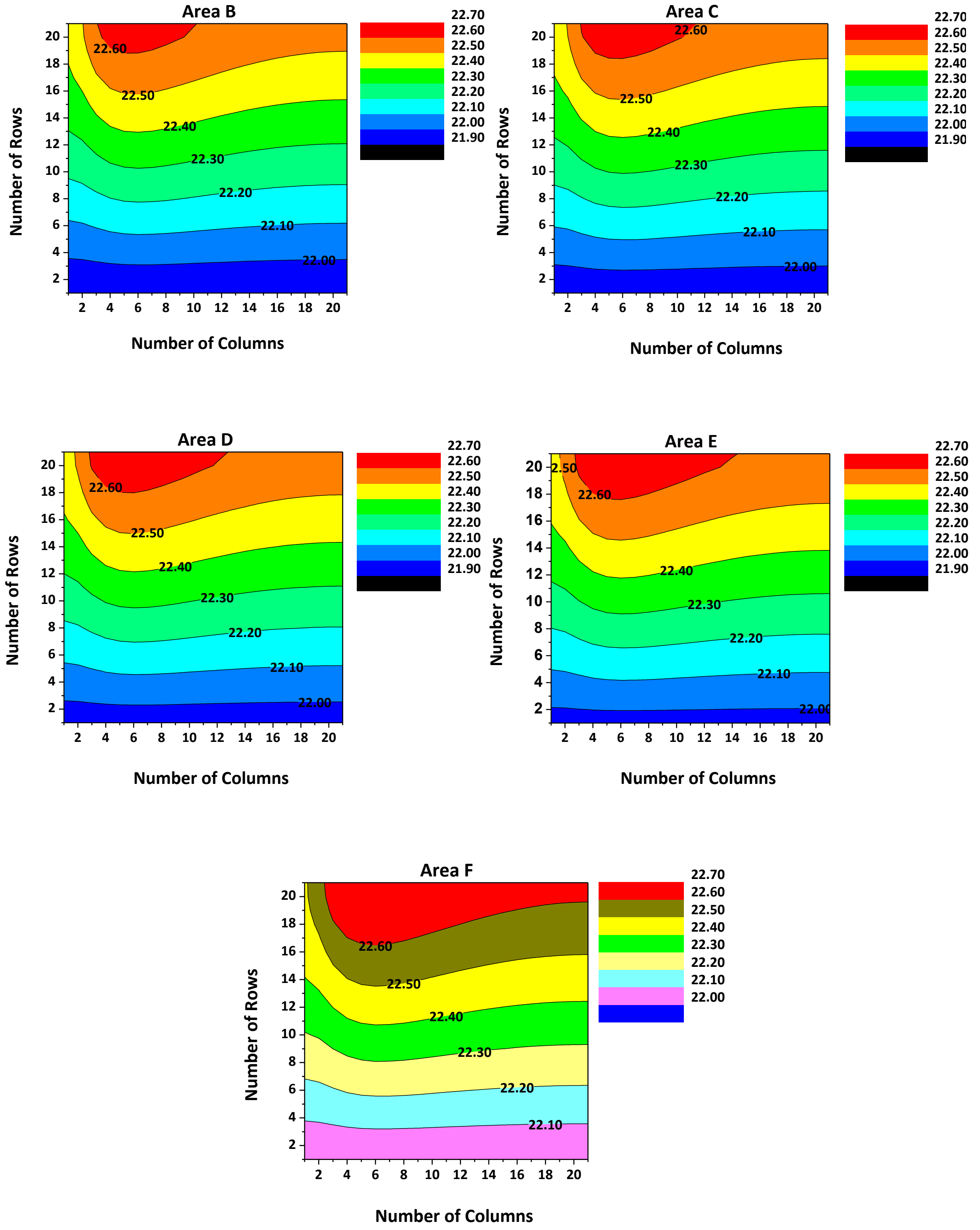


Fig. 4. 7. Contour map of quasi-fermi potentials of different emitter area coverages.

Improvement in the lateral voltage distribution is observed as the emitter coverage is extended gradually. This can be translated as lower current crowding advantage in the full extended emitter.

4.3.6. Front Surface Passivation

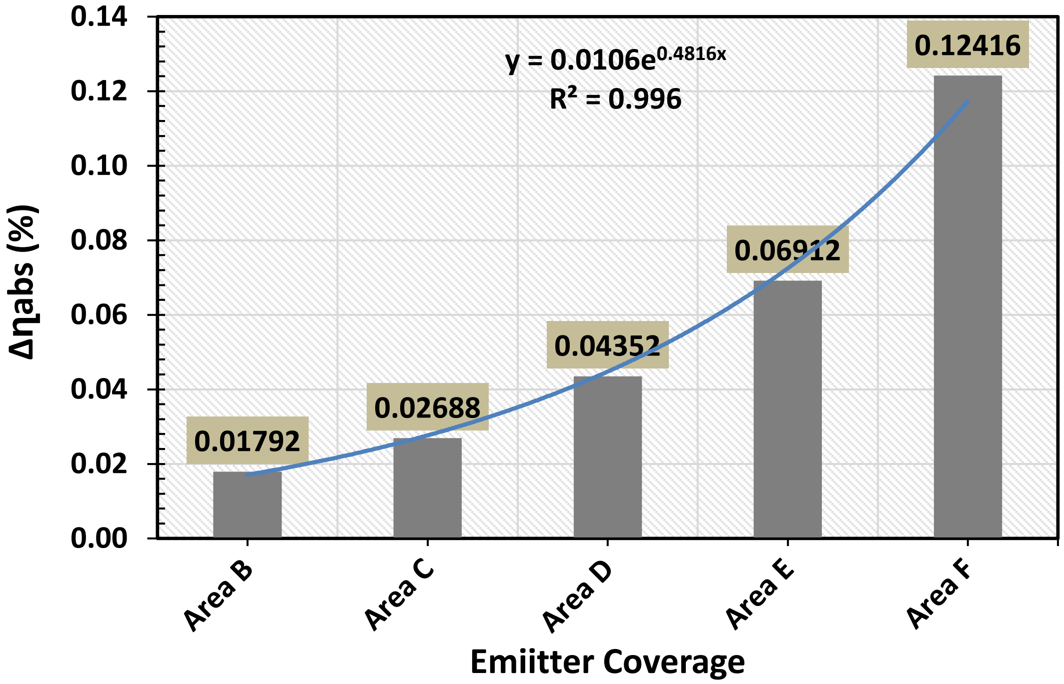


Fig. 4. 8. Modeled absolute efficiency gains when surface passivation is improved from 50000 cm/s to 100 cm/s in extended emitter approach. The 0.12%absolute efficiency gain is observed in the full emitter.[69]

The front surface passivation is an important degree of merit in the n-type FSF solar cell performance. Fig. 4.8. shows the absolute efficiency gain by improving the surface passivation from 50,000 cm/s to 100 cm/s. The 50,000 cm/s surface recombination velocity is utilized as a baseline for this simulation model. This data is extracted from the experimental result of internal quantum efficiency. It is clear from the figure that with full emitter, an absolute efficiency gain of ~0.12% is achievable. Thereby, highly passivated surface with full emitter can lead to the full potential of FSF cell.

4.4. Results and Discussion

The best simulated efficiency is ~18.64%. However, by varying emitter coverage and surface there is scope to further improve the efficiency. The electrical output parameters with varying emitter coverage is shown in Fig. 4.9. By increasing coverage, a gain in J_{SC}, V_{OC}, FF and the total efficiency, η is realized. An absolute ~1.4% J_{SC} gain is observed with a full emitter compared to the base. This is mainly due to the increased carrier collection with the extension of Al edge in the rear side. The V_{OC} is improved by ~3 mV since extended emitter causes better rear surface passivation. It is interesting to note that FF increases to 1.3 %absolute in the modeled results. This can be attributed to better lateral current flow as shown in the contour maps in Fig. 4.7. An improved lateral current can result in a lower current crowding and hence a lower series resistance. Thus, a combination of improved collection, passivation and lateral current contributed to the total efficiency gain of $0.33\%_{absolute}$.

Table 4. 2. Simulation Output Parameters of FSF cell.

Sample	**Metallization Design**	V_{OC} **(mV)**	J_{SC} **(mA/cm^2)**	**FF (%)**	η **(%)**
Simulated Cell	4s-5BB	638	36.3	79.1	18.64

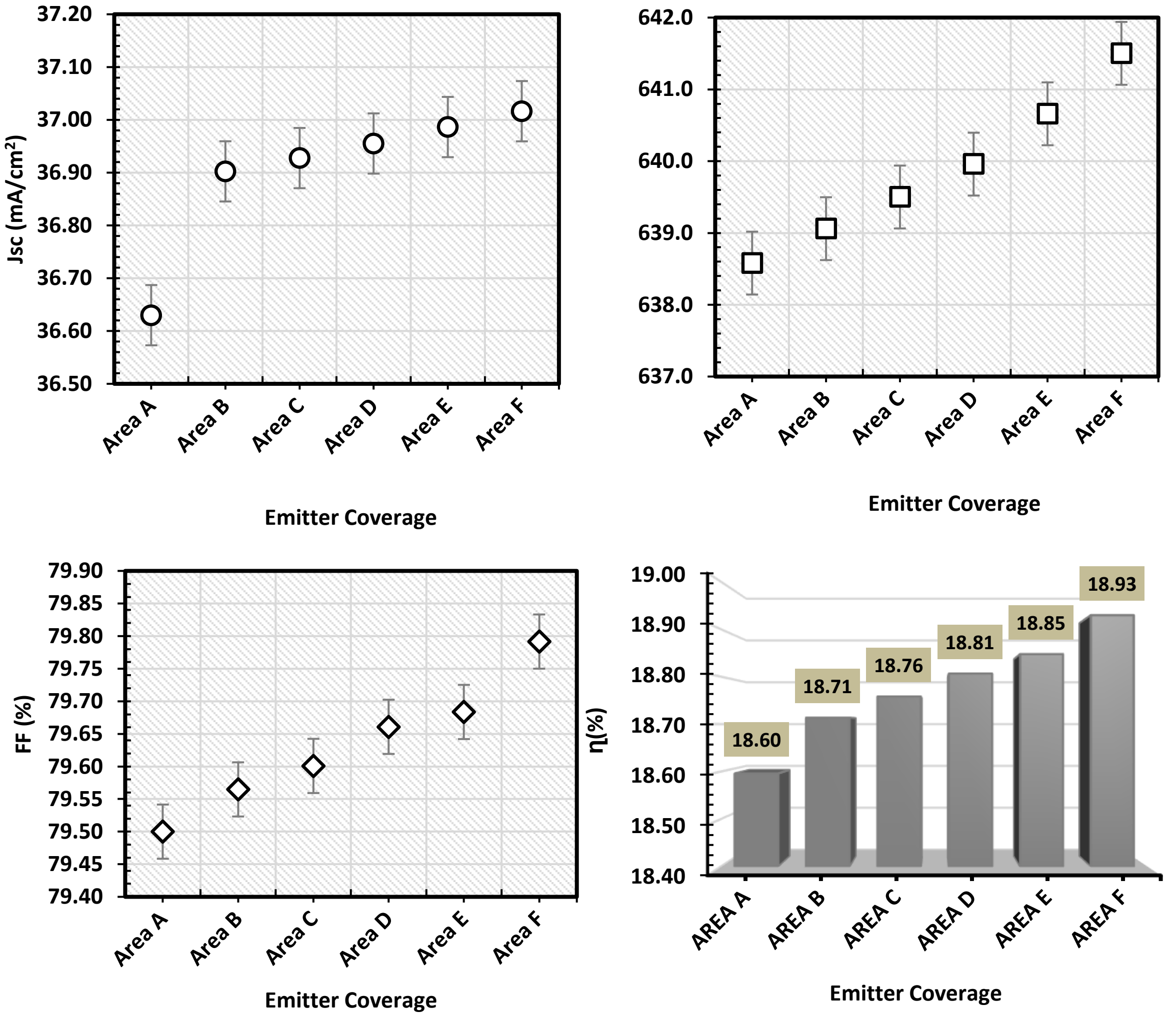


Fig. 4. 9. Electrical output parameters with varying emitter area coverage. With full emitter, a ~0.33%absolute efficiency gain is observed from the modeled simulation.

4.5. Fabrication Process of FSF Cell

Cells were fabricated using the commercial process flow given in Fig. 4.10. A 10 Ω-cm base resistivity Czochralasky (CZ) n-type wafers were used with FSF sheet resistance of 80 Ω/sq. The wafers had 180 μm thickness and 239 cm^2 surface area. Same processing sequences are utilized as used in the fabrication of Al-BSF structure. The only difference is the starting wafer is n-type wafer. At UNC Charlotte Photovoltaic Research Laboratory (UNCC PVRL) we performed a) back and front screen-printing, b) drying and c) belt furnace co-firing steps. Since, same front Ag paste and rear Al paste were utilized for this purpose as used in Al-BSF structure, we maintained uniform process parameters during screen-printing and IR belt furnace cofiring. Thus, no further optimization was required to the existing fabrication line.

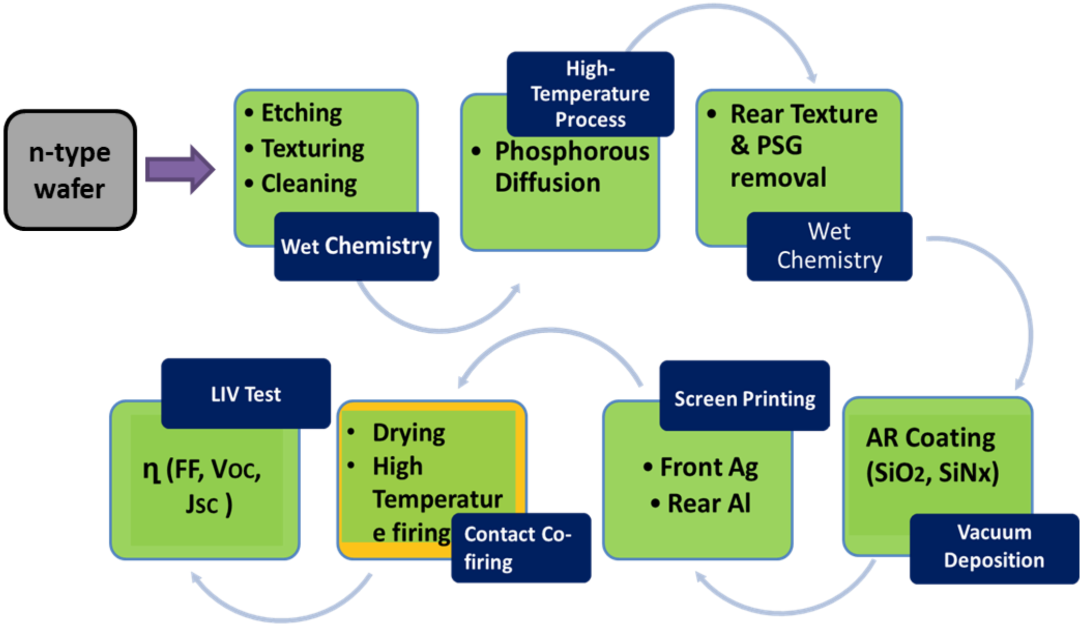


Fig. 4. 10. Commercial solar cell processing sequence for FSF cell.

4.6. Characterization of FSF cell

4.6.1. Light I-V measurement

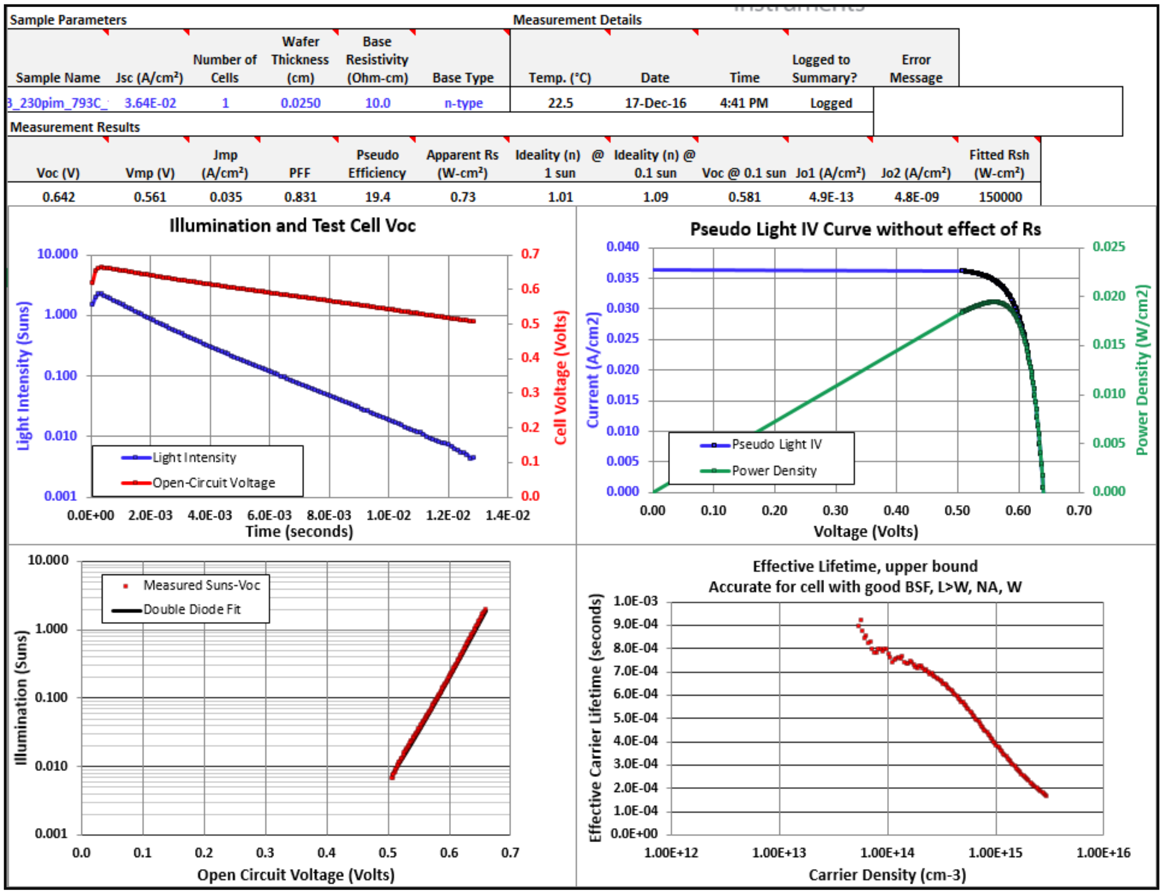
Table 4.3 summarizes the electrical output parameters of the fabricated FSF cell. The best efficiency of ~18.4% was measured with the average efficiency of 18.1%. The best FF of 79.3% compared to average of 78.5% was obtained. The somewhat low FF is due to poor printing as was discovered after contact co-firing. The relatively low JSC value of ~36.1 mA/cm^2 can be attributed to the non-optimized peak front doping concentration and ARC thickness and refractive index. The smaller emitter area than the wafer size due to 0.5 mm edge requirement around the back side to avoid shunting causes low J_{SC}. However, if the Al-Si alloy emitter is extended close to the wafer edge as demonstrated by use of implant boron [68] the J_{SC} will increase. The V_{OC} of only ~638 mV was measured, which is ~2-7 mV lower than the p-type Al BSF counterpart [70].

Table 4. 3. Electrical Output Parameters OF FSF cells measured under Standard Test Conditions (AM 1.5G, 100mw/cm2, 25 C)

Cell ID	**V_{OC} (mV)**	**J_{SC} (mA/cm^2)**	**FF (%)**	**η (%)**
Best	638	36.4	79.3	18.42
Average (10 cells)	638	36.2	78.5	18.13

4.6.2. Suns-V_{OC} measurement

The Suns-V_{OC} measurement was carried to assess the wafer quality and shunting. There is no shunting effect is observed since implied V_{OC} and R_{Shunt} was high enough from Fig. 4.11. Moreover, this was verified by J_{O1} and J_{O2} values of 4.9e-13 A/cm^2 and 4.8e-13 A/cm^2 respectively. The ideality factor at 0.1 sun~1.09 was relatively high compared to the light IV n~1.04. This indicates that cells might had overfired which resulted a reduced 18.4% efficiency. The pseudo FF of 83.1% and pseudo efficiency of 19.4% indicates that cells has further potential to improve the cell performance by optimization in tailoring contact and gridline resistance during IR contact co-firing. Finally, the effective lifetime was observed which is ~800 μs. The bulk lifetime of this wafer was measured 1000 μs. The loss in lifetime might be due to the passivation in the base area since, IQE in the base area was not very promising.



Sample Parameters

Sample Name	Jsc (A/cm²)	Number of Cells	Wafer Thickness (cm)	Base Resistivity (Ohm-cm)	Base Type
3_230pim_793C_	3.64E-02	1	0.0250	10.0	n-type

Measurement Details

Temp. (°C)	Date	Time	Logged to Summary?	Error Message
22.5	17-Dec-16	4:41 PM	Logged	

Measurement Results

Voc (V)	Vmp (V)	Jmp (A/cm²)	PFF	Pseudo Efficiency	Apparent Rs (W-cm²)	Ideality (n) @ 1 sun	Ideality (n) @ 0.1 sun	Voc @ 0.1 sun	Jo1 (A/cm²)	Jo2 (A/cm²)	Fitted Rsh (W-cm²)
0.642	0.561	0.035	0.831	19.4	0.73	1.01	1.09	0.581	4.9E-13	4.8E-09	150000

Fig. 4. 11. Suns-VOC measurement for FSF cell.

4.6.3. Series Resistance Breakdown

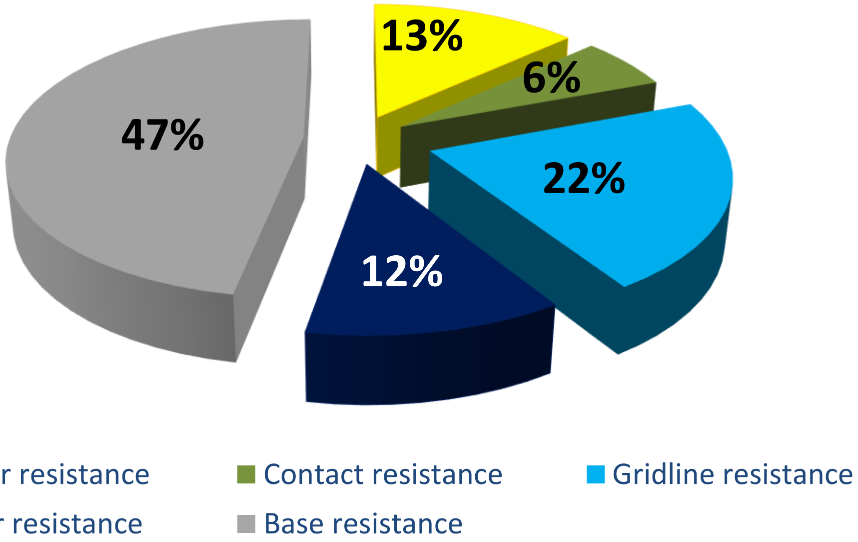


Fig. 4. 12. Series resistance components of FSF Cells.

The series resistance pie chart is presented in Fig. 4.12. As anticipated the most contributing factor towards the series resistance is the base resistance. In the n-type cell the base resistance is chosen high compared to the p-type cells to account the high-level injection. Second, contributor factor was gridline resistance, which is an indication that gridline was not continuous and therefore a better printing can further reduce the gridline resistance and thus cell performance can be improved. The emitter and busbar resistance was expected to be same as it is observed for choosing this particular emitter and front Ag busbars. Although contact resistance was low, however from the Suns-V_{OC} data reveals that there is still room to reduce contact resistance via co-firing optimization.

4.6.4. Quantum Efficiency

The IQE and reflectance graph for the best cell is shown in Fig.4.13. The blue wavelength response was relatively low than what is anticipated. This is might be due to thenonoptimized ARC layer. The reflectance data from the ARC layer verified that reflectance was high at the front surface which caused a reduction in IQE. Moreover, the response at the base was low which is due to bulk recombination. This might be caused by the low minority carrier lifetime. Although, 1000 μs lifetime is much higher compared to the p type material lifetime however, since the junction is located in FSF cell, a higher lifetime n-type material is required to overcome the recombination at base. Finally. the high wavelength response was high which is an indication rear reflectance from full Al-Si alloy.

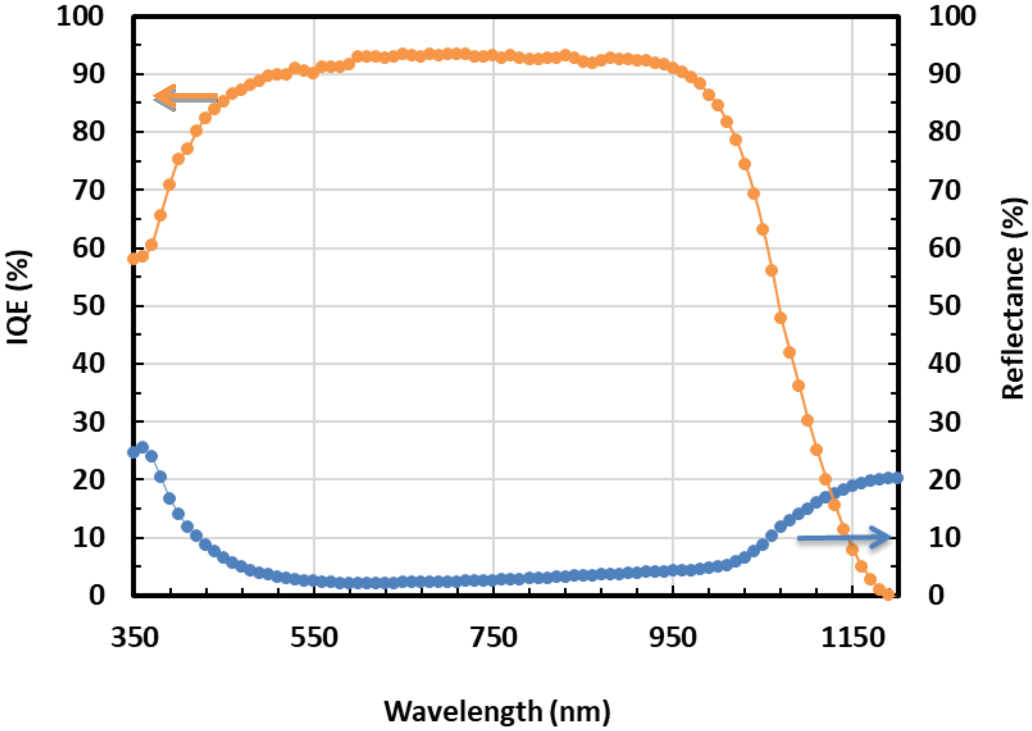


Fig. 4. 13. Internal quantum efficiency (IQE) – orange, and reflectance – blue, for the best FSF cell.

4.7. Towards ~22% Efficiency FSF Solar Cell

Table 4.4. and Fig. 4.14. shows a step by step improvements that can be carried out to realize up to ~22% efficiency. By reducing the wafer thickness to 140 µm and 5 ms minority carrier lifetime, efficiency gain of 0.22%$_{\text{absolute}}$ can be realized. Next, by decreasing the front surface recombination velocity (FSRV) to ~100 cm/s, another 0.57%$_{\text{absolute}}$ efficiency is obtained. Another 0.04%$_{\text{absoulte}}$ efficiency can be attained if FSRV is further reduced to 10 cm/s. A whopping 1.56%absolute efficiency is recorded by introducing the rear passivation and implement an n-PERT structure. Finally, a bifacial or Bi-PERT structure can give additional 0.32%$_{\text{absolute}}$ efficiency and leading to ~22% target.

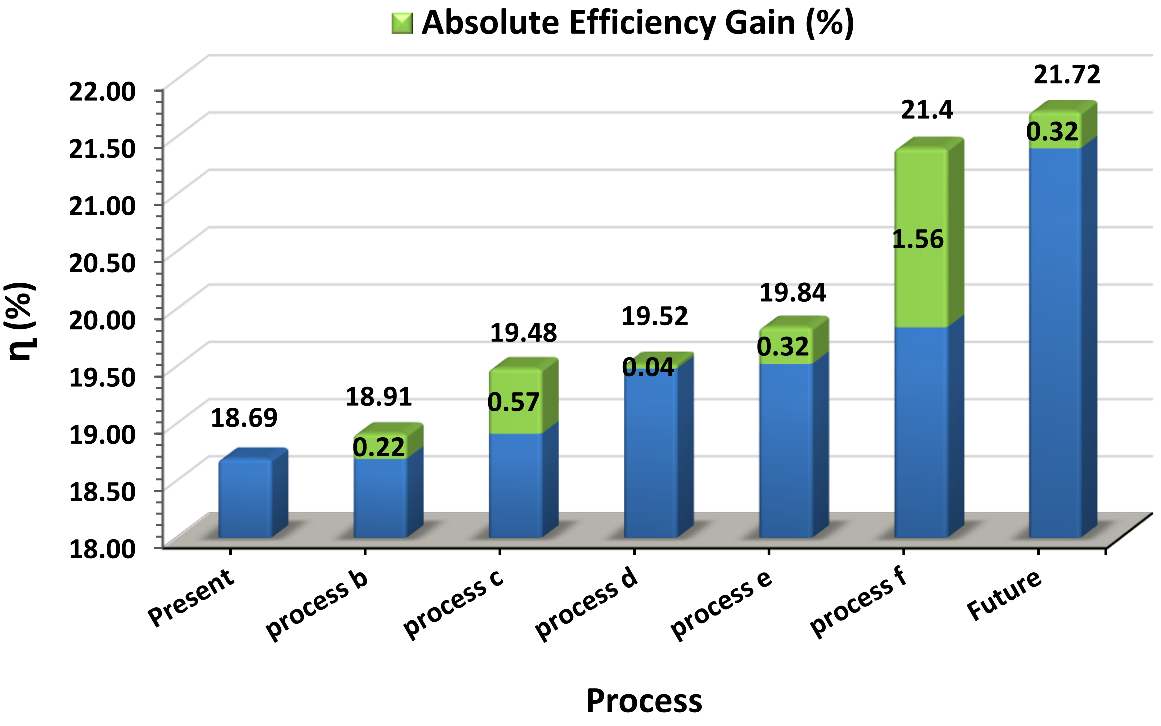


Fig. 4. 14. Efficiency Gain Model of FSF Cell.

Table 4. 4. Development of FSF Cell Performance

Process	**Cell Structure**	**Development**
Present	FSF	Best Experimental Cell with improved Front ARC layer
Process b	FSF	Optimized Base thickness (140 µm) + increasing bulk lifetime (5ms)
Process c	FSF	Increasing front surface passivation to 100 cm/s
Process d	FSF	Increasing front surface passivation to 10 cm/s
Process e	FSF	Adopting extended emitter approach
Process f	n-PERT	Introducing rear passivation
Future	Bi-PERT	Converting the cell to the bifacial

4.8. Summary & Conclusion

An industrial size n-type FSF solar cell was modeled, fabricated and characterized in this chapter. In modeling lateral characteristics are investigated in detail in adopting the rear emitter design. The best efficiency of ~18.4% is fabricated in this work. J_{SC} of 36.4 mA/cm^2 was realized for the best cell due to use of non-optimum FSF peak surface concentration and less emitter due to 0.5 mm back edge requirement for the Al screen. V_{OC} of 638 mV represents that there is recombination in the base area. Hence, a higher lifetime wafer is recommended to improve the V_{OC}. Since, same production line is applied as followed in the fabrication process of Al-BSF cell, no additional steps are required in manufacturing line. The result indicates that if the emitter is extended to cover most of the back side, in addition to other improvements outline in the work, the FSF cells efficiency of ~22% is achievable.

CHATPER 05: MODELING, FABRICATION AND CHARACTERIZATION OF INDUSTRIAL BIFACIAL SOLAR CELL

5.1. Introduction

After exploring p-type and n-type cells, we further delved into the bifacial cells aiming to exploit additional output power rooted from the current generation in rear illumination. Bifacial cells have numerous advantages in contrast to the conventional monofacial structures. a) Increased output power from both front and rear illumination, b) avoiding bowing effect from the full rear Al, and c) lower heat consumption due to the absence of Al and d) simple interconnections from wafer to wafer in the module fabrication are the primary reasons of recent growth in the bifacial cells. Concurrently, development of boron diffusion in order to form p^+ BSF is also an influential factor for choosing such structure. This chapter discusses fabrication and characterization of screen printed bifacial cells. Performance from both front and rear illumination was evaluated individually to ascertain the bifacial characteristics of the cell. Subsequently, a detail loss analysis was conducted to pinpoint the future prospect of such cell.

5.2. Energy Band Diagram of Bifacial Cell

Fig.5.1. shows the energy band diagram of Bifacial cell on p-type wafer. The front side of the bifacial cell consists of emitter and the rear side is boron doped p+ layer which is active creates the BSF. The electrons at the rear side is repealed by the rear BSF due to the formation of high low junction. This results an improved passivation and high V_{OC}. Unlike the monofacial cells, photon is incident on both sides and contributes towards higher output power.

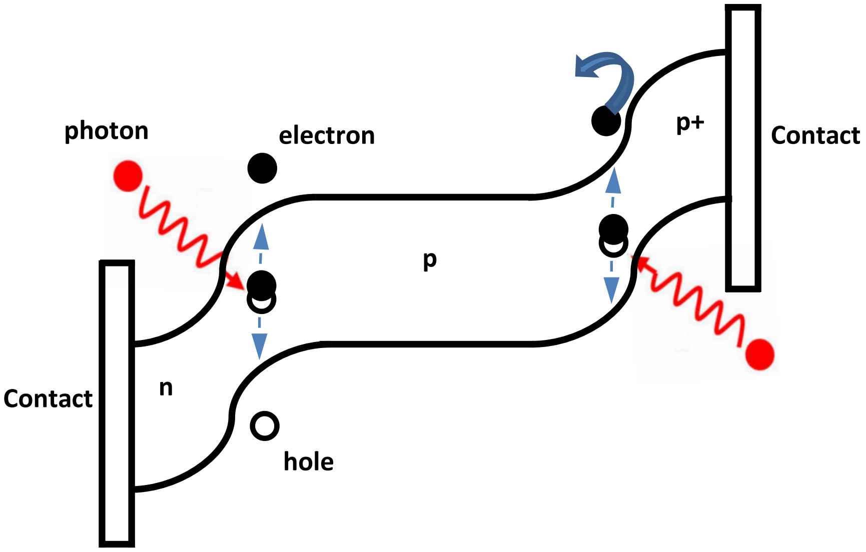


Fig. 5. 1. Energy band diagram of bifacial solar cell.

5.3. Literature Review

The first bifacial solar cell was proposed by Mori et al. in 1960 with a conversion efficiency of ~7%. [71] Since then different research groups and institutions have investigated how to increase its performance for commercialization [10, 72-86]. Mostly earlier efforts were based on the small area cells. The first commercial size bifacial solar cell with screen printed contacts was reported in 2010 with efficiency of 16% by Yang et al. [87]. However, because of the fast pace in developing the Al-BSF cell to higher efficiency, this was not materialized.

Recently PERC (passivated emitter rear cell -BiPERC) [88] and PERL (passivated emitter rear localized -BiPERT) [89] concepts have been built into the bifacial structure as reported in references to improve bifacial performance. Other such new structures are BICORE [90] and BiSON [91]. Recently, best industrial cell efficiencies for BiPERC [92] and BiPERT [93] are 21.3% and 22.3%, respectively. Despite the recent progress, the industrial growth of bifacial structure is relatively slow due to the complexity in the processing steps. Therefore, there is need to simplify the processing sequence for cost effectiveness. Thus, the use of high throughput screen printed technique needs to be implemented for contact metallization.

5.4. Modelling of Bifacial Solar Cell

For a bifacial design, first columns in both sides represent the contact area as illustrated in Fig. 5.2. The rest of the area at the front and rear surfaces are passivated areas. The 20th column is essentially the midpoint between two adjacent gridlines. Modelling further extended towards optimization of gridlines, cost calculation, recombination currents mapping and understanding the effect of rear illumination. The detail analysis is conducted in order to find cost-effective and high efficiency bifacial cell.

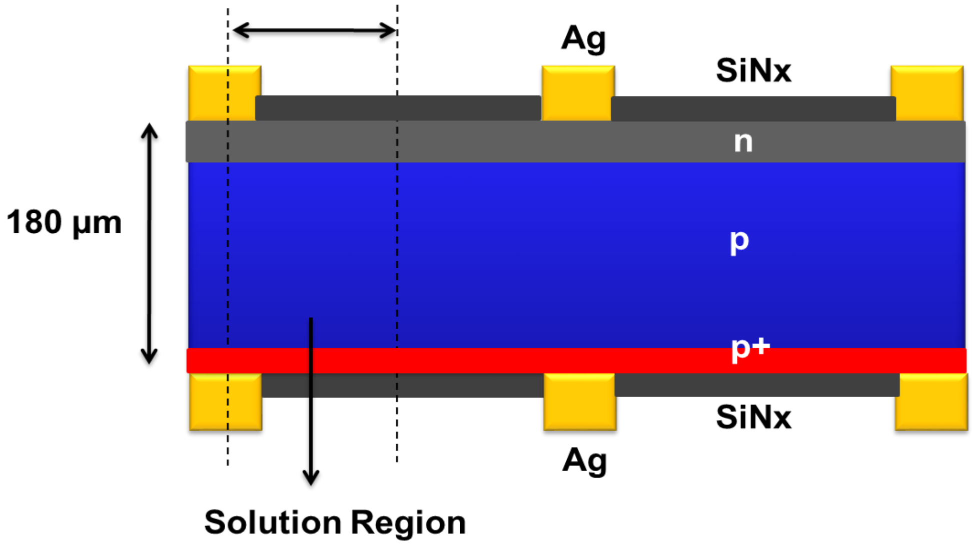


Fig. 5. 2. Schematic of modeling design in PC2D.

5.4.1. Input Parameters

Table 5. 1. Input Parameters of Bifacial Cell

Parameter	Value	Source
Minority Carrier Bulk Lifetime	100 µs	Experimental Data
Wafer resistivity	1.5 Ω-cm	Experimental Data
Sheet Resistance	Varied 80-100 Ω/sq.	Standard Doping profile
Emitter depth	0.35-0.48 µm	Standard Doping Profile
BSF sheet Resistance	Varied 80-100 Ω/sq.	Fabrication Standard
BSF depth	10 µm	Fabrication Standard
Gridline Width (front and rear)	55 µm	Screen printed Fabrication Standard
Busbar Width	0.9 mm major, 0.45 mm minor	Uneven Busbar Design
FSF Passivation	100-50000 cm/s	Standard passivation Standard
Metallization Factor (F_M)	3%-5%	Analytical Calculation

5.4.2. Results & Discussion

The results for the two gridline configurations: (i) non-segmented or continuous and (ii) The three gridline widths, 30µm, 40µm and 50 µm are fixed, while the impact of the number of gridlines on efficiency, FF, J_{SC}, V_{OC} are investigated.

5.3.2.1. Continuous or non-segmented gridlines

Fig.5.3. shows the efficiency as a function of the three gridline widths (30, 40 and 50 microns). For the 30µm gridline width, the efficiency ranges from 21.45% (lowest) to >21.8% as the number of gridline increases to 120. At 78 gridlines, the emitter, contact and gridline resistances dominate the total series resistance, and the FF (Fig. 3.18.c) decreases.

The 40 µm gridline width on the other hand started at ~21.6% efficiency, which is highest for the three widths, but ended in between 30µm and 50 µm as the number of gridline increases to 120. However, at 89 gridlines, the efficiency exhibited by the two gridline widths, 30 and 40 µm are similar ~ 21.7%. Thus, the slight advantage of ~0.1% efficiency at 120 gridlines may not be commensurate with the additional cost of metallization.

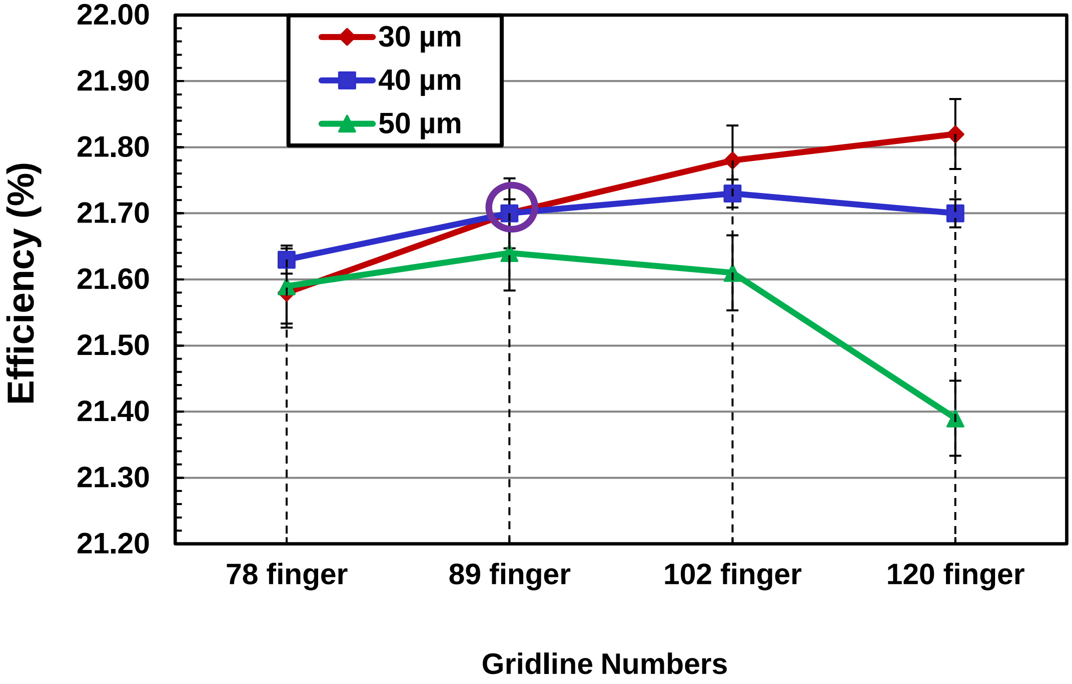


Fig. 5. 3. Efficiency as a function of the number and widths of gridlines.

Fig. 5.4(a) shows the variation of J_{SC} as the number of front gridlines with fixed widths at 30 µm, 40µm, and 50µm. This clearly shows that larger number and wider gridlines, increase the metal shadowing and decrease the number of photon absorption from the sun radiation. Thus, leading to lower J_{SC}.

From Fig. 5.4 (b), the impact of the three widths and number of busbars on the V_{OC}, the same trend as in J_{SC} is observed. This can be attributed to the metallization factor, F_m, which determines the metal-Si recombination current that influences the Voc. The area weighted

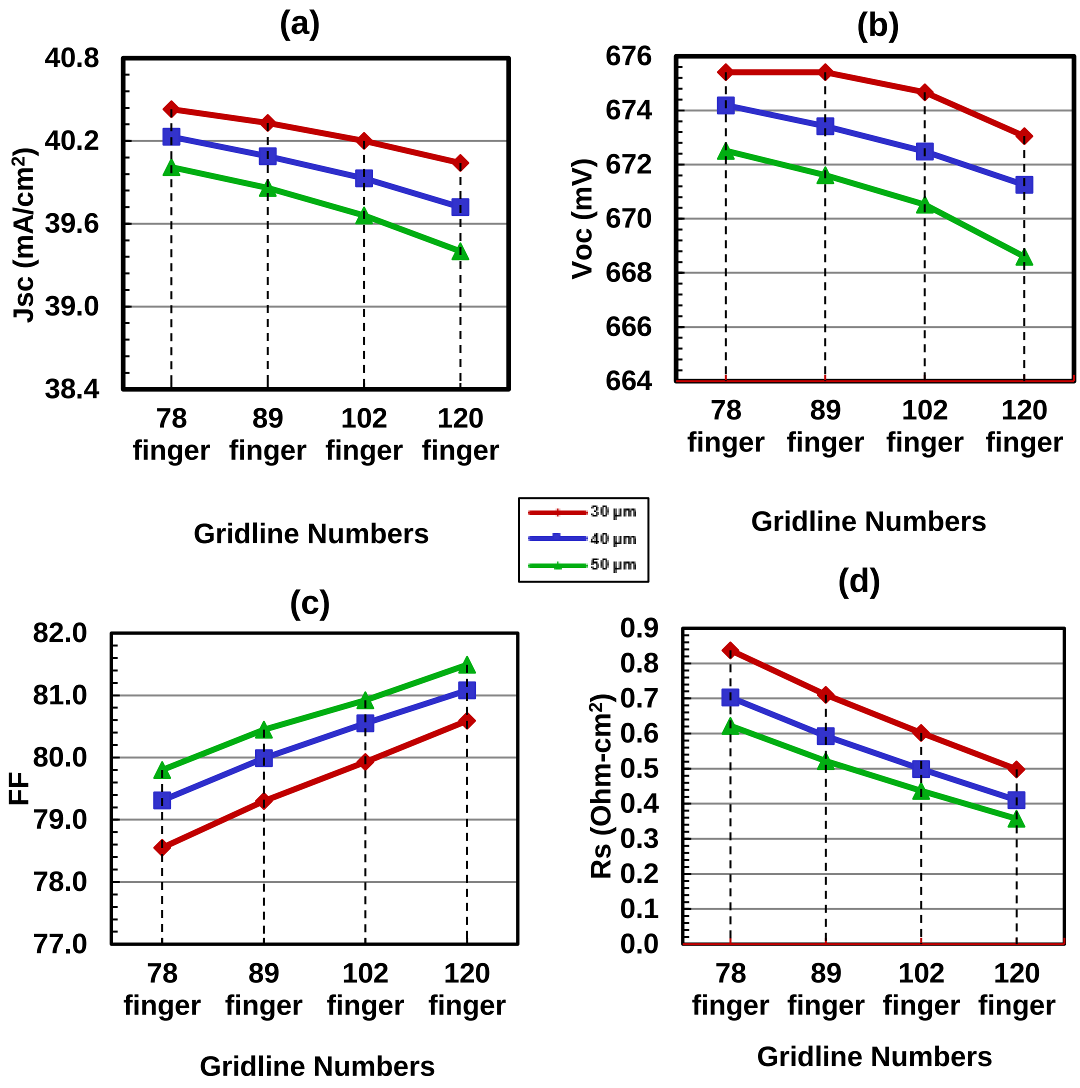


Fig. 5. 4. Bifacial electrical output parameters with varying number and width of gridline.

emitter saturation current is a function of metal-Si recombination current under the contact region and passivation induced recombination current in the rest of the surface region. For the 30μm gridline, F_m is low, therefore the emitter recombination current is small, and hence the V_{OC} is high. For the case of 89 gridlines an absolute increase of 3mV is obtained when the gridline width decreases from 50μm to 30μm.

The R_S and FF have opposite relationship with the gridline widths and numbers - Figs. 5.4(c) and 5.4(d). As the width is decreased, Rs increases, which results in a proportional FF loss. It is observed that, the wider the gridlines, the lower the R_S and the higher the FF. For 89 gridlines, when the width decreases from 50 μm to 30 μm, an absolute increase of 0.3 ohm-cm^2 R_S causes an absolute 1.5% loss in FF.

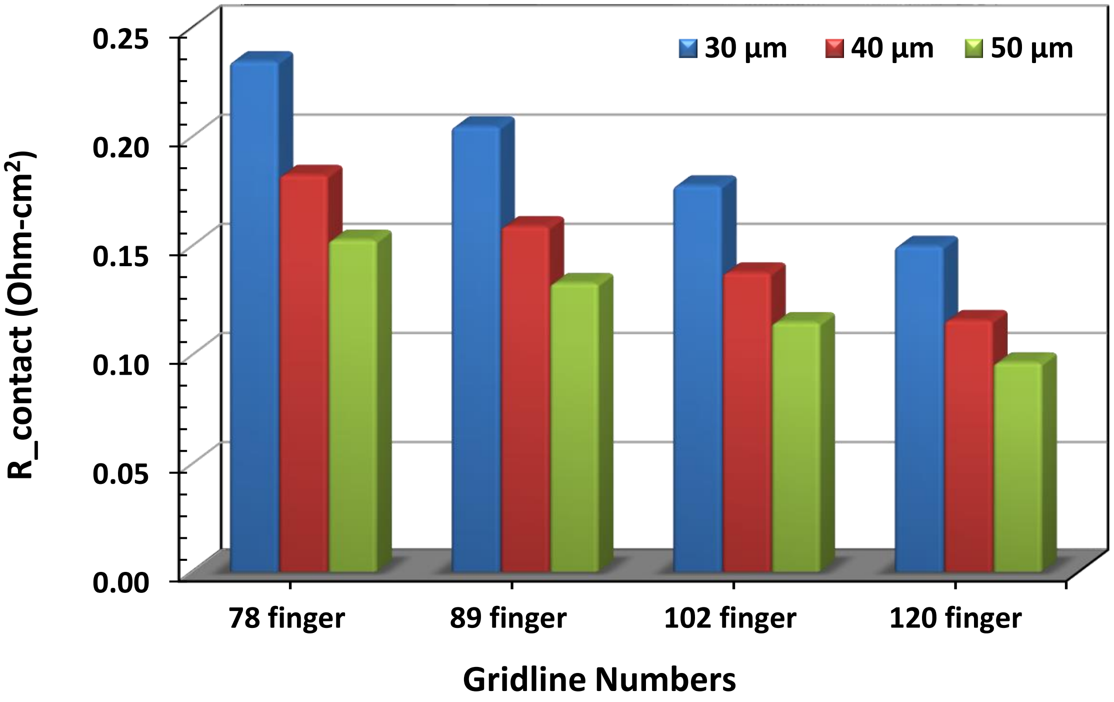


Fig. 5. 5. Contact resistance (R_contact) as a function of number and gridline width.

The six components of the series resistance are (i) R$_{\_contact}$, (ii) R$_{\_emitter}$, (iii) R$_{\_gridline}$ (iv) R$_{\_Bus\text{-}Bar}$ (v) R$_{\_substrate}$ (vi) R$_{\_back}$. Of these six components, the contact and emitter are further explored to understand their impact as the number of gridline increases - Figs. 5.5. and 5.6. Fig. 5.5. shows that, the contact resistance decreases as the gridline width and number of gridlines. However, the emitter resistance dominates as the number of gridline decreases with very little margin for the different widths (Fig. 5.6).

It is interesting to note that, with varying number of gridlines R_S, J_{SC}, FF maintains almost linear relationship. However, there is some nonlinearity observed in the Voc. Especially for gridline widths of 30 µm and 50 µm there are more nonlinearity compared to the 40 µm width

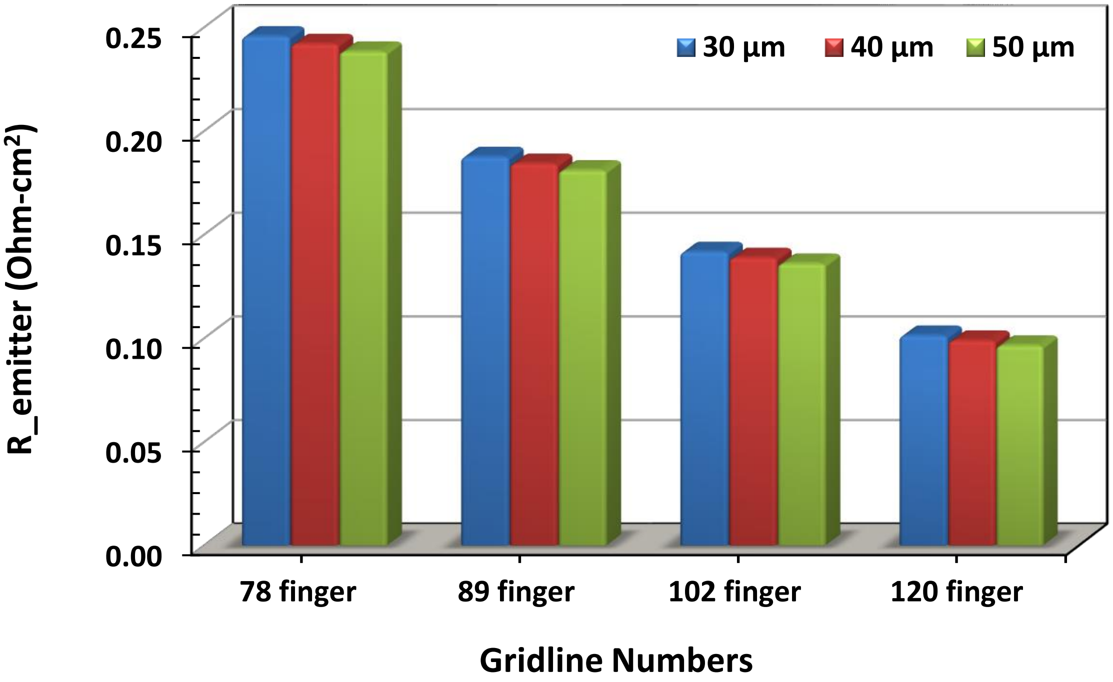


Fig. 5. 6. Emitter resistance (R_emitter) as a function of gridline number and width of gridlines.

counterpart. To investigate this phenomenon, the impact of lateral current was modeled. Fig. 5.7. presents the contour maps for a 78, 89 and 120 gridlines, respectively, with 30 µm width. Each map is a representation of electron quasi-fermi potential which indicates the electron flows in the unit area of the simulated region. The upper left corner is the contact and the upper right corner is exactly the middle point between two consecutive gridlines. Different spectrum represents different voltage levels, hence the contour with 78 gridlines exhibits the largest lateral voltage drop compared to the 120.gridlines. Thus, even though the lateral voltage drop is lowest for the 120 gridlines, the loss in short circuit current due to increased shadowing, over shadows this advantage.

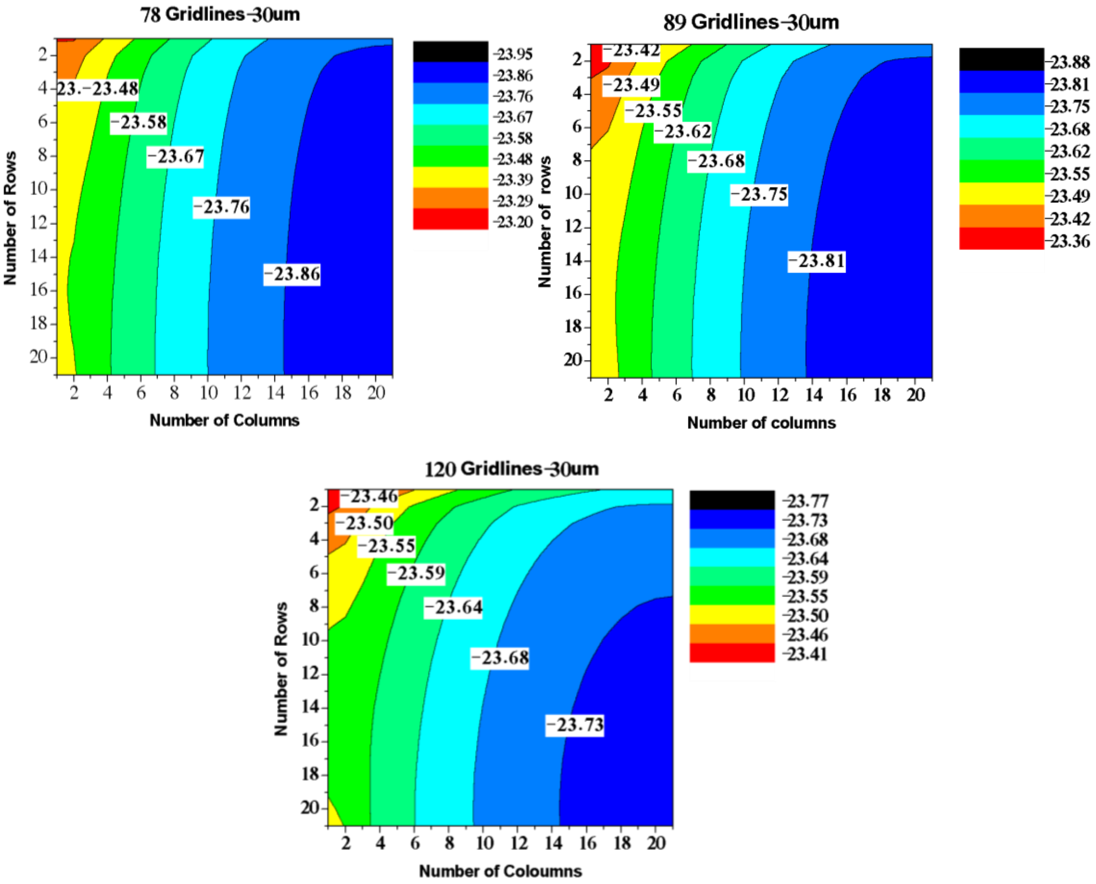


Fig. 5. 7. Contour maps showing electron flow in the modeled unit area representing the electron fermi potentials. The maximum lateral voltage drops observed in 78 gridlines contour compared to the 120 gridlines.

5.3.2.2. Segmented Gridlines

Segmented Gridline concept is adopted for the bifacial cells in designing the front and rear contacts. The advantage of street concept is to reduce the metallization cost (Ag consumption) and without losing on the efficiency. This concept was applied to the bifacial structure with 89 gridlines with 30μm gridlines. The 30μm width was chosen because it exhibited the best efficiency with the continuous gridlines (CG).

The simulated electrical output parameters are listed in Table 5.2. The street widths were varied from 0 to 5-mm and the impact on cell performance was recorded. The absolute V_{OC} decreases

Table 5. 2. Performance of bifacial cell with different street widths

Street Width (mm)	Effective number of fingers	Shadow (%)	Voc (mV)	Jsc (mA/cm2)	FF (%)	PC2D η (%)
0	**89**	**3.30**	**676.33**	**40.34**	**79.56**	**21.70**
1	**87**	**3.26**	**676.50**	**40.35**	**79.47**	**21.69**
2	**84**	**3.21**	**676.72**	**40.37**	**79.07**	**21.60**
3	**82**	**3.17**	**676.90**	**40.39**	**78.70**	**21.52**
4	**80**	**3.12**	**677.12**	**40.41**	**78.43**	**21.46**
5	**78**	**3.08**	**677.29**	**40.43**	**77.90**	**21.33**

of 0.38 mV was observed for the 5-mm street width compared to the CG configuration. However, for 1-mm street width, the efficiency reduced minimally by ~0.01%. This indicates, the 1-mm street width for the SG is comparable to the CG in efficiency, while decreasing Ag consumption. Thus, a more cost effective bifacial cell can be fabricated. The slight increase in J_{SC} and V_{OC} is due to lower F_M, which has less shadowing and lower area weighted recombination current, respectively. The FF decreases because of the influence of R_S, which has the tendency to reduce the efficiency as shown in Fig. 5.8.

To understand the FF loss, detail resistance breakdown is shown in Fig. 5.9 for CG and SG having street widths of 5-mm. Among the six components of R_S, contact and emitter resistances are significantly impacted by the street concept. The contact and emitter resistances increased to 0.041 ohm-cm^2 (absolute) and 0.258 ohm-cm^2 (absolute) for the 5-mm street width design. The contact resistance increase is due to the increase in lateral current as shown in Fig. 5.10. The current crowding is maximum at the point adjacent to the contact and it reduces to minimum in the middle point between the two contacts.

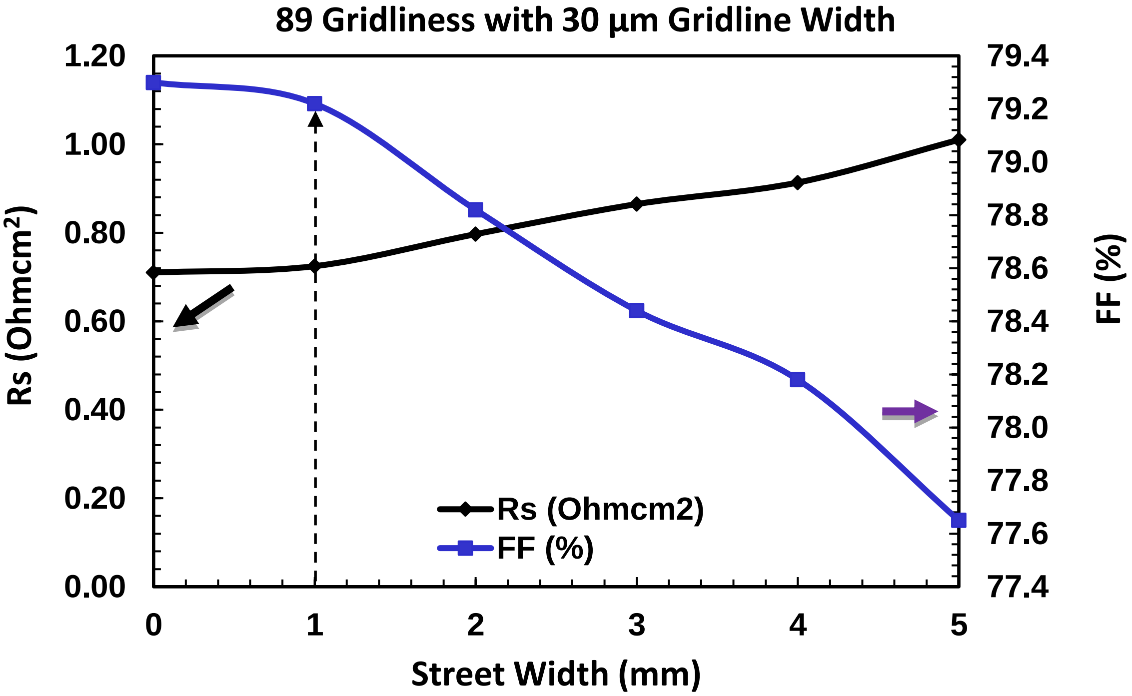


Fig. 5. 8. The RS and FF variation with different street widths.

5.3.2.3. Cost Analysis

Fig. 3.25. shows the Δ%Shadowing as a function of the number of gridlines for continuous (CG) and segmented (SG with 1 mm street width) gridlines. The Δ%Shadowing was derived by first calculating the shadowing for each of the three gridline widths (30µm, 40µmand 50µm) as a function of the number of gridlines. Then find the difference between them for each number of gridlines for both cells configuration. The Δ% Shadowing is linear and scales with the number of gridlines. However, since 89 gridlines gave the best efficiency for both 30 µm and 40 µm widths (Fig. 5.3.), the cost analysis will be focused around the difference between these two gridline widths as highlighted in Fig. 5.11. and Fig. 5.12. Fig.

5.12. shows the ΔCost (₵) as a function of the number of gridlines. Again, the ΔCost (₵) is a linear function of the number of gridlines. Thus, the cost per cell increases with the number of gridlines. Interesting to note is the difference between the CG and SG, which shows a 0.02₵ per wafer. This means, for a typical bifacial cell with ~4.8W power output, 0.096₵ would be saved in Ag consumption. Although it seems very minuscule for a single cell, but for a 4.8-GW plant, this will result in $9.6M savings in Ag paste. Applying segmented gridlines on both sides of the cell, the cost savings will be doubled to ΔCost (₵) 0.196₵. For a large-scale production this cost saving has a significant effect.

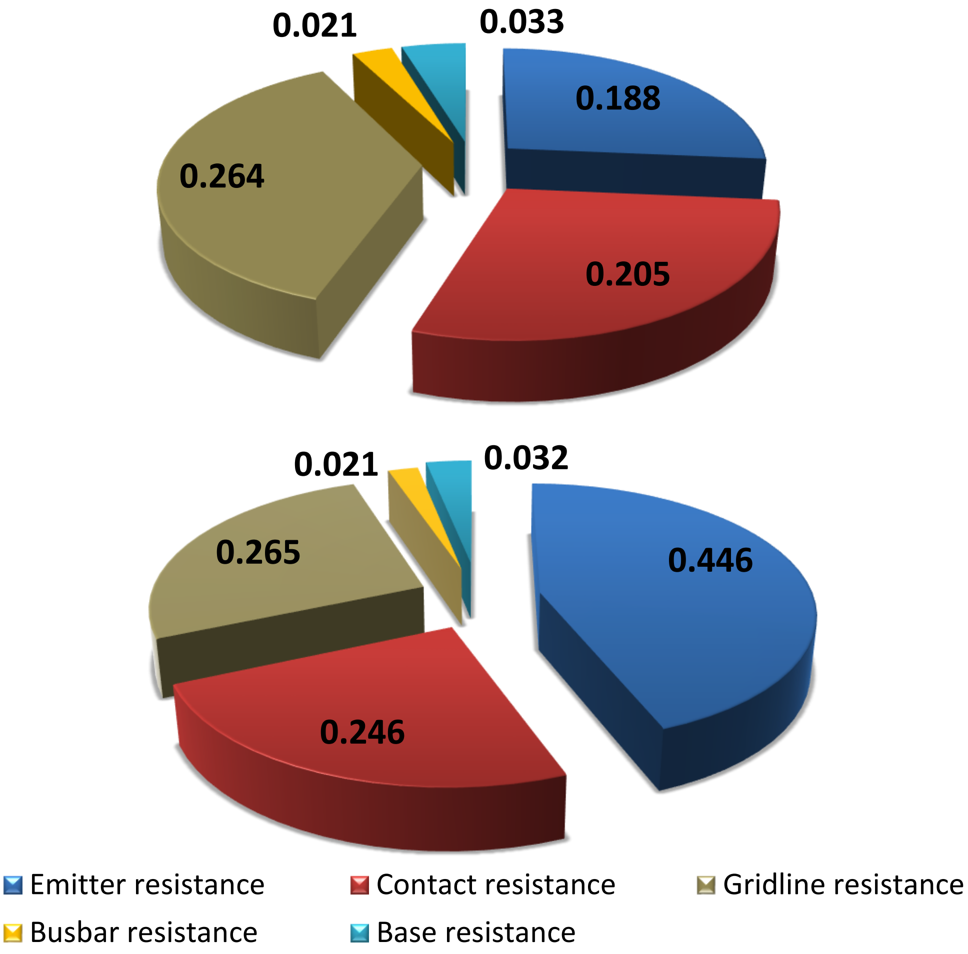


Fig. 5. 9. The RS components of 89 gridlines with 30μm width for continuous (top) and segmented (bottom) gridlines.

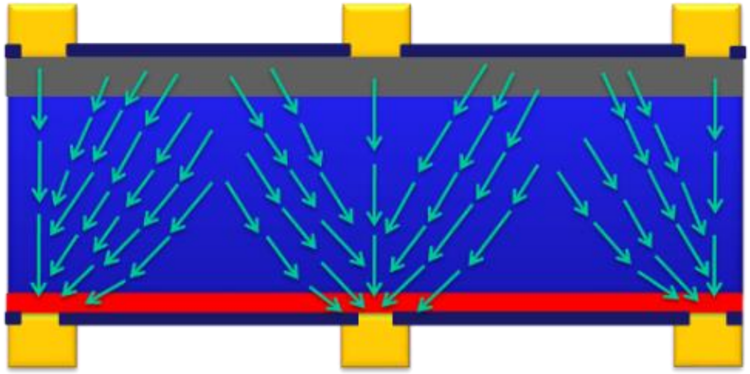


Fig. 5. 10. The sketch of lateral current crowding adjacent to the contacts.

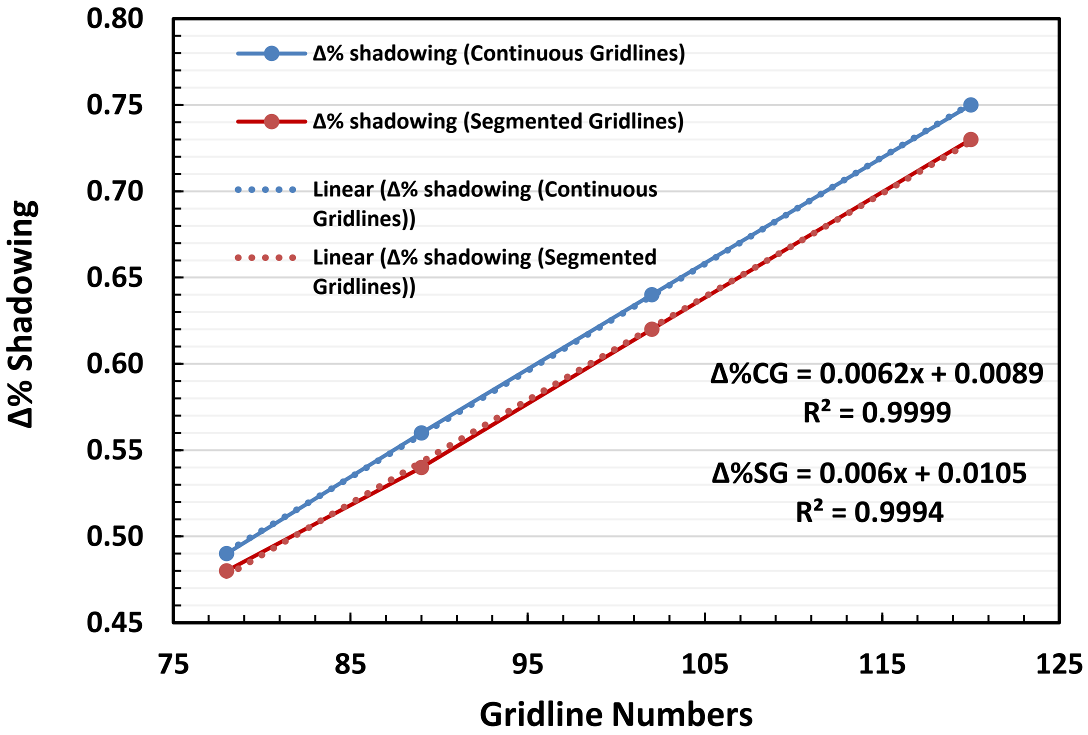


Fig. 5. 11. Δ% shadowing as a function of gridline numbers.

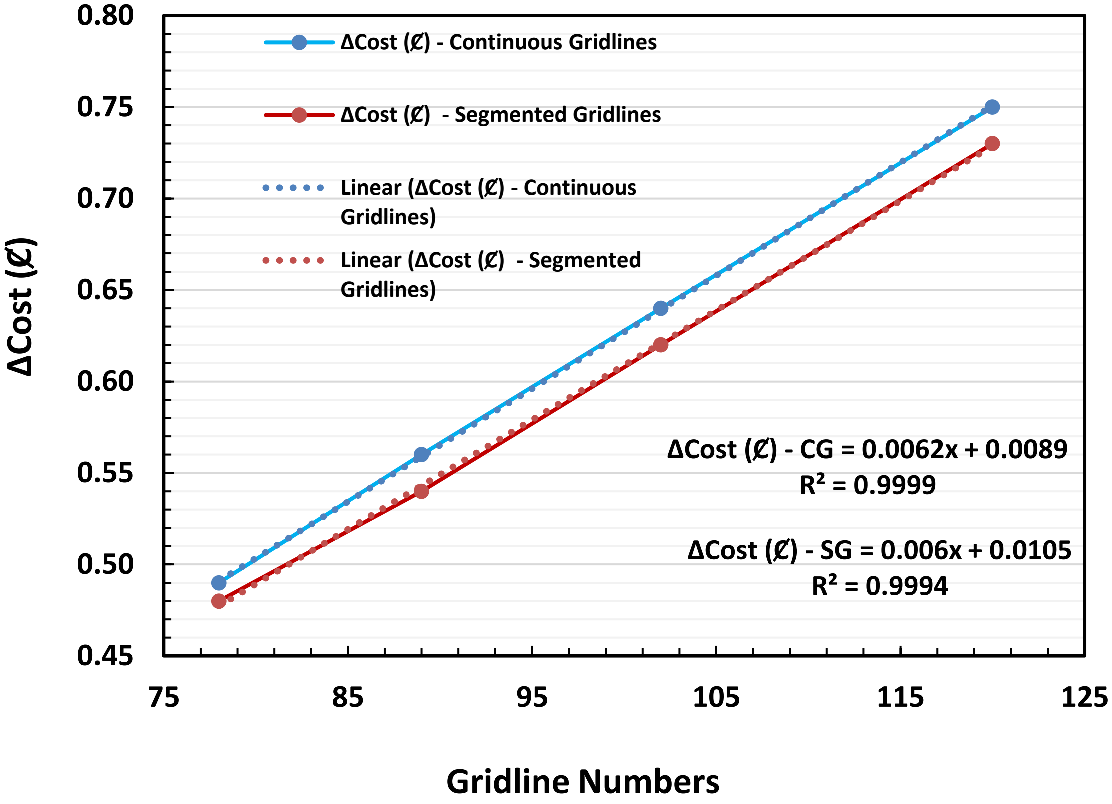


Fig. 5. 12. Δ Cost (₡) as a function of number of gridlines.

5.3.2.4. Impact of Rear Recombination

The recombination current density (J_{o1}) in a solar cell consists of J_{oe} and J_{ob}. In a bifacial cell, the J_{ob} can further be divided into $J_{o(ob)}$ and $J_{o(bsf)}$, respectively, representing base and back surface field recombination. This is related in Eq. (5.1), where J_{oe} is the emitter recombination current density.

$$J_{o1} = J_{oe} + J_{ob} + J_{obsf} \tag{5.1}$$

The base recombination current is an inherent material property, which depends on bulk lifetime of the wafer. In the simulation design the J_{ob} value of ~100 fA/cm^2 was assumed. The front and rear recombination currents are dependent on the front and rear metallization design.

$$J_{oe} = J_{oe(metal)} \times F_m + J_{oe(pass)} \times (1 - F_m) \tag{5.2}$$

$$J_{obsf} = J_{obsf(metal)} \times F_m + J_{obsf(pass)} \times (1 - F_m) \tag{5.3}$$

The $J_{oe(metal)}$ and J_{obsf} are due to front and rear contacts. The recombination current density at the ARC in the remaining surface area depends on the quality of both front and rear surface passivation. In the simulation design, $J_{o(pass)}$ of ~ 20 fA/cm^{2}was assumed, which can be realized for a well-passivated surface with minimum recombination. For a typical Ag-Si and Ag/Al-Si contacts, the $J_{oe(m)}$ can be ~1000 fA/cm^2. The total recombination current density breakdown is shown in Fig. 5.13. and Table 5.3. displays the summary of the recombination currents components. The dominant contribution is from the front and rear metal-Si contacts, ~47%. However, efforts to decrease the dominance to increase V_{OC} is recently reported new contacting scheme of TOPCon [94]. Nevertheless, this technology involves additional processing steps which is not cost efficient.

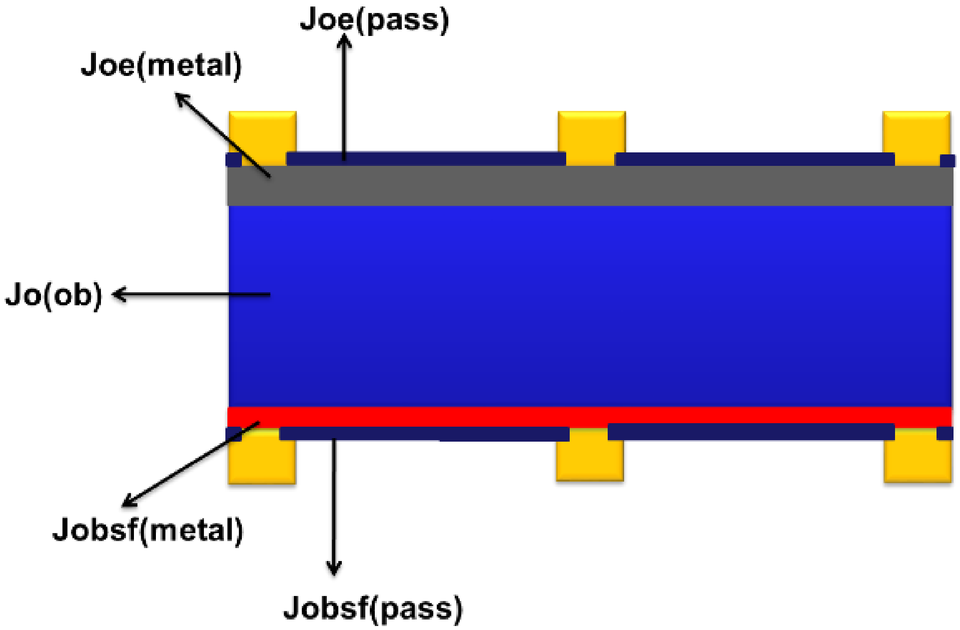


Fig. 5. 13. Bifacial solar cell recombination currents components.

Table 5. 3. Recombination current components of Bifacial cells.

Joe (metal) fA/cm^2	**Joe (pass) fA/cm^2**	**Jo(ob) fA/cm^2**	**Jobsf (metal) fA/cm^2**	**Jobsf (pass) fA/cm^2**
10	20	100	20	10

Fig. 5.14. shows the comparison of the percentage rear recombination loss in the bifacial and Al-BSF cells for the three gridline widths. The advantage of the rear passivation as in bifacial cell is evident in higher V_{OC} of 675 mV as opposed to 640 mV for the Al-BSF counterpart. The best observed performance in rear recombination is associated with 30 µm gridline widths as expected due to lower F_m. The relationship for F_M, J_{oe} and J_{o1} are shown in Fig. 5.15. The 30 µm gridline width has the lowest recombination current compared to the 40 µm and 50 µm counterparts.

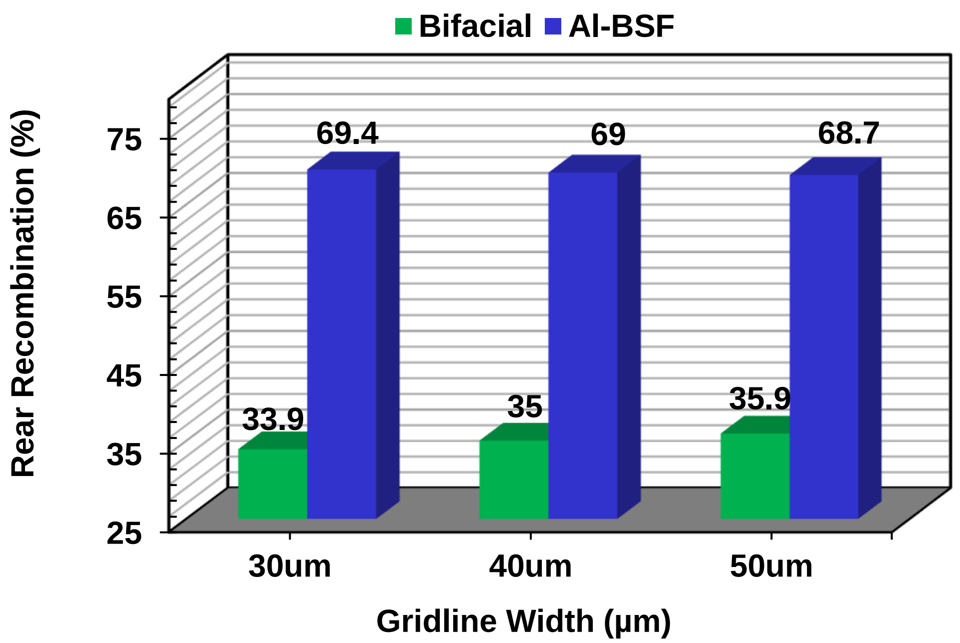


Fig. 5. 14. Rear recombination loss in Al-BSF and Bifacial structures.

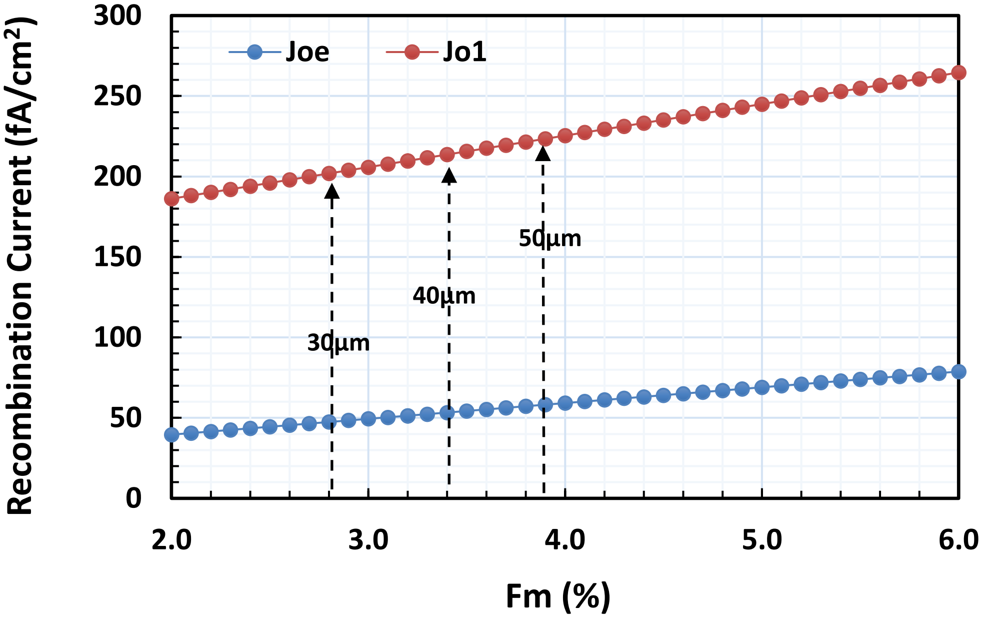


Fig. 5. 15. Different components of recombination currents in the bifacial structure.

5.3.2.5. Bifacial Illumination

Additional output power from the rear surface illumination is an additional attribute of an industrial bifacial solar cell application. Therefore, the rear illumination was varied to investigate the total output power, in addition to the front 1-sun illumination. Fig. 5.16. shows the output power as a function of total illumination level for 89 gridlines with 30 µm gridline width. Total power output increases with increasing illumination level from the rear side in addition to the front 1-sun. The ~28.11 mW output power attained at 1.3 suns (1 sun from front plus 0.3 suns from rear) is practically viable because 0.3 suns is the albedo – ground reflection. This implies a minimum effort is required to boost the power output from a bifacial cell. Moreover, rear illumination is increased beyond 0.3 suns to see potential of the structure. Under rear and front, 1 sun each, illumination, output power of 42.22 mW can be realized. It is important to note that with current technology advancement, rear surface illumination is of growing interest to meet the demand of high output power. Particularly by designing the rear reflector, bifacial cell is quite suited in concentrators for CPV.

Fig. 5.17. shows the FF, V_{OC} and J_{SC} as a function of total illumination. The FF decreases with total illumination level, while J_{SC} increases linearly and V_{OC} logarithmically. A relative gain of ~11.86 mA/cm^2 in J_{SC} is achieved compared to monofacial illumination. Also, additional illumination confirms increased carrier injection and thus improvement in rear surface passivation. Unlike J_{SC} and V_{OC} improvements, FF degrades with the total illumination level due to increased series resistance with total illumination.

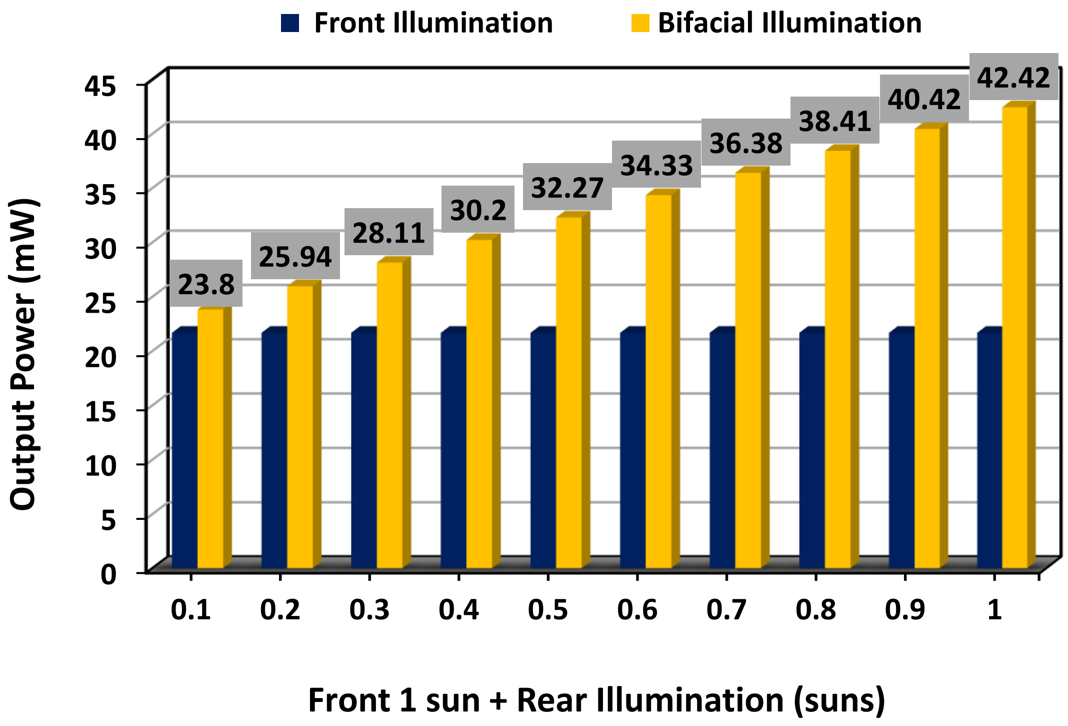
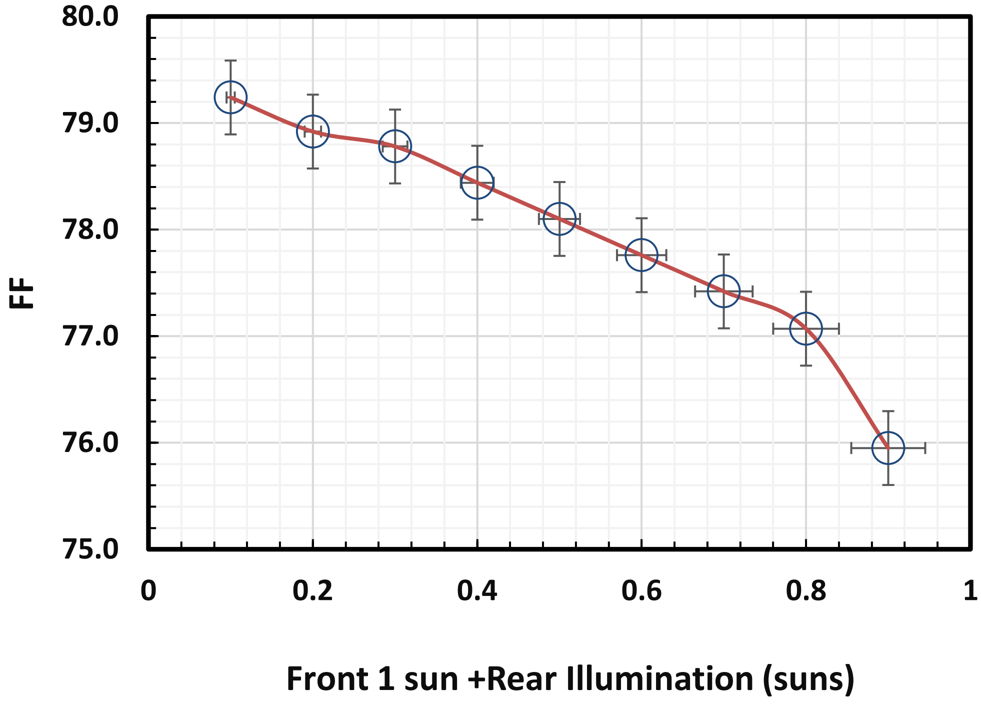


Fig. 5. 16. Total output power obtained from the bifacial illumination.



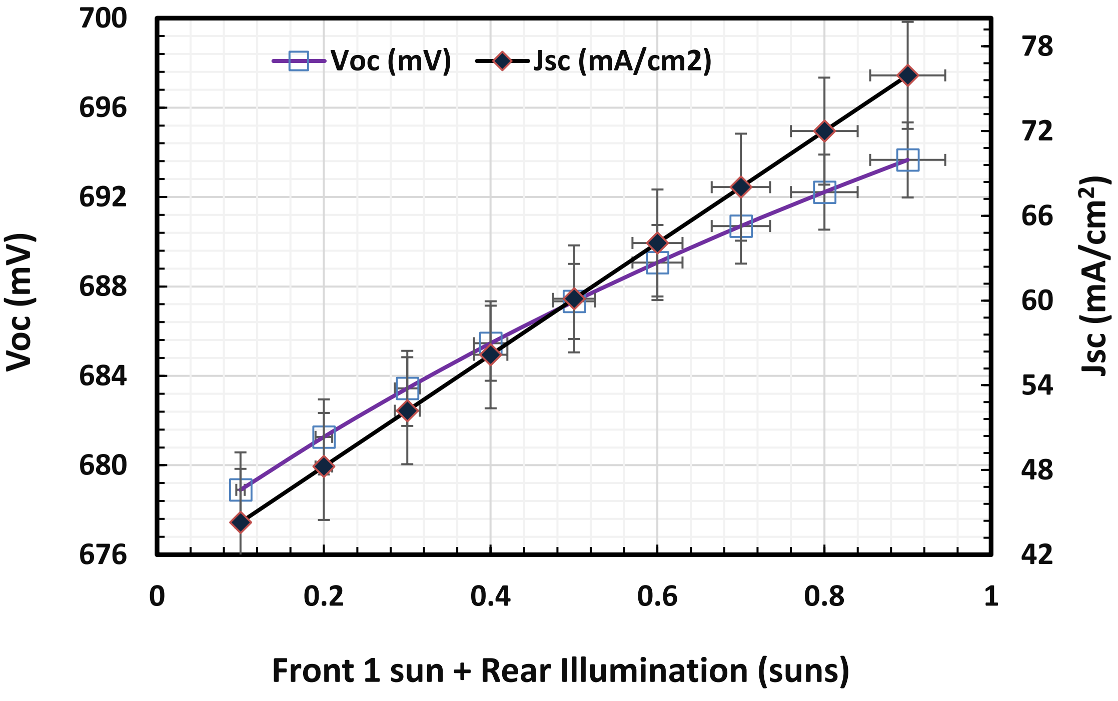


Fig. 5. 17. Electrical output parameters FF, V_{OC} and J_{SC} relationship with the Bifacial illumination.

5.4.3. Summary of Bifacial Cell Modeling

A cost effective high efficiency bifacial solar cell was designed and simulated using PC2D. Three gridline widths: 30μm, 40μm, and 50μm with varying number of gridlines, was simulated and the impact on η, FF, R_S, and V_{OC} were observed. The 30μm width showed superior performance in efficiency compared to the other two in continuous and segmented gridline designs. It was observed that, segmented gridline design having 1-mm street width resulted in the same efficiency compared with continuous design. This implies that the segmented design can achieve the same efficiency but at a lower cost of metallization.

Two-dimensional modelling reveals the lateral characteristics of minority carriers in the bifacial structure. Although the 120 gridlines resulted in the maximum lateral conductivity, the shading loss and cost-effectiveness are more important. Therefore, the 89 gridlines and 30 μm width having efficiency of ~21.70%, which is only $0.12\%_{\text{absolute}}$ difference, is preferable. The 30 μm gridline width at the rear contact has further potential in reducing the recombination and consequently achieving higher output power.

5.5. Fabrication of Screen printed Bifacial Solar Cell

This section demonstartes fabrication of industrial bifacial solar cells based on screen-printed technique. The detail fabrication process of bifacial cell is illustrated in Fig. 5.18. 2 Ω-cm base resistivity Czochralasky (CZ) n-type wafers were used with emitter sheet resistance of 60 Ω/sq and BSF sheet resistance of 45 Ω/sq. The fabrication of bifacial cell thus requires additional step of Boron diffusion in the rear side followed by rear SiN deposition which acts as a passivation and ARC layer. After treating the rear surface same processes were followed to develop the front surface, such as, a) texture b) $POCl_3$ diffusion and b) front SiN deposition. The metallization on both sides were conducted with screen printed technique.

We used same Ag paste for both front and rear contact formation. Finally, cofiring were conducted to form contact on both sides. Same firing profile as used in Al-BSF and FSF cell was implemented for the IR belt furnace cofiring.

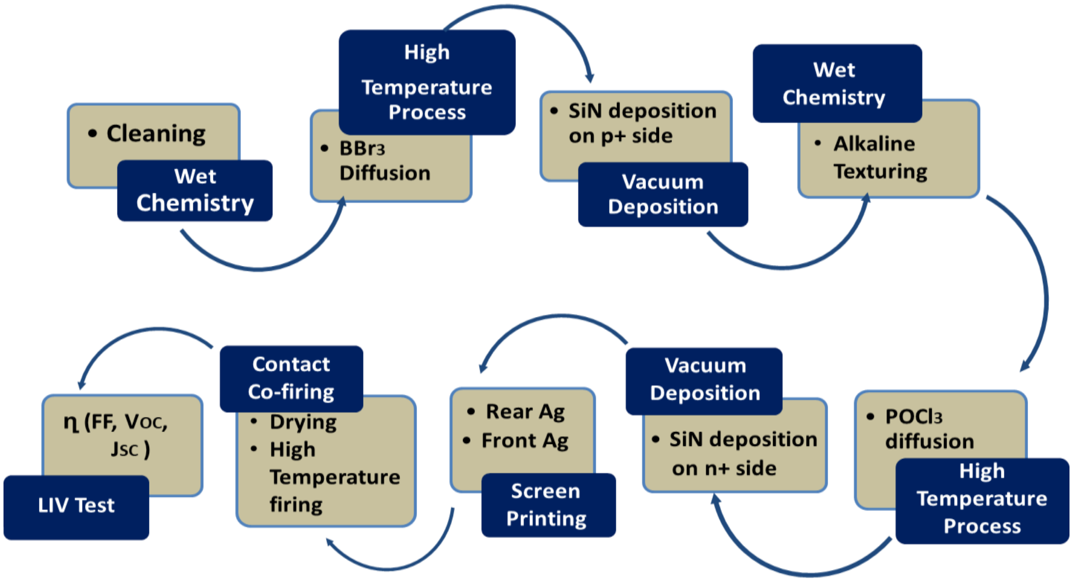


Fig. 5. 18. Commercial processing sequence for the fabrication of Bifacial cell.

5.6. Characterization of Bifacial Cell

5.6.1. Light IV Measurement

As shown in Table 5.4., The front and rear efficiency of ~13 % and ~9% were achieved. The V_{OC} of 618 mV is an indication bulk recombination in the wafer is very high resulting a poor-quality wafer. Another factor behind the low V_{OC} might be originated from the high J_{om} at the rear metal-Si contact on both front and rear sides. Unlike monofacial cells, the total area coverage of metal-Si contact is doubled. Hence, impact of J_{om} is more significant. Relatively low J_{SC} ~33.13 mA/cm^2 is caused by the unoptimized ARC thickness failed to provide maximum absorption. The J_{SC} ~32.73 mA/cm^2 at the rear side is somehow lower since high minority carrier lifetime is required to reach the junction at the front side. The extracted FF from front and rear side are ~65% and ~48% respectively. This caused the reduction of bifaciality factor to ~ 74%. The ideality factor of ~1.23 at the front side indicates over fired contact. On the other hand, the rear ideality factor ~1.03 represents a good contact formation.

Table 5. 4. Electrical Output Parameters OF Bifacial cells measured under Standard Test Conditions (AM 1.5G, 100mw/cm^2, 25^{o}C)

Cell ID	**n**	**V_{OC} (mV)**	**J_{SC} (mA/cm^2)**	**FF (%)**	**η (%)**	**Bifaciality Factor (%)**
Front	1.23	610.42	33.17	65.7	13.13	74.25
Rear	1.03	609.27	32.73	48.2	9.75	

5.6.2. Suns-V_{OC} Measurement

To find out the reason behind poor V_{OC} we conducted the Suns-V_{OC} measurement. Result from implied V_{OC} attributes a poor wafer quality with 617mV. The pseudo efficiency is ~17% is an indication that wafer quality needs to be improved. Although, J_{O1} and J_{O2} were not too low as expected, the front and rear FF reduction however did not occur from poor contact.

5.6.3. Resistance Breakdown

The series resistance is obtained from the following analytical relation,

$$R_S = \frac{V_{OC} \times J_{SC} \times (pFF - FF)}{J_{mp}^2} \tag{5.6}$$

From the light IV data, the R_S for different structures is shown in Fig. compared to monofacial cells, bifacial cells exhibit high R_S of 12.03 **Ω**-cm^2 and 3.61 **Ω**-cm^2 for front and rear illuminations respectively. In contrast, monofacial cells exhibits lowers Rs as shown in Fig. To investigate the high Rs furthermore contact resistance was measured with 4-point probe

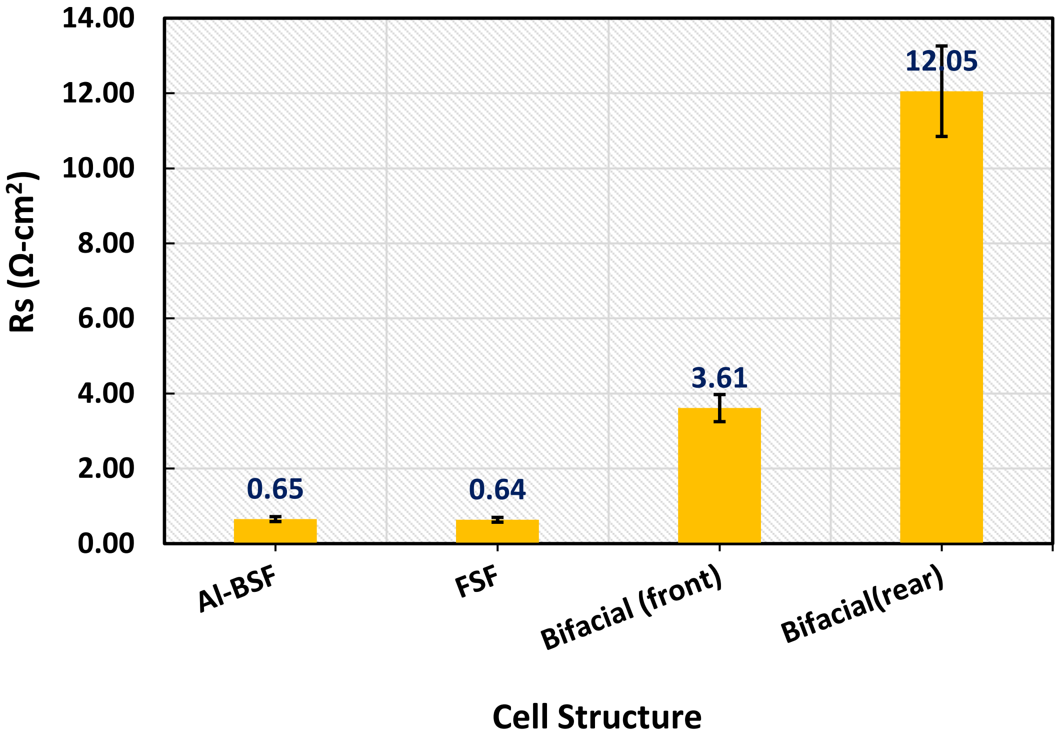


Fig. 5. 19. Series Resistance analysis based on various solar cell structures.

technique. Front and rear contact resistances were 20 mΩ-cm^2 and 2 mΩ-cm^2 respectively as shown in Table 5.5. Since the sheet resistances of both front and rear sides are low, higher contact resistance were expected. However, contact resistances were relatively low. This further raised the concern on gridline resistances. As observed from the top view of front and rear gridlines in Fig.5.20., there were breakage and discontinuity in the gridlines. This probably caused towards high Rs and thus poor cell performance. Thus, even though same Ag paste was utilized for both front and rear contact formation, it was quite remarkable that very low contact resistance was achieved. Generally, with Ag paste the rear p+ contact does not acquire good contact resistance, therefore Ag-Al paste has been utilized by the scientific community to reduce the contact resistance. Our experimental result is an indication that this Ag paste can be a suitable alternative to the conventional Ag-Al paste used for rear contact formation in bifacial screen printed solar cell.

Table 5. 5. Series Resistance and contact resistance measurement for Bifacial Cell

Cell ID	**pFF**	**R_S (Ω-cm^2)**	**R_C (mΩ-cm^2)**
Front	0.83	3.61	2.7
Rear	0.832	12.053	20.56

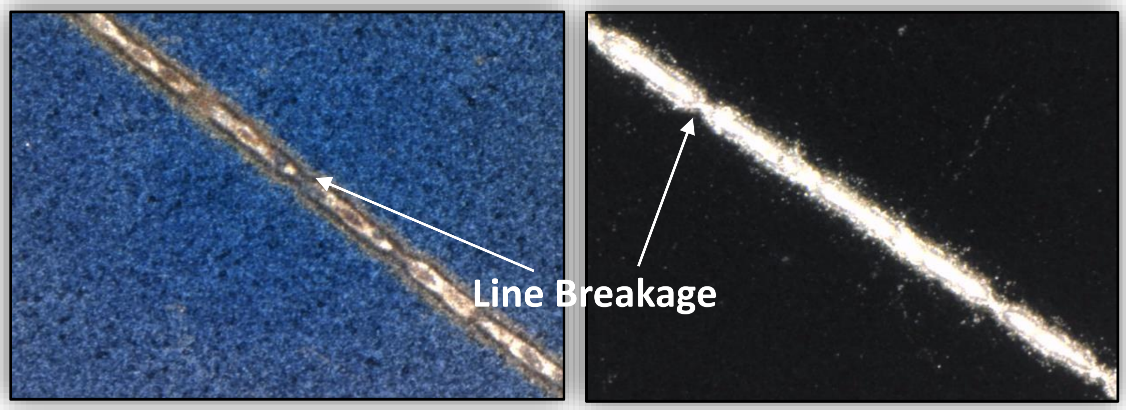


Fig. 5. 20. Top view of screen printed bifacial solar cell gridlines obtained from high resolution camera; (a) front side, and (b) rear side.

To understand the impact of series resistance components, the detail R_S of a bifacial cell is presented in Fig 5.21. The analytical solution is carried out on the basis of Dan Meier model et al. [95] For the bifacial cell, the model is extended considering the impact of rear surface. The total series resistance components of bifacial cell can be expressed as,

$$R_S = R_{busbar(front)} + R_{gridline\,(front)} + R_{contact(front)} + R_{sheet(front)} + R_{base} + R_{sheet(rear)} + R_{contact(rear)} + R_{gridline\,(rear)} + R_{busbar(rear)} \tag{5.7}$$

The Gridline and sheet resistance from both and rear sides are major two components that dominates the overall resistance. Improvement can be done in the contact resistance by using a more optimized Ag paste for both front and rear contact formation. By overcoming the gridline resistance loss by better printing will further improve the FF. Considering, optimized gridline and contact resistance, the best modeled bifacial front and rear FF can be achieved ~77% and ~79% respectively. The differences in FF mainly originated by the ideality factor as observed in the empirical data. Since, both front and rear has the same F_M, the discrepancy in FF is not caused by the very minute J_{SC} difference from front and rear sides. Therefore, an optimized firing needs to be implemented to improve the FF and efficiency.

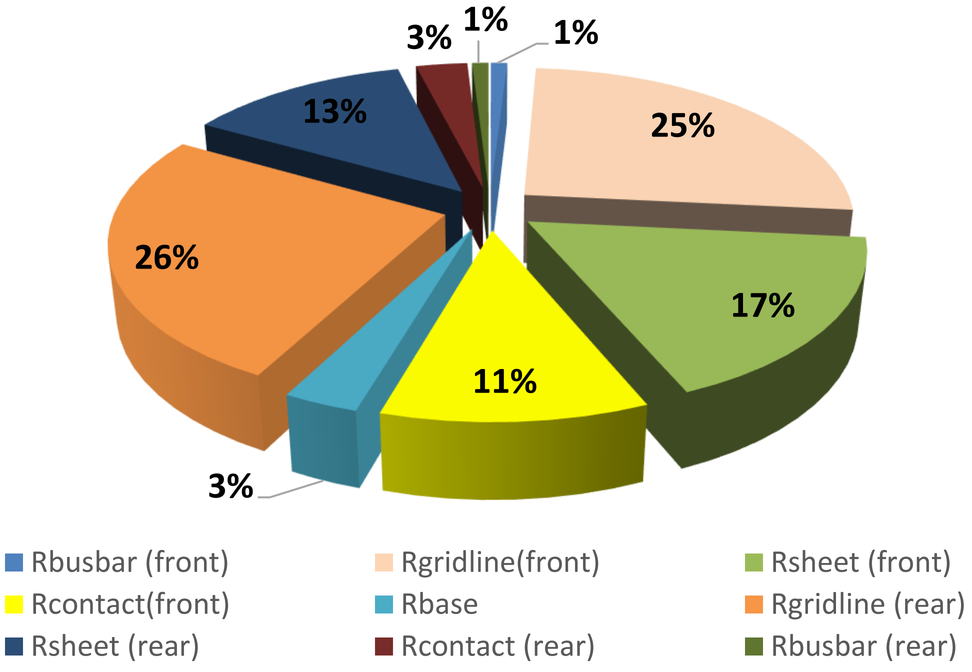


Fig. 5. 21. Percentage Series Resistance breakdown of a bifacial cell.

5.7. Analysis towards achieving high efficiency bifacial cell

To improve the cell performance of bifacial cell, we performed step by step modeling in PC2D. The goal is to achieve high efficiency cell performance at the end of the process. Firstly, front and rear sheet resistances were improved. We utilized current trend of homogeneous high sheet resistance emitter and BSF. This resulted a gain of 2.05%$_{abs}$. In order to gain high J_{SC} we optimized the SiN layer thickness using OPAL2. This improved the cell performance 1.05%$_{abs}$. Additionally, a double stack SiN/SiO$_2$ layer can improve the cell performance 1.15%$_{abs}$. High FF from a bifacial cell can be achieved by optimizing the firing conditions. Since, rear side Ag-Si contact is critical, by optimizing Ag paste or Ag-Al pate or Al paste can improve the cell performance significantly. Thus, improving FF of 80% from both front and rear side can help to increase the cell efficiency by 3%$_{abs}$. Finally, wafer lifetime was increased to 200 µs, and front and rear recombination velocity was reduced to 10 cm/s, which resulted a bifacial cell ~ 21.68%. (Fig. 5.22. and Table 5.6.)

Table 5. 6. Development of Bifacial Cell Performance

Process	**Development**
Present	Best Experimental Cell
Process b	Optimization in front and rear sheet resistance
Process c	Optimization of Single layer ARC
Process d	Implementing double layer SiN/SiO$_2$ ARC
Process e	Improving contact resistance though front Ag
Process f	Improving rear contact resistance by Al-Ag paste
Future	Improved bulk life time and surface recombination velocity

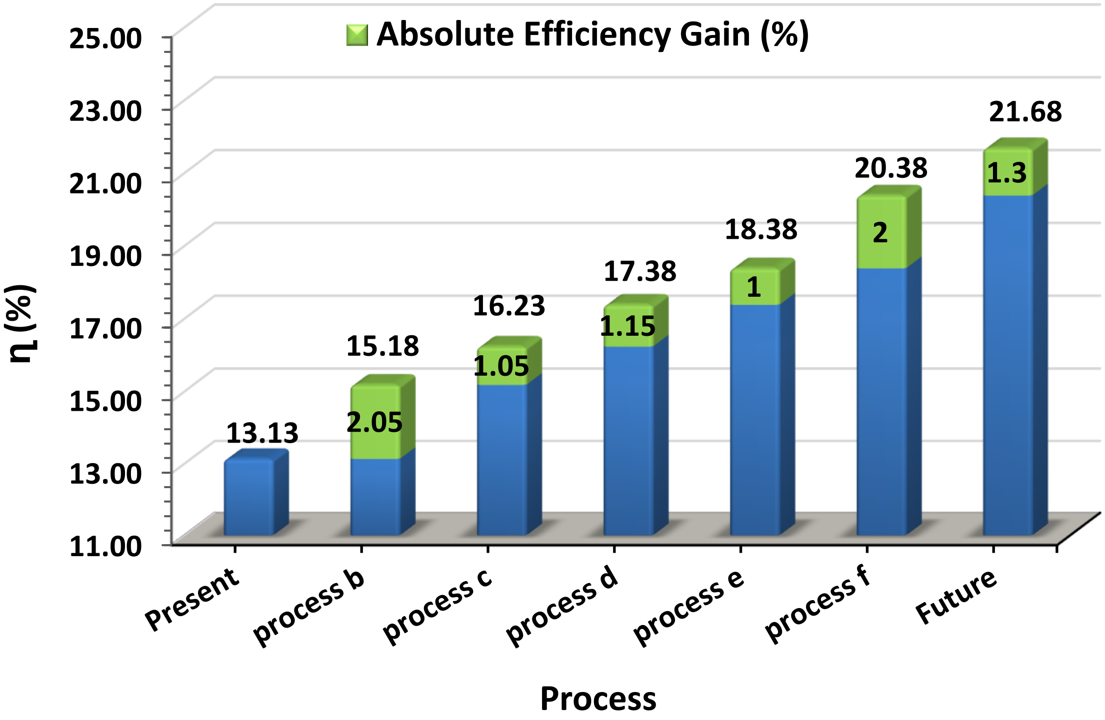


Fig. 5. 22. Loss analysis and approach towards front 21.68% efficiency bifacial cell.

5.8. Summary & Conclusions

Detail modeling was carried out to exploit the scopes of screen-printed bifacial cells. ~21.68% bifacial cell was modeled with 89 gridlines in 30 µm width. The innovative metallization design was followed to reduce the Ag cost from both and sides of the cell. Cost analysis results unfolded that, ~0.02 Cents/wafer is savings is possible which can be translated as a collective savings of 9.6 M$ for a 4.8 GW plant. Following, the modeling and detail cost analysis bifacial cells are processed in substrate independent fabrication technique. ~13.13% front and ~9.75% rear efficiencies are reported in the fabricated bifacial solar cell. The cells were characterized in detail to investigate the loss analysis. It was found that wafer quality was poor thus the maximum capacity of ~17% efficiency is achievable with this test wafer. Although, high Rs were observed from in both front and rear sides, resistance breakdown result shows that contact resistance did not contribute towards low FF. The combined effect of high base and gridline resistance impacted the cell performance significantly. Since, the Ag paste represents low R_C further microanalysis is needed to find out the potential of such paste. Detail resistive loss analysis was carried out to achieve front and rear FF of ~77% and 79% respectively. Finally, a roadmap is shown to improve the screen printed bifacial cell cell performance towards ~21.68% efficiency.

CHAPTER 06: SUMMARY & FUTURE WORK

6.1. Summary

A detail investigation on industrial Si solar cells is carried out this thesis. To curtail the cost while retaining high efficiency cell performance we focused on the contact metallization design. Based on this, Al-BSF, FSF and bifacial cells were modeled to project maximum efficiency capacity. The modeling was conducted in two-dimensional simulation software to account the effect of lateral current. The modelled result reveals that >20.5% Al-BSF, >22% FSF cell and ~22% bifacial cells can be achievable.

Modeling was further extended to FSF and bifacial cells to assess the lateral current impact on cell performance. It was found that high sheet resistance combined with high base resistivity n-type wafer improves the lateral performance of FSF cell by reducing the current crowding. The rear emitter at the FSF cell also had significant impact on cell performance, thus emitter coverage was varied. A combination of emitter extension and improved surface passivation resulted an absolute gain of $0.42\%_{abs}$ in FSF cell. For bifacial cell, emphasize was given on the cost effectivity since both front and rear surface had metallization contacts. Optimization on the gridline widths was performed to find out the best cell result with reduced cost. It was revealed that 89 gridlines on 1 mm street width is capable of attaining high efficiency ~21.68% while reducing the cost at the same time. The impact of rear illumination and rear recombination were studied in order to achieve high efficiency bifacial cells.

To translate the modeled result into the fabrication process, we made an effort to fabricate, characterize and analyze Al-BSF, FSF and bifacial cells. The processing sequences are adapted with substrate independent fabrication technique. The best fabricated result of~19.4%

efficiency is achieved with Al-BSF cell. During metallization, screen-printing process was monitored carefully to find out optimum a) print speed, b) print pressure, and the c) snap off. Furthermore, cell performance was investigated by variation of co-firing belt speed cells. It is observed that, fast belt speed enables high cell performance and high throughput. In order to achieve throughput 5000 wafer>hr., implementation of fast firing belt speed is necessary. Subsequently, a step by step improvement of cell performance is demonstrated to achieve >20.5% Al-BSF cell.

Since, n-type cells are immune with material impurity and thus no LID, we further explored the n-type FSF cells. The best attained efficiency was 18.4% with a FF of 79.3%. Unlike, p type cells for n-type cells it is critical to maintain a high carrier lifetime base material. The characterization result reveals that further improvement in cell performance is possible by optimizing the front ARC layer. Additionally, a roadmap is provided to reach ~22% FSF cell by incorporating a) emitter extension b) improved surface passivation and c) double layer SiN/SiO_2 passivation/ARC.

Finally, bifacial cells were fabricated and characterized. The best bifacial cell achieved 13.13% front and 9.65% rear efficiency with a bifaciality factor of 72%. The characterization in implied result reveals that maximum efficiency of 17% can be achievable with these wafers. In loss analysis we found that contact resistance did not contribute in the degradation of cell performance, rather high base resistance and gridline resistances were responsible in low FF. Provided that a high-quality base wafer can be utilized, step by step progress in cell performance is demonstrated to attain ~21.68% screen printed bifacial cell. The Summary of this work is portrayed in Fig. 6.2.

6.2. Future Works

6.2.1. Improving Metallization Design

The metallization design in this thesis was based predominantly on the street concept. This design worked as an alternative approach for reducing the Ag cost owing to lower shading factor. We will further strive to find a lower shading factor via metallization design. Nonuniform gridlines can be a solution towards this search. In this concept, the gridline width gradually reduces away from the busbars. As shown in Fig. 7.1. the gridlines adjacent to the busbars are wider, and width further shrinks. This concept is more effective in our street metallization design. Current underneath the street is lowest and as it approaches towards the busbars current crowding increases. Thus, current collection can be effective with this nonuniform gridlines providing a path for reduction in current crowding.

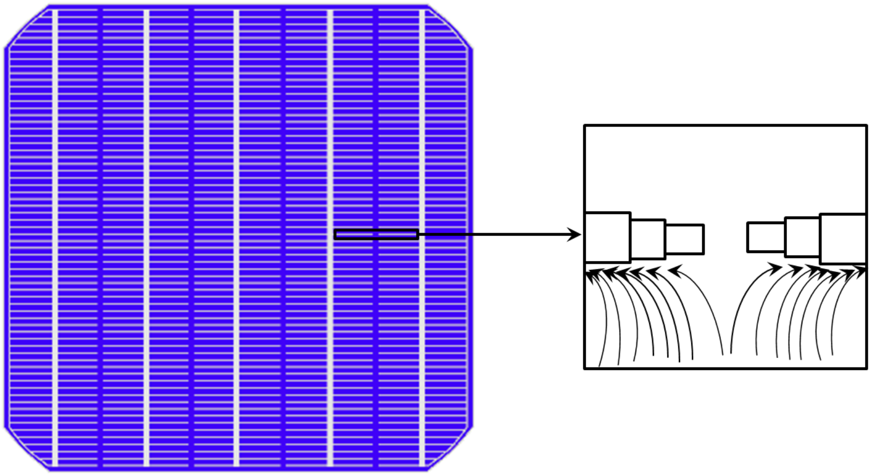


Fig. 6. 1. Concept of nonuniform gridlines and current crowding underneath the gridlines.

6.2.2. Implementing Al_2O_3 Passivation in Screen Printed Bifacial cell

In future, Al_2O_3 passivation layer will be utilized for the rear passivation in bifacial cells. The Al_2O_3 layer is commonly used in PERC (Passivated Emitter Rear Contact) cell to improve the V_{OC} and hence overall cell performance. [96] Combining the Al_2O_3 layer in the fine line

(~30 µm gridline width) screen-printing technique, bifacial cell therefore has the potential to attain ~23% efficiency.

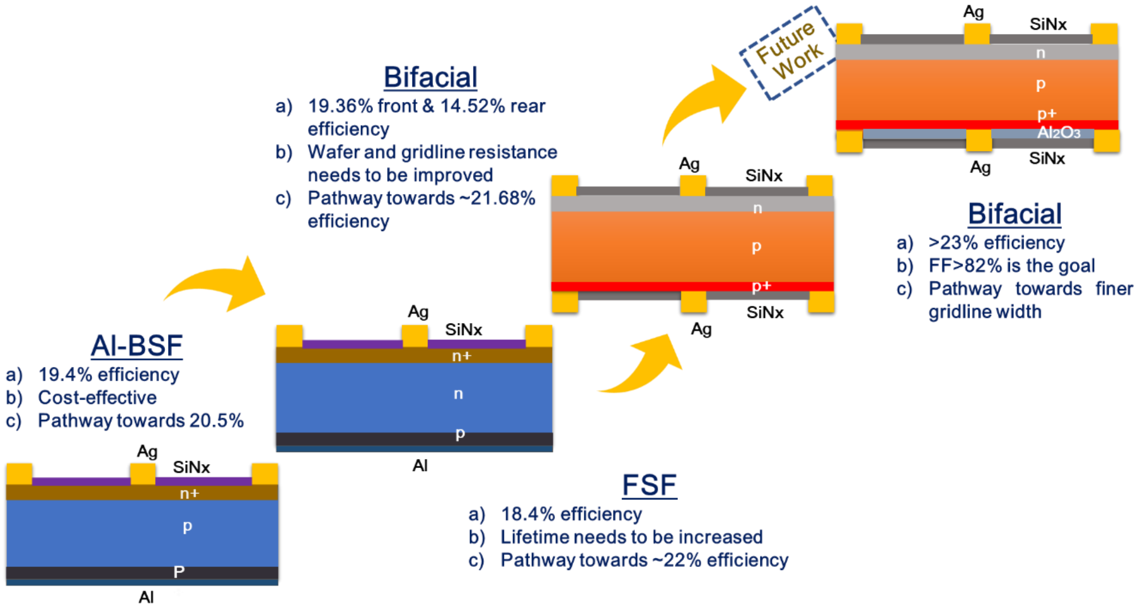


Fig. 6. 2. Summary and future work pertaining to this thesis.

REFERENCES

[1] (2017). http://www.worldenergyoutlook.org/resources/energydevelopment/energyaccessdatabase/.

[2] (2017). https://www.eia.gov/outlooks/ieo/pdf/0484(2017).pdf.

[3] (2017, July 12,2017). https://www.ise.fraunhofer.de/en/publications/studies/photovoltaics-report.html.

[4] http://resourceirena.irena.org/gateway/dashboard/?topic=17&subTopic=55.

[5] (2016). https://www.bloomberg.com/news/articles/2017-01-03/for-cheapest-power-on-earth-look-skyward-as-coal-falls-to-solar.

[6] http://resourceirena.irena.org/gateway/dashboard/?topic=3&subTopic=1057.

[7] "ITRPV Eighth Edition 2017," 2017.

[8] P. A. Basore and K. Cabanas-Holmen, "PC2D: A Circular-Reference Spreadsheet Solar Cell Device Simulator," *IEEE Journal of Photovoltaics,* vol. 1, pp. 72-77, 2011.

[9] M. T. Zarmai, N. N. Ekere, C. F. Oduoza, and E. H. Amalu, "A review of interconnection technologies for improved crystalline silicon solar cell photovoltaic module assembly," *Applied Energy,* vol. 154, pp. 173-182, 2015/09/15/ 2015.

[10] T. Uematsu, K. Tsutsui, Y. Yazawa, T. Warabisako, I. Araki, Y. Eguchi*, et al.*, "Development of bifacial PV cells for new applications of flat-plate modules," *Solar Energy Materials and Solar Cells,* vol. 75, pp. 557-566, 2003/02/01/ 2003.

[11] O. Isabella, K. Jäger, A. Smets, R. v. Swaaij, and M. Zeman, *Solar Energy: The Physics and Engineering of Photovoltaic Conversion, Technologies and Systems*: UIT Cambridge Ltd, 2016.

[12] *Basic Photovoltaic Principles and Methods*, 1982.

[13] A. Richter, M. Hermle, and S. W. Glunz, "Reassessment of the Limiting Efficiency for Crystalline Silicon Solar Cells," *IEEE Journal of Photovoltaics,* vol. 3, pp. 1184-1191, 2013.

[14] *WCT-120 Photoconductance Lifetime Tester and optional Suns-Voc User Manual, Sinton Instruments*.

[15] R. A. Sinton, A. Cuevas, and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," in *Photovoltaic Specialists Conference, 1996., Conference Record of the Twenty Fifth IEEE*, 1996, pp. 457-460.

[16] M. J. Kerr, A. Cuevas, and R. A. Sinton, "Generalized analysis of quasi-steady-state and transient decay open circuit voltage measurements," *Journal of applied physics,* vol. 91, pp. 399-404, 2002.

[17] F. Wenner, "A Method of Measuring Earth Resistivity,," *Bulletin of the Bureau of Standards* vol. 12, pp. 469–478, 1915.

[18] L. B. Valdes, "Resistivity Measurements on Germanium for Transistors, ," in *Proc. IRE*, Feb. 1954, pp. 420–427.

[19] W. S. in, A. Goetzberger, and R. M. Scarlett, *"Research and Investigation of Inverse Epitaxial UHF Power Transistors,"*. Wright-Patterson Air Force Base, OH: Air Force Avionics Lab., Sept. 1964.

[20] "Black silicon: fabrication methods, properties and solar energy applications," *Energy Environ. Sci.,* vol. 7, p. 3223, 2014.

[21] "Hybrid gold/porous silicon thin films for plasmonic solar cells," *Scripta Materialia,* vol. 74, p. 33, 2014.

[22] C. Schmiga, H. Nagel, and J. Schmidt, "19% efficientn-type Czochralski silicon solar cells with screen-printed aluminium-alloyed rear emitter," *Progress in Photovoltaics: Research and Applications,* vol. 14, pp. 533-539, 2006.

[23] *en.wikipedia.org/wiki/Screen_printing.*

[24] W. I. Son, Y. J. Sim, C. H. Paik, and M. K. Kim, "Glass frit, and conductive paste composition and solar cell comprising the same," ed: Google Patents, 2015.

[25] M. S. Kim and S. Y. Heo, "Silver paste composition and solar cell using the same," ed: Google Patents, 2012.

[26] M. Wolf and H. Rauschenbach, "Series resistance effects on solar cell measurements," *Advanced Energy Conversion,* vol. 3, pp. 455-479, 1963/04/01/ 1963.

[27] L. Frisson, P. Lauwers, R. Mertens, R. Van Overstraeten, and R. Govaerts, "Screen Printed Metallization of Silicon Solar Cells," *ElectroComponent Science and Technology,* vol. 7, 1980.

[28] K. Firor and S. Hogan, "Effects of processing parameters on thick film inks used for solar cell front metallization," *Solar Cells,* vol. 5, pp. 87-100, 1981/12/01/ 1981.

[29] G. C. Cheek, R. P. Mertens, R. Van Overstraeten, and L. Frisson, "Thick-film metallization for solar cell applications," *IEEE Transactions on Electron Devices,* vol. 31, pp. 602-609, 1984.

[30] A. Cuevas and M. Balbuena, "Thick-emitter silicon solar cells," in *Photovoltaic Specialists Conference, 1988., Conference Record of the Twentieth IEEE*, 1988, pp. 429-434.

[31] J. Nijs, E. Demesmaeker, J. Szlufcik, J. Poortmans, L. Frisson, K. De Clercq*, et al.*, "Latest efficiency results with the screenprinting technology and comparison with the buried contact structure," in *Photovoltaic Energy Conversion, 1994., Conference Record of the Twenty Fourth. IEEE Photovoltaic Specialists Conference-1994, 1994 IEEE First World Conference on*, 1994, pp. 1242-1249.

[32] A. Rohatgi, D. S. Kim, K. Nakayashiki, V. Yelundur, and B. Rounsaville, "High-efficiency solar cells on edge-defined film-fed grown (18.2%) and string ribbon (17.8%) silicon by rapid thermal processing," *Applied Physics Letters,* vol. 84, pp. 145-147, 2004.

[33] A. Rohatgi, Z. Chen, P. Doshi, T. Pham, and D. Ruby, "High-efficiency silicon solar cells by rapid thermal processing," *Applied Physics Letters,* vol. 65, pp. 2087-2089, 1994.

[34] S. Narasimha, A. Rohatgi, and A. Weeber, "An optimized rapid aluminum back surface field technique for silicon solar cells," *IEEE Transactions on Electron Devices,* vol. 46, pp. 1363-1370, 1999.

[35] P. Doshi, A. Rohatgi, M. Ropp, Z. Chen, D. Ruby, and D. L. Meier, "Rapid thermal processing of high-efficiency silicon solar cells with controlled in-situ annealing," *Solar Energy Materials and Solar Cells,* vol. 41, pp. 31-39, 1996/06/01/ 1996.

[36] A. Rohatgi, S. Narasimha, A. U. Ebong, and P. Doshi, "Understanding and implementation of rapid thermal technologies for high-efficiency silicon solar cells," *IEEE Transactions on Electron Devices,* vol. 46, pp. 1970-1977, 1999.

[37] B. Hartiti, A. Slaoui, J. C. Muller, R. Stuck, and P. Siffert, "Phosphorus diffusion into silicon from a spin-on source using rapid thermal processing," *Journal of Applied Physics,* vol. 71, pp. 5474-5478, 1992.

[38] L. Cai, A. Rohatgi, D. Yang, and M. A. El-Sayed, "Effects of rapid thermal anneal on refractive index and hydrogen content of plasma-enhanced chemical vapor deposited silicon nitride films," *Journal of Applied Physics,* vol. 80, pp. 5384-5388, 1996.

[39] P. Doshi, J. Mejia, K. Tate, and A. Rohatgi, "Modeling and characterization of high-efficiency silicon solar cells fabricated by rapid thermal processing, screen printing, and plasma-enhanced chemical vapor deposition," *IEEE Transactions on Electron Devices,* vol. 44, pp. 1417-1424, 1997.

[40] R. J. Martín-Palma, L. Vázquez, J. M. Martínez-Duart, M. Schnell, and S. Schaefer, "Antireflective porous-silicon coatings for multicrystalline solar cells: the effects of chemical etching and rapid thermal processing," *Semiconductor Science and Technology,* vol. 16, p. 657, 2001.

[41] A. Ebong, M. Hillali, and A. Rohatgi, "Rapid photo-assisted forming gas anneal (FGA) for high quality screen-printed contacts for silicon solar cells," in *Photovoltaic Specialists Conference, 2000. Conference Record of the Twenty-Eighth IEEE*, 2000, pp. 264-267.

[42] A. Upadhyaya, A. Ebong, D. S. Kim, V. Yelundur, B. Rounsaville, V. Upadhyaya, *et al.*, "High efficiency mono-crystalline solar cells with simple manufacturable technology," in *21 st European Photovoltaic Solar Energy Conference*, 2006.

[43] M. L. Terry, A. Straub, D. Inns, D. Song, and A. G. Aberle, "Large open-circuit voltage improvement by rapid thermal annealing of evaporated solid-phase-crystallized thin-film silicon solar cells on glass," *Applied Physics Letters,* vol. 86, p. 172108, 2005.

[44] D. M. HuljiC, D. Biro, R. Preu, C. C. Castillo, and R. Ludemann, "Rapid thermal firing of screen printed contacts for large area crystalline silicon solar cells," in *Photovoltaic Specialists Conference, 2000. Conference Record of the Twenty-Eighth IEEE*, 2000, pp. 379-382.

[45] T. Buonassisi, A. A. Istratov, S. Peters, C. Ballif, J. Isenberg, S. Riepe, *et al.*, "Impact of metal silicide precipitate dissolution during rapid thermal processing of multicrystalline silicon solar cells," *Applied Physics Letters,* vol. 87, p. 121918, 2005.

[46] M. D. Pickett and T. Buonassisi, "Iron point defect reduction in multicrystalline silicon solar cells," *Applied Physics Letters,* vol. 92, p. 122103, 2008.

[47] S. Noël, H. Lautenschlager, and J. C. Muller, "Highest efficiency rapid thermal processed multicrystalline silicon solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 9, pp. 41-47, 2001.

[48] V. Meemongkolkiat, M. Hilali, and A. Rohatgi, "Investigation of RTP and Belt fired screen printed Al-BSF on textured and planar back contact surfaces of silicon solar cells," in *3rd World Conference on Photovoltaic Energy Conversion*, 2003, pp. 1467-1470.

[49] J.-W. Jeong, A. Rohatgi, V. Yelundur, A. Ebong, M. D. Rosenblum, and J. P. Kalejs, "Enhanced silicon solar cell performance by rapid thermal firing of screen-printed metals," *IEEE Transactions on Electron Devices,* vol. 48, pp. 2836-2841, 2001.

[50] V. Yelundur, A. Rohatgi, J.-W. Jeong, and J. I. Hanoka, "Improved string ribbon silicon solar cell performance by rapid thermal firing of screen-printed contacts," *IEEE Transactions on Electron Devices,* vol. 49, pp. 1405-1410, 2002.

[51] A. Rohatgi and J.-W. Jeong, "High-efficiency screen-printed silicon ribbon solar cells by effective defect passivation and rapid thermal processing," *Applied Physics Letters,* vol. 82, pp. 224-226, 2003.

[52] J. Schmidt and A. Cuevas, "Progress in understanding and reducing the light degradation of Cz silicon solar cells," 2000.

[53] K. Bothe, R. Sinton, and J. Schmidt, "Fundamental boron-oxygen-related carrier lifetime limit in mono- and multicrystalline silicon," *Progress in Photovoltaics: Research and Applications,* vol. 13, pp. 287-296, 2005.

[54] J. Lagowski, P. Edelman, A. M. Kontkiewicz, O. Milic, W. Henley, M. Dexter, *et al.*, "Iron detection in the part per quadrillion range in silicon using surface photovoltage and photodissociation of iron-boron pairs," *Applied Physics Letters,* vol. 63, pp. 3043-3045, 1993.

[55] H. H. A.A. Istratov, E.R. Weber, "Iron contamination in silicon technology," *Appl. Phys. A* pp. 489-534, 2004.

[56] J. R. Patel, L. R. Testardi, and P. E. Freeland, "Electronic effects on dislocation velocities in heavily doped silicon," *Physical Review B,* vol. 13, pp. 3548-3557, 04/15/ 1976.

[57] T. Saitoh, H. Hashigami, S. Rein, and S. Glunz, "Overview of light degradation research on crystalline silicon solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 8, pp. 537-547, 2000.

[58] F. A. Trumbore, "Solid Solubilities of Impurity Elements in Germanium and Silicon*," *Bell System Technical Journal,* vol. 39, pp. 205-233, 1960.

[59] (2016). Available: http://www.itrpv.net/Reports/

[60] D. L. Meier, H. P. Davis, R. A. Garcia, J. Salami, A. Rohatgi, A. Ebong, *et al.*, "Aluminum alloy back p–n junction dendritic web silicon solar cell," *Solar Energy Materials and Solar Cells,* vol. 65, pp. 621-627, 2001/01/01/ 2001.

[61] A. Ebong, M. Hilali, A. Rohatgi, D. Meier, and D. S. Ruby, "Belt furnace gettering and passivation of n-web silicon for high-efficiency screen-printed front-surface-field solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 9, pp. 327-332, 2001.

[62] R. Kopecek, T. Buck, J. Libal, I. Rover, K. Wambach, L. J. Geerligs*, et al.*, "Large Area Screen Printed N-Type Silicon Solar Cells with Rear Aluminium Emitter: Efficiencies Exceeding 16%," in *2006 IEEE 4th World Conference on Photovoltaic Energy Conference*, 2006, pp. 1044-1047.

[63] C. Schmiga, H. Nagel, and J. Schmidt, "19% efficient n-type Czochralski silicon solar cells with screen-printed aluminium-alloyed rear emitter," *Progress in Photovoltaics: Research and Applications,* vol. 14, pp. 533-539, 2006.

[64] M. R. Christian Schmiga, Marc Rüdiger, Karsten Meyer, Jan Lossen, Hans-Joachim Krokoszinski, Martin Hermle and Stefan W. Glunz, "Aluminium-Doped p+ Silicon for Rear Emitters and Back Surface Fields: Results and Potentials of Industrial n- and p-Type Solar Cells," in *25th European Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photovoltaic Energy Conversion*, Valencia, Spain, 2010.

[65] D. L. Meier, V. Chandrasekaran, H. P. Davis, A. M. Payne, X. Wang, V. Yelundur*, et al.*, "N-Type, Ion-Implanted Silicon Solar Cells and Modules," *IEEE Journal of Photovoltaics,* vol. 1, pp. 123-129, 2011.

[66] R. C. G. N. A.R. Burgers, A.J. Carr1, P.C. Barton, L.J. Geerligs, XiongJingfeng, Li Gaofei, Song Weipeng, An Haijiao, Hu Zhiyan, P.R. Venema, A.H.G. Vlooswijk, "19% EFFICIENT N-TYPE SI SOLAR CELLS MADE IN PILOT PRODUCTION " in *25th European Photovoltaic Solar Energy Conference and Exhibition 5th World Conference on Photovoltaic Energy Conversion* Valencia, Spain, 2010.

[67] F. Book, T. Wiedenmann, G. Schubert, H. Plagwitz, and G. Hahn, "Influence of the Front Surface Passivation Quality on Large Area n-Type Silicon Solar Cells with Al-Alloyed Rear Emitter," *Energy Procedia,* vol. 8, pp. 487-492, 2011/01/01/ 2011.

[68] V. Chandrasekaran, H. P. Davis, A. M. Payne, V. Yelundur, A. Rohatgi, and D. L. Meier, "20% n-Type silicon solar cell fabricated by a simple process with an aluminum alloy rear junction and extended emitter," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, 2016, pp. 2412-2416.

[69] M. Balucani, L. Serenelli, K. Kholostov, P. Nenzi, M. Miliciani, F. Mura*, et al.*, "Aluminum-silicon Interdiffusion in Screen Printed Metal Contacts for Silicon based Solar Cells Applications," *Energy Procedia,* vol. 43, pp. 100-110, 2013.

[70] A. Ebong, N. Chen, V. Unsur, A. Chowdhury, and B. Damiani, "Innovative Front Grid Design, Four-Streets and Five-Busbars (4S-5BB), for High Efficiency Industrial Al-BSF Silicon Solar Cell," *IEEE Electron Device Letters,* vol. 37, pp. 459-462, 2016.

[71] M. Hiroshi, "Radiation energy transducing device," US3278811 A, 1966.

[72] Y. Chevalier and I. Chambouleyron, "Capteur photovoltaique a retroilumination (Bifacial solar cell)," France Patent Patent F 77 24669, 1977.

[73] J. G. Fossum and E. L. Burgess, "High-efficiency p+-n-n+ back-surface-field silicon solar cells," *Applied Physics Letters,* vol. 33, pp. 238-240, 1978.

[74] A. Luque, J. M. Ruiz, A. Cuevas, J. Eguren, and M. G. Agost, "Double sided /D.S./ solar cells to improve static concentration," in *Photovoltaic Solar Energy Conference*, Luxembourg, 1978, pp. 269-277.

[75] A. Cuevas, A. Luque, J. Eguren, and J. del Alamo, "High efficiency bifacial back surface field solar cells," *Solar Cells,* vol. 3, pp. 337-340, July 1, 1981.

[76] K. Jaeger and R. Hezel, "Bifacial MIS inversion layer solar cells based on low temperature silicon surface passivation," in *19th IEEE Photovoltaic Specialists Conference*, Germany, 1987, pp. 388-391.

[77] A. P. Silard and G. Nani, "Design/technological experiments on low cost, BSF-type, bifacial solar cells fabricated on large-area silicon wafers," *Solar Energy Materials,* vol. 17, pp. 73-87, 1988/02/01/ 1988.

[78] A. Ebong, S. Ghozati, M. Taouk, F. Yun, Y. Tang, C. B. Honsberg*, et al.*, "Towards 20% Double Sided Buried Contact Silicon Solar Cells," in *32nd Annual Conf., International Solar Energy Society (ANZ Section)*, Sydney, Australia, 1994, pp. 247-252.

[79] A. Moehlecke and A. Luque, "New approach to obtain boron selective emitters [for Si solar cells]," in *Proceedings of 1994 IEEE 1st World Conference on Photovoltaic Energy Conversion - WCPEC (A Joint Conference of PVSC, PVSEC and PSEC)*, 1994, pp. 1492-1495 vol.2.

[80] S. W. Glunz, J. Knobloch, D. Biro, and W. Wettling, "OPTIMIZED HIGH-EFFICIENCY SILICON SOLAR CELLS WITH JSC= 42 mA/cm2 AND η= 23.3%," in *14th European Photovoltaic Solar Energy Conference*, Barcelona, Spain, 1997, pp. 392 -395

[81] C. Z. Zhou, P. J. Verlinden, R. A. Crane, R. M. Swanson, and R. A. Sinton, "21.9% efficient silicon bifacial solar cells," in *Conference Record of the Twenty Sixth IEEE Photovoltaic Specialists Conference - 1997*, 1997, pp. 287-290.

[82] H. Ohtsuka, M. Sakamoto, K. Tsutsui, and Y. Yazawa, "Bifacial silicon solar cells with 21·3% front efficiency and 19·8% rear efficiency," *Progress in Photovoltaics: Research and Applications,* vol. 8, pp. 385-390, 2000.

[83] A. Hübner, A. G. Aberle, and R. Hezel, "20% Efficient Bifacial Silicon Solar Cells," in *14th European Photovoltaic Solar Energy Conference*, Munich, Germany, 2001, pp. 1796-1798.

[84] G. Jiun-Hua and J. E. Cotter, "Laser-grooved backside contact solar cells with 680-mV open-circuit voltage," *IEEE Transactions on Electron Devices,* vol. 51, pp. 2186-2192, 2004.

[85] V. D. Mihailetchi, J. Jourdan, A. Edler, R. Kopecek, R. Harney, D. Stichtenoth*, et al.*, "Screen Printed n-Type Silicon Solar Cells for Industrial Application," in *25th European Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photovoltaic Energy Conversion*, Valencia, Spain, 2010, pp. 1446 - 1448.

[86] D. Suwito, U. Jager, J. Benick, S. Janz, M. Hermle, and S. W. Glunz, "Industrially Feasible Rear Passivation and Contacting Scheme for High-Efficiency n-Type Solar Cells Yielding a Voc of 700 mV," *IEEE Transactions on Electron Devices,* vol. 57, pp. 2032-2036, 2010.

[87] L. Yang, Q. H. Ye, A. Ebong, W. T. Song, G. J. Zhang, J. X. Wang*, et al.*, "High efficiency screen printed bifacial solar cells on monocrystalline CZ silicon," *Progress in Photovoltaics: Research and Applications,* vol. 19, pp. 275-279, 2011.

[88] T. Dullweber, C. Kranz, R. Peibst, U. Baumann, H. Hannebauer, A. Fülle*, et al.*, "PERC+: industrial PERC solar cells with rear Al grid enabling bifaciality and reduced Al paste consumption," *Progress in Photovoltaics: Research and Applications,* vol. 24, pp. 1487-1498, 2016.

[89] F. Kiefer, J. Krügener, F. Heinemeyer, M. Jestremski, H. J. Osten, R. Brendel*, et al.*, "Bifacial, fully screen-printed n-PERT solar cells with BF2 and B implanted emitters," *Solar Energy Materials and Solar Cells,* vol. 157, pp. 326-330, 2016/12/01/ 2016.

[90] T. Dullweber, N. Wehmeier, A. Nowack, T. Brendemühl, S. Kajari-Schröder, and R. Brendel. *BiCoRE: Combining a PERC-type cell process with n-type wafers*. Available: https://www.pv-tech.org/technical-papers/bicore-combining-a-perc-type-cell-process-with-n-type-wafers

[91] Available: http://isc-konstanz.de/en/isc/news/news/article/our-contribution-to-co2-reduction-21-bison-at-megacell/ibc.html?tx_ttnews%5BbackPid%5D=5&cHash=99ce1f69bb2158dc3ee9029c03e32823

[92] (2017). *Trina Solar Press Release*. Available: http://www.trinasolar.com/en-uk/resources/newsroom/mon-05012017-1500

[93] (2017). *Imec Press Release*. Available: https://www.imec-int.com/en/articles/imec-develops-bifacial-n-pert-solar-cell-with-a-record-22-8-percent-front-side-efficiency

[94] S. W. Glunz, F. Feldmann, A. Richter, M. Bivour, C. Reichel, H. Steinkemper*, et al.*, "The Irresistible Charm of a Simple Current Flow Pattern – 25% with a Solar Cell Featuring a

Full-Area Back Contact," in *31st European Photovoltaic Solar Energy Conference and Exhibition*, Hamburg, Germany, 2015, pp. 259-263.

[95] D. L. Meier and D. K. Schroder, "Contact resistance: Its measurement and relative importance to power loss in a solar cell," *IEEE transactions on electron devices,* vol. 31, pp. 647-653, 1984.

[96] H. Huang, J. Lv, Y. Bao, R. Xuan, S. Sun, S. Sneck*, et al.*, "Data of ALD Al(2)O(3) rear surface passivation, Al(2)O(3) PERC cell performance, and cell efficiency loss mechanisms of Al(2)O(3) PERC cell," *Data in Brief,* vol. 11, pp. 19-26, 12/21

APPENDIX A: SCREEN-PRINTING METALLIZATION PROCEDURE

Screen-printing metallization procedure consists of five basic operations; a) Wafer Alignment, b) Screen Alignment, c) Squeege placement, d) Checking print pressure and snap off, and e) Printing cycle, While operating these procedures extreme care was taken to ensure screen does not break due to its fragile characteristics. Another important aspect before start the priniting is to make sure previously used screen is well cleaned. Typically, after the printing there is high chance exists of blocking the screen by Ag paste. Specially, for fine line opening ~50 μm the probability of blocking is even higher. Therefore, screen prior to prinitng was cleaned well with Iso propyl alcohol. Step by step printing procesure is described in following,

Step 01: Wafer Alignment

Wafer alignment is key for a good prinited cell. Wafer was first placed to the wafer holding stage as shown in Fig. It is important to put the wafer in between these knobs such that wafer has enough place to move if require after first printing. Usually, first printing gives a indication of alignment, thereby after finding the optimum alignment, electric tapes were used trace the correct position of wafer for the next printing. During printing vaccum was turned on which holds the wafer on the stage.

Step 02: Screen Alignment

The screen alignment is critical to avoid shunting effect during the printing and cofiring process. An unalighned screen is more prope towards the edge shunting primarily caused by rear Al. Hence, to maintain a good alignment first off, snap off was reduced to 0.3 mm which is very close to the wafer thickness ~180 μm. This reduced the distance between wafer top edge and screen edge. A better resolion at the edge helped to observe the minimum distance from the wafer edge to the screen edge. For both front and rear printing, screen alignment needs to be followed prior to start the printing. To make sure screen was attached, the was turned on acordingly. Another important observation during screen placement is to make sure that screen gridlines are perpendicular to the squeegee poistion. Thus, busbars are parallel to the squeegee and gridlines are perpendicular during the printing cycle. The setup of screen is shown in Fig. A1.

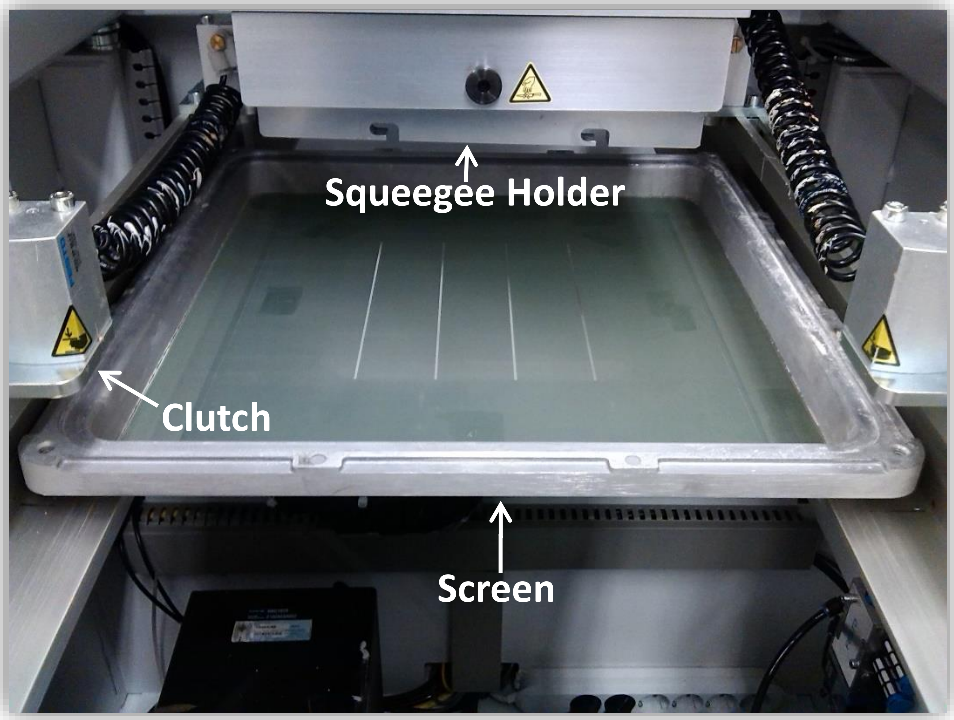


Fig. A1. Screen prior to the alignment

Step 03: Squeegee placement

There are two squeegees that were utilized during the printing. Fist one is the rubber squeege which was attached at the back (or closer to the front edge) and the other one is flat squeegee which is placed at the front (or closer to the rear edge). The rubber squeegeee was attached with a certain angle ~45^o to allow an optimum pressure. The flat squeegee were attached parallelly from the screen. It is important to make the the flat squeegee as much as parallel as possible which confirms uniform spreading of pastes during the printing. The squeegee used for rear full Al and front Ag printing is shown in Fig. A2.

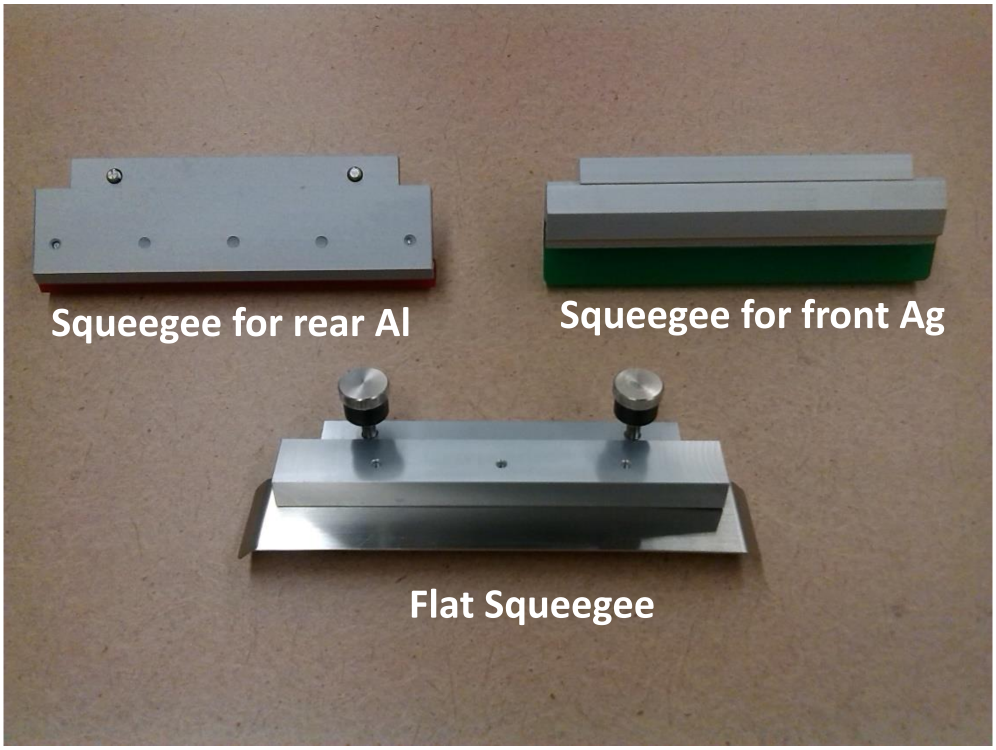


Fig. A2. Different squeegee used for the screen-priniter

Step 04: Check the print pressure and snapoff

After placing the squeegees, print pressure was observed by the assistance of two white papers. The reason for using two A4 size white papers is to mimicing the wafer thickness of 180 µm. The rubber squeege snap off and pressure was checked by placing these two papers and then pulling the two papers once squeegee was down. If the two papers were too tight, then it indicates pressure and snap off are not favorable since it has high risk of breaking the screen. Hence, a moderate pressure was maintained when two papers were pulled such that this is not neither too tight nor too loose. A loose paper pull is the indication of either snap off is too high or pressure is too low. Therefore, an optimum print pressure and snap off was achieved following the optimization. In our experiments we mostly used print pressure of ~1.6 bar/N and snap off ~0.7 mm. As mentioned, this might vary depending on the wafer thickness and rear Al thickness.

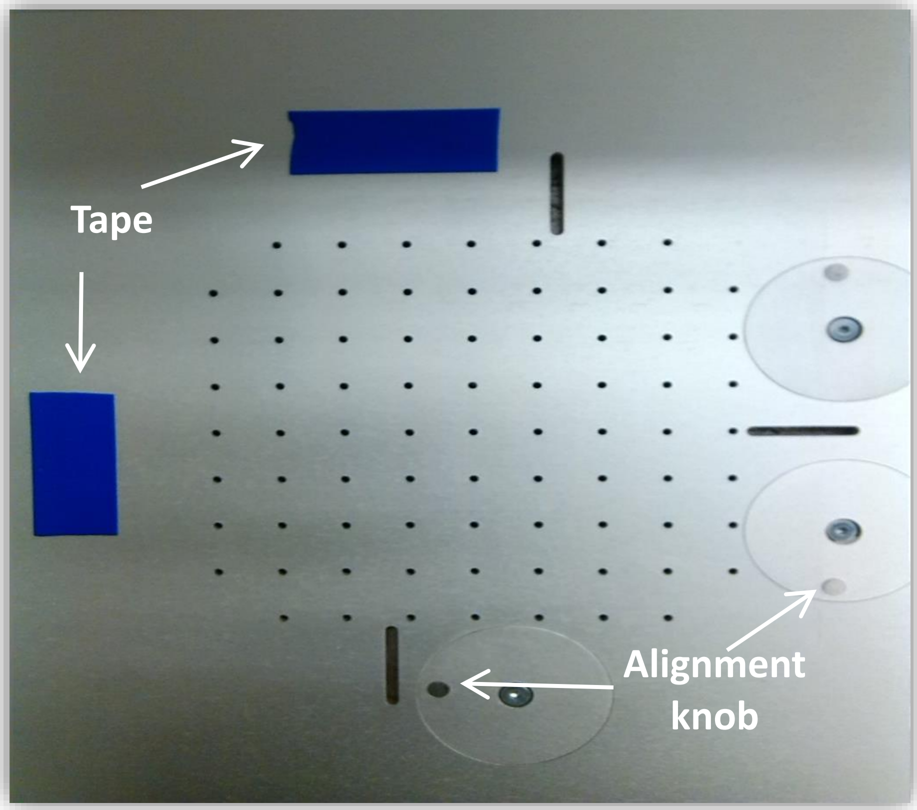


Fig. A3. Top view of Wafer holder stage

Step 05: Printing Cycle

Once, the print pressure and snap off is set up, the wafers are now ready for printing. The pastes are put uniformly towards the front edge in vicinity of rubber squeegee. It needs to make sure that, pastes are put with a little bit distance from the screen edge so that paste does not block printing area. After placing the paste, printing cycle is initiated. At this point basic position, In one printing cycle, rubber squeege a) comes down b) pushes paste through the screen, c) and approaches comes towards the reat edge and d) then rubber squeege comes up.

Then, the flat squeege a) goes down, b) uniformly spreads the paste at the entire screen area , c) approaches from the rear edge to front edge and d) finally comes up. Both squeeges are now in the top position and ready for the next printing. Wafers holder stage is then placed to the basic position. Then vaccum is turned off and twizer was used to hold the wafer and then placing in the dryer. It is important to note that, if there is any misalignment observed following the first printing, then alignment needs to be adjusted again for the upcoming printing cycles.

APPENDIX B: CONTACT RESISTANCE MEASUREMENT

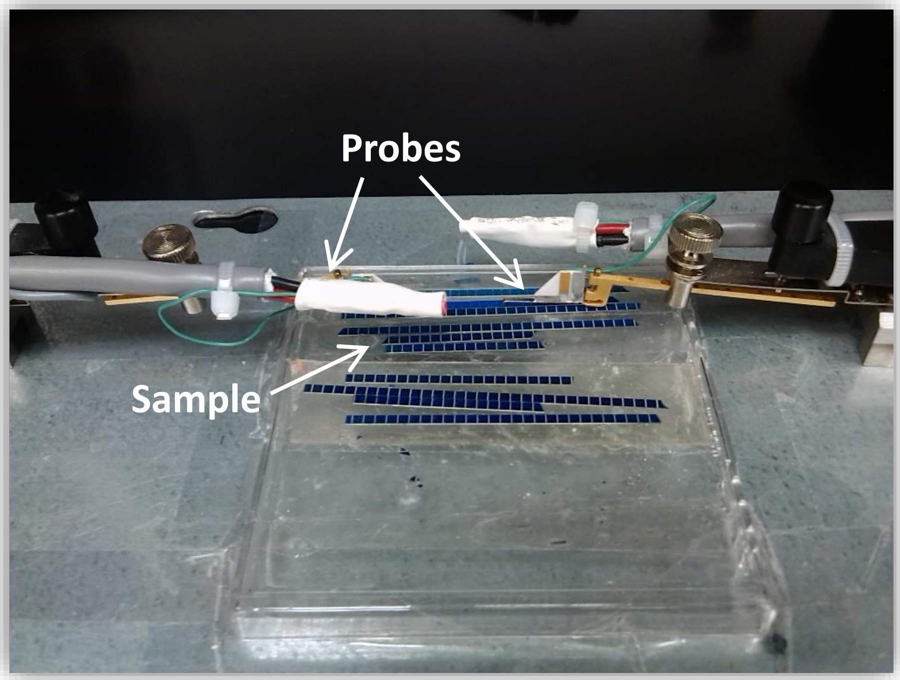


Fig.B1. Contact resistance probe with sample.

The 4-point probe for the contact resistanc measurment was built up in the laboratory. A kehtley current source was employed to provice current for this measurement. The 4 probes measuring the 2mm samples are shown in Fig.B1. When current is supplied, corresponding voltage is measure in following procedure,

B.1. Setting up Input parameters

An excel sheet was created to setup the input parameters. In input parameters, line spacing was setup. The live spacing either analytically calculated or a high resolution camera was used to observe the distance between two adjacent gridlines. Additionally, width of the sample was setup which is 2 mm.

B.2.2. Measuring the Output parameters

a) Under the source section, current was pressed.

b) Current was setup ±20 μA by using the arrow sign. Then enter was pressed

c) Under the measure section, voltage was selected.

d) then output was selected to measure the corresponding voltage.

e) For every measurment voltage was recorded for both directions of currents.

f) Then these voltage measurements were used via excel sheet to calculate contact and sheet resistance.

PUBLICATIONS

JOURNAL PUBLICATIONS

1. **A. A. Chowdhury**, V. Unsur and A. Ebong, “Simulation of Cost Effective High Efficiency Front Surface Field (FSF) Silicon Solar Cell”, *IEEE Journal of Photovoltaics*, August 2017, (submitted).

2. **A. A. Chowdhury**, V. Unsur and A. Ebong, “Exploring the Potentials of a Front Surface Field (FSF) Industrial Silicon Solar Cell”, *Solar Energy Materials and Solar Cells*, August 2017. (submitted).

3. A. Ebong, N. Chen, V. Unsur, **A. A. Chowdhury**, and B. Damiani, “Innovative Front Grid Design, Four- Streets and Five-Busbars (4S-5BB), for High Efficiency Industrial Al-BSF Silicon Solar Cell”, *IEEE Electron Device Letters*, Vol. 37-4, April 2016.

4. V. Unsur, Y. Hsu, **A.A. Chowdhury** and A. Ebong, “Stabilization of Minority Carrier Lifetime in PERC Structured Silicon Solar Cell”, *IEEE Journal of Photovoltaics*, 2017 (submitted).

5. **A. A. Chowdhury**, V. Unsur and A. Ebong, “Loss Analysis of Cost Effective High Efficiency Bifacial Solar Cell”, *IEEE Journal of Photovoltaics*. (To be submitted.)

CONFERENCE PUBLICATIONS

6. A. Ebong, **A.A. Chowdhury** and V. Unsur, “The Impact of Nano Ag particles in the Contact Formation of a Silicon Solar Cell”, *5th Nano Today Conference*, Hawaii, December 2017.

7. A. Ebong, V. Unsur, N. Bezawada and **A.A. Chowdhury**, “Investigation of Tellurite based Ag pastes for Fire-Through Dielectric Contacts (FTDC) Solar Cells with Lightly Doped Emitter”, *7th Workshop on Metallization & Interconnection for Crystalline Silicon Solar Cells*, Konstanz, Germany, 2017.

8. **A. A. Chowdhury**, Y. Hsu, V. Unsur and A. Ebong, “Exploiting the Potentials of the Front Surface Field (FSF) Industrial Silicon Solar Cell”, 43rd IEEE Photovoltaic Specialists Conference, Washington, DC, 2017.

9. V. Unsur, **A. A. Chowdhury**, N. Chen and A. Ebong, “The Effects of Nano Ag Particles on Gridline Sintering for Silicon Solar Cells”, *42nd IEEE Photovoltaic Specialists Conference*, New Orleans, June 2015.

10. **A. A. Chowdhury** and A. Ebong, “A Simulation Model for Optimizing the Performance of Bifacial Si Solar Cells.” *12th International Conference on High-capacity Optical Networks and Enabling/Emerging Technologies (HONET)*, 2015.

11. A. Ebong, N. Chen, V. Unsur, **A. A. Chowdhury**, “Understanding the Impact of Rapid Thermal Processing (RTP) on the Light Induced Degradation (LID) of Mono and Multi Crystalline Silicon Solar Cells.” *31st European Photovoltaic Solar Energy Conference (EUPVSEC)*, October 2015.

12. A. Ebong, N. Chen, V. Unsur, **A.A. Chowdhury**, "The Impact of Rapid Thermal Processing (RTP) on Crystalline Silicon Solar Cell Performance and Light Induced Degradation (LID)", *42nd IEEE Photovoltaic Specialists Conference (PVSC)*, June 2015. **(Best poster award nominee)**

13. A. Ebong, V. Unsur, N. Chen, **A. A. Chowdhury**, "Understanding the Sintering of Digital Inkjet Printed (DIP) Contacts to Achieve Low-contact Resistance on Silicon Solar Cells", *1st Africa Photovoltaic Solar Energy Conference*, March 2014.

14. N. Chen, **A. A. Chowdhury**, A. Ebong, "Comprehensive Empirical Model for Evaluation of the Series Resistance of a Solar Cell", *IEEE 11th International Conference on High Capacity Optical Networks and Enabling Technologies (HONET)*, December 2014.

15. N. Chen, **A. A. Chowdhury**, V. Unsur, A. Ebong, "Assessing the Impact of Multi-Busbars on Metallization Cost and Efficiency of Solar Cells with Digital Inkjet-Printed Gridlines", *IEEE 10th International Conference on High Capacity Optical Networks and Enabling Technologies (HONET)*, December 2013.

16. N. Chen, **A. A. Chowdhury**, V. Unsur and A. Ebong," Comprehensive Assessment of the p-n Junction Formation Technologies for Solar Cell Emitter Uniformity, Contact Formation and Performance", *6th World Conference on Photovoltaic Energy Conversion*, November 2014.