ANALYSIS, DESIGN AND EXPERIMENTAL VERIFICATION OF A NOVEL AC-AC BUCK BOOST BASED DYNAMIC VOLTAGE REGULATOR

by

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ABSTRACT

NAKUL SHAH. Analysis, design and experimental verification of a novel ac-ac buck boost based dynamic voltage regulator. (Under the direction of DR. MADHAV MANJREKAR)

This thesis investigates a unique direct ac-ac converter based topology that can be used to shield the load from any disturbance occurring in the grid voltage. The proposed converter topology uses disturbed source itself to synthesize required series compensation voltage to restore the load voltage to its pre-defined amplitude and shape. Termed AC Dynamic Voltage Regulator, offers advantages of smaller size, superior effectiveness and absence of DC storage systems over conventional Dynamic Voltage Regulators. Moreover, because of its unique system architecture and control strategy, AC-DVR offers instantaneous sinusoidal power extraction from the grid, irrespective of any disturbance that is introduced in the grid voltage. The proposed topology, overall system architecture, operating principle and control are discussed thoroughly in this article. The behavior of AC-DVR is evaluated against various grid voltage disturbances such as voltage sag, voltage swell, harmonics etc. and results are documented for each disturbance. Simulation results are presented for various disturbance scenarios to prove the efficacy of the proposed methodology. It is shown that the proposed AC-DVR is capable of shielding load from almost any kind of disturbance that is occurring in grid voltage. Experimental results demonstrating the AC-AC Dynamic Voltage Regulation are also presented in this article. A possible modification that can be made for proposed topology is also offered and discussed. Simulation results supporting the behavior of proposed modification against similar voltage disturbances are also discussed and documented.

DEDICATION

This thesis is dedicated to my parents, Indravadan Shah and Vibha Shah, my sister, Hemangi Shah and my grandparents, Ratilal Shah and Kanta Shah.

ACKNOWLEDGEMENTS

First, I would like to express my gratitude towards my parents, my sister, my grandmother and entire Shah family for believing in me and making it possible for me to follow my dream of pursuing higher education.

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LIST OF ABBREVIATIONS

s	second
ns	nanosecond
μs	microseconds
ms	millisecond
kHz	kilohertz
MHz	megahertz
min	minute
pu	per unit
ESD	electrostatic discharge
EMI	electromagnetic interference
RFI	radio frequency interference
AC	alternating current
DC	direct current
PWM	pulse width modulation
IGBT	insulated gate bipolar transistor
MOSFET	metal oxide semiconductor field effect transistor
kVA	kilo volt ampere
PCC	point of common coupling

CHAPTER 1: INTRODUCTION

1.1 Introduction

With increase in power demand from various industries and the non-linear nature of industrial load, utility companies and customers are becoming more concerned about the quality of electrical power [1]. The word Power Quality is becoming a frequent topic for discussion and research and has gained a considerable amount of attention over the past few decades. This chapter presents a brief overview of power quality and its significance. The concluding sections of this chapter provides a brief introduction of this article and overall thesis organization.

1.2 Power Quality

The definition of power quality is quite subjective. It varies from one perspective to another [2]. Utility companies providing electrical power may define it as reliability. While, a load manufacturer may define it as a quality of power under which their equipment will perform properly. This definition also changes with change in load manufacturers. On the other hand, consumer may define it as reliability and their flexibility with the utility companies. Figure 1.1 shows results of a survey conducted by Georgia Power Co on the causes of power quality problems. It clearly indicates that apart from natural problems, most consumers blame utility for their power issues. However, from utility side, there may not be any issue in their service at customer end. So, it is completely possible that the cause of power problem originated at customer end only.

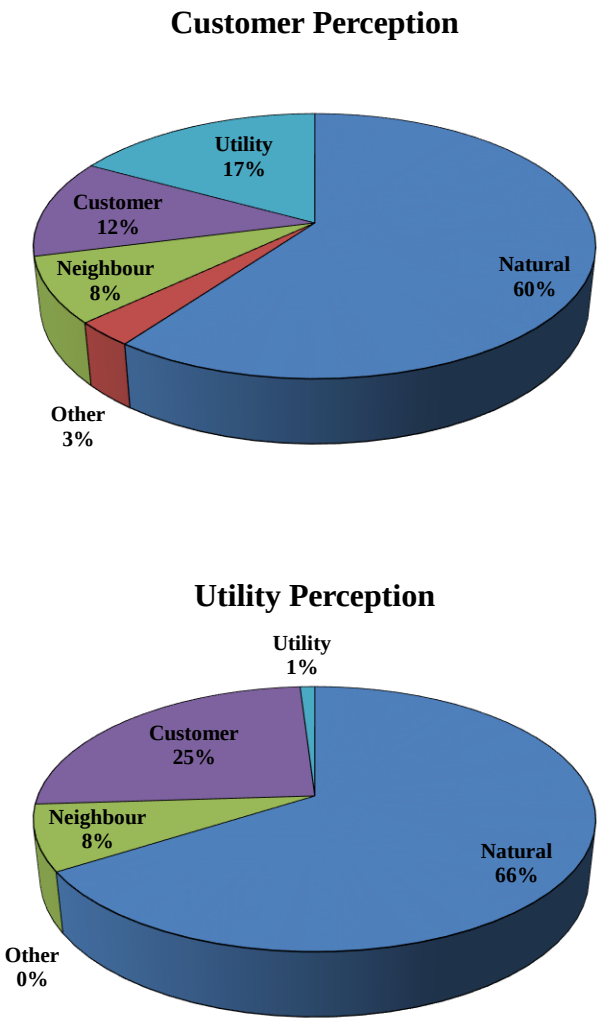


Figure 1.1: Results of a survey conducted by Georgia Power Co on the causes of power quality problems [2]

Hence, power quality may be defined as “Degree to which both the utilization and delivery of electric power affects the performance of electrical equipment [3].” or “Any power problem manifested in voltage, current or frequency deviations that results in failure or disoperation of customer equipment [2].” or “The electrical network's or the grid's ability to supply a clean and stable power supply. In other words, power quality ideally creates a perfect power supply that is always available, has a pure noise-free sinusoidal wave shape, and is always within voltage and frequency tolerances [4].”

1.3 Voltage Quality as Power Quality

Power is basically flow of energy defined by a product of voltage and current. The current drawn by load is highly dependent on the type of load which is connected to a defined voltage source and is highly uncontrollable. Any type of variation or disturbance in voltage can affect the quality of power. Where for most linear loads the shape of current is dependent on the shape of voltage, for non-linear loads it isn't true. For example, the current shape of a voltage source type harmonic load contains harmonics and is not sinusoidal resulting injection of voltage harmonics on grid side causing grid voltage to distort [5]. While for current harmonic source type load's current is also not sinusoidal but it doesn't distort the voltage but it contains current harmonics which results into poor power quality [5]. In addition to that, short circuit currents and currents caused by lightning strokes also cause voltage interruption [2]. Thus, it can be said that most power quality issues can be the result of poor voltage quality, but the involvement of the current should also be taken account for. So, power quality is dependent on both voltage and current but in the end voltage takes precedence. Hence, power quality can be realized as quality of voltage than quality of current or power itself. However, effect of current on voltage and power quality is addressed later in this chapter.

1.4 Significance of Power Quality

Manufacturing industries are adopting automation in their plants to be more effective and efficient that result in using power electronic devises, digital controllers and solid state devises etc. which are more sensitive to power disturbances. Any minor disturbance or interruption in voltage can cause a major loss in terms of money and time. For instance, a voltage sag in a paper mill can waste a whole day of production causing

the loss of $250,000 according to Business Week (June 17, 1996). Similarly, according to New York Times (January 2000) a manufacturing company lost more than $3 million in one day in Silicon Valley when lights went out.

Moreover, the utilities are getting deregulated and it is being more difficult to survive in competitive business world. As discussed in section 1.1, consumers blame utility companies for most power quality issues apart from natural causes. Thus, satisfying customer needs and maintaining their confidence in them are becoming more important factors for utilities as losing a valuable customer to other utility provider can cause a significant financial loss.

Power quality problems do not have any major impact on residential customers in terms of financial losses. However, world is becoming more digitized, and a major part of residential customers are a part of it. Many of them are working from home on their computers, business transactions are getting more online, and dependency on technology is increasing rapidly. According to Contingency Planning Research, LAN Times, half of computer problems and one-third data loss can be tracked back to power line. Thus, power quality disturbances, can affect residential customers in terms of data loss and waste of time.

Summing all this, USA is lost $50 billion per year due to power quality breakdown according to Bank of America report and the annual cost of power interruption is estimated to be $80 billion by Berkeley Lab on February 2, 2005.

To maintain a decent quality of power throughout, different standards are made such as IEEE 519-1992, IEEE 1159-1995, IEEE 1250-1995, IEEE 1100-1999, IEEE 242, IEEE 1336-2012, IEEE/ANSI C62.45, IEEE/ANSI C57.110, IEC 61000-2-2, IE C61000-

2-4, IEC 61000-3-2, IEC 61000-4-15 and EN 50160 [7,9] and imposed on the customers and manufacturers. To maintain these standards and guidelines and provide good power quality, need of mitigation techniques for different disturbances arise.

1.5 Thesis Motivation

Direct AC-AC converters are gaining attention of researchers due to their lower cost and higher system reliability. Most of the power quality devices employed in utility grids uses indirect AC-AC conversion systems. An indirect AC-AC conversion system uses several power stages such as AC power is converted into DC power by AC-DC conversion systems and then DC power is in turn converted back to AC power by using DC-AC converter systems. The intermediate stage of AC-DC-AC power conversion system requires some intermediate energy storage systems such as capacitors. These capacitors can be bulky in size and come with a disadvantage of high unreliability. Although, indirect AC-AC power conversion systems offer advantages of competitive cost and ease of control, their disadvantages outweigh their advantages. On the other hand, direct AC-AC power conversion systems provides advantages of single stage power conversion, better efficiency, smaller size and lack of intermediate energy storage systems. Multiple direct AC-AC power conversion systems are available in the literature. However, which methodology should be chosen or weather to come up with any novel topology or not remains a major challenge. Despite these challenges associated with control complexity of AC-AC conversion and power circuit minimization, the motive of this thesis is to investigate a unique direct AC-AC conversion system for Dynamic Voltage Regulation where power conversion happens in one stage unlike conventional dynamic voltage regulation systems which uses indirect ac-ac conversion systems.

1.6 Organization of Thesis

This section presents an overview of the organization of the thesis as follows:

Chapter 1: Introduction

This chapter starts by describing relative definition of power quality in Section 1.2. The role of voltage quality in power quality is briefly discussed in Section 1.3. Section 1.4 stresses the importance of power quality leading to thesis motivation in Section 1.5. The organization of the thesis is presented in Section 1.6.

Chapter 2: Power Quality Issues and Mitigation Techniques

This chapter presents various power quality problems, their possible causes, effects and mitigation techniques. A brief overview of the chapter is presented in Section 2.1. Various power quality problems are discussed in Section 2.2 along with their typical spectrum, typical time duration, typical voltage magnitude, possible causes and possible effects. Section 2.3 stresses the importance of power quality problems leading to their mitigation techniques in Section 2.4.

Chapter 3: Buck Boost Based Direct AC-AC Dynamic Voltage Regulator

In this chapter, a novel topology of AC-AC converter for Dynamic Voltage Regulation is presented. A brief overview of state of the art AC-AC buck boost converter and microinverter is presented in Section 3.2 and 3.3 respectively. Section 3.4 describes detailed circuit schematic and overall system architecture of proposed AC-AC Dynamic Voltage Regulator (AC-DVR). The operating principle of AC-DVR is discussed in Section 3.5.

Chapter 4: Analysis and Design of AC-AC Dynamic Voltage Regulator

This chapter presents the analysis of proposed AC-AC Dynamic Voltage Regulator along with inductor and capacitor design. The duty cycle derivation is presented in Section 4.2. Section 4.3 and Section 4.4 discusses the design of inductor and capacitor based on power calculations. Overall control architecture of proposed AC-AC Dynamic Voltage Regulator is explained in Section 4.5.

Chapter 5: Modelling of Direct AC-AC Dynamic Voltage Regulator

This chapter presents the modelling of AC-AC Dynamic Voltage Regulator. Matlab Simulink model of overall system architecture is presented and discussed in Section 5.2. Simulation model of unprotected source, AC-AC Dynamic Voltage Regulator, load and transformer are explained in Section 5.3, Section 5.4, Section 5.5 and Section 5.6 respectively.

Chapter 6: Simulation Results

This chapter presents the simulation results verifying the efficacy of the AC-AC Dynamic Voltage Regulator. An introduction to the chapter and Simulation Parameters are presented in Section 6.1 and Section 6.2 respectively. The simulation results verifying the operating principle of AC-DVR under various voltage disturbances are discussed and presented in Section 6.3.

Chapter 7: Experimental Results

This chapter explains experimental results obtained from laboratory prototype under similar disturbances discussed for simulations. The objective of the chapter is described in Section 7.1. The laboratory setup and control architecture in OPAL-RT are discussed and presented in Section 7.2. Experimental results verifying the practical realization of AC-DVR are presented in Section 7.3.

Chapter 8: Conclusion and Future Work

This chapter discussed the conclusion drawn from the simulation and experimental results presented in Chapter 6 and Chapter 7 respectively. It also contains a summary of overall thesis and recommendations for future work.

Appendix A: Modification in Proposed AC-DVR

A possible modification in previously discussed AC-AC Dynamic Voltage Regulator is proposed in this chapter. Overall circuit schematic of proposed modification and operating principle are discussed in Section A.2. Simulation results verifying the efficacy of proposed modification under similar disturbances discussed in Chapter 6 are presented and discussed in Section A.3.

CHAPTER 2: POWER QUALITY ISSUES AND MITIGATION TECHNIQUES

2.1 Introduction

Providing a reliable supply of power which is disturbance free and within pre-defined limits is one of the most important requirements of any electrical system. However, with increase in power demand [1] from various industries, these loads often introduce disturbances into power grid which causes the grid to deviate from its pre-defined standards. There are different solutions available in literature depending on the type of disturbance. This chapter presents a brief review of various power quality issues and their solution methodologies.

2.2 Power Quality Issues

There are various types of power quality problems in the power world and they affect the quality of power differently. To determine the cause of the disturbance and apply its mitigation technique, classification and generalization of these disturbances are necessary. International Electro-Technical Commission classifies these disturbances in six groups: (I) Conducted low-frequency phenomena, (II) Radiated low-frequency phenomena, (III) Conducted high-frequency phenomena, (IV) Radiated high-frequency phenomena, (V) Electrostatic discharge phenomena and (VI) Nuclear electromagnetic phenomena. Among these groups, conducted and radiated phenomena have major impact on the power quality issues and thus this article will be more focused on these groups. Table 2.1 shows the different categories of power system electromagnetic phenomena

along with typical spectral content, duration and voltage magnitude [6]. This categorization falls into the first four groups of the classification. The definition of different electromagnetic disturbances can be easily realized using information provided in Table 2.1 and proper attributes. For steady state phenomena amplitude, frequency, spectrum, modulation, source impedance, notch depth and notch area can be used and for non-steady state phenomena rate of rise, amplitude, duration, spectrum, frequency, rate of occurrence, energy potential and source impedance can be utilized.

These disturbances can be caused by natural events such as lightening, weather conditions, faults etc. or man-made events such as non-linear loads and system operations [7]. Natural causes mainly result in non-steady state type of disturbances while non-steady state and steady state both disturbances can be caused by man-made events. The primary effects of these problems are equipment failure/reduced life, system halts, loss of important data, flickering and system shutdown. Table 2.2 provides information regarding the causes and effects of different power quality issues along with their wave shape for better understanding of this topic [6-8]. These power quality problems can be defined using the information provided in Table 2.1. For instance, temporary voltage sag can be identified if the magnitude of measured voltage is greater than 0.1 pu but less than 1 pu and it is sustained for 3s-1min. However, if it is sustained for greater than 1min, it can be identified as undervoltage. Due to the importance of power quality as discussed in section 1.4, there are various power quality devices that are available as solutions to these power quality problems. Some of the frequently used devices are presented and discussed in brief in next section.

Table 2.1: Categories and characteristics of power system electromagnetic phenomena

Categories	Typical Spectral Content	Typical Duration	Typical Voltage Magnitude
1.0 Transients			
1.1 Impulsive			
1.1.1 Nanosecond	5-ns rise	<50 ns	
1.1.2 Microsecond	1-μs rise	50 ns-1 ms	
1.1.3 Millisecond	0.1-ms rise	>1 ms	
1.2 Oscillatory			
1.2.1 Low frequency	<5 kHz	0.3-50 ms	0-4 pu
1.2.2 Medium frequency	5-500 kHz	20 μs	0-8 pu
1.2.3 High frequency	0.5-5 MHz	5 μs	0-4 pu
2.0 Short duration variations			
2.1 Instantaneous			
2.1.1 Interruption		0.5-30 cycles	<0.1 pu
2.1.2 Sag (dip)		0.5-30 cycles	0.1-0.9 pu
2.1.3 Swell		0.5-30 cycles	1.1-1.8 pu
2.2 Momentary			
2.2.1 Interruption		30 cycles-3s	<0.1 pu
2.2.2 Sag (dip)		30 cycles-3s	0.1-0.9 pu
2.2.3 Swell		30 cycles-3s	1.1-1.8 pu
2.3 Temporary			
2.3.1 Interruption		3s-1min	<0.1 pu
2.3.2 Sag (dip)		3s-1min	0.1-0.9 pu
2.3.3 Swell		3s-1min	1.1-1.8 pu
3.0 Long duration variations			
3.1 Interruption sustained		>1 min	0.0 pu
3.2 Undervoltages		>1 min	0.8-0.9 pu
3.3 Overvoltages		>1 min	1.1-1.2 pu
4.0 Voltage unbalance		Steady state	0.5-2 %
5.0 Waveform distortion			
5.1 DC offset		Steady state	0-0.1 %
5.2 Harmonics	0-100th harmonic	Steady state	0-20 %
5.3 Inter harmonics	0-6 kHz	Steady state	0-2 %
5.4 Notching		Steady state	
5.5 Noise	Broadband	Steady state	0-1 %
6.0 Voltage fluctuations	<25 Hz	Intermittent	0.1-7 % 0.2-2 Pst
7.0 Power frequency variations		<10s	

Table 2.2: Power quality issues, causes and effects

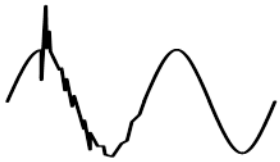
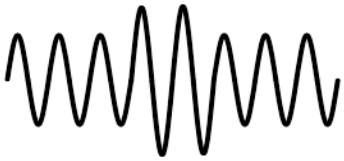
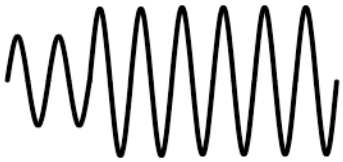
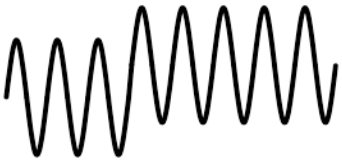
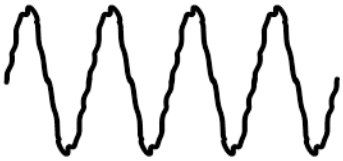
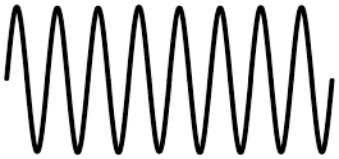
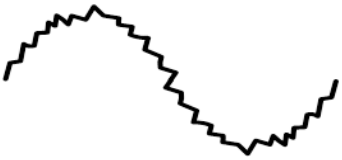
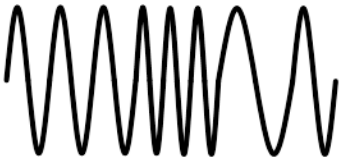
Categories	Waveform	Effects	Possible Causes
1.0 Transients			
1.1 Impulsive		Loss of data, possible damage, system halts, electronic interference	Lightning, ESD, switching impulses, utility fault clearing
1.2 Oscillatory		Loss of data, possible damage, microprocessor based equipment errors	Switching of capacitive/inductive loads, ferrorasonance, transformer energization
2.0 Variations			
2.1 Interruption		Loss of data possible, damage shutdown	Switching, Utility faults, circuit breaker tripping, component failures, control malfunctions
2.2 Sag (dip)		System halts, loss of data, shutdown, motor stalling	Heavy load starting, faults, starting large motors
2.3 Swell		Nuisance tripping, equipment damage/reduced life	Load changes, utility faults, improper wiring
2.4 Undervoltage		System halts, loss of data, shutdown, reduced equipment life	Load changes, utility faults, incorrect tap setting
2.5 Overvoltage		Equipment damage/reduced life	Load changes, utility faults, incorrect tap settings

Table 2.2 (continued)

3.0 Waveform distortion			
3.1 Dc offset		Transformer heated, ground fault currents, nuisance tripping	Faulty rectifiers, power supplies, asymmetry of electronic power converters
3.2 Harmonics		Transformer heated, system halts	Electronic loads (non-linear loads)
3.3 Inter-harmonics		Light flicker, heating, communication interference	Control signals, faulty equipment, cycloconverters, frequency converters, induction motors, arching devices
3.4 Notching		System halts, data loss	Variable speed drives, arc welders, light dimmers
3.5 Noise		System halts, data loss	Transmitters (radio), faulty equipment, ineffective grounding, proximity to EMI/RFI source
4.0 Voltage Fluctuations		System halts, data loss	Transmitters (radio), faulty equipment, ineffective grounding, proximity to EMI/RFI source
5.0 Power frequency variations		System halts, light flicker	Intermittent operation of load equipment

2.3 Importance of Power Quality

Various power quality problems and their effects were discussed in previous section. These effects can cause major financial losses to both utility companies and users of electrical power as discussed in section 1.4. Due to increasing demand of power from various industries, losses related to power quality issues are increasing and thus both utility companies and customers are becoming more concerned about the quality of electrical power. Apart from noticeable financial impacts, there are also various indirect cost associated with the power quality problems. For instance, utility companies can lose their customers due to poor quality of power, residential customers relying on digital technologies can lose important data and time over poor power quality etc. Thus, the need of various power quality devices is increasing.

2.4 Mitigation Techniques

According to Leonardo Power Quality Initiative voltage sag (dip), swells and harmonics are the most common power quality issues faced by US companies. Hence, this section will be primarily concerned about sag (dip), swells, undervoltage, overvoltage, interruption and harmonic type of power quality disturbances.

There are number of custom power devices reported in literature as a solution of various power quality disturbances such as Distribution Static VAr Compensator (D-SVC), Distribution Static synchronous Compensator (D-STATCOM), Distribution Series Capacitor (DSC), Static Voltage Restorer (SVR), Dynamic Voltage Restorer (DVR), Battery Energy Storage System (BESS), Solid State Transfer Switches (SSTS), Surge Arrestors (SA), Solid State Fault Current Limiter (SSFCL), Uninterruptible Power Supply (UPS), Super conducting Magnetic Energy System (SMES), Unified Power

Quality Conditioner (UPQC), Passive Power Filters (PPF), Active Power Filters (APF), Isolation Transformers and Constant Voltage Transformer (CVT) . Some of these devices can be used for a disruption whereas some of them can provide solutions for several disturbances. Several mainstream devices and their capability of mitigating different disturbances are tabulated in Table 2.3.

Table 2.3 Mitigation Techniques

Mitigation Technique→ / Disturbance↓	Static VAr Compensators (SVC)	Distribution Static Compensators (D-STATCOM)	Distribution Series Capacitors (DSC)	Static Voltage Restorer (SVR)	Dynamic Voltage Restorer (DVR)	Series passive filters (SPF) and Series Active filters (SAF)	Parallel passive filters (PPF) and Parallel Active filters (PAF)	Uninterruptible Power Supply (UPS)	Unified Power Quality Conditioner (UPQC)	Surge Arrestors (SA)	Battery Energy Storage Systems (BESS)
Transients										✓	
Interruption					✓			✓			✓
Sag (dip)	✓	✓	✓	✓	✓			✓			✓
Swell	✓	✓	✓	✓	✓			✓			✓
Undervoltage	✓	✓	✓	✓	✓			✓			✓
Overvoltage	✓	✓	✓	✓	✓			✓			✓
Harmonics					✓	✓	✓	✓			
Voltage fluctuations				✓	✓			✓			✓
Power frequency variations								✓			

2.4.1 Distribution Static VAr Compensator (D-SVC)

D-SVCs are shunt connected custom power devices being used for fast acting reactive power compensation since 1970s [10-12]. They are a part of Distribution Flexible Alternating Current Transmission System (D-FACTS) family. Thyristors are used as a switch or control mechanism to connect them completely or partially in the system. By controlling the firing angles of thyristors, output of D-SVCs can be controlled to provide or consume reactive power in terms of leading or lagging currents to maintain voltage stability and unity power factor at any bus [13]. Different components of D-SVCs are illustrated in Figure 2.1.

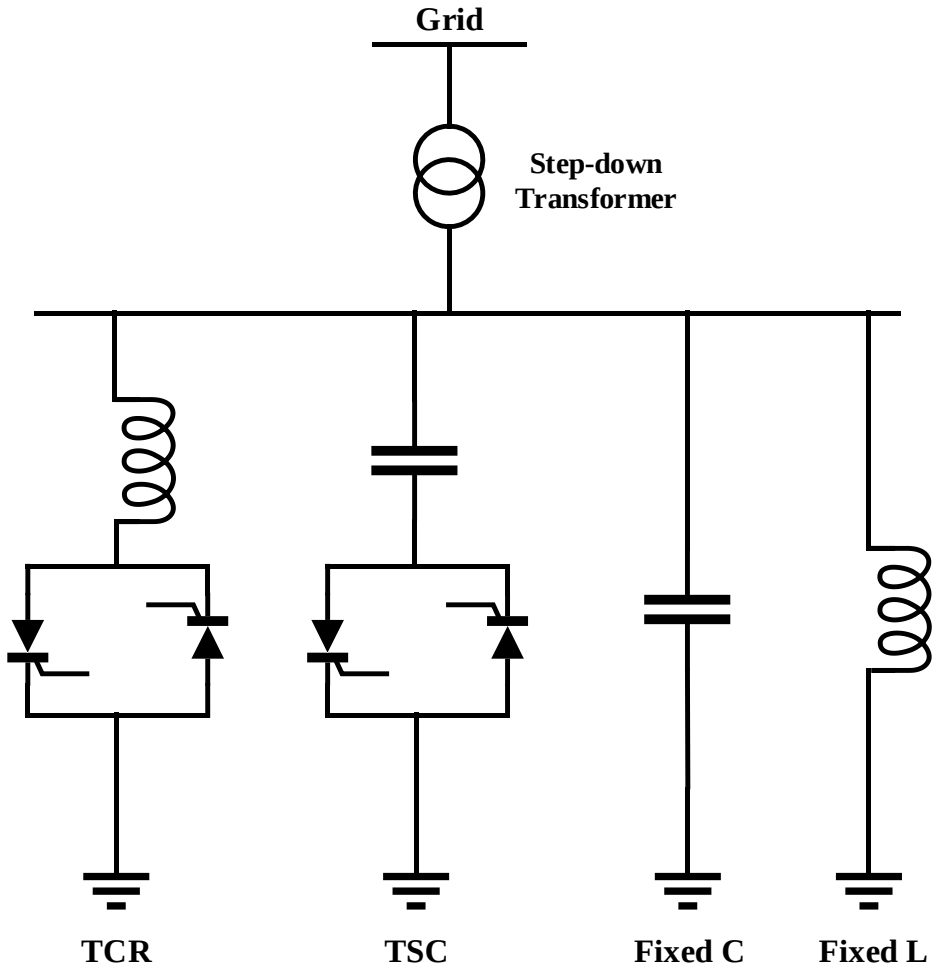


Figure 2.1: D-SVC components

Thyristor Switched Capacitor (TSC) is a shunt connected component of D-SVC as shown in Figure 2.1. TSCs cannot be operated partially such as by controlling firing angles of thyristors because it creates large amplitude resonant currents which overheat the capacitors and thyristors and introduce harmonic distortion into the grid. Hence, TSCs are always operated as fully on or fully off. Usually, each TSC is a combination of number of parallel connected thyristor capacitor units. The total susceptance can be varied in step wise manner and may be any possible combination of 0, 1, 2… or n at a time. These steps can be made smaller by having different values of susceptances leading to smoother and better control. However, it is unlikely to have various values of susceptances it any power system due to their complex control and higher cost. Though, one possible solution is to have (n -1) equal susceptances and one half susceptance to increase possible combinations to 2 n [14]. When the load is inductive, these capacitors are switched as discussed earlier to provide reactive power and increase the system voltage to its nominal value. The discrete VI characteristic of TSC is shown in figure 2.2. It is mainly a function of number of TSC units, their susceptance rating and voltage ripple ΔV. Individual TSC units are operated accordingly to maintain the bus voltage within a range of $V_{ref} \pm \Delta V/2$. The voltage interval ΔV should be chosen reasonably to avoid frequent switching of capacitors.

Thyristor switched Reactor (TSR) also contains an anti-parallel thyristor switch and a reactor as shown in Figure 2.1. Unlike TCR, TSR can be switched partially by changing firing angle α of thyristor providing varying susceptance of the reactor continuously. Usually, the TCR is operated for $90° \leq \alpha \leq 180°$ which corresponds to continuous to minimum current conduction as shown in Figure 2.3. However, for

operating range 90° ≤ α, TCR introduces considerable amount of odd harmonic currents which can cause system voltage distortion [15]. In order to block these currents from entering into the grid, usually series connected LC network is connected in parallel with TSR. For operating range of 0° ≤ α ≤ 90°, DC offsets are introduced to reactor current and thus this operating range is avoided for the conduction of TCR [14].

The typical VI characteristic of a TSR shows the current of TCR as a function of its voltage for different firing angles α and susceptance B_L as illustrated in Figure 2.4. Note that any operating point within two limits is possible to achieve depending on the system voltage and firing angles but it is restricted by the maximum limits of voltage and current of thyristor valve. For capacitive loads, TCR is switched within this operating range to absorb reactive power thus enabling system voltage to be decreased and maintained at its defined value.

As shown in Figure 2.1 fixed reactor (FR) and fixed capacitors (FC) can be cheaper solutions for the given purpose. Use of Fixed Capacitor (FC) can dampen out the

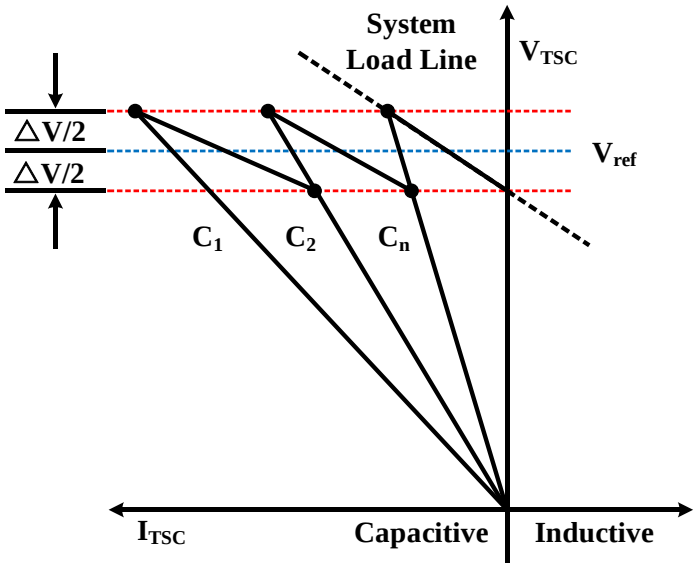


Figure 2.2: VI characteristics of a TSC

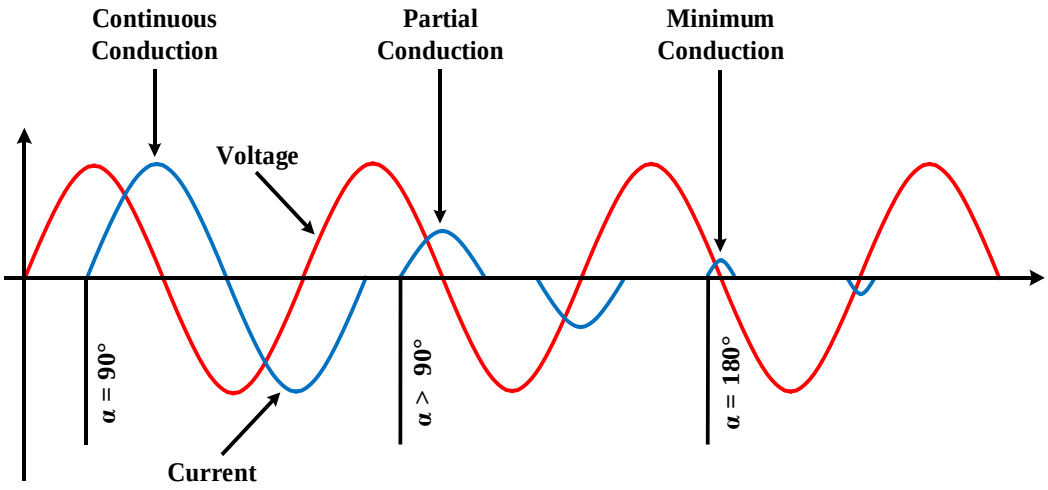


Figure 2.3: TSR current for different firing angles

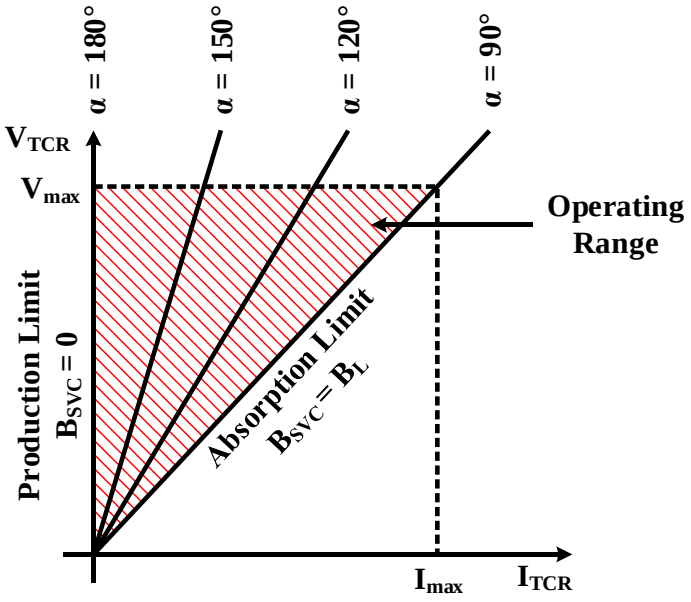


Figure 2.4: VI characteristics of a TSR

current harmonics generated by TCR [15] and it also eliminates the complex control and expensive thyristors. However, TCR current is higher in FC-TCR configuration and hence the losses are higher [15]. Thus, they are used only at buses where the load is mostly capacitive. Therefore, Fixed Capacitor Thyristor Switched Reactor (FC-TCR) and TCR-TSC are the most common topologies used for D-SVC.

2.4.2 Distribution Static Synchronous Compensator (D-STATCOM)

Distribution Static Synchronous Compensators (D-STSTCOMs) are being widely used for regulating system voltages, improving voltage profiles and load compensation since 1990s [16]. Typically, D-STATCOMs are composed of inverter, reactive storage and coupling transformer. They can be classified mainly according to their converter type or topology type. For example, they may be connected to the AC system via non-isolating transformer topology or by isolating transformer topology. Similarly, if reactive storage is capacitor, voltage source type converter is used and if inductor is used for reactive storage, current source type converter is implemented. These converters can be composed of GTOs or IGBTs or any gate controlled devices. Mainly IGBTs are used for high frequency operation at less handling power rather than thyristors as in TCR or TSC. A VSI based D-STATCOM with capacitive energy storage is shown in Figure 2.5.

D-STATCOM works as a sink or source of reactive power. The reactive power supplied or consumed by the device is determined by the difference between AC source voltage V_s and voltage generated by the inverter V_c. The natural and controlled characteristics are shown in Figure 2.6 and 2.7. D-STATCOMs can be realized as a variable voltage generator V_c. V_s and V_c are kept to be nearly in phase with each other. So, when $V_c < V_s$ the D-STATCOM behaves as an inductive load (providing lagging currents) consuming reactive power from the source. Conversely, the D-STATCOM behaves as a shunt connected capacitor to the AC source thus generating capacitive (leading) current and providing reactive power to the grid when $V_c > V_s$ [17]. As any practical system, D-STATCOMs are also not lossless. These losses and DC link voltage maintenance are provided by the AC system itself because of the absence of active source [37].

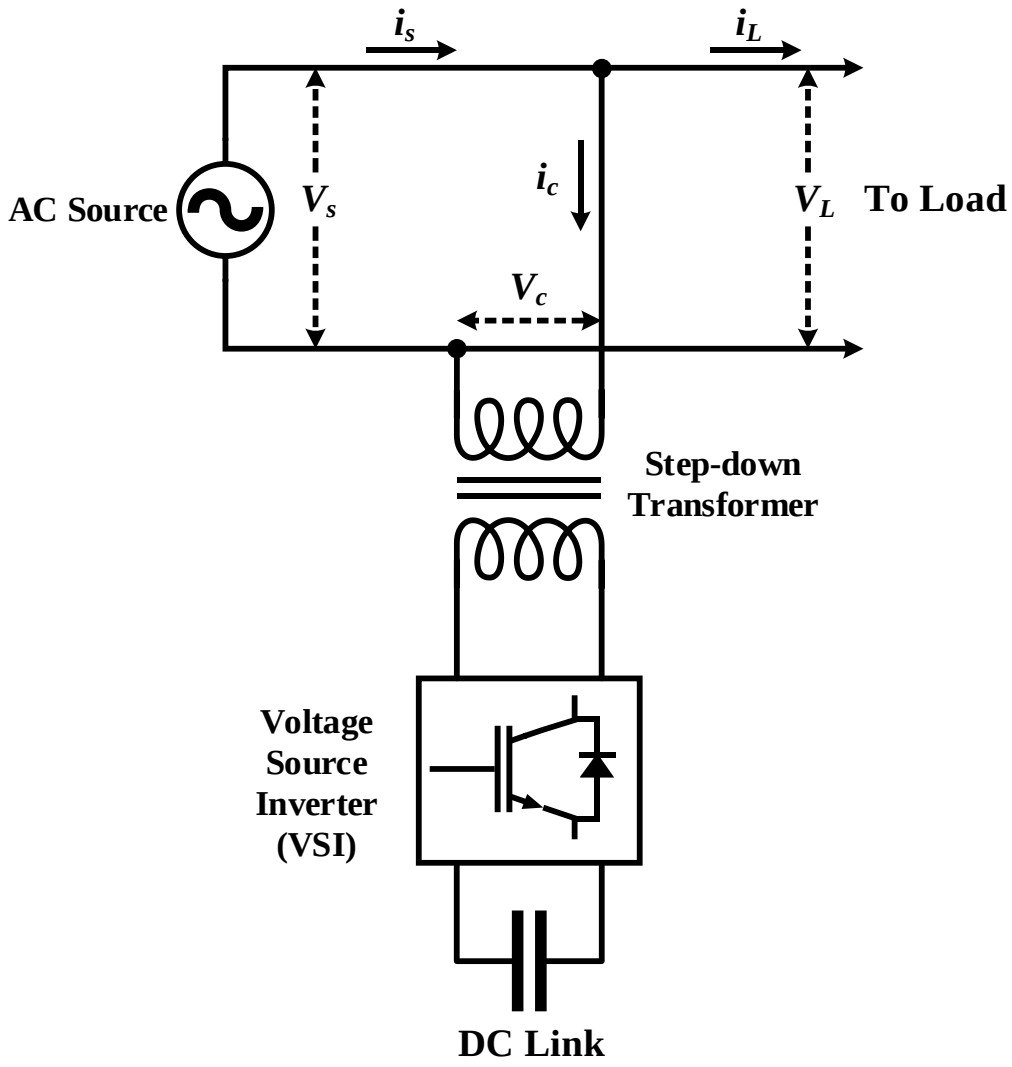


Figure 2.5: VSI (Voltage Source Inverter) based D-STATCOM

As described earlier D-STATCOMs are used for voltage stability, reactive power compensation and load compensation. For load compensation, D-STATCOMs are controlled in current control mode (CCM) and for voltage and reactive power compensation they are operated in voltage control mode (VCM). Apart from that, they also can be used for current harmonic compensation and transient voltage disturbances. The classification, various topologies and their control methodologies and operation characteristics for different control modes are explained in detail in [7] and [17].

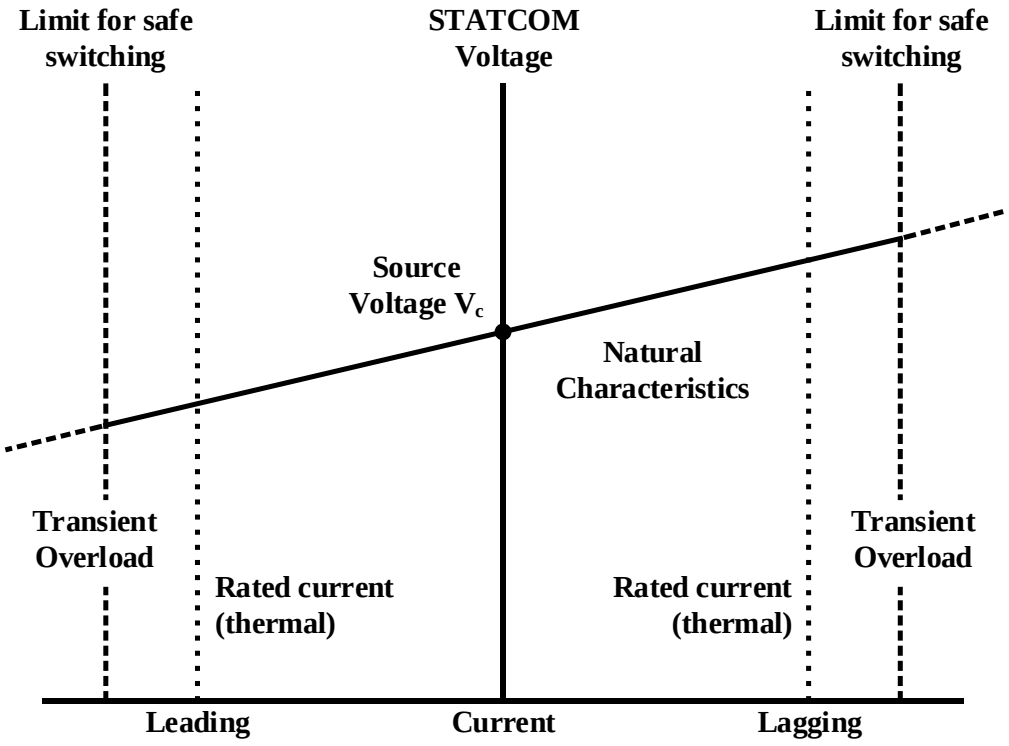


Figure 2.6: Natural characteristic of D-STATCOM

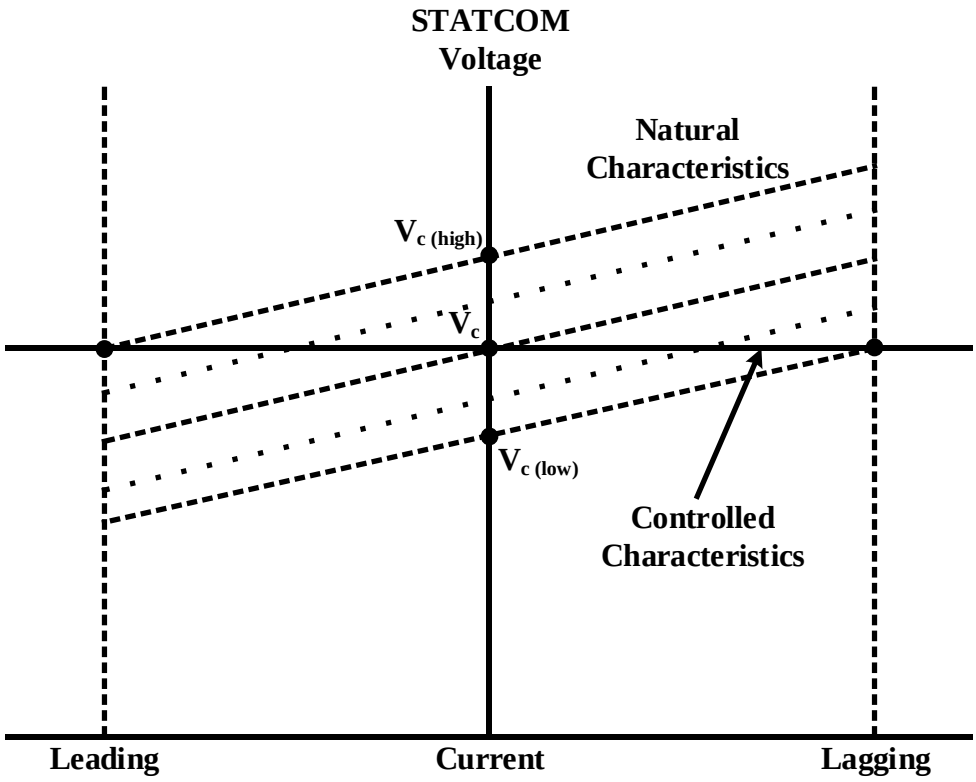


Figure 2.7: Controlled characteristic of D-STATCOM

2.4.3 Dynamic Voltage Regulator (DVR)

Dynamic Voltage Regulator (DVR) is a series connected solid state device used to shield sensitive loads from voltage sag, swell, undervoltage, overvoltage and harmonics. When the source voltage is distorted, DVR injects suitable amount of voltage in series with grid voltage to regulate the load voltage at its desired value. Conventional solutions for these disturbances include uninterruptible power supplies (UPS), tap changing transformers, static voltage regulator, D-STATCOM, D-SVC etc. DVR is preferred over these devices due to its lower cost, higher capacity, higher efficiency and smaller size.

The DVR is composed of battery storage with a DC link capacitor, a voltage source inverter, a filter circuit and a series transformer. The purpose of inverter is to synthesize controlled voltage and injecting it in series with the source voltage to provide well-conditioned voltage to sensitive loads. The inverter is mainly a voltage source inverter which can be composed of MOSFETs or IGBTs for faster regulation. Due to high frequency operation of inverter, a LC filter is used in series with the inverter output to eliminate high frequency components from synthesized voltage. The basic schematic and concept of DVR along with voltage waveforms are illustrated in Figure 2.8 [18].

Determination of voltage disturbance type and generation of reference signal are two major parts of the DVR control system. The voltage available at source is measured and compared with its set reference value to detect any disturbance in the grid voltage including its starting point, ending point, amount of sag/swell/harmonics order and phase shift. There are different methods available such as Fourier Transform (FT), Phase Locked Loop (PLL), Peak Value detection, Root Mean Square detection (RMS) and Wavelet Transform (WT) to determine the type and characteristics of the disturbance.

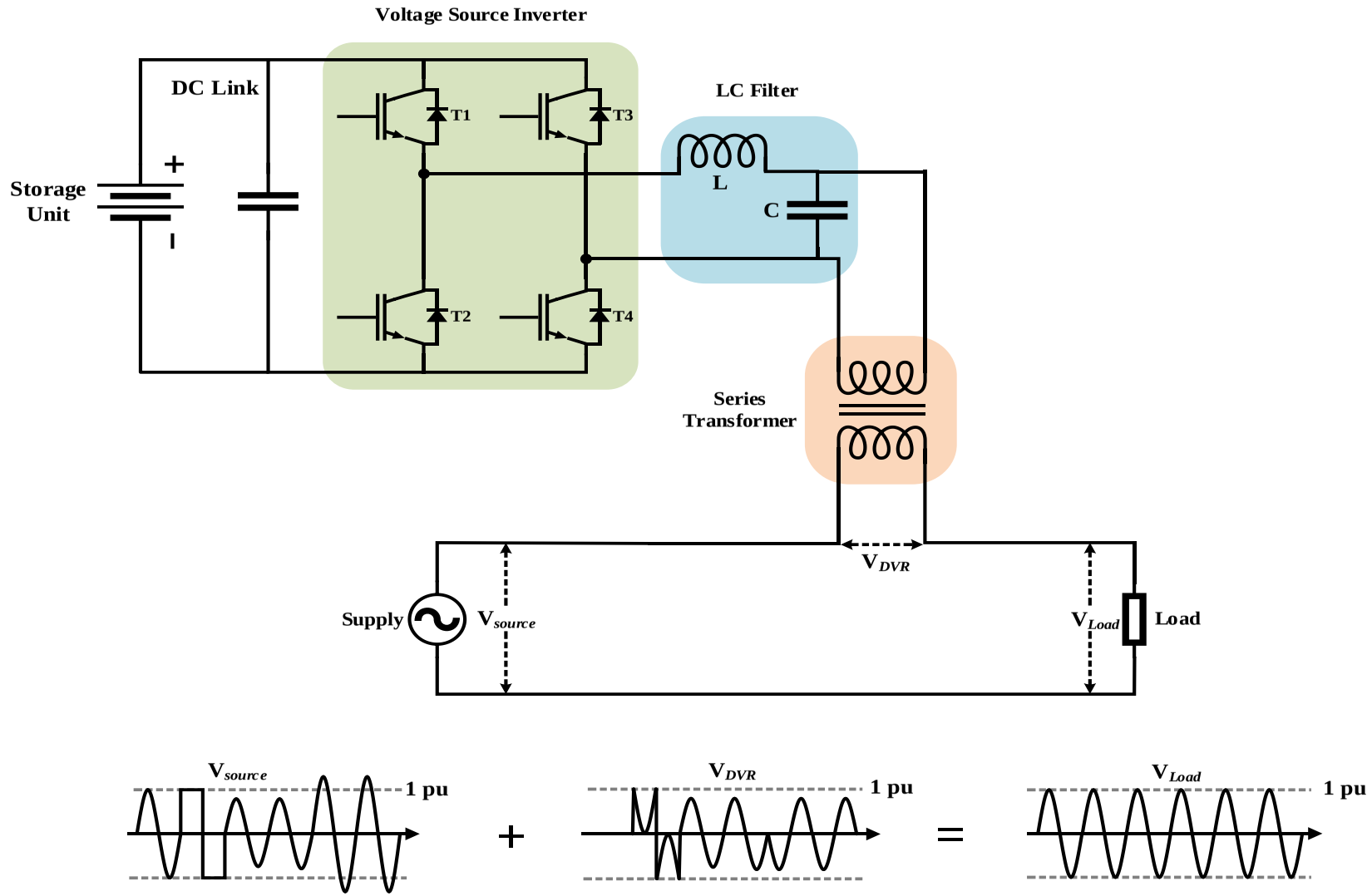


Figure 2.8: Schematic and operation of Dynamic Voltage Regulator (DVR)

The next and most important step of DVR control system is to determine the reference signal for inverter switching to inject suitable voltage in series with grid for load voltage compensation. In-phase, Pre-sag and energy minimize compensation are the primary approaches for load voltage compensation. The selection of the approach depends on the type of storage device used in DVR, active power support capability of DVR and sensitivity of load to various disturbances [18].

The In-phase approach is commonly used and easiest method for load voltage compensation. The compensation voltage is injected in phase with the source voltage. The phasor diagram for such method is shown in Figure 2.9 in which V_{Load}, V_{source} and I_{Load} corresponds to before sag conditions and V'_{Load}, V'_{source}, I'_{Load} and V'_{DVR} indicates after sag conditions. Moreover, Ø is the angle between voltage and current and α is phase jump of voltage with respect to former voltage. The advantage of using this strategy is that the magnitude of the series injected voltage; voltage rating of DVR and voltage rating of DC link is minimal. However, it requires active power during compensation and it cannot restore phase jump caused by the voltage disturbance [18-19].

The phasor diagram for Pre-sag compensation is shown in Figure 2.10 in which the series compensation voltage is determined in such a way that the voltage magnitude and phase remains the same as before the voltage sag. Phasors V_{Load}, V_{source} and I_{Load} indicate before sag conditions whereas V'_{Load}, V'_{source}, I'_{Load} and V'_{DVR} refer to after sag conditions. Also, Ø is the angle between voltage and current and α is the phase jump. This method can restore both voltage jump and magnitude of the voltage so that sensitive loads are not affected with any disturbance. Moreover, it also blocks any circulating or transient currents from entering the load but it requires active power during compensation

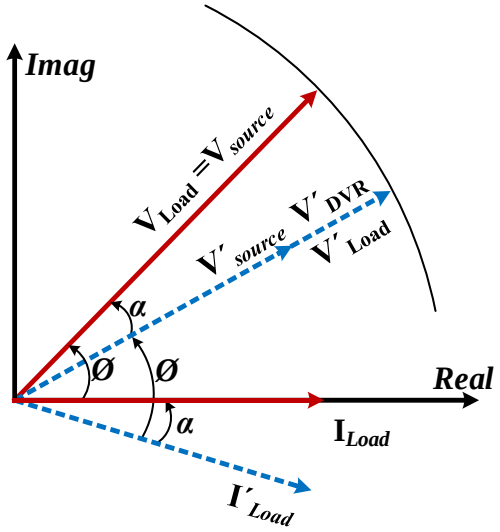


Figure 2.9: In-phase compensation phasor diagram

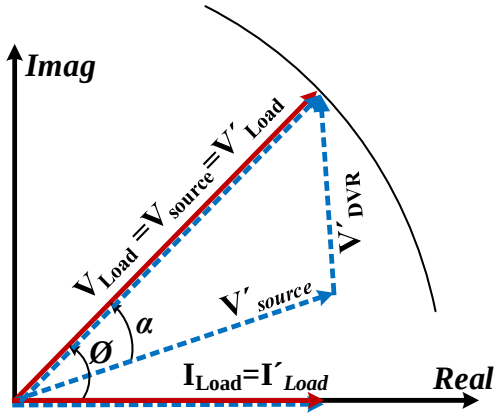


Figure 2.10: Pre-sag compensation phasor diagram

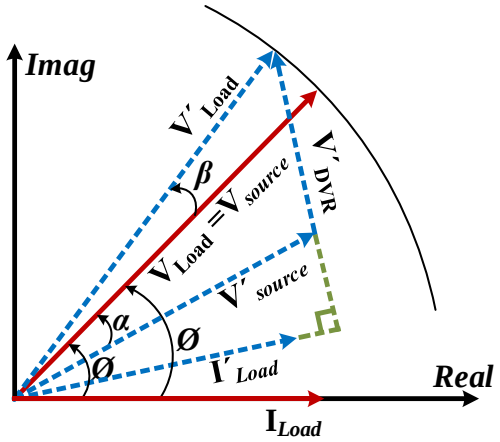


Figure 2.11: Energy minimized compensation phasor diagram

and the magnitude of the compensation voltage is also not minimal [18-19].

While all the former methods require active power for voltage compensation, energy minimized compensation strategy is designed to reduce the amount of active power requirement by injecting the compensation voltage which is perpendicular to the load current. The phasor diagram for such strategy is shown in Figure 2.11; V_{Load}, V_{source} and I_{Load} are before sag phasors whereas V'_{Load}, $V'source$, I'_{Load} and V'_{DVR} refer to after sag phasors. The angle between voltage and current is denoted by Ø and phase jump experienced by voltage is indicated by α. As the name suggests this compensation method minimizes active power requirement most of the times. However, for high power factor load, compensation of deep sag requires active power. Also, the voltage is injected perpendicular to the load current which results in higher magnitude of the compensation voltage. It also have some other drawbacks such as higher rating of DVR, higher DC bus rating and causing voltage jumps (denoted by β in Figure 2.11) at load voltage.

These compensation methods are discussed for voltage sag mitigation but they can also be used as a solution for voltage swell. However, for voltage harmonics mitigation only in phase compensation strategy can be used.

The only disadvantage of DVR systems is the battery life. As battery storage is used to mitigate various voltage disturbances, it cannot provide load voltage compensation if the swell or swag is sustained for longer period [20]. The DVR should be able to mitigate voltage sag, swell, undervoltages, overvoltages and harmonics simultaneously and continuously irrespective of duration of disturbance. Hence the proposed DVR topology in this article will be focused on eliminating the storage device requirement and will primarily be using in phase compensation strategy.

2.4.4 Static Voltage Regulator (SVR)

Power electronics based converters provide more flexibility and control over the conventional technologies because they use electrical switches to generate desired output and do not include any moving mechanical parts. Static Voltage Regulator (SVR) is a good example of power electronics based converter topology that is replacing servo voltage regulator which is used for mainly voltage sag and swell mitigation. Schematics of servo voltage regulator and static voltage regulator are shown in Figure 2.12 and 2.13 respectively.

A servo voltage regulator comprises a buck-boost series transformer, a variable transformer driven by motor and an output sensing circuit as shown in Figure 2.12. The primary of buck-boost transformer is connected between input and output of voltage regulator while one end of secondary winding is connected to a fixed tap of variable transformer and another end is connected to a tap changing shaft which is driven by motor. The driving motor can either be DC servo motor or AC synchronous motor. The output at load terminals is regulated by adding (in phase) or subtracting (180° out of phase) the error voltages. Sensing circuit of the device continuously senses the output voltage and if the voltage is greater or lesser than its fixed point, it gives driving signal to the motor. So, if the sensed voltage is lesser than its fixed value, motor drives the variable shaft in upwards direction from fixed tap across the variable transformer, thus adding the error voltage in order to have a stabilized output. Similarly, if the voltage is higher than its reference, the motor moves the shaft downwards from the fixed tap, thus inducing negative voltage on the buck-boost transformer. This negative voltage is added to input maintaining output at its defined value [21].

Static Voltage regulator (SVR) has the same configuration as servo voltage regulator only the motor and variable transformer mechanism is replaced by bridge based AC-AC converter in case of SVR. The working principle of Static Voltage Regulator (SVR) is same as servo regulator. When the sensing circuitry senses low voltage on input side, AC-AC converter is operated to generate the remaining voltage in phase with input voltage thus adding the voltages. Likewise, in case of high voltage at input side, the AC-AC converter is triggered to provide the extra voltage which is 180° out of phase with input. Thus, subtracting the extra voltage from input and regulating desired level of voltage at output terminals. Variation in input voltage V_s, their corresponding compensation filtered voltage V_c, unfiltered voltage V_o and load voltage V_L are also provided in Figure 2.13. The color coding corresponds to the change in input voltage and its corresponding correction voltages [22].

SVRs use AC-AC converter based configuration to generate desired voltage as discussed earlier. This converter mainly consists of high frequency switching devices like IGBTs or MOSFETs to ensure fast voltage correction compared to servo regulators. In addition to that it has few more advantages over servo regulators such as silent operation, low maintenance, compact size and no wear and tear of mechanical parts [23]. Moreover, unlike DVR; Static Voltage Regulator eliminates the need of storage unit hence making the system more reliable as it can provide voltage sag/swell mitigation regardless of period of the voltage disturbance. Although, SVR cannot provide solutions for voltage harmonic type of disturbance like DVR. Hence this article investigates the direct AC-AC converter based solution to eliminate the storage device requirement and to provide solutions for voltage sag, swell and harmonics.

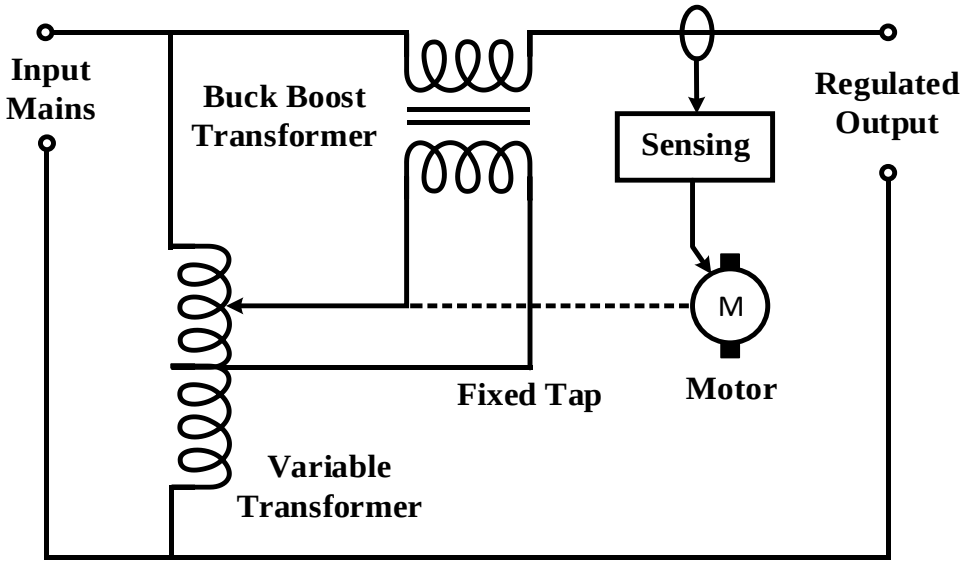


Figure 2.12: Servo Voltage Regulator

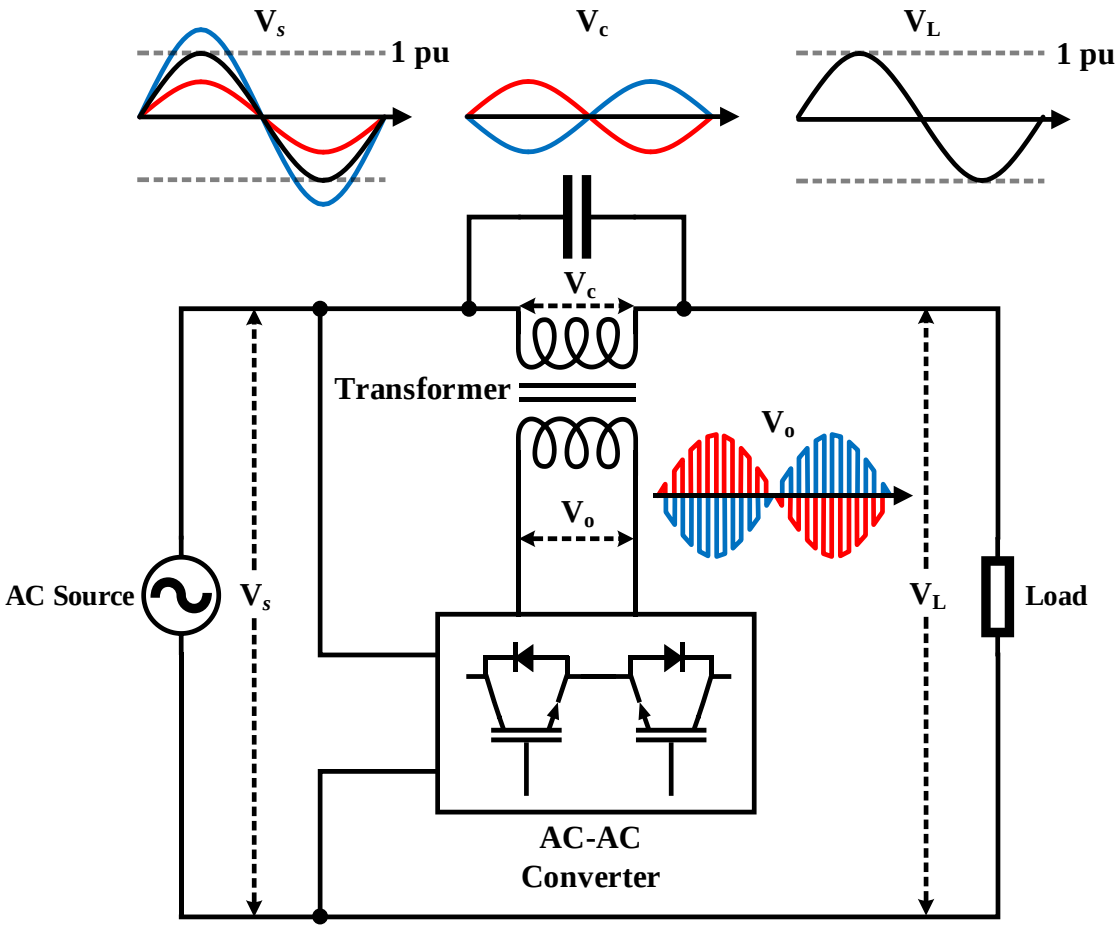


Figure 2.13: Static Voltage Regulator (SVR)

2.4.5 Passive and Active Power Filters

The usage of power electronic converters is increasing rapidly due to their capability of quick and flexible electric power control with higher efficiency. Variable Frequency Drives (VFDs), electrical furnaces, solid state converters, inverters, battery chargers etc. are good examples of semiconductor switches based power electronic converters. These converters are classified as non-linear loads as their current or voltage waveforms are not sinusoidal but distorted at fundamental frequency. Being non-linear loads, these converters draw harmonic and reactive currents from their respective grid thus injecting harmonics into the grid. The injection of harmonic and reactive power results in lower system efficiency, poor power factor and causes disturbance to other consumers connected to the same electrical network [7].

These non-linear loads can be further classified as Voltage Source Non-linear Loads (VSNLs) or Current Source Non-linear Loads (CSNLs) depending on their effects on voltage or current. Diode rectifier with smoothing capacitors is a good example of voltage source non-linear load. The input current of the rectifier is highly distorted and its harmonic content is highly dependent on grid voltage unbalance and grid side impedance whereas the voltage at rectifier input terminal is less dependent on the grid side impedance. Thus, it is defined as a voltage source non-linear load. On the other hand, the current distortion caused by switching operation of converters is not affected by the ac side in case of current source non-linear loads such as thyristor controlled converters, rectifier with dc inductor, highly inductive load with thyristor control converters, etc. [24]

Passive Power Filters (PPFs) are providing solutions for current harmonics, voltage harmonics, reactive power and voltage regulation since long time. Depending on

the objective to be achieved, they have evolved in terms of different configurations in last five decades. Series Passive Filters (SPFs) and Parallel Active Filters (PAFs) are most popular and widely used technologies for voltage and current harmonics compensation. Figure 2.14 shows simplified schematic diagram of Series Passive Filter (SPF) in which a resonant parallel LC network tuned at a harmonic frequency is connected in series with AC mains and voltage source type harmonic source. Usually, LC blocks tuned at various harmonic frequencies are connected in series to form a SPF as shown in Figure 2.14. The SPF provides high impedance (Z_s) path to frequency matching its resonance frequency thus blocking voltage at that harmonic frequency from entering AC mains. On the other hand, a Parallel Passive Filter (PPF) is a shunt connected resonant series LC network as depicted in Figure 2.15. Unlike SPF, PPF provides low impedance (Z_p) path to the frequency matching its resonance frequency hence working as a harmonic current sink. A PPF consist of 3^{rd}, 5^{th}… N^{th} order filters is shown as an example in Figure 2.15.

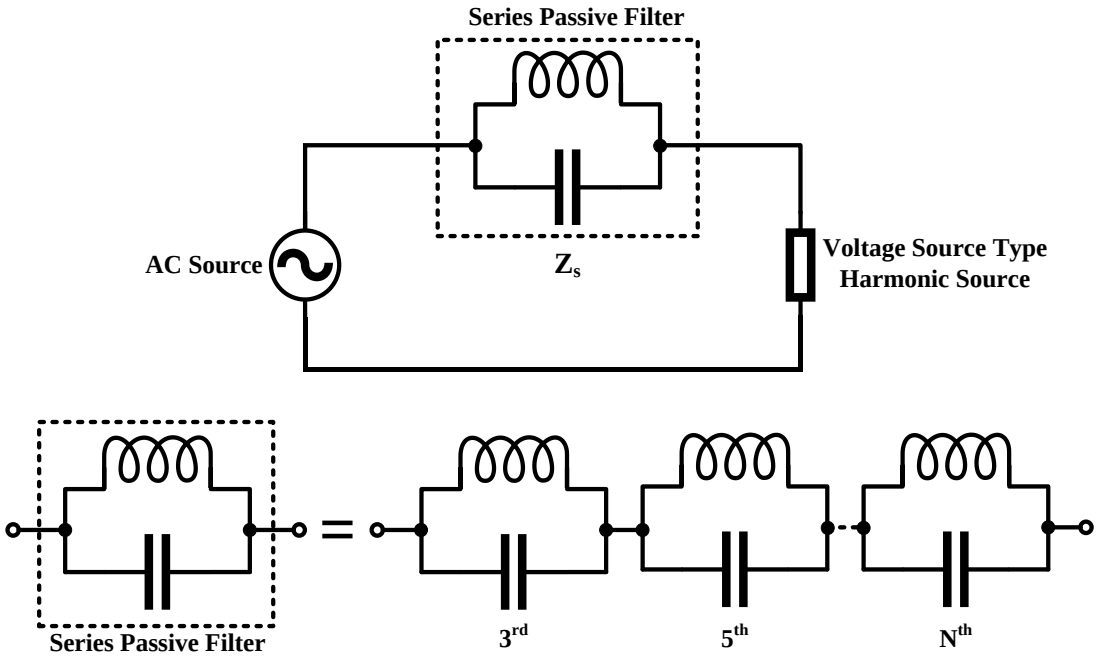


Figure 2.14: Series Passive Filter (SPF) schematic [44]

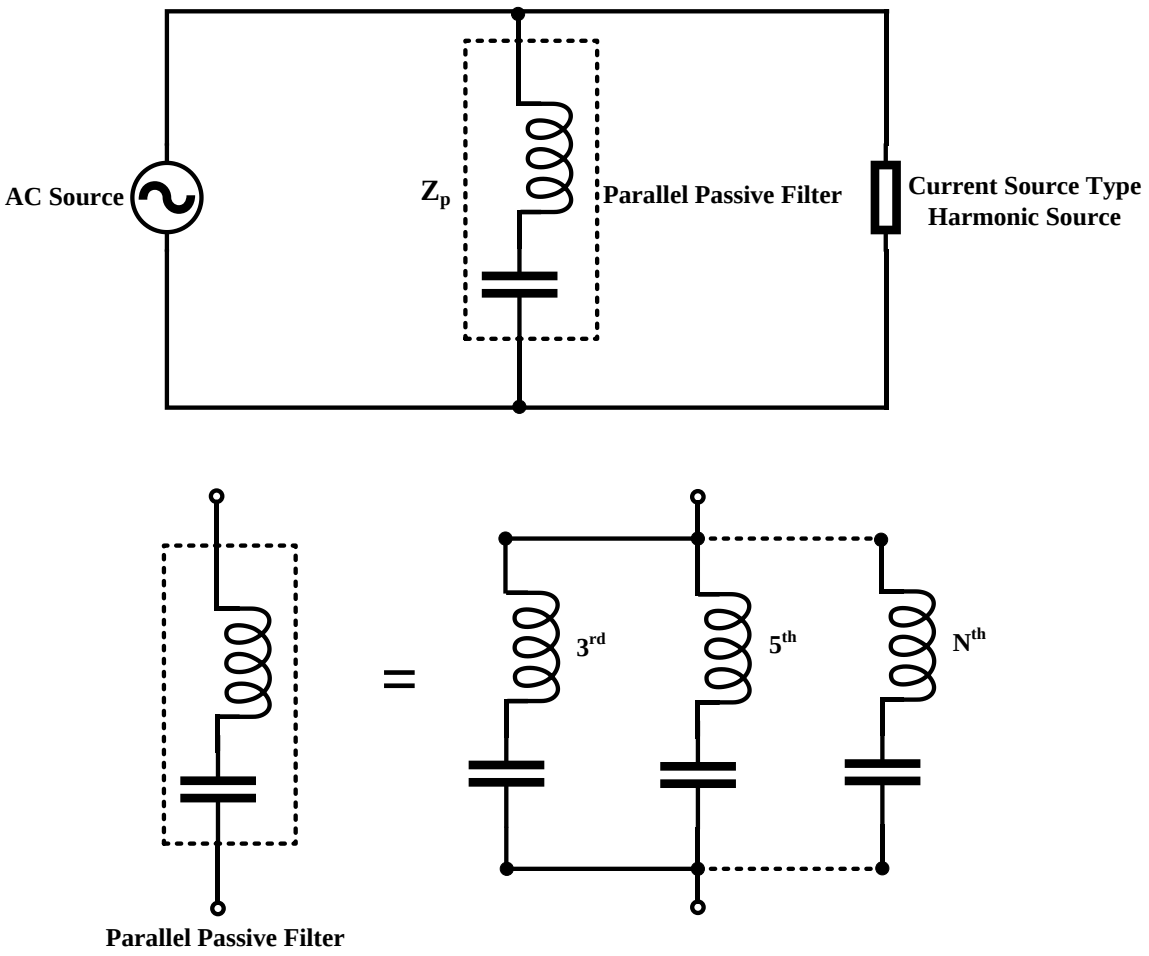


Figure 2.15: Parallel Passive Filter (PPF) schematic [24]

Passive Power Filters have some advantages such as simplicity, flexibility, and cost. However, the major drawbacks of PPF includes, fixed compensation, resonance effects on grid, large size and possible tuning and detuning issues. To overcome the drawbacks of passive power filters, efforts have been made to develop adaptable solutions for harmonic and reactive power problems known as active power filters. Generally, a power filter consists of a dc link or battery storage and a voltage source inverter or current source inverter to synthesize AC voltage from dc storage [7]. A voltage source inverter based Series Active Filter (SAF) and its operating principle is illustrated in Figure 2.16. The SAF injects opposite phase harmonic voltage of same

amplitude in series with load voltage thus acting as a voltage source to block harmonics currents from flowing into the AC grid. The voltage and current waveforms of diode rectifier (voltage-source type harmonic source) without SAF and with SAF are also illustrated in Figure 2.16. Contrary to SAF, Parallel Active Filter (PAF) injects out of phase harmonic current of same amplitude in AC line thus behaving like a harmonic current source to block the load current harmonics entering the grid. The voltage and current waveforms of thyristor controlled converter with inductive load (current-source type harmonic source) with PPF and without PPF is also depicted in Figure 2.17 [25].

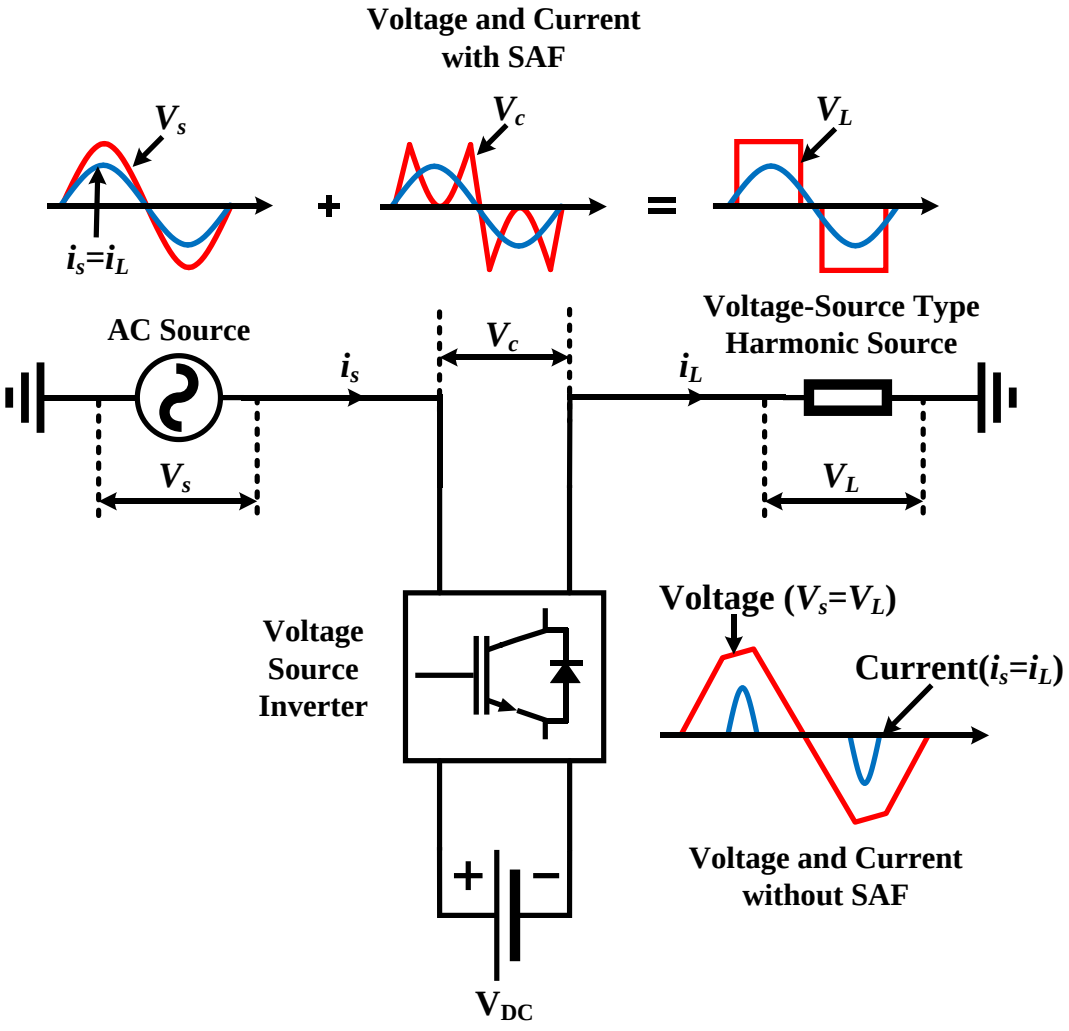


Figure 2.16: Series Active Filter (SAF) schematic and operation

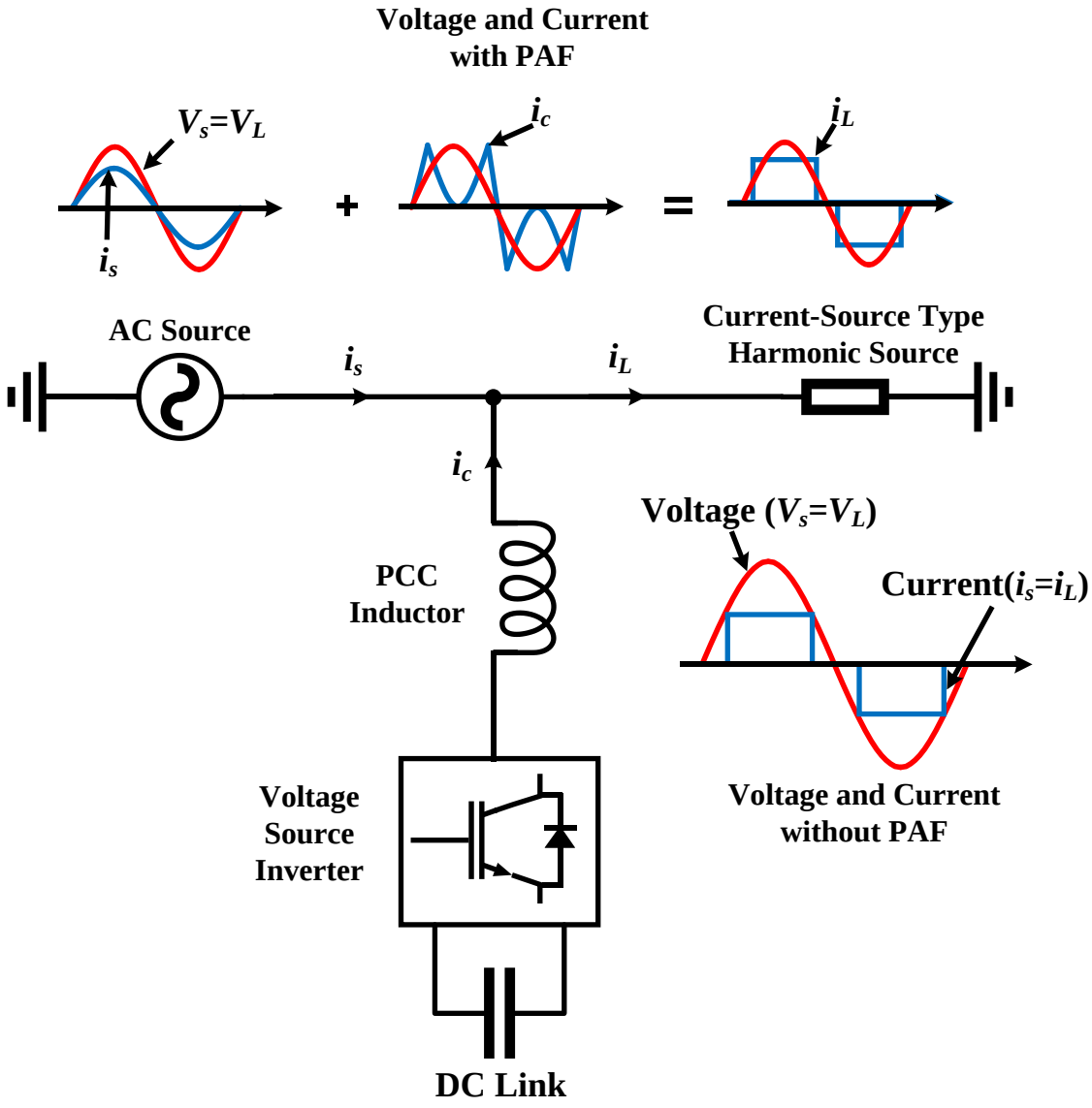


Figure 2.17: Parallel Active Filter (PAF) schematic and operation

The performance of PAF is better for the elimination of low order harmonics (3rd, 5th, 7th), while PPF is more suitable for higher order harmonics (11th, 13th, 15th). Hence, to enhance the performance of the filters and achieve better voltage/current compensation, various combinations of PAF, SAF, PPF and SPF called Hybrid Filters are being researched and developed. Various combinations of such filters along with their individual and combined performance is discussed and explained in brief in [7, 24].

2.4.6 Uninterruptible Power Supply (UPS)

Uninterruptible Power Supply or Uninterruptible Power Source (UPS) are being widely used and researched in recent years due to its ability of providing clean, uninterruptible and conditioned power to sensitive equipment such as computers, data centers, telecommunication, medical equipment etc. under almost any power quality disturbance as shown in Table 2.2. In pursuance of maintaining load power uninterrupted in case of main AC power failure, power is supplied by energy storage systems such as batteries, supercapacitors or flywheels. Usually, energy of storage devices and power conversions are maintained by using various power electronics stages such as DC-DC and DC-AC at higher frequencies [26].

A variety of UPS systems are available each having discrete characteristics and applications. They are mainly classified into six different categories: (I) Standby, (II) Line Interactive, (III) Standby Online-Hybrid, (IV) Standby Ferro, (V) Double Conversion Online and (VI) Delta Conversion online. The standby UPS is the most commonly used system for household applications. The schematic of the system is proposed in Figure 2.18 along with its normal and back up operative direction. The AC power from utility is the primary source of power for loads and battery charging (through battery charger). When the primary power source fails, transfer switch is operated to transfer the load to battery storage. The AC power is synthesized via DC-AC conversion from DC power stored in battery. Inverter is operated only when the AC power fails, hence it is called “standby” UPS. However, in line interactive UPS system, battery and inverter are always connected to the output of UPS system as depicted in Figure 2.19. The inverter operates as a rectifier in order to charge the battery when AC power is

available and in case of AC power fail, the transfer switch is operated to isolate the system from AC mains, and power is provided by the battery inverter combination. This type of UPS system is mainly used for small business, web and departmental servers [27].

The standby online hybrid UPS topology and its operation are described in Figure 2.20. The load is always connected to the inverter and DC power to inverter is fed via rectifier or battery storage. Note that AC power from utility is still the primary source of power for this system. When AC power is available, battery is charged by means of battery charger and power to the load is delivered by rectifier inverter combination. Whereas, in case of power failure, transfer switch connects inverter to the UPS output thus connecting inverter with battery via DC-DC converter. These systems are being used for power level lesser than 10 kVA [27].

Standby Ferro UPS has a special saturating transformer called as Ferro transformer with Ferro Resonance capability. It consists of two primary windings and one secondary winding. The secondary winding is always connected to load whereas one of the primary winding is connected to AC mains via transfer switch and other one is connected to battery via inverter. The primary path of power flow is still the utility power. In normal condition, transfer switch is closed, battery is charged via charger and load is supplied via Ferro transformer connected with utility. However, when AC power is not available, transfer switch is opened and power is supplied by the inverter. Inverter is energized only in case of power failure hence it is called “Standby Ferro”. The Ferro transformer provides the isolation from AC transients and limited voltage regulation. Yet, it also distorts the output waveform, adds transients to it, highly inefficient and bulky. The schematic and operation modes are presented in Figure 2.21 [27-28].

Figure 2.22 describes the block diagram and different modes operation of double conversion online UPS system. Unlike other UPS systems as discussed above, primary source or power is not AC mains for this type of system but battery storage is. In normal condition, battery - inverter combination delivers the power to the load and battery is charged via charger. When battery charger – battery – inverter combination fails for any reason, utility power is used as a backup power source. Hence, while transaction from AC power to UPS affects the output in all other UPS systems in case of AC power failure, the output is affected by transaction from battery to AC power for this type of UPS topology. The load is always supplied by battery charger – battery – inverter combination which leads to reduced efficiency and considerate amount of heat generation.

The double conversion online UPS converts AC power to DC to charge the battery and the same DC power is utilized to synthesize AC power for loads under normal circumstances or AC power failure. The efficiency of such UPS is considerably less due to dual power conversion stages. On the other hand, line interactive UPS has only one power conversion stage as discussed earlier but it provides limited voltage regulation and reactive power compensation. Therefore, to overcome the drawbacks of other UPS systems and combine their advantage, a new UPS technology is introduced called as delta conversion online UPS or series parallel UPS as depicted in Figure 2.23. It consists of a parallel connected converter labeled as main inverter and a series converter labeled as delta converter. During normal operation, battery is charged through the main inverter and load is supplied by the utility AC power. However, when AC power is not available, static switch is operated to isolate the load from AC mains and load power is

maintained by the battery. The main inverter is also used to provide current harmonics and reactive power compensation apart from functioning as a battery charger. The additional delta converter facilitates the voltage regulation when sag or swell occurs in AC mains voltage. Thus, the series parallel connection of the converter enables independent control of voltage regulation, reactive power compensation and harmonic power compensation. Although, it contains two power converters like double conversion online UPS, the efficiency is comparatively higher as the delta converter only provides the voltage difference between AC mains and load [26-28].

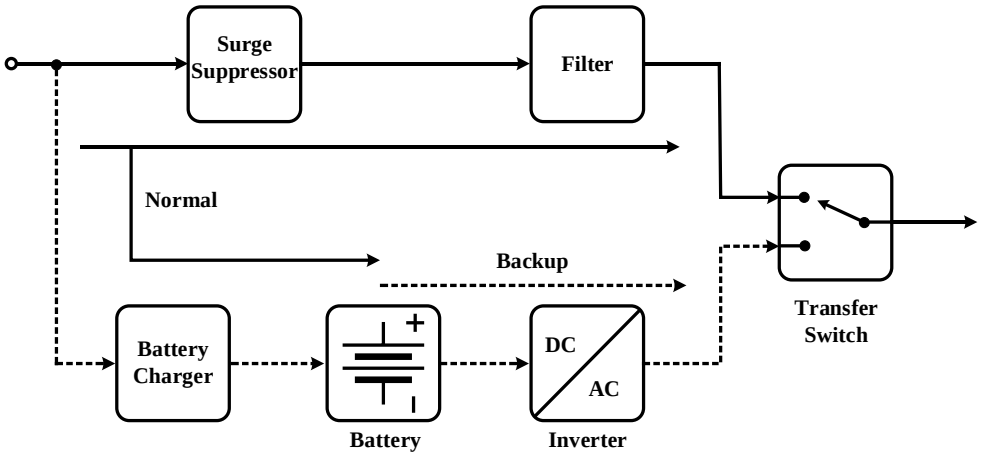


Figure 2.18: Standby UPS

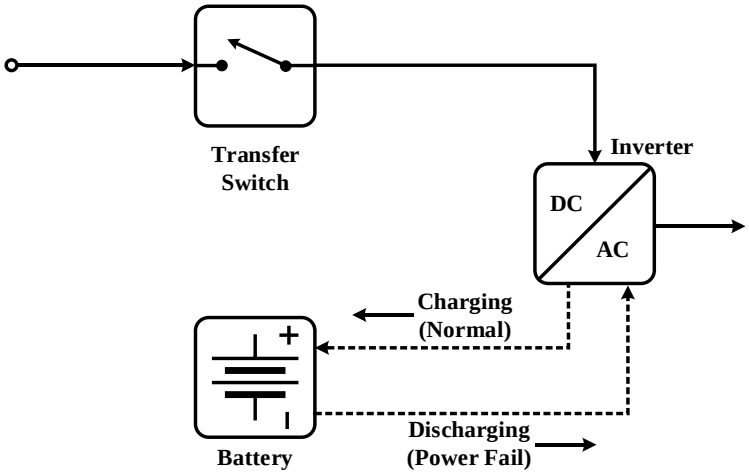


Figure 2.19: Line interactive UPS

The working principle of delta conversion online UPS is as same as Unified Power Quality Conditioner (UPQC) which can work as SAF and PAF simultaneously. The delta inverter works as a PAF and main inverter works as a SAF when required because of their parallel and series connection respectively. Due to their higher efficiency and multiple functionality delta conversion online UPS is most popular and mature technology that is being used nowadays.

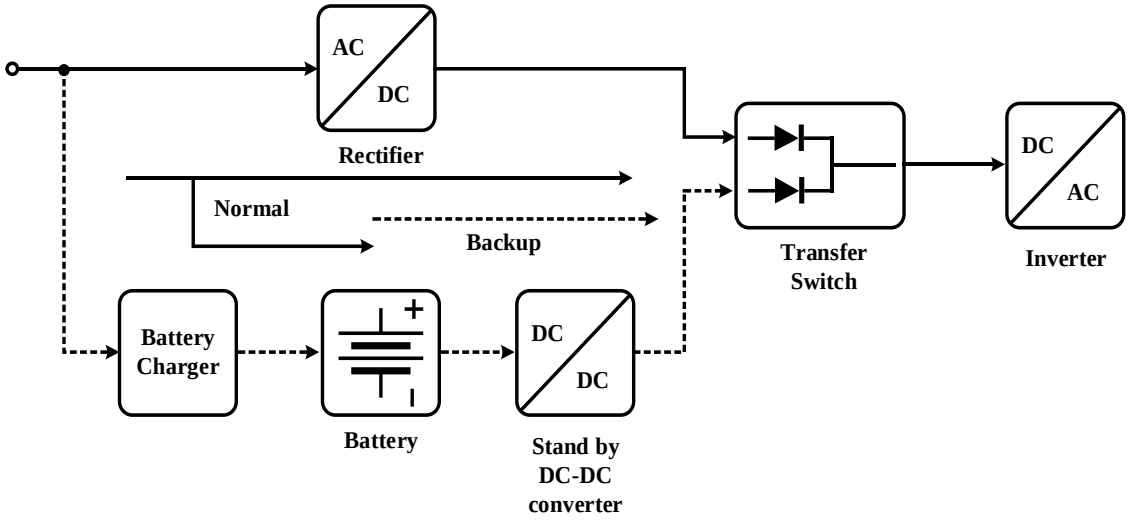


Figure 2.20: Standby online hybrid UPS

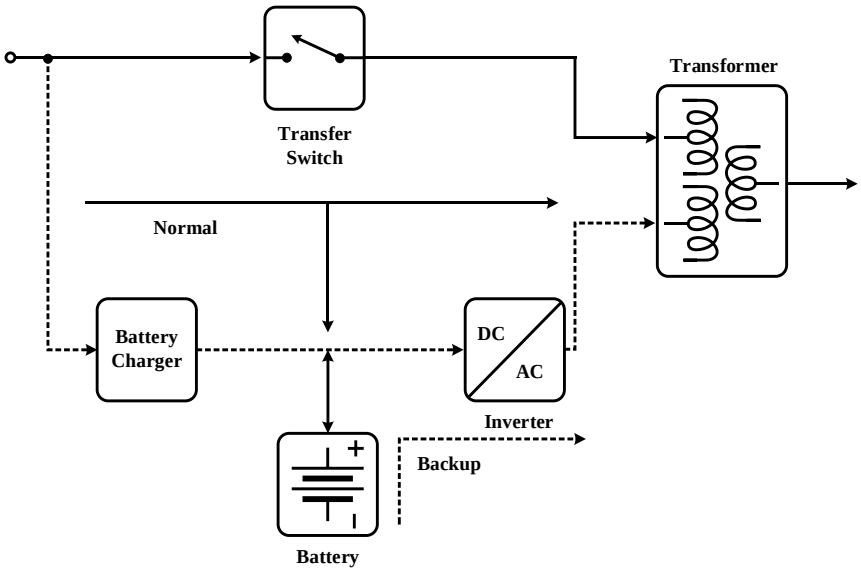


Figure 2.21: Standby ferro UPS

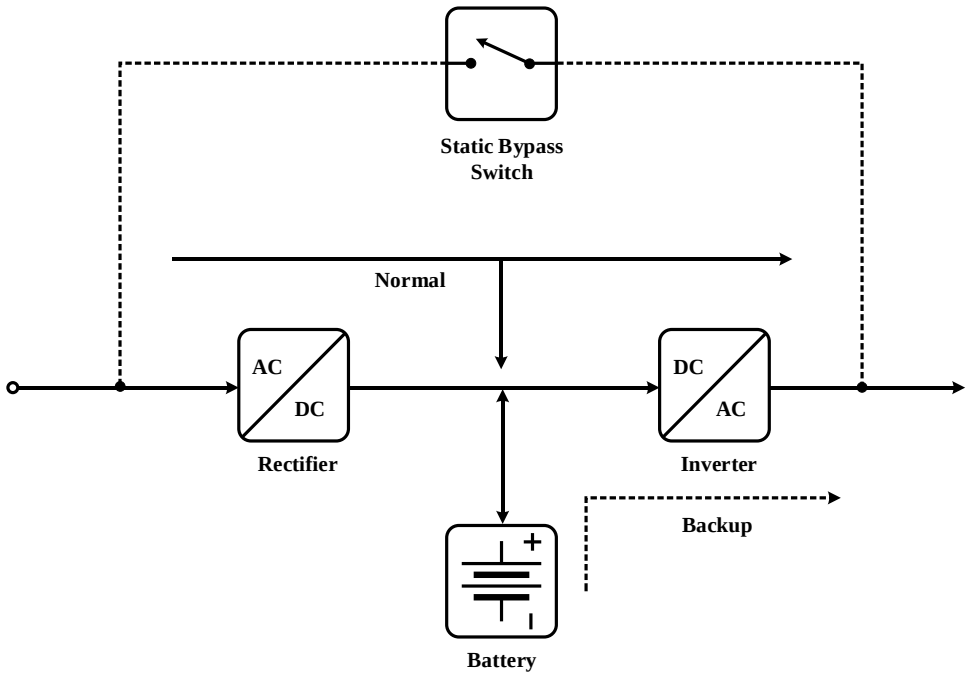


Figure 2.22: Double conversion online UPS

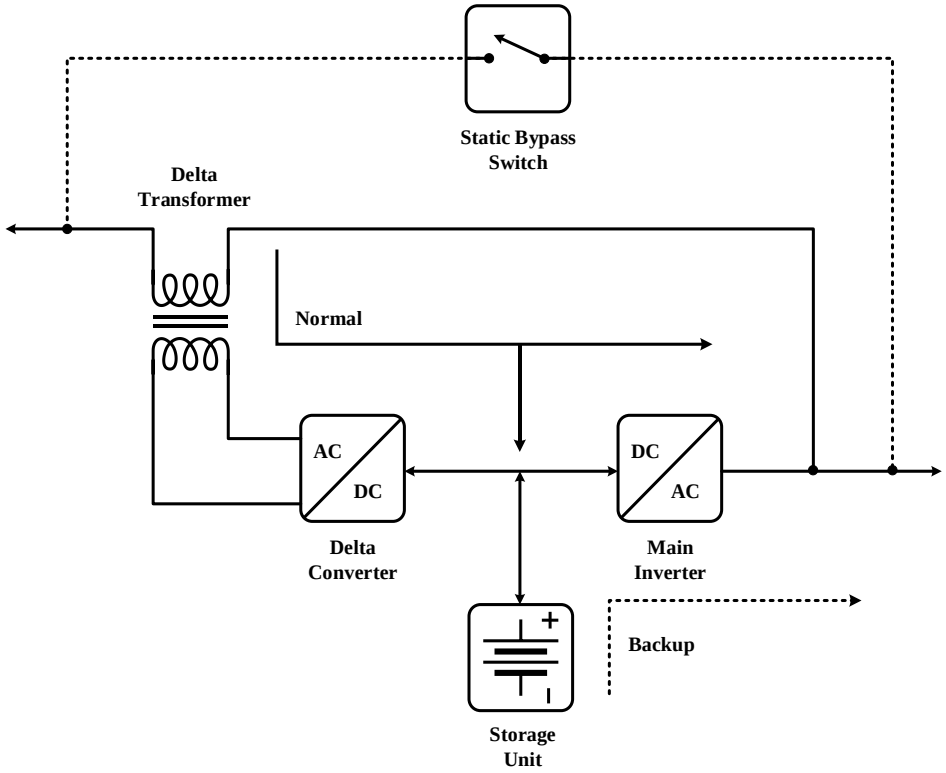


Figure 2.23: Delta conversion online UPS

CHAPTER 3: BUCK BOOST BASED DIRECT AC-AC DYNAMIC VOLTAGE REGULATOR

3.1 Introduction

The conventional DVR topology, its working principle, advantages and disadvantages were discussed in brief in previous chapter. Various AC-AC converter based topologies such as Matrix Converter (MC) and Vector Switching Converters (VeSC) are being researched and developed for eliminating the need of storage device [29-35]. A novel buck boost based AC-AC Dynamic Voltage Regulator (AC-DVR) is proposed in this chapter. The working principle, schematic of proposed architecture and its inspiration is described thoroughly in next sections.

3.2 State of The Art AC-AC Buck Boost Converter

The buck-boost converter is a matured technology being used for both DC-DC and AC-AC step up and down applications [36]. The operating principle of AC-AC buck boost converter is as same as DC-DC buck boost; only the unidirectional switches in DC-DC buck boost converter are replaced by bidirectional switches in case of AC-AC buck boost converter. The output AC voltage thus can be bucked or boosted by controlling the duty cycle D which is given by Equation 3.1 where V_{out} and V_{in} are peak or RMS value of the output and input voltages respectively. Switches T1 and T2 are operated in D while T3 and T4 are switched in $D' = 1 - D$. The inductor is charged in D and discharged in D' via C and load. The output voltage is boosted when D is greater than 0.5 and it is bucked when D is less than 0.5 as per Equation 3.1. The input AC voltage and output bucked

boosted voltages are also depicted in Figure 3.1. The inductor voltage and capacitor current characteristics are identical to the DC-DC buck boost converter. Hence, if the duty cycle is kept constant, the output follows the input shape.

$$D = \frac{V_{out}}{V_{out} + V_{in}} \tag{3.1}$$

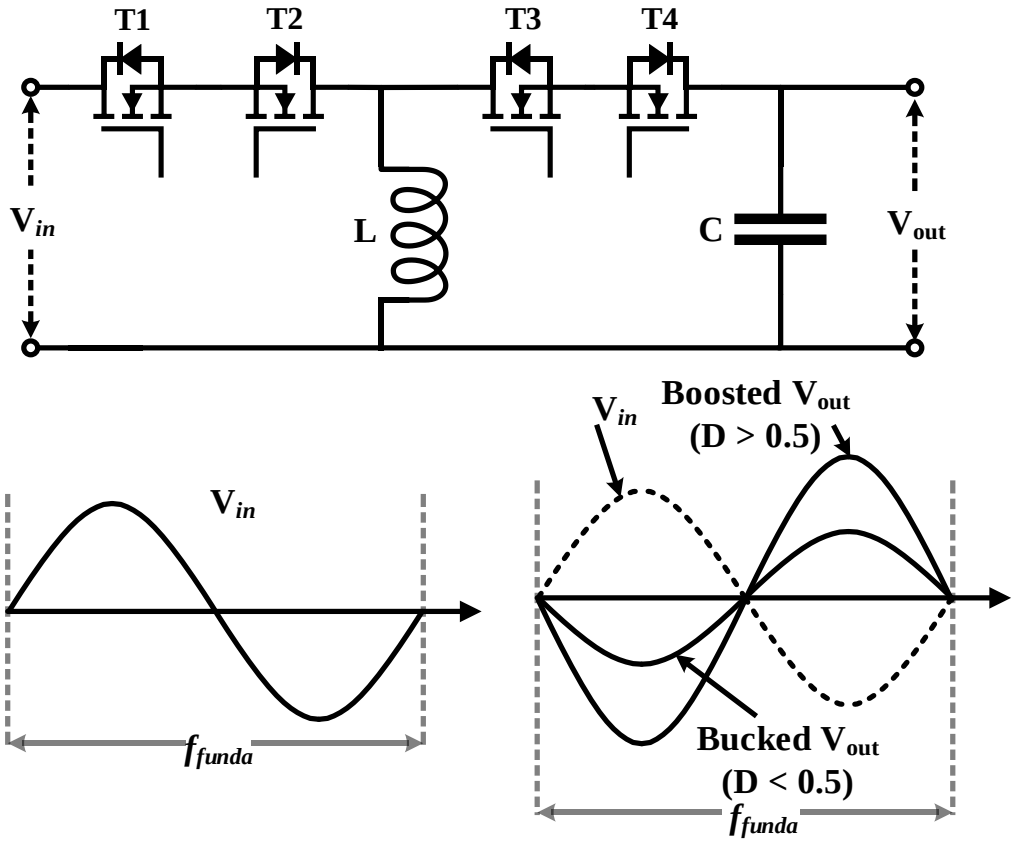


Figure 3.1: Schematic and operating principle of AC-AC buck boost converter

There are several topological improvements in AC-AC buck boost converter such as z-network converters, flyback buck boost converter, center point clamped ac-ac buck boost converter etc. [37-39]. Although, their purpose is to provide variable peak /RMS amplitude of the voltage, they can be different in terms of circuitry and operating principle. The proposed converter in this article is inspired by the buck boost converter discussed in this section and will be working on the described principle.

3.3 Microinverter for Photo Voltaic Applications

Microinverters are most commonly discussed technology for photo voltaic applications due to their advantages such as easy installation, highest yield, better reliability, etc. There are multiple technologies reported in literature for microinverter applications. The most common topology used for microinverter consists of one shaping circuit and one unfolding circuit. The shaping circuit synthesizes rectified sinusoidal voltage i.e. $|\sin(wt)|$ from available DC voltage and the unfolding bridge is then used to create $\sin(wt)$. The shaping mechanism shapes the voltage as well as takes care of Maximum Power Point Tracking (MPPT) of photo voltaic panels. The output of the bridge is then connected to AC grid via reactance to enable power transfer to the AC grid [40-42]. The simplified schematic of such technology and its operating principle is illustrated in Figure 3.2.

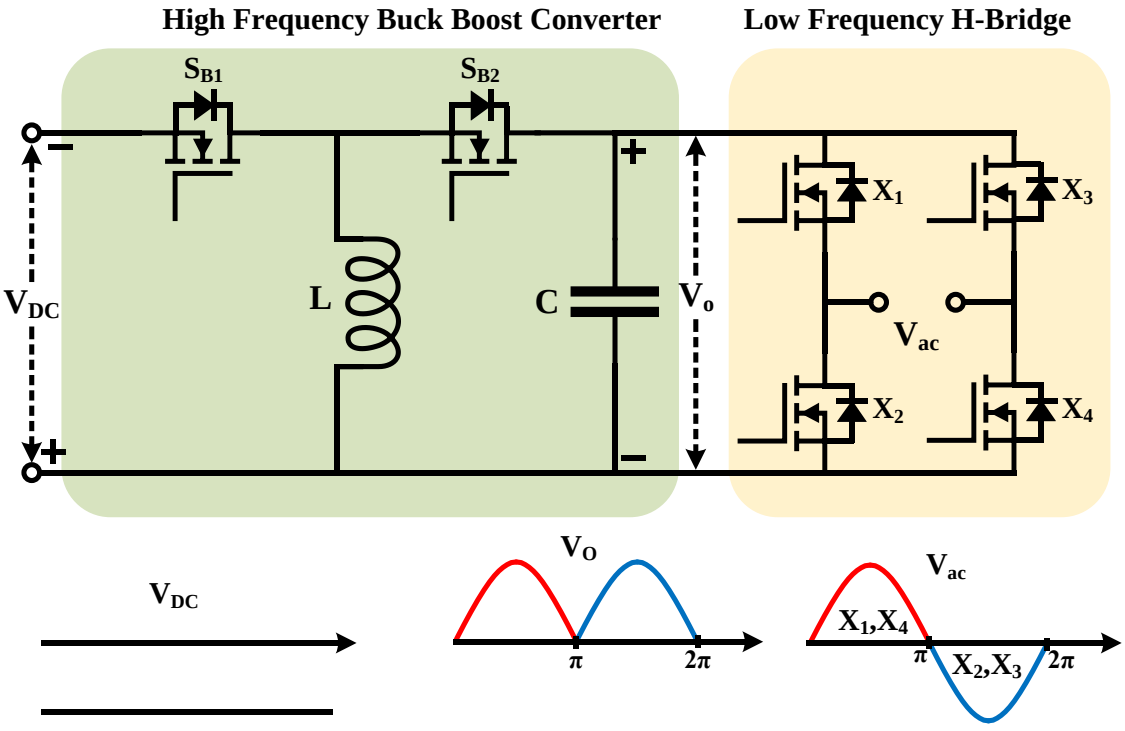


Figure 3.2: Microinverter schematic and operating principle

3.4 Buck Boost Based AC-AC Dynamic Voltage Regulator (AC-DVR)

The proposed topology of AC-DVR is designed to synthesize required AC compensation voltage from the disturbed AC source itself. To accomplish that, the AC-DVR uses a bidirectional bridge and a wave shaping circuit just as the microinverter topology. As discussed earlier, the microinverter topology may use DC-DC buck boost converter as wave shaper because input of the microinverter is always DC (PV module). To serve the same purpose of wave shaping, the proposed AC-DVR uses direct AC-AC buck boost converter as both input and output of the converter is going to be AC. For the same reason, the unfolding H-bridge in microinverter is replaced by bidirectional bridge in case of AC-DVR. The schematic of the proposed system is illustrated in Figure 3.3 while its connection with AC source and load is depicted in Figure 3.4.

The AC-DVR is connected in parallel-series connection as SVR (Static Voltage Regulator). The input to the AC-DVR is the AC source and the generated load compensation voltage is added in series with the AC supply via series transformer as shown in Figure 3.4. The bidirectional bridge is consisting of four bidirectional switches viz. Q1Q2', Q2Q1', Q3Q4' and Q4Q3' which can be MOSFETs or IGBTs. The sensing unit senses the input voltage and identifies the phase (in phase or out of phase), magnitude and frequency of the compensation voltage. The bidirectional bridge gets gating signals from sensing unit and changes the frequency of input voltage to frequency of compensation voltage. The output of the bidirectional bridge is then given to the high frequency AC-AC buck boost converter or wave shaper to synthesize the shape of the desired compensation voltage. The wave shaper consists a similar construction as AC-AC buck boost converter i.e. two bidirectional switches namely S1S2 and S3S4, an inductor

and a capacitor. The working principle of wave shaper is as same as AC-AC buck boost converter i.e. S1S2 is operated in duty cycle D and S3S4 is operated in D'. The only difference is the generation of dedicated duty cycle D. As the output of the AC-AC buck boost is always out of phase with input, if the compensation voltage required to be out of phase, the bidirectional bridge synthesizes in phase voltage and vice versa.

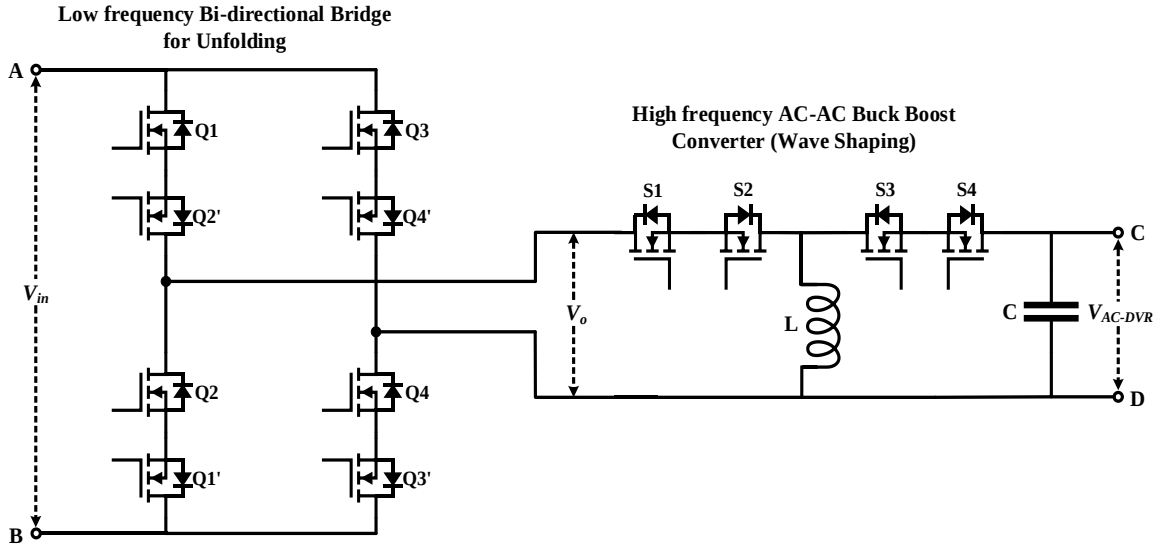


Figure 3.3: Proposed buck boost based AC-AC Dynamic Voltage Regulator (AC-DVR)

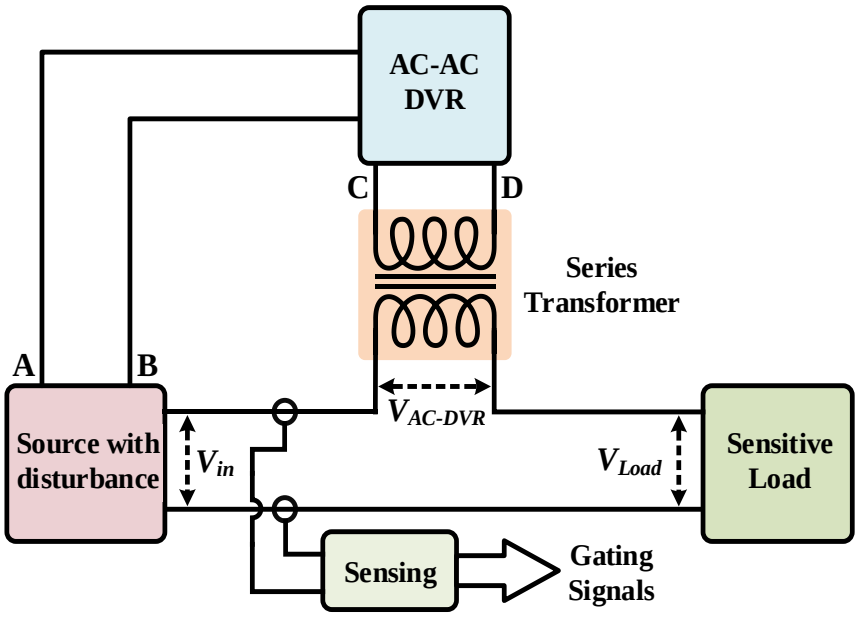


Figure 3.4: AC-DVR connection with source and load

3.5 Operating Principle of AC-DVR

The detailed schematic of proposed AC-DVR and its connection with AC source and load is illustrated in Figure 3.5. The operating principle of the AC-DVR for 3rd harmonic mitigation, 5th harmonic mitigation, swell/overvoltage mitigation and sag/undervoltage mitigation is tabulated in Table 3.1 along with waveforms at various nodes and switching instances for bidirectional bridge.

The first example shows the AC input with the presence of third harmonic voltage. Hence, to compensate load voltage and make it fine sinusoidal, the AC-DVR should inject 180° out of phase third harmonic voltage with same magnitude. As the AC-AC buck boost/wave shaper's output is always 180° out of phase with the input, the input of the wave shaper should be positive when the required output is negative. Hence, the bidirectional bridge changes the frequency and the phase of input voltage from fundamental to third harmonic frequency which is three times the fundamental as shown in Table 3.1. The wave shaper changes the shape of its input voltage to its desired stage and synthesized voltage is then injected in series via series transformer. Thus, the load voltage is compensated and its shape is restored to fundamental sine wave. The switching of the bidirectional bridge to synthesize such voltage is also tabulated in Table 3.1. The AC source containing fifth harmonic voltage is shown as next example in Table 3.1. The sensing circuit senses the fifth harmonic voltage and thus switches the bidirectional switches of the bridge to change the frequency of the input by five times of fundamental. As the fifth harmonic has to be eliminated and wave shaper's output will be 180° out of phase; when the output needed to be negative, the bridge synthesizes positive voltage from the AC source as shown in Table 3.1. The wave shaper then changes the shape of

the input to fifth harmonic voltage i.e. sinusoidal. This voltage is injected in series with the AC source via series transformer thus compensating the load voltage.

The effect of voltage sag/overvoltage is tabulated as example three in Table 3.1. The extra voltage that is present in the grid must be subtracted for load voltage compensation. Hence 180° out of phase voltage at fundamental frequency should be injected by AC-DVR. Hence, as the output of the wave shaper will be out of phase with input, the bidirectional bridge does not change the phase of the input and provides the same voltage at same phase at the input of wave shaper. The wave shaper synthesizes the appropriate voltage amplitude at 180° out of phase which is added to the input via series injection transformer. Hence the load is provided by fine sinusoidal voltage.

The AC source experiencing voltage sag/undervoltage is shown as final example in Table 3.1. The appropriate amount of voltage is needed to be added in order to compensate the load voltage. Hence, the bidirectional bridge changes the phase of input/source voltage by 180° at the input of wave shaper. The AC-AC buck boost converter then synthesizes appropriate voltage magnitude at fundamental frequency which is needed to be added by AC-DVR. The synthesized voltage is injected in series via transformer therefore restoring the load voltage at its predefined value.

The operating principle of AC-DVR for various voltage disturbances is briefly described in previous passages. Apart from third and fifth harmonic voltage, the proposed AC-DVR is also capable of synthesizing voltage at different frequencies using the same operating principle if the zero crossing points of input and output voltages matches. Apart from that, the ability of synthesizing various frequencies may also depend on the converter bandwidth i.e. switching frequency for better and effective performance.

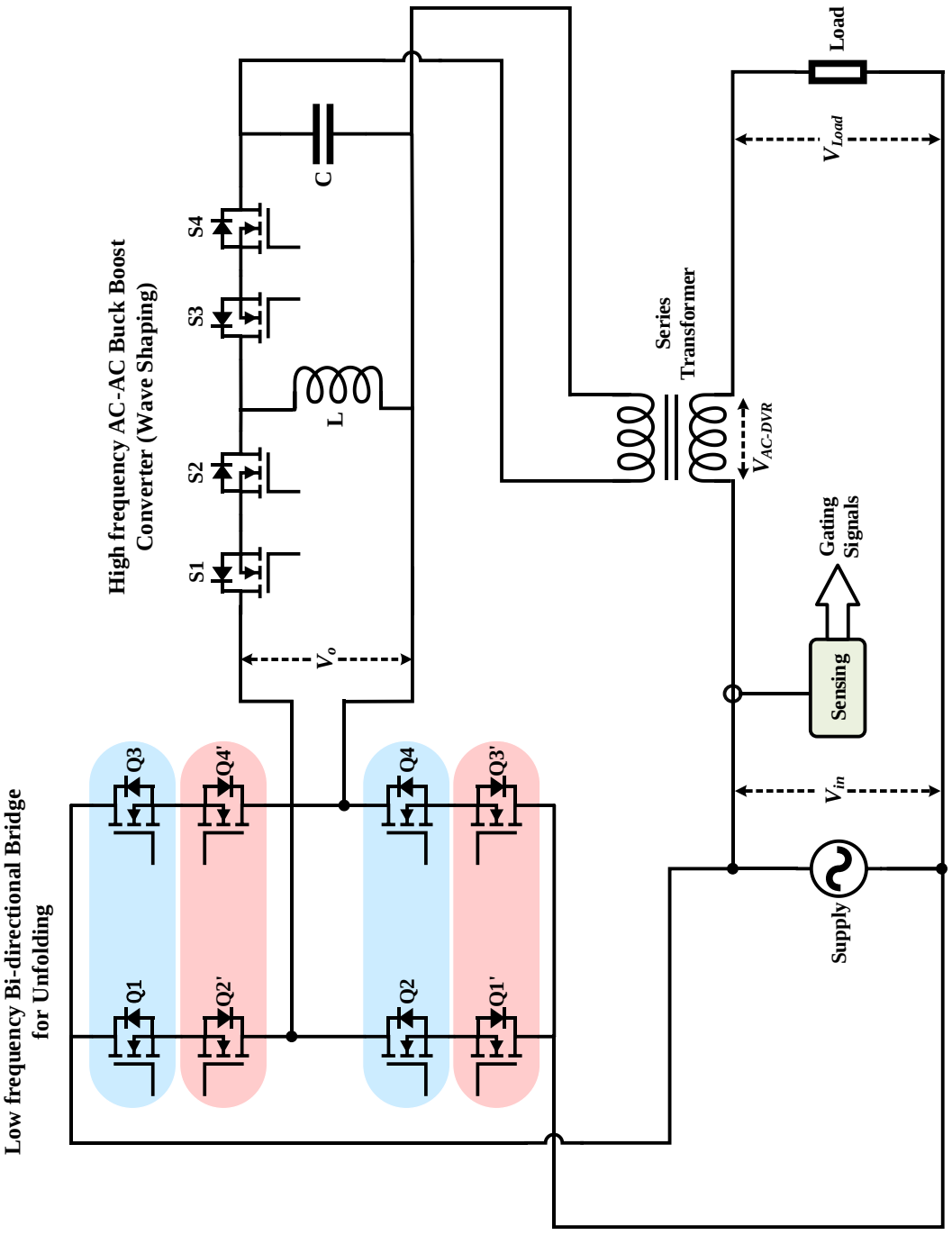


Figure 3.5 Detailed schematic of buck boost based AC-AC Dynamic Voltage Regulator (AC-DVR)

Table 3.1: Operating principle of AC-DVR for various voltage disturbances

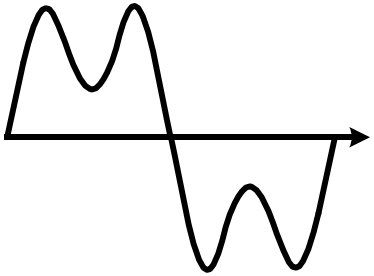
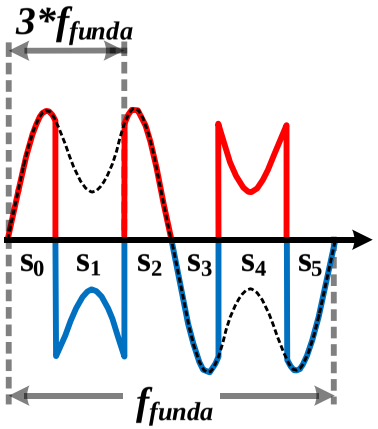
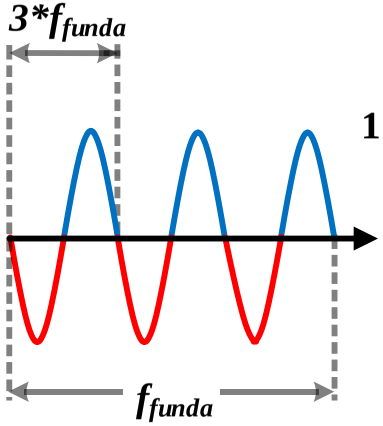
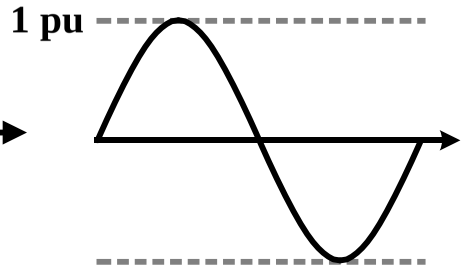
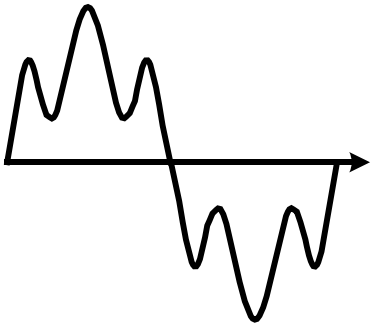
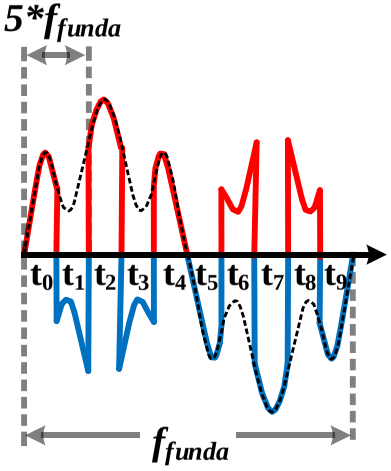
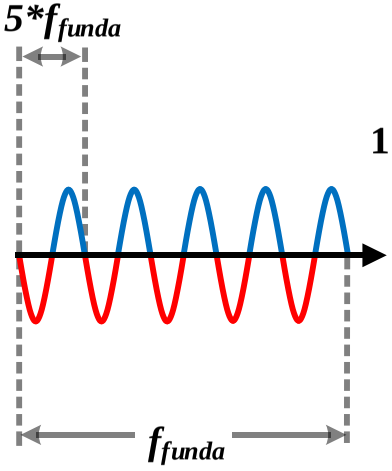
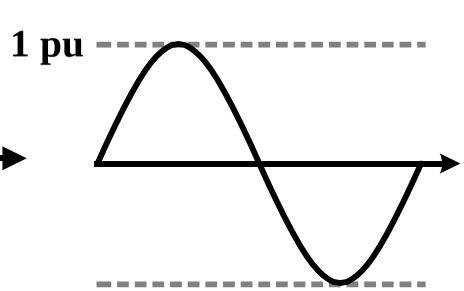
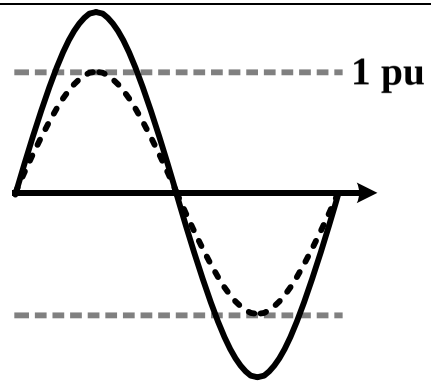
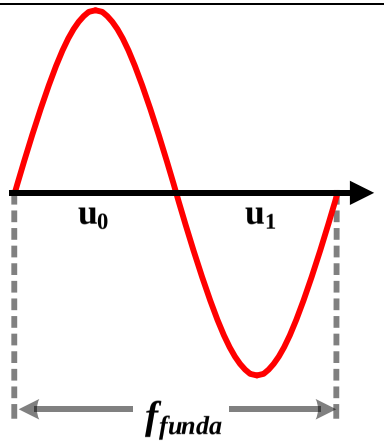
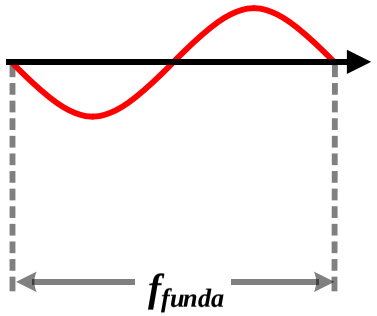
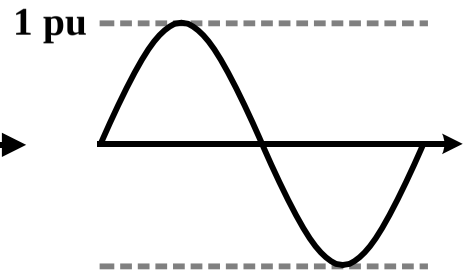
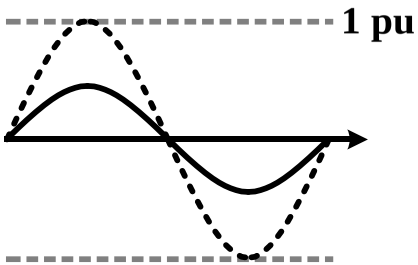
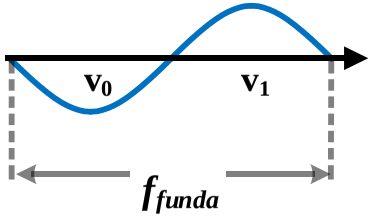
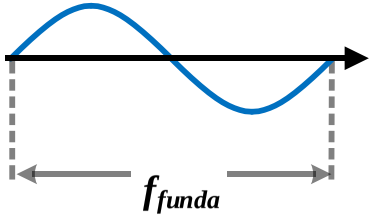
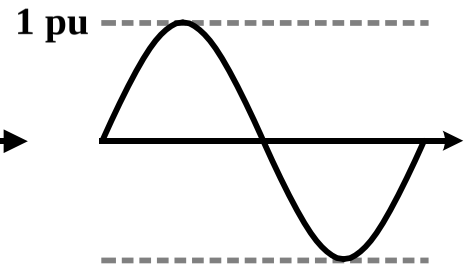
V_{in}	V_o	V_{AC-DVR}	$V_{Load} = V_{in} + V_{AC-DVR}$
			
			

Table 3.1 (continued)

V_{in}	V_o	V_{AC-DVR}	$V_{Load} = V_{in} + V_{AC-DVR}$
			
			

Timing Intervals and Switch Conduction:

s_0: Q1Q4, s_1: Q2Q3, s_2: Q1Q4, s_3: Q2'Q3', s_4: Q1'Q4', s_5: Q2'Q3', t_0: Q1Q4, t_1: Q2Q3, t_2: Q1Q4, t_3: Q2Q3, t_4: Q1Q4, t_5: Q2'Q3', t_6: Q1'Q4', t_7: Q2'Q3', t_8: Q1'Q4', t_9: Q2'Q3', u_0: Q1Q4, u_1: Q2'Q3', v_0: Q2Q3, v_1: Q1'Q4'.

CHAPTER 4: ANALYSIS, DESIGN AND CONTROL OF AC-DVR

4.1 Introduction

This chapter presents the analysis of proposed AC-AC Dynamic Voltage Regulator along with inductor and capacitor design. The duty cycle derivation is presented in Section 4.2. Section 4.3 and Section 4.4 discusses the design of inductor and capacitor based on power calculations. Overall control architecture of proposed AC-AC Dynamic Voltage Regulator is explained in Section 4.5.

4.2 Duty Cycle Derivation

The duty cycle equation for DC-DC buck boost converter is well known and presented in Eq. (1) in section 5. In case of AC-AC buck boost converter where the frequency of input and output voltage is same, the duty cycle is given by:

$$D = \frac{V_{out}}{V_{in} + V_{out}} \tag{2}$$

The major difference in this duty cycle equation is that the values V_{out} and V_{in} are the peak or RMS value of the output voltage and input voltage respectively. The wave shaper proposed in this article synthesizes different frequency output from the fundamental frequency of the input. Hence, the duty cycle of the wave shaper should contain information of both magnitude and shape of both input and output voltages.

Let w_1 and w_2 be the frequencies of input and output voltages respectively and; V_{m1} and V_{m2} be the magnitudes of input and output voltages respectively. Hence, the instantaneous voltages of input and output can be given by:

$$V_{in} = V_{m1} \sin(w_1 t) \tag{3}$$

$$V_{out} = V_{m2} \sin(w_2 t) \tag{4}$$

The volt-second balance on inductor voltage is applied over a switching frequency in case of DC-DC buck converter or AC-AC buck boost converter where frequencies of input and output is same. In case of different frequencies, the volt-second balance should be applied over the fundamental frequency i.e. the input frequency. Thus, volt-second balance of inductor voltage can be presented as:

$$\frac{T_f(DV_{in}T_s + D'V_{out}T_s)}{T_s T_f} = 0 \tag{5}$$

$$DV_{in} + D'V_{out} = 0 \tag{6}$$

$$DV_{m1} \sin(w_1 t) + D'V_{m2} \sin(w_2 t) = 0 \tag{7}$$

$$D = \frac{V_{m2} \sin(w_2 t)}{V_{m1} \sin(w_1 t) + V_{m2} \sin(w_2 t)} \tag{8}$$

Where;

T_s= Period of switching frequency = $1/f_s$

T_f= Period of fundamental frequency = $1/f_f$

This equation provides instantaneous information about both shape and magnitude of the input and output voltages. The duty cycle cannot be negative and hence only the positive values of the voltages should be considered for the generation of instantaneous duty cycle. Thus, Eq. (8) can be re-written as:

$$D\ (t) = \frac{V_{m2}|\sin(w_2 t)\,|}{V_{m1}|\sin(w_1 t)\,| + V_{m2}|\sin(w_2 t)|} \quad (9)$$

The bidirectional bridge changes the phase of the input voltage according to the phase of required output voltage as discussed in section 3.5. As the duty cycle equation only contains the positive values i.e. mode of the signal; the phase change imposed by bidirectional bridge does not impact the equation of duty cycle.

This duty cycle is fed to the comparator for PWM pulses generation. The switches S1S2 are operated in duty cycle D and S3S4 are switched in D'.

4.3 Source Power and AC-DVR Current

As shown in Figure 3.5, source voltage is denoted by V_{in} which can be written as a fundamental component V_f and error voltage component V_e. The error voltage can be a harmonic component at any harmonic frequency or sag or swell component at fundamental frequency. Thus, the instantaneous source voltage can be written as:

$$V_{in}(t) = V_f(t) + V_e(t) \quad (10)$$

The source current is denoted by I_{in} in Figure 3.5. As the proposed AC-AC DVR injects the error voltage in series with the disturbed source, the load voltage is always fundamental and so does the load current. Hence, the instantaneous source current can be written as:

$$I_{in}(t) = I_{Load}(t) + I_{AC-DVR}(t) \quad (11)$$

$$I_{in}(t) = I_f(t) + I_{AC-DVR}(t) \quad (12)$$

Equating the input and output power,

$$V_{in}(t)I_{in}(t) = V_{Load}(t)I_{Load}(t) \quad (13)$$

$$\big(V_f(t) + V_e(t)\big)\big(I_f(t) + I_{AC-DVR}(t)\big) = V_f(t)I_f(t) \quad (14)$$

$$V_f(t)I_f(t) + V_f(t)I_{AC-DVR}(t) + V_e(t)I_f(t) + V_e(t)I_{AC-DVR}(t) = V_f(t)I_f(t) \quad (15)$$

$$I_{AC-DVR}(t)\left(V_f(t) + V_e(t)\right) + V_e(t)I_f(t) = 0 \quad (16)$$

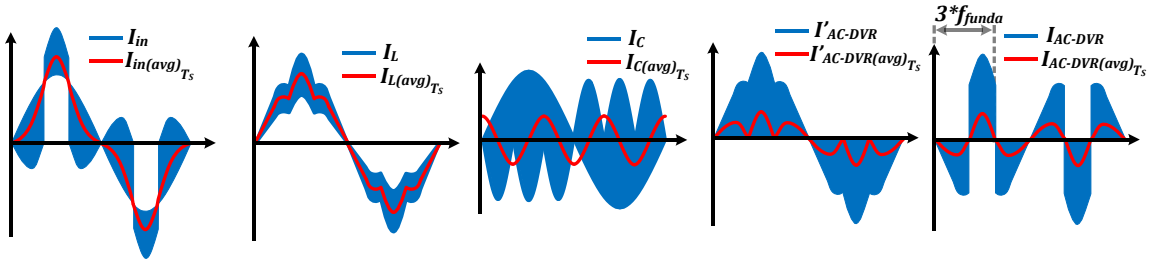
$$I_{AC-DVR}(t)\left(V_f(t) + V_e(t)\right) = -V_e(t)I_f(t) \quad (17)$$

$$I_{AC-DVR}(t) = \frac{-V_e(t)I_f(t)}{\left(V_f(t) + V_e(t)\right)} \quad (18)$$

Hence, the input current of AC-DVR is given by Eq. (18). This equation presents the information of both shape and magnitude of the input current of AC-DVR. Also, this current enables the sinusoidal power extraction from the source irrespective of the type of disturbance in the source.

4.4 Inductor and Capacitor Design

The source current and input current of AC-DVR under third harmonic disturbance are depicted in Figure 5(a) and 5(e) respectively. The input current of AC-AC buck boost converter for third harmonic compensation is depicted in Figure 5(d). It can be noted that the input current of AC-AC buck boost has the same shape as input current of AC-DVR except its polarity due to the switching of bidirectional bridge. The relation between the input current of AC-AC buck boost, average inductor current (over switching cycle), average capacitor current and output current of AC-AC buck boost can be given by Eq. (19) by applying KCL. Although, the polarity of I'_{AC-DVR}will be different from I_{AC-DVR}, the peak value of I'_{AC-DVR} can be determined by the peak value of I_{AC-DVR}. Hence the peak average inductor current can be determined by using Eq. (18-21) and inductor can be designed as per Eq. (22) whereas capacitor can be designed as per Eq. (20). However, inductor and capacitor values used for simulation and experimental results are empirical values obtained from number of simulations.



(a) (b) (c) (d) (e)

Figure 4.1: Actual (switched) and average current waveforms (a) Source current, (b) Inductor current, (c) capacitor current, (d) Wave shaper input current, (e) AC-DVR input current

$$I'_{AC-DVR} = I_{L(avg)} + I_{C(Avg)} + I_f \tag{19}$$

$$C = I_{out} DT_s / 2\Delta V_e = I_f DT_s / 2\Delta V_e \tag{20}$$

$$I_{C(Avg)} = -V_e / wc \tag{21}$$

$$L = V_{in} DT_s / 2\Delta I_L \tag{22}$$

4.5 Control Algorithm for Proposed AC-DVR

The overall control block diagram for proposed AC-DVR is depicted in Figure 4.2. As it can be seen from the block diagram, the source voltage V_{in} is sensed and wt is obtained via PLL. The OSR (Original Signal Reconstruction) block is used to recreate the sensed signal because output of PLL sometimes oscillates at zero crossing points [43]. As it can be seen from duty cycle equation presented in Eq. (9) that zero crossing point locking is very important for the duty cycle. A small oscillation at zero crossing point can cause major distortion in duty cycle. Hence, OSR block is used to recreate the sensed signal using wt obtained from PLL. The block diagram of OSR block is presented in Figure 4.3. It consists of different fourier blocks. The generalized block diagram of fourier block is depicted in Figure 4.4. The fourier block gives information about magnitude and phase of frequency of interest. These information is used to recreate any

harmonic component that present in the sensed signal. Fourier blocks for fundamental, 3rd harmonic, 5th harmonic, 7th harmonic, 9th harmonic, 11th harmonic and 13th harmonic are used to obtain as much information possible from sensed signal. The magnitude obtained from the fundamental fourier block is compare to a constant of 120 V RMS to maintain the load voltage at 120 V RMS with only fundamental. Any other frequency components and error voltage obtained from fundamental voltage magnitude comparison is considered as compensation voltage. This compensation voltage signal works as a reference for AC-DVR. Whereas, the original signal is reconstructed from the information obtained from fourier blocks. The block diagram presented in Figure 4.3 gives better understanding of original signal reconstruction and AC-DVR reference generation algorithm. The AC-DVR refence and recreated sensed signal V_{in-rc} is then used to generate duty cycle and gate pulses for bidirectional switches.

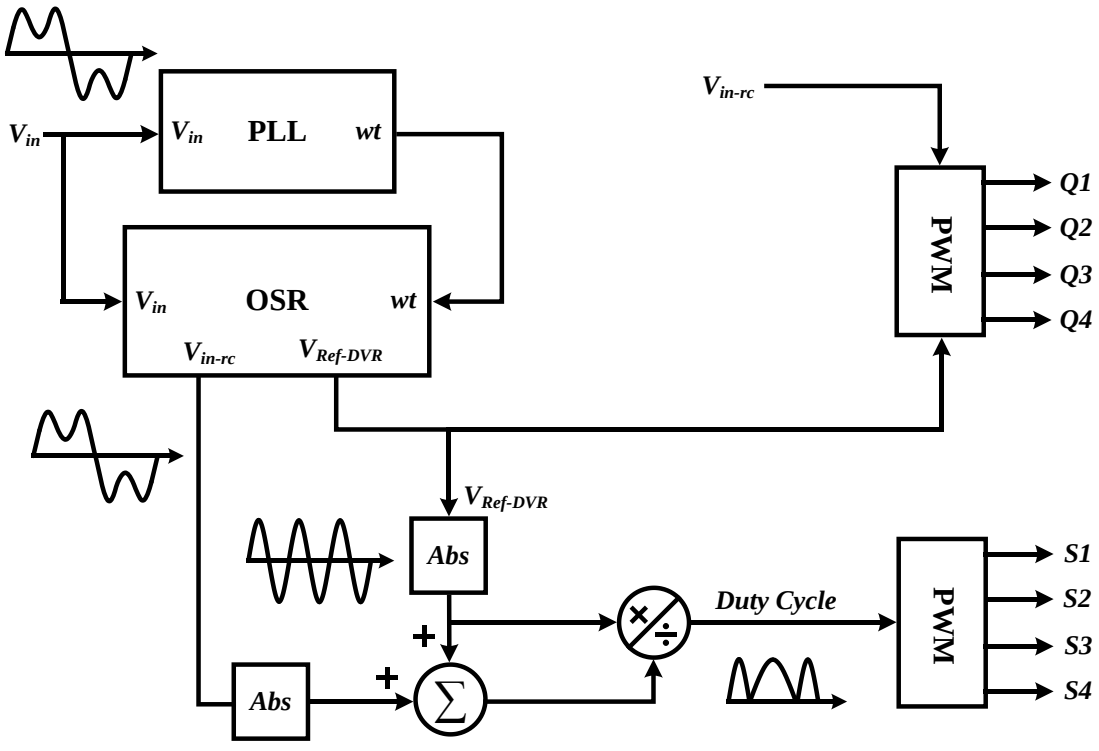


Figure 4.2 Control block diagram for proposed AC-AC DVR

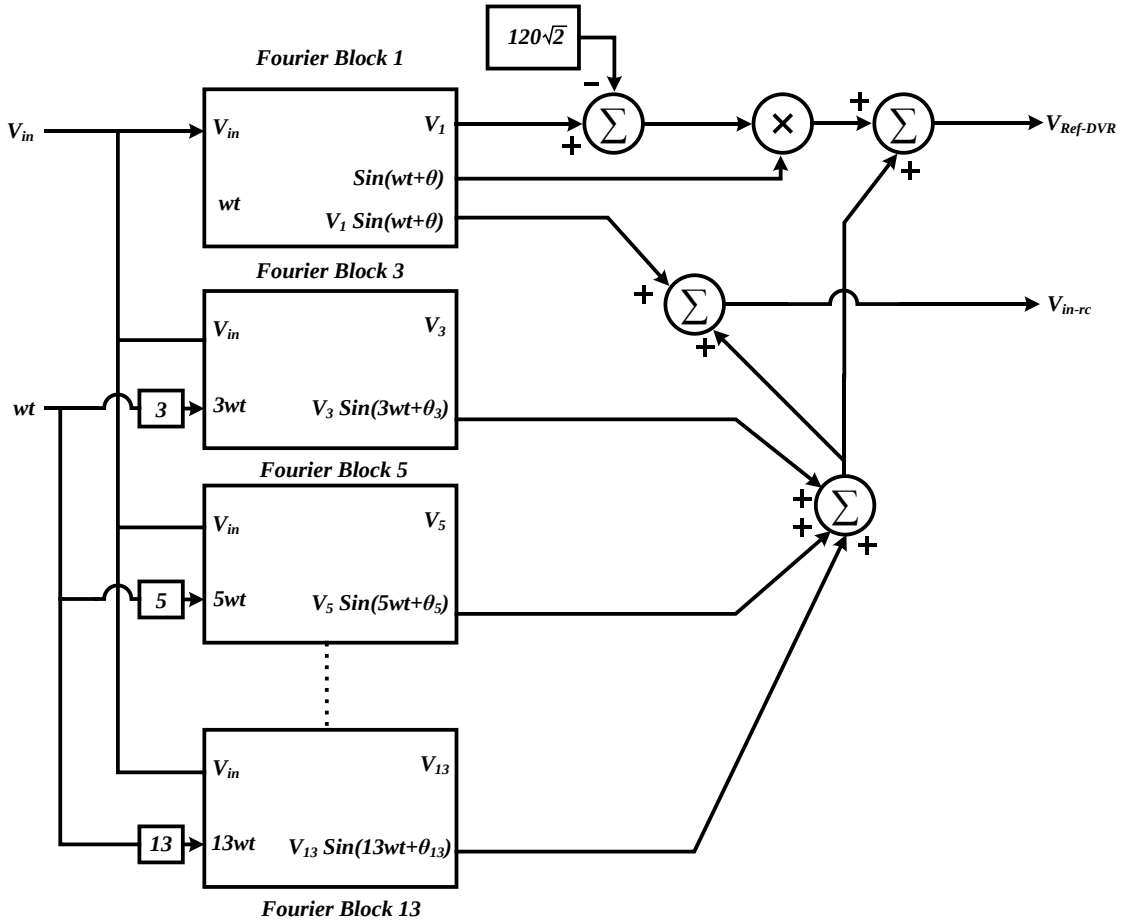


Figure 4.3: Block diagram of OSR (Original Signal Reconstruction) block

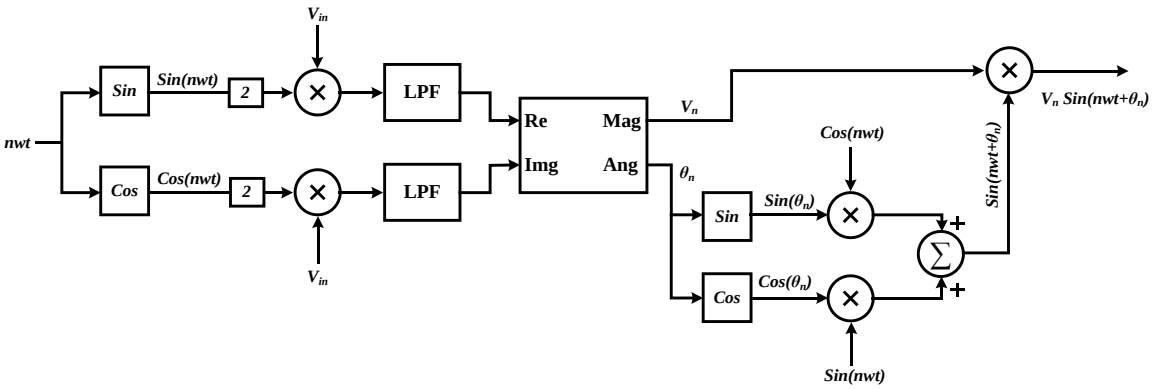


Figure 4.4: Block diagram of Fourier blocks

CHAPTER 5: MODELLING OF DIRECT AC-AC DYNAMIC VOLTAGE REGULATOR

5.1 Introduction

This chapter presents the modelling of direct AC-AC Dynamic Voltage Regulator (AC-DVR). The overall system architecture described in Figure 3.4 and Figure 3.5 and control strategy discussed in chapter 4 were modelled in MATLAB/Simulink platform and are discussed thoroughly in this chapter. Moreover, different blocks that are used to model the overall system are also presented and discussed in brief.

5.2 Model of Overall System Architecture

A complete model of AC-AC Dynamic Voltage Regulator (AC-DVR) along with its connection with source and load is shown in Figure 5.1. As discussed it chapter 3 and presented in Figure 3.4, the AC-DVR is connected in series parallel connection. The input to the AC-DVR is the source and compensation voltage generated by AC-DVR is added in series with source and load via series transformer. The nominal source parameters are set to 120V RMS and 60 Hz and the system was designed for 1-1.5 kVA operation. The performance of AC-DVR is evaluated under different operating scenarios including sag, swell, harmonics and step load changes and relative voltages, currents and power are measured using scopes block. The modelling of source, bidirectional bridge and AC-AC buck boost converter and overall control architecture is presented and discussed in following sections.

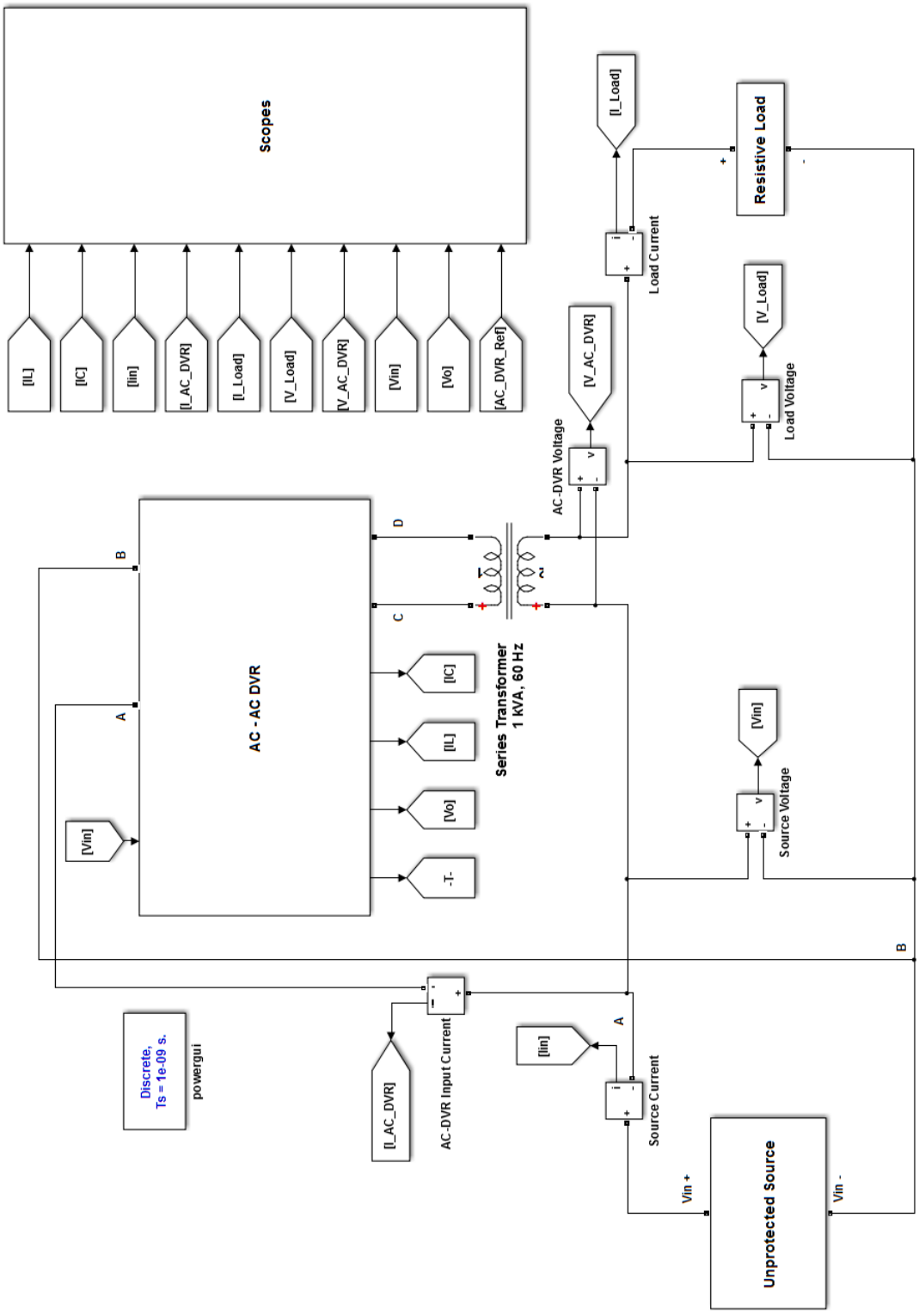


Figure 5.1: Model of overall system including unprotected source, load and proposed AC-DVR

5.3 Model of Unprotected Source

To evaluate the performance and ability of AC-DVR to restore load voltage under both normal and abnormal source conditions, the source must be modelled as controllable voltage source which can be modified to have disturbances such as harmonics, sag and swell. Thus, the source is modelled by using controlled voltage source block which can convert user defined wave shapes into voltage. The input to this block is given by sine blocks as shown in Figure 5.2. These sine blocks are modelled for fundamental component which is set to 120V RMS at 60 Hz and harmonics components mainly 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th} and 13^{th} at their respective frequencies. The magnitude of fundamental block is changed to create voltage sag and swell type of disturbances whereas magnitudes of harmonic blocks are changes to create harmonic disturbances in source voltage. In addition, repeating sequence block has been utilized to model UNC Charlotte's voltage.

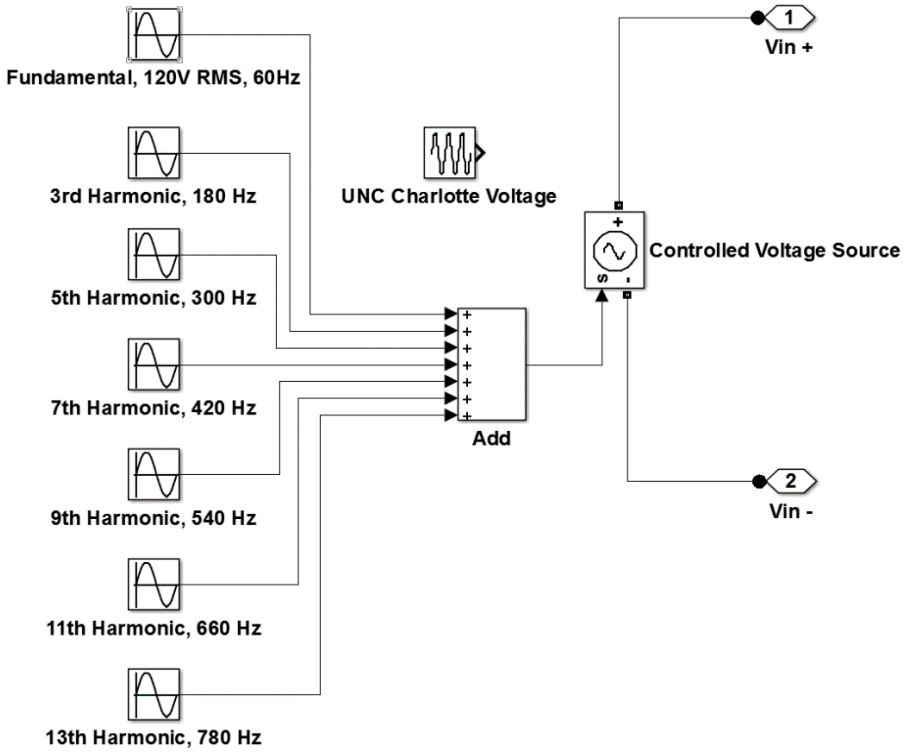


Figure 5.2: Model of unprotected source

5.4 Model of AC-AC Dynamic Voltage Regulator (AC-DVR)

The model of AC-AC Dynamic Voltage Regulator (AC-DVR) comprises low frequency bidirectional bridge and high frequency AC-AC buck boost converter (wave shaper) as shown in Figure 5.3. The AC source is the input to bidirectional bridge and wave shaper is connected at the output of bidirectional bridge. The output of wave shaper is connected to the primary of series transformer. Figure 5.4 shows the model of the bidirectional bridge. The bidirectional switches of the bridge are modelled by using two IGBT/Diode blocks with their emitters shorted and are connected in a similar manner as discussed in chapter 3 and presented in Figure 3.4. The bidirectional switches are operated by the control block shown in Figure 5.4. The detailed modelling of the bidirectional bridge control block is depicted in Figure 5.5. The control block uses measured source voltage and AC-DVR reference to operate the bidirectional switches of the bridge as discussed in chapter 4. The detailed model of high frequency AC-AC buck boost converter is presented in Figure 5.6 along with duty cycle and AC-DVR reference generation block and gate pulses generation block. The bidirectional switches of wave shaper are modelled in a similar manner as bidirectional bridge. The input terminals of wave shaper are connected to the output of bidirectional bridge and output terminals are connected to the primary of series transformer as discussed in chapter 3 and presented in Figure 3.5. The detailed model of duty cycle generation block is presented in Figure 5.7. The PLL for 120V 60 Hz reference generation and logic behind duty cycle and AC-DVR reference generation is implemented as discussed in chapter 4. The gate pulses for bidirectional switches of the wave shaper are modelled by similar logic as discussed in chapter 4 and the logic is shown in Figure 5.8.

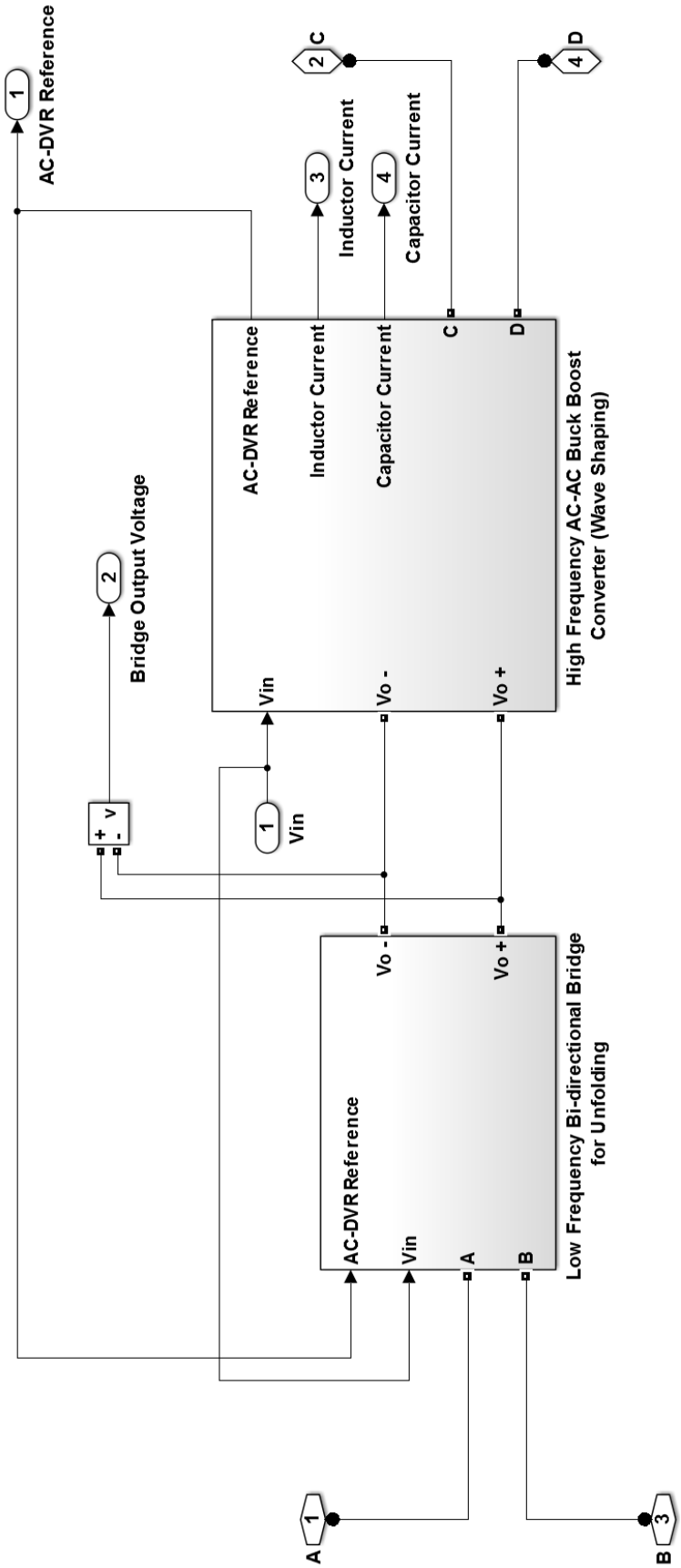


Figure 5.3: Model of proposed AC-DVR system architecture including Low Frequency Bidirectional Bridge and high frequency AC-AC buck boost converter

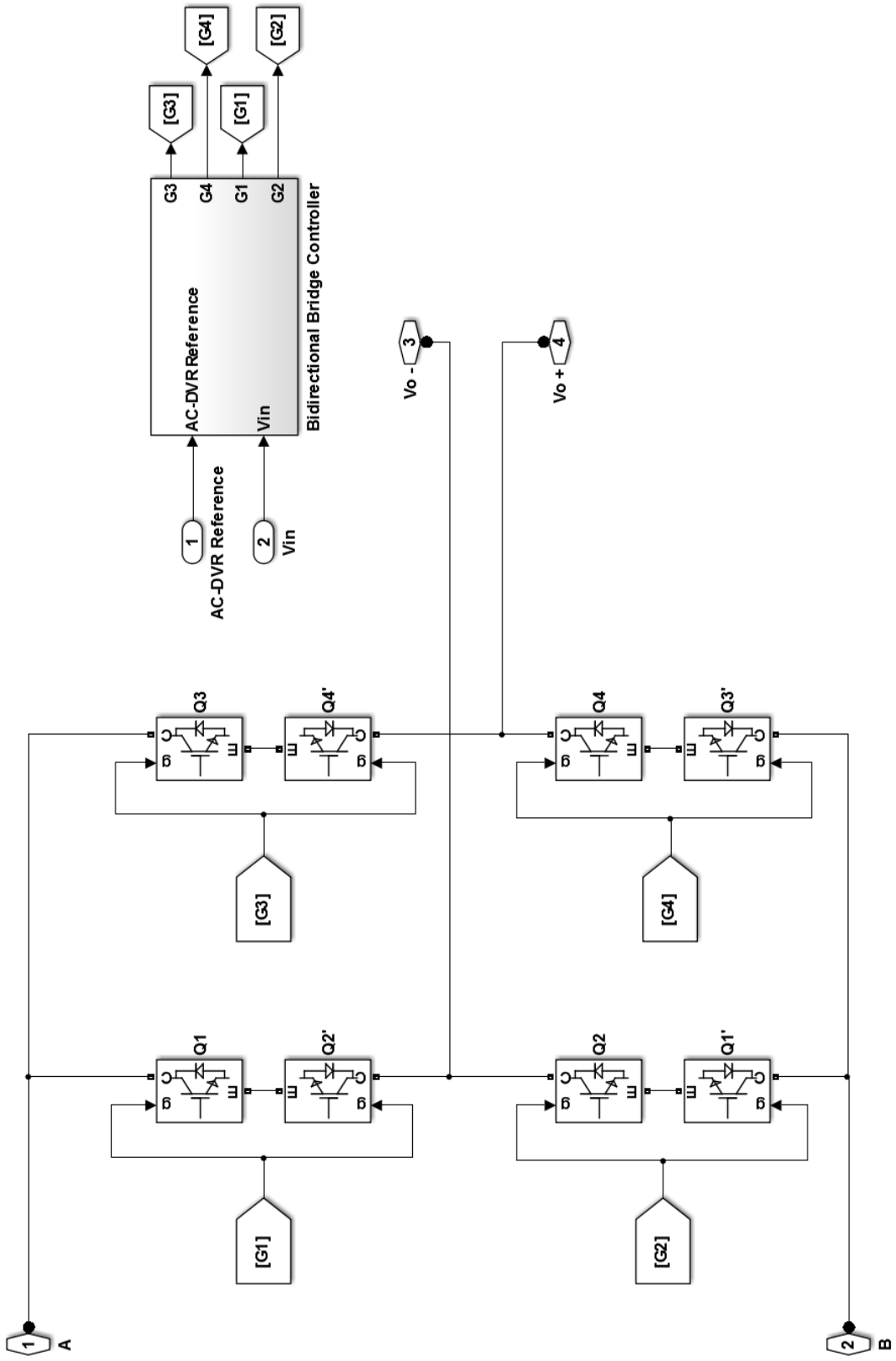


Figure 5.4: Model of low frequency bidirectional bridge and controller

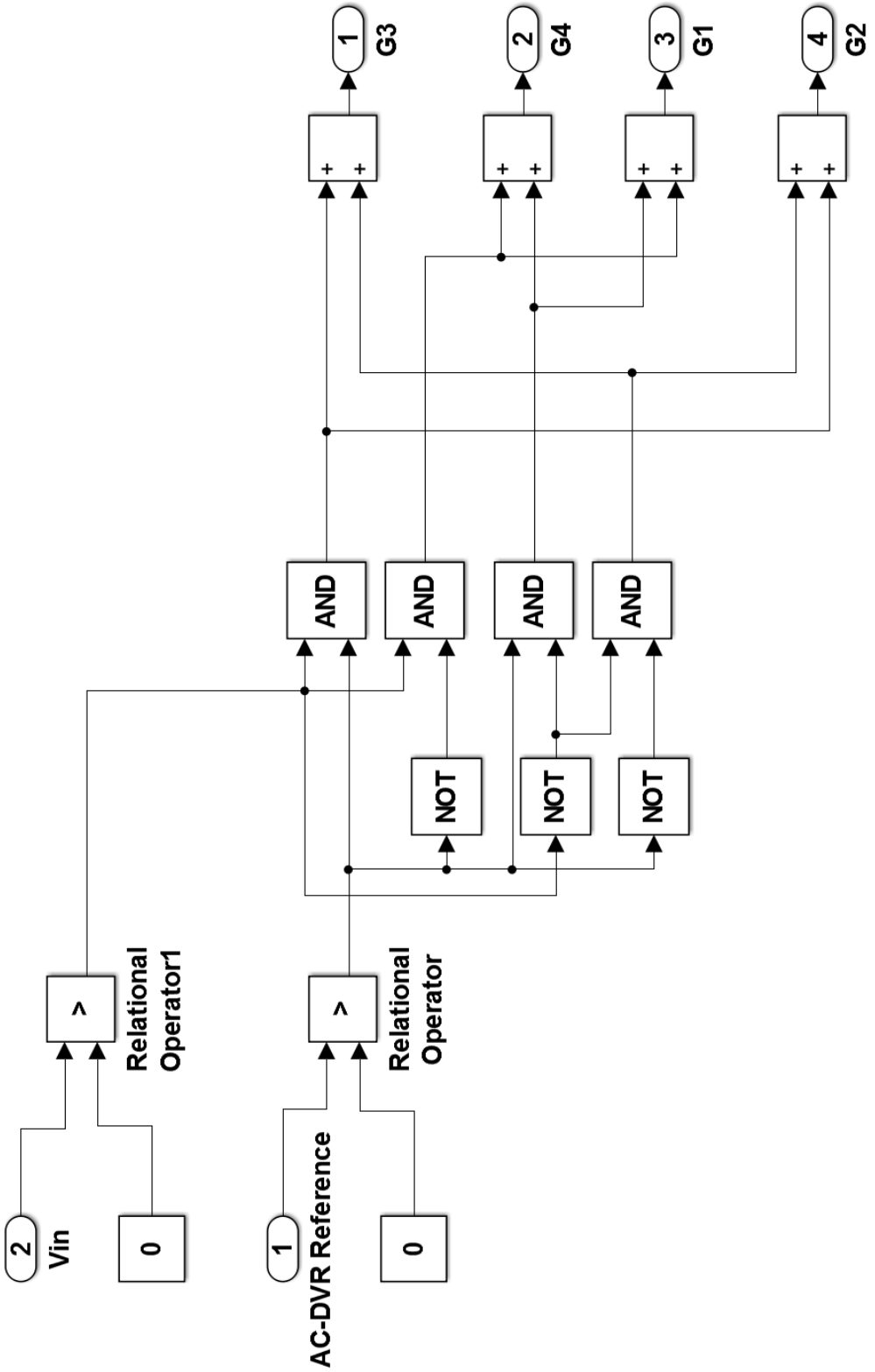


Figure 5.5: Control logic for bidirectional switches Q1Q2', Q2Q1', Q3Q4' and Q4Q3'

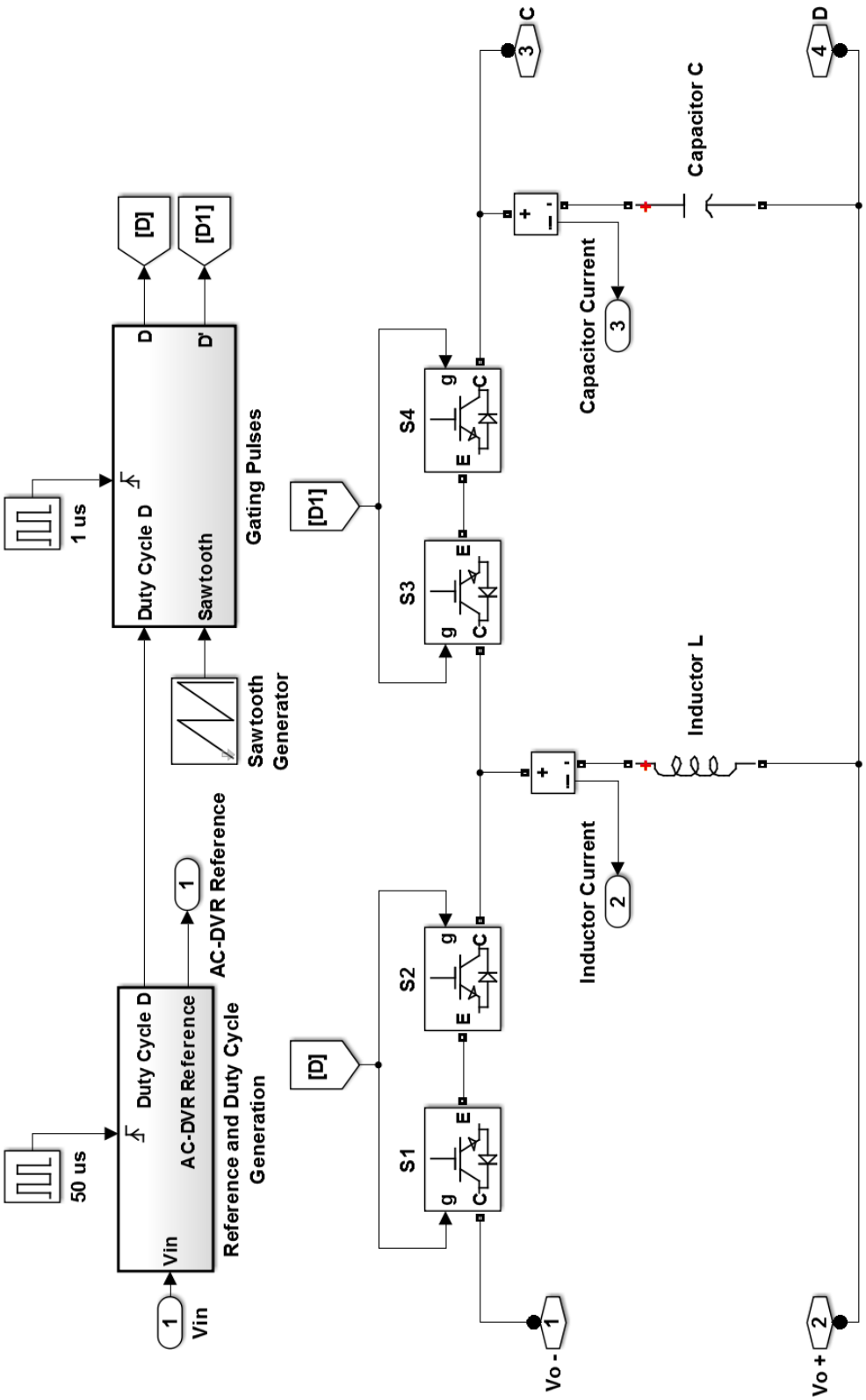


Figure 5.6: Model of AC-AC Buck Boost Converter (Wave shaper) and controller

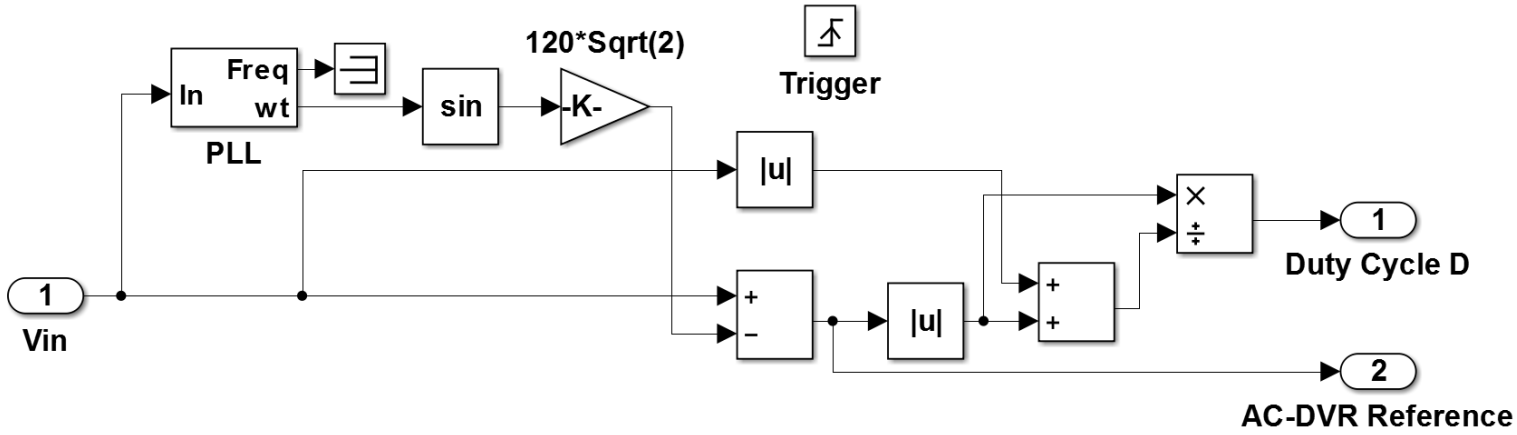


Figure 5.6: Duty cycle generation and AC-DVR reference generation block

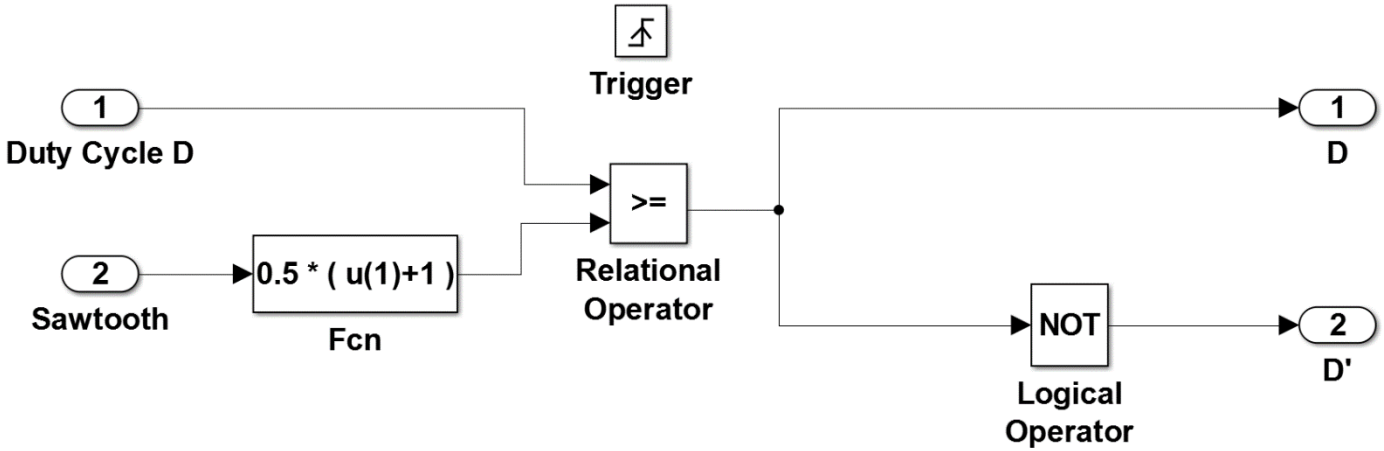


Figure 5.7: Gate pulses generation for switches S1S2 and S3S4

5.5 Model of Load

The load is modelled to be resistive for simulations. To determine the behavior of AC-DVR under step load changes, a variable resistance has been modelled by utilizing well known ohm's law. As it can be seen in Figure 5.9, the variable resistance is modelled by using controlled current block whose input is V/R. The V is determined by measuring the voltage across the load terminals while R is user defined. Resistance 14.4Ω and 9.6Ω are chosen for 1 kW and 1.5 kW load operations respectively. Resistance values 14.4Ω and 9.6Ω are passed for $0 \leq t \leq 0.0208$s and $0.0208 \leq t \leq 0.05$s respectively by the control logic shown in Figure 5.9 to increase the load to 1.5 kW from 1 kW at t=0.0208s.

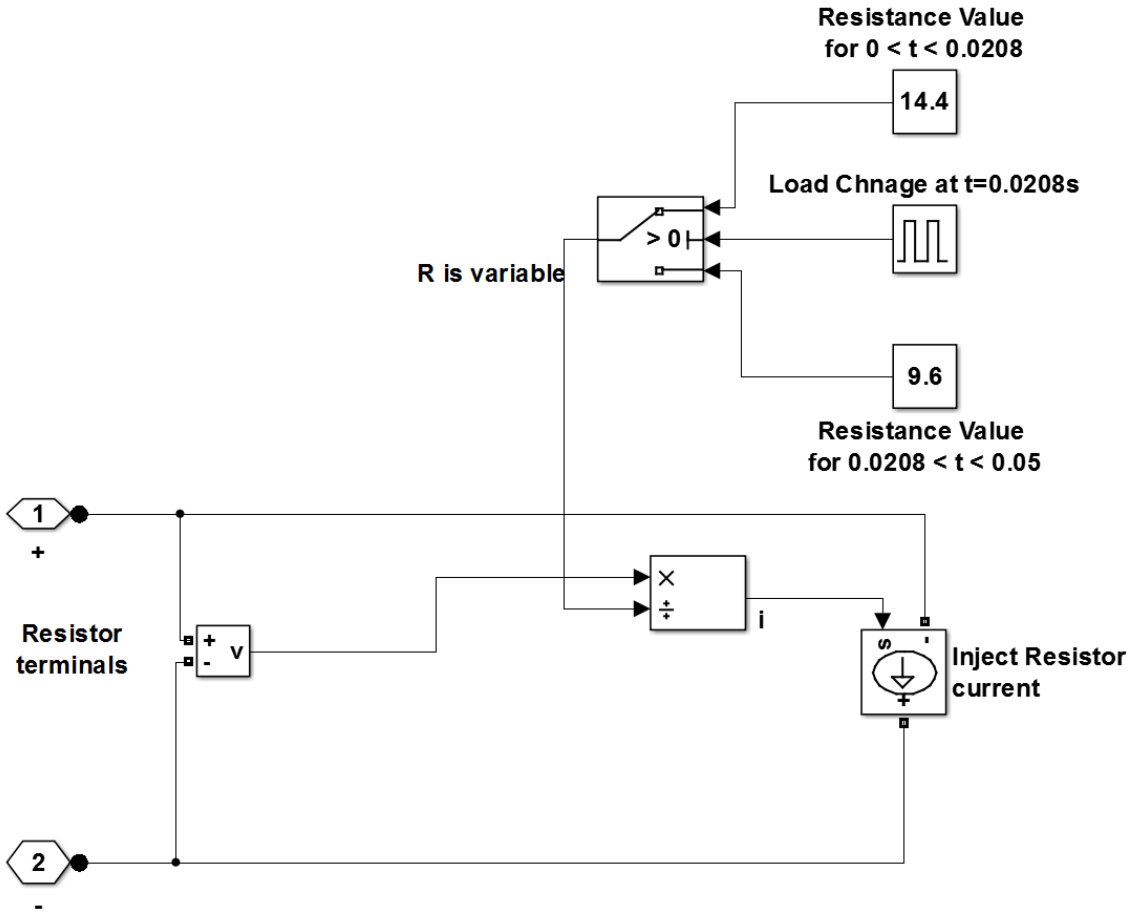


Figure 5.8: Model of variable resistive load

5.6 Model of Series Transformer and Scopes

The series transformer is modelled by using linear transformer block. The transformer is designed for 120V RMS, 60 Hz, 1 kVA and considered ideal. The transformer parameters are shown in Figure 5.10. Figure 5.11 shows the scopes used for various voltage and currents measurements which are to be presented in next chapter.

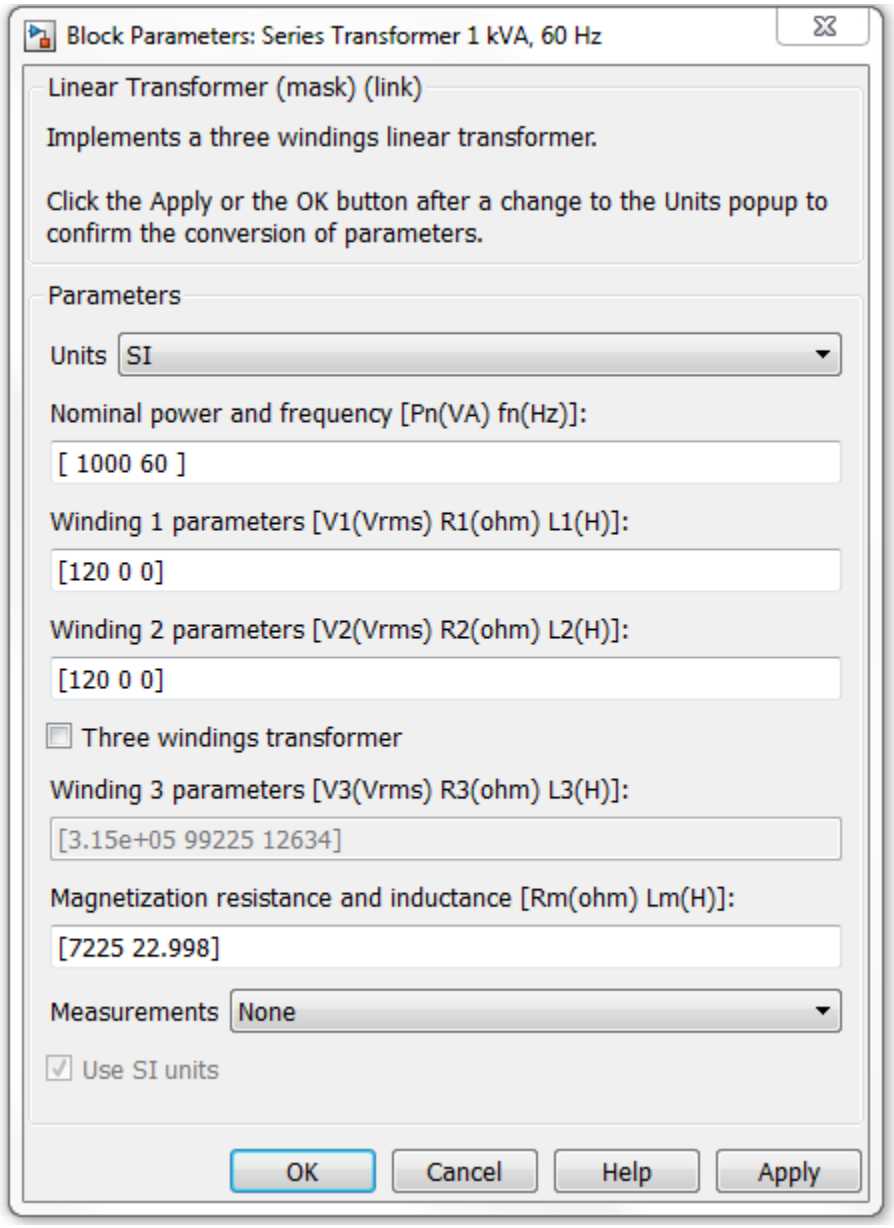


Figure 5.9: Series transformer parameters

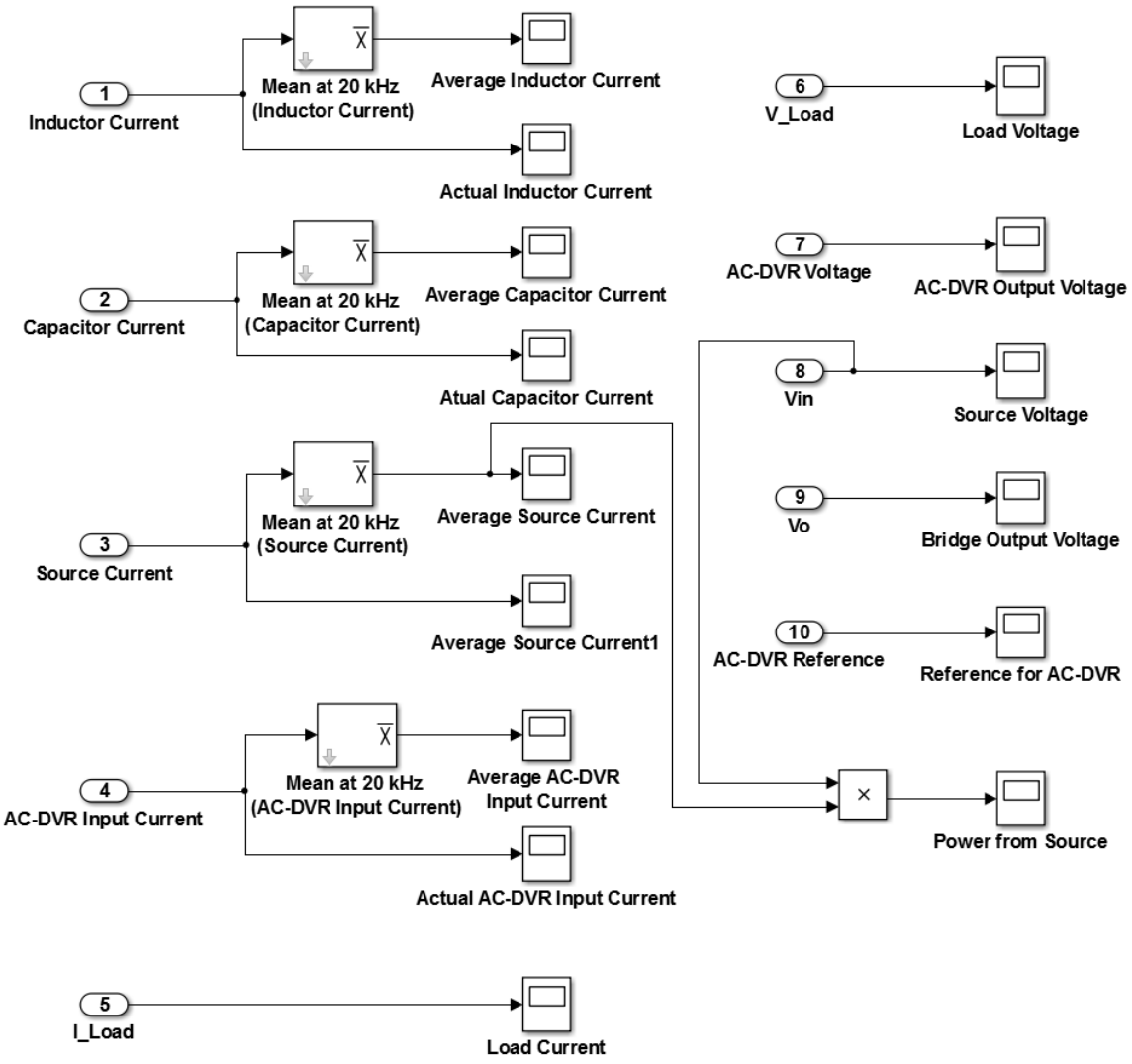


Figure 5.10: Scopes for voltage, current and power measurements

CHAPTER 6: SIMULATION RESULTS

6.1 Introduction

The brief overview of proposed direct AC-AC Dynamic Voltage Regulator (AC-DVR), its operating principle and control strategy were discussed thoroughly in previous chapters. The overall architecture of the system is modelled and simulated on MATLAB/Simulink platform. The behavior and dynamic response of AC-DVR under various voltage and load disturbances were simulated and presented in this chapter.

6.2 Simulation Parameters

The system is simulated on MATLAB/Simulink platform under the parameters tabulated in Table 6.1. The grid and transformer are considered ideal for the simulation purpose. The simulations have been performed under various voltage and load scenarios to validate the working principle of AC-DVR. These scenarios were created by changing some of the simulation parameters of Table 6.1. The changes in parameters are mentioned for each simulation scenario in next section while the other parameters remain unchanged.

Table 6.1 Simulation parameters

Model	Parameters
Source/Grid	120 V (RMS), 60 Hz
Load	14.4 Ω and 9.6 Ω (1kW and 1.5 kW)
Series transformer	1 kVA, 60 Hz
Inductor L	250 µH
Capacitor C	15 µF
AC-AC Buck Boost switching frequency f_{sw}	20 kHz

6.3 Simulation Results

The key area of focus is maintaining the THD and magnitude of load voltage within permissible limits by adding or subtracting needed voltage through AC-DVR when any disturbance occurs in source voltage. Thus, simulations for seventeen various source voltage distortion scenarios such as individual harmonic voltage distortion, combined harmonic voltage distortion, voltage sag, voltage swell and combined harmonic voltage and voltage sag distortion have been performed to validate the performance and capability of AC-DVR to maintain the load voltage. Moreover, to understand the dynamic response of the AC-DVR, simulations have been carried out for step change in load and disturbance type. The parameters for each operating scenario are tabulated in Table 6.2. The simulated waveforms for some selected scenarios are presented and discussed in following subsections. The behavior of AC-DVR under normal conditions, individual harmonic distortion (3^{rd}, 5^{th}, 11^{th}) and combined harmonic distortion (3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th} and 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th}, 13^{th}) are provided in subsections 6.3.1-6.3.6 respectively. Likewise, simulations under voltage sag, voltage swell and combined harmonic and sag (3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th} and sag) type of disturbances are discussed in subsections 6.3.7-6.3.9 respectively. Whereas, scenarios consisting of step load change under normal conditions and combined harmonic and sag (3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th} and sag) conditions are discussed in 6.3.10 and 6.3.11 to determine the dynamic behavior of AC-DVR under step load change. Similarly, step change in harmonic and swell type of disturbance is considered for scenarios discussed in 6.3.12 and 6.3.13. To determine the performance of AC-DVR under usual harmonic type disturbances, simulations under service voltage at UNC Charlotte have been performed and results are provided in 6.3.14.

Table 6.2: Summary of various operating scenarios and simulation results

Operating Scenario No.	Time (t) a=0, b=0.0208, c=0.05	Input Voltage RMS (V)	Fundamental Voltage RMS (V)	Harmonic Order (n) and magnitude as percentage of fundamental (%)						Input Voltage THD (%)	Load (W)	Output Voltage RMS (V)	Output Voltage THD (%)
				3	5	7	9	11	13				
I	$a \leq t \leq c$	120	120	-	-	-	-	-	-	0	1000	120	0
II	$a \leq t \leq c$	126.5	120	33.33	-	-	-	-	-	33.33	1000	119.9	1.91
III	$a \leq t \leq c$	122.4	120	-	20	-	-	-	-	20	1000	119.9	1.53
IV	$a \leq t \leq c$	121.2	120	-	-	14.29	-	-	-	14.29	1000	119.9	1.44
V	$a \leq t \leq c$	120.7	120	-	-	-	11.11	-	-	11.11	1000	120	1.48
VI	$a \leq t \leq c$	120.5	120	-	-	-	-	9.09	-	9.09	1000	120	1.58
VII	$a \leq t \leq c$	120.4	120	-	-	-	-	-	7.69	7.69	1000	120	1.73
VIII	$a \leq t \leq c$	121.1	120	8	9	5	-	2	2	13.34	1000	120	1.22
IX	$a \leq t \leq c$	131.3	120	33.33	20	14.29	11.11	9.09	7.69	44.5	1000	119.9	6.35
X	$a \leq t \leq c$	84	84	-	-	-	-	-	-	0	1000	119.7	2.06
XI	$a \leq t \leq c$	156	156	-	-	-	-	-	-	0	1000	120.2	1.42
XII	$a \leq t \leq c$	97.33	96	10	11	6.25	-	2.5	2.5	16.68	1000	119.7	1.95
XIII	$a \leq t \leq c$	116.1	115.9	1.78	3.36	1.6	0.19	2.52	1.43	5.12	1000	120	1.06
XIV	$a \leq t \leq b$	120	120	-	-	-	-	-	-	0	1000	120	0
	$b \leq t \leq c$	120	120	-	-	-	-	-	-	0	1500	120	0
XV	$a \leq t \leq b$	97.33	96	10	11	6.25	-	2.5	2.5	16.68	1000	119.7	1.95
	$b \leq t \leq c$	97.33	96	10	11	6.25	-	2.5	2.5	16.68	1500	119.7	2.62
XVI	$a \leq t \leq b$	144	144	-	-	-	-	-	-	0	1000	120.1	1.07
	$b \leq t \leq c$	168	168	-	-	-	-	-	-	0	1000	120.3	1.68
XVII	$a \leq t \leq b$	122.4	120	20	-	-	-	-	-	20	1000	119.9	1.21
	$b \leq t \leq c$	125.3	120	-	30	-	-	-	-	30	1000	119.9	2.32

6.3.1 Normal Grid Condition: Operating scenario I

The first simulation was performed for normal grid operation such as magnitude and THD of source voltage is 120V RMS and zero respectively as shown in Figure 6.1. Hence, as per the control strategy discussed in previous chapter, switches Q3Q2 and Q3'Q2' in bidirectional bridge operates and synthesizes rectified output at the input terminals of the AC-AC buck boost converter or wave shaper as depicted in Figure 6.2. But, as per the control, duty cycle for AC-AC buck boost is zero thus switches S1S2 remains open while switches S3S4 remains closed. Therefore, the AC-DVR synthesizes almost zero voltage as shown in Figure 6.3. This voltage is added in series with source voltage via series transformer enabling the load voltage to be same as source voltage as shown in Figure 6.4. Hence, under normal grid conditions, AC-DVR does not operate and source voltage and current are same as load voltage and current with zero THD.

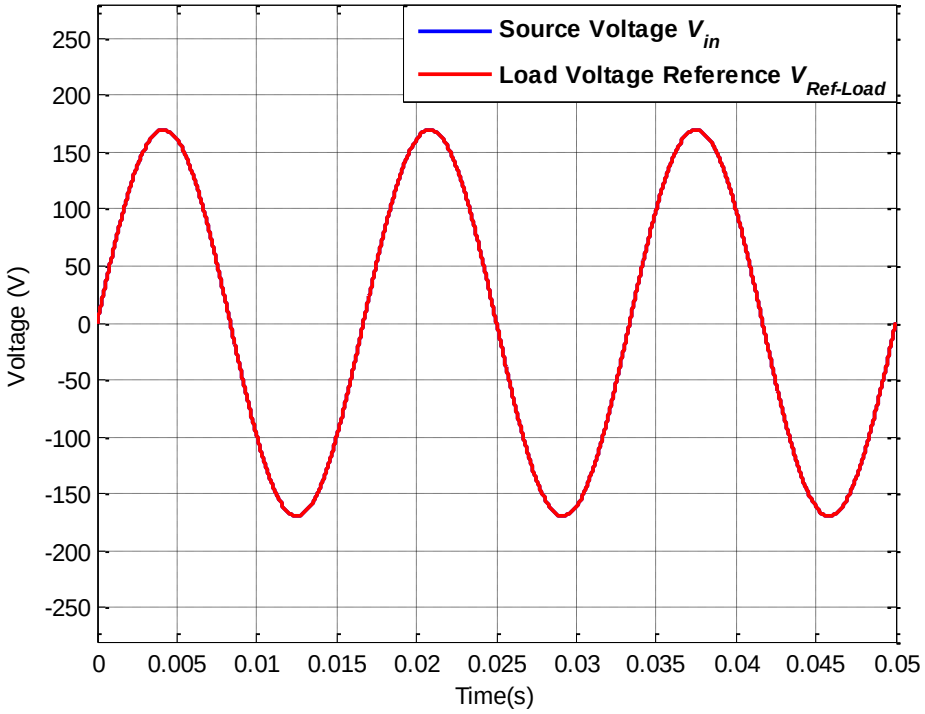


Figure 6.1: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario I

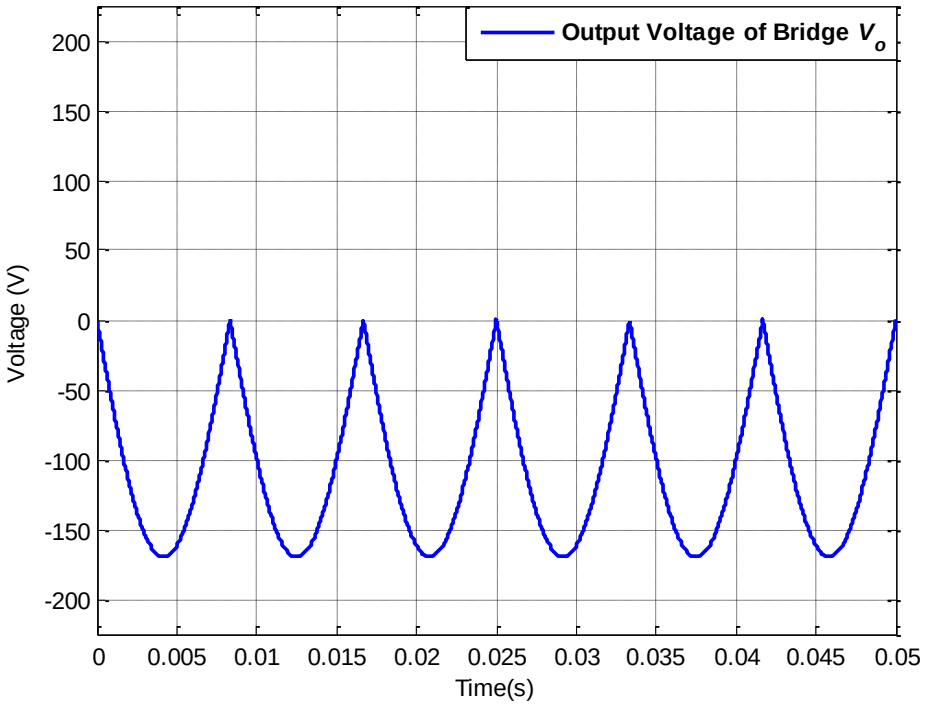


Figure 6.2 Bridge output voltage V_o for operating scenario I

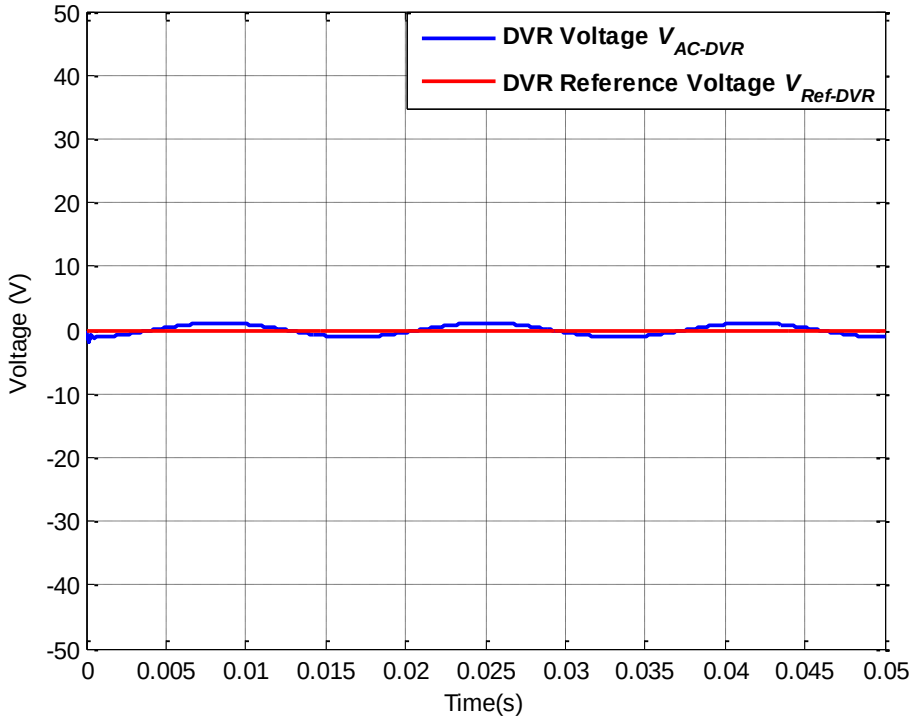


Figure 6.3 AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario I

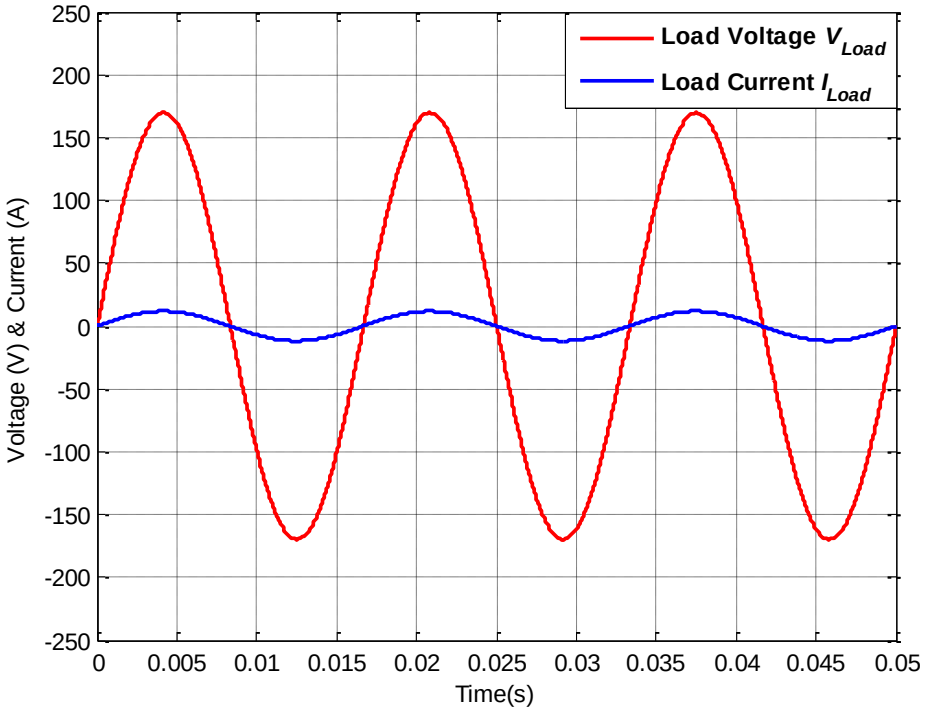


Figure 6.4: Load voltage V_{Load} and load current I_{Load} for operating scenario I

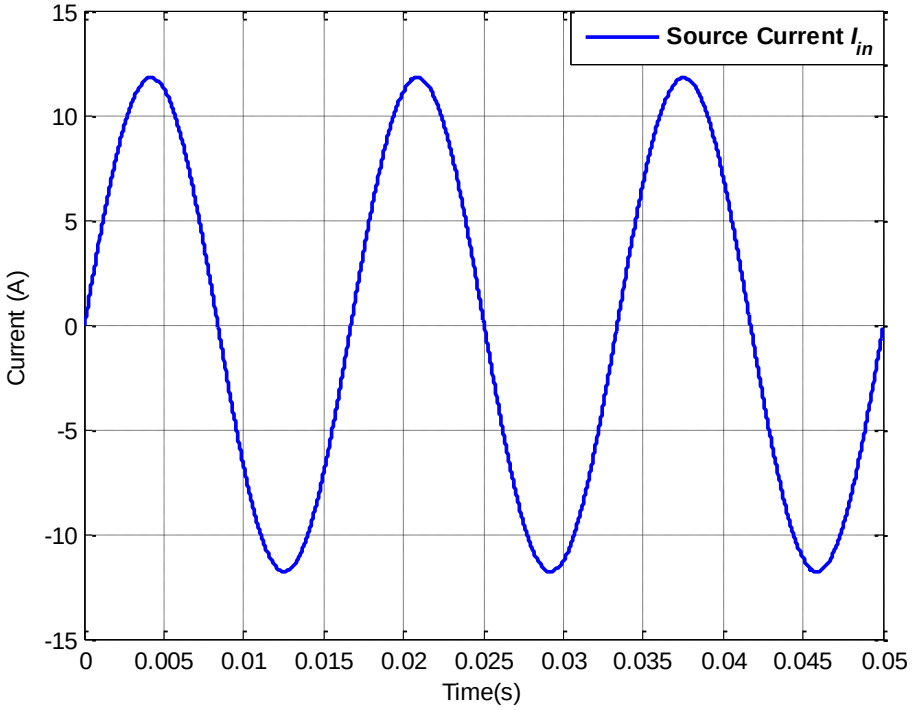


Figure 6.5: Source current I_{in} for operating scenario I

6.3.2 3rd Harmonic distortion: Operating scenario II

In this scenario, the source voltage has a fundamental component of 120V RMS at 60Hz and a 3rd harmonic component of 33.33% with frequency of 180Hz. Thus, RMS and THD of input voltage becomes 126.5V and 33.33% respectively. The AC-DVR should inject needed amount of voltage at 180Hz to restore the magnitude and shape of voltage at load side. The sensing and control unit of the system senses the source voltage and compares it to the reference 120V RMS sinusoid signal. The AC-DVR is supposed to synthesize 180° out of phase third harmonic voltage to restore the load voltage in terms of RMS and shape. Also, whenever the output of AC-DVR needed to be negative, the bidirectional bridge synthesizes positive voltage from the source and vice versa as discussed and presented in section 3.5 and Table 3.1. Then the AC-AC buck boost converter is operated with dedicated duty cycle as presented in Eq. (9) to synthesize shape and magnitude of injection voltage from the output of bidirectional bridge. The source voltage, output voltage of bridge and AC-DVR voltage are shown in Figure 6.6, 6.7 and 6.8 respectively. The voltage synthesized by AC-DVR is injected via series transformer and load voltage is restored with RMS and THD of 119.9V and 1.91% as depicted in Figure 6.9 along with load current. The actual and average input currents for AC-DVR and inductor are presented in Figure 6.11 and 6.12. The actual and average capacitor currents are shown in Figure 6.13 and 6.14 respectively. Note that both inductor and capacitor currents follow same principle as discussed in previous chapter. Furthermore, the source current as shown in Figure 6.10 also follows Eq. (18) resulting sinusoidal power extraction from source as shown in Figure 6.15 which does not contain any 3rd harmonic frequency oscillations.

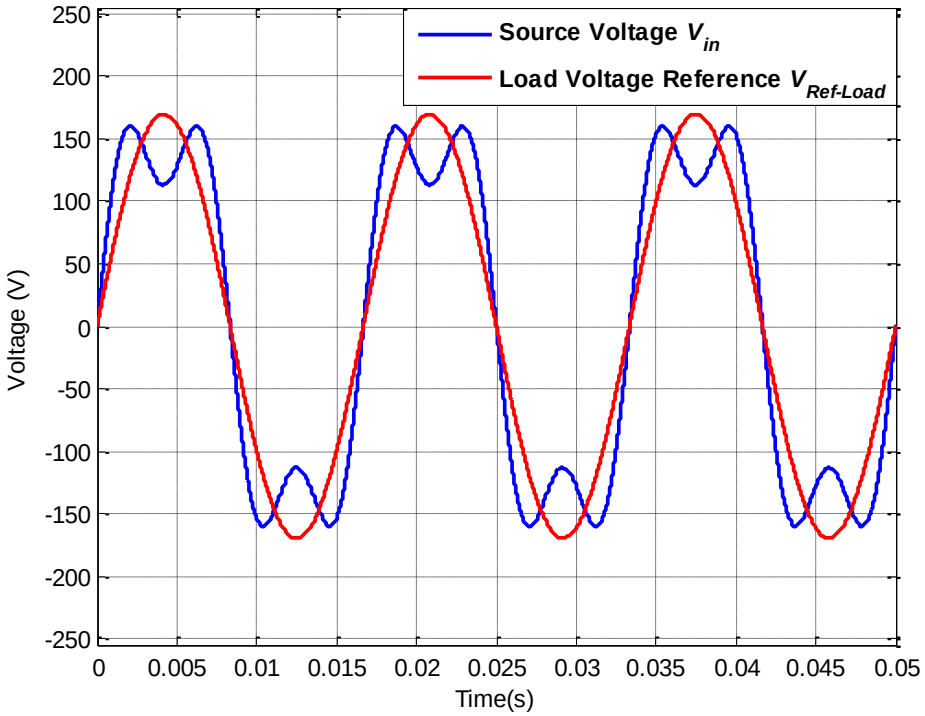


Figure 6.6: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario II

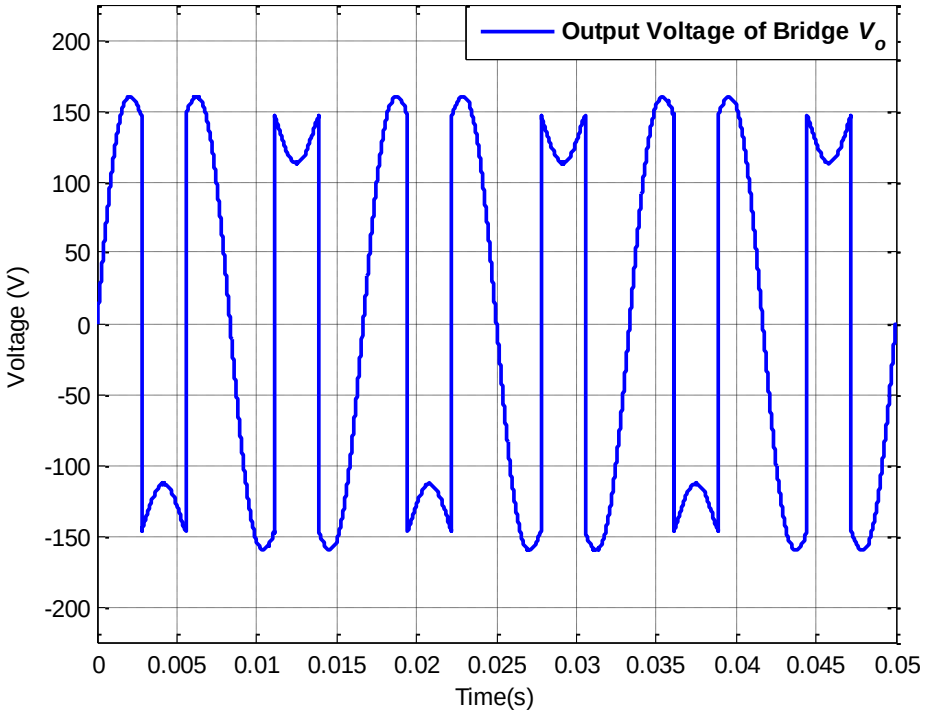


Figure 6.7: Bridge output voltage V_o for operating scenario II

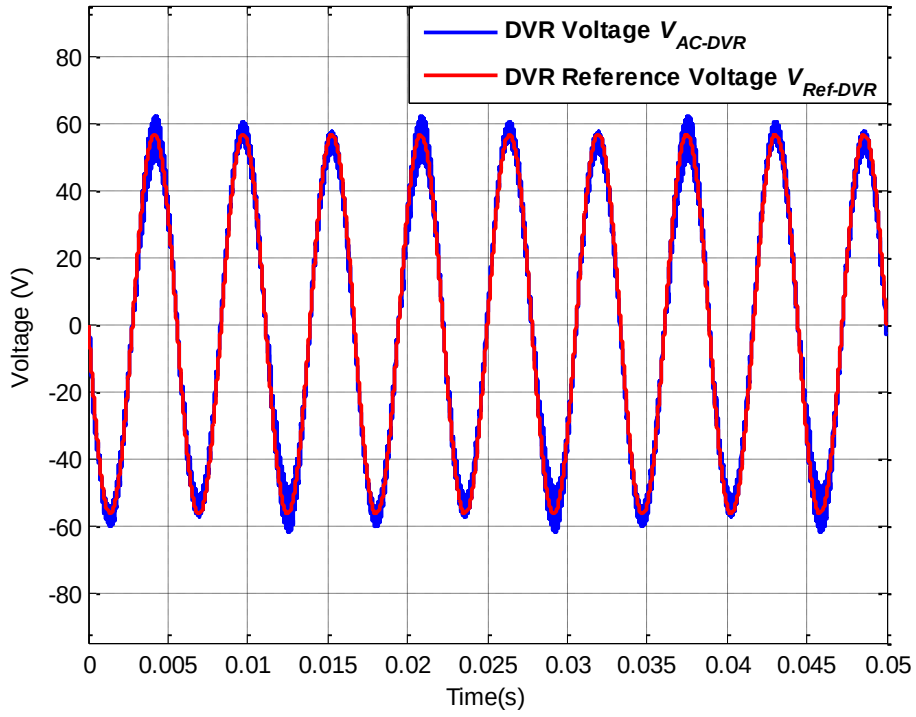


Figure 6.8: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario II

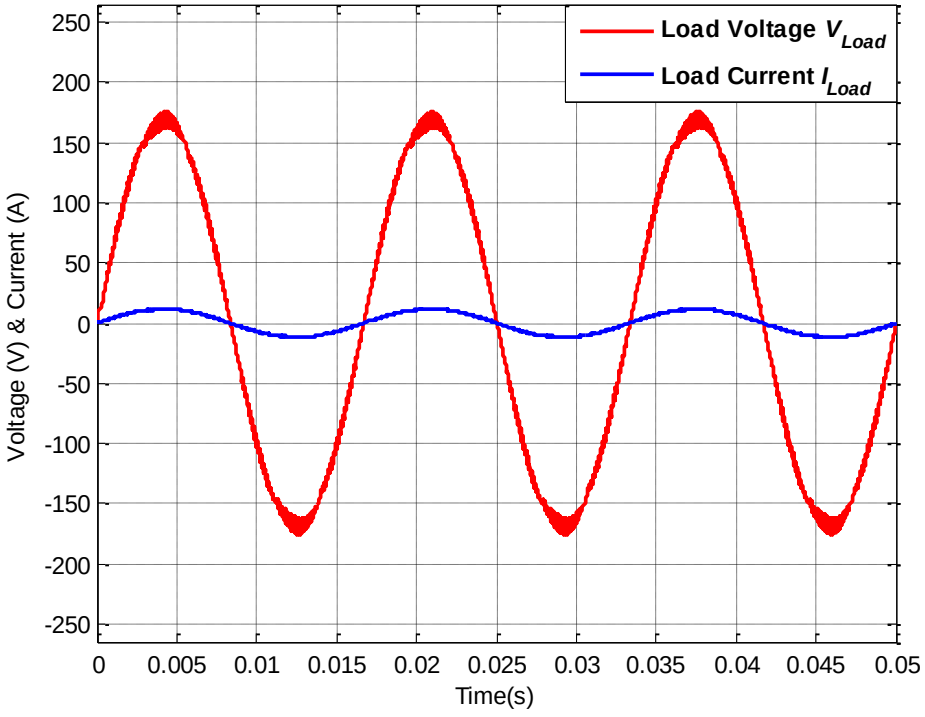


Figure 6.9: Load voltage V_{Load} and load current I_{Load} for operating scenario II

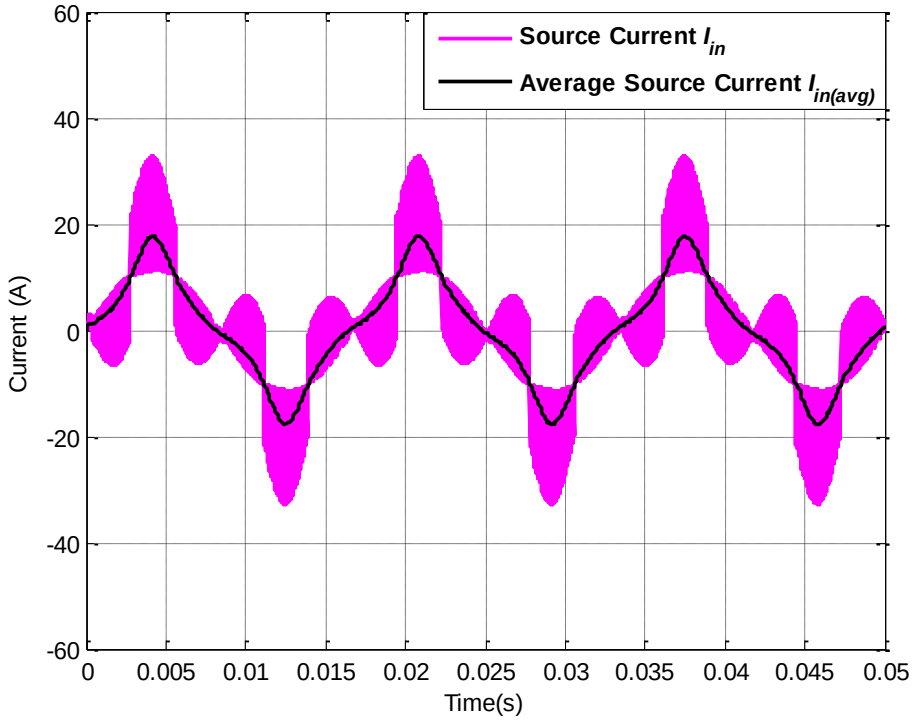


Figure 6.10: Actual source current I_{in} and average source current $I_{in(avg)}$ for operating scenario II

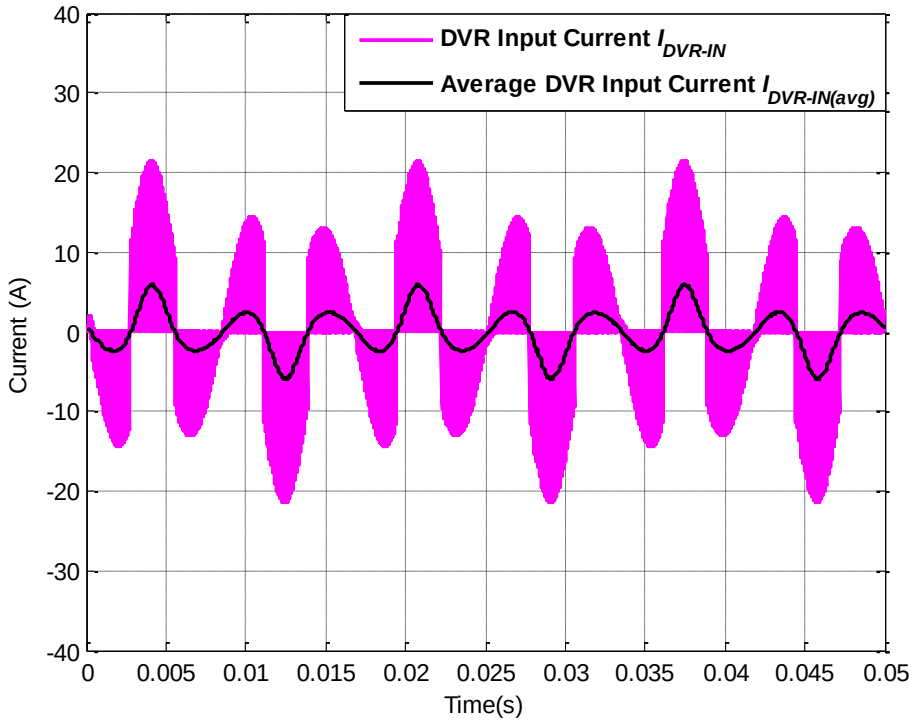


Figure 6.11: Actual DVR current I_{DVR-IN} and average DVR current $I_{DVR-IN(avg)}$ for operating scenario II

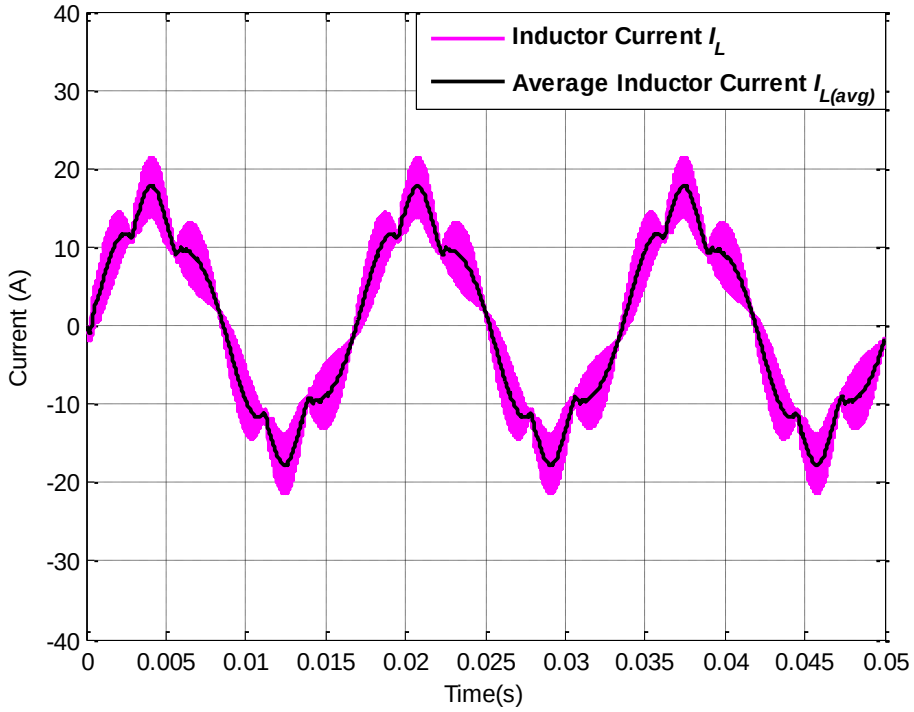


Figure 6.12: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario II

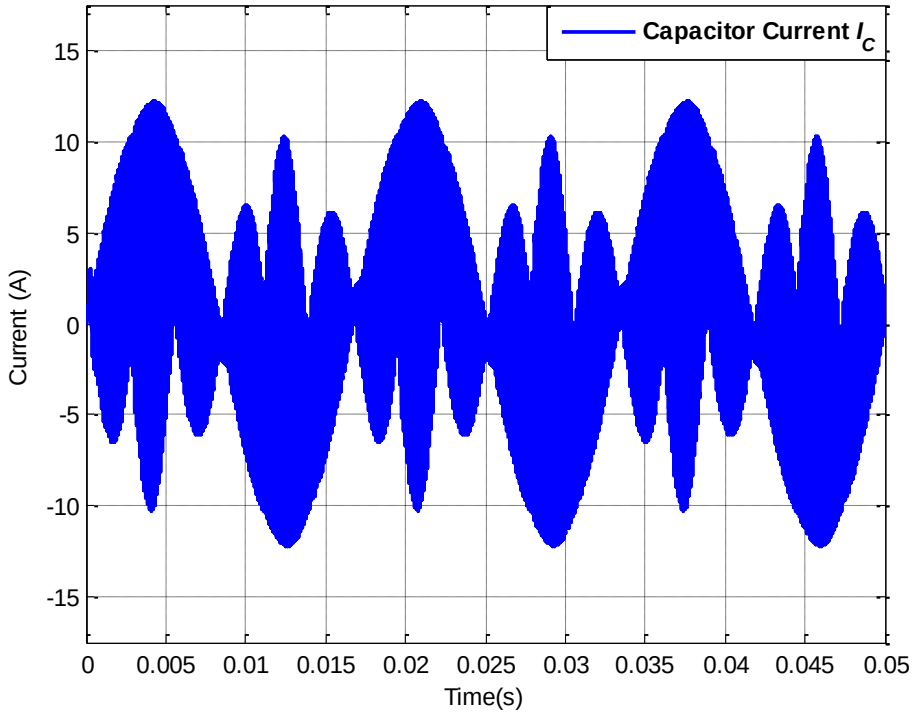


Figure 6.13: Actual capacitor current I_C for operating scenario II

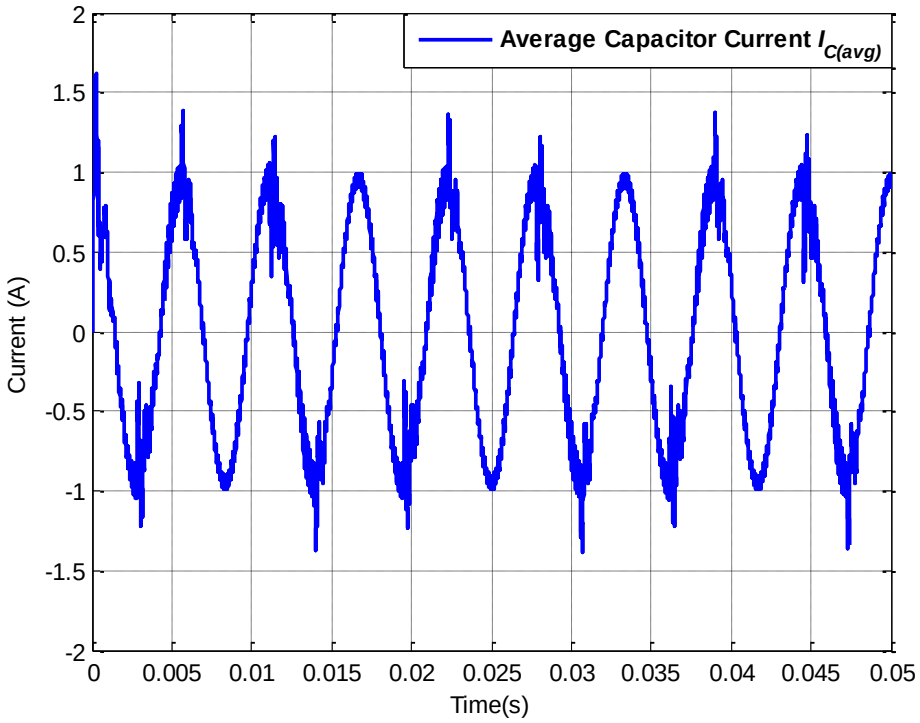


Figure 6.14: Average capacitor current $I_{C(avg)}$ for operating scenario II

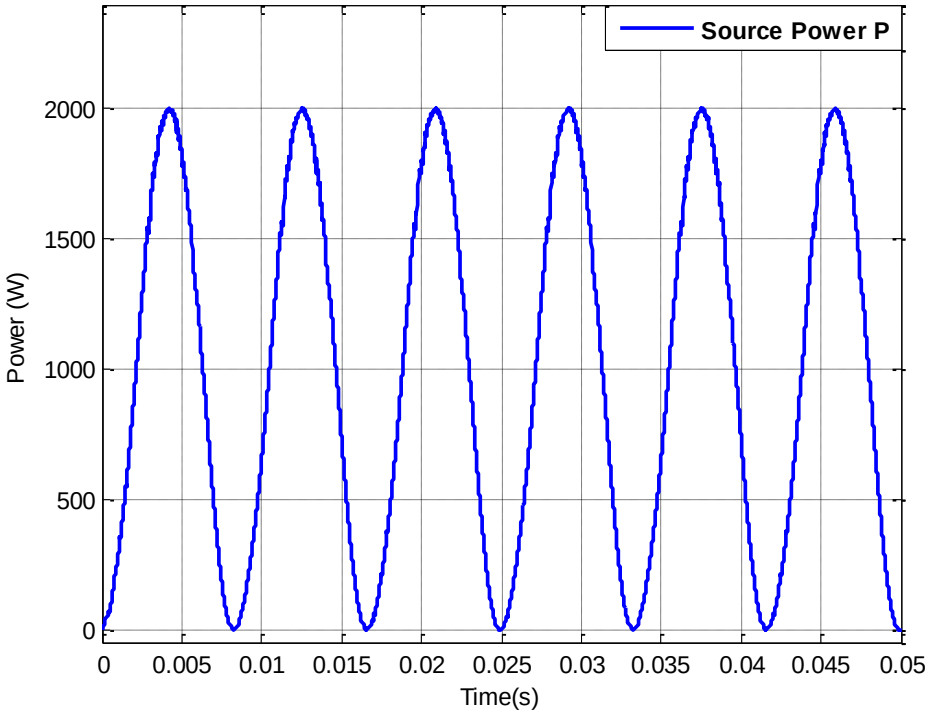


Figure 6.15: Grid power for operating scenario II

6.3.3 5th Harmonic distortion: Operating scenario III

This operating scenario is like the scenario discussed in previous subsection. The only difference is the harmonic order and its percentage. In this operating condition, source voltage experiences 5th harmonic distortion with harmonic magnitude of 20% resulting input RMS and THD to be 112.4V and 20% respectively. The AC-DVR is operated with dedicated control and principle as discussed in previous subsections. The simulation was performed for three fundamental cycles such as t=0 to t=0.05 seconds. The source voltage with 5th harmonic distortion and output voltage of bidirectional bridge are depicted in Figure 6.16 and 6.17 respectively. The output of AC-DVR is shown in Figure 6.18 which is added in series with source voltage via series transformer. Hence, the load voltage RMS is restored to 119.9V whereas the THD is reduced to 1.53%. The load voltage and load current are presented in Figure 6.19.

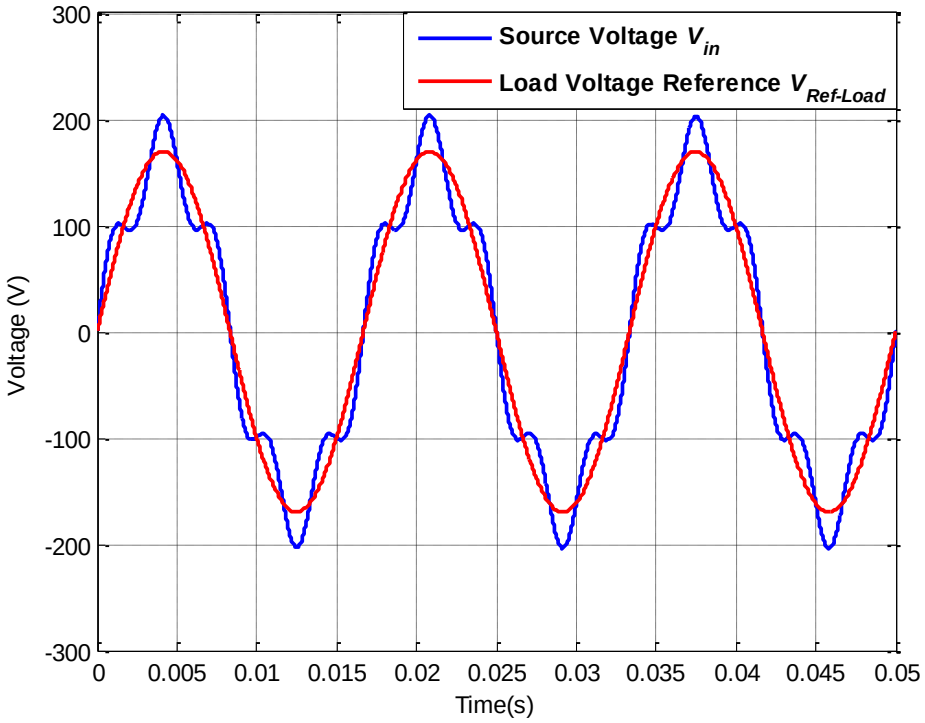


Figure 6.16: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario III

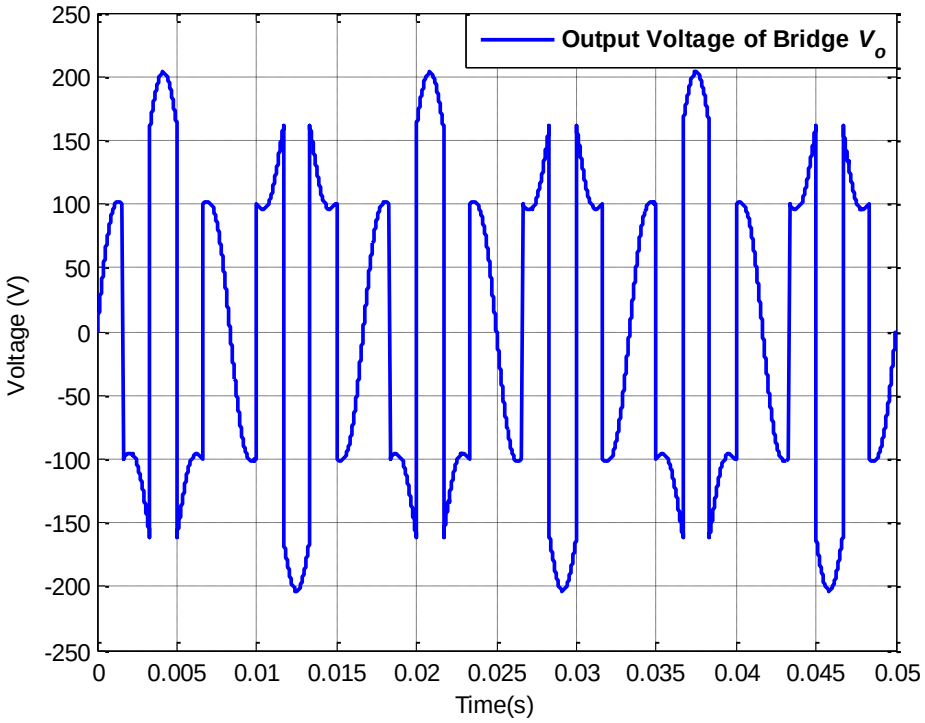


Figure 6.17: Bridge output voltage V_o for operating scenario III

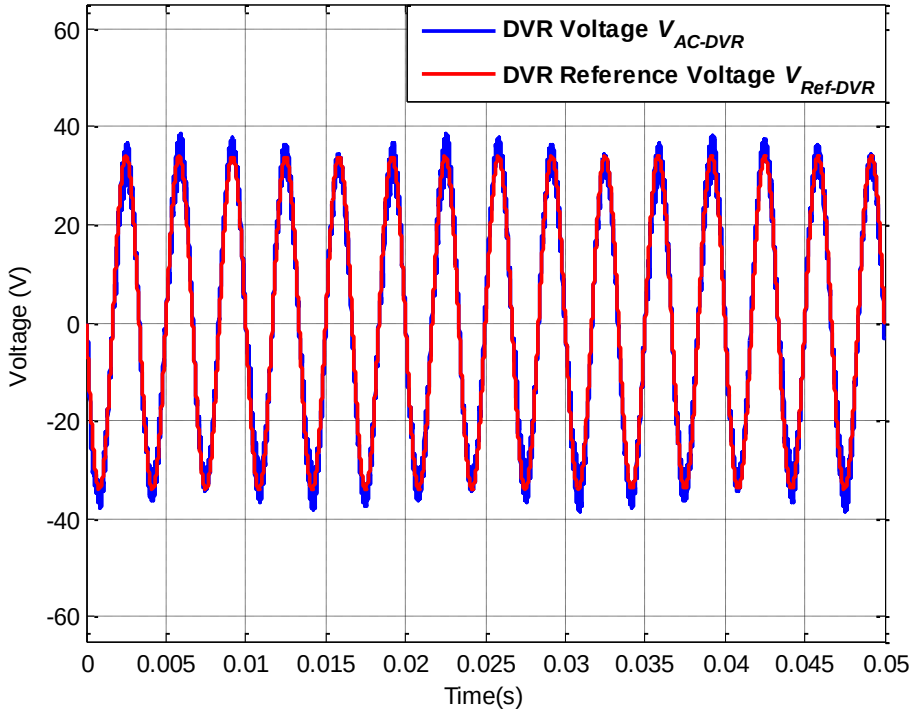


Figure 6.18: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario III

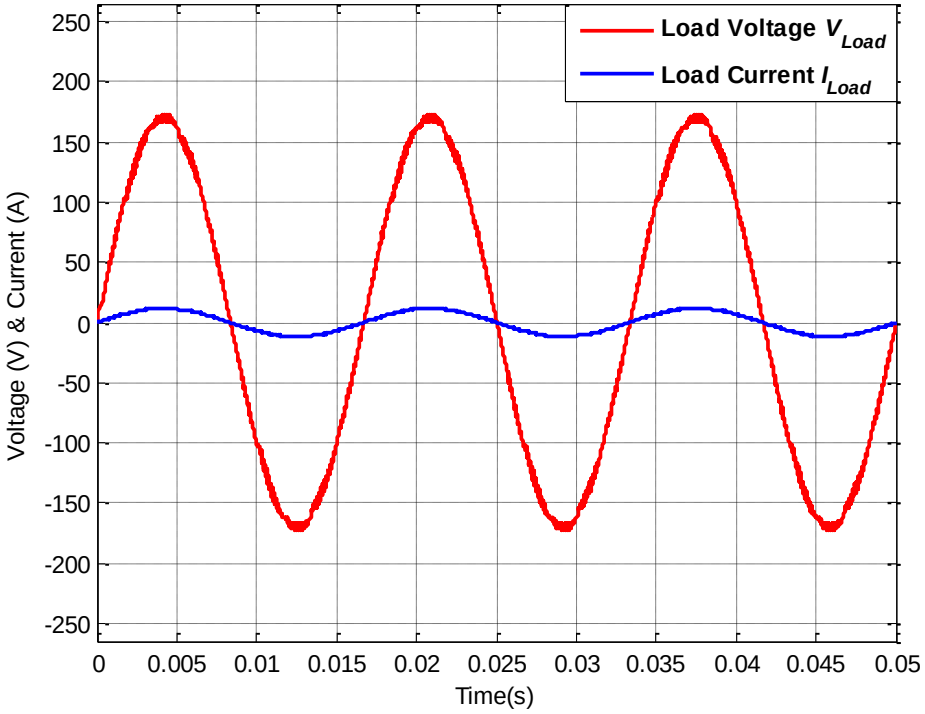


Figure 6.19: Load voltage V_{Load} and load current I_{Load} for operating scenario III

6.3.4 11th Harmonic distortion: Operating scenario VI

The source voltage has 9.09% of 11th harmonic distortion in this scenario which makes input RMS voltage 120.5V. The source voltage is sensed and compared with a 120V RMS sinusoidal reference signal and AC-DVR is operated to synthesize the error voltage which will be 11th harmonic voltage with 9.09% magnitude in this case. The simulation results for source voltage and bidirectional bridge output are shown in Figure 6.20 and 6.21 respectively. The AC-AC buck boost converter working as a wave shaper, synthesizes the 11th harmonic sinusoid with appropriate magnitude from the output of bidirectional bridge as shown in Figure 6.22. This voltage is injected in series with source voltage and load voltage is restored to 120V RMS with 1.53% THD. The results for restored fine sinusoidal load voltage and load current are depicted in Figure 6.23.

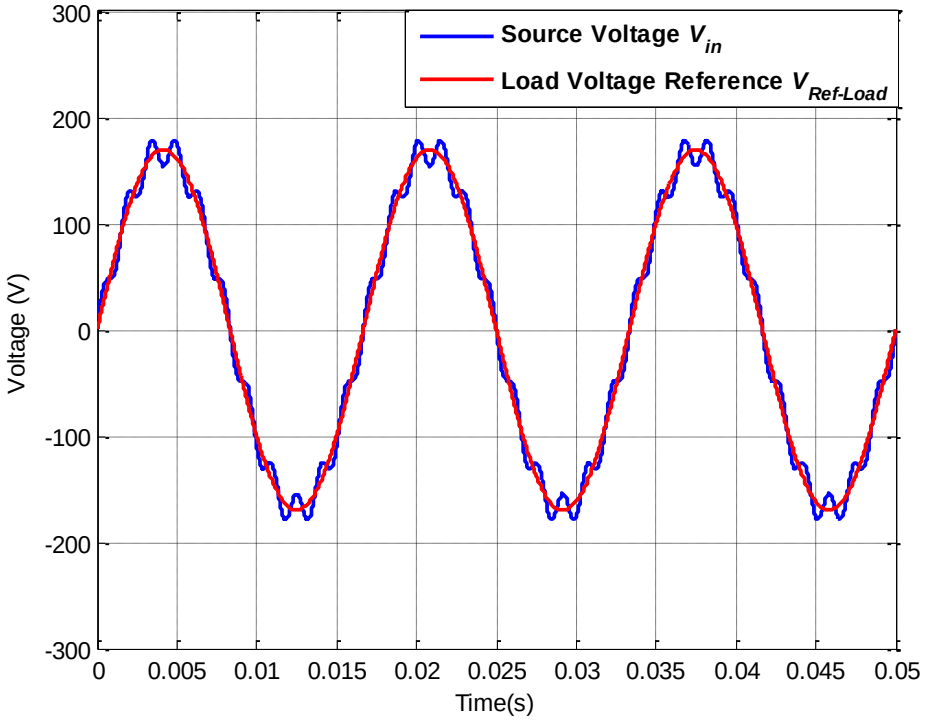


Figure 6.20: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario VI

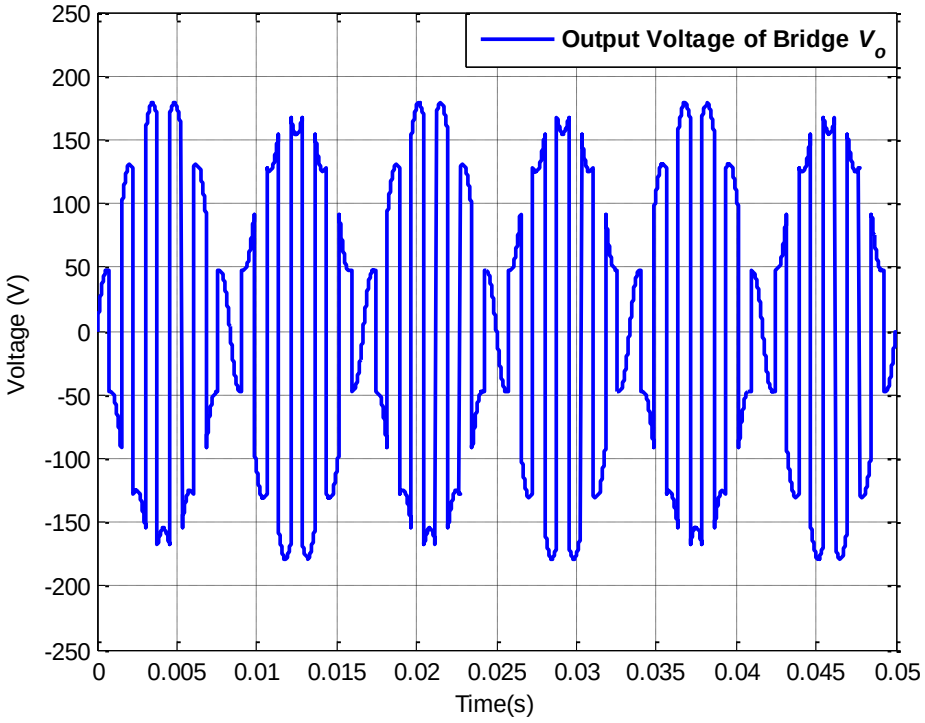


Figure 6.21: Bridge output voltage V_o for operating scenario VI

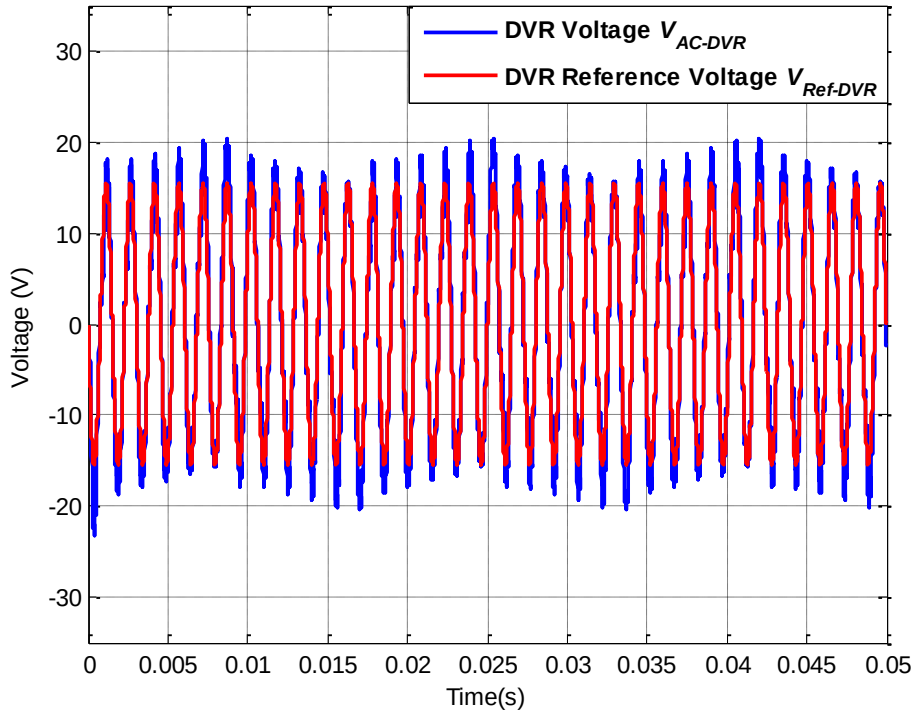


Figure 6.22: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario VI

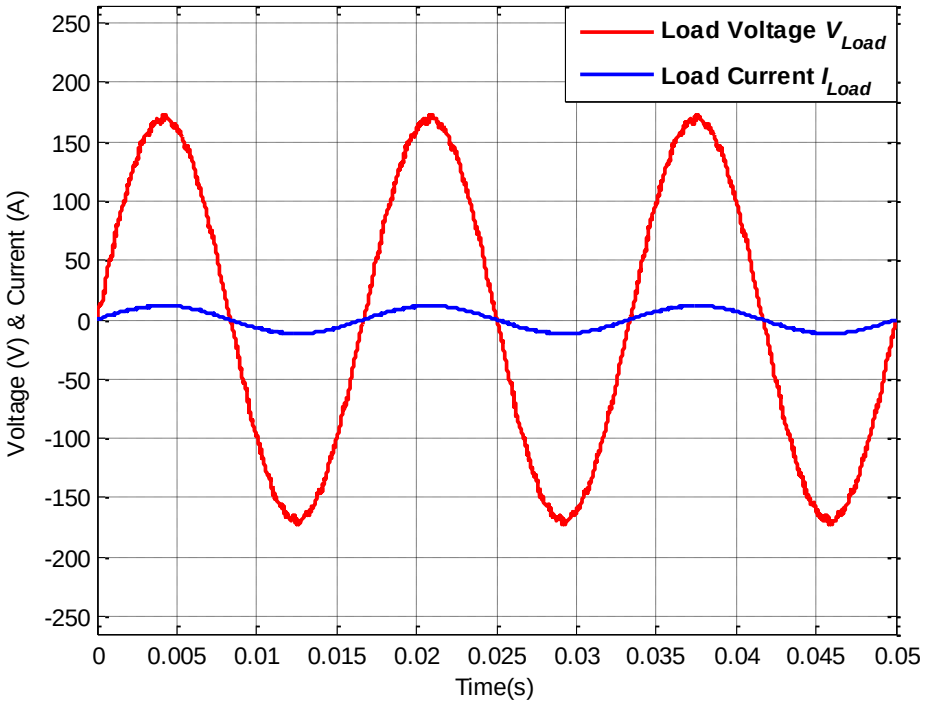


Figure 6.23: Load voltage V_{Load} and load current I_{Load} for operating scenario VI

6.3.5 Combined harmonic distortion: Operating scenario VIII

Simulations for individual harmonic voltage distortion are discussed and presented in previous scenarios. In this operating condition, performance of AC-DVR under combined effect of various harmonic orders will be evaluated. Thus, the source voltage is modelled with harmonic orders of 3^{rd}, 5^{th}, 7^{th}, 11^{th} and 13^{th} with magnitudes of 8%, 9%, 5%, 2% and 2% respectively as shown in Figure 6.24. The control circuit of the AC-DVR senses this voltage and compares it with 120V RMS reference signal and generates reference for AC-AC buck boost converter. Also, the bidirectional bridge is operated in similar manner as discussed in previous operating scenarios such as when the output of AC-AC buck boost converter is needed to be positive, the bidirectional bridge changes the source voltage to negative at the input terminals of wave shaper and vice versa. The simulation results for the output of bidirectional bridge is depicted in Figure 6.25. Then, the AC-AC buck boost converter is operated by dedicated duty cycle as presented in Eq. (9) and synthesizes 180° out of phase voltage with desired shape and magnitude which is presented in Figure 6.26 for this case. This voltage is added in series with source voltage by means of series transformer. Hence, the load voltage RMS voltage is restored to 119.7V and THD is reduced to 1.95% from 13.34%. Simulation results for load voltage and current, AC-DVR input currents, inductor currents, actual capacitor current and average capacitor current are presented in Figure 6.27, 6.29, 6.30, 6.31, and 6.32 respectively. The inductor currents and capacitor currents follow the Equations presented in 4.12 and 4.13. The source currents are presented in Figure 6.28 which are governed by Eq. (18). Thus, the power delivered by the source is almost sinusoidal and does not have any other frequency components except fundamental frequency as shown in Figure 6.33.

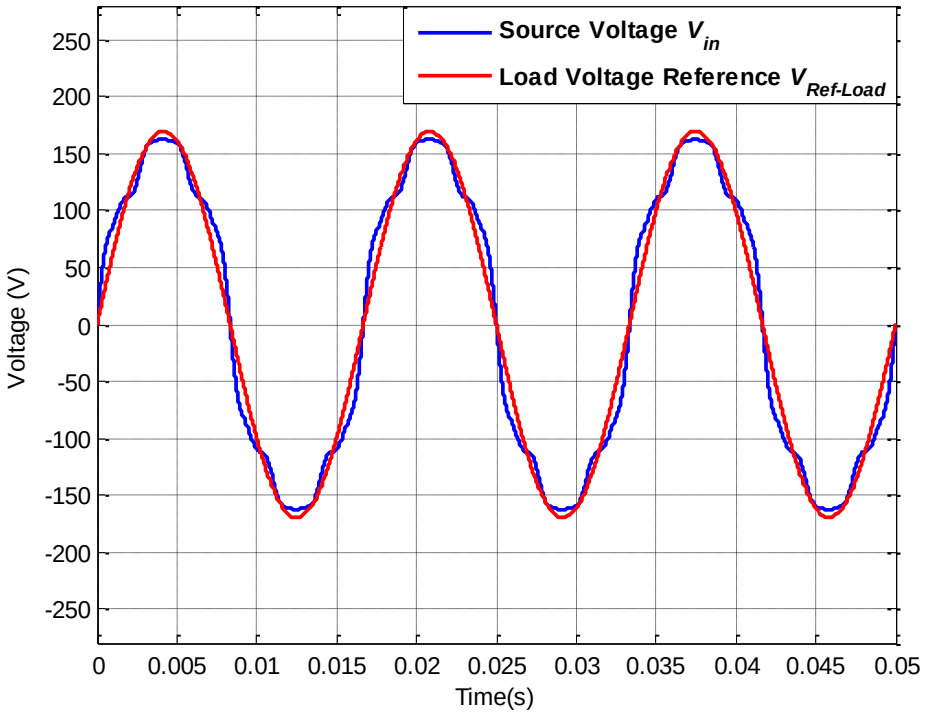


Figure 6.24: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario VIII

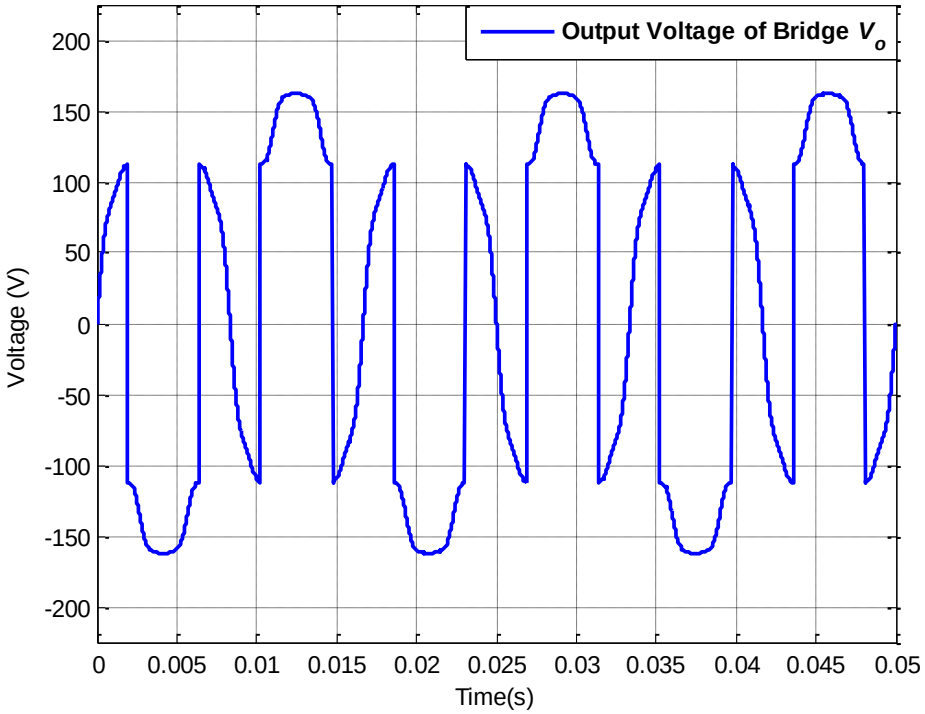


Figure 6.25: Bridge output voltage V_o for operating scenario VIII

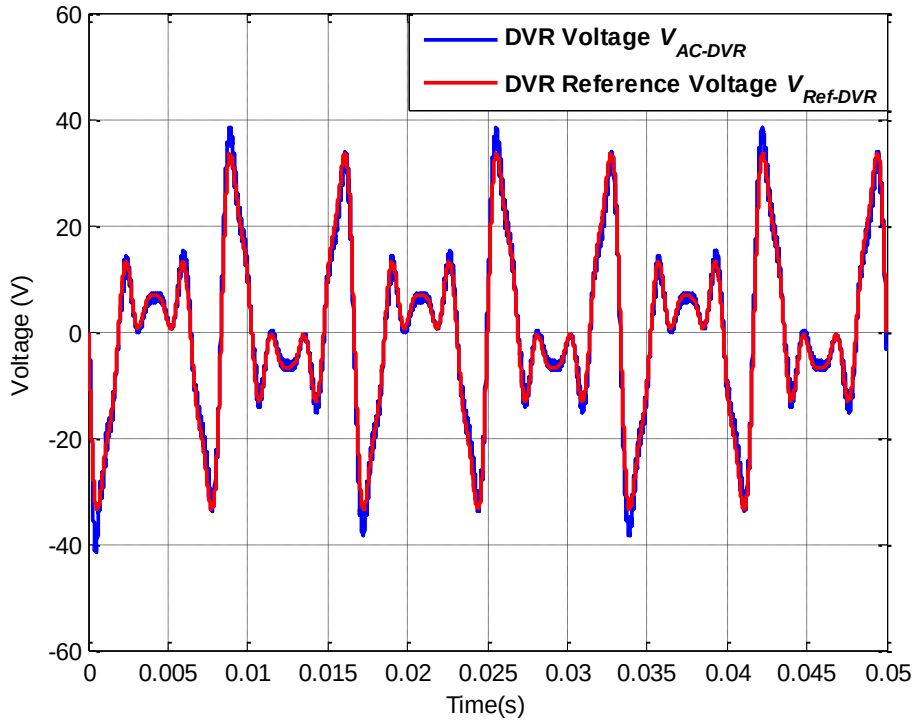


Figure 6.26: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario VIII

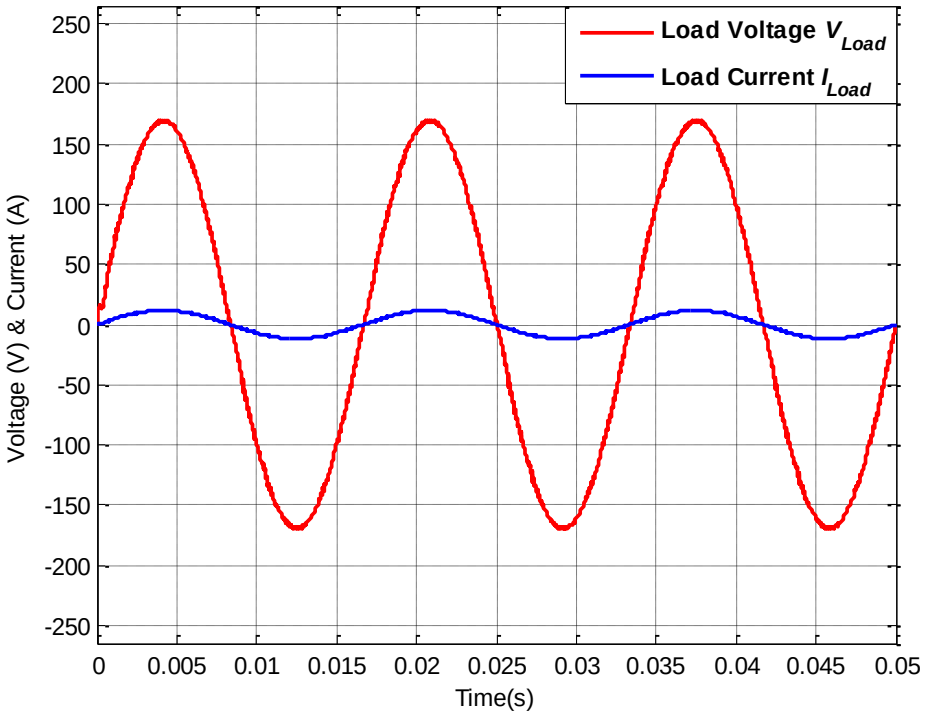


Figure 6.27: Load voltage V_{Load} and load current I_{Load} for operating scenario VIII

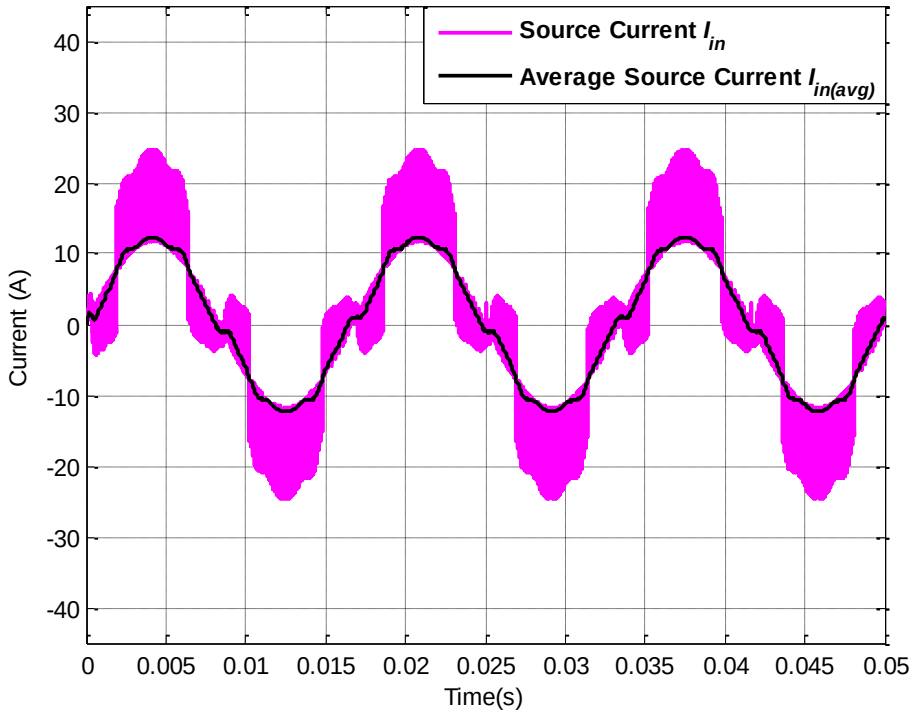


Figure 6.28: Actual source current I_{in} and average source current $I_{in(avg)}$ for operating scenario VIII

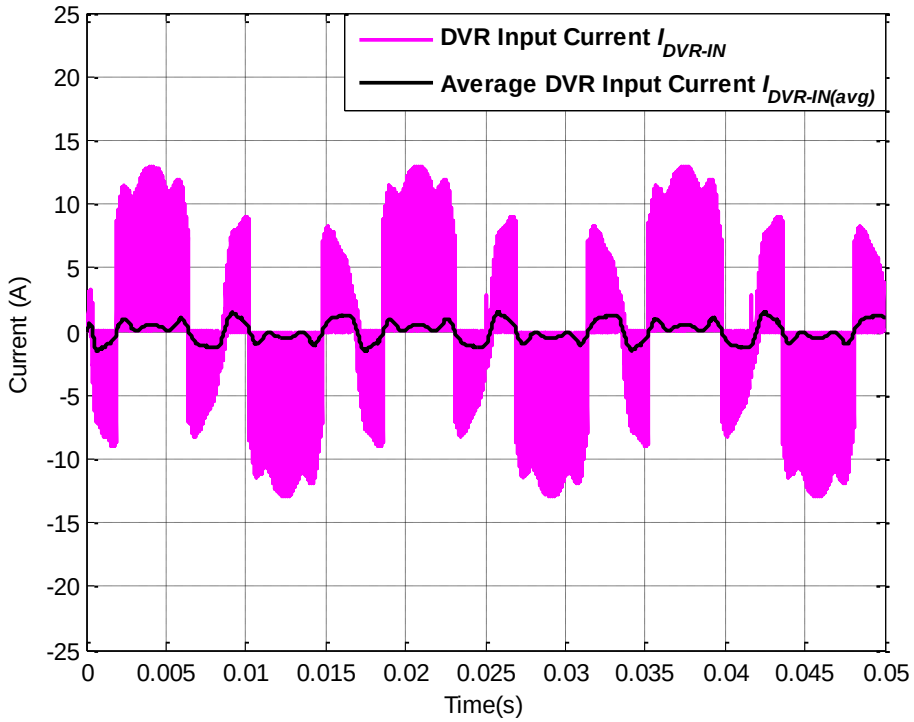


Figure 6.29: Actual DVR current I_{DVR-IN} and average DVR current $I_{DVR-IN(avg)}$ for operating scenario VIII

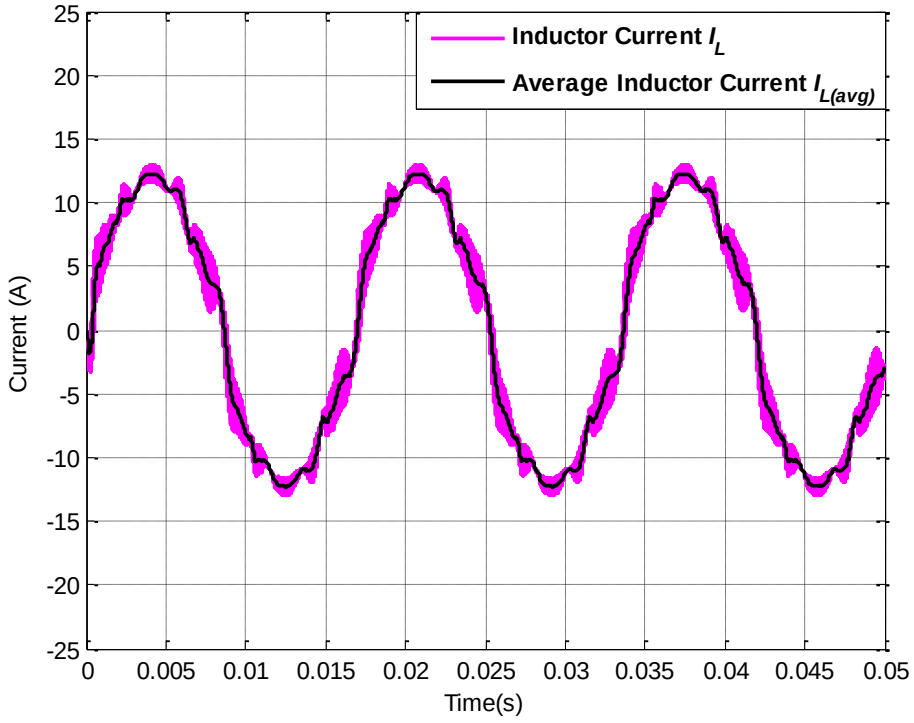


Figure 6.30: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario VIII

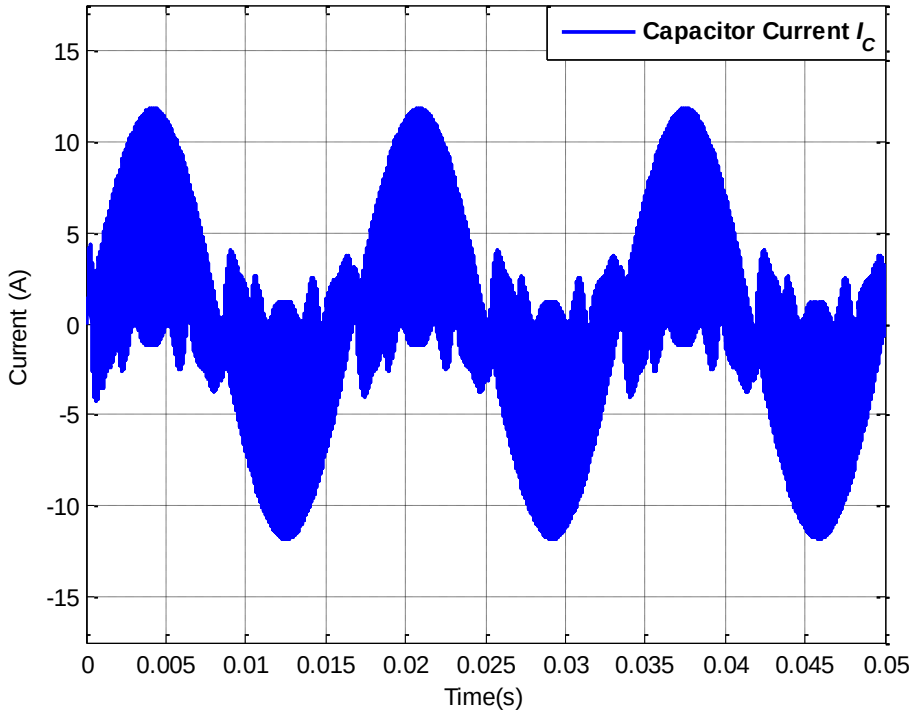


Figure 6.31: Actual capacitor current I_C for operating scenario VIII

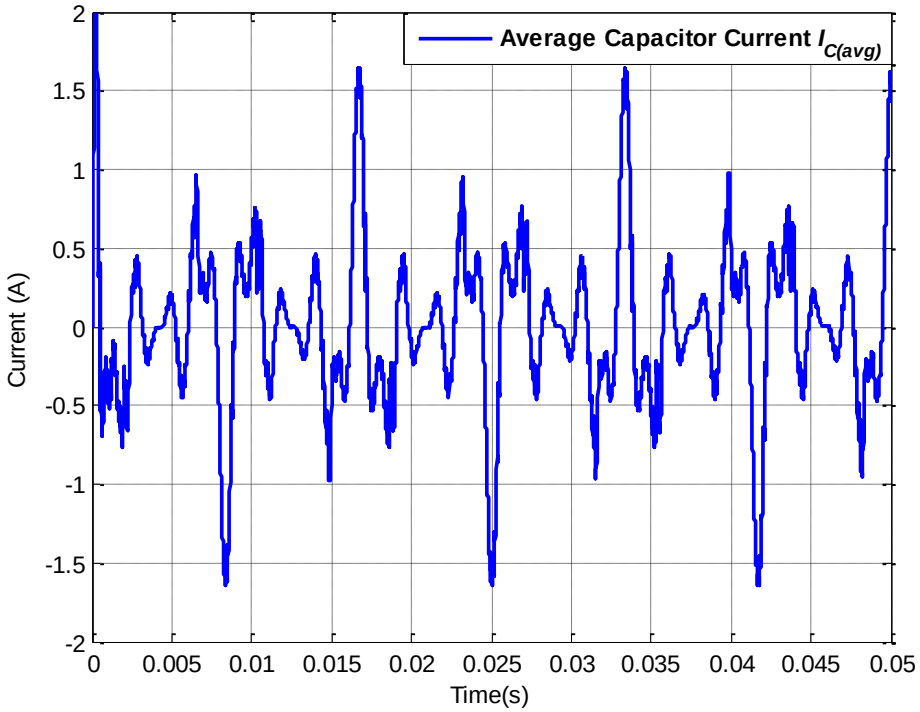


Figure 6.32: Average capacitor current $I_{C(avg)}$ for operating scenario VIII

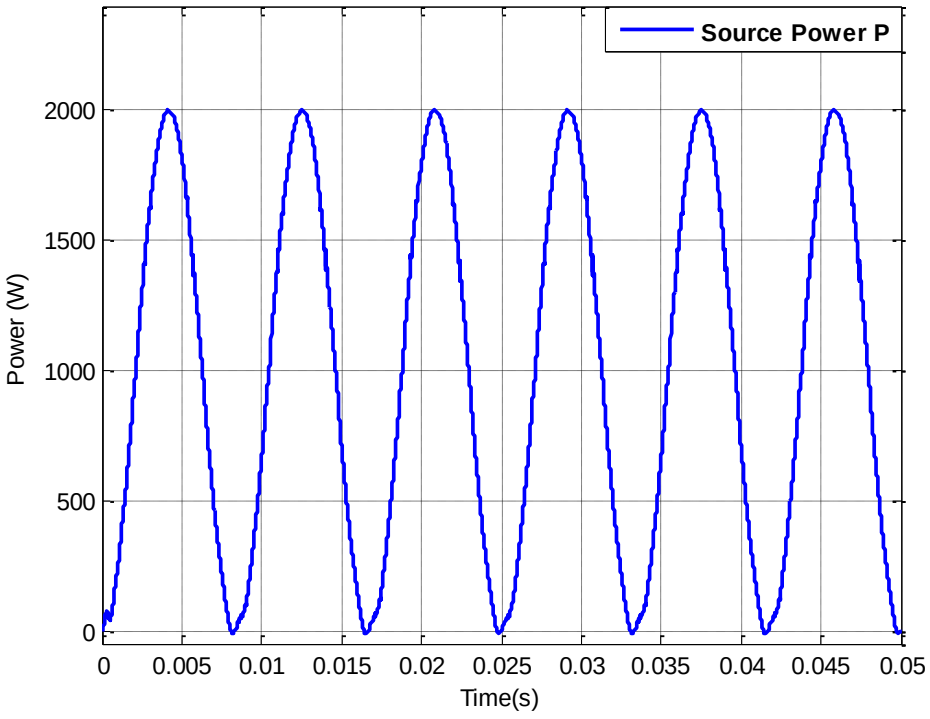


Figure 6.33: Grid power for operating scenario VIII

6.3.6 Combined harmonic distortion: Operating scenario IX

The performance of AC-DVR is simulated for combined harmonic distortion in source in previous scenario. The simulations for same type of disturbance with different types of harmonic order and their magnitude have been performed in this subsection. The source voltage has 3rd, 5th, 7th, 9th, 11th, and 13th harmonic with 33.33%, 20%, 14.29%, 11.11%, 9.09% and 7.69% magnitude which results in THD of 44.5% and RMS of 131.3V. The bidirectional bridge operates to change the source voltage polarity at each zero crossings of the error voltage. Then the wave shaper synthesizes the shape and magnitude of series injection voltage from the output of bridge. That voltage is injected in series with source voltage and load voltage is restored with 119.9V RMS and 6.35% of THD. The simulations for source voltage, bidirectional bride output, AC-DVR output and load voltage and current are presented in Figure 6.34, 6.35, 6.36 and 6.37 respectively.

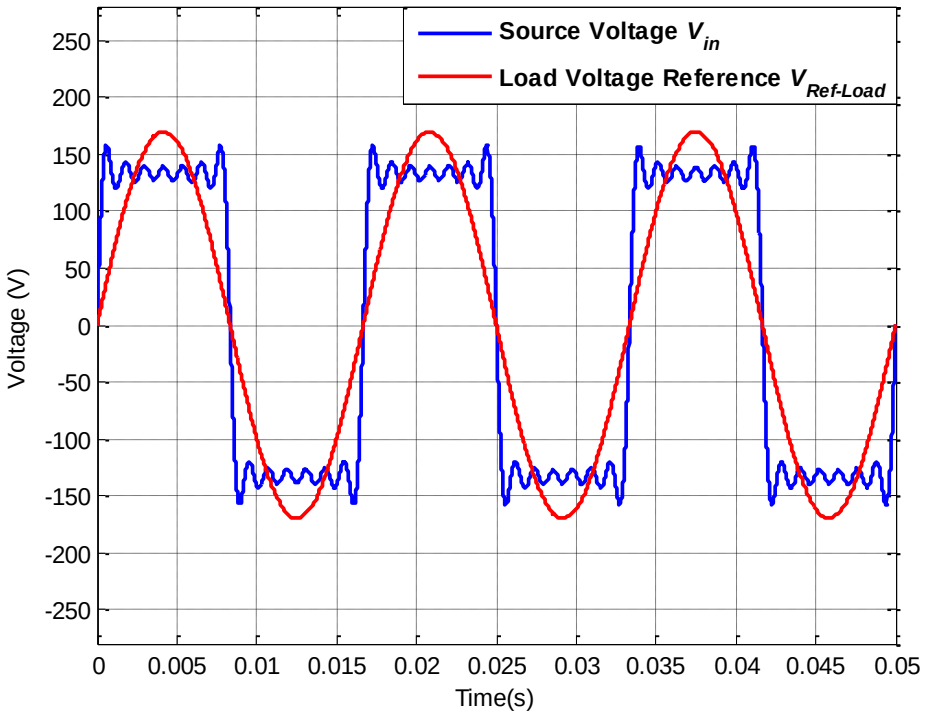


Figure 6.34: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario IX

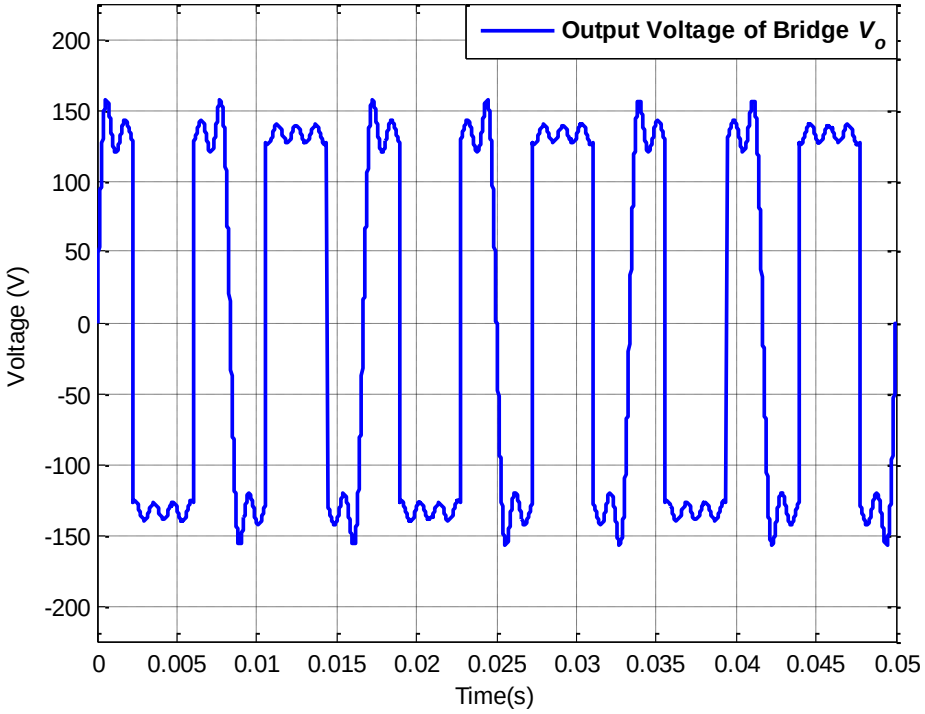


Figure 6.35: Bridge output voltage V_o for operating scenario IX

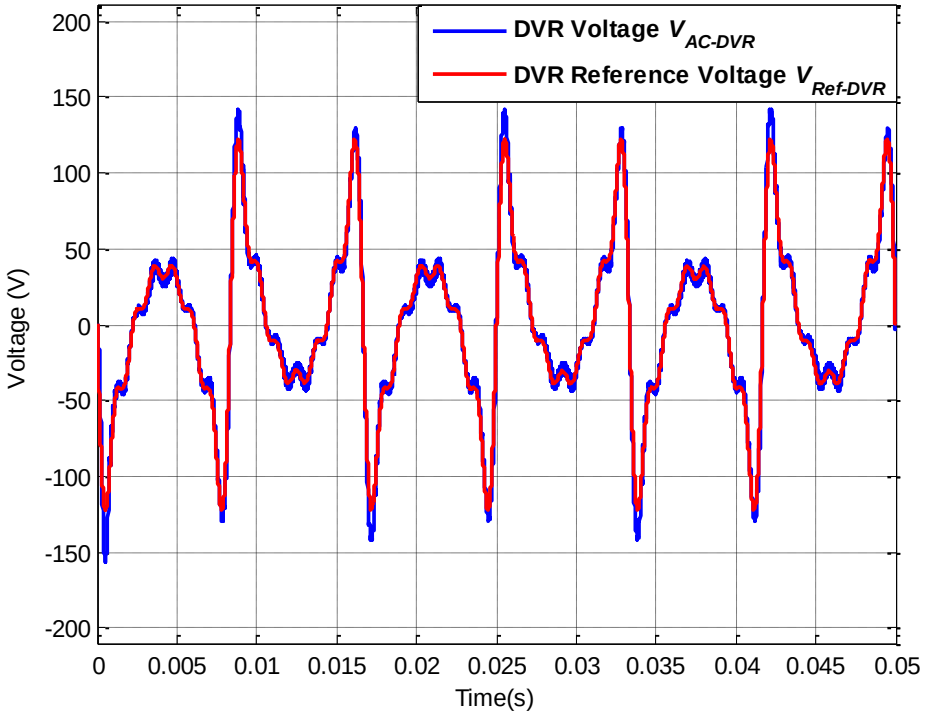


Figure 6.36: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario IX

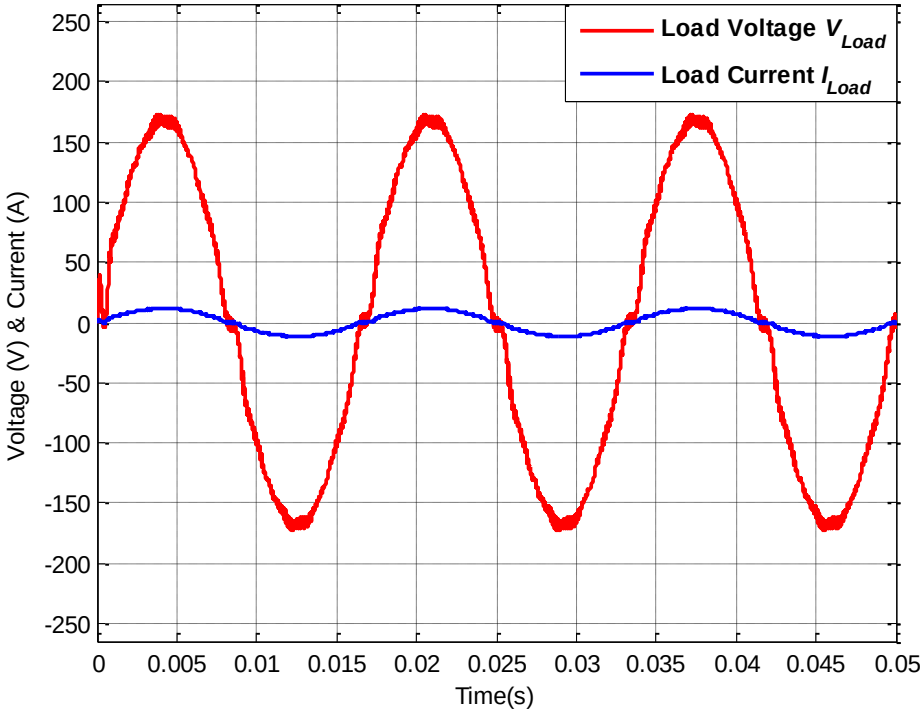


Figure 6.37: Load voltage V_{Load} and load current I_{Load} for operating scenario IX

6.3.7 Voltage sag: Operating scenario X

In previous scenarios both individual and combined harmonic disturbances were discussed. In this scenario, the performance of AC-DVR under voltage sag condition is validated. The source experiences 30% voltage sag as shown in Figure 6.38 thus RMS come to be 84V. The bidirectional bridge provides 180° out of phase source voltage to the AC-AC buck boost converter and the wave shaper synthesizes the voltage which needs to be added to restore the load voltage to 120V RMS. The simulation results for source voltage, bidirectional bridge output and output of AC-DVR are depicted in Figure 6.38, 6.39 and 6.40 respectively. The voltage synthesized by AC-DVR is added in series with source voltage via series transformer and load voltage is restored to 119.7V RMS with 2.06% THD. The simulations for load voltage and current are shown in Figure 6.41.

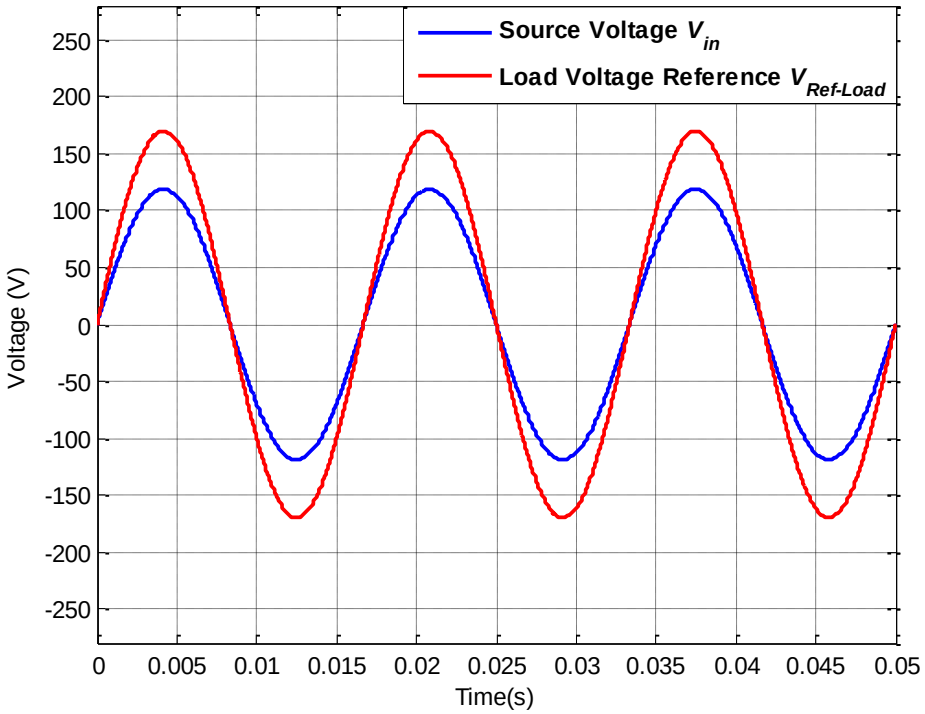


Figure 6.38: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario X

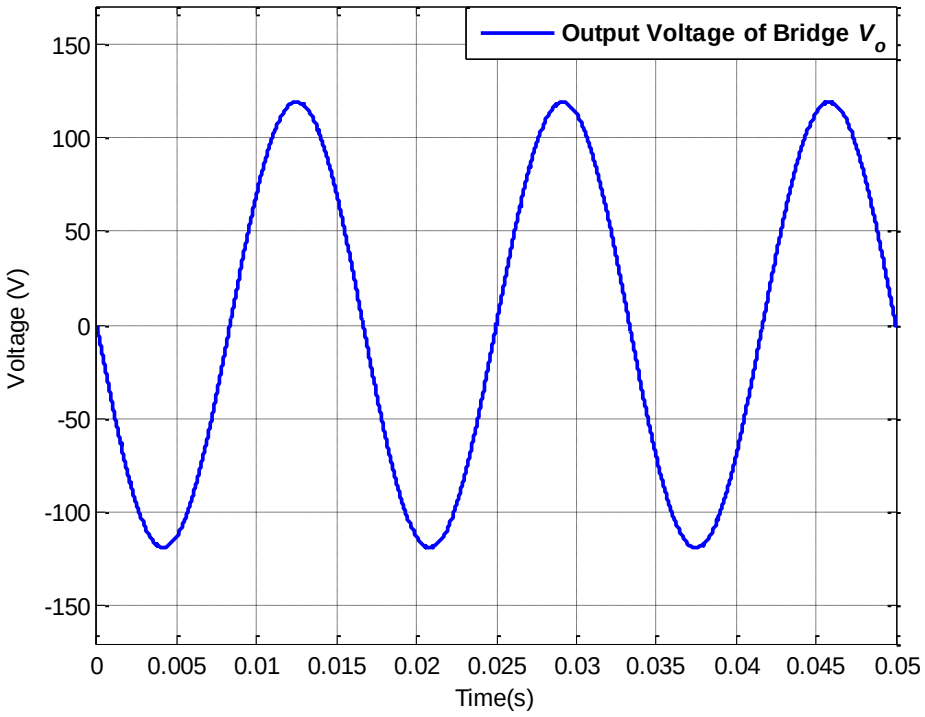


Figure 6.39: Bridge output voltage V_o for operating scenario X

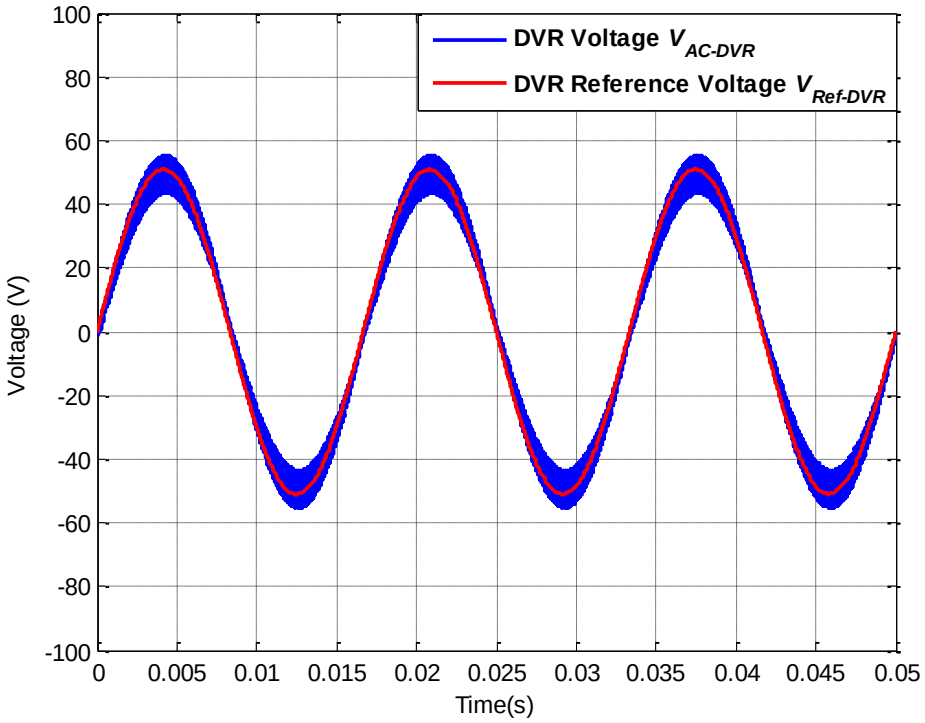


Figure 6.40: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario X

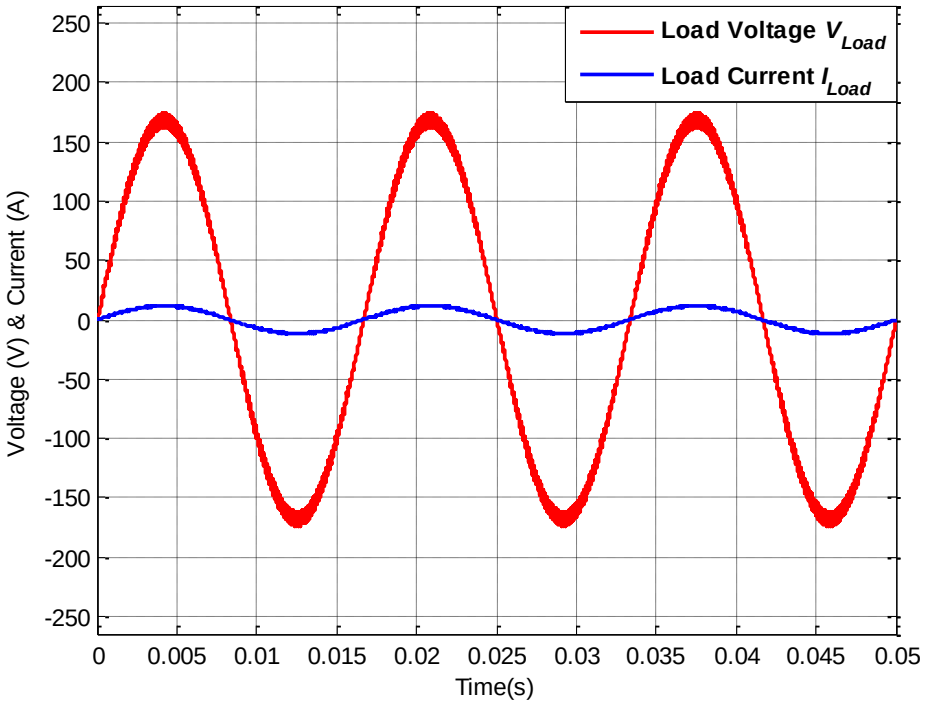


Figure 6.41: Load voltage V_{Load} and load current I_{Load} for operating scenario X

6.3.8 Voltage swell: Operating scenario XI

This operating condition has been created to evaluate the performance of AC-DVR under voltage swell or overvoltage type of disturbances. The source voltage contains 30% overvoltage which increases the RMS voltage from 120V to 156V. Thus, to restore the voltage to 120V RMS, the bidirectional bridge is operated to provide voltage same as source voltage at input terminals of the AC-AC buck boost. The AC-AC buck boost then synthesizes 180° out of phase voltage with appropriate magnitude form the output of bidirectional bridge. This voltage is added in series with the source and load voltage is restored to 120.2V RMS with 1.42% of THD. Simulations for source voltage experiencing 30% swell, output of bidirectional bridge, voltage synthesized by AC-DVR and load voltage and current are depicted in Figure 6.42, 6.43, 6.44 and 6.45 respectively.

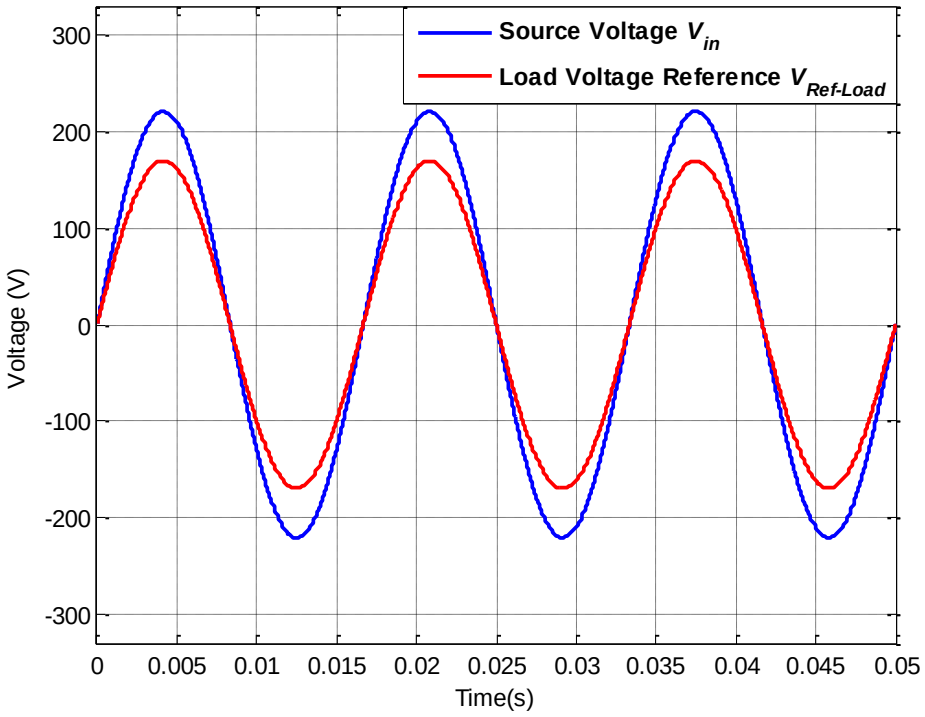


Figure 6.42: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario XI

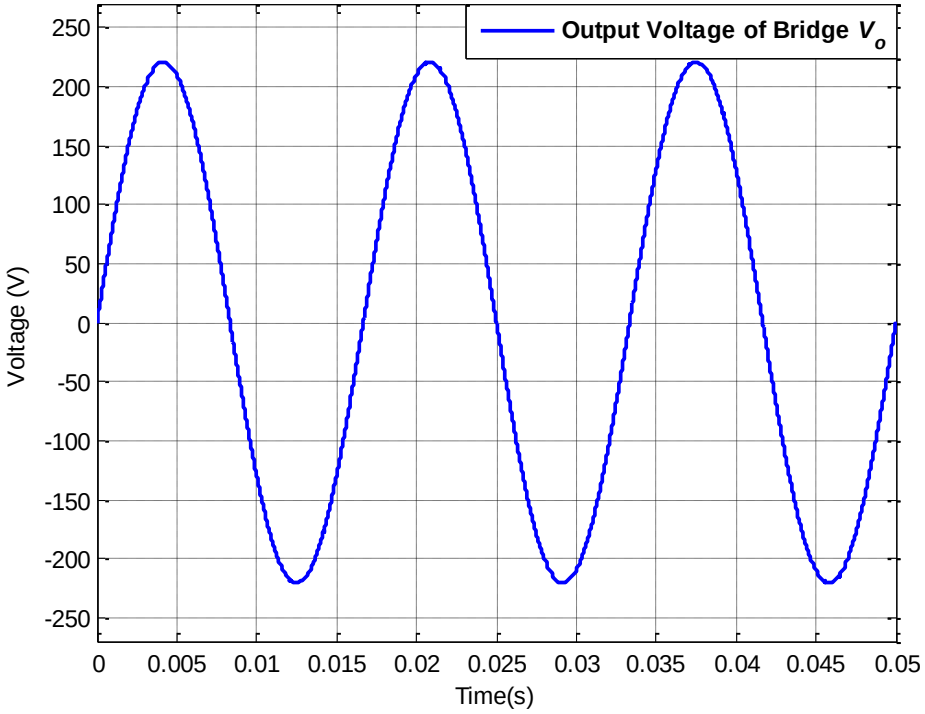


Figure 6.43: Bridge output voltage V_o for operating scenario XI

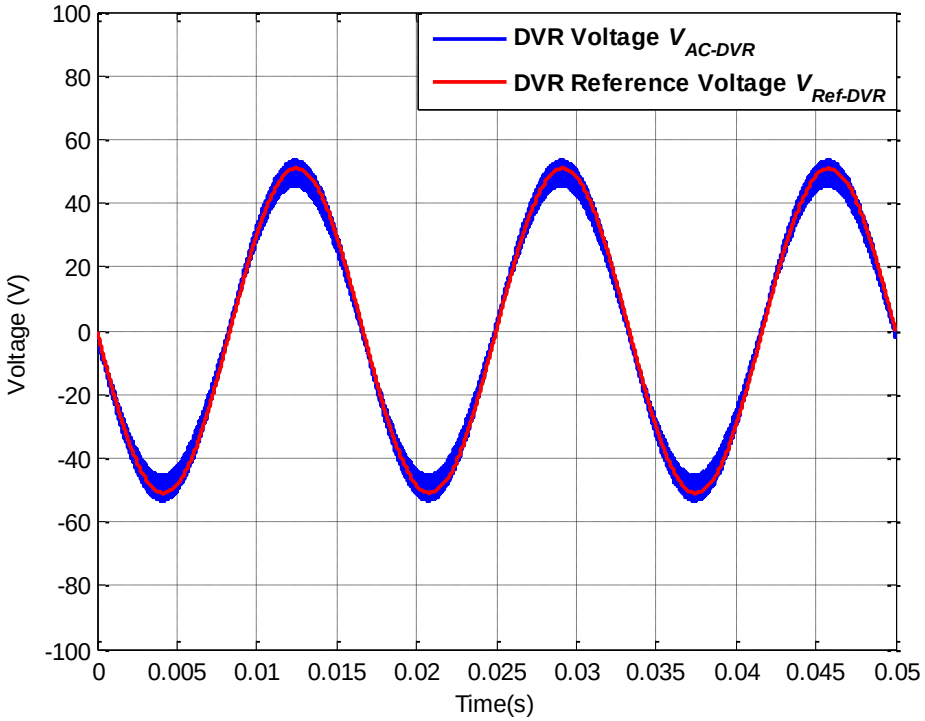


Figure 6.44: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario XI

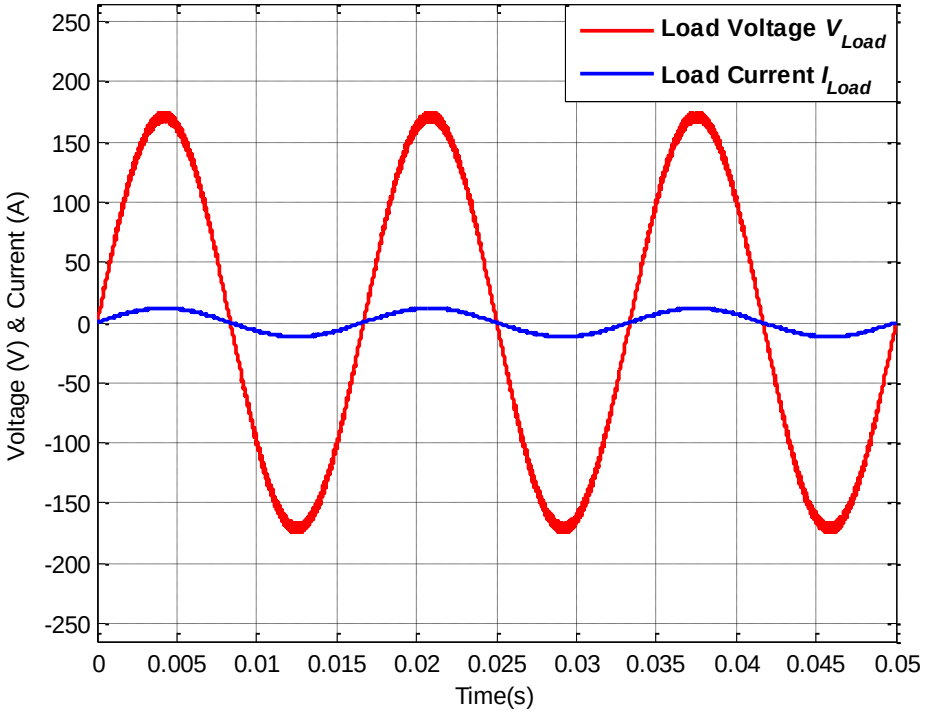


Figure 6.45: Load voltage V_{Load} and load current I_{Load} for operating scenario XI

6.3.9 Combined harmonic and voltage sag: Operating scenario XII

In this operating scenario, behavior of AC-DVR is validated for combination of two different types of disturbances which will be harmonics and sag. The source experiences harmonic distortion of same orders as discussed in scenario VIII with magnitudes of 10%, 11%, 6.25%, 2.5% and 2.5% with THD of 16.68% and 20% voltage sag as shown in Figure 6.46. The sensing unit of the system generates the reference for AC-AC buck boost and the bidirectional bridge is switched to provide positive and negative portions when needed from source voltage as shown in Figure 6.47. The AC-AC buck boost shapes the needed voltage with appropriate magnitude as shown in Figure 6.48 which is injected in series with source voltage via series transformer and the load voltage is restored to 119.7V RMS with 1.95% THD as shown in Figure 6.49.

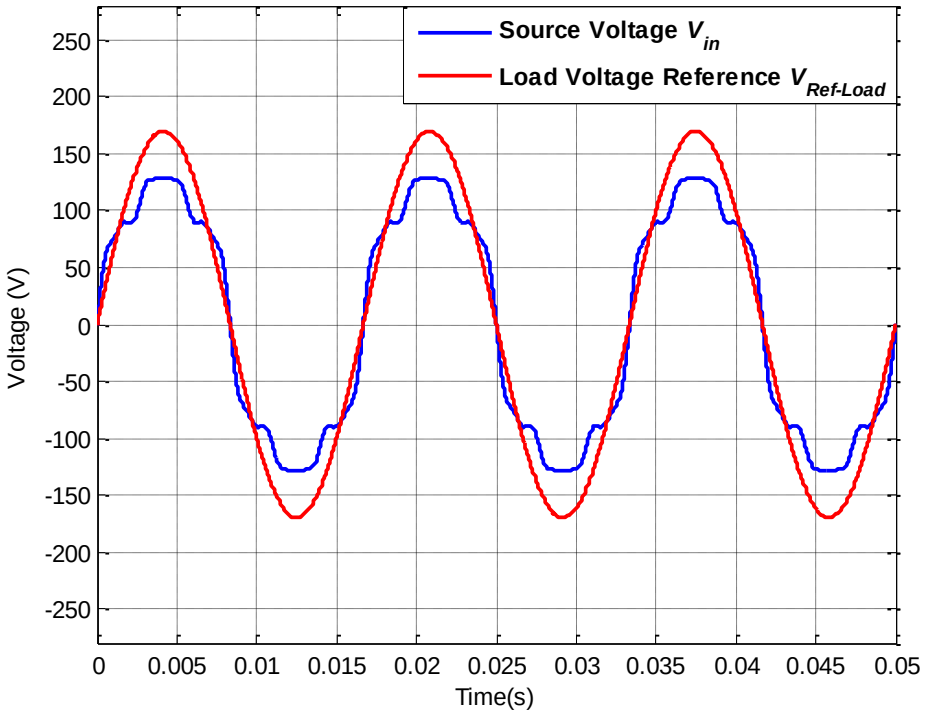


Figure 6.46: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario XII

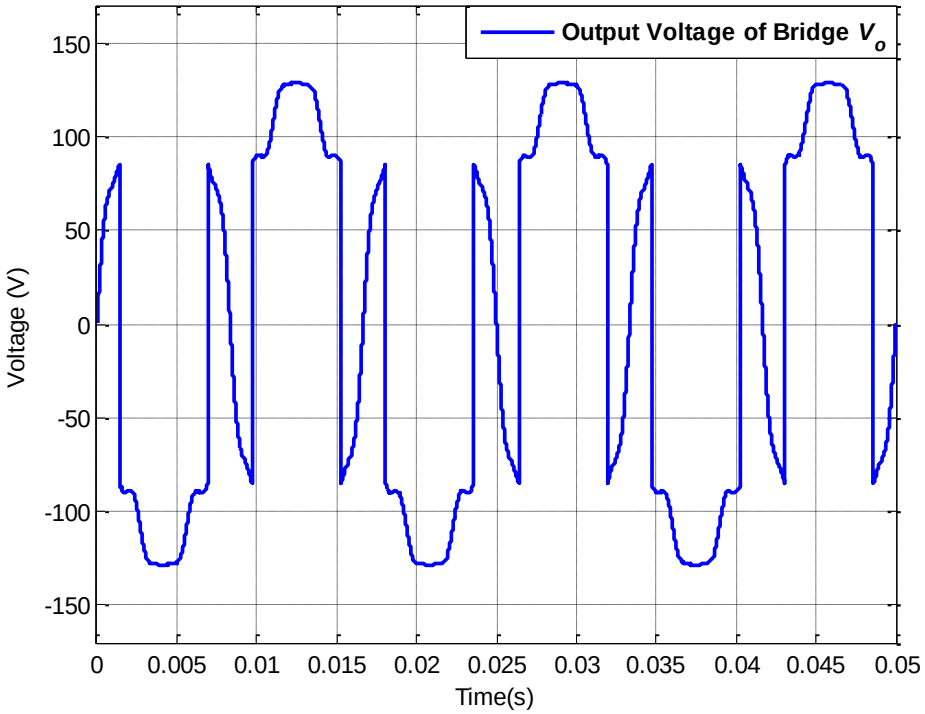


Figure 6.47: Bridge output voltage V_o for operating scenario XII

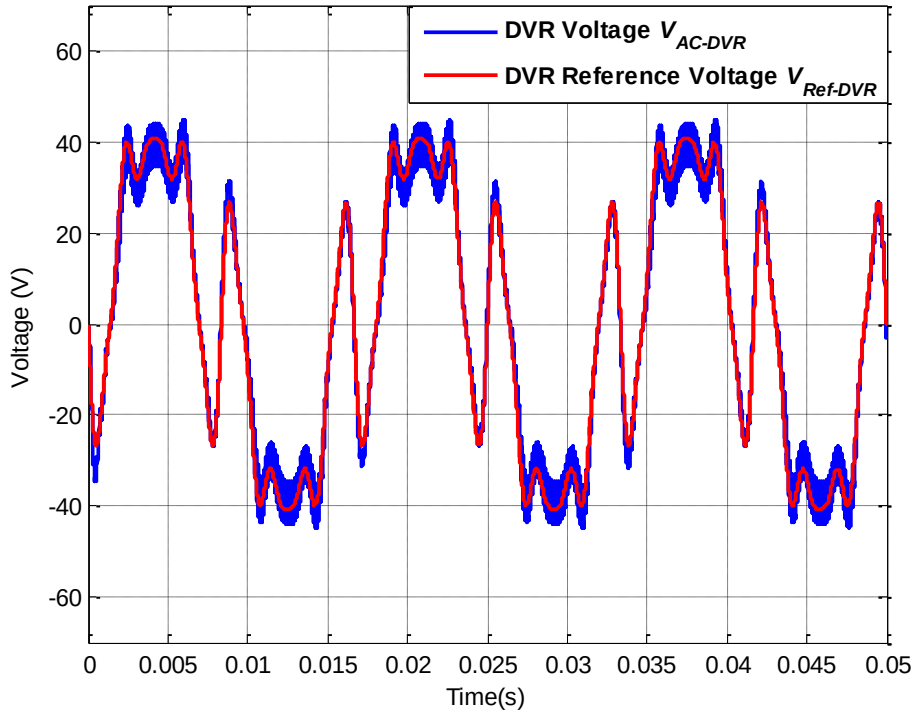


Figure 6.48: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario XII

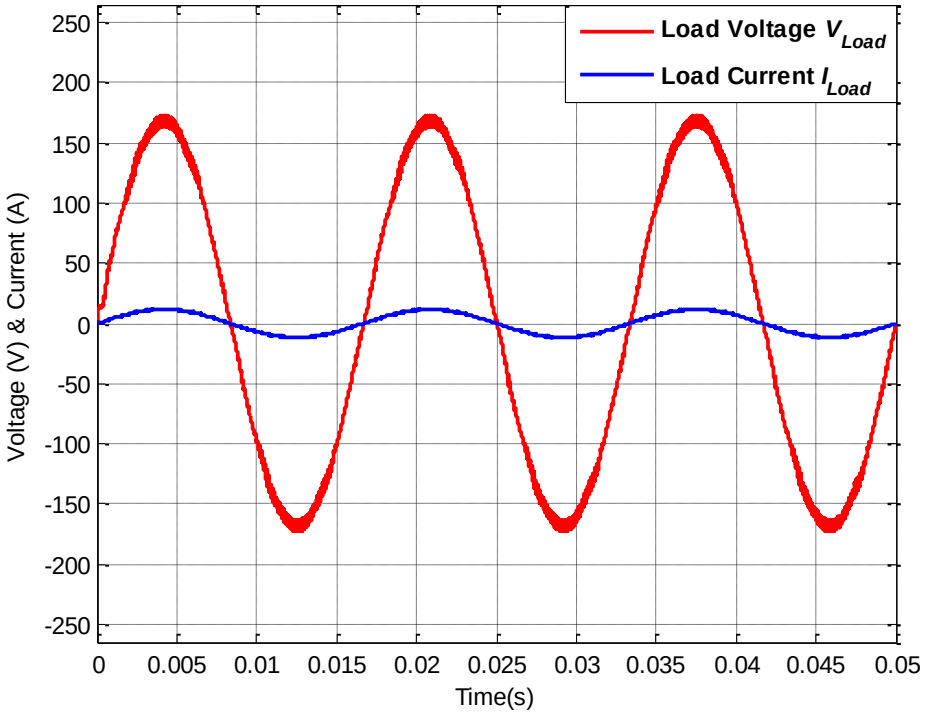


Figure 6.49: Load voltage V_{Load} and load current I_{Load} for operating scenario XII

6.3.10 UNC Charlotte service voltage: Operating scenario XIII

In this operating scenario, simulations for behavior of AC-DVR under more realistic grid conditions have been performed. The grid voltage available at 120V power outlet at UNC Charlotte is used for this scenario. The voltage at UNC Charlotte's outlet contains 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th} and 13^{th} order harmonics with magnitudes of 1.78%, 3.36%, 1.6%, 0.19%, 2.52%, and 1.43% with THD of 5.12% and 116V RMS. The source voltage is shown in Figure 6.50. The working of bidirectional bridge and AC-AC buck boost converter is same as discussed before. Such as, the source voltage is compared with 120V RMS sinusoid signal and error voltage is generated. The AC-AC buck boost converter should be switched to synthesize this error voltage to eliminate it from load voltage. Thus, bidirectional bridge is switched to provides positive and negative portions from source voltage whenever the error voltage is negative or positive respectively. The simulated output voltage for bidirectional bridge is depicted in Figure 6.51. The AC-AC converter then synthesizes the error voltage with desired shape and magnitude which is injected in series with the source voltage via series transformer. The voltage synthesized by AC-DVR is presented in Figure 6.52. Thus, load voltage is restored to 120V RMS with 1.06% of THD. The simulation results for load voltage and current are presented in Figure 6.53. Also, results for AC-DVR current, Inductor current, actual capacitor current and averaged capacitor current are presented in Figure 6.55, 6.56, 6.57 and 6.58 respectively. As discussed in previous subsections, these currents follow their respective equations stated in chapter 4. The actual and average source currents are depicted in Figure 6.54 which is governed by Eq. (18) resulting almost sinusoidal power extraction from source as shown in Figure 6.59.

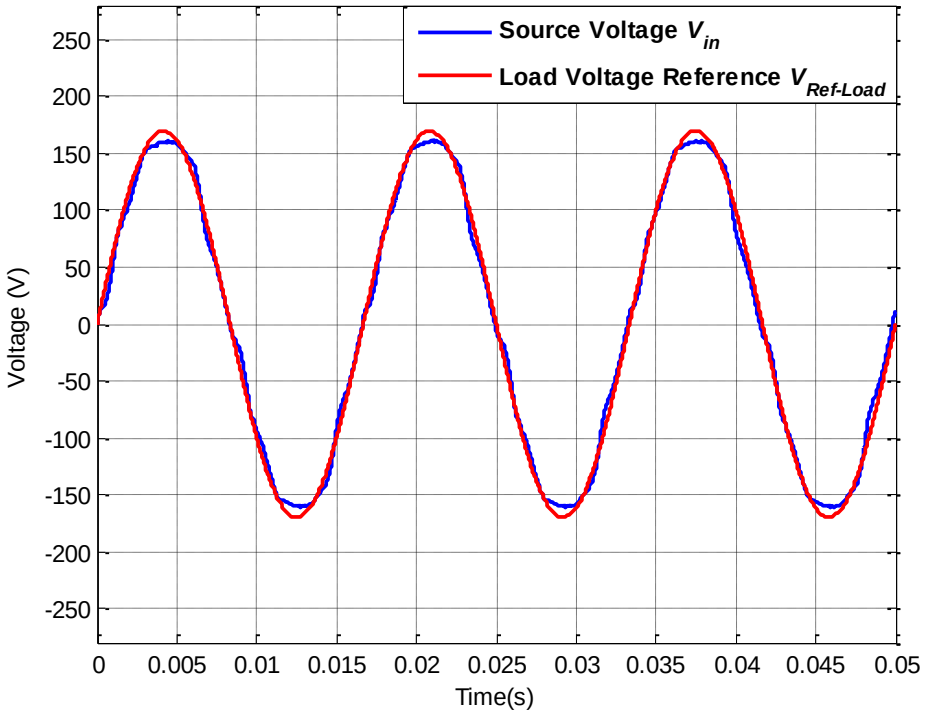


Figure 6.50: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario XIII

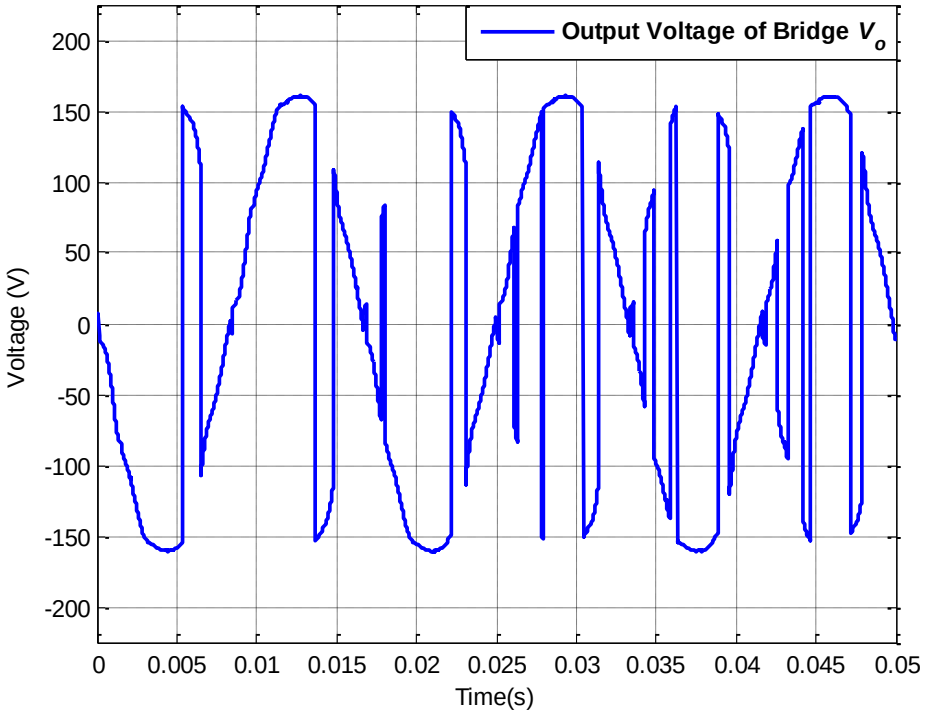


Figure 6.51: Bridge output voltage V_o for operating scenario XIII

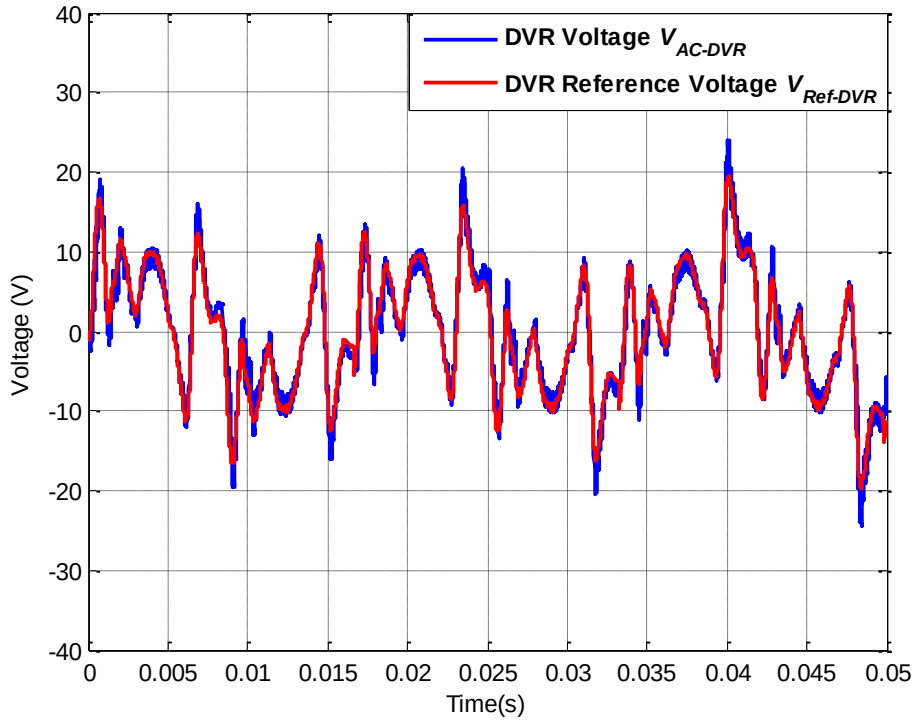


Figure 6.52: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario XIII

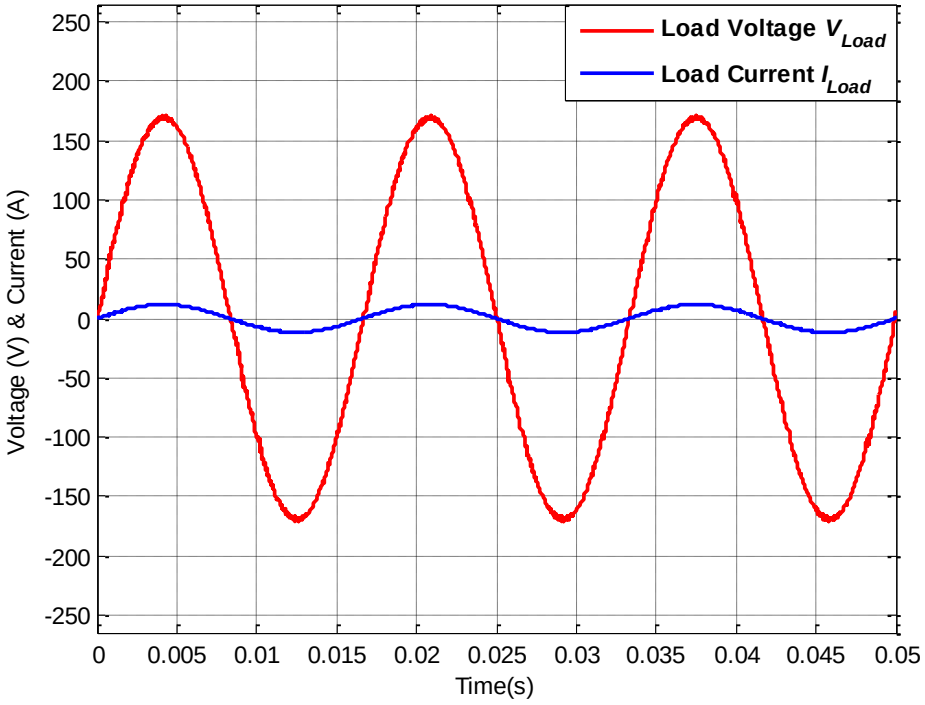


Figure 6.53: Load voltage V_{Load} and load current I_{Load} for operating scenario XIII

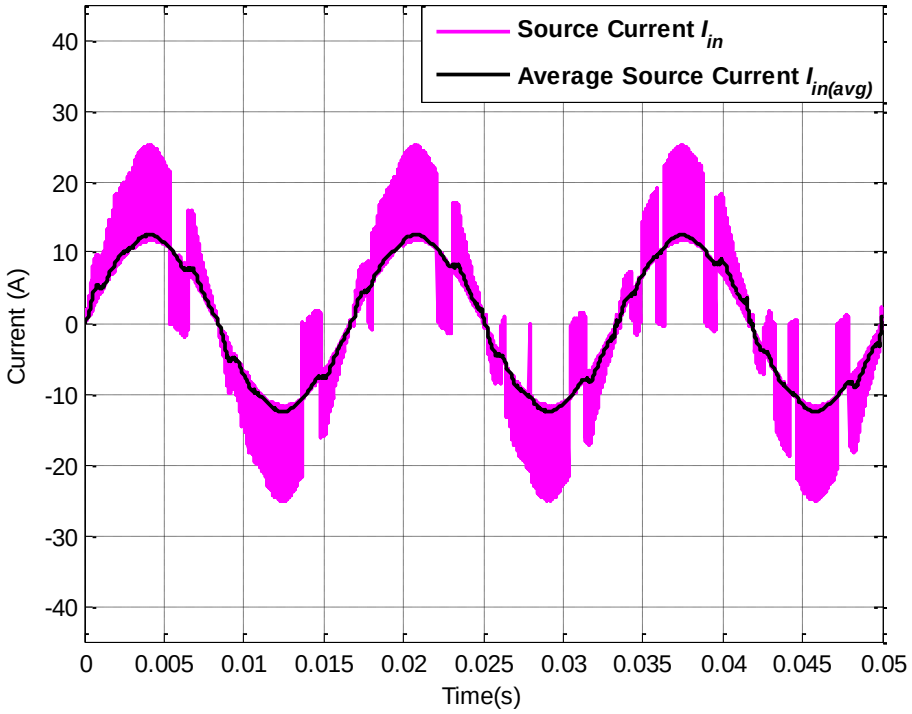


Figure 6.54: Actual source current I_{in} and average source current $I_{in(avg)}$ for operating scenario XIII

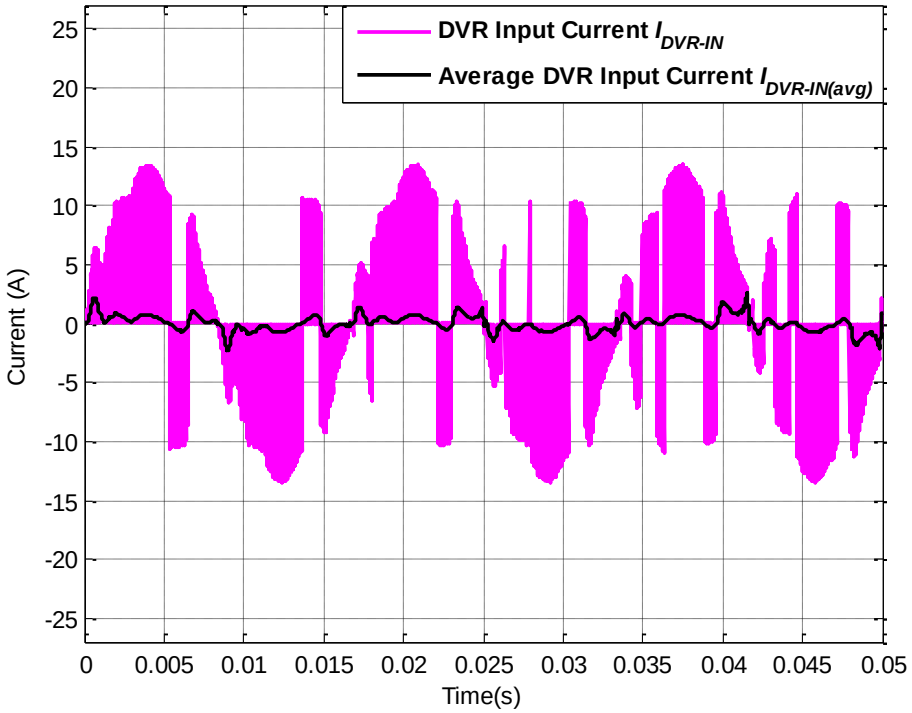


Figure 6.55: Actual DVR current I_{DVR-IN} and average DVR current $I_{DVR-IN(avg)}$ for operating scenario XIII

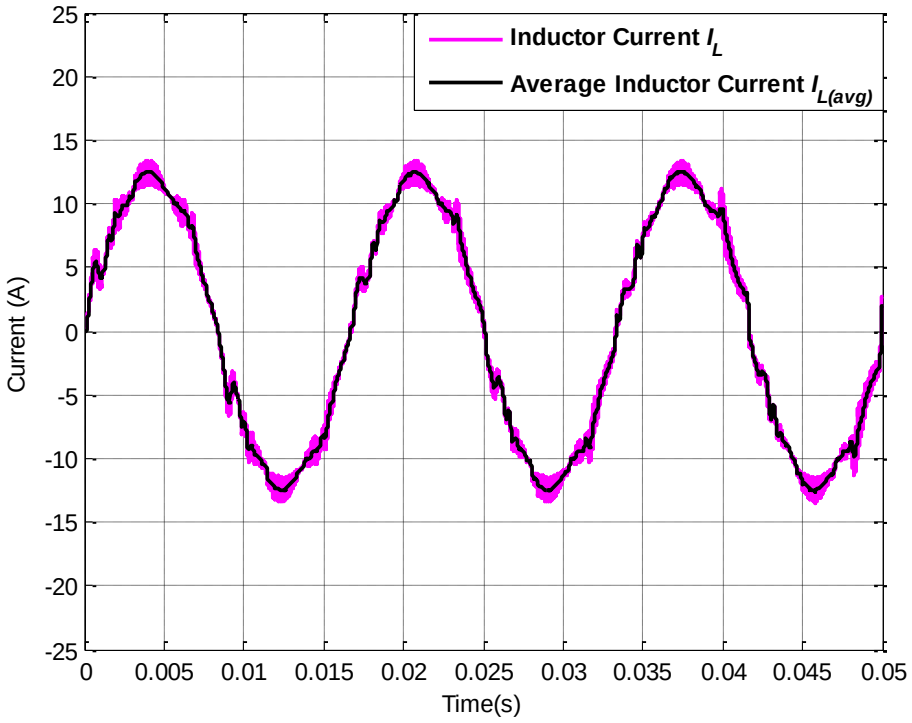


Figure 6.56: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario XIII

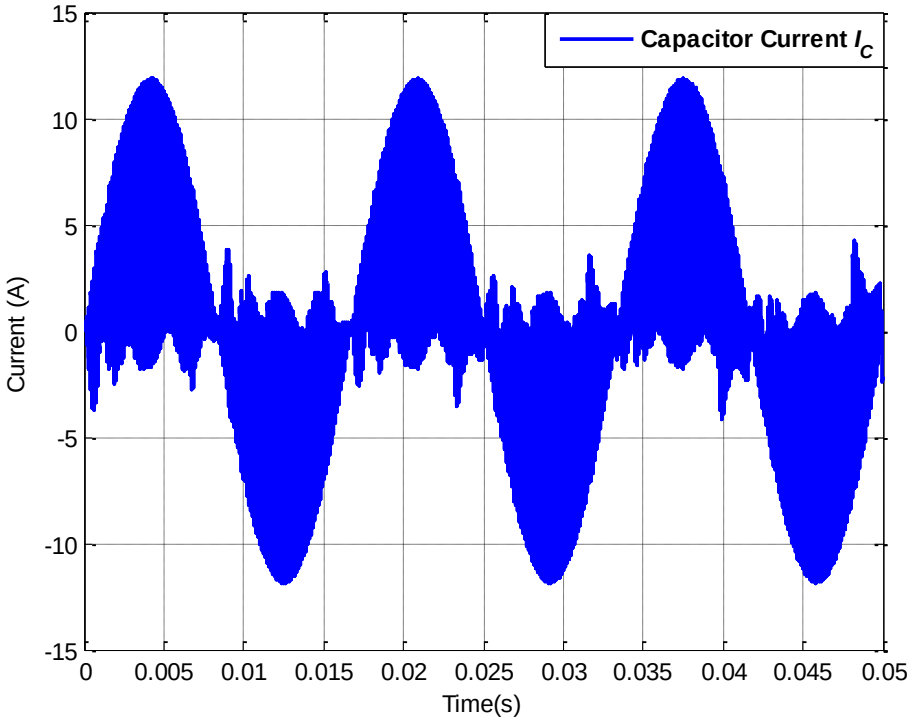


Figure 6.57: Actual capacitor current I_C for operating scenario XIII

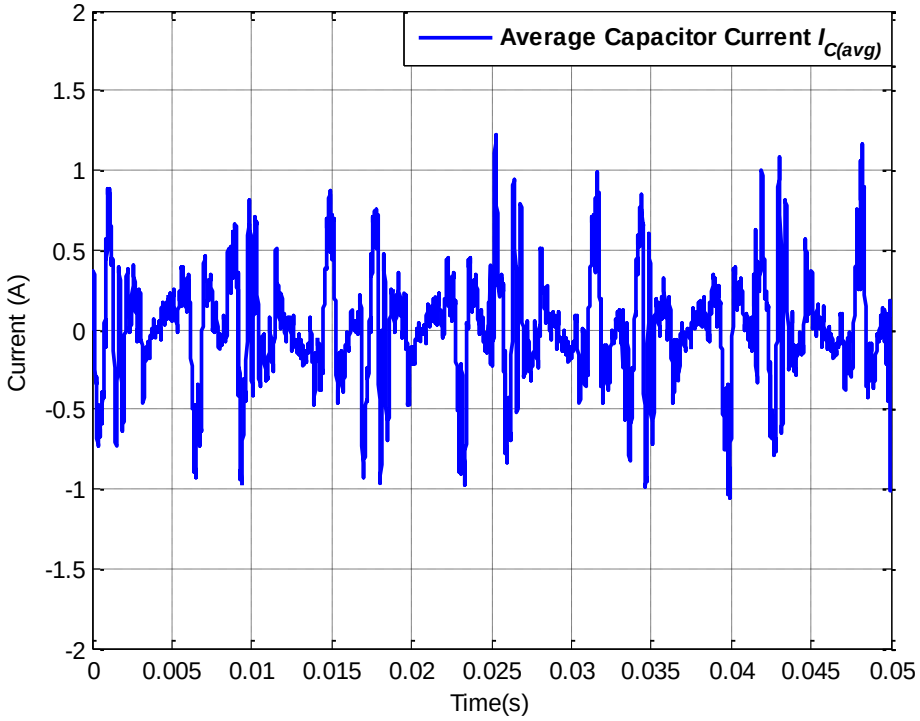


Figure 6.58: Average capacitor current $I_{C(avg)}$ for operating scenario XIII

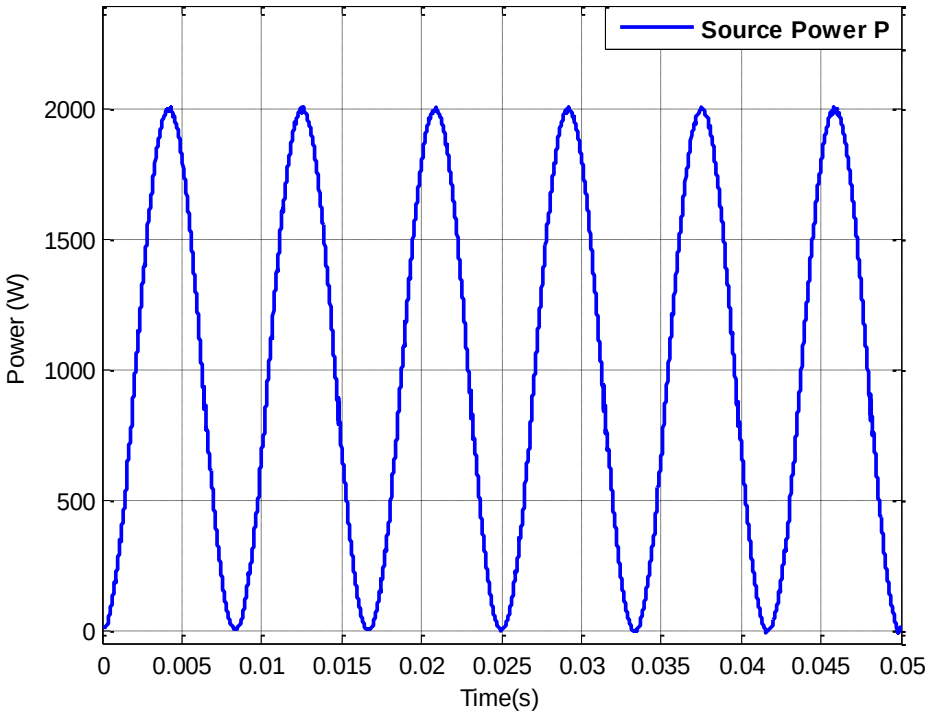


Figure 6.59: Grid power for operating scenario XIII

6.3.11 Step change in load under normal conditions: Operating scenario XIV

Effects of step change in load under normal grid conditions are simulated and presented in this operating condition. The source voltage with no disturbance is presented in Figure 6.60. The load is 14.4 Ω (1 kW) for time period $0 \leq t \leq 0.0208$ whereas the load changes to 9.6 Ω (1.5 kW) at t=0.0208 seconds and continues till t=0.05 seconds. The operation of bidirectional bridge and AC-AC buck boost is same as scenario I such as the bridge behaves as a rectifier and provides negative rectified voltage at the input terminals of AC-AC buck boost as shown in Figure 6.61 and AC-AC buck boost converter synthesizes almost zero voltage with transients at t=0.0208 seconds as duty cycle for AC-AC buck boost operation is zero as shown in Figure 6.62. Simulation results for load voltage and load current is presented in Figure 6.63. The transient effect of load change at t=0.0208 seconds on load voltage is also depicted in Figure 6.63.

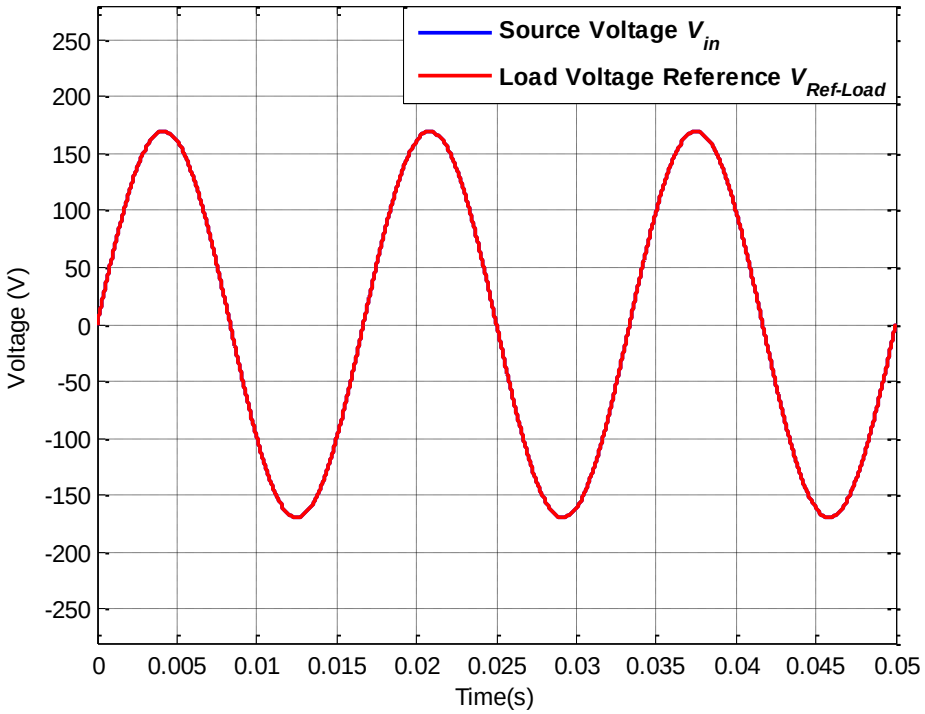


Figure 6.60: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario XIV

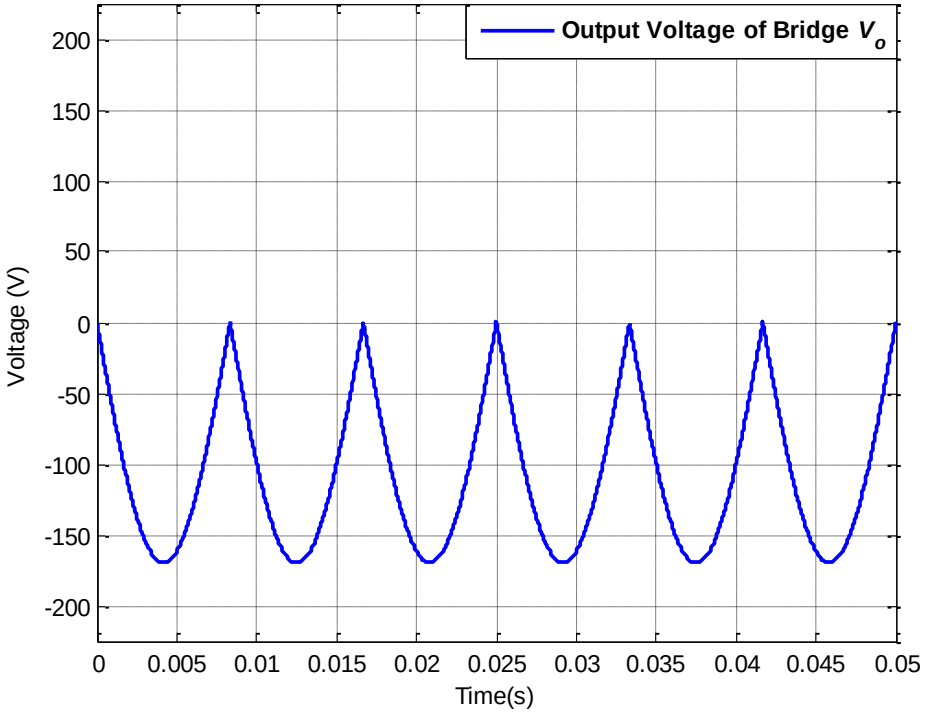


Figure 6.61: Bridge output voltage V_o for operating scenario XIV

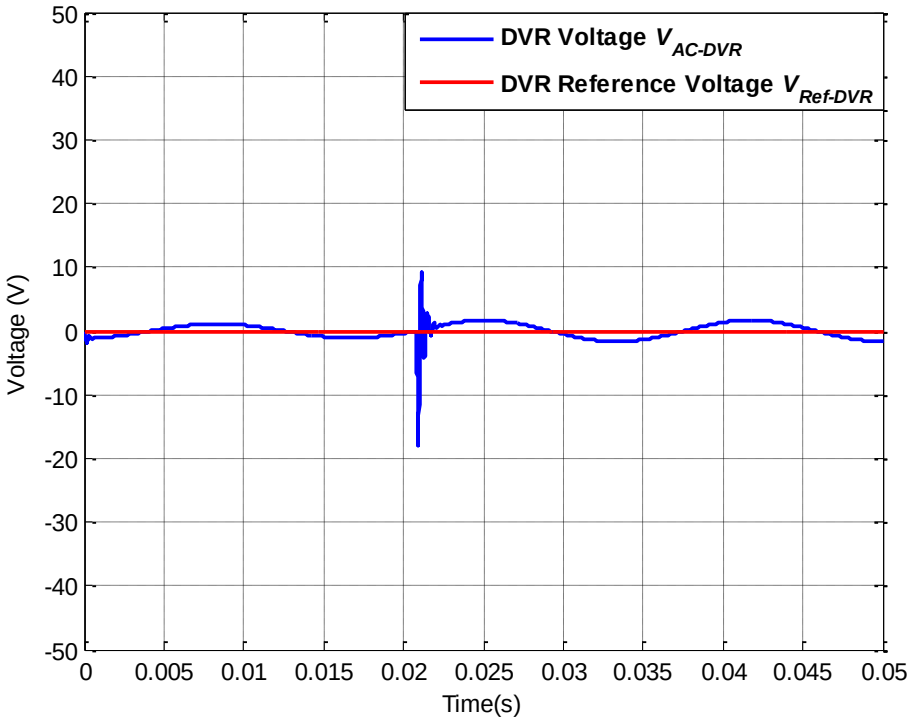


Figure 6.62: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario XIV

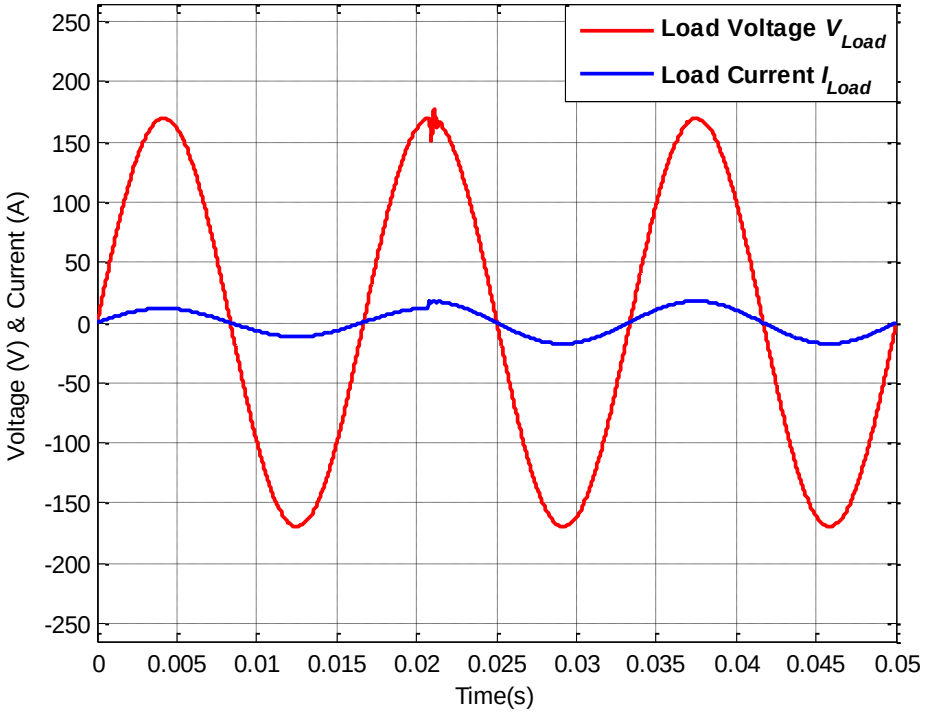


Figure 6.63: Load voltage V_{Load} and load current I_{Load} for operating scenario XIV

6.3.12 Step load change under combined harmonic distortion: Operating scenario XV

The behavior of proposed DVR for step change in load under normal grid condition has been discussed and presented in previous scenario. In this operating scenario, performance of proposed DVR for step load change under combined harmonic and sag distortion is discussed and simulation results are presented. The parameters for the grid voltage are same as for scenario XII discussed in subsection 6.3.9 such as 20% sag and harmonic voltage distortion at orders 3rd, 5th, 7th, 11th and 13th with magnitudes of 10%, 11%, 6.25%, 2.5% and 2.5% with THD of 16.68%. The load is 14.4 Ω (1 kW) for time period $0 \leq t \leq 0.0208$ and changed to 9.6 Ω (1.5 kW) at t=0.0208 seconds and continues till t=0.05 seconds. The source voltage is compared to 120V sinusoid reference as shown in Figure 6.64 and error voltage is generated. The bidirectional bridge operates

to provide positive and negative portions of source voltage to AC-AC buck boost converter according to error voltage polarity as shown in Figure 6.65. The AC-AC buck boost converter then shapes the output of bridge in terms of magnitude and shape of error voltage. The error voltage and output of AC-AC buck boost converter are presented in Figure 6.66. The error voltage generated by AC-AC converter is injected in series with source voltage via series transformer and load voltage is restored to 119.7V RMS with 1.95% and 2.62% THD for $0 \leq t \leq 0.0208$ and $0.0208 \leq t \leq 0.05$ respectively as depicted in Figure 6.67. The actual and average source currents, AC-DVR input currents, inductor currents and capacitor currents are presented in Figures 6.68-6.72. It can be observed that these currents are governed by their respective equations presented in chapter 4. The source power is almost sinusoidal and changes to 1500 kW from 1000 kW at t=0.0208 seconds as shown in Figure 6.73.

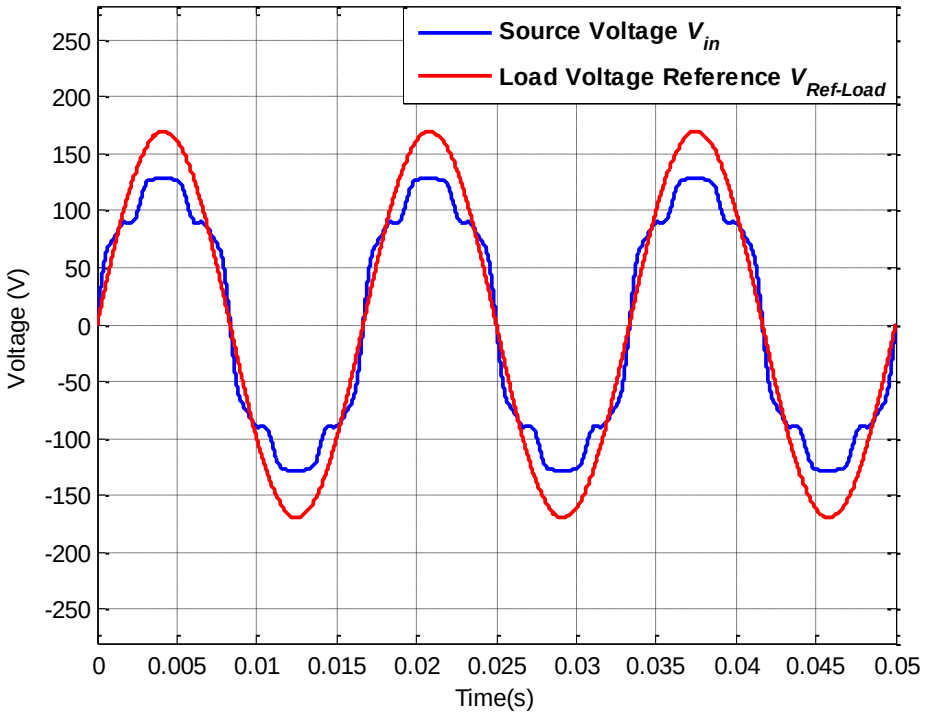


Figure 6.64: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario XV

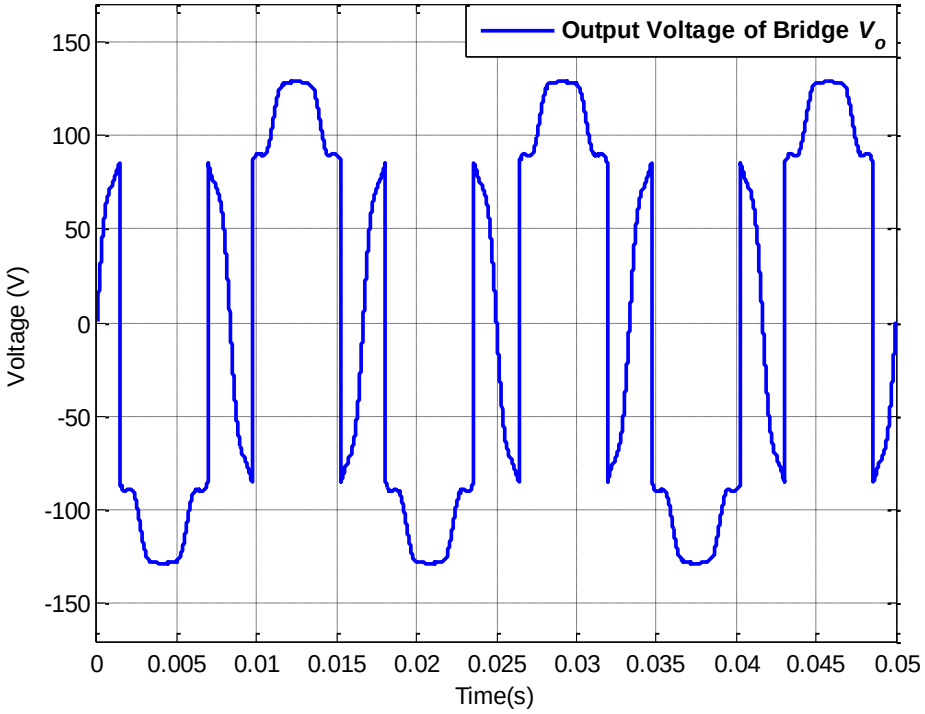


Figure 6.65: Bridge output voltage V_o for operating scenario XV

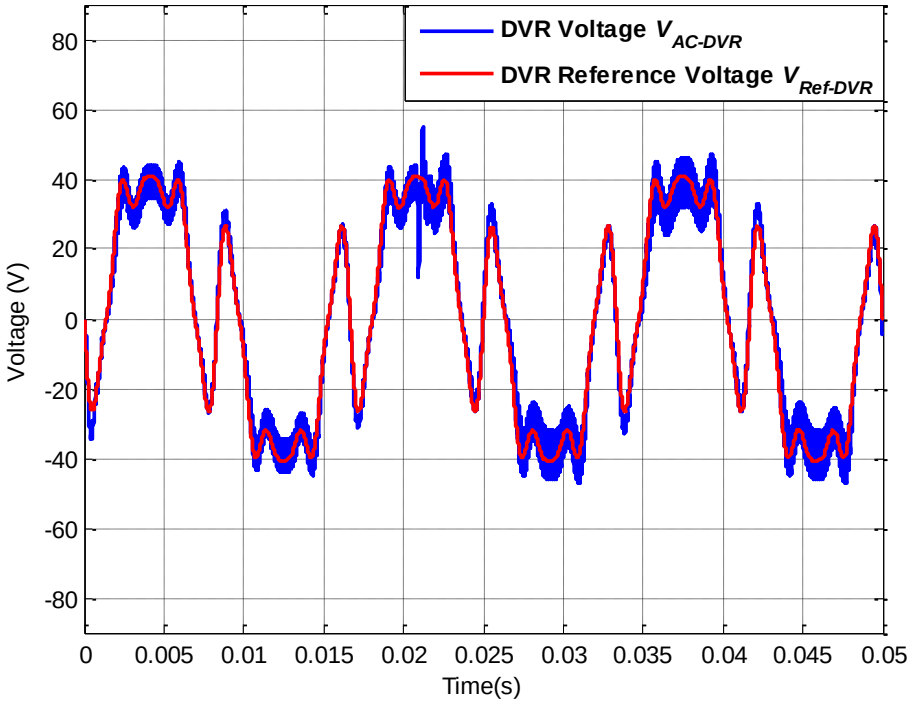


Figure 6.66: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario XV

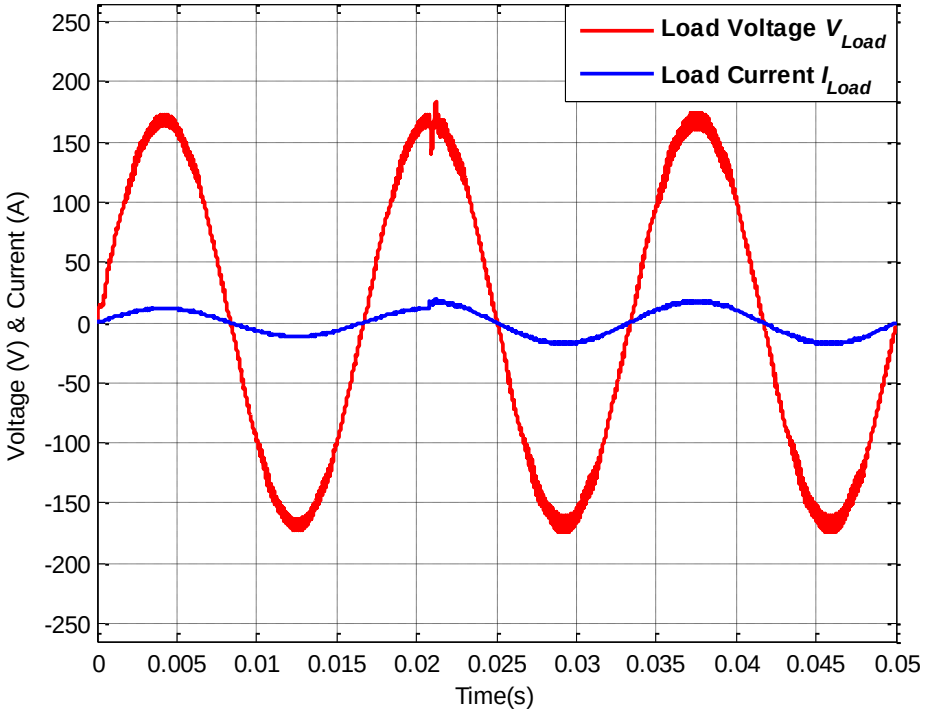


Figure 6.67: Load voltage V_{Load} and load current I_{Load} for operating scenario XV

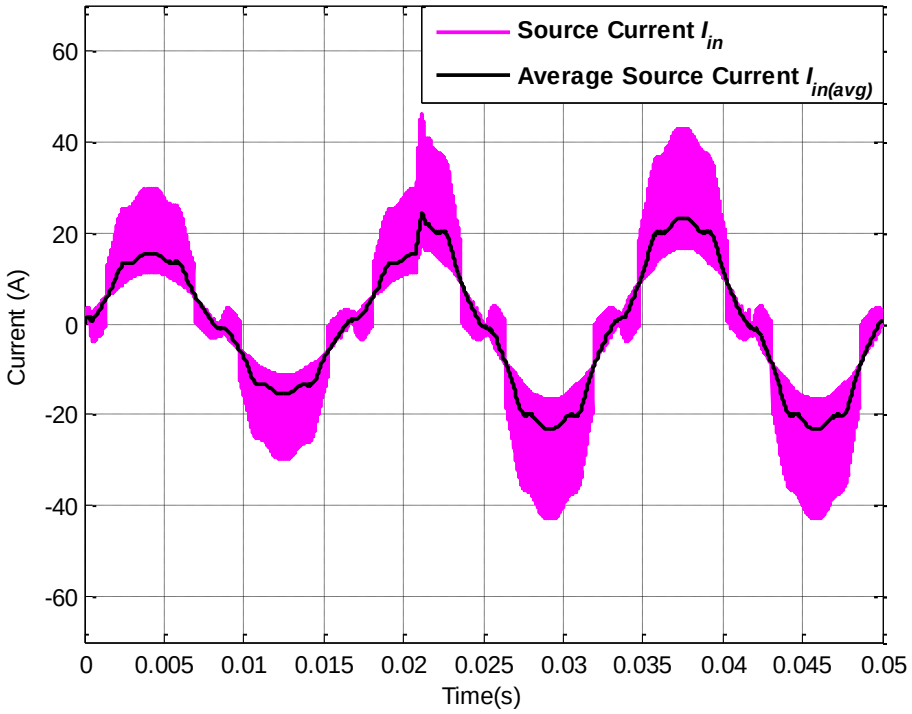


Figure 6.68: Actual source current I_{in} and average source current $I_{in(avg)}$ for operating scenario XV

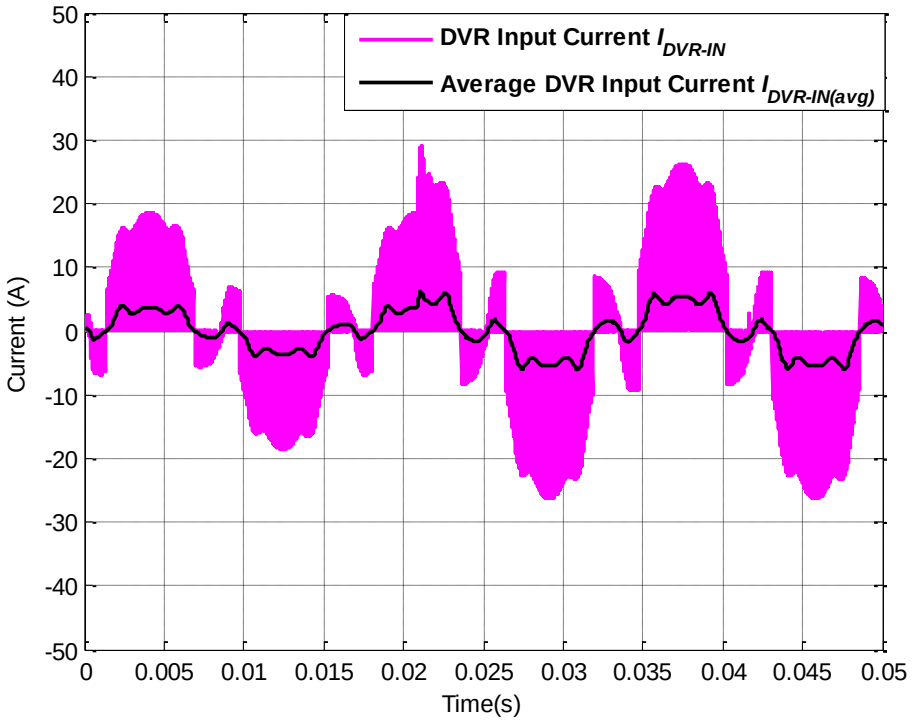


Figure 6.69: Actual DVR current I_{DVR-IN} and average DVR current $I_{DVR-IN(avg)}$ for operating scenario XV

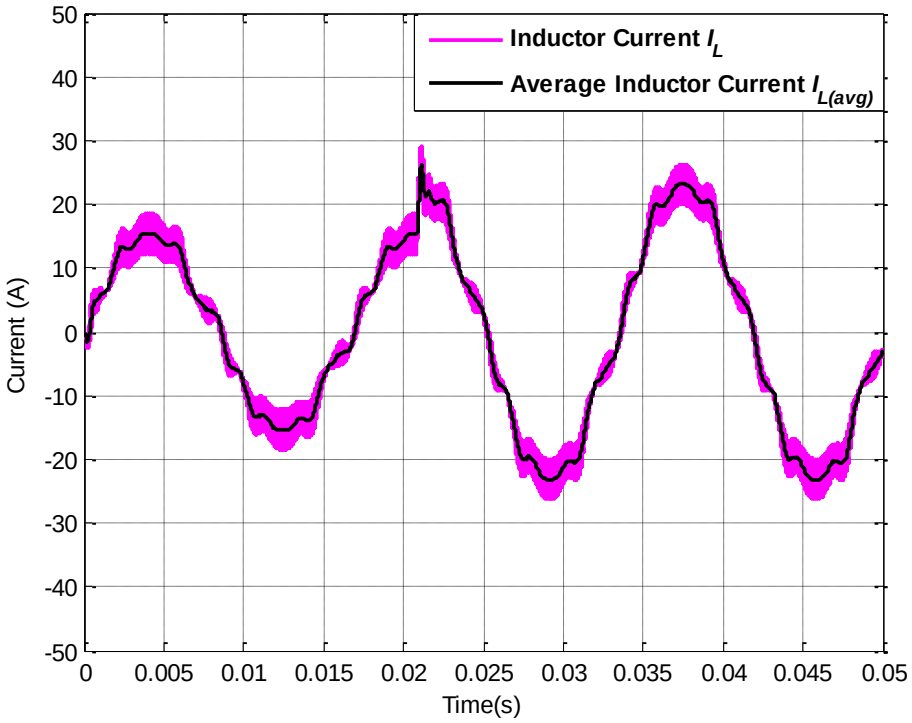


Figure 6.70: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario XV

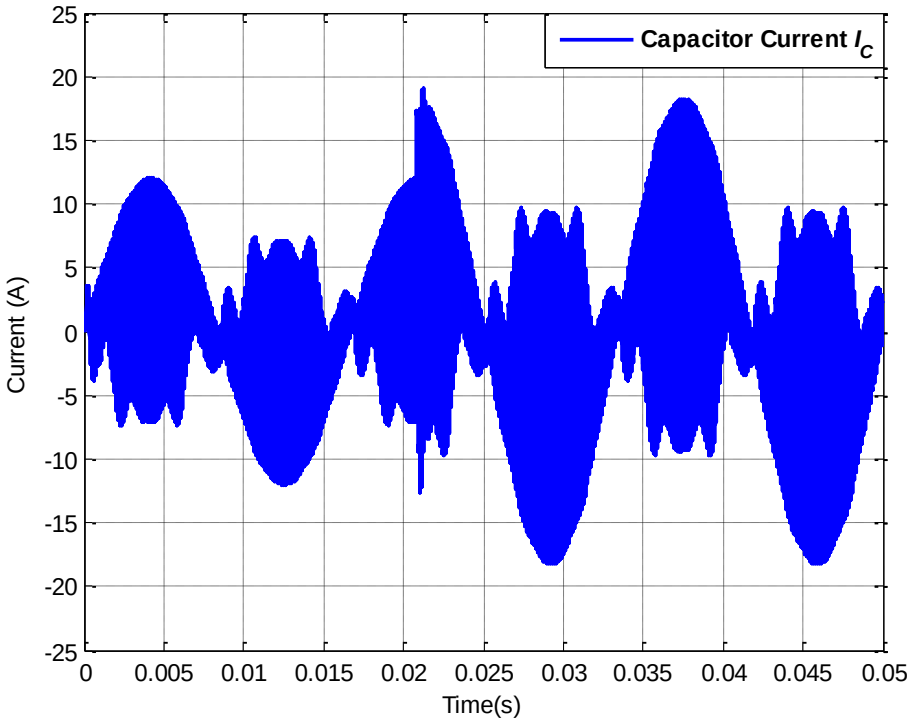


Figure 6.71: Actual capacitor current I_C for operating scenario XV

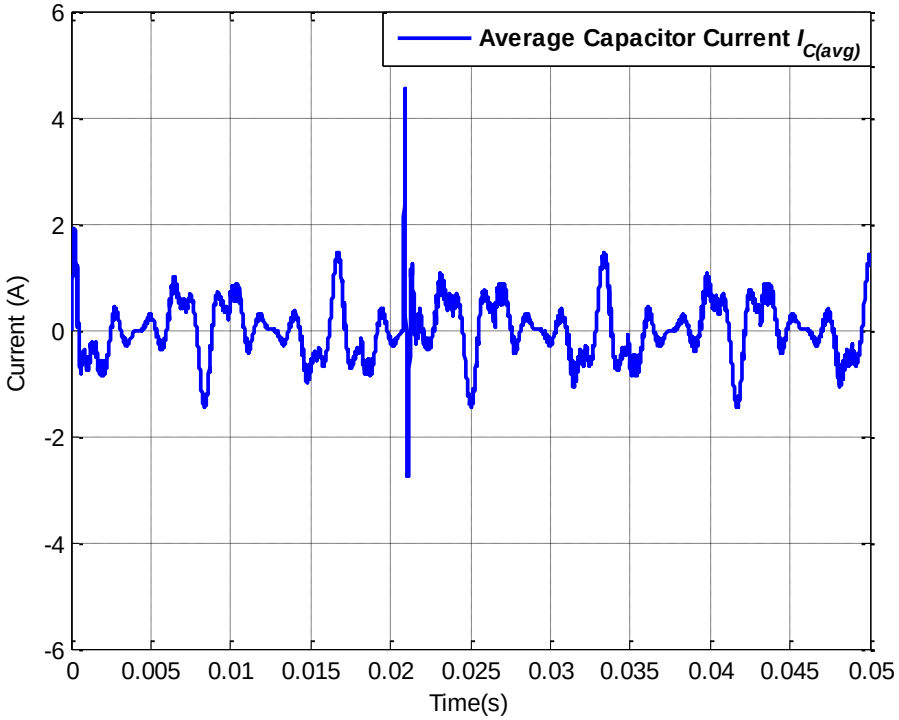


Figure 6.72: Average capacitor current $I_{C(avg)}$ for operating scenario XV

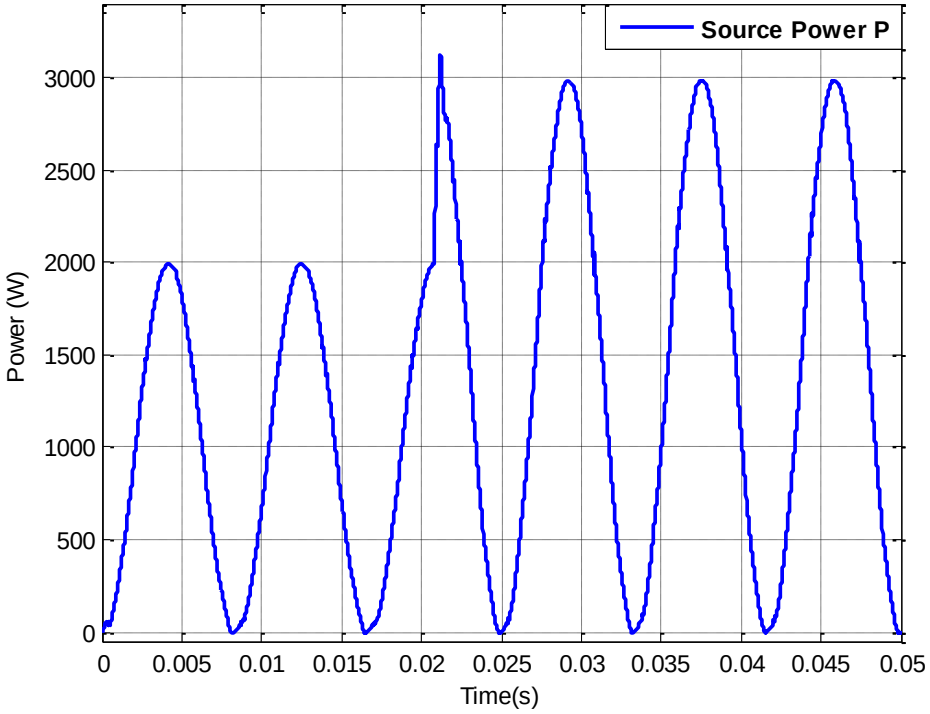


Figure 6.73: Grid power for operating scenario XIV

6.3.13 Step change in voltage swell: Operating scenario XVI

The simulations of AC-DVR for step change in load under various conditions were discussed and presented in previous scenarios. However, in this scenario simulations for step change in voltage swell have been performed. The source voltage experiences 20% voltage sag for 0 to 0.0208 seconds. At t=0.0208 second the swell is increased to 40% and continues till 0.05 seconds. The working of AC-DVR under this operating condition is same as discussed previously in subsection 6.3.8. The simulation results for source voltage, bidirectional bridge output voltage and AC-DVR voltage are presented in Figure 6.74, 6.78 and 6.79 respectively. The load voltage is restored to 121.1V with 1.07% THD for $0 \leq t \leq 0.0208$ and 120.3V with 1.68% THD for $0.0208 \leq t \leq 0.05$ after having some transients at t=0.0208 second for couple of milliseconds as shown in Figure 6.77.

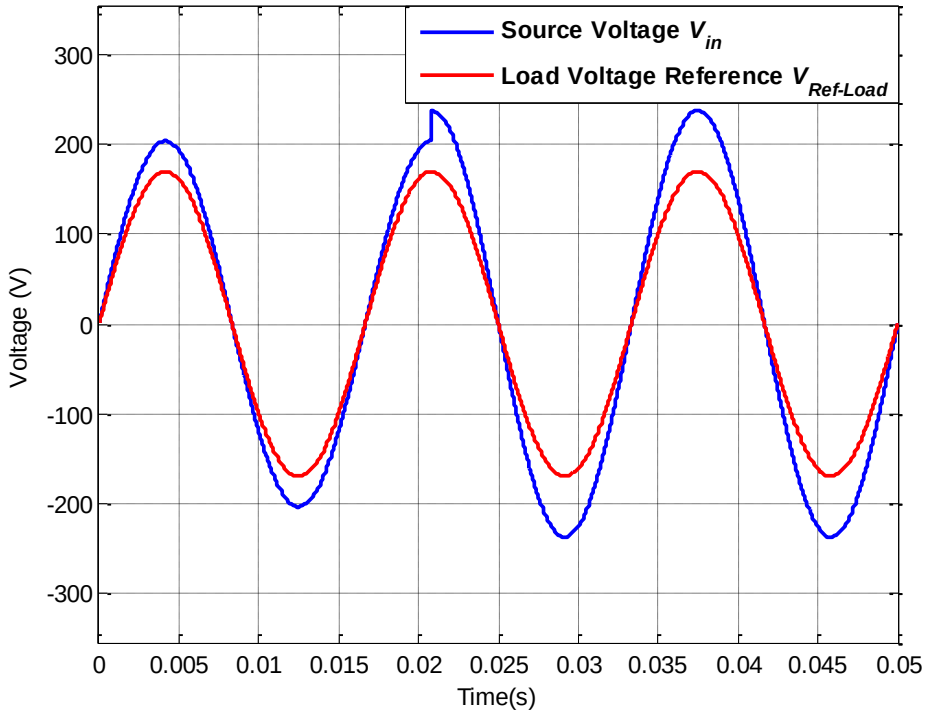


Figure 6.74: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario XVI

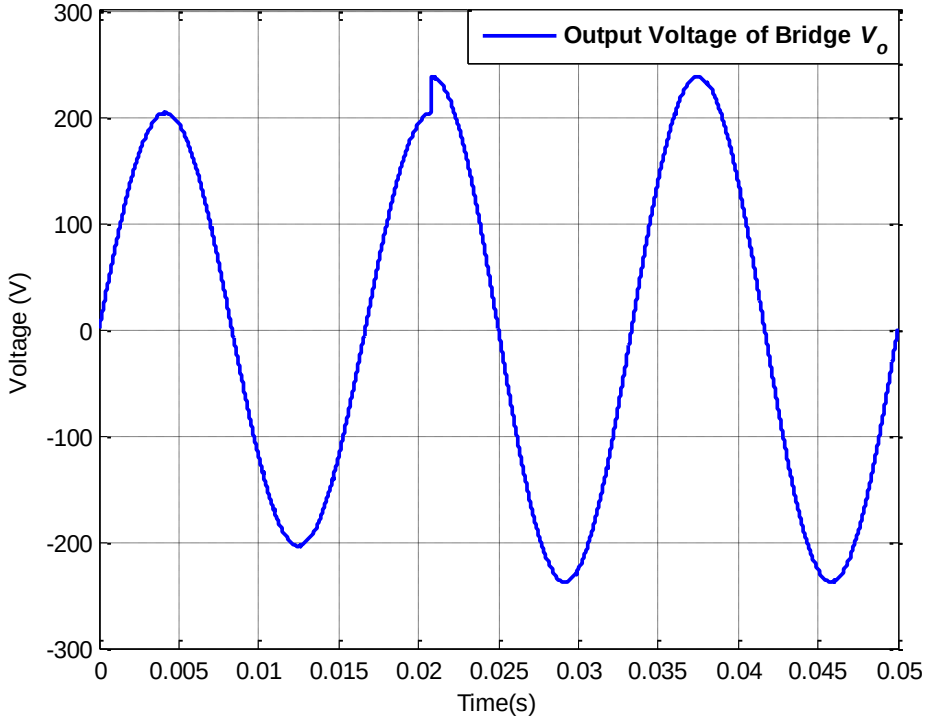


Figure 6.75: Bridge output voltage V_o for operating scenario XVI

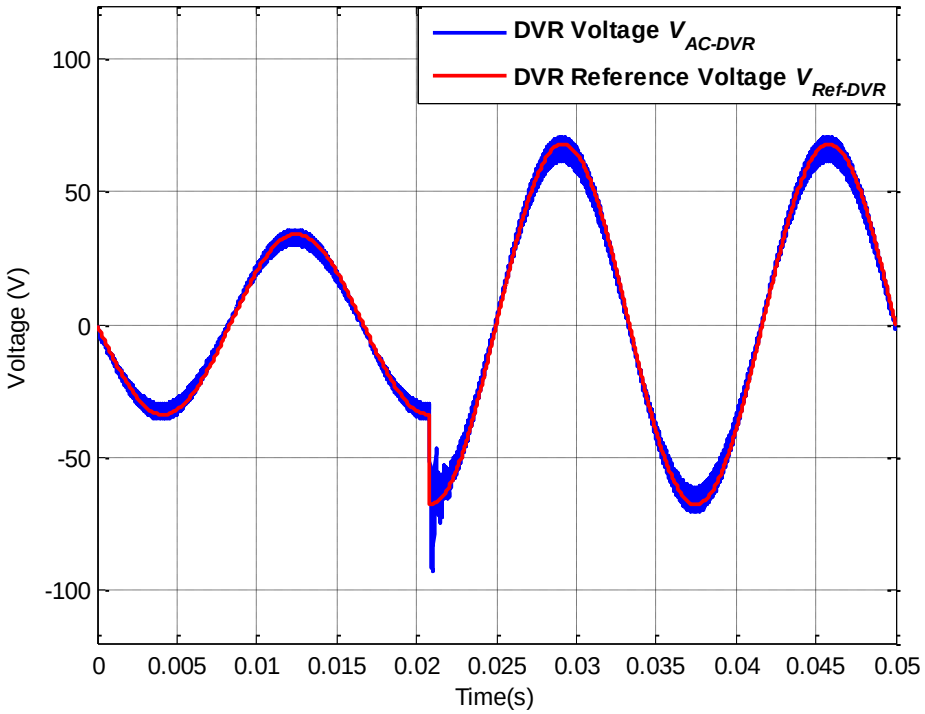


Figure 6.76: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario XVI

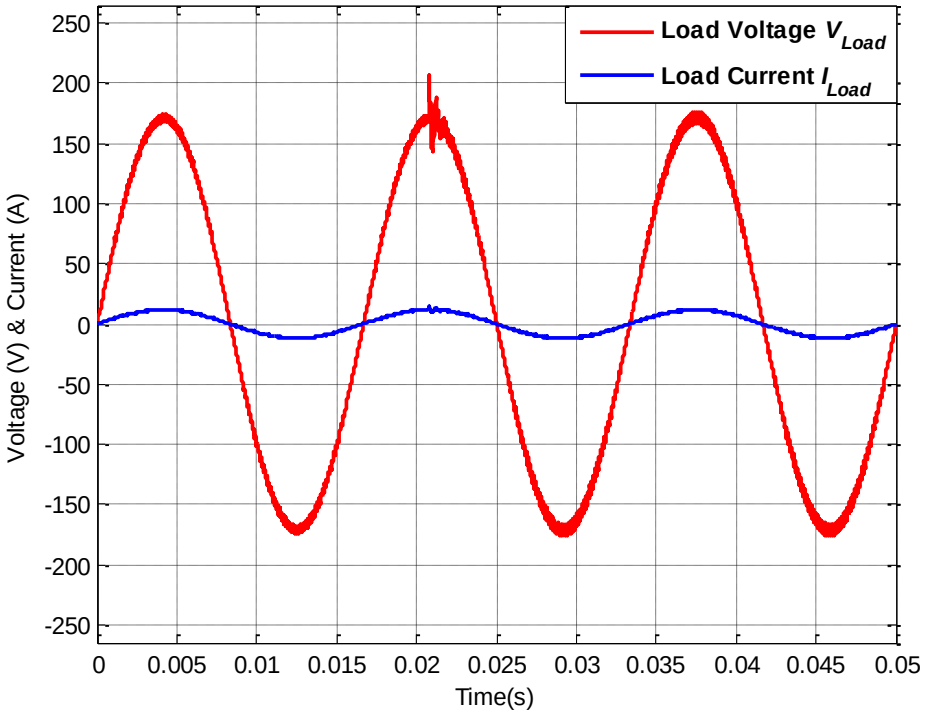


Figure 6.77: Load voltage V_{Load} and load current I_{Load} for operating scenario XVI

6.3.14 Step change in harmonic distortion: Operating scenario XVII

Simulations with step change in voltage swell are presented and discussed in 6.7.13. Likewise, in this scenario, source voltage comprises of 3rd harmonic voltage of 20% for time period $0 \leq t \leq 0.0208$ and 5th harmonic voltage of 30% for $0.0208 \leq t \leq 0.05$ as shown in Figure 6.78. The source voltage is compared with 120V RMS sinusoid signal and AC-AC buck boost converter is switched accordingly to synthesize injection voltage of desired shape and magnitude. The bidirectional bridge provides portions of source voltage in both negative and positive polarity according to the need of AC-AC buck boost converter. Simulation results for bidirectional bridge output and AC-DVR output voltage are depicted in Figure 6.79 and 6.80 respectively. This voltage is injected in series with source voltage and source is restored to 119.9V RMS with 1.21% THD for $0 \leq t \leq 0.0208$ and 119.9V RMS with 2.32% THD for $0.0208 \leq t \leq 0.05$ as shown in Figure 6.81.

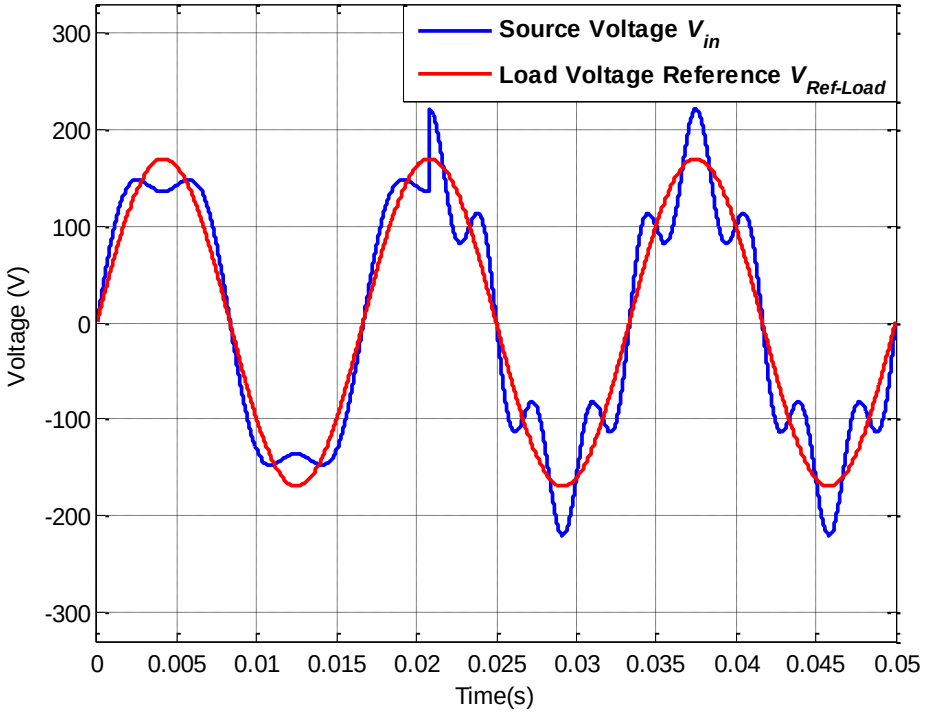


Figure 6.78: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario XVII

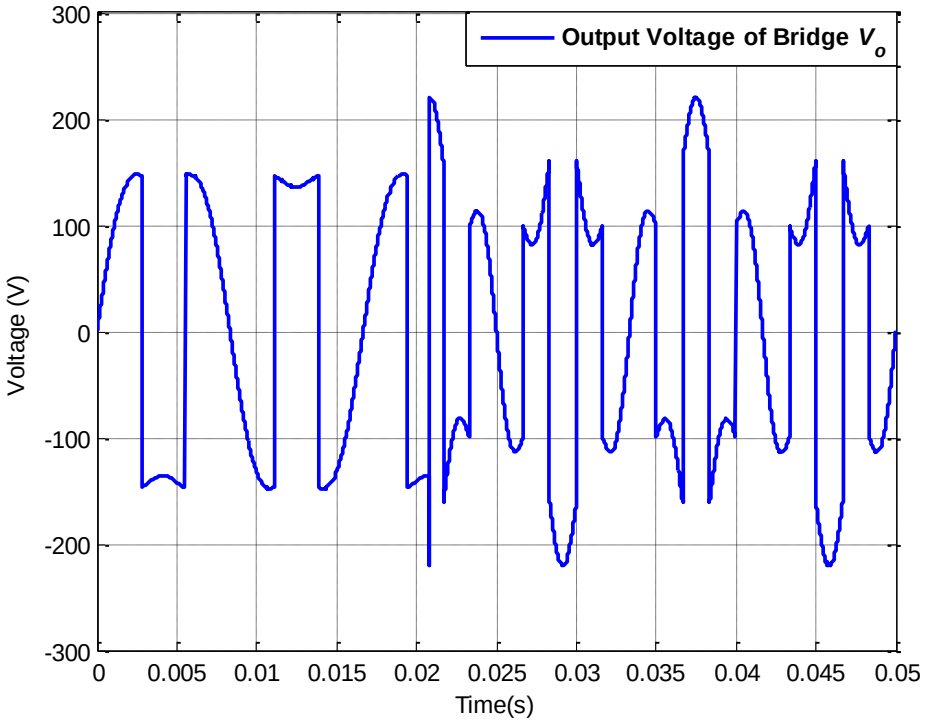


Figure 6.79: Bridge output voltage V_o for operating scenario XVII

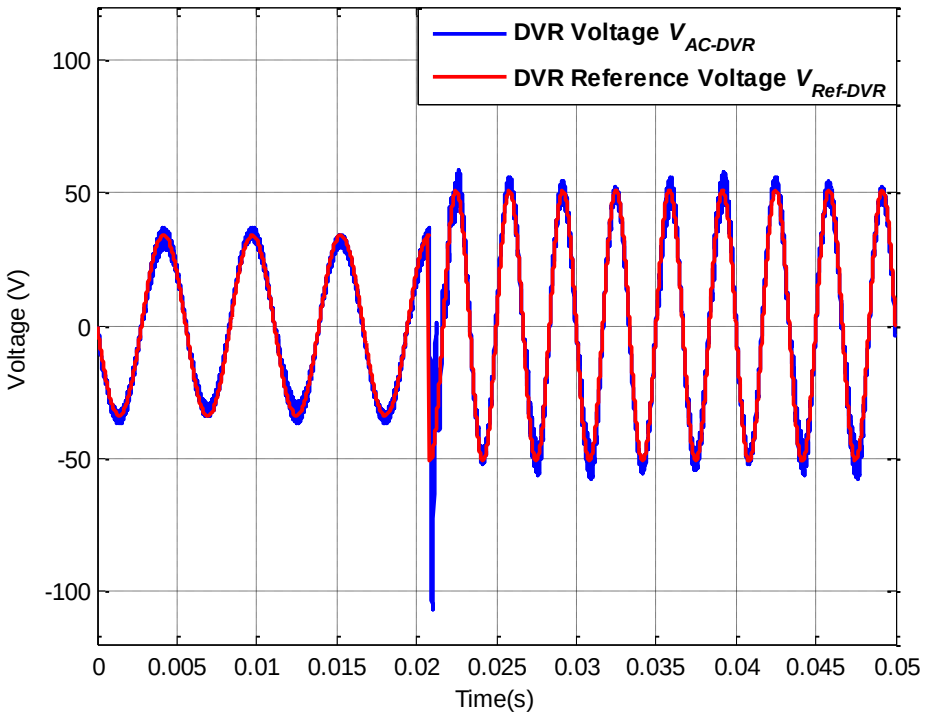


Figure 6.80: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario XVII

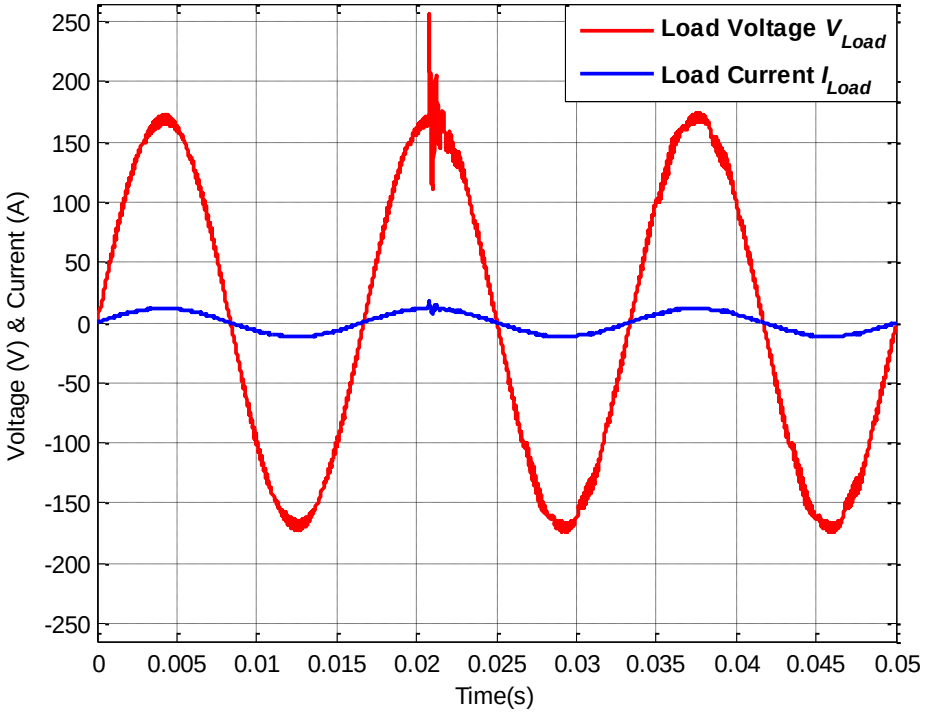


Figure 6.81: Load voltage V_{Load} and load current I_{Load} for operating scenario XVII

CHAPTER 7: EXPERIMENTAL RESULTS

7.1 Introduction

The behavior of proposed AC-DVR is evaluated under various voltage disturbances and simulation results verifying the efficacy of proposed methodology are discussed and presented in previous chapter. A laboratory prototype of proposed topology has been constructed to evaluate the performance of AC-DVR on real time basis. Experimental results verifying the practical realization of the AC-DCR under similar disturbances discussed in previous chapter are presented and discussed in brief in this chapter.

7.2 Experiment Parameters

A hardware prototype of proposed methodology has been built with the parameters tabulated in Table 7.1. Experiments have been performed under similar disturbance scenarios discussed in previous chapter by changing some of the parameters of Table 7.1. The results obtained are discussed in next sections.

Table 7.1 Experiment parameters

Model	Parameters
Source/Grid	120 V (RMS), 60 Hz
Load	24 Ω and 16 Ω (0.6kW and 0.9 kW)
Series transformer	1 kVA, 400 Hz Isolation Transformer
Inductor L	250 µH
Capacitor C	15 µF
AC-AC Buck Boost switching frequency f_{sw}	20 kHz
Control platform	OPAL-RT (RT-LAB)

7.3 Experimental Results

A hardware prototype has been built with parameters provided in Table 7.1 as presented in Figure 7.1. IGBTs are used to construct bidirectional bridge and AC-AC buck boost converter. A programmable power supply (Agilent 6813B) is used to emulate 120V, 60 Hz grid. A 400 Hz isolation transformer is utilized for series voltage injection. The overall control discussed in chapter 4 is implemented using real time simulator OPAL-RT. The THD and RMS of input voltage and out voltage is observed via harmonic analyzer (PPA 1530). The overall system architecture including AC source, AC-DVR, load and OPAL-RT is depicted in Figure 7.2. The model of control architecture in OPAL-RT is presented in Figure 7.3.

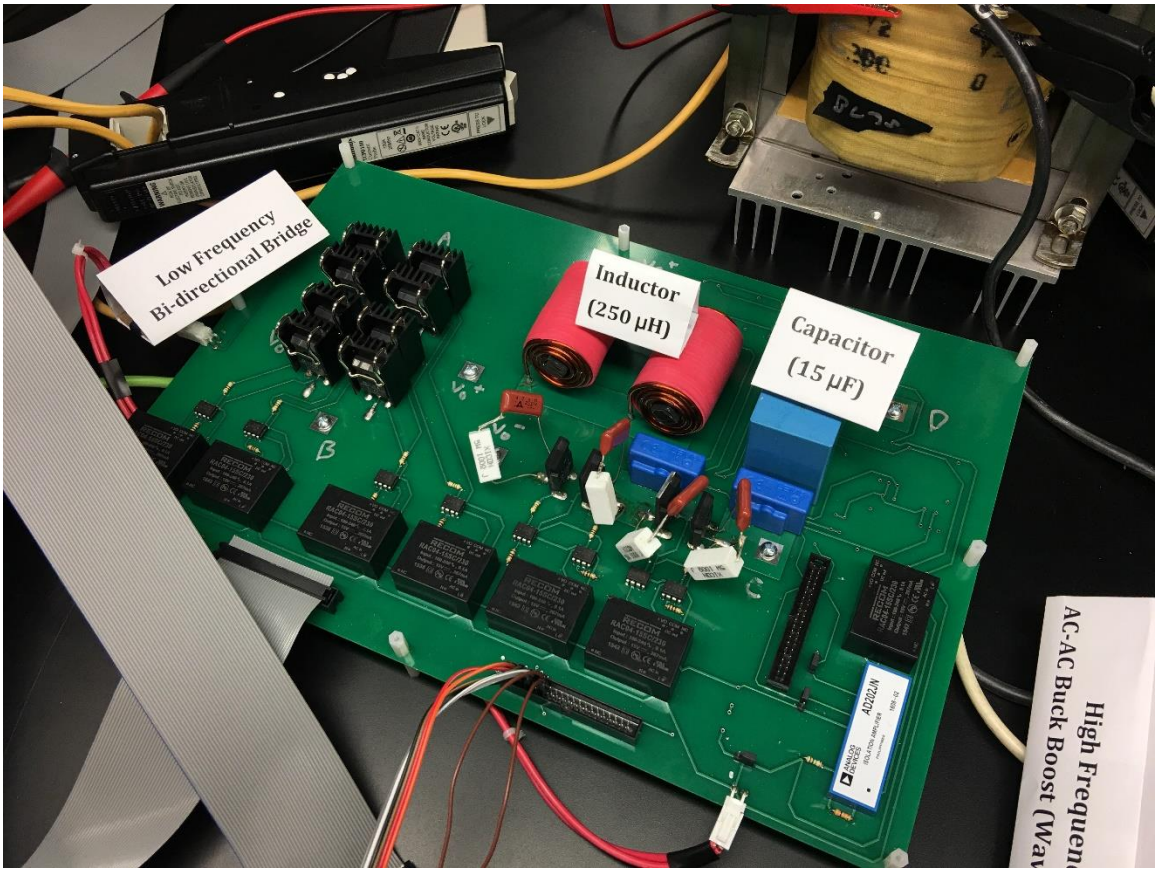


Figure 7.1: Experimental setup of AC-DVR

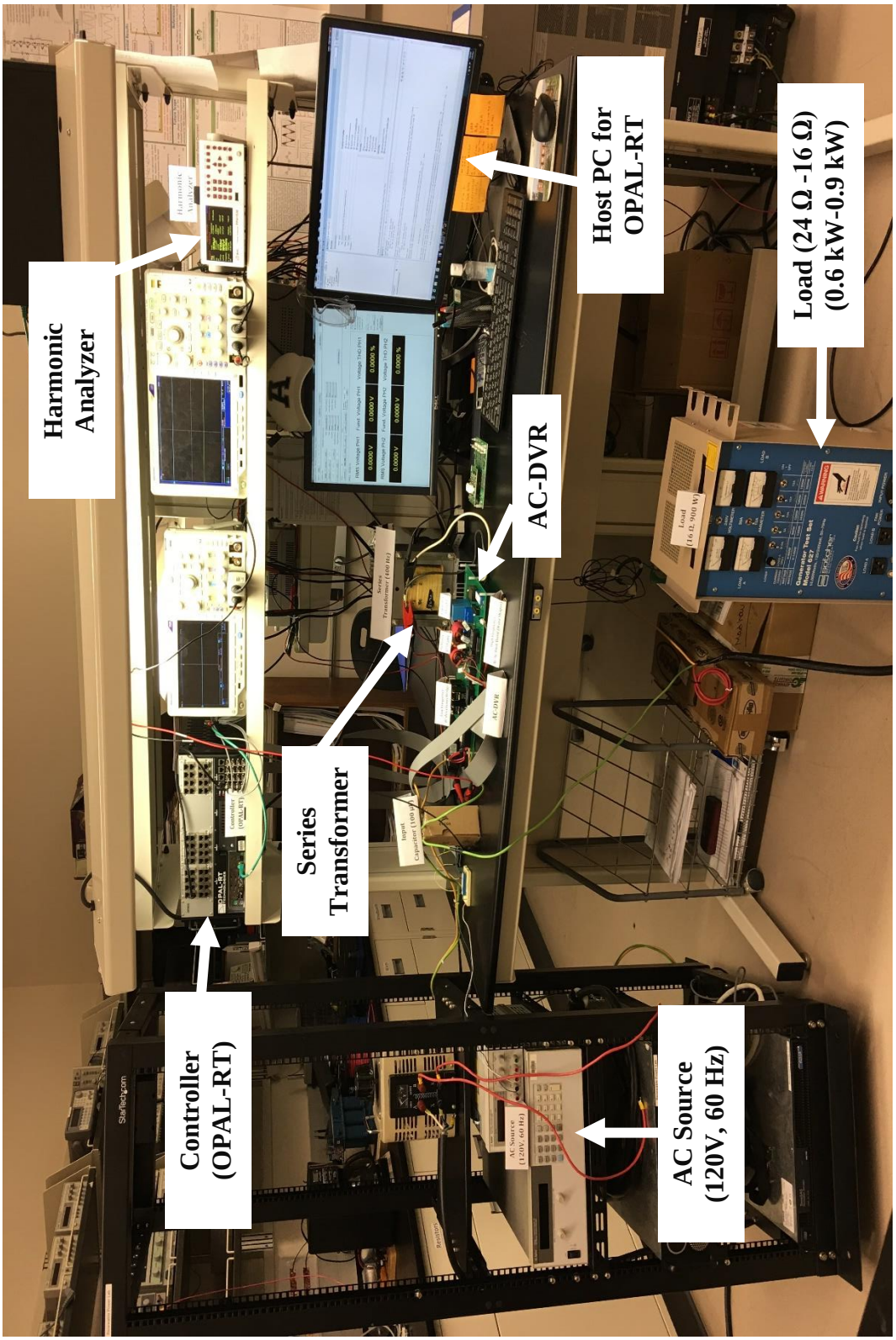


Figure 7.2: Experimental setup of overall system

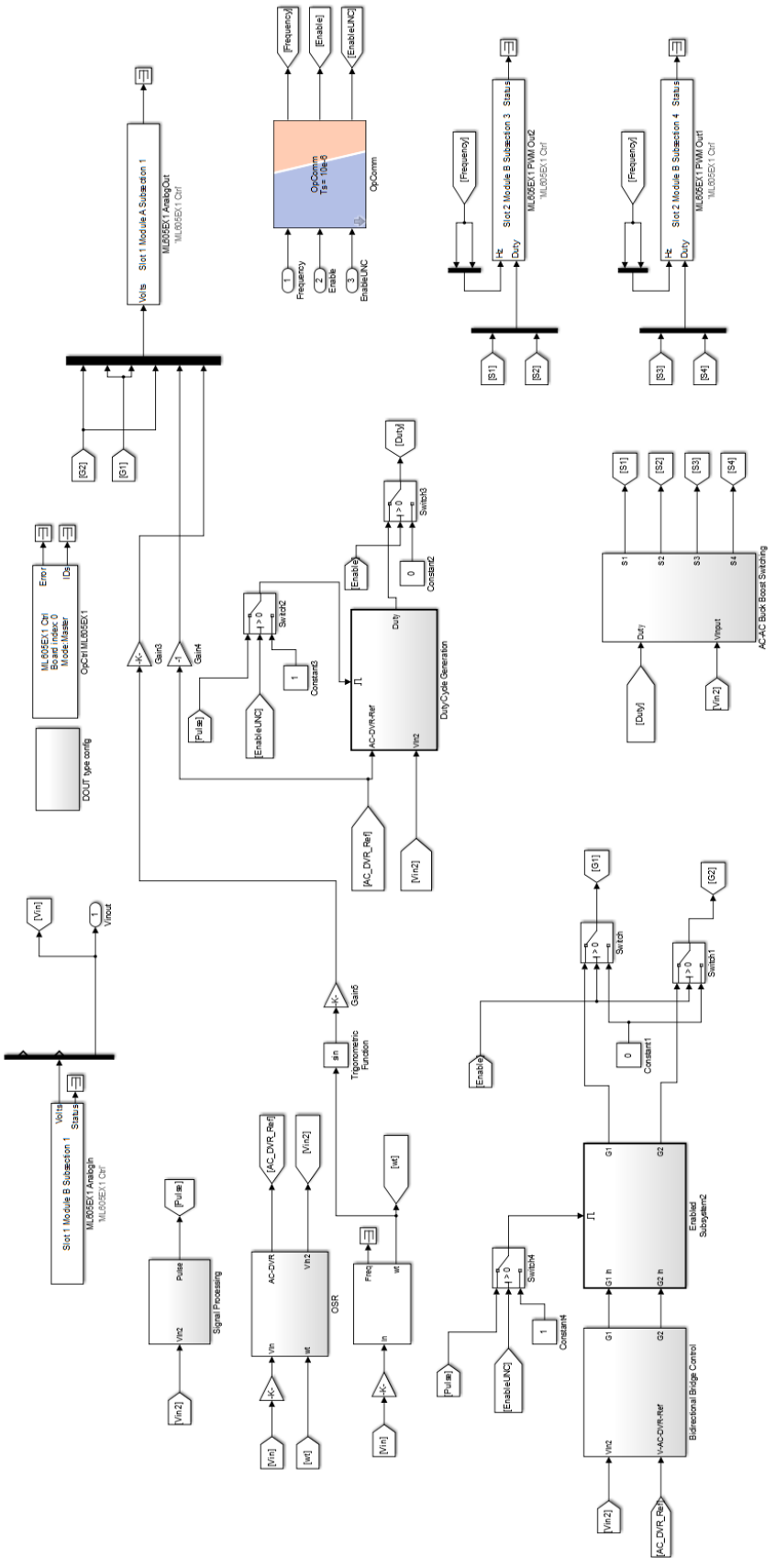


Figure 7.3: Control architecture in OPAL-RT

7.3.1 Nominal grid condition: Experiment scenario I

The first experiment was performed under similar parameters discussed in section 6.3.1. The source voltage and load voltage reference are presented in Figure 7.4. Source -

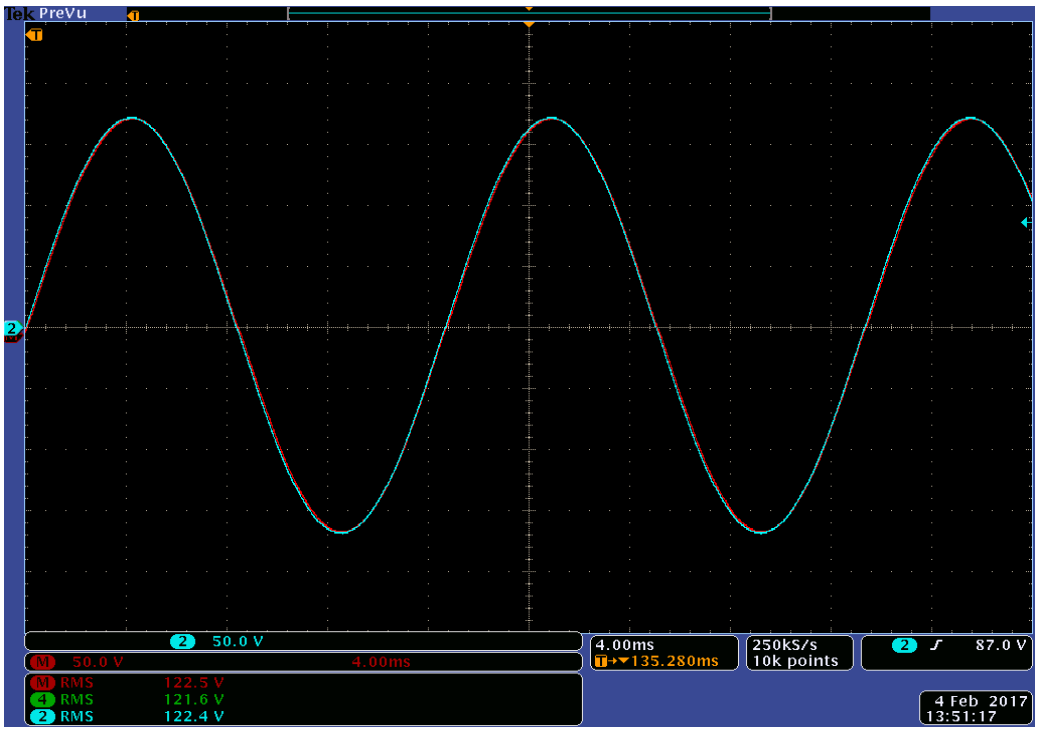


Figure 7.4: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario I

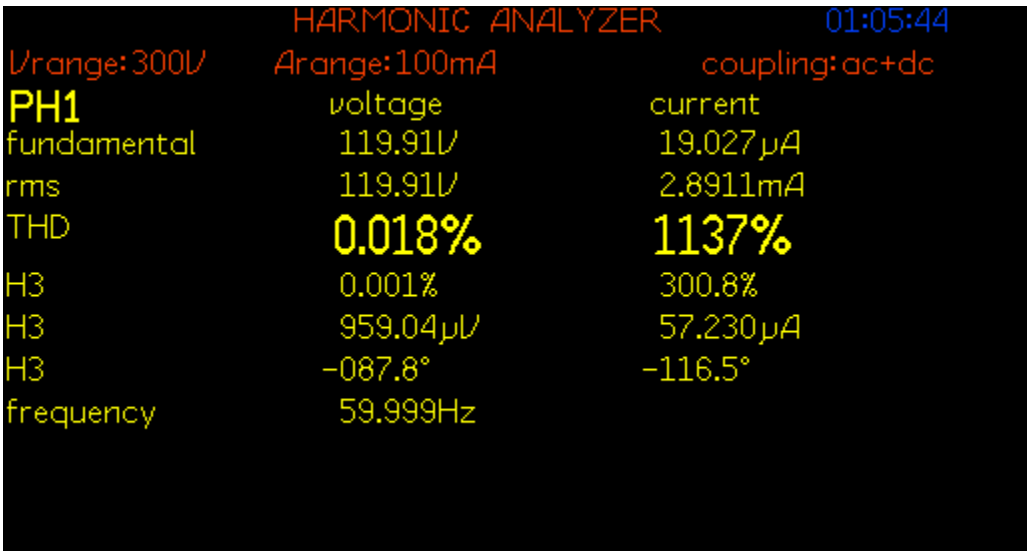


Figure 7.5: THD of source voltage V_{in} for experiment scenario I

voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.5, 7.6, 7.7, 7.8,7.9, 7.10 and 7.11 respectively.

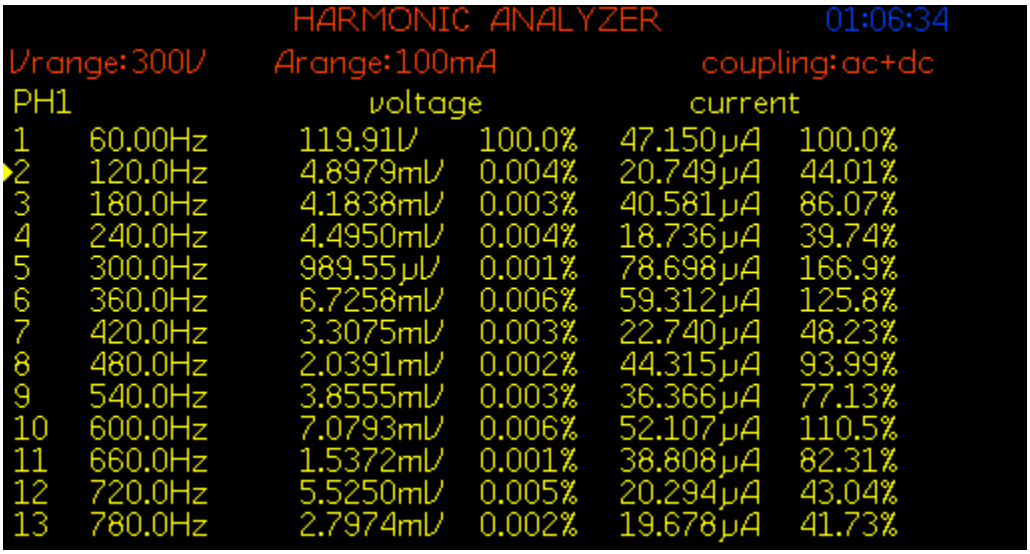


Figure 7.6: FFT of source voltage V_{in} for experiment scenario I

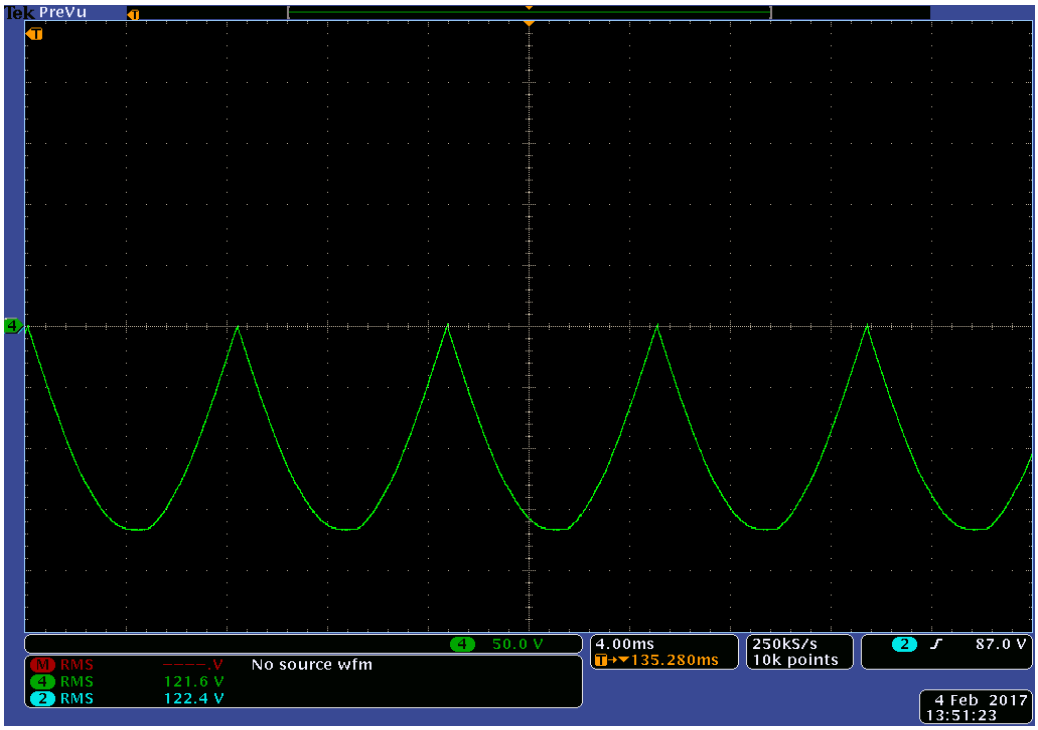


Figure 7.7: Experimental results of Bridge output voltage V_o for experiment scenario I

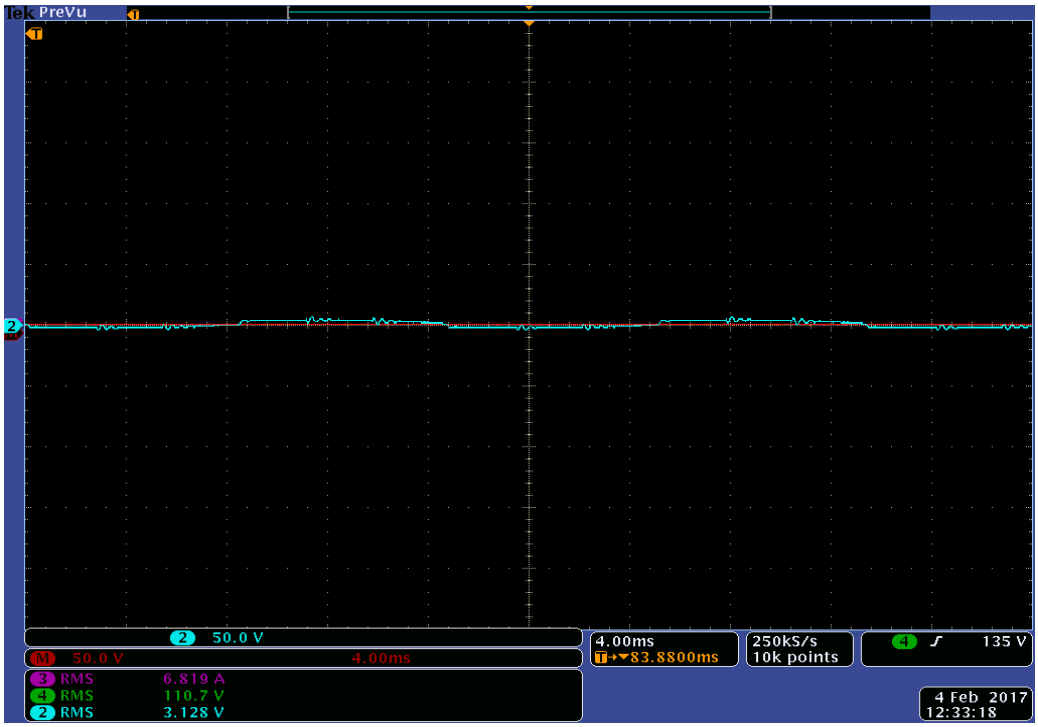


Figure 7.8: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario I

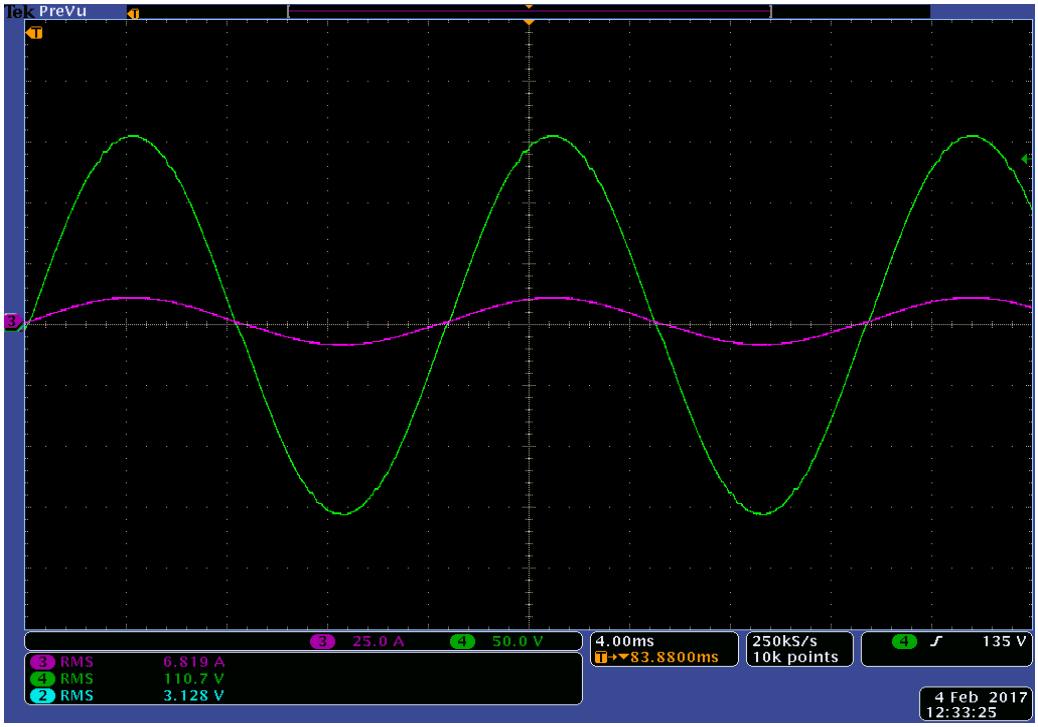


Figure 7.9: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario I

The load voltage is measured to be 109 V RMS with 0.744% THD. The magnitude of load voltage is not exactly equal to the input because of the losses occurring in the system. Although, as it can be seen that experimental results closely resemble with simulation results presented in section 6.3.1. The AC-DVR operates in similar way as discussed in section 6.3.1 in chapter 6.

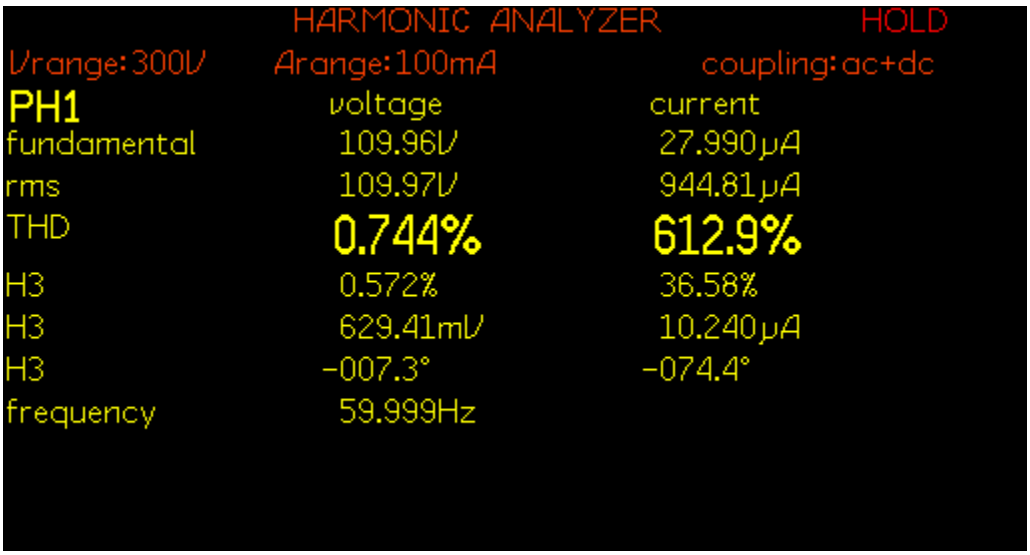


Figure 7.10: THD of load voltage V_{Load} for experiment scenario I

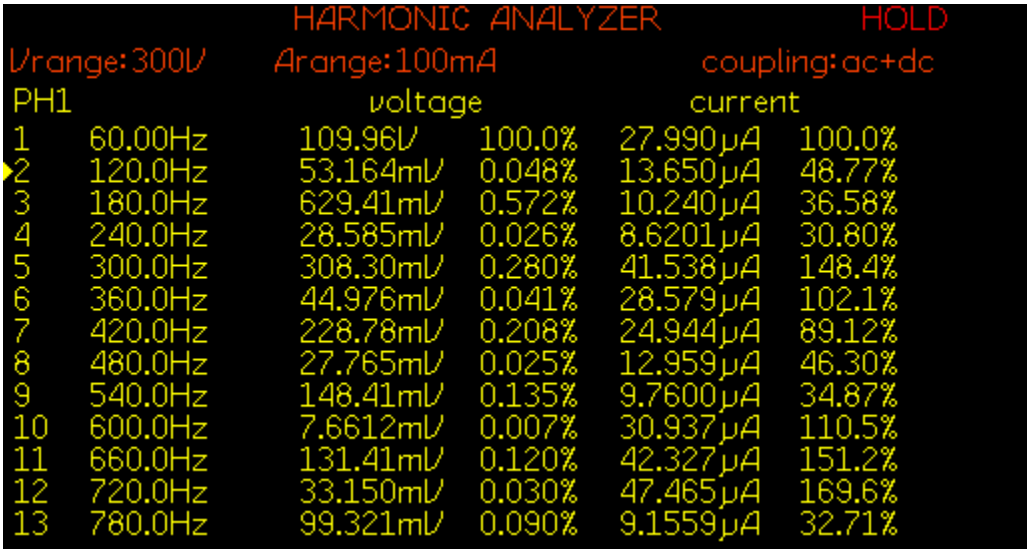


Figure 7.11: FFT of load voltage V_{Load} for experiment scenario I

7.3.2 3rd Harmonic distortion: Experiment scenario II

The second experiment was performed under similar parameters discussed in section 6.3.2. The source voltage and load voltage reference are presented in Figure 7.12.

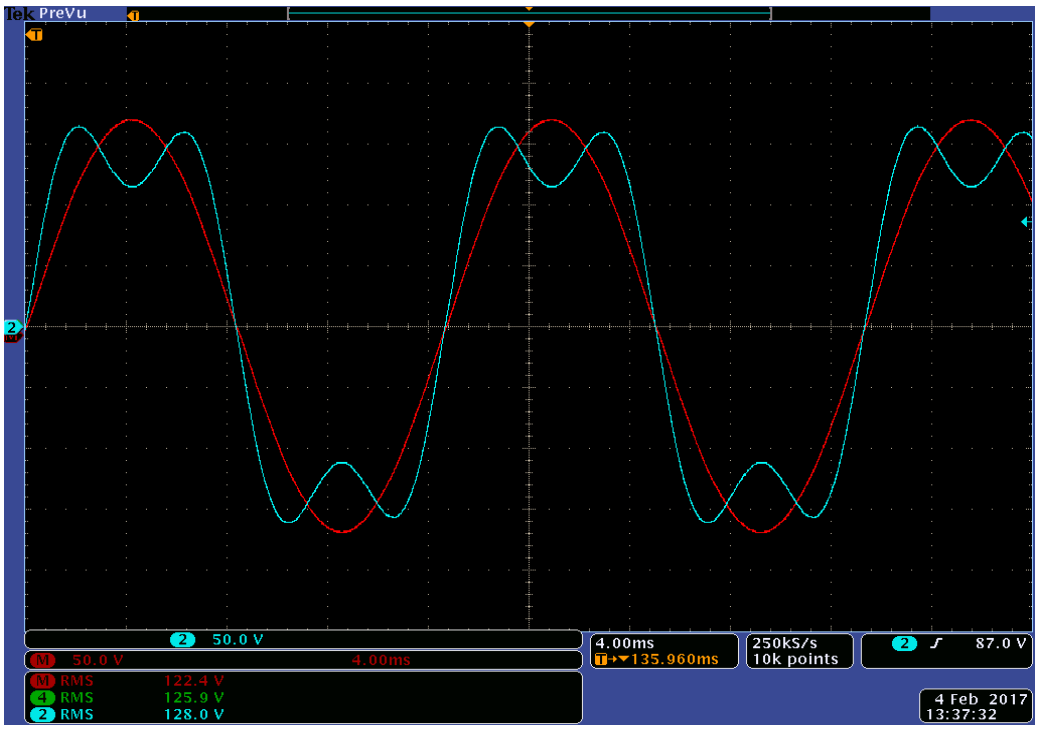


Figure 7.12: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario II

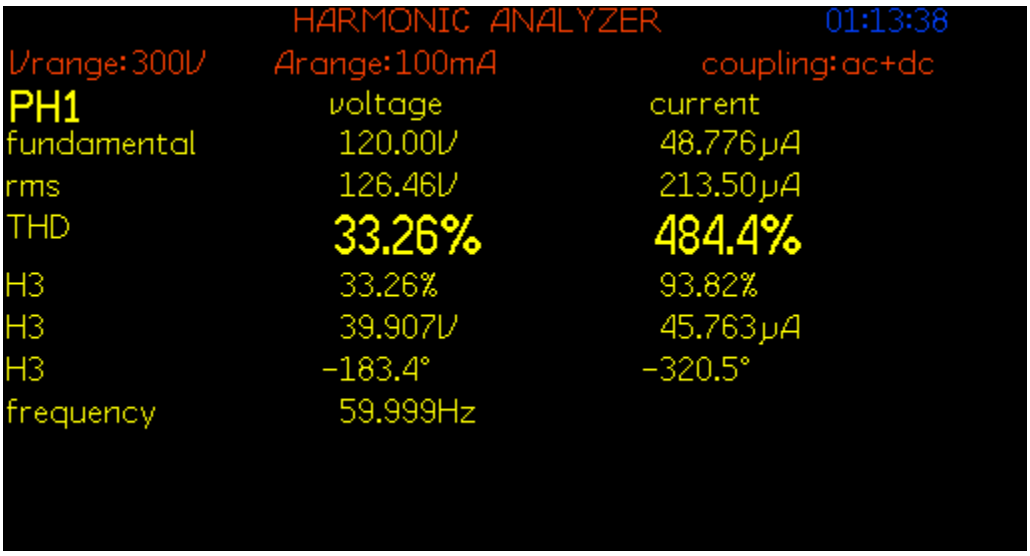


Figure 7.13: THD of source voltage V_{in} for experiment scenario II

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.13, 7.14, 7.15, 7.16,7.17, 7.18 and 7.19 respectively.

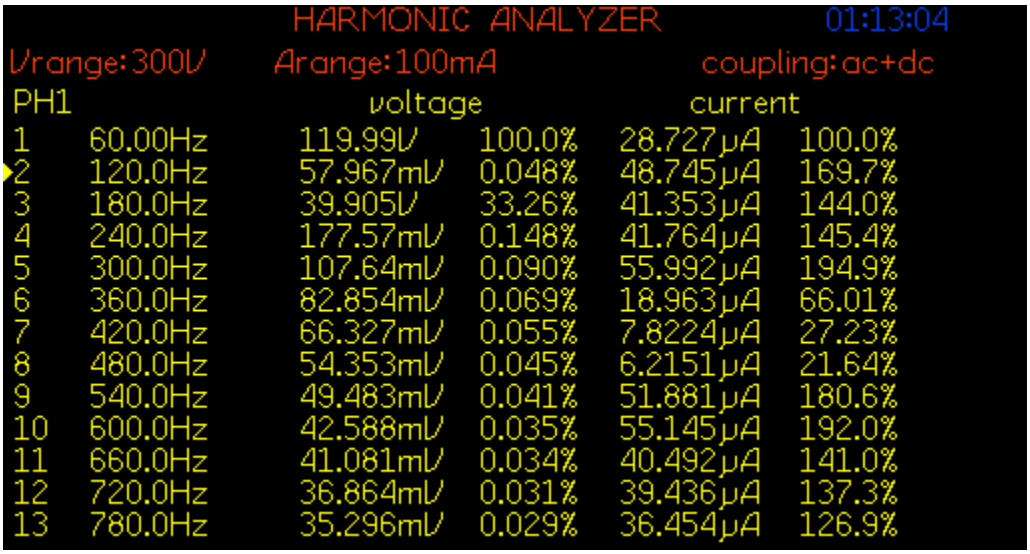


Figure 7.14: FFT of source voltage V_{in} for experiment scenario II

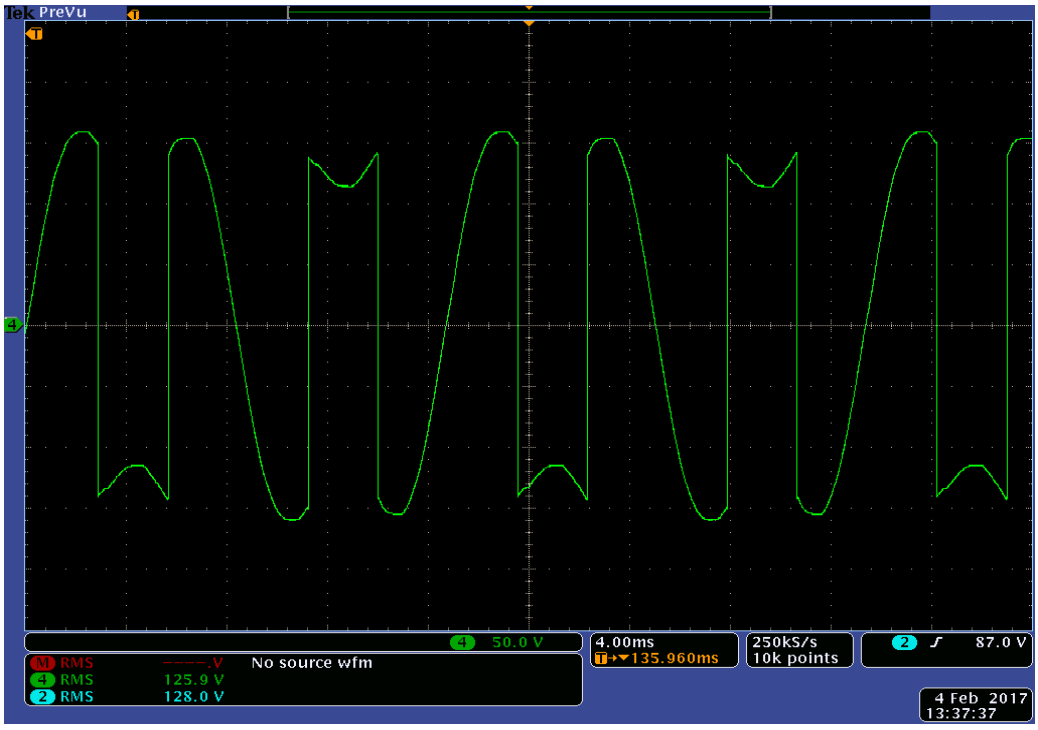


Figure 7.15: Experimental results of Bridge output voltage V_o for experiment scenario II

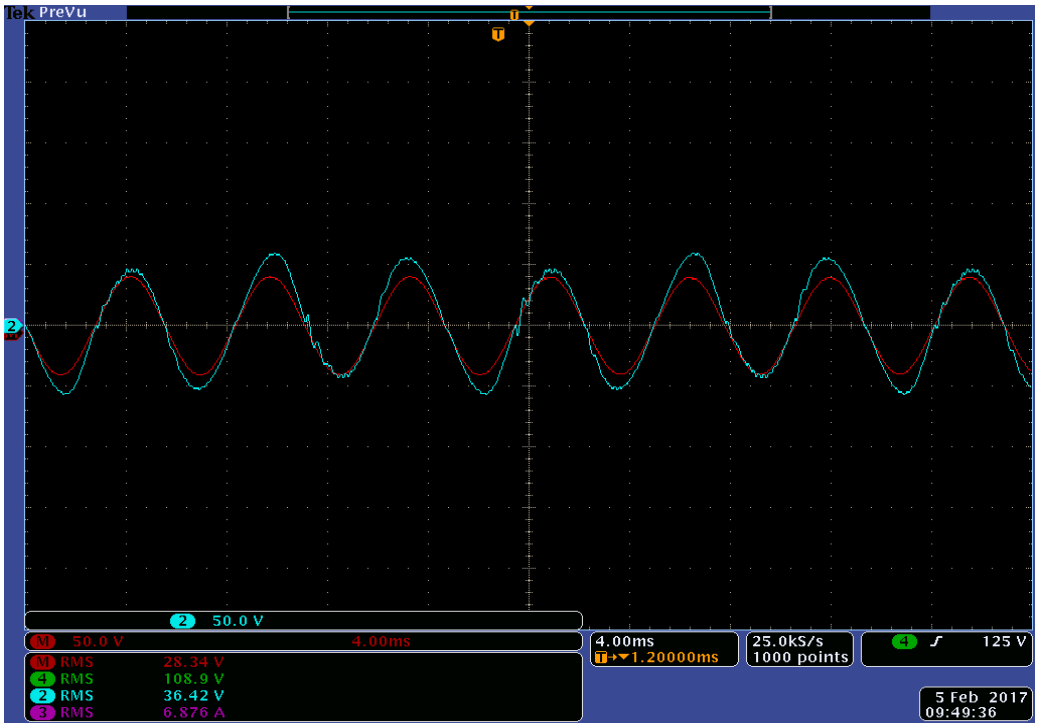


Figure 7.16: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario II

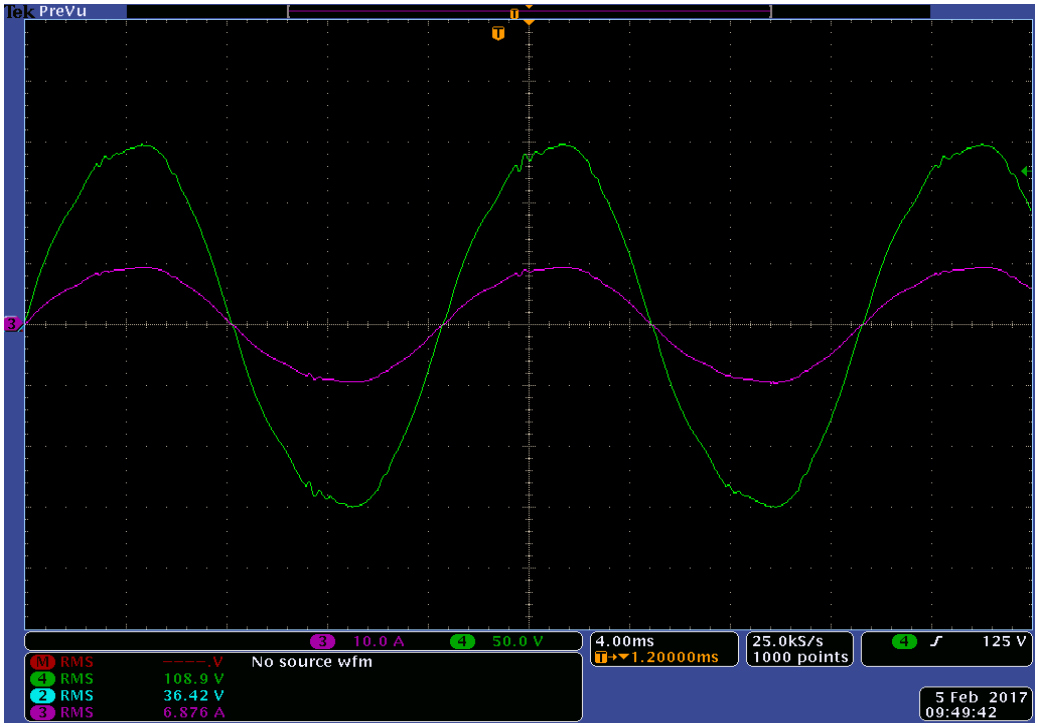


Figure 7.17: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario II

The load voltage is restored to 109 V RMS with 2.5% THD from source voltage of 126.5 V RMS with 33.26% THD. The source current, AC-DVR input current, inductor current and capacitor current are presented in Figures 7.20-7.23 respectively. It can be noted that AC-DVR operates in similar manner discussed in section 6.3.2 and experimental results presented in this section closely resemble to the simulation results presented in section 6.3.2 for same operating scenario of 3rd harmonic distortion.

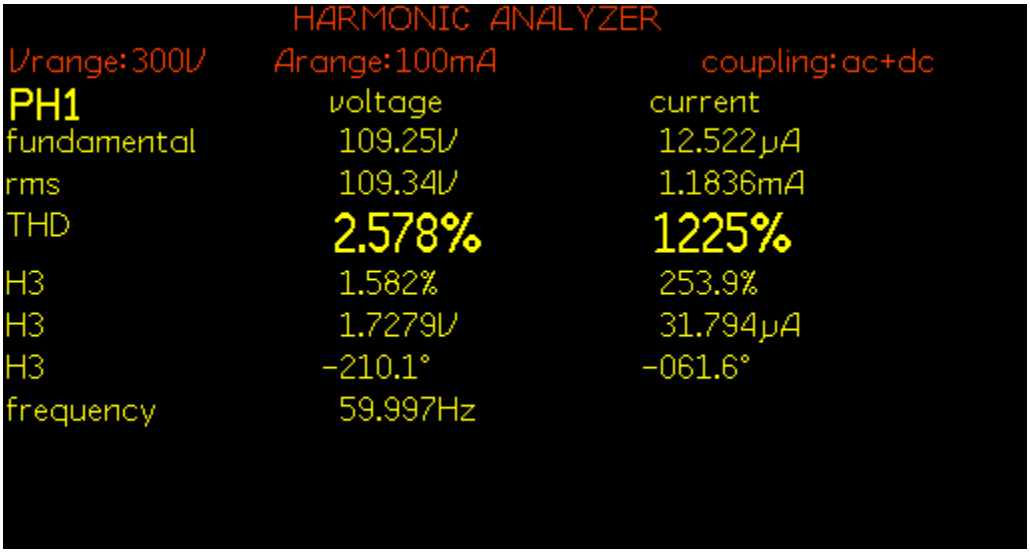


Figure 7.18: THD of load voltage V_{Load} for experiment scenario II

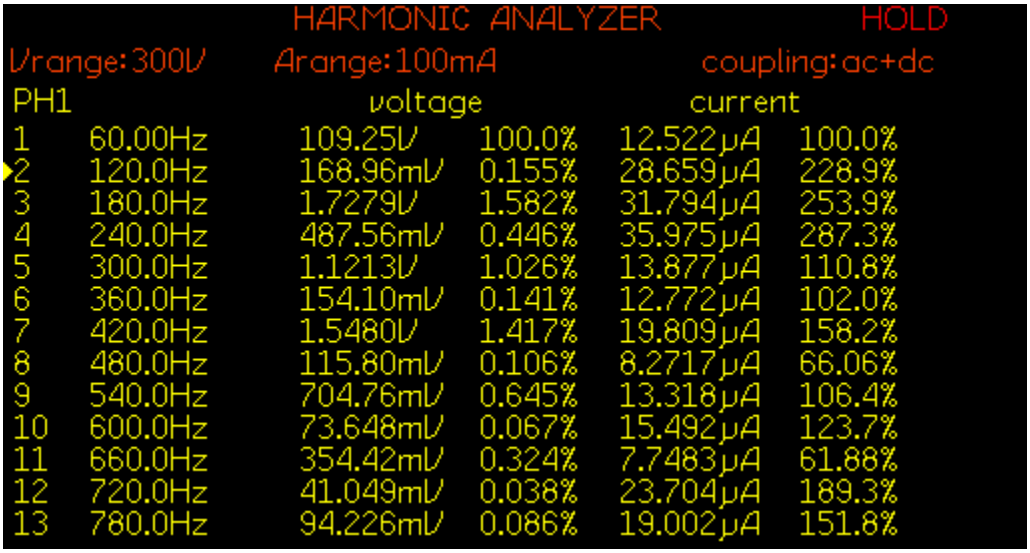


Figure 7.19: FFT of load voltage V_{Load} for experiment scenario II

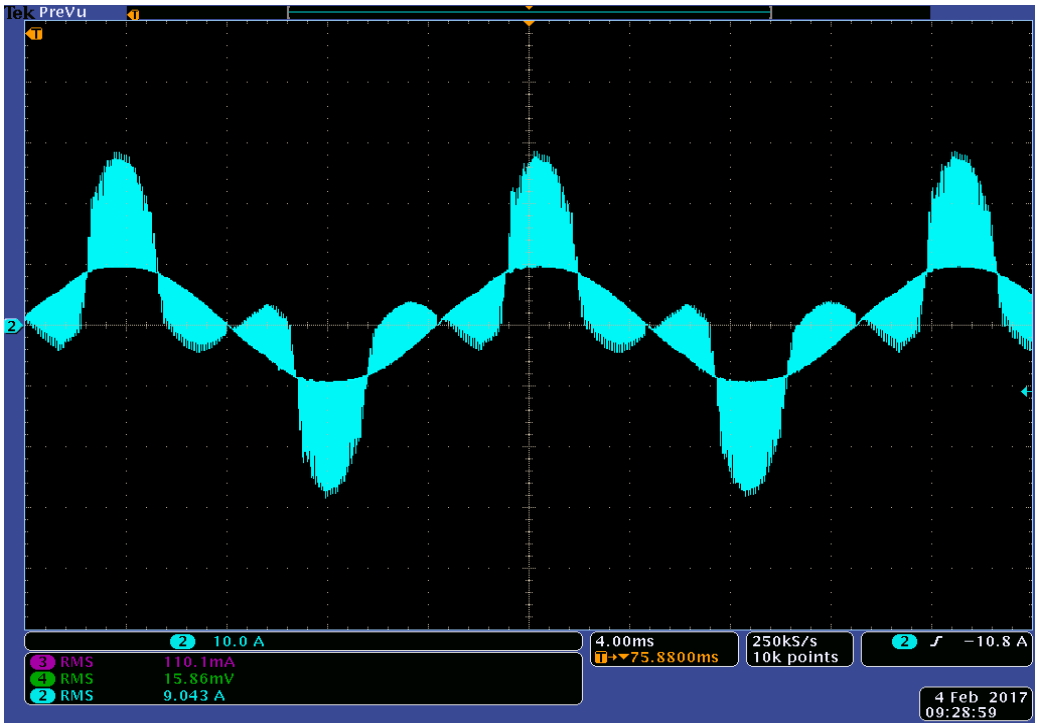


Figure 7.20: Experimental Results of Actual source current I_{in} for experiment scenario II

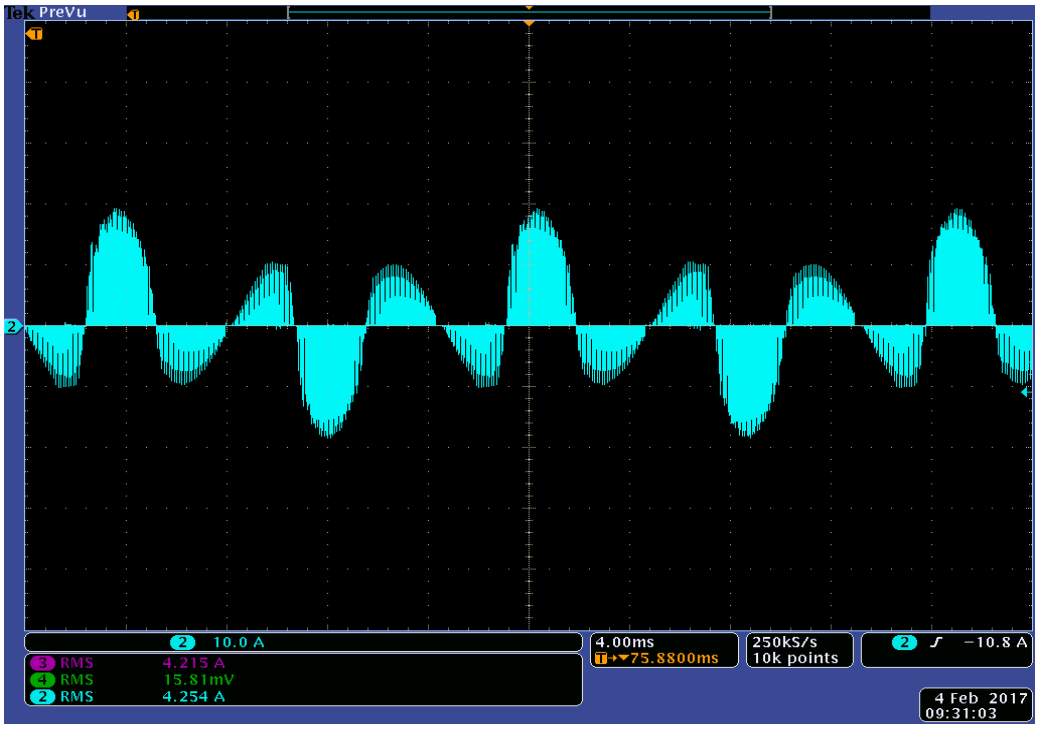


Figure 7.21: Experimental Results of Actual DVR current I_{DVR-IN} for experiment scenario II

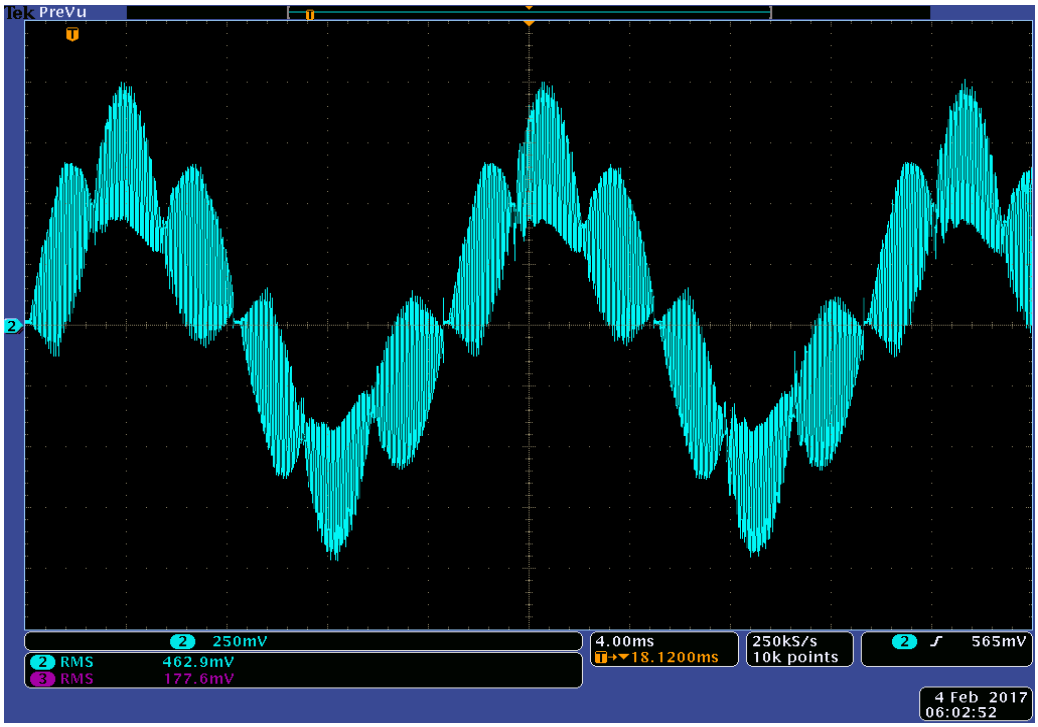


Figure 7.22: Experimental Results of Actual inductor current I_L for experiment scenario II

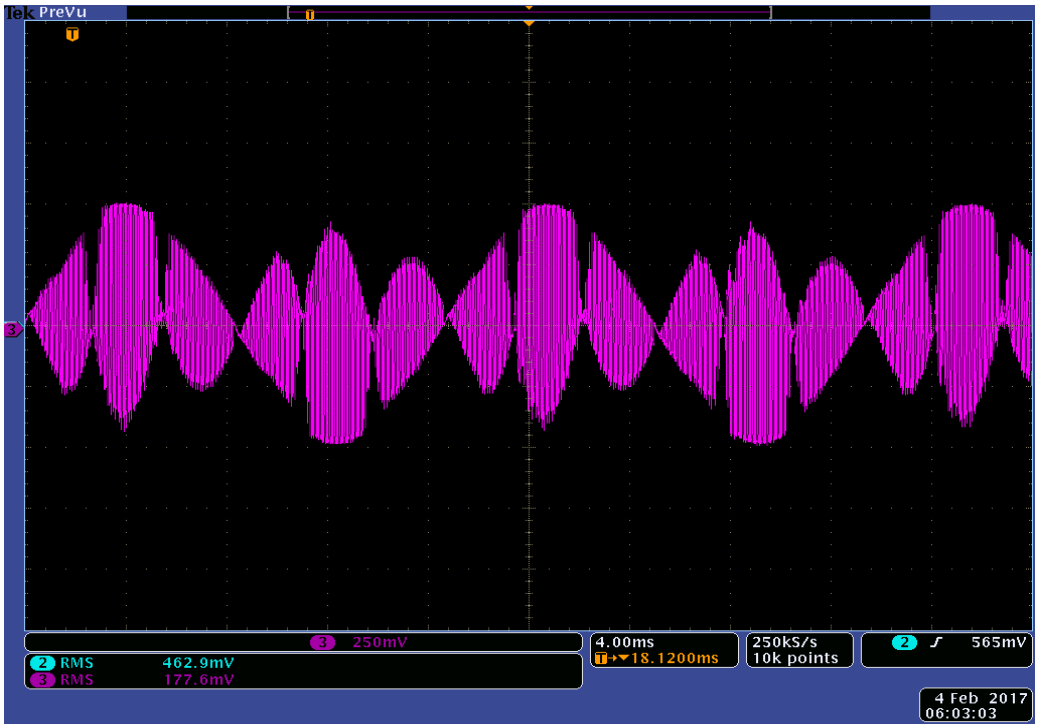


Figure 7.23: Experimental Results of Actual capacitor current I_C for operating scenario II

7.3.3 5th Harmonic distortion: Experiment scenario III

The third experiment was performed under similar parameters discussed in section 6.3.3. The source voltage and load voltage reference are presented in Figure 7.24.

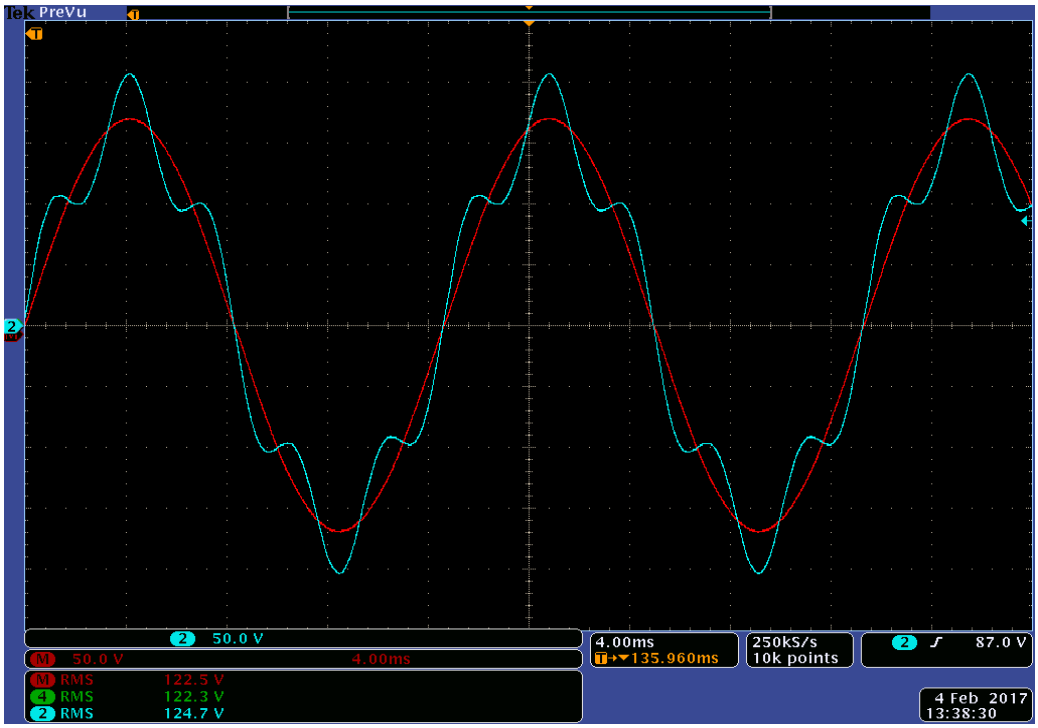


Figure 7.24: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario III

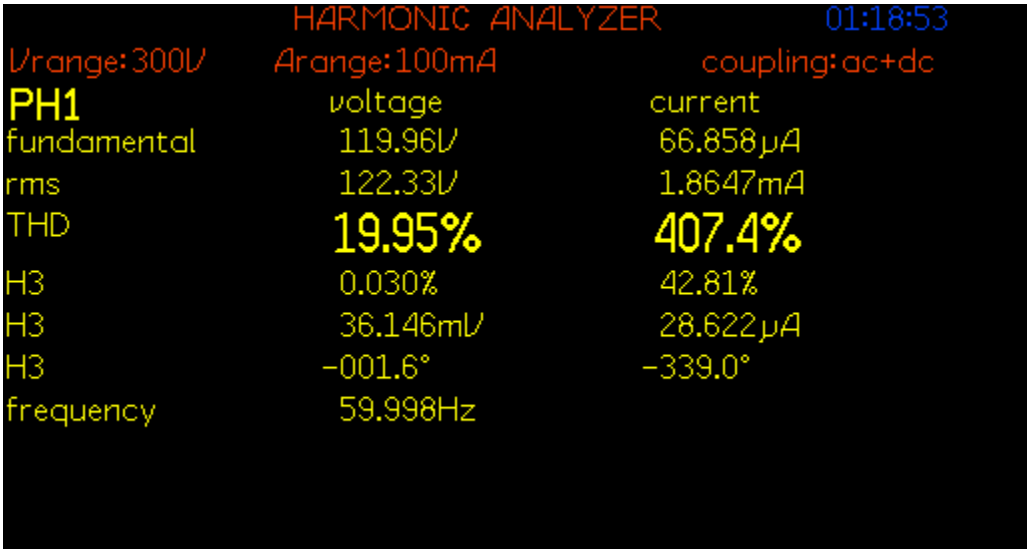


Figure 7.25: THD of source voltage V_{in} for experiment scenario III

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.25, 7.26, 7.27, 7.28,7.29, 7.30 and 7.31 respectively.

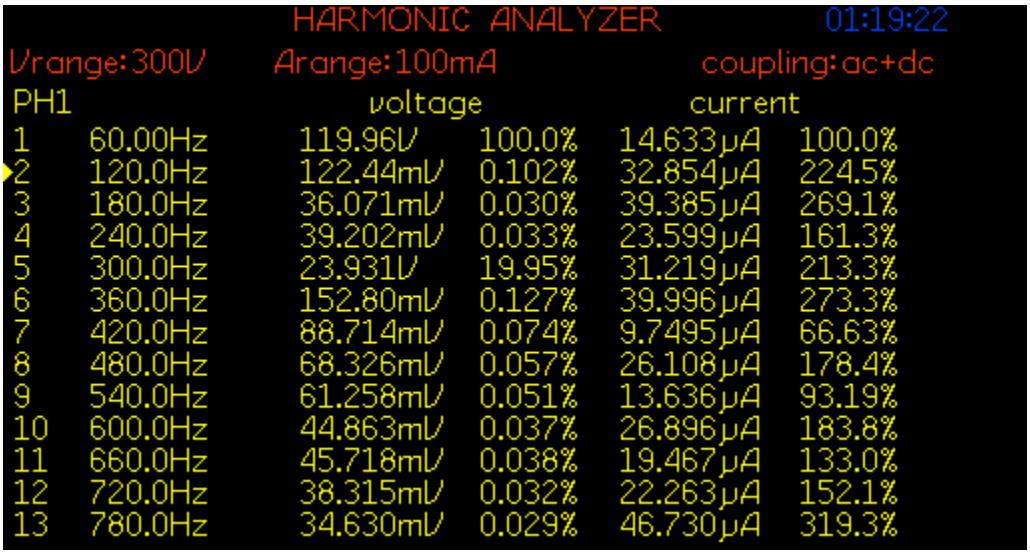


Figure 7.26: FFT of source voltage V_{in} for experiment scenario III

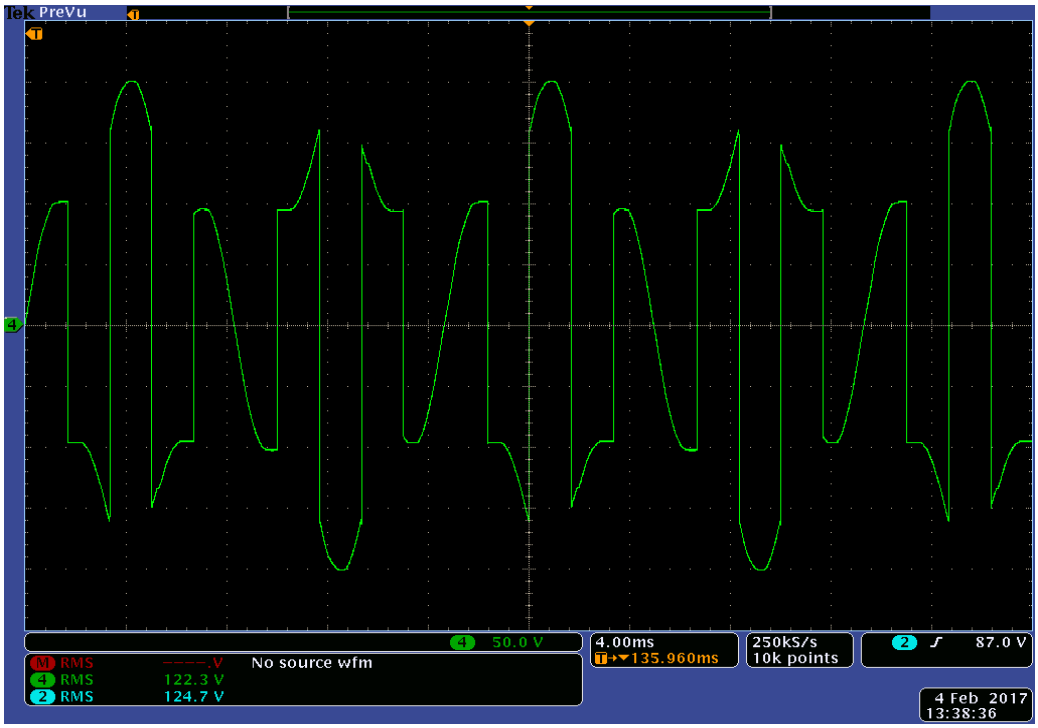


Figure 7.27: Experimental results of Bridge output voltage V_o for experiment scenario III

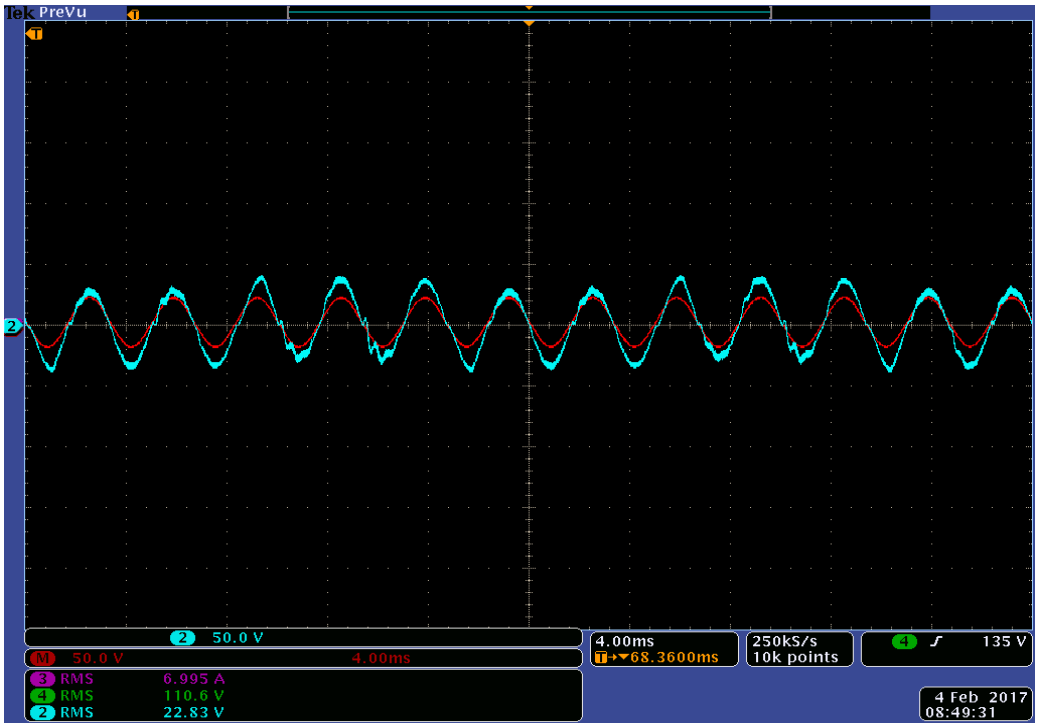


Figure 7.28: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario III

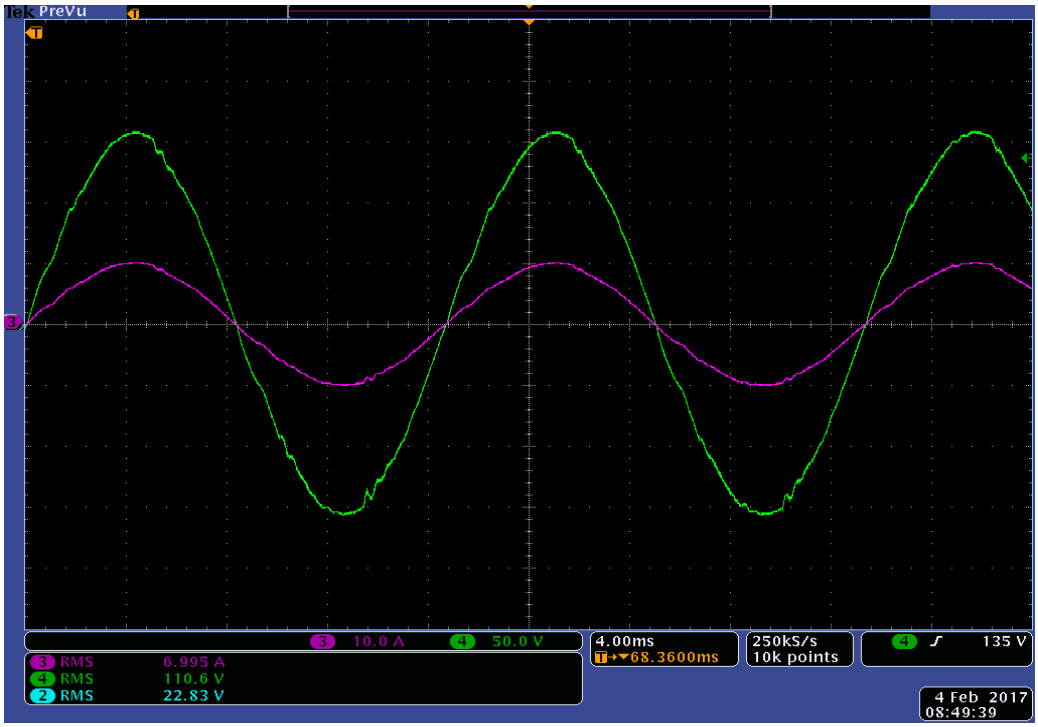


Figure 7.29: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario III

The load voltage is restored to 109 V RMS with 2.36% THD from source voltage of 122.23 V RMS with 19.95% THD. The load voltage is not completely restored to 120 V RMS due to the losses occurring in the system. It can be noted that AC-DVR operates in similar manner discussed in section 6.3.3 and experimental results presented in this section closely resemble to the simulation results presented in section 6.3.3 for same operating scenario of 5th harmonic distortion.

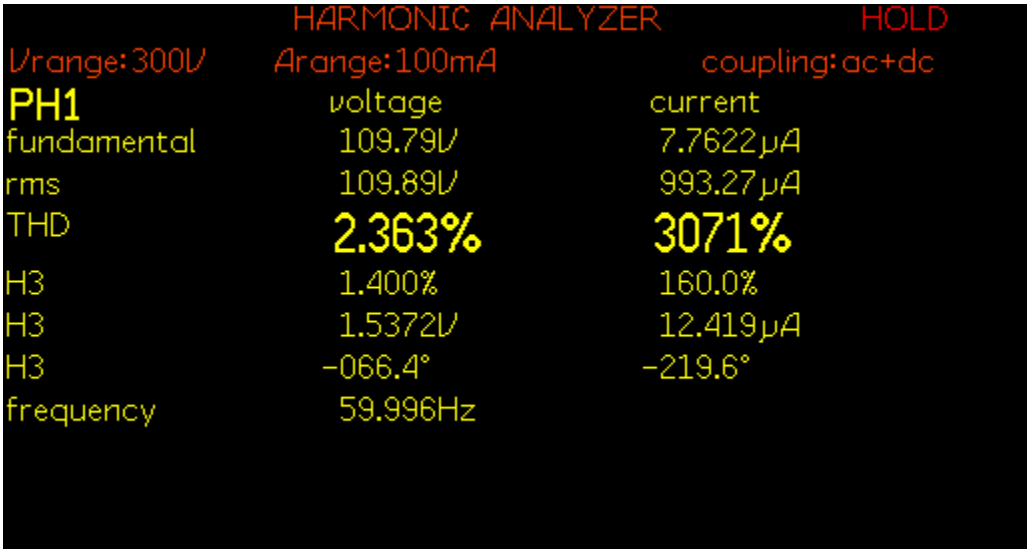


Figure 7.30: THD of load voltage V_{Load} for experiment scenario III

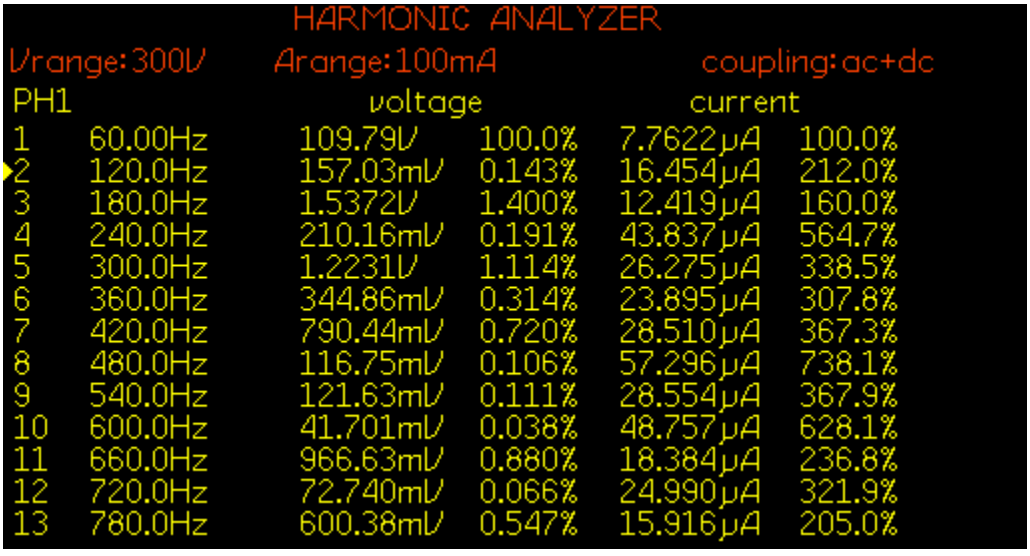


Figure 7.31: FFT of load voltage V_{Load} for experiment scenario III

7.3.4 11th Harmonic distortion: Experiment scenario VI

This experiment was performed under similar parameters discussed in section 6.3.4. Distorted source voltage and load voltage reference are presented in Figure 7.32.

Figure 7.32: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario VI

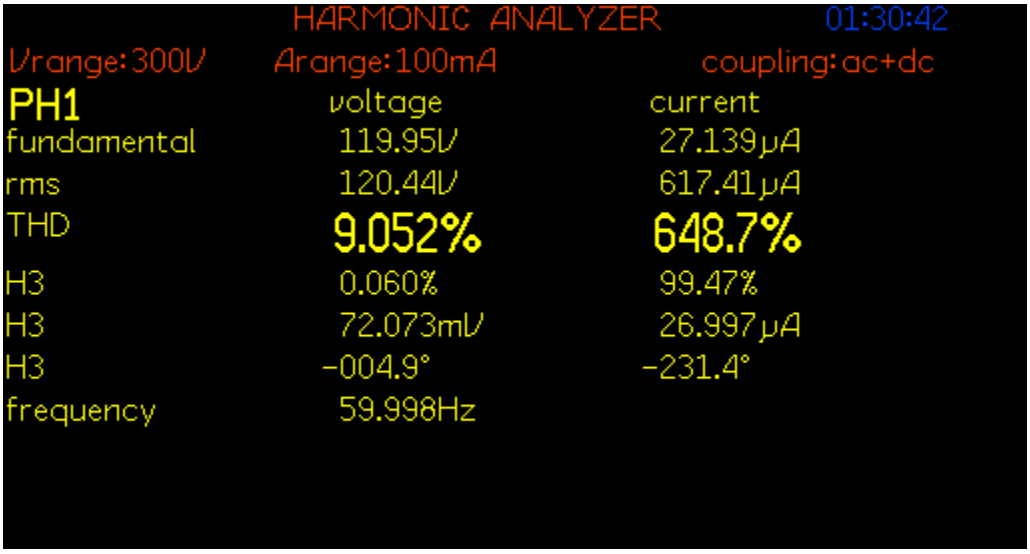


Figure 7.33: THD of source voltage V_{in} for experiment scenario IV

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.33, 7.34, 7.35, 7.36,7.37, 7.38 and 7.39 respectively.

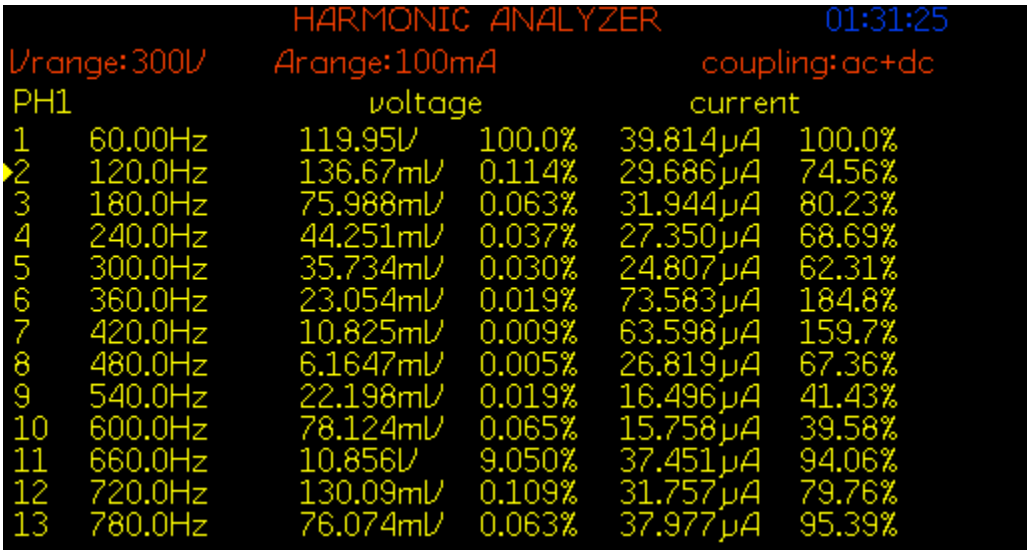


Figure 7.34: FFT of source voltage V_{in} for experiment scenario IV

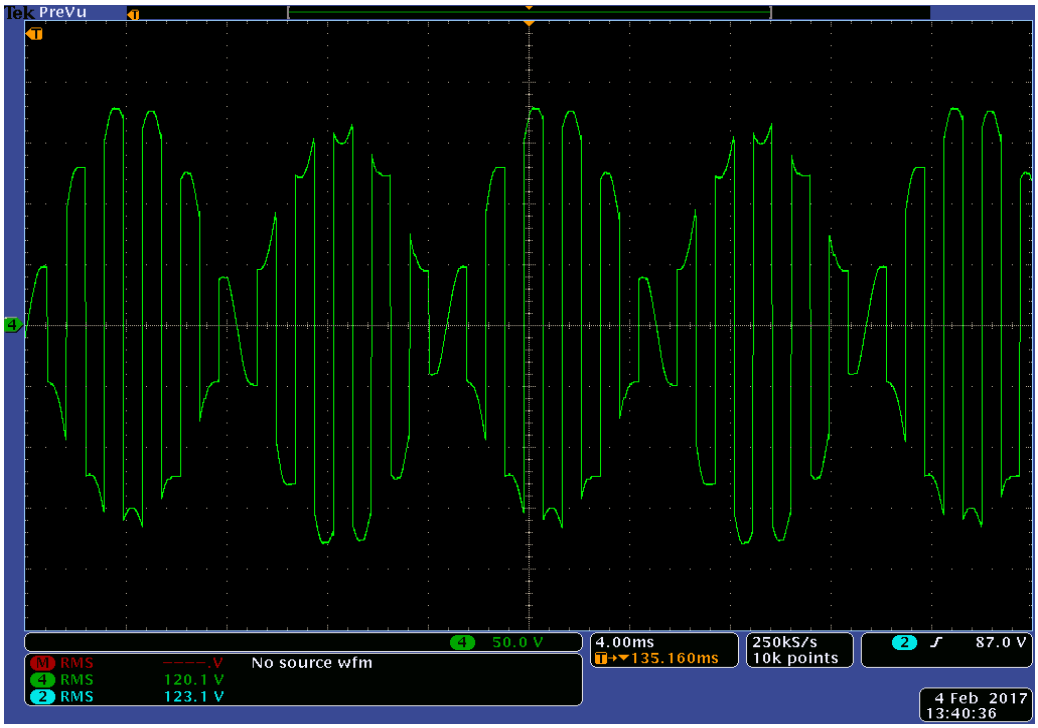


Figure 7.35: Experimental results of Bridge output voltage V_o for experiment scenario IV

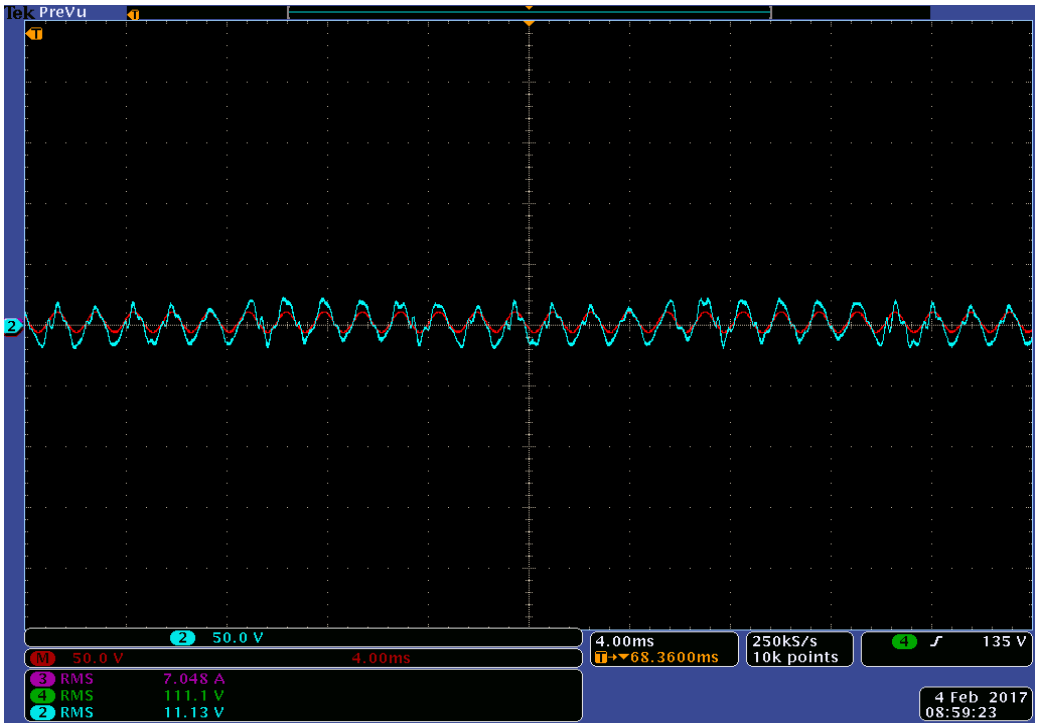


Figure 7.36: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario IV

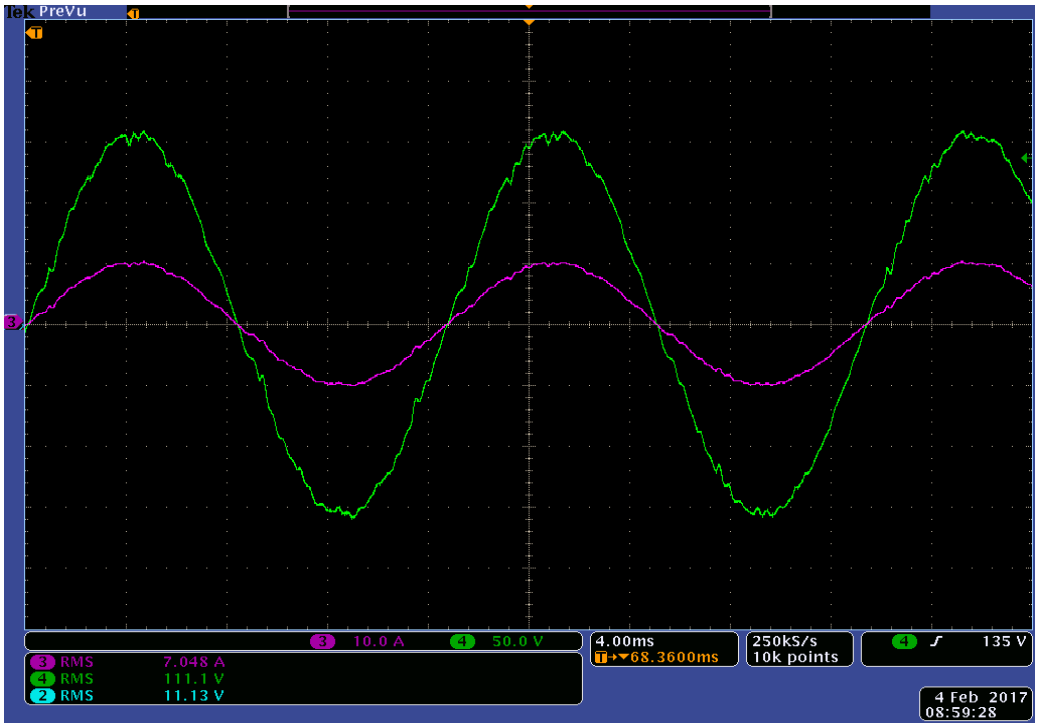


Figure 7.37: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario IV

The load voltage is restored to 110 V RMS with 2.05% THD from source voltage of 120.4 V RMS with 9.05% THD. The load voltage is not completely restored to 120 V RMS due to the losses occurring in the system. It can be noted that AC-DVR operates in similar manner discussed in section 6.3.4 and experimental results presented in this section closely resemble to the simulation results presented in section 6.3.4 for same operating scenario of 11th harmonic distortion.

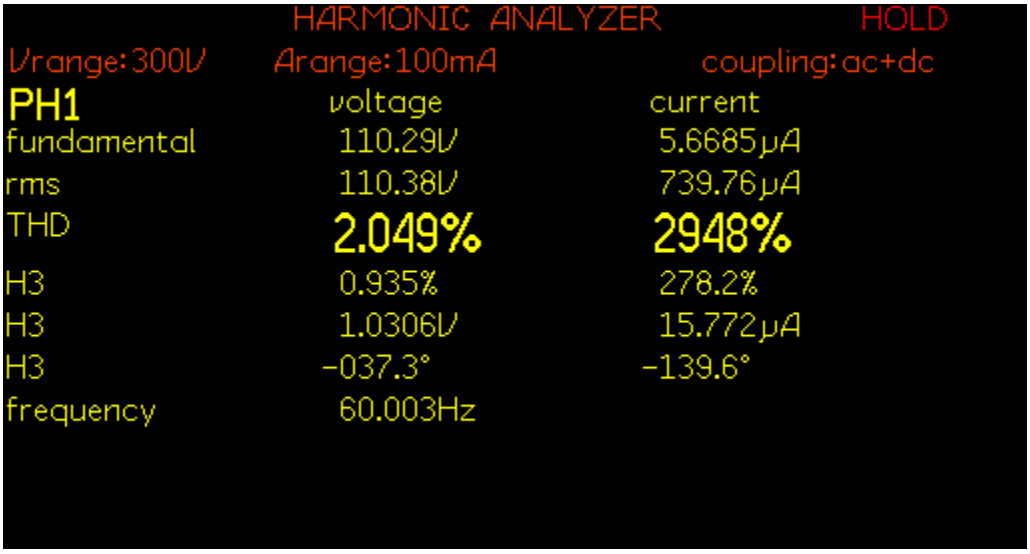


Figure 7.38: THD of load voltage V_{Load} for experiment scenario IV

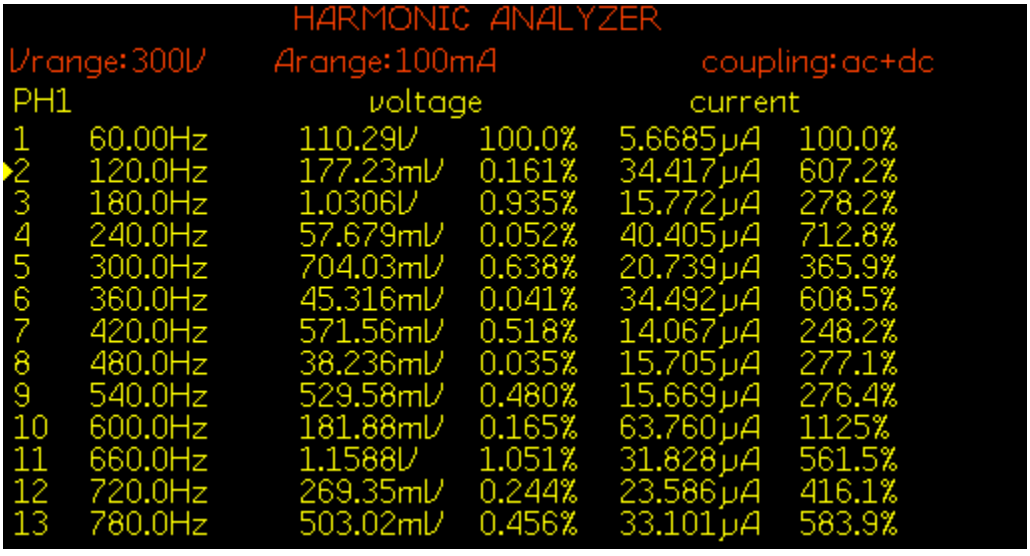


Figure 7.39: FFT of load voltage V_{Load} for experiment scenario IV

7.3.5 Combined harmonic distortion: Experiment scenario VIII

The fifth experiment was performed under similar parameters discussed in section 6.3.5. Distorted source voltage and load voltage reference are presented in Figure 7.40.

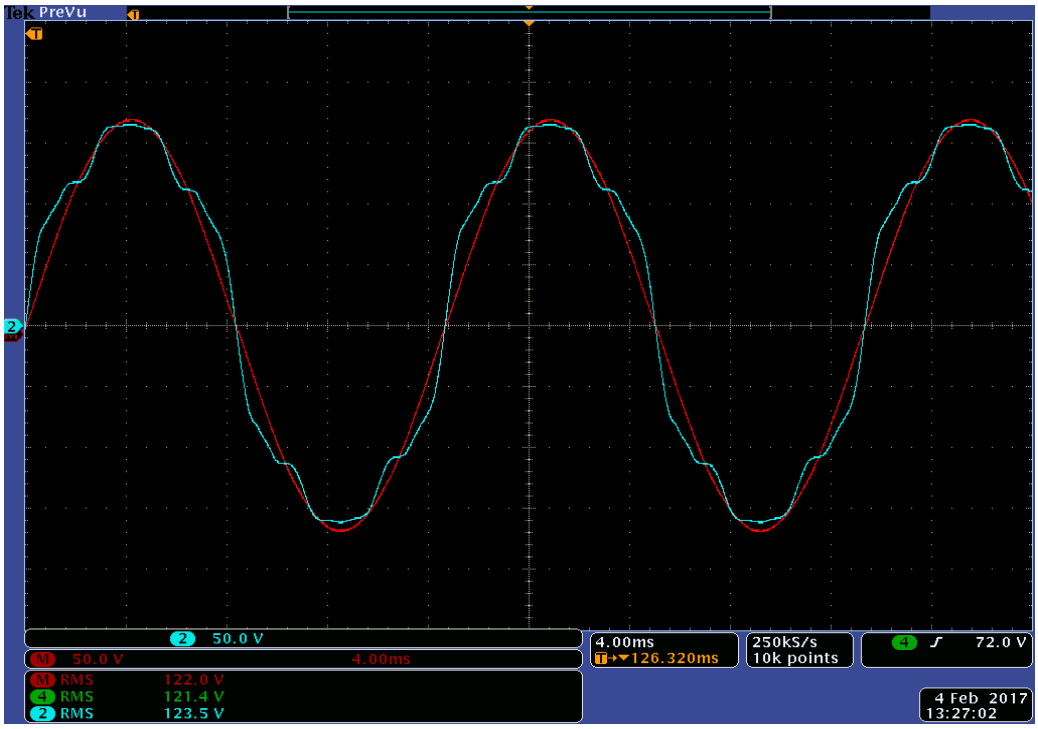


Figure 7.40: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario VIII

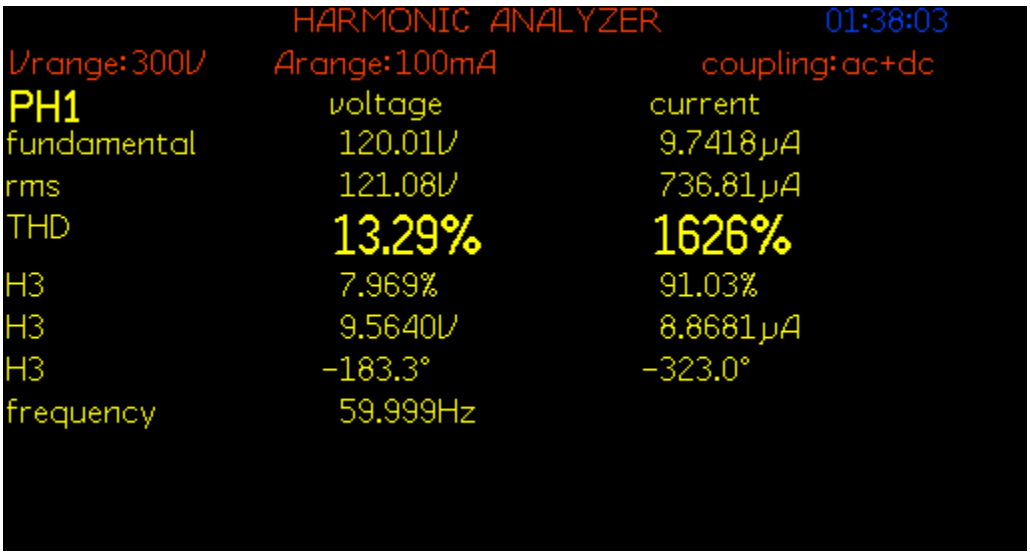


Figure 7.41: THD of source voltage V_{in} for experiment scenario VIII

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.41, 7.42, 7.43, 7.44,7.45, 7.46 and 7.47 respectively.

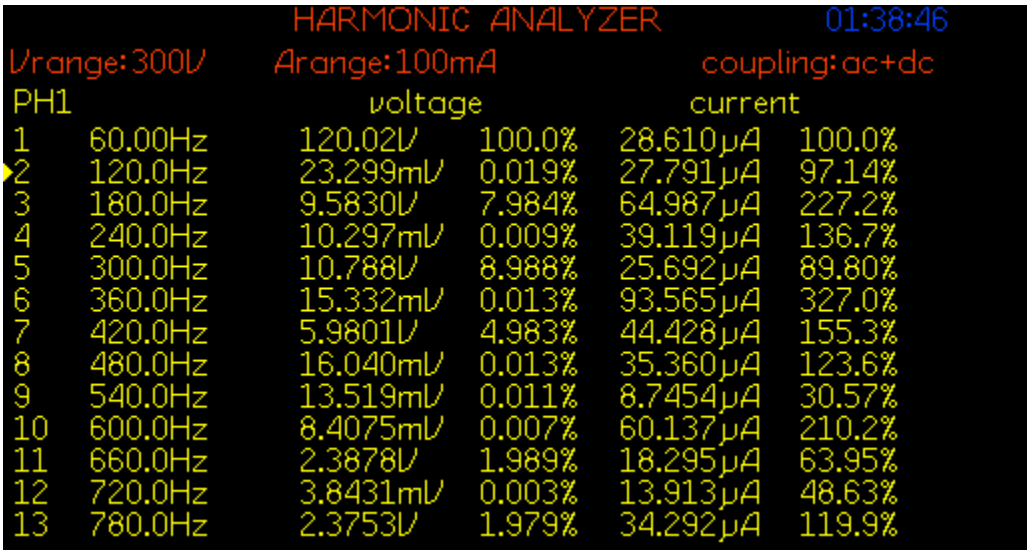


Figure 7.42: FFT of source voltage V_{in} for experiment scenario VIII

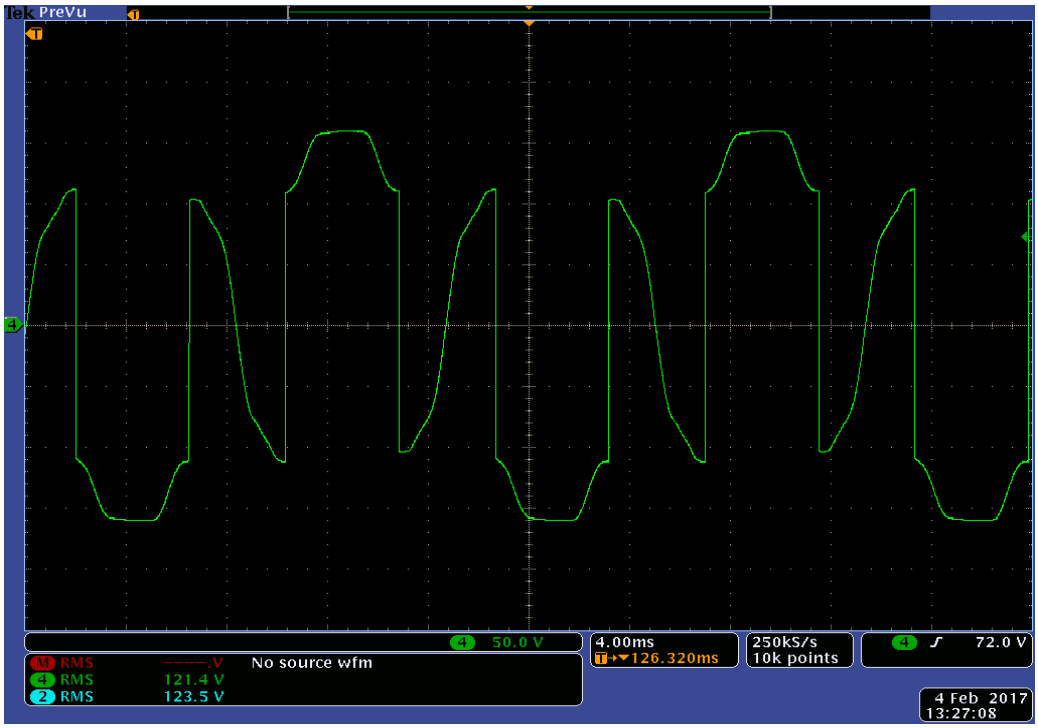


Figure 7.43: Experimental results of Bridge output voltage V_o for experiment scenario VIII

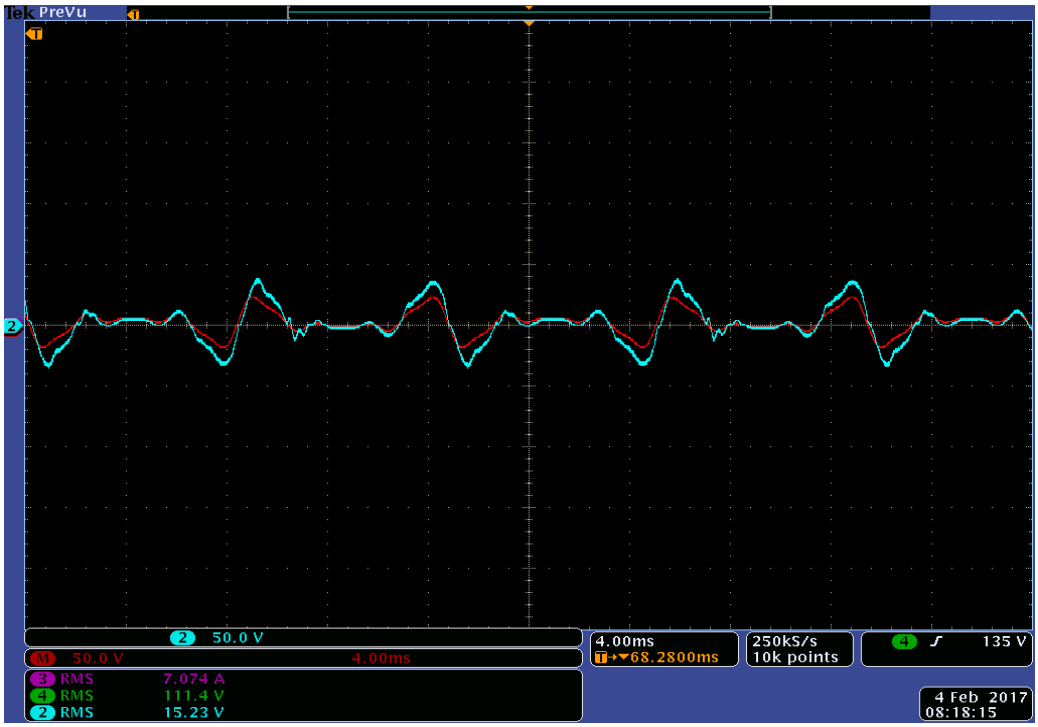


Figure 7.44: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario VIII

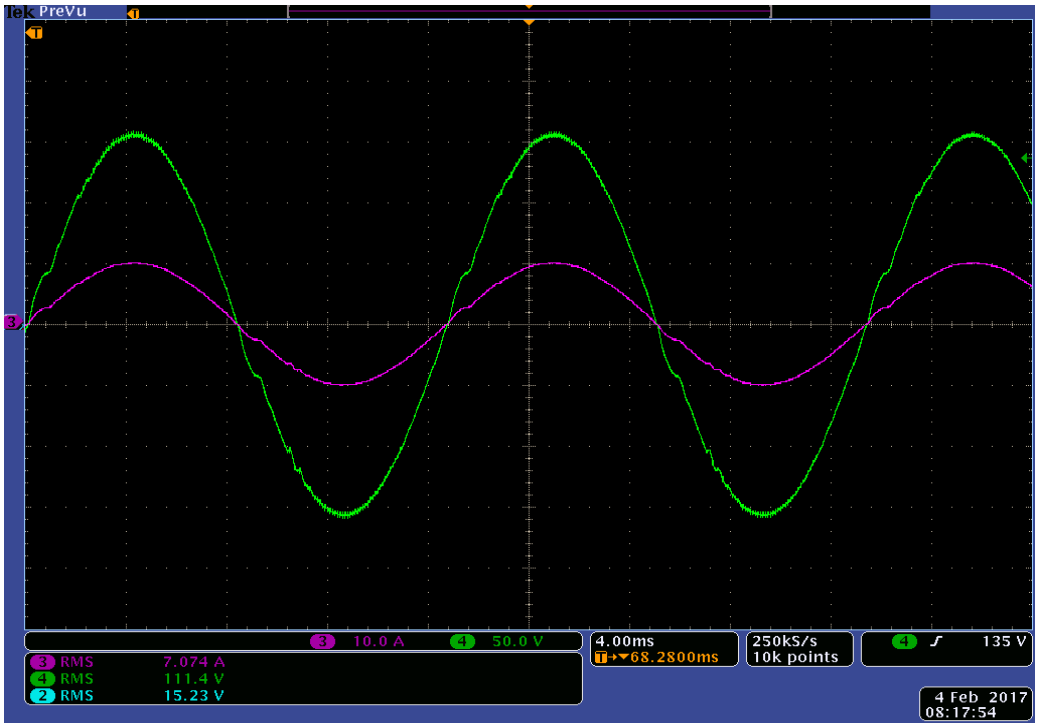


Figure 7.45: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario VIII

The load voltage is restored to 110 V RMS with 2.4% THD from source voltage of 121 V RMS with 13.29% THD. The source current, AC-DVR input current, inductor current and capacitor current are presented in Figures 7.48-7.51 respectively. It can be noted that AC-DVR operates in similar manner discussed in section 6.3.5 and experimental results presented in this section closely resemble to the simulation results presented in section 6.3.5 for same operating scenario of combined harmonic distortion.

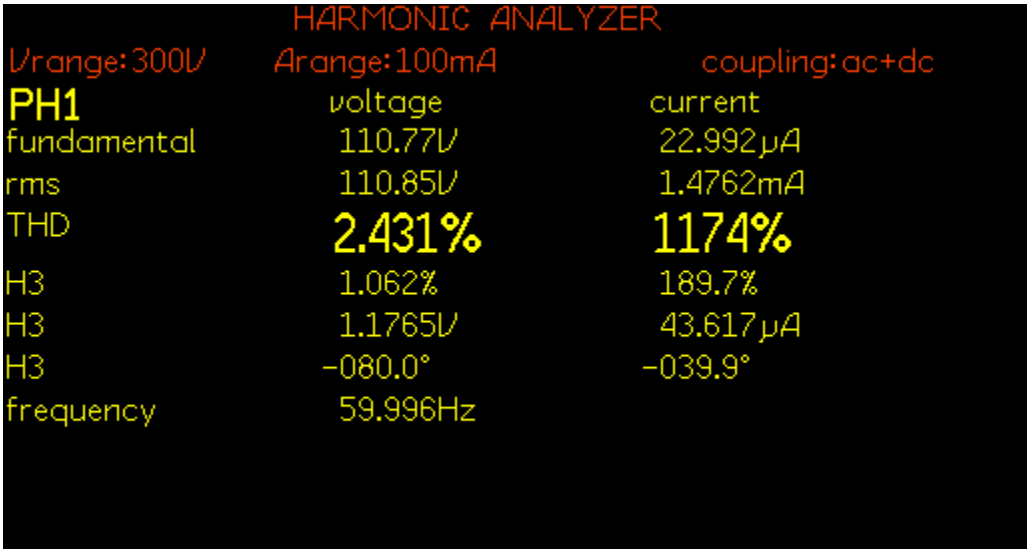


Figure 7.46: THD of load voltage V_{Load} for experiment scenario VIII

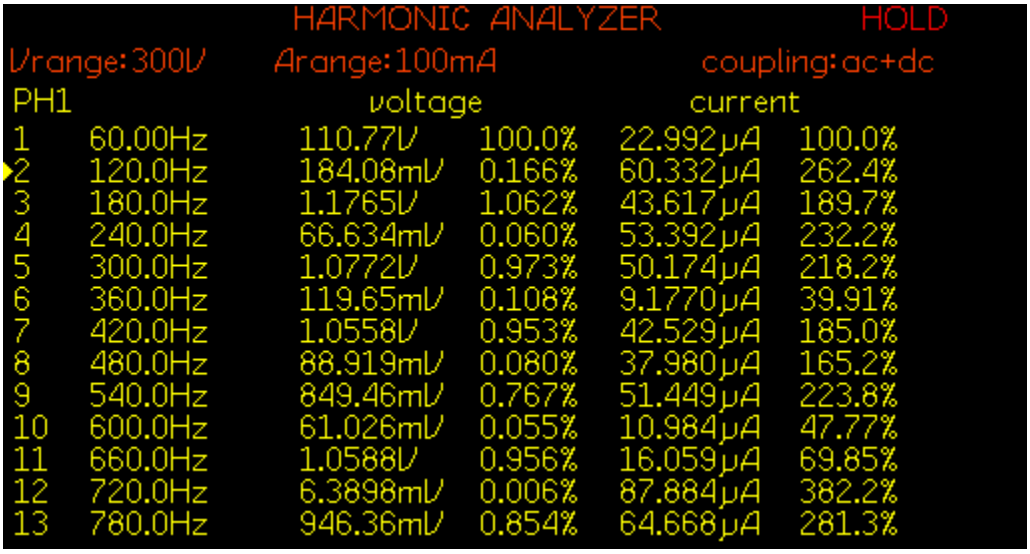


Figure 7.47: FFT of load voltage V_{Load} for experiment scenario VIII

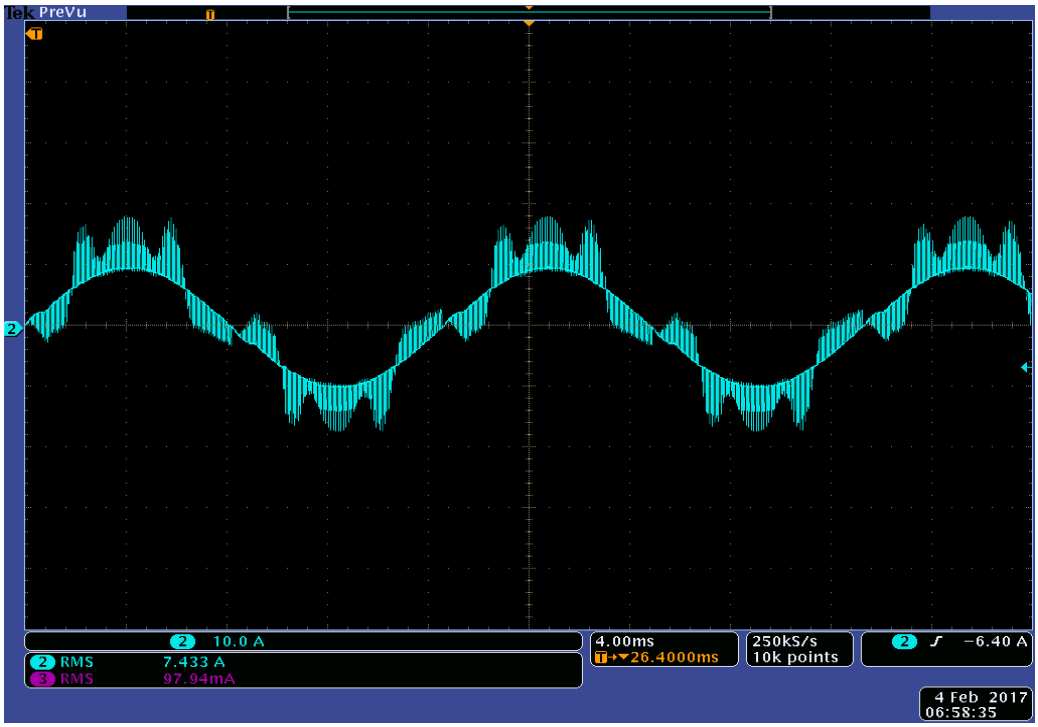


Figure 7.48: Experimental Results of Actual source current I_{in} for experiment scenario VIII

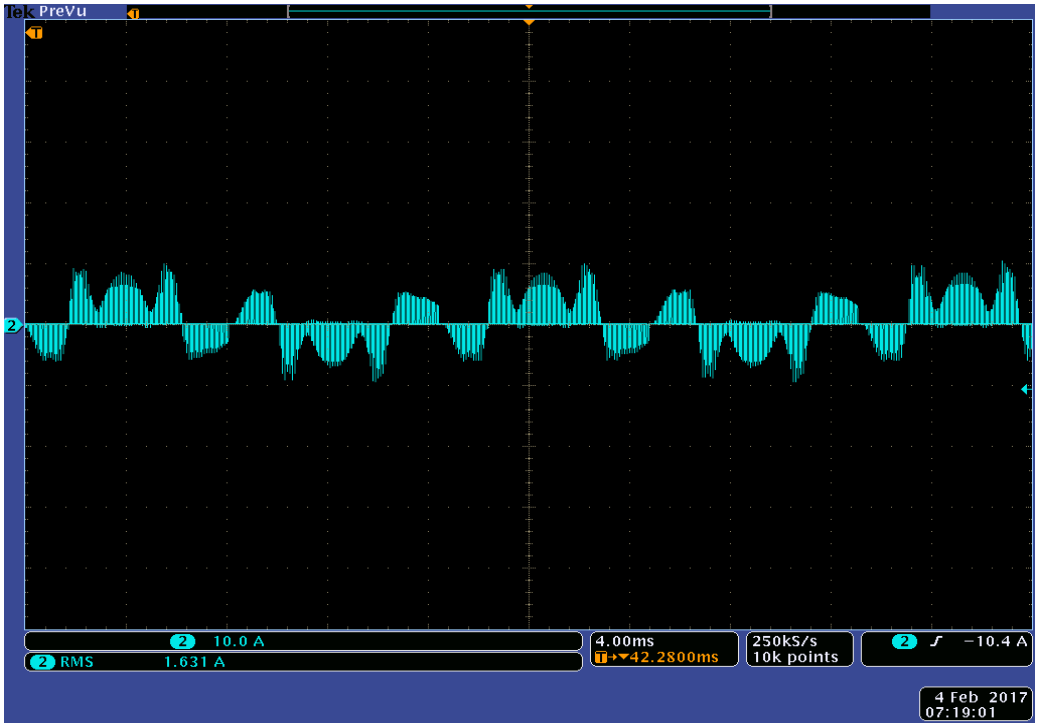


Figure 7.49: Experimental Results of Actual DVR current I_{DVR-IN} for experiment scenario VIII

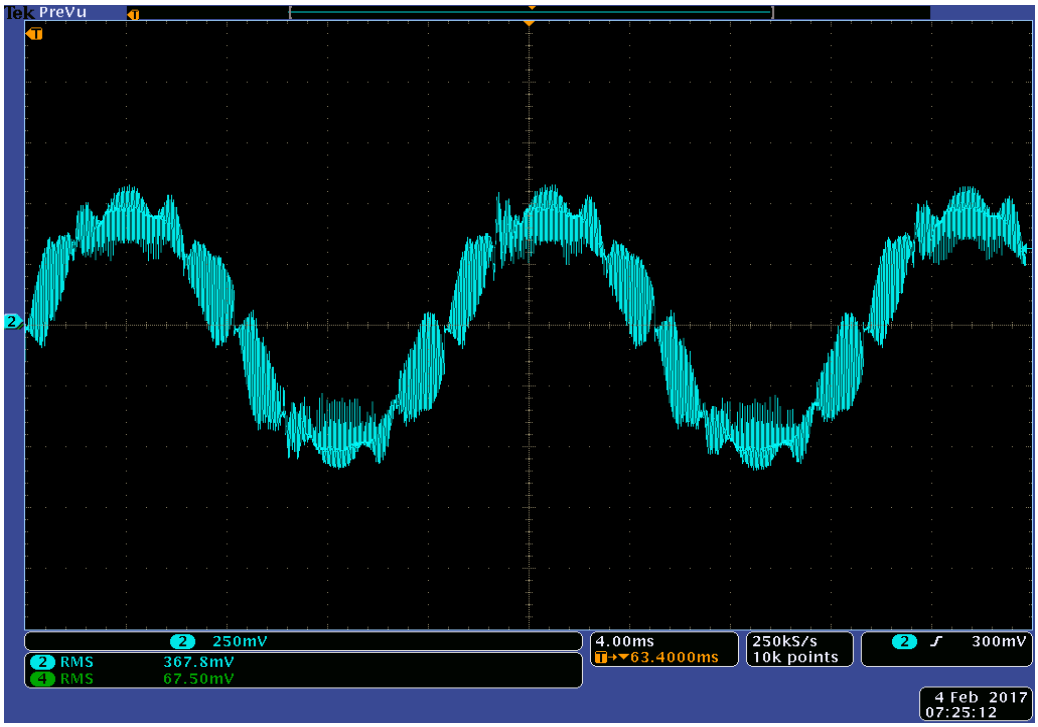


Figure 7.50: Experimental Results of Actual inductor current I_L for experiment scenario VIII

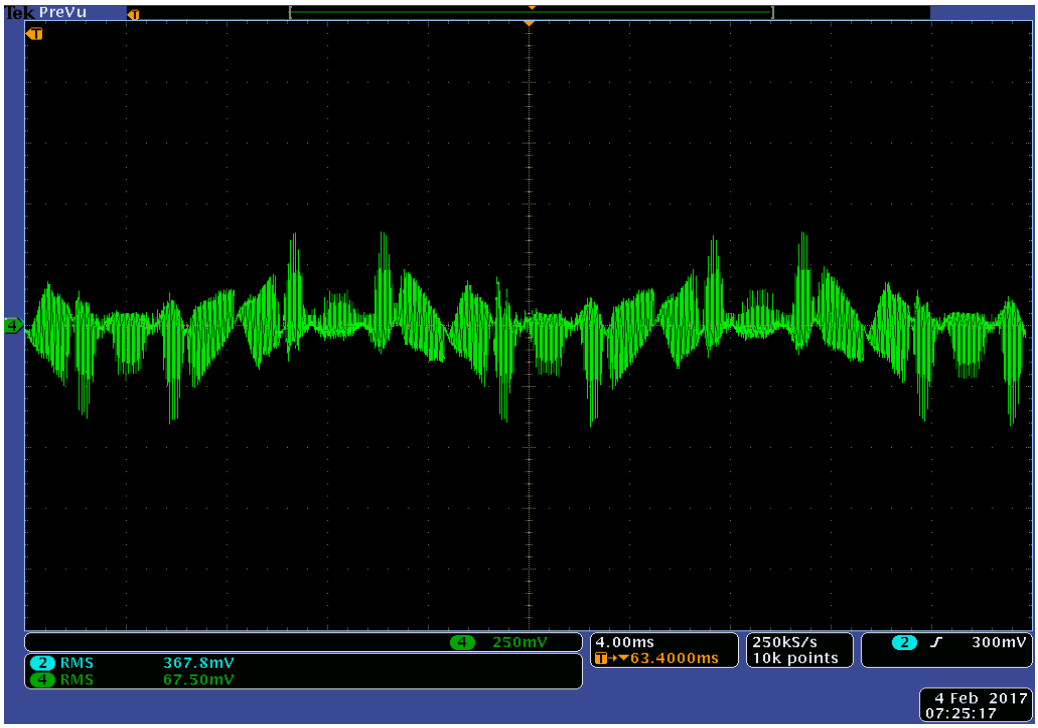


Figure 7.51: Experimental Results of Actual capacitor current I_C for operating scenario VIII

7.3.6 Combined harmonic distortion: Experiment scenario IX

The sixth experiment was performed under similar parameters discussed in section 6.3.6. The source voltage and load voltage reference are presented in Figure 7.52.

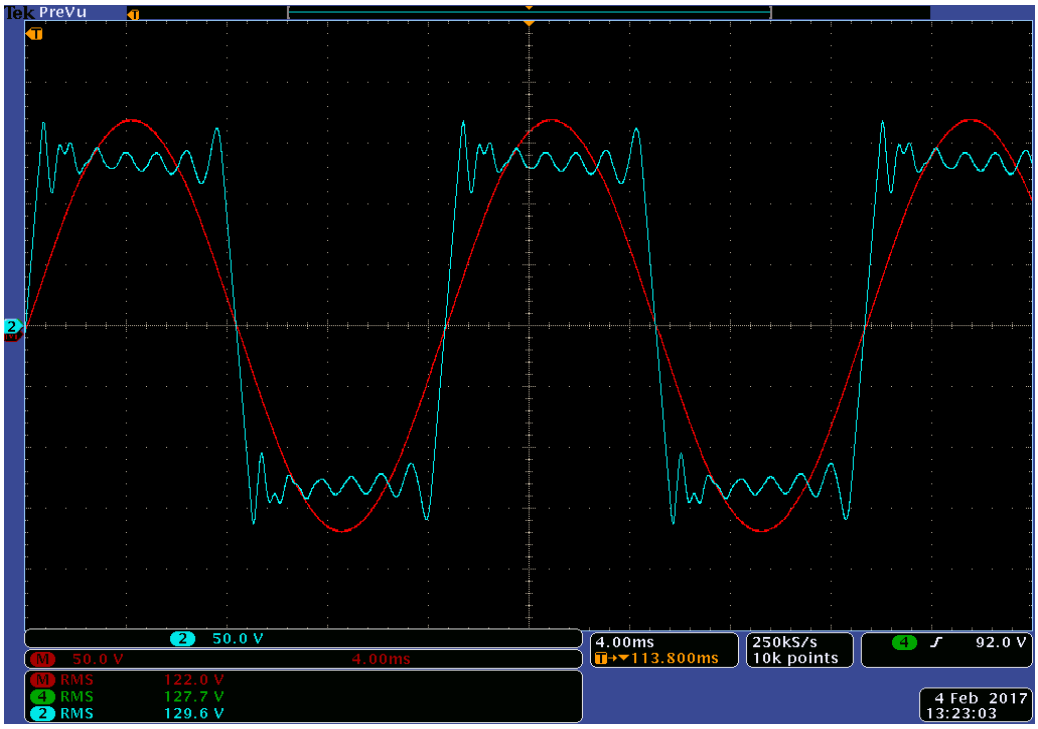


Figure 7.52: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario IX

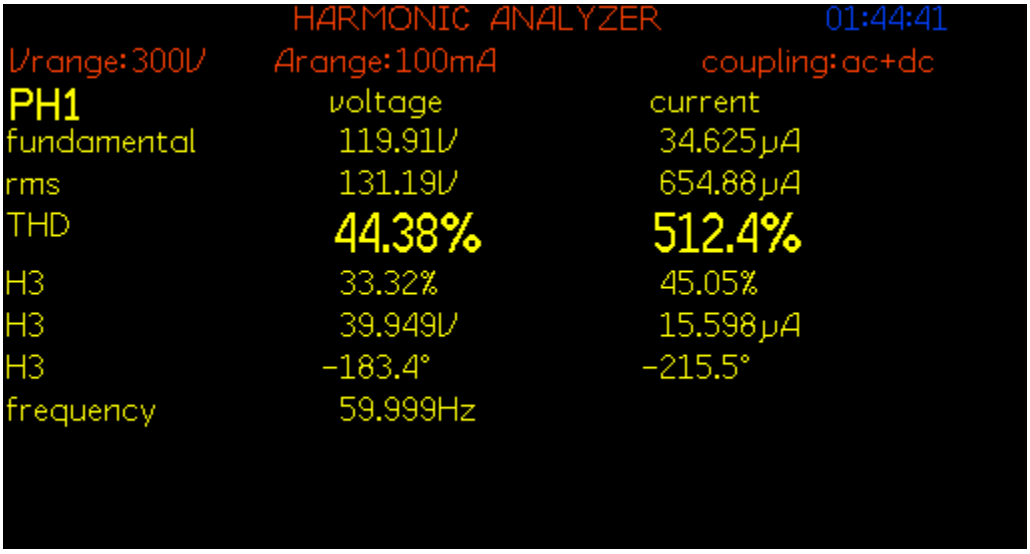


Figure 7.53: THD of source voltage V_{in} for experiment scenario IX

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.53, 7.54, 7.55, 7.56,7.57, 7.58 and 7.59 respectively.

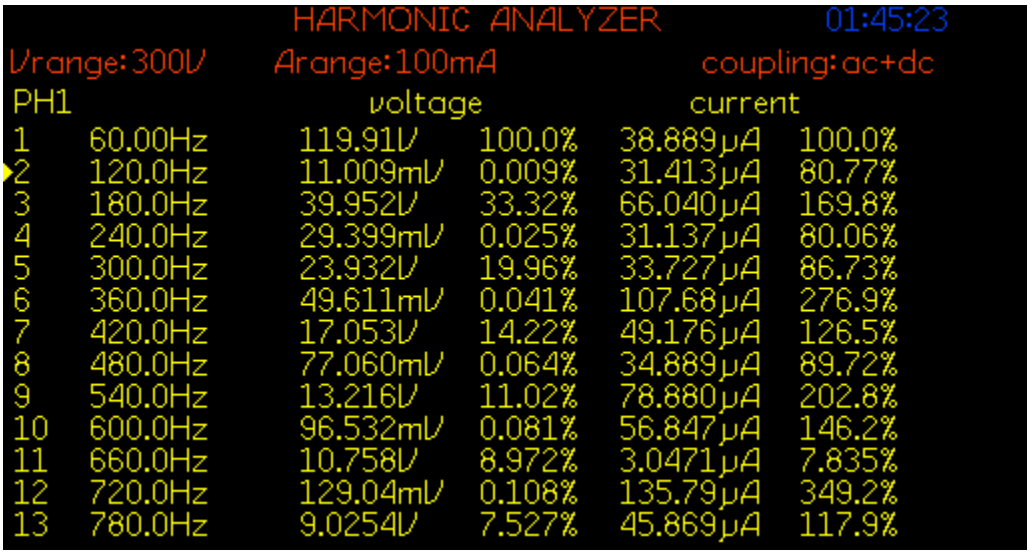


Figure 7.54: FFT of source voltage V_{in} for experiment scenario IX

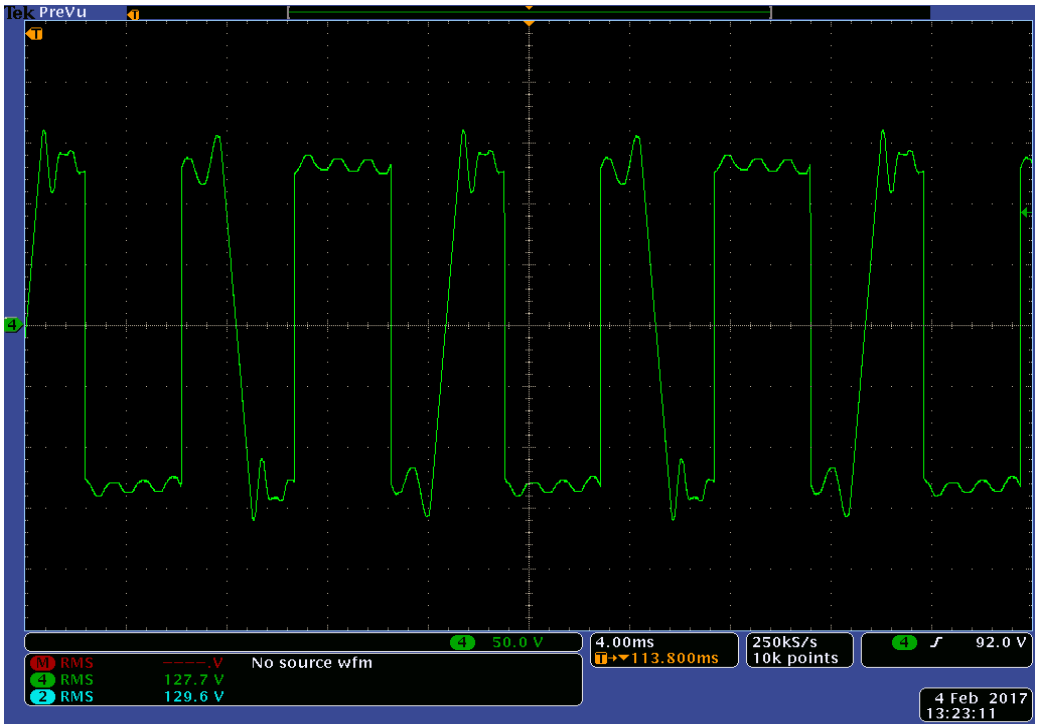


Figure 7.55: Experimental results of Bridge output voltage V_o for experiment scenario IX

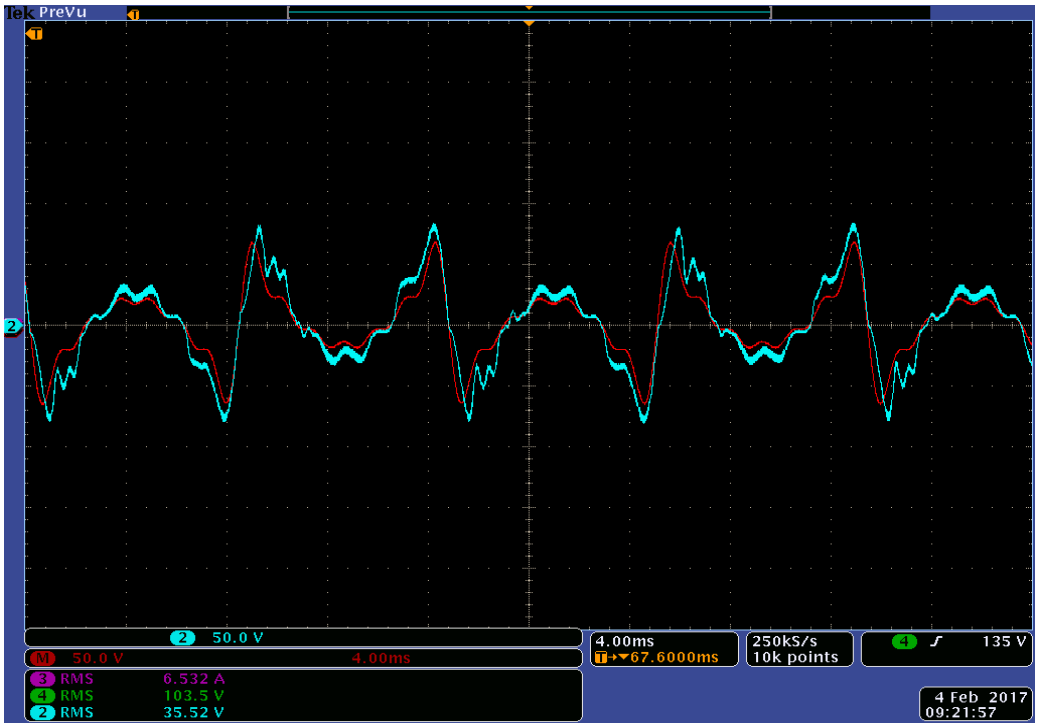


Figure 7.56: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario IX

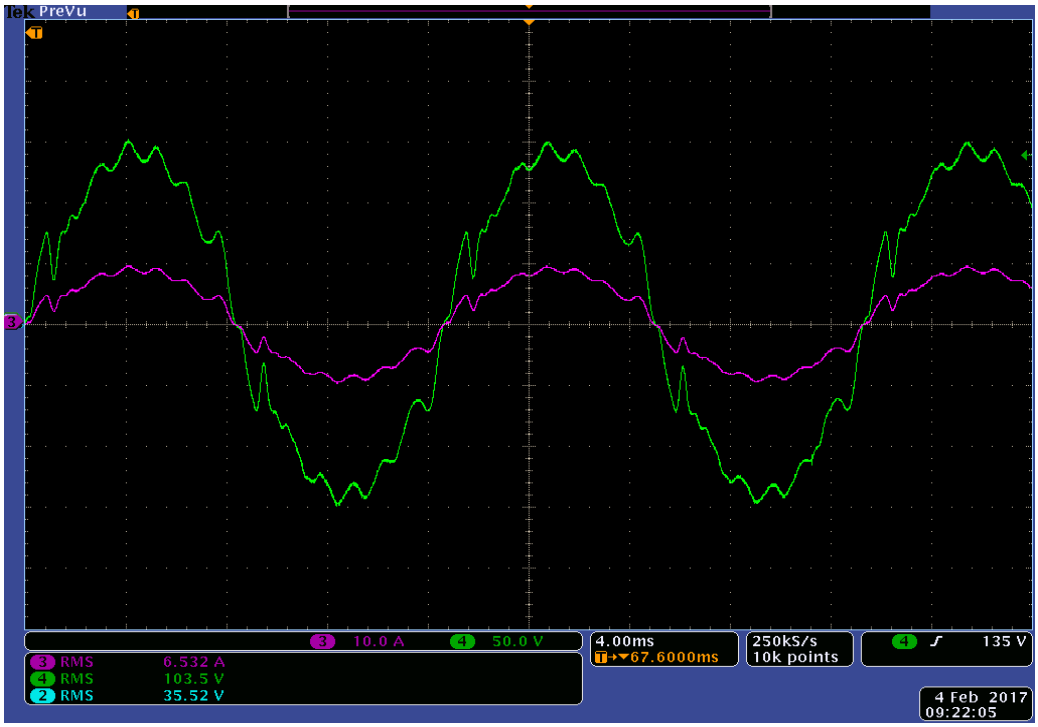


Figure 7.57: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario IX

The load voltage is restored to 100 V RMS with 12% THD from source voltage of 131.2 V RMS with 44.38% THD. It can be observed that AC-DVR fails to restore load voltage with less than 5% THD and shape of the load voltage is also not sinusoidal. The drop in load voltage magnitude is caused by system losses. Empirical design of L and C; unknown boundary conditions and lower switching frequency of buck boost can be the reasons of AC-DVR failure under this operating scenario.

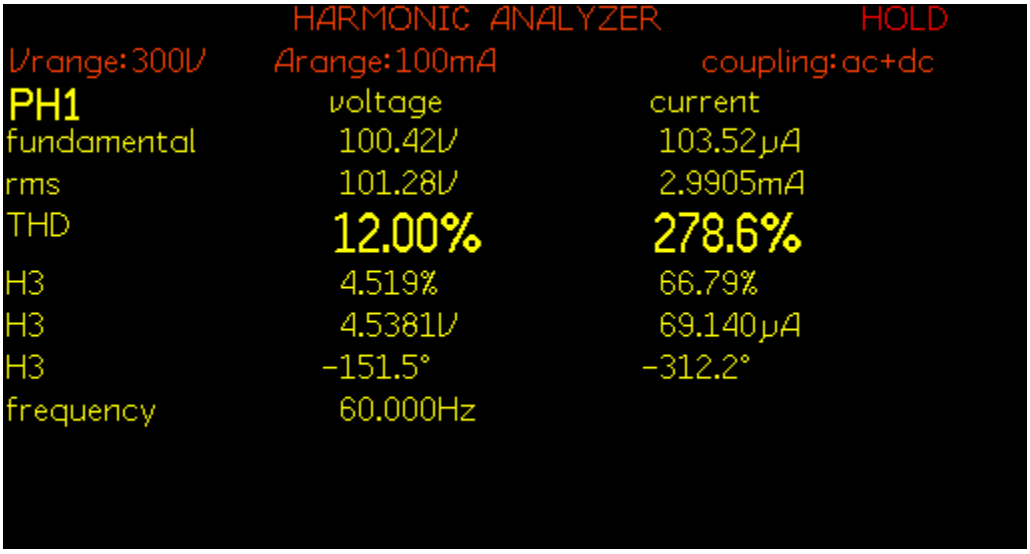


Figure 7.58: THD of load voltage V_{Load} for experiment scenario IX

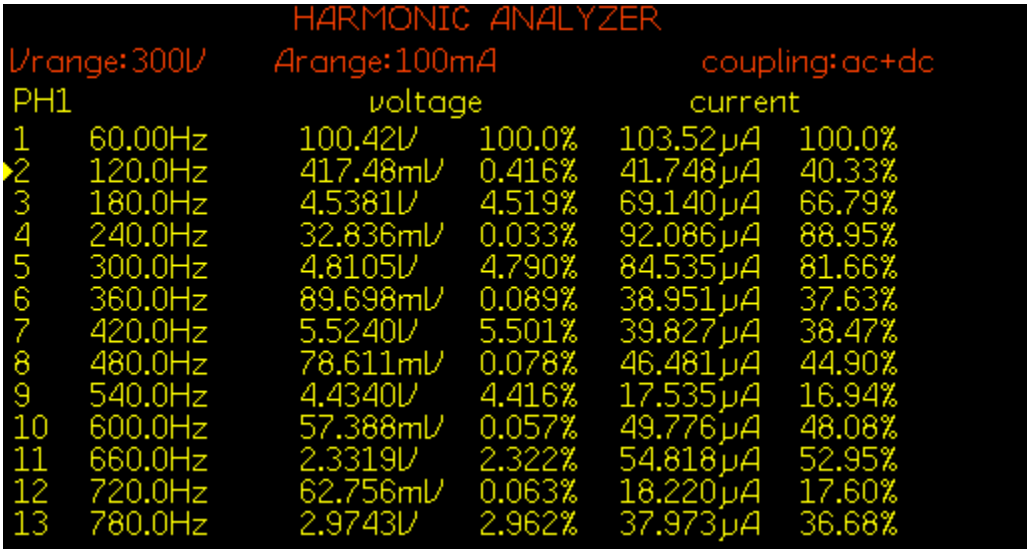


Figure 7.59: FFT of load voltage V_{Load} for experiment scenario IX

7.3.7 Voltage sag: Experiment scenario X

This experiment was performed under similar parameters of sag discussed in section 6.3.7. The source voltage and load voltage reference are presented in Figure 7.60.

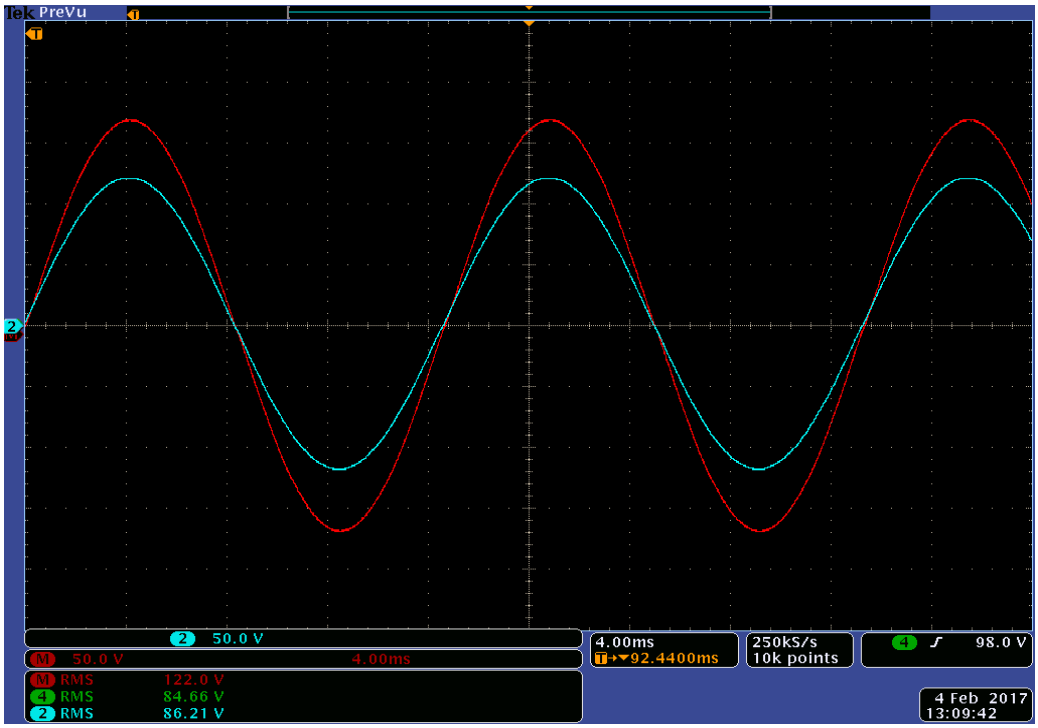


Figure 7.60: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario X

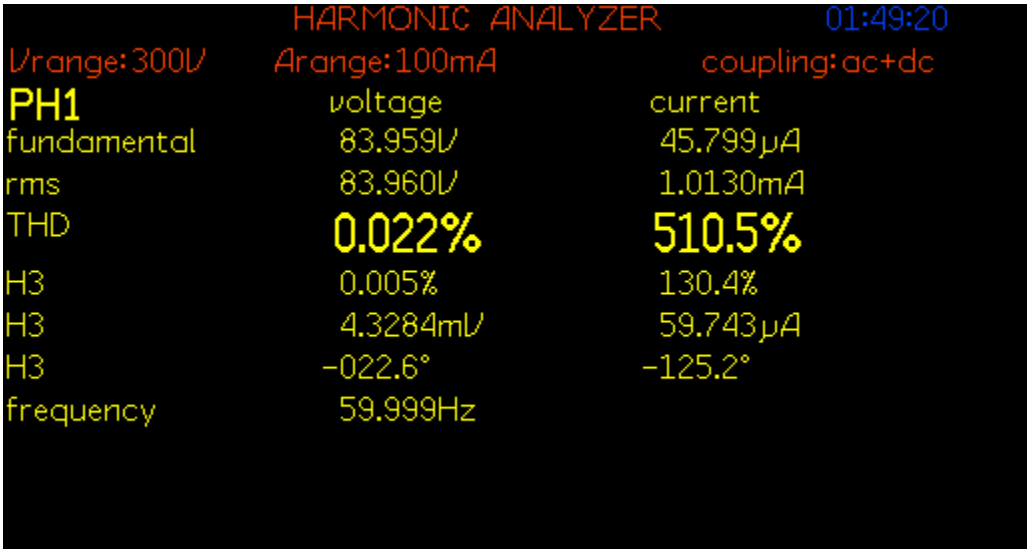


Figure 7.61: THD of source voltage V_{in} for experiment scenario X

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.61, 7.62, 7.63, 7.64,7.65, 7.66 and 7.67 respectively.

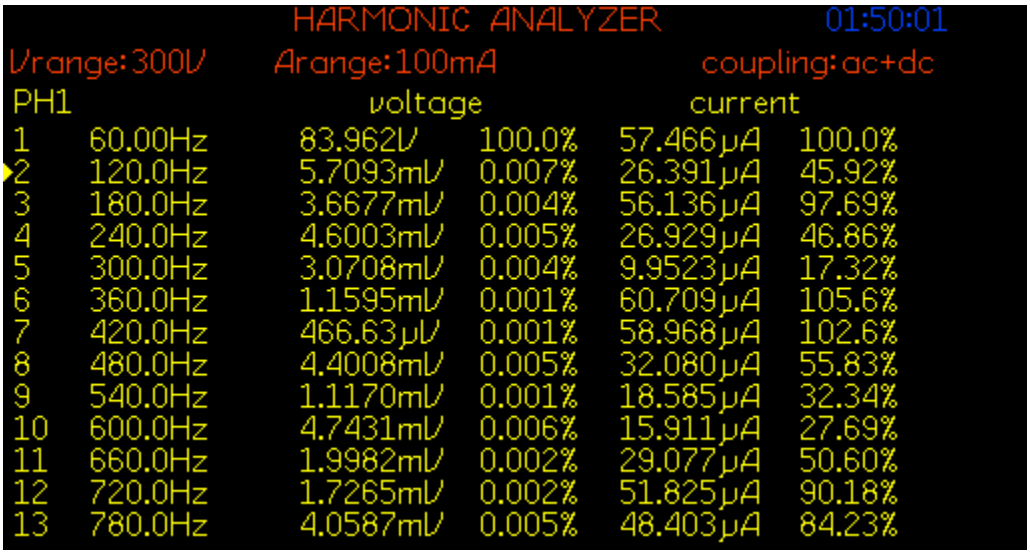


Figure 7.62: FFT of source voltage V_{in} for experiment scenario X

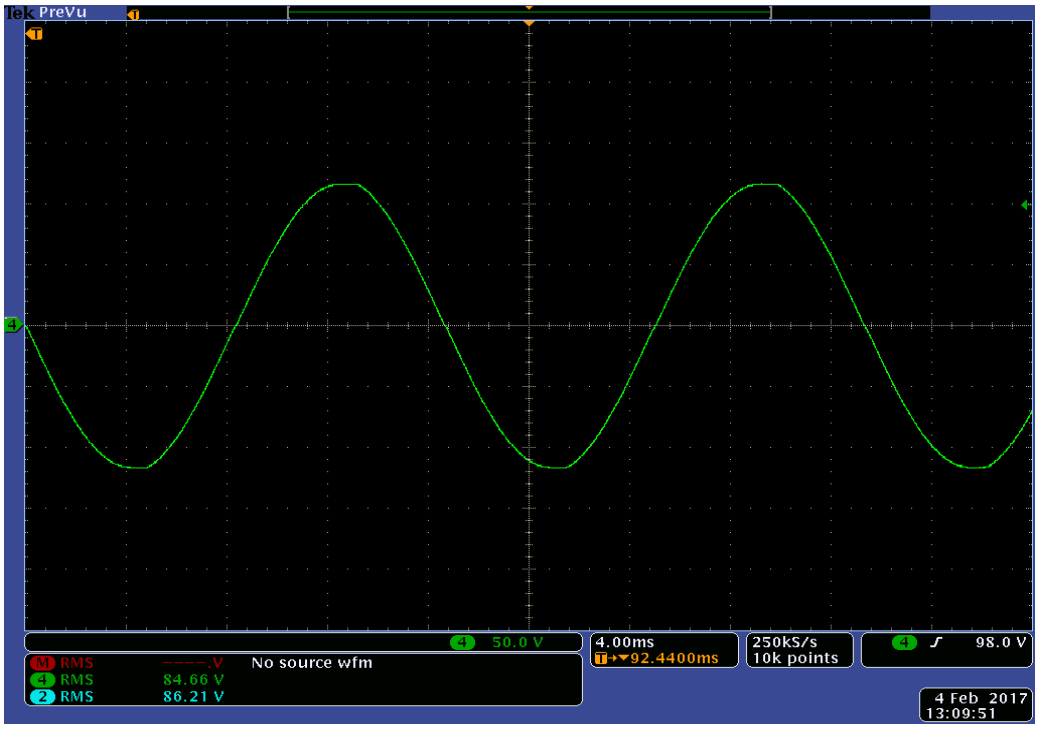


Figure 7.63: Experimental results of Bridge output voltage V_o for experiment scenario X

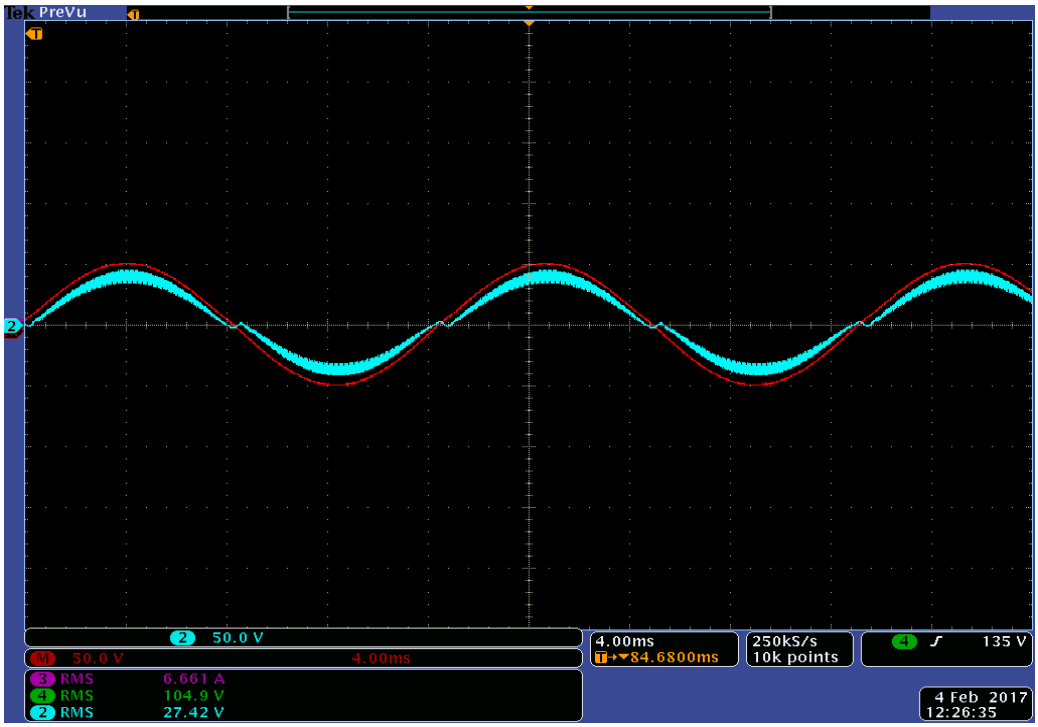


Figure 7.64: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario X

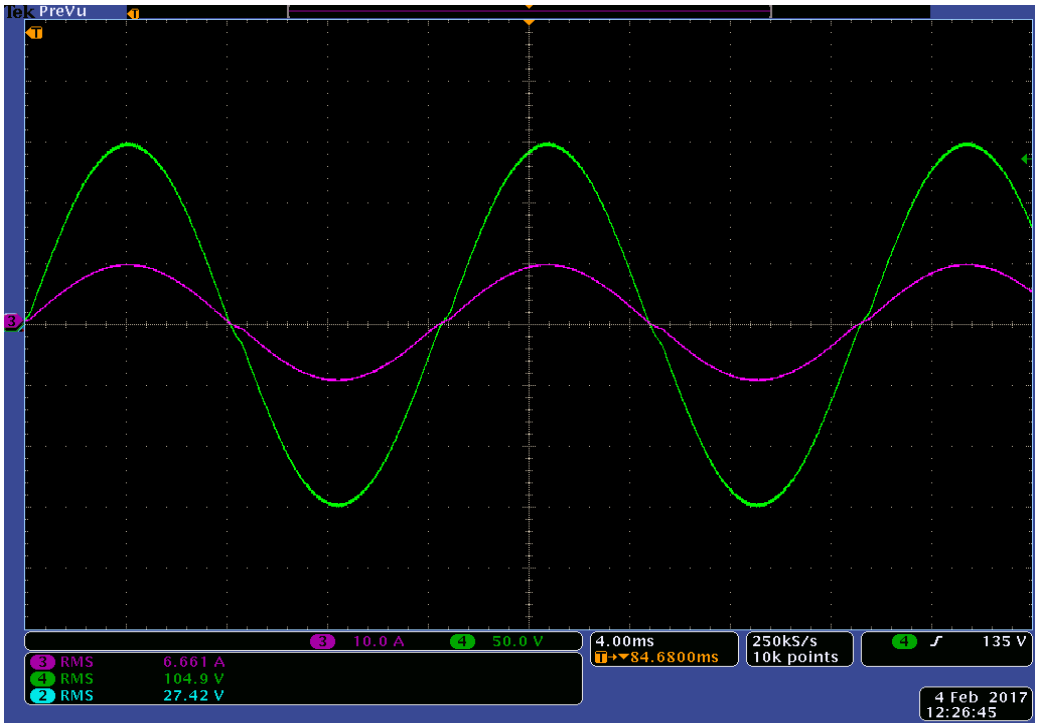


Figure 7.65: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario X

The load voltage is restored to 104 V RMS with 1.98% THD from source voltage of 84 V RMS with 0.022% THD. The load voltage is not completely restored to 120 V RMS due to the losses occurring in the system. It can be noted that AC-DVR operates in similar manner discussed in section 6.3.7 and experimental results presented in this section closely resemble to the simulation results presented in section 6.3.7 for same operating scenario of voltage sag harmonic distortion.

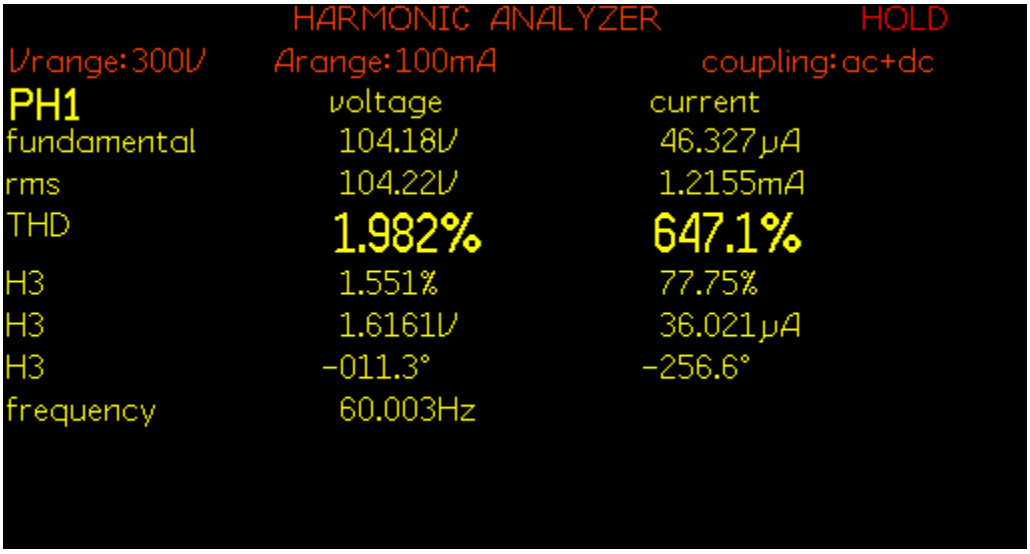


Figure 7.66: THD of load voltage V_{Load} for experiment scenario X

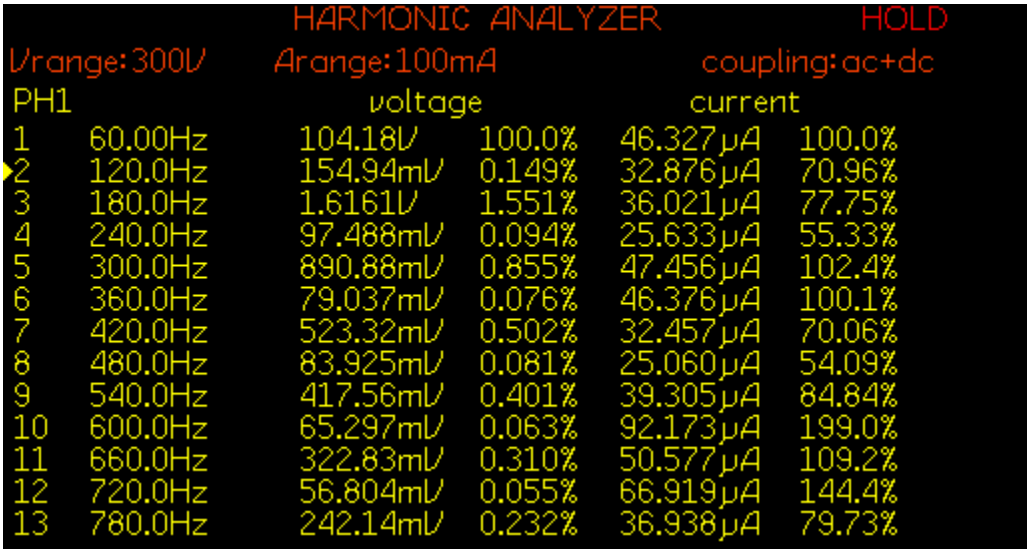


Figure 7.67: FFT of load voltage V_{Load} for experiment scenario X

7.3.8 Voltage swell: Experiment scenario XI

This experiment was performed under similar parameters of swell discussed in section 6.3.8. The source voltage and load voltage reference are presented in Figure 7.68.

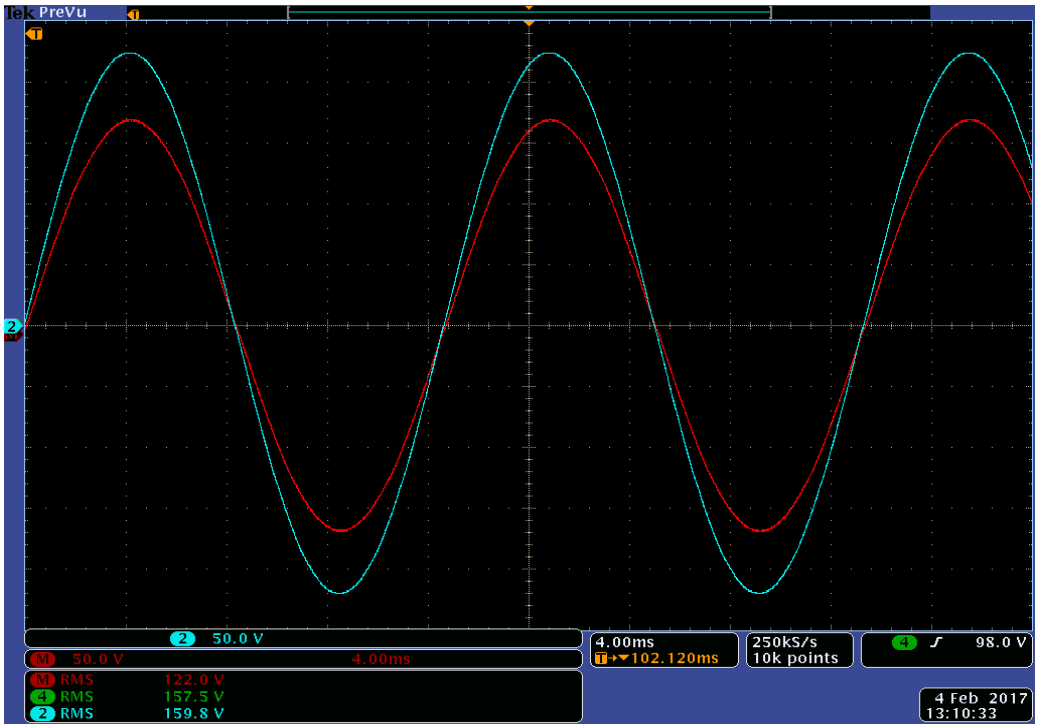


Figure 7.68: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario XI

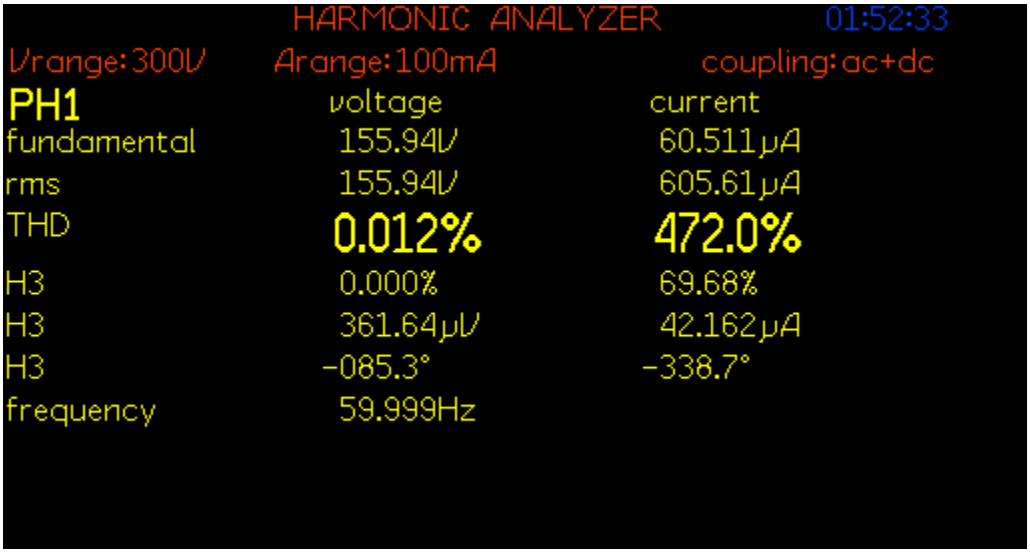


Figure 7.69: THD of source voltage V_{in} for experiment scenario XI

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.69, 7.70, 7.71, 7.72,7.73, 7.74 and 7.75 respectively.

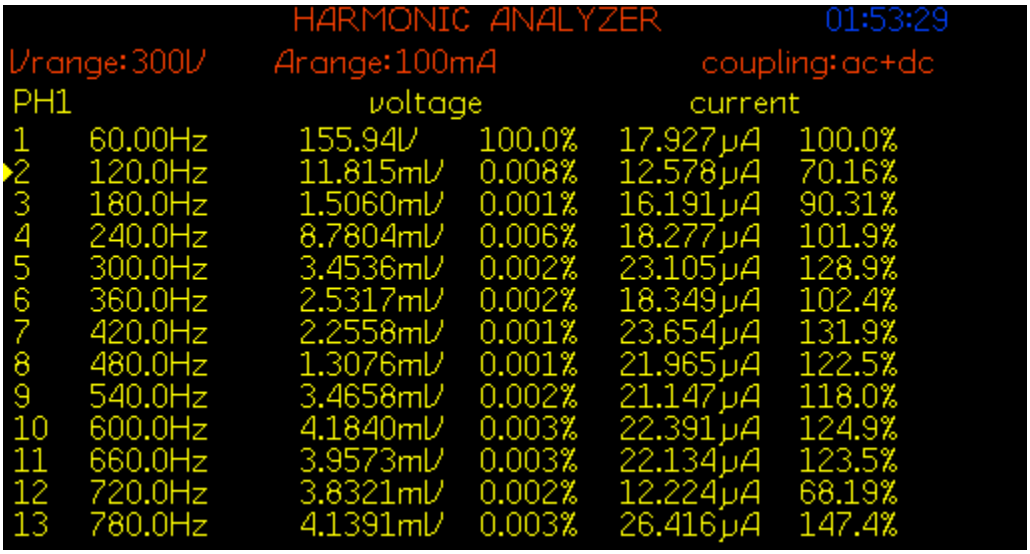


Figure 7.70: FFT of source voltage V_{in} for experiment scenario XI

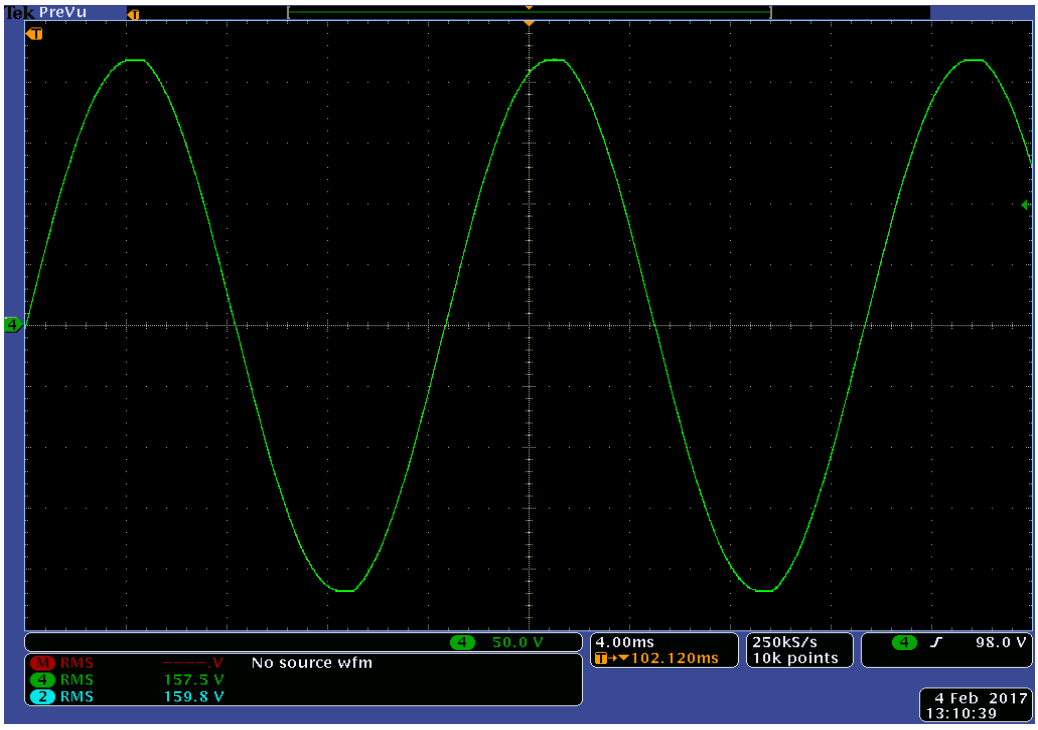


Figure 7.71: Experimental results of Bridge output voltage V_o for experiment scenario XI

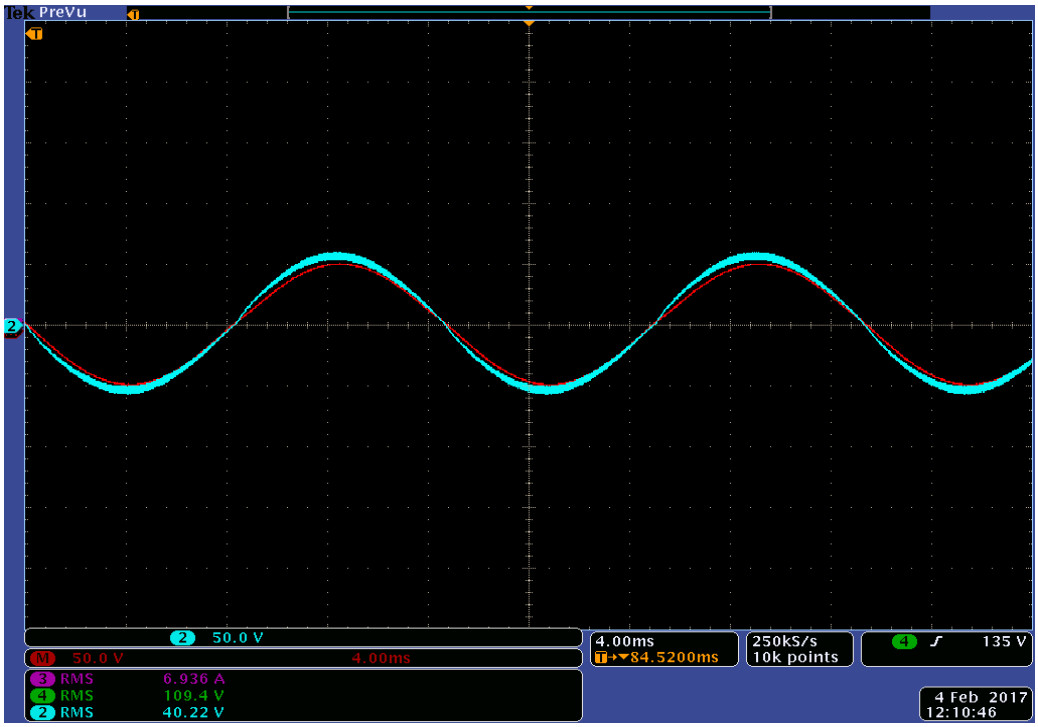


Figure 7.72: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario XI

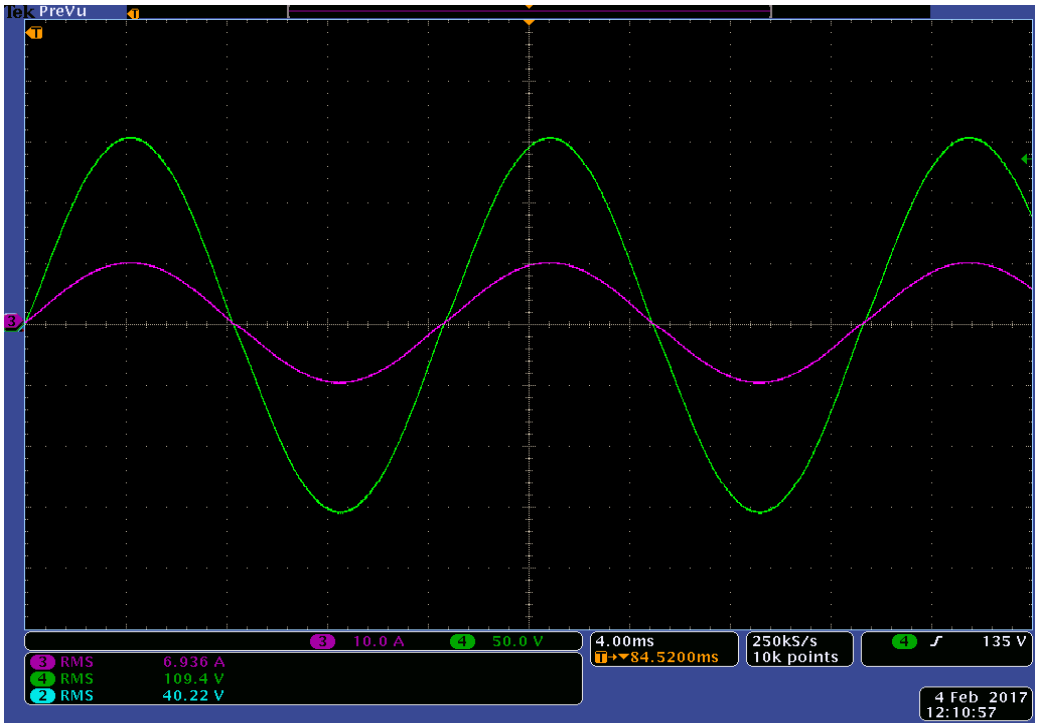


Figure 7.73: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario XI

The load voltage is restored to 108 V RMS with 1.07% THD from source voltage of 156 V RMS with 0.012% THD. The load voltage is not completely restored to 120 V RMS due to the losses occurring in the system. It can be noted that AC-DVR operates in similar manner discussed in section 6.3.8 and experimental results presented in this section closely resemble to the simulation results presented in section 6.3.8 for same operating scenario of voltage swell harmonic distortion.

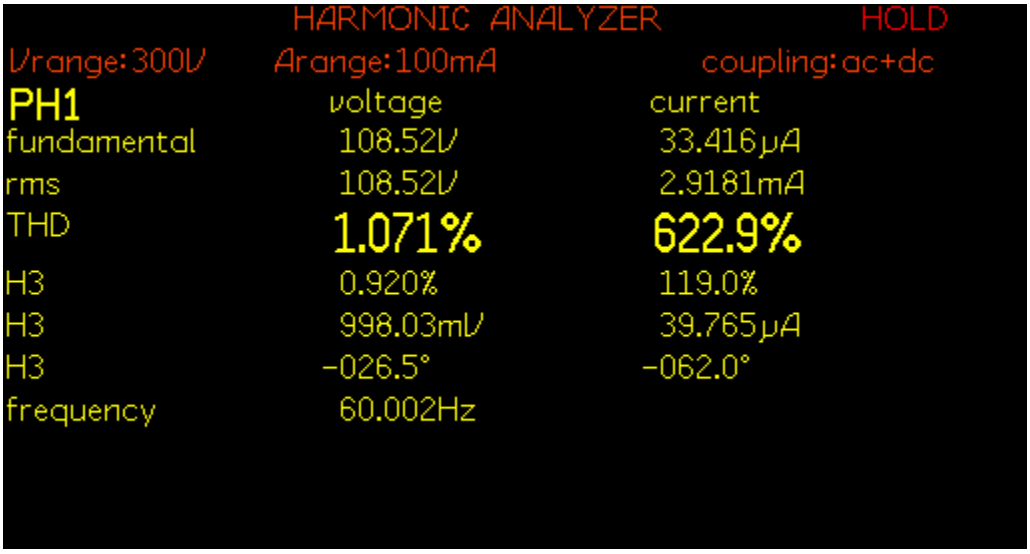


Figure 7.74: THD of load voltage V_{Load} for experiment scenario XI

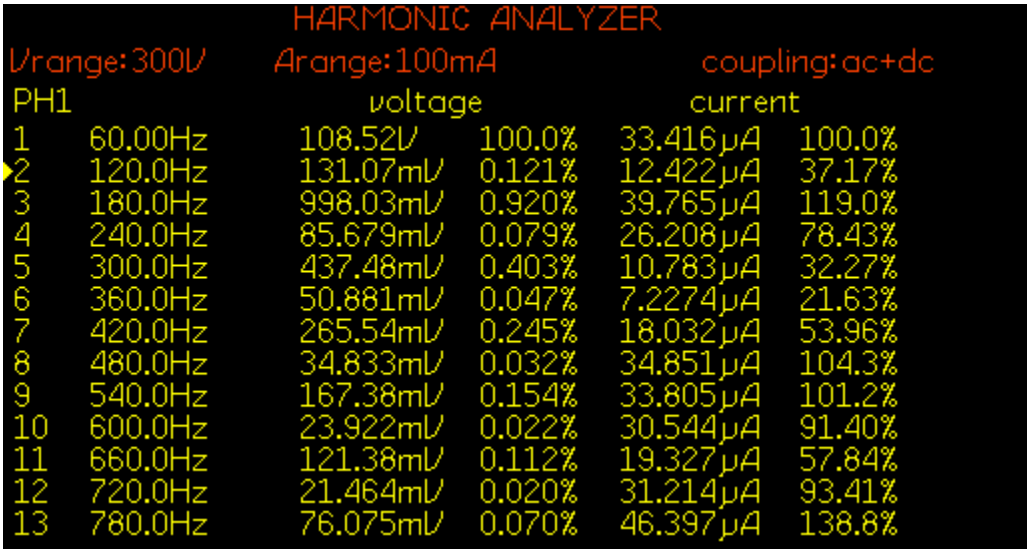


Figure 7.75: FFT of load voltage V_{Load} for experiment scenario XI

7.3.9 Combined harmonic and voltage sag: Experiment scenario XII

The ninth experiment was performed under similar parameters discussed in section 6.3.9. The source voltage and load voltage reference are presented in Figure 7.76.

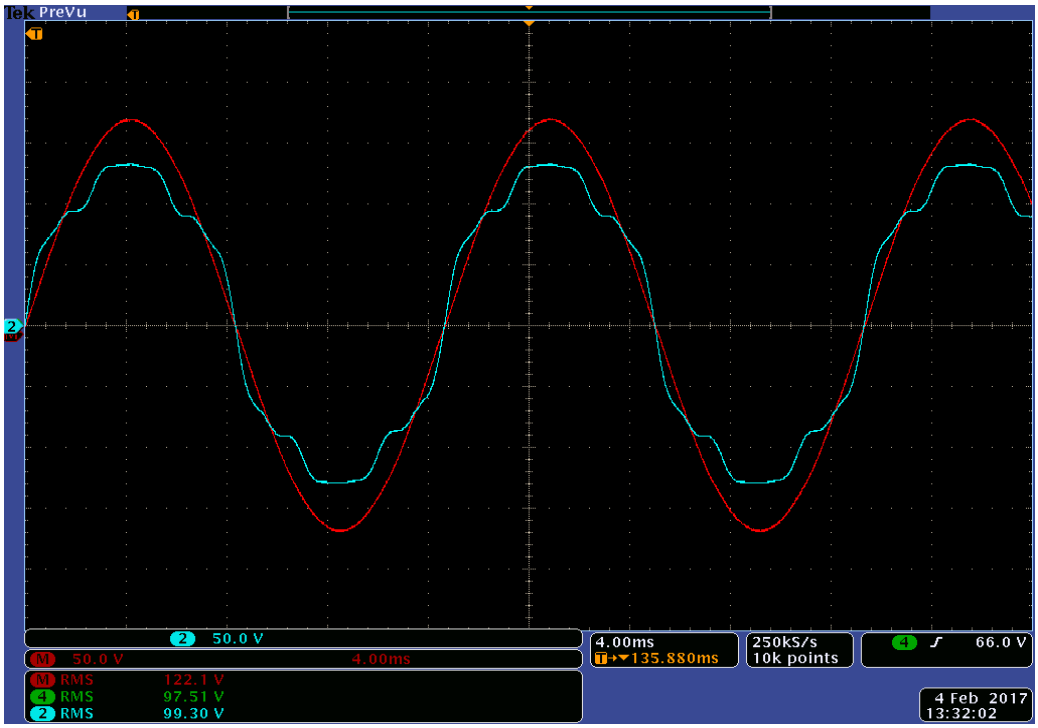


Figure 7.76: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario XII

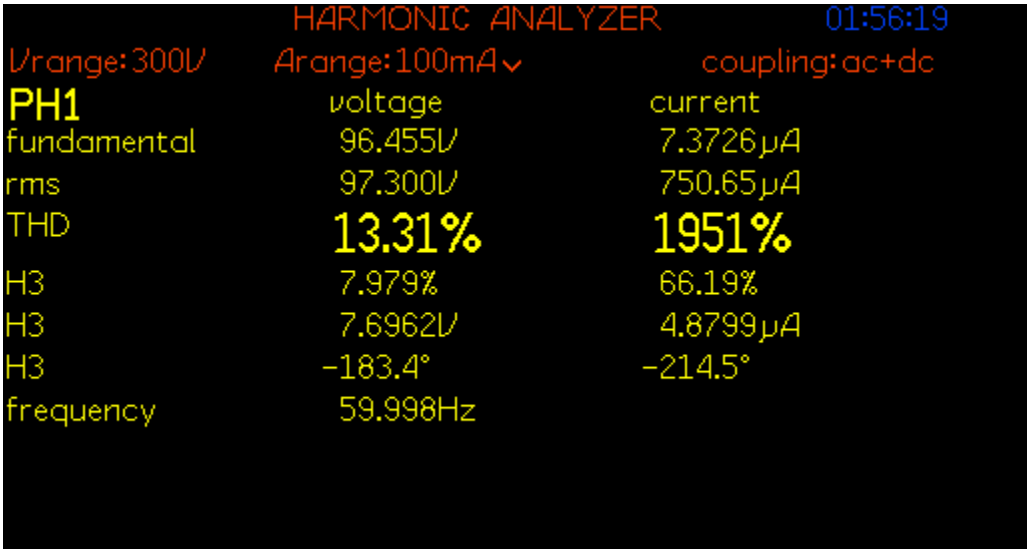


Figure 7.77: THD of source voltage V_{in} for experiment scenario XII

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.77, 7.78, 7.79, 7.80,7.81, 7.82 and 7.83 respectively.

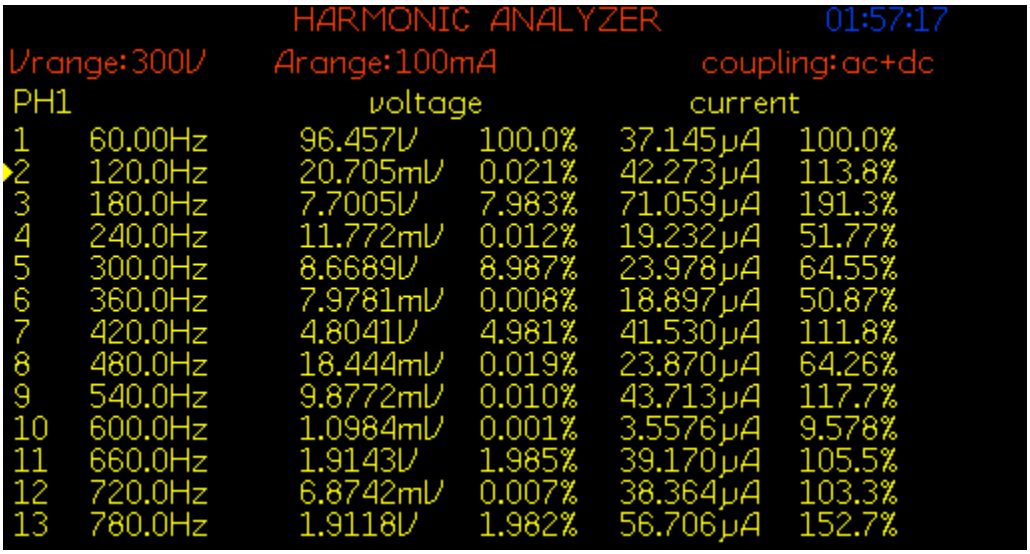


Figure 7.78: FFT of source voltage V_{in} for experiment scenario XII

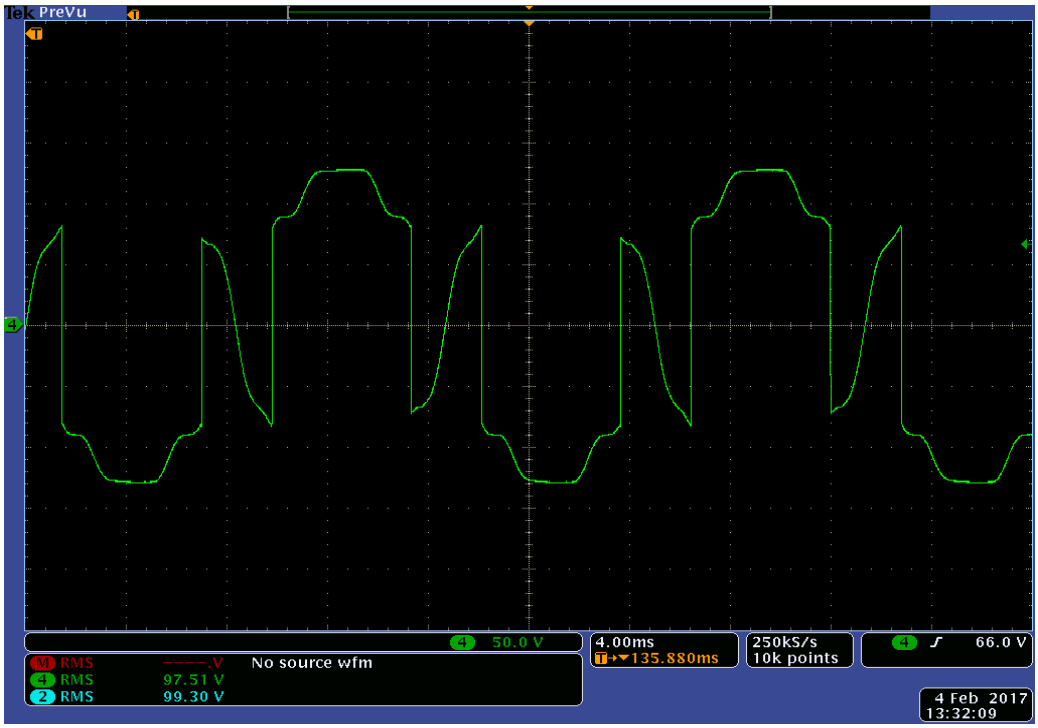


Figure 7.79: Experimental results of Bridge output voltage V_o for experiment scenario XII

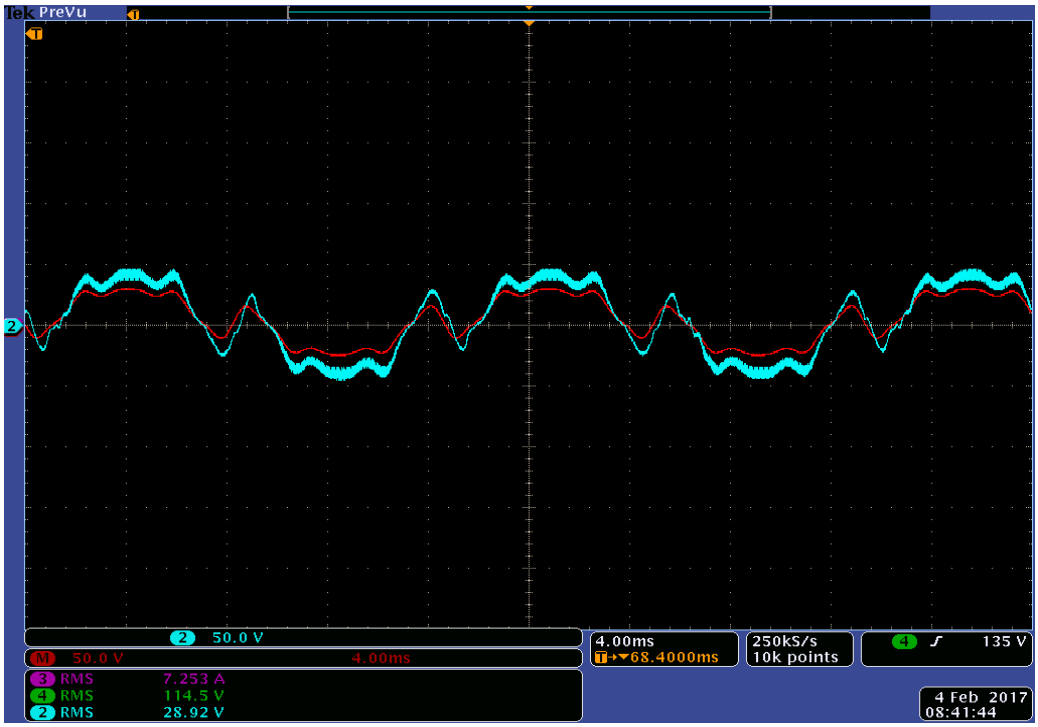


Figure 7.80: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario XII

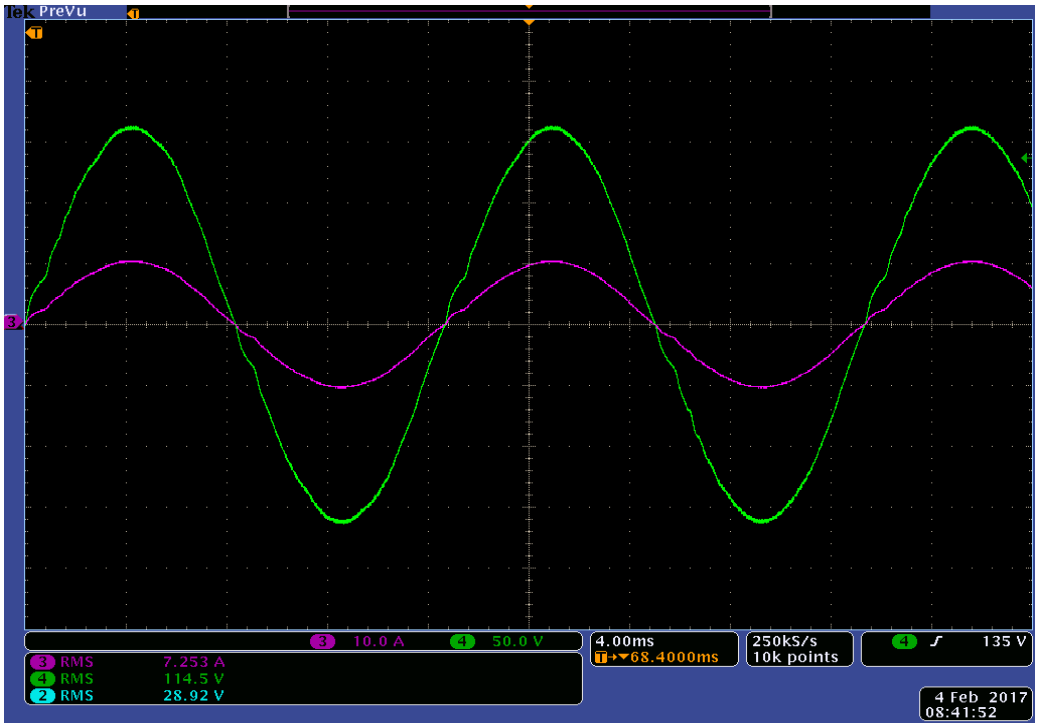


Figure 7.81: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario XII

The load voltage is restored to 113 V RMS with 2.26% THD from source voltage of 97.3 V RMS with 13.31% THD. The load voltage is not completely restored to 120 V RMS due to the losses occurring in the system. It can be noted that AC-DVR operates in similar manner discussed in section 6.3.9 and experimental results presented in this section closely resemble to the simulation results presented in section 6.3.9 for same operating scenario of combined voltage sag and harmonic distortion.

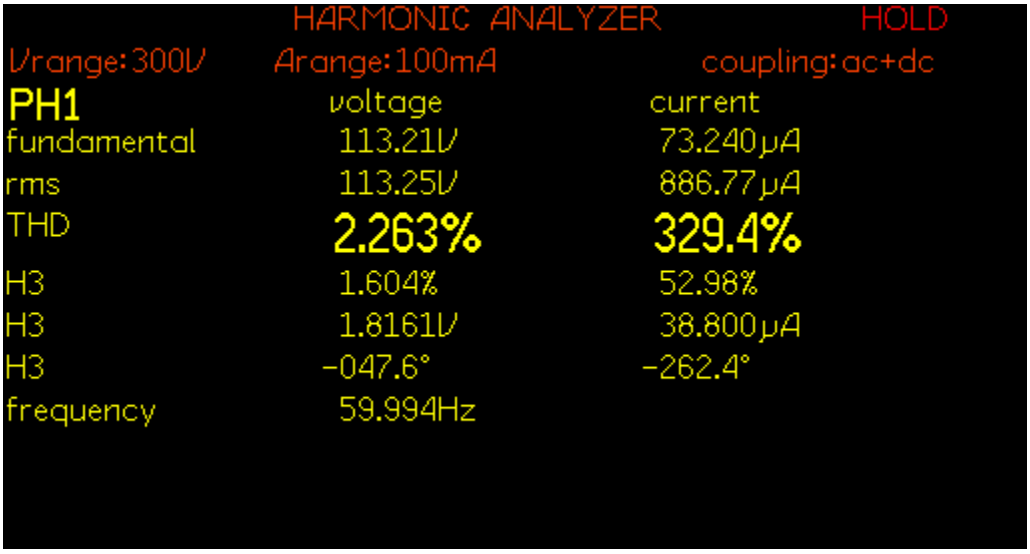


Figure 7.82: THD of load voltage V_{Load} for experiment scenario XII

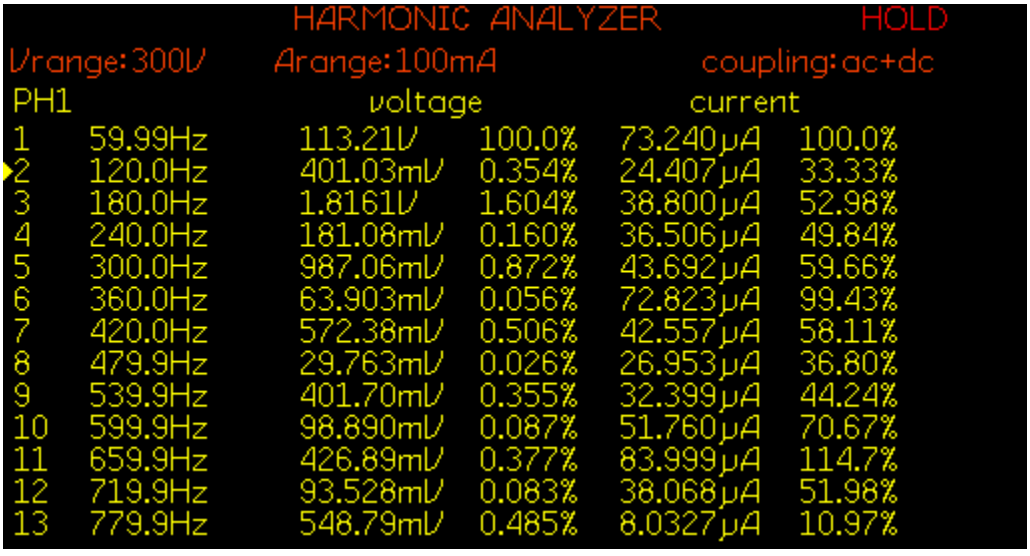


Figure 7.83: FFT of load voltage V_{Load} for experiment scenario XII

7.3.10 UNC Charlotte service voltage: Experiment scenario XIII

This experiment was performed with UNC Charlotte's voltage available at wall outlet. The source voltage and load voltage reference are presented in Figure 7.84.

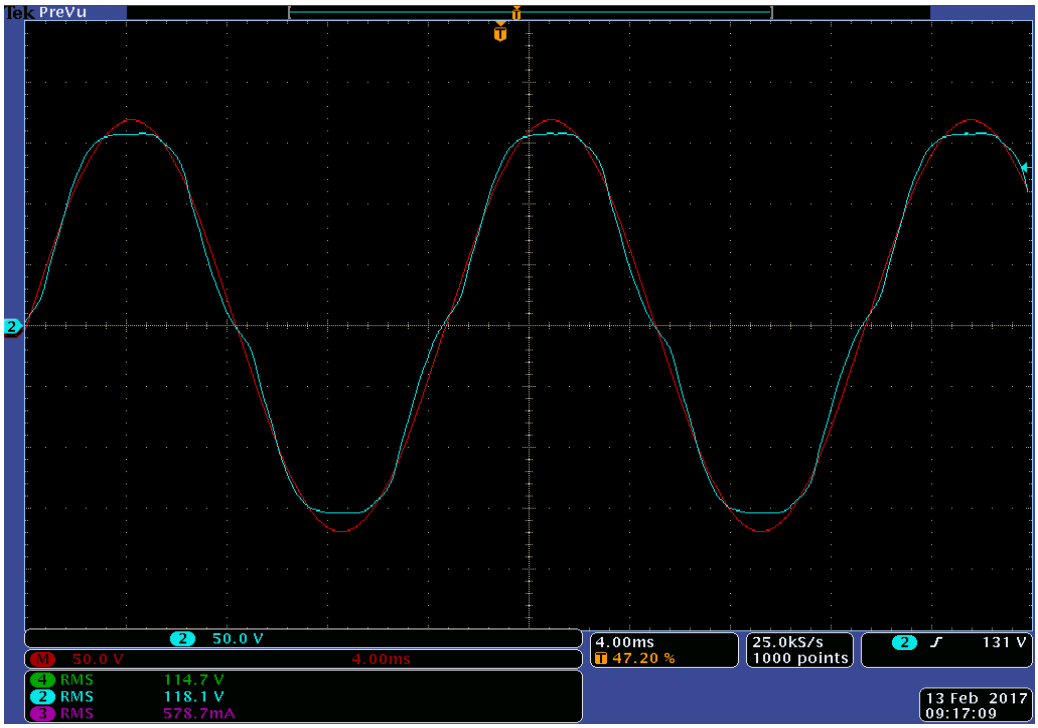


Figure 7.84: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario XIII

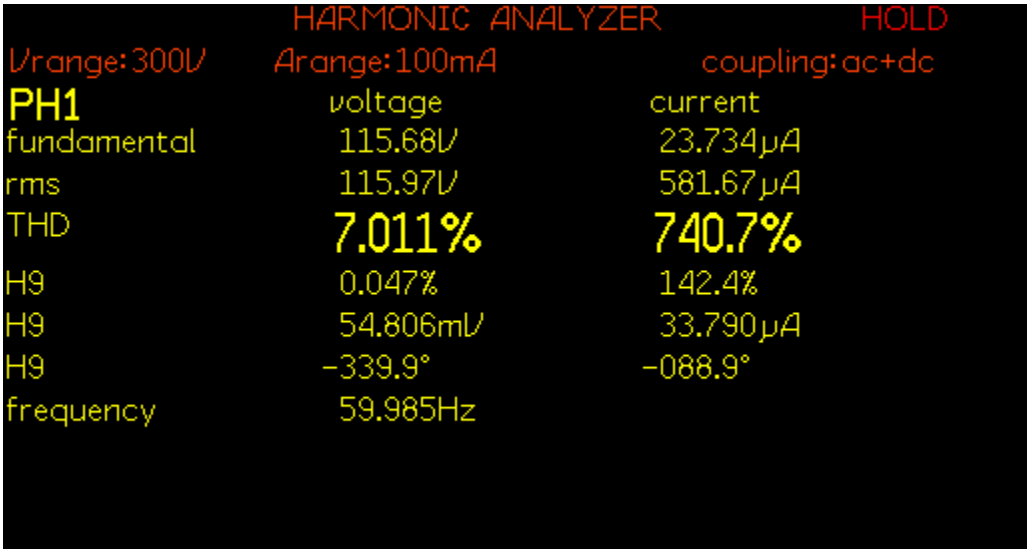


Figure 7.85: THD of source voltage V_{in} for experiment scenario XIII

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.85, 7.86, 7.87, 7.88,7.89, 7.90 and 7.91 respectively.

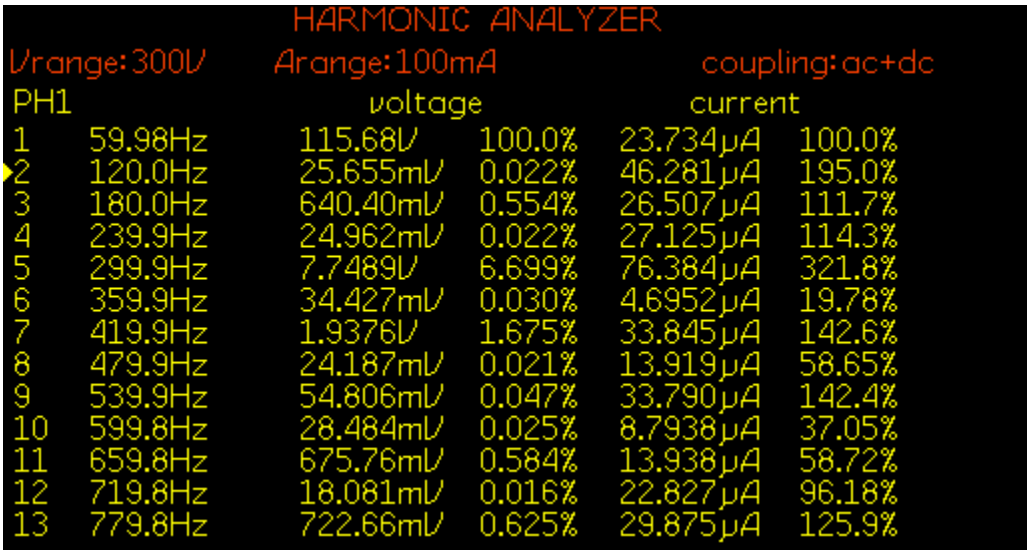


Figure 7.86: FFT of source voltage V_{in} for experiment scenario XIII

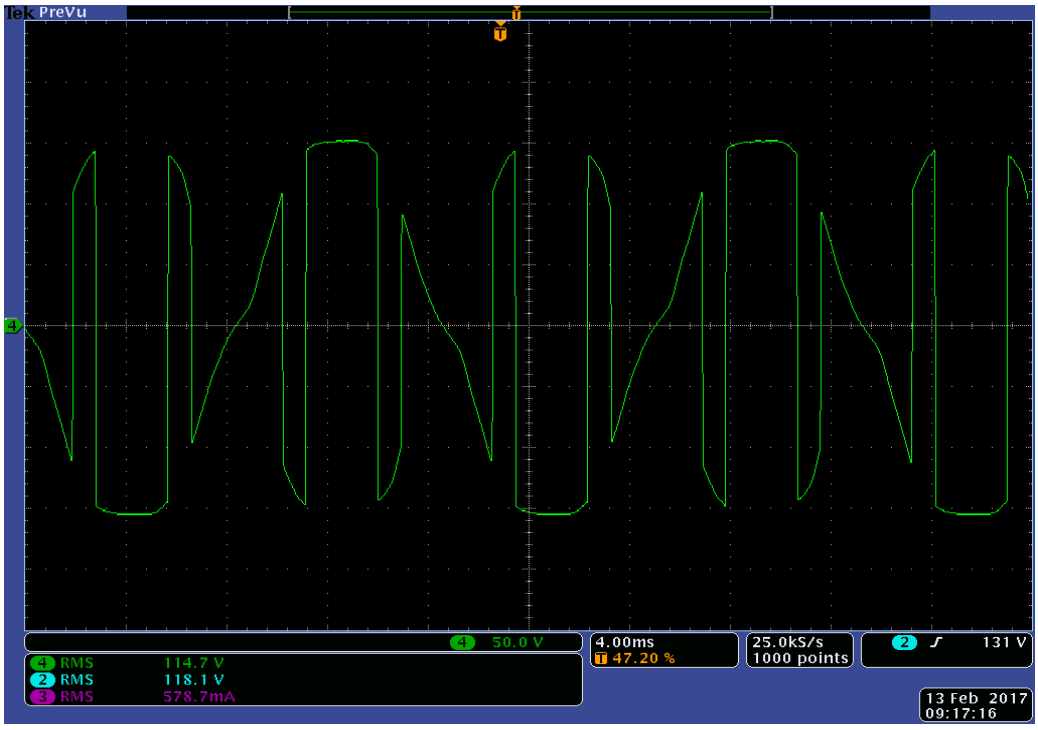


Figure 7.87: Experimental results of Bridge output voltage V_o for experiment scenario XIII

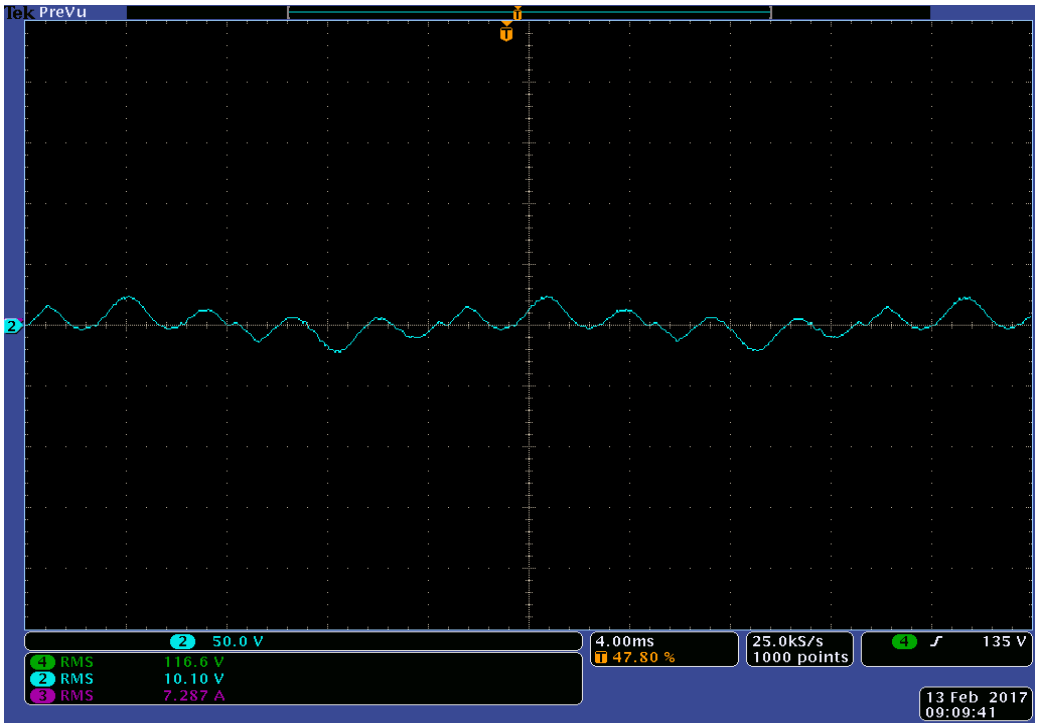


Figure 7.88: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario XIII

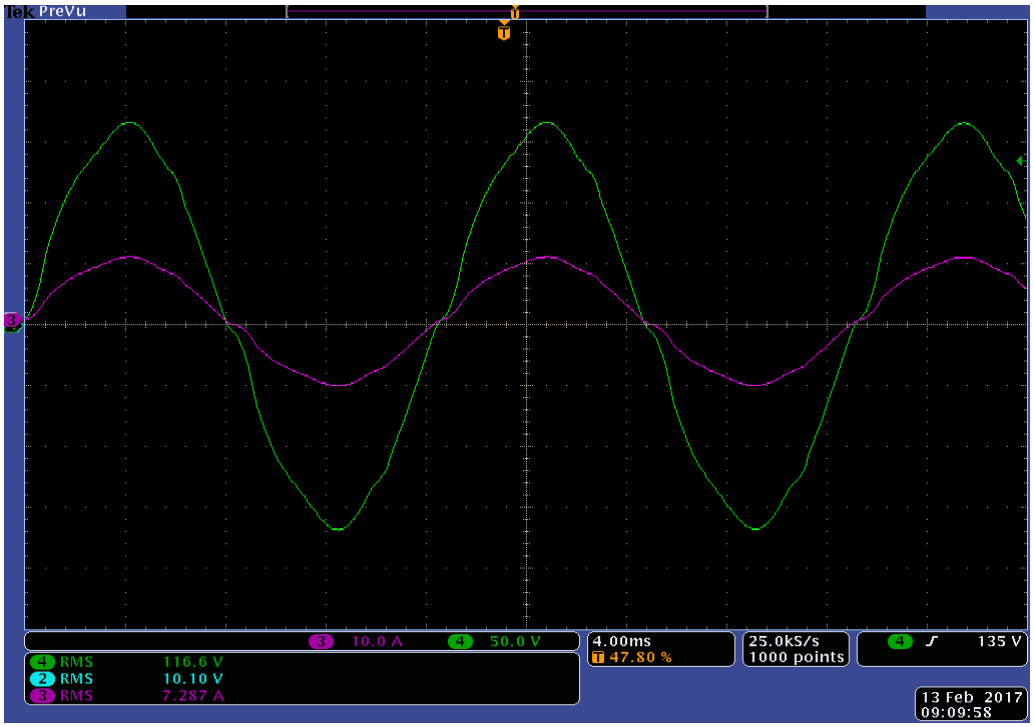


Figure 7.89: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario XIII

The load voltage is restored to 119 V RMS with 3.24% THD from source voltage of 115 V RMS with 7.01% THD. The load voltage is not completely restored to 120 V RMS due to the losses occurring in the system. It can be noted that AC-DVR operates in similar manner discussed in section 6.3.10 and experimental results presented in this section closely resemble to the simulation results presented in section 6.3.10 for same operating scenario of UNC Charlotte's voltage available at wall outlets.

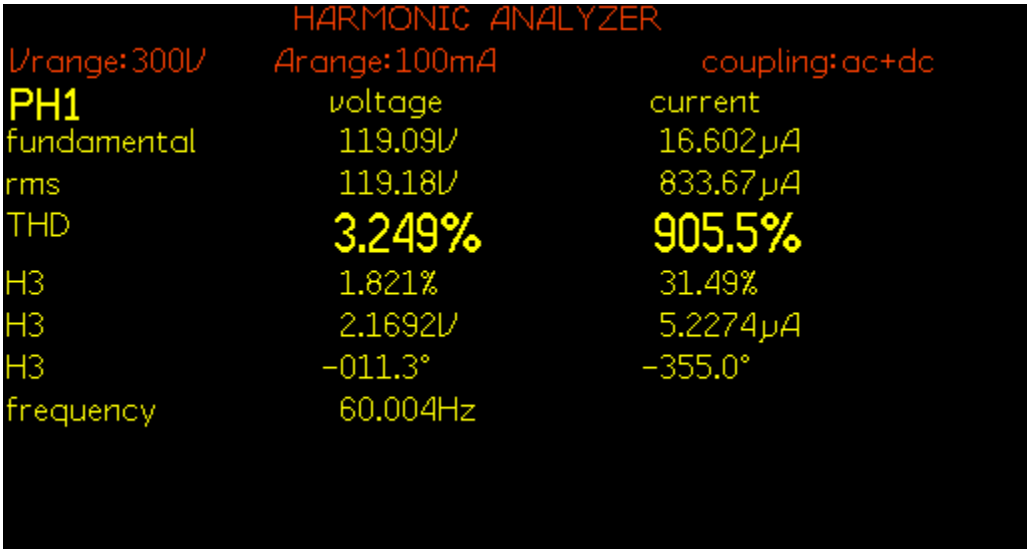


Figure 7.90: THD of load voltage V_{Load} for experiment scenario XIII

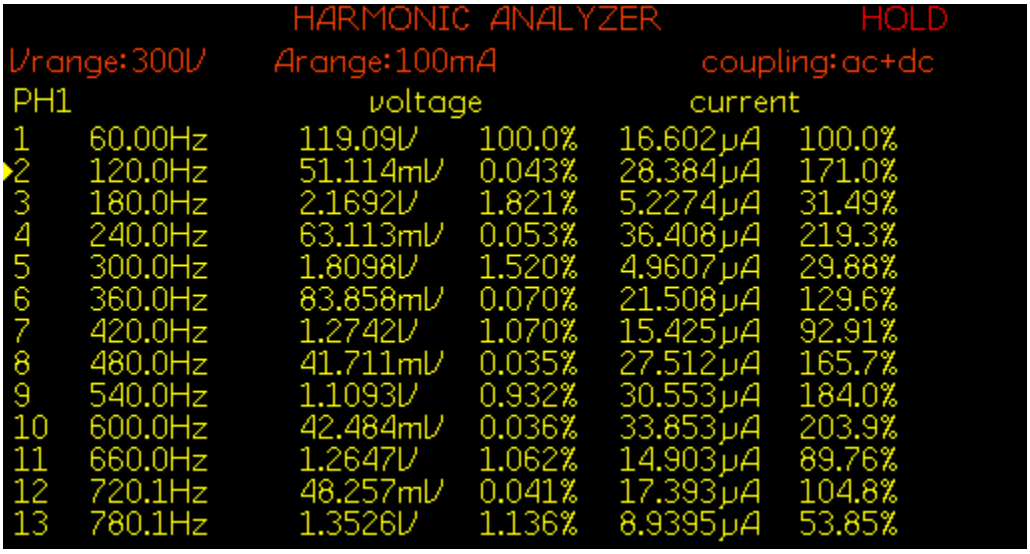


Figure 7.91: FFT of load voltage V_{Load} for experiment scenario XIII

7.3.11 Step change in load under normal conditions: Experiment scenario XIV

In this experiment, load is changed from 0.6 kW to 0.9 kW under nominal grid condition. The source voltage and load voltage reference are presented in Figure 7.92.

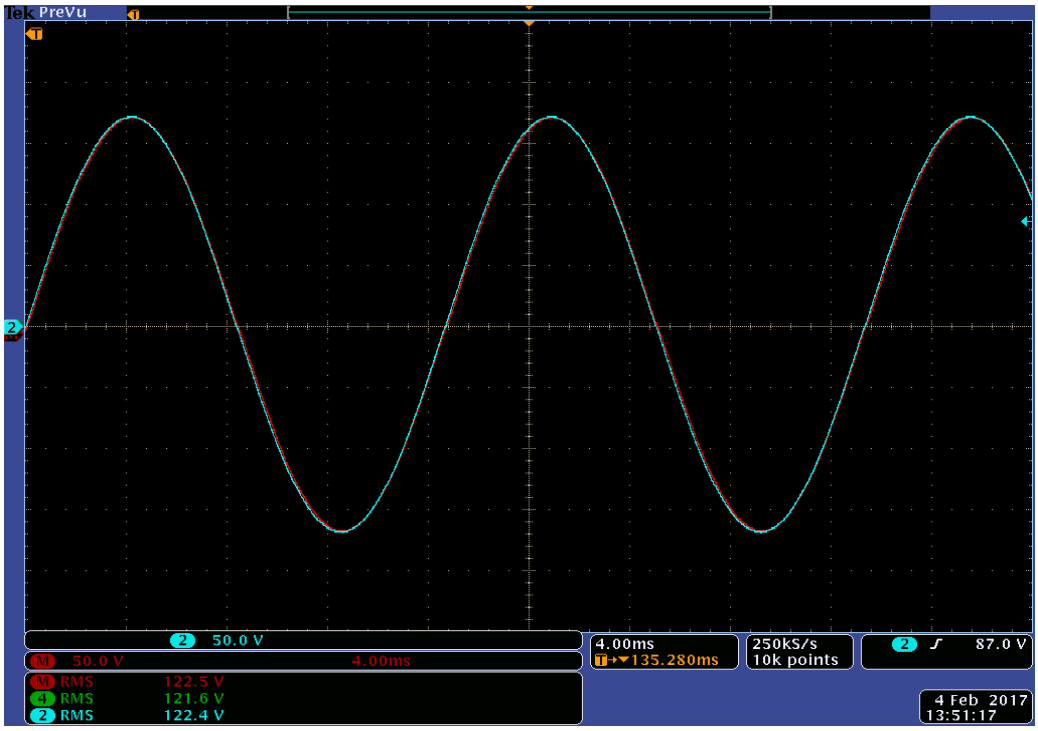


Figure 7.92: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario XIV

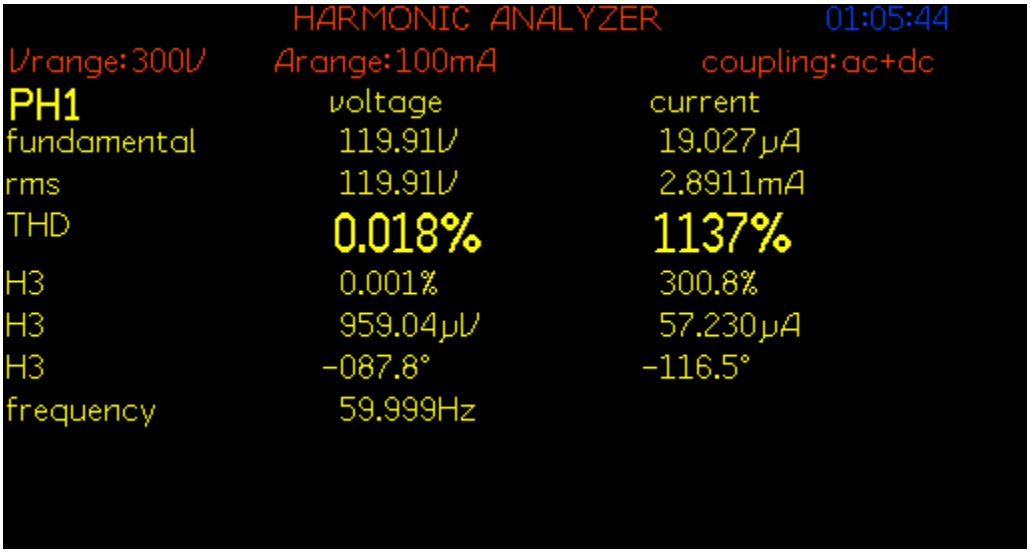


Figure 7.93: THD of source voltage V_{in} for experiment scenario XIV

Source voltage THD, source voltage FFT, bidirectional bridge output voltage, AC-DVR voltage and reference; load voltage and current; load voltage THD and load voltage FFT are depicted in Figures 7.93, 7.94, 7.95, 7.96,7.97, 7.98 and 7.99 respectively.

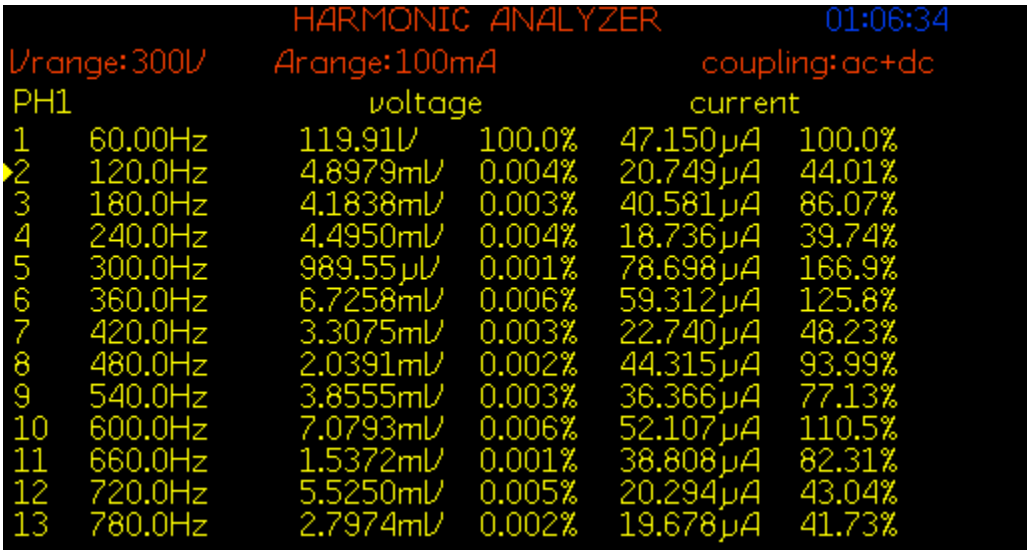


Figure 7.94: FFT of source voltage V_{in} for experiment scenario XIV

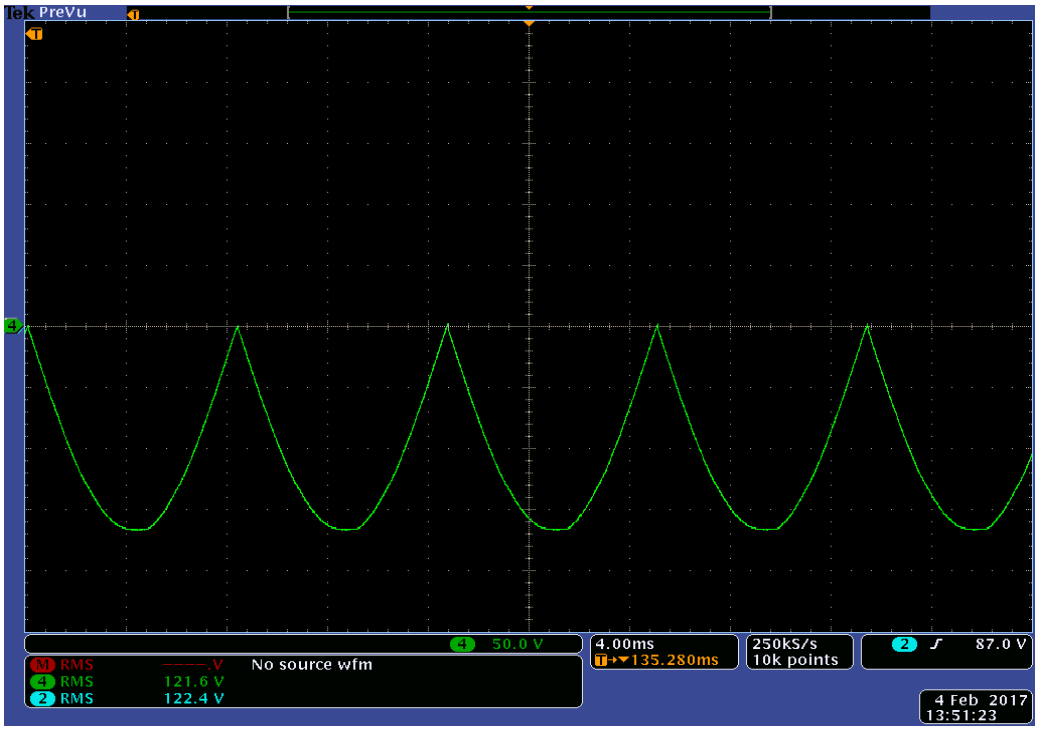


Figure 7.95: Experimental results of Bridge output voltage V_o for experiment scenario XIV

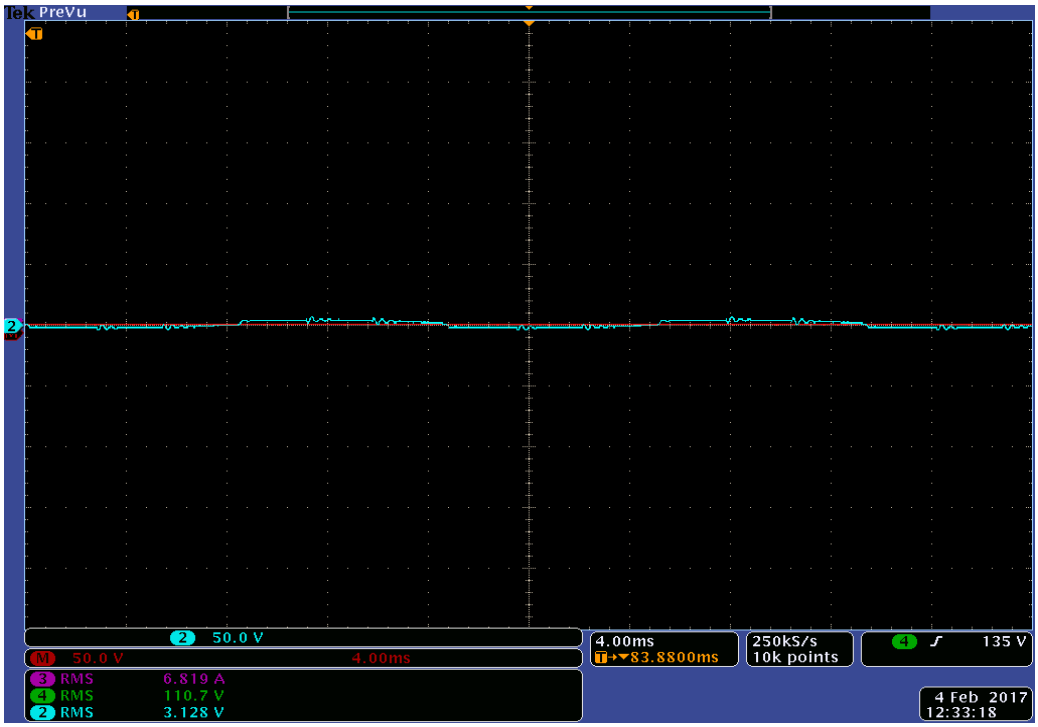


Figure 7.96: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario XIV

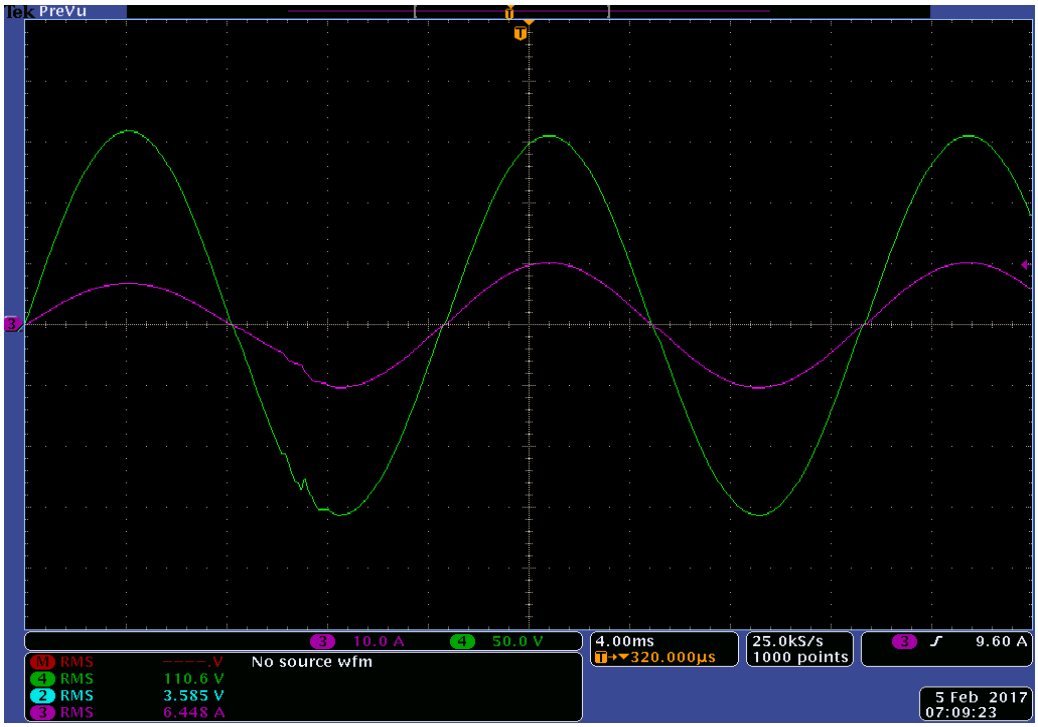


Figure 7.97: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario XIV

The load voltage is measured to be 109 V RMS with 0.744% THD. The magnitude of load voltage is not exactly equal to the input because of the losses occurring in the system. Although, as it can be seen that experimental results closely resemble with simulation results presented in section 6.3.11. The AC-DVR operates in similar way as discussed in section 6.3.11 in chapter 6. The only difference is that load is changed to 0.9 kW from 0.6 kW unlike simulation were load change was 1 kW to 1.5 kW.

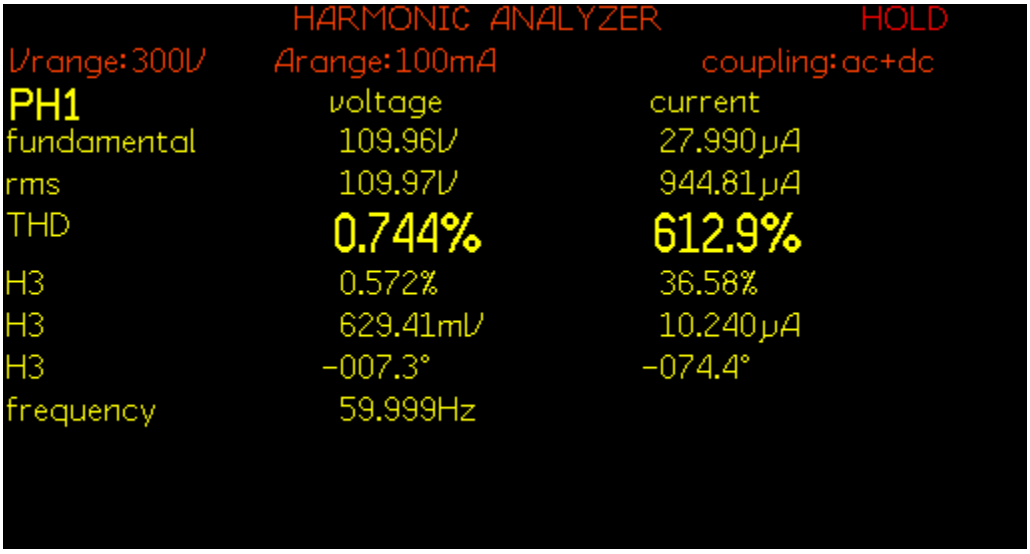


Figure 7.98: THD of load voltage V_{Load} for experiment scenario XIV

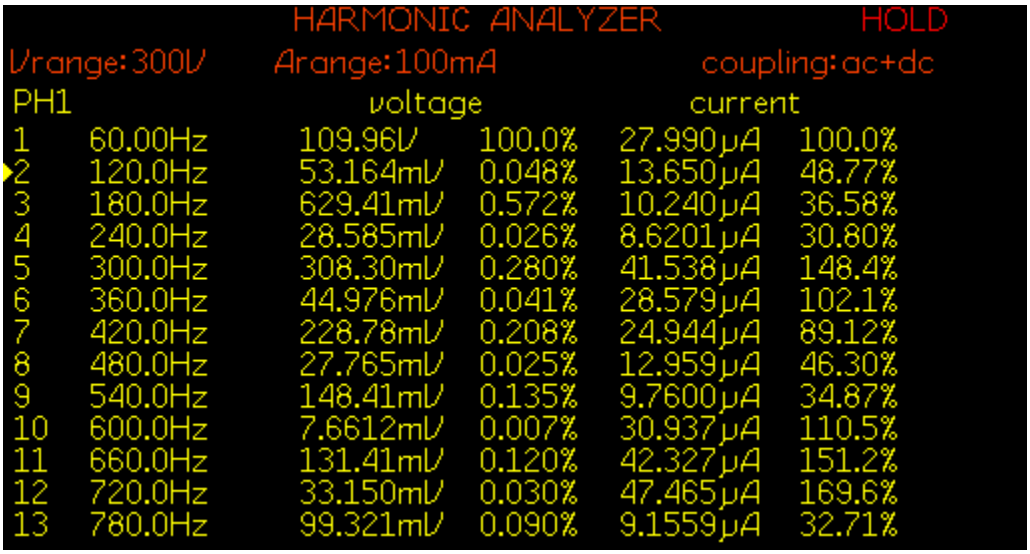


Figure 7.99: FFT of load voltage V_{Load} for experiment scenario XIV

7.3.12 Step change in harmonic distortion: Operating scenario XVII

In this experiment, disturbance was changed from third harmonic to 5th harmonic. The source voltage and load voltage reference are presented in Figure 7.100.

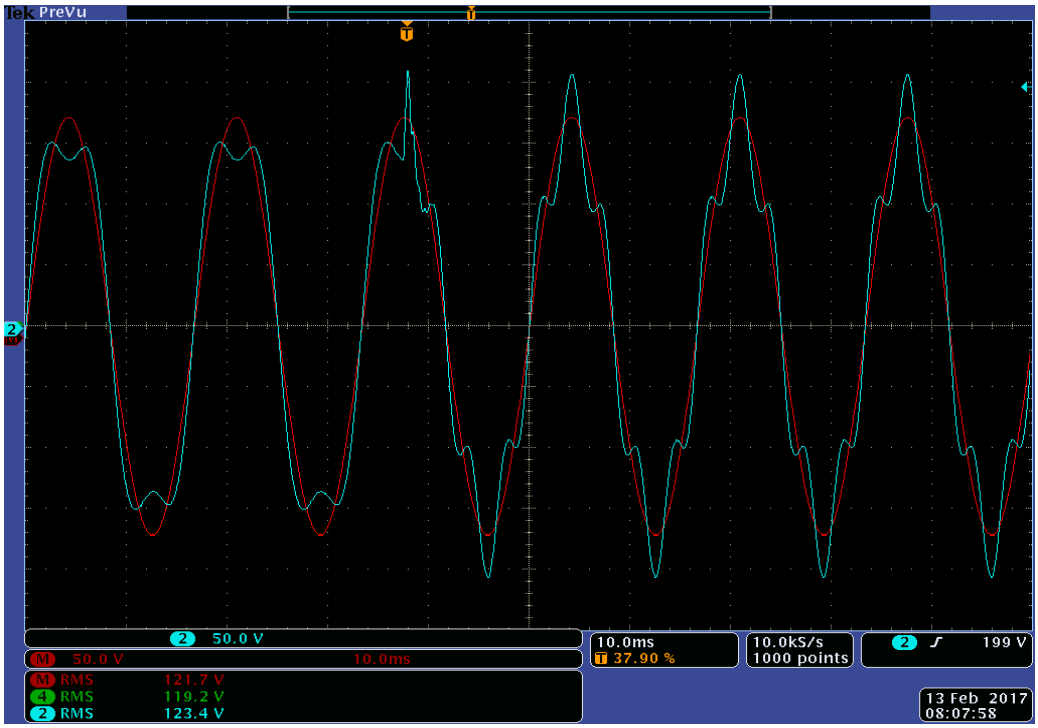


Figure 7.100: Experimental results of Source voltage V_{in} (Blue) and load reference voltage $V_{Ref-Load}$ (Red) for experiment scenario XVII

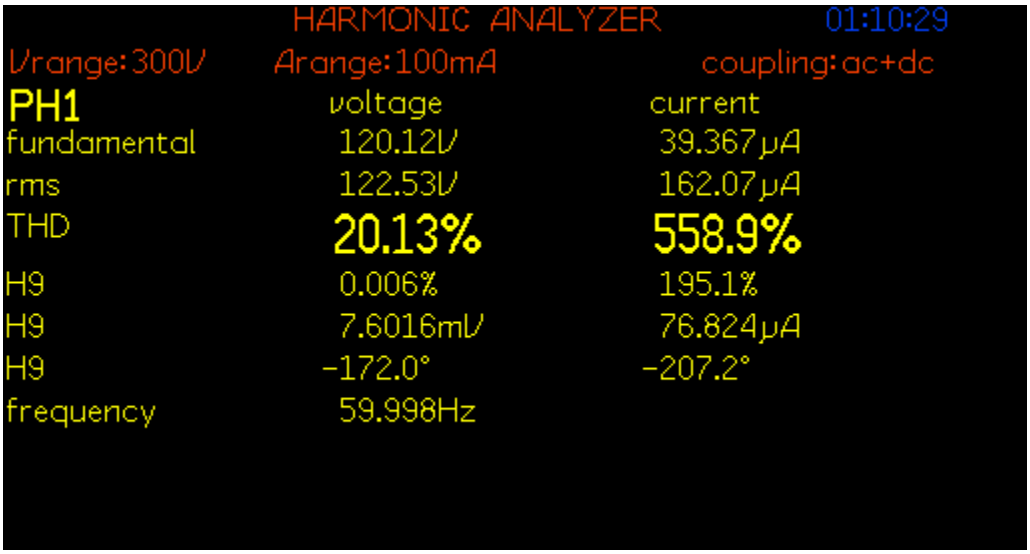


Figure 7.101: THD-3rd of source voltage V_{in} for experiment scenario XVII

Source voltage THD and FFT for third harmonic voltage and fifth harmonic voltage are depicted in Figures 7.101, 7.102, 7.103, 7.104 respectively. The source was experiencing third harmonic distortion before and a step change of fifth harmonic voltage was introduced to verify the response of proposed control architecture. The bidirectional bridge output voltage and voltage synthesized by AC-DVR are depicted in Figure 7.105 and 7.106 respectively.

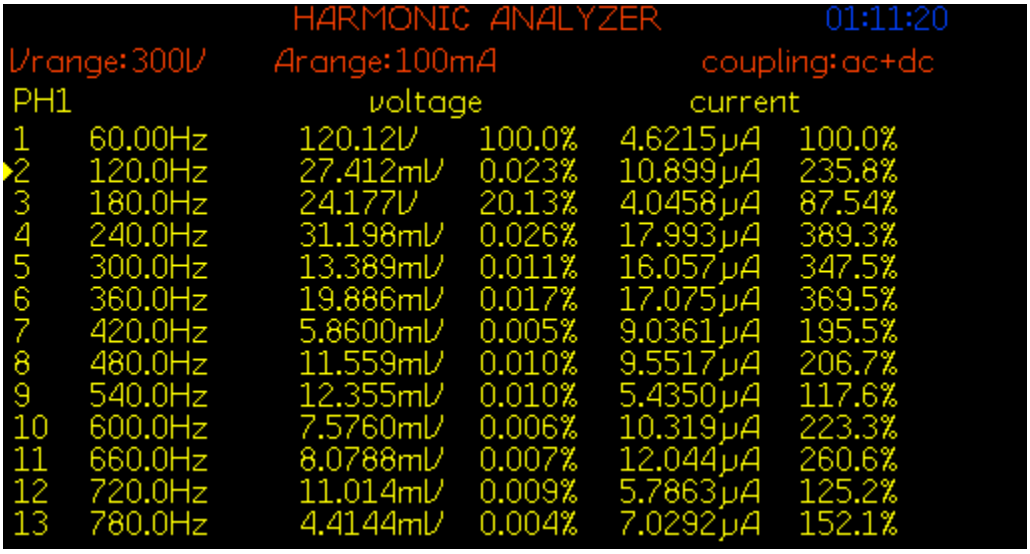


Figure 7.102: FFT-3rd of source voltage V_{in} for experiment scenario XVII

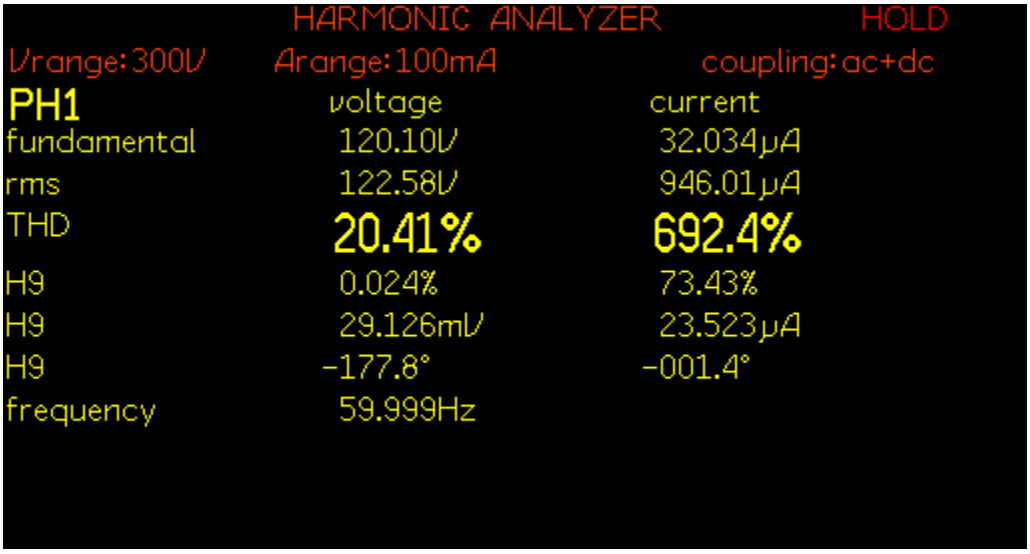


Figure 7.103: THD-5th of source voltage V_{in} for experiment scenario XVII

Whereas, load voltage and load current are depicted in Figure 7.107. The THD and FFT of load voltage for before disturbance change and after disturbance change are presented in Figure 7.108, 7.109, 7.110 and 7.111.

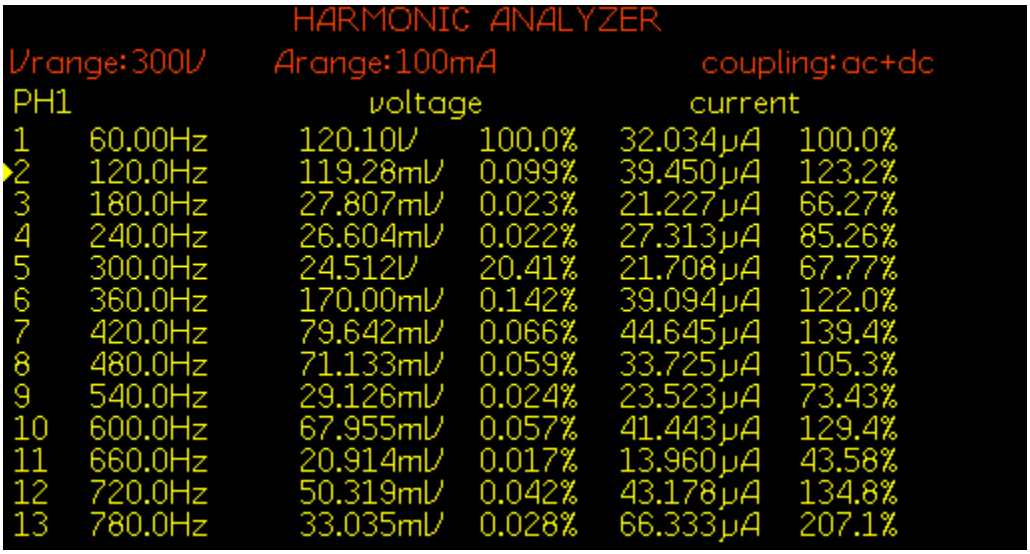


Figure 7.104: FFT-5th of source voltage V_{in} for experiment scenario XVII

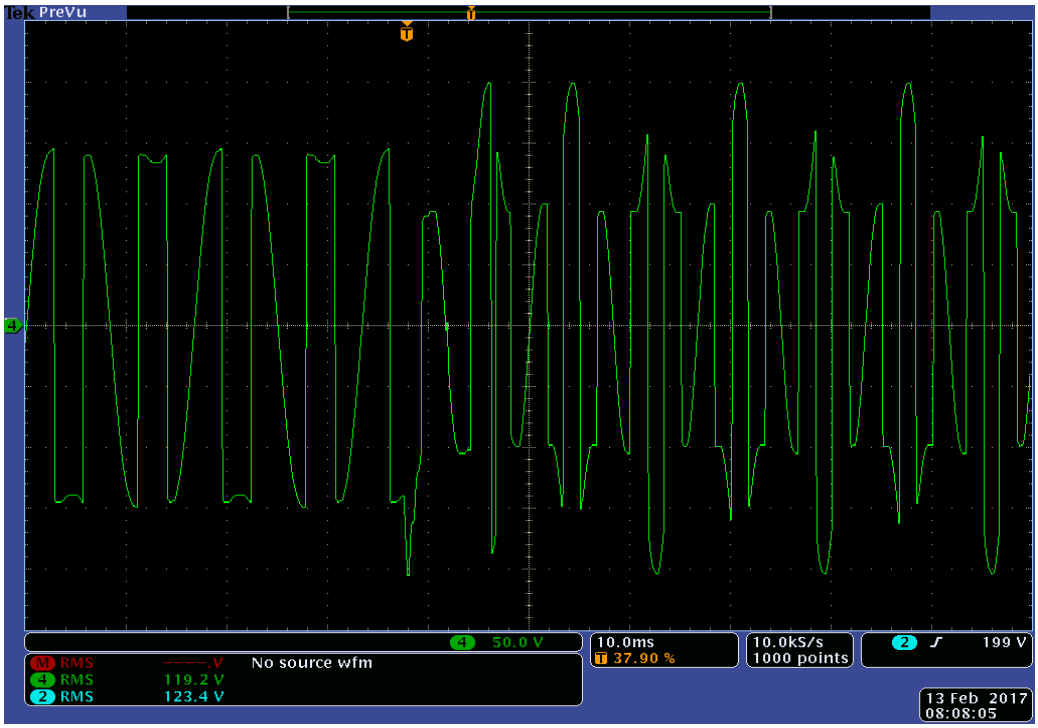


Figure 7.105: Experimental results of Bridge output voltage V_o for experiment scenario XVI

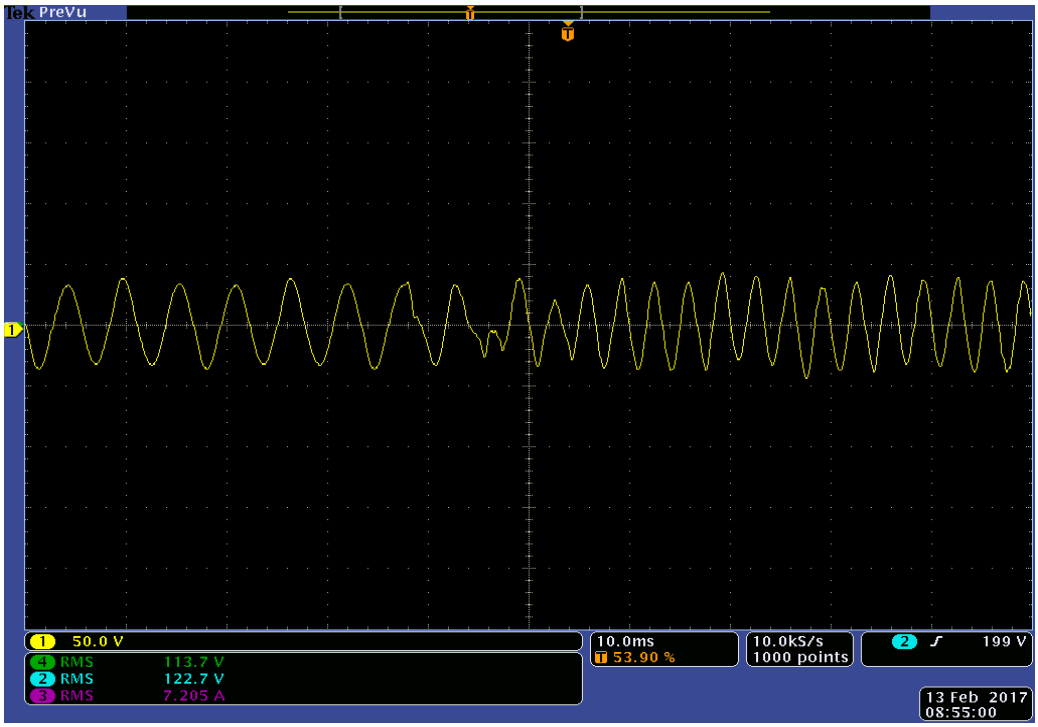


Figure 7.106: Experimental results of AC-DVR voltage V_{AC-DVR} (Blue) and DVR reference voltage $V_{Ref-DVR}$ (Red) for experiment scenario XVII

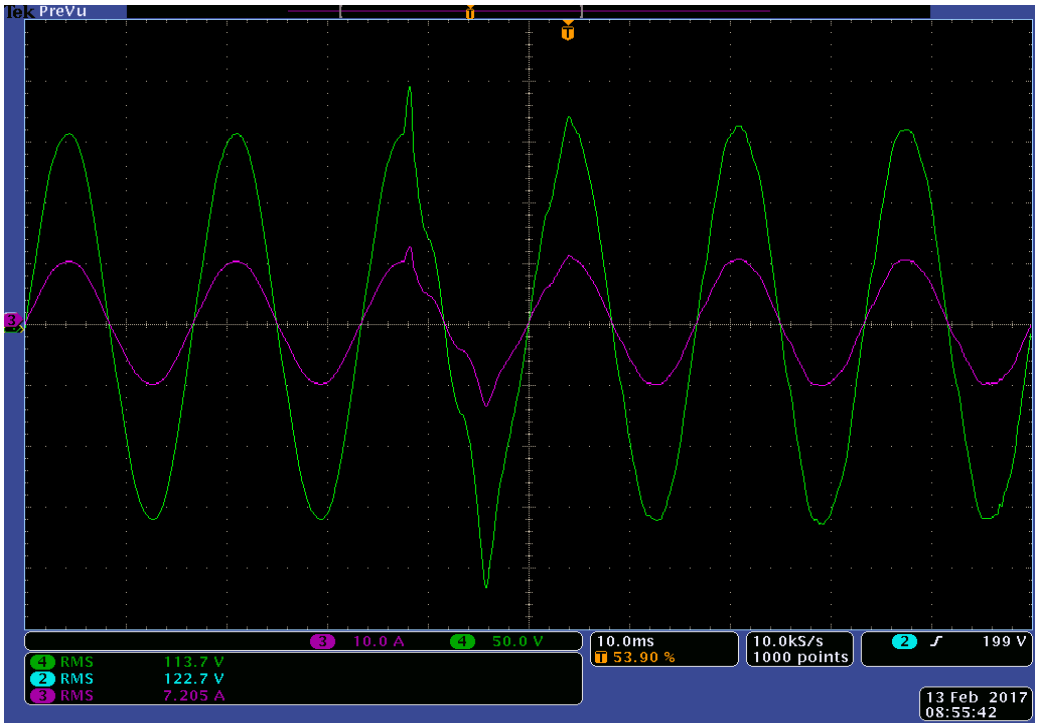


Figure 7.107: Experimental Results of Load voltage V_{Load} (Green) and load current I_{Load} (Pink) for experiment scenario XVII

It can be seen from Figure 7.107 that it takes at least one fundamental cycle for AC-DVR to calculate fifth harmonic compensation voltage after the step change of fifth harmonic disturbance is introduced. A closed loop control or feedback loop control for load voltage can be implemented for better dynamic response and superior load voltage compensation.

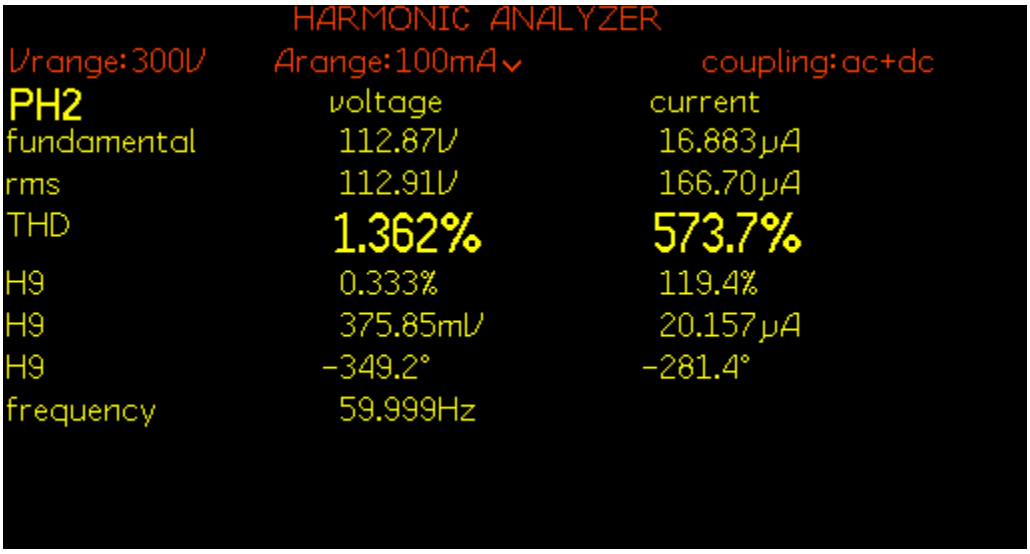


Figure 7.108: THD-3rd of load voltage V_{Load} for experiment scenario XVII

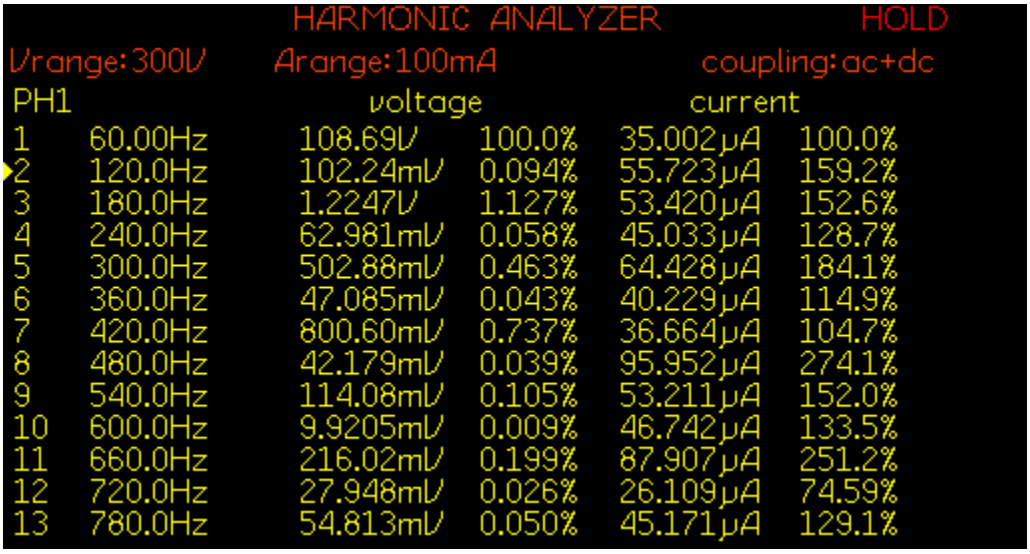


Figure 7.109: FFT-3rd of load voltage V_{Load} for experiment scenario XVII

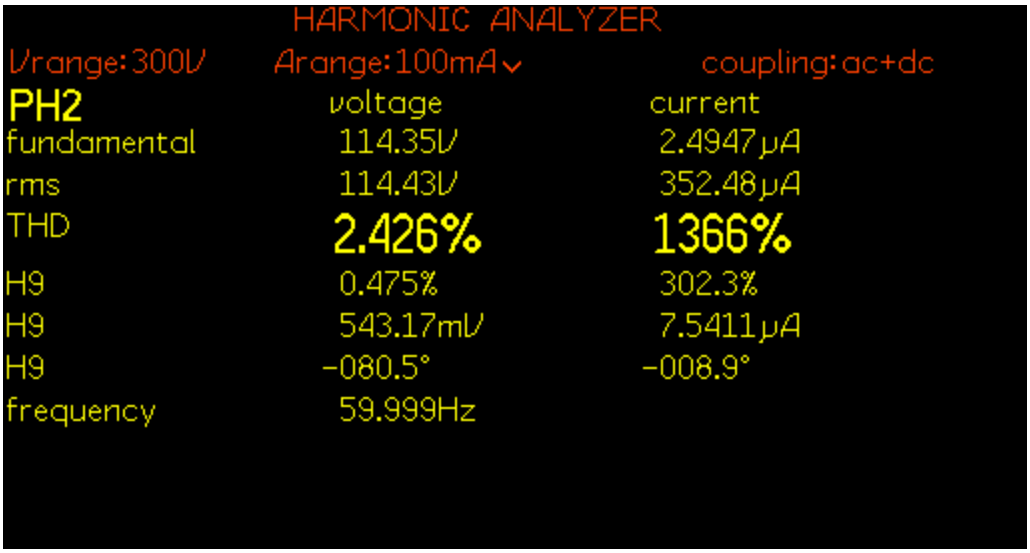


Figure 7.110: THD-5th of load voltage V_{Load} for experiment scenario XVII

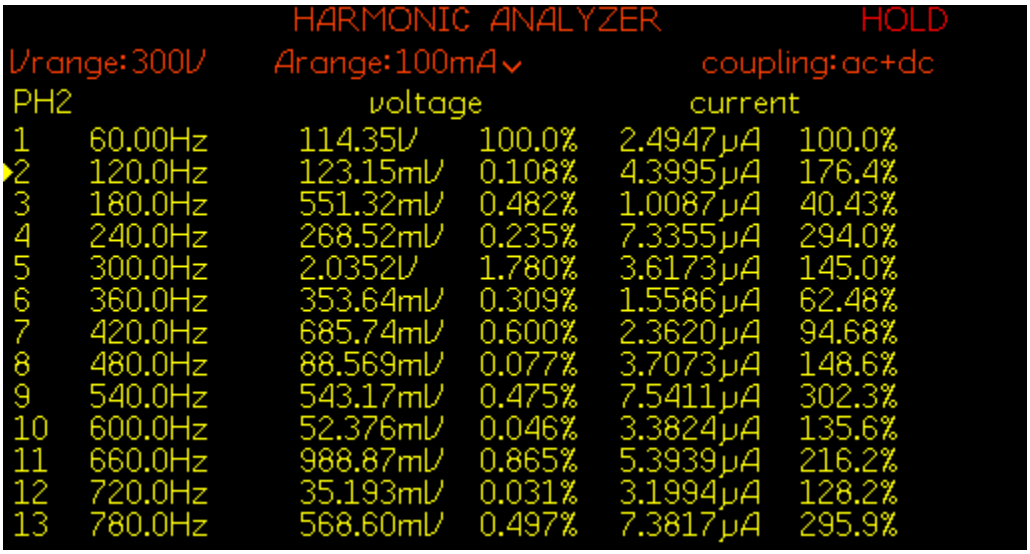


Figure 7.111: FFT-5th of load voltage V_{Load} for experiment scenario XVII

CHAPTER 8: CONCLUSION & FUTURE WORK

8.1 Overview

A novel methodology to synthesize voltage at fundamental frequency or at harmonic frequency from fundamental frequency voltage is proposed in this article. Direct AC-AC Dynamic Voltage Regulator and its efficacy is shown via simulation and experimental results as an application of such methodology. This alternative method of voltage regulation offers smaller size, lower cost and enhanced performance capability due to the lack of bulky energy storage systems, capacitors and intermediate power stages in comparison with conventional Dynamic Voltage Regulators. The following are the important observations drawn from the simulation and experimental results:

- Proposed direct AC-AC DVR can be a good choice for the replacement of existing conventional DVR systems
- THD of load voltage is maintained below 5% for most of the operating conditions
- The output voltage THD and magnitude can be further refined by using feedback loop control
- The capability of AC-DVR to synthesize compensation voltage with disturbed shape is highly dependent on switching frequency

8.2 Recommendations and Future Work

The efficacy of the proposed methodology is verified via experimental set up. It can be seen from the results that due to losses occurring in the converter, load voltage is not being held at its reference value. Moreover, AC-DVR synthesizes harmonic frequency voltage for harmonic compensation while providing different shape of current. Thus, voltage drop occurring due the odd shape of current, affects the voltage synthesized by AC-DVR which in turn affects the THD level of load voltage. In consideration of these challenges, future work includes but not limited to:

- Optimized design of inductor L and capacitor C
- Close loop control of proposed converter for loss compensation
- Dynamic and transient analysis
- Converter characteristics and analysis for higher switching frequency operation
- Efficiency and cost analysis

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APPENDIX A: MODIFICATION IN PROPOSED AC-DVR

A.1 Introduction

The circuit architecture, working principle, circuit analysis, simulation results and experimental results for proposed AC-DVR have been discussed and presented in previous chapters of this article. This appendix presents a possible modification in proposed AC-DVR along with circuit architecture and simulation results.

A.2 Possible Modification of AC-DVR

The use of DC storage and series injection transformer is two major drawbacks of conventional DVR systems. The proposed AC-DVR system discussed in previous sections eliminates the need of DC storage device. However, it still uses a fundamental frequency series transformer for isolation and injection of compensation voltage which can be large and heavy. This disadvantage can be eliminated by suitable modification in proposed AC-DVR. The concept is to use a high frequency isolation transformer instead of fundamental frequency transformer which can be smaller, compact and less bulky in comparison of fundamental frequency transformer.

The proposed modification uses flyback buck boost converter as a replacement of buck boost converter. The operating principle of flyback converter is well known and it serves the same purpose as buck boost converter. The advantage of using flyback is that by introducing one more winding in the flyback transformer, it can also work as a replacement of bidirectional bridge used in previously proposed AC-DVR. The detailed schematic of the possible modification is shown in Figure 3.6. It consists of three high frequency bidirectional switches (S1S2, S2S3 and S4S5), a flyback transformer and a capacitor. The flyback transformer has two primary windings/inductors to change the

phase of input voltage and one secondary winding/inductor to discharge the primary inductors. The requirement of in phase and out of phase voltage is taken care by the switching of S1S2 and S3S4. The switches S1S2 and S3S4 switches in duty cycle D and ensures the in phase or out of phase voltage requirement by switching L1 or L2. When the input voltage is positive, either switch S1 charges the winding/inductor L1 or S3 charges winding/inductor L2 to provide positive and negative voltage respectively. Similarly, when input is negative, either switch S2 charges L1 or S4 charges L2 to provide negative and positive voltage respectively. Both L1 or L2 are discharged through winding/inductor L3 and capacitor C by switching of S5S6 in duty cycle D'.

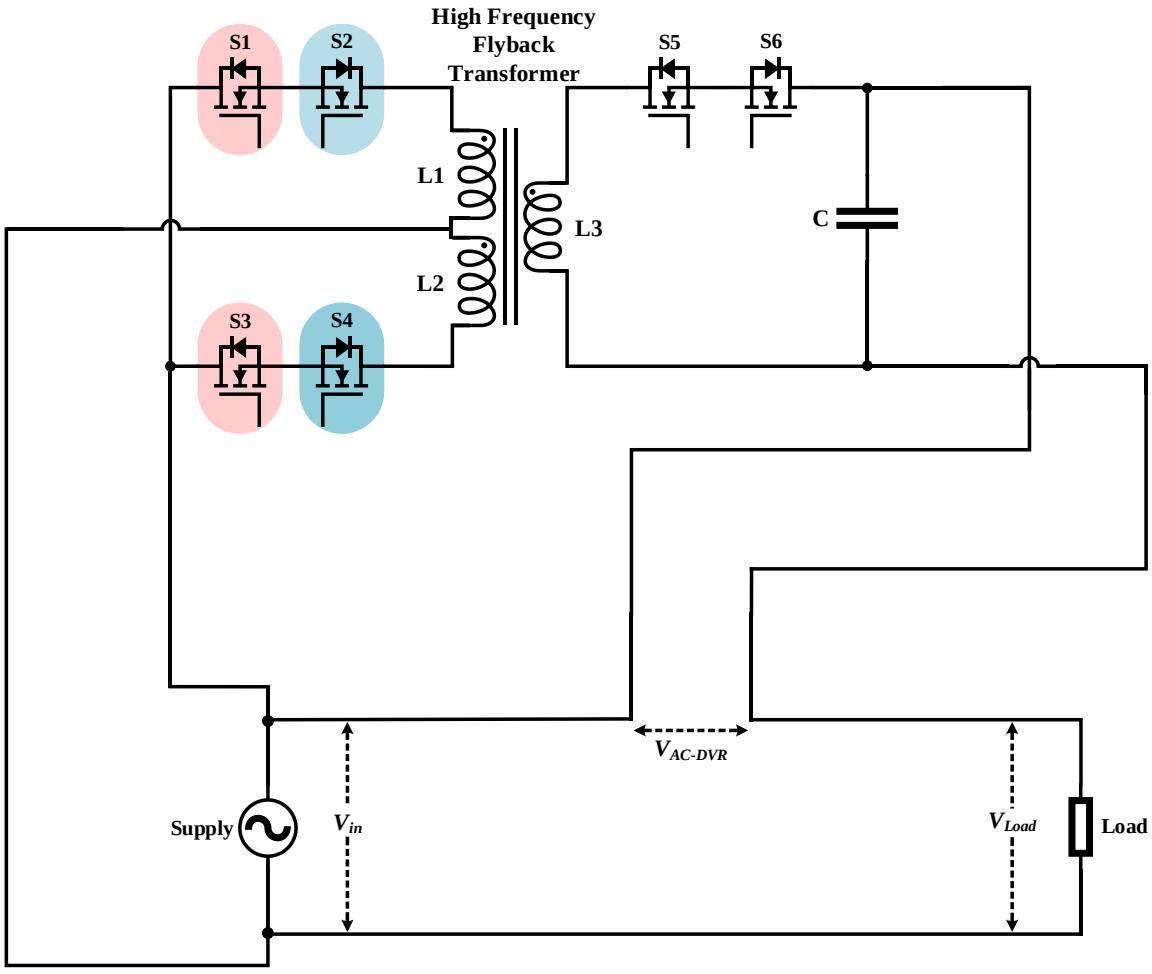

Figure A.1 Possible modifications in proposed AC-DVR

The use of flyback converter eliminates the use of two discrete converters used in previously discussed AC-DVR as both wave shaping and unfolding can be achieved by using three bidirectional switches and one flyback transformer. The number of bidirectional switches are also reduced in case of flyback based AC-DVR system. Thus, by using flyback based AC-DVR, the AC-DVRs can be made smaller, more effective and faster than conventional DC DVR systems.

The proposed modified AC-DVR is simulated for similar operating scenarios as performed before for previously discussed AC-DVR topology. The simulation parameters for modified AC-DVR, operating scenarios and simulation results are presented and discussed in brief in following sections.

Simulation Parameters

The system is simulated on MATLAB/Simulink platform under the parameters tabulated in Table A.1. The grid and transformer are considered ideal for the simulation purpose. The simulations have been performed under various voltage and load scenarios to validate the working principle of modified AC-DVR. These scenarios were created by changing some of the simulation parameters of Table A.1. The changes in parameters are mentioned for each simulation scenario in next section while the other parameters remain unchanged.

Table A.1 Simulation parameters for modified AC-DVR

Model	Parameters
Source/Grid	120 V (RMS), 60 Hz
Load	14.4 Ω and 9.6 Ω (1kW and 1.5 kW)
Flyback transformer	1 kVA, 20 kHz
Inductors $L1, L2, L3$	250 µH
Capacitor C	15 µF
Switching frequency f_{sw}	20 kHz

A.3 Simulation Results of Modified AC-DVR

The key area of focus is maintaining the THD and magnitude of load voltage within permissible limits by adding or subtracting needed voltage through AC-DVR when any disturbance occurs in source voltage. Thus, simulations for seventeen various source voltage distortion scenarios such as individual harmonic voltage distortion, combined harmonic voltage distortion, voltage sag, voltage swell and combined harmonic voltage and voltage sag distortion have been performed to validate the performance and capability of AC-DVR to maintain the load voltage. Moreover, to understand the dynamic response of the AC-DVR, simulations have been carried out for step change in load and disturbance type. The parameters for each operating scenario are tabulated in Table A.2. The simulated waveforms for some selected scenarios are presented and discussed in following subsections. The behavior of AC-DVR under normal conditions, individual harmonic distortion (3^{rd}, 5^{th}, 11^{th}) and combined harmonic distortion (3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th} and 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th}, 13^{th}) are provided in subsections A.3.1-A.3.6 respectively. Likewise, simulations under voltage sag, voltage swell and combined harmonic and sag (3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th} and sag) type of disturbances are discussed in subsections A.3.7-A.3.9 respectively. Whereas, scenarios consisting of step load change under normal conditions and combined harmonic and sag (3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th} and sag) conditions are discussed in A.3.10 and A.3.11 to determine the dynamic behavior of AC-DVR under step load change. Similarly, step change in harmonic and swell type of disturbance is considered for scenarios discussed in A.3.12 and A.3.13. To determine the performance of AC-DVR under usual harmonic type disturbances, simulations under service voltage at UNC Charlotte have been performed and results are provided inA.3.14.

Table A.2: Summary of various operating scenarios and simulation results for modified AC-DVR

Scenario No.	Time (t) a=0, b=0.0208, c=0.05	Input Voltage RMS (V)	Fundamental Voltage RMS (V)	Harmonic Order (n) and magnitude as percentage of fundamental (%)						Input Voltage THD (%)	Load (W)	Output Voltage RMS (V)	Output Voltage THD (%)
				3	5	7	9	11	13				
i	$a \leq t \leq c$	120	120	-	-	-	-	-	-	0	1000	120	0
ii	$a \leq t \leq c$	126.5	120	33.33	-	-	-	-	-	33.33	1000	119.9	2.03
iii	$a \leq t \leq c$	122.4	120	-	20	-	-	-	-	20	1000	119.9	1.41
iv	$a \leq t \leq c$	121.2	120	-	-	14.29	-	-	-	14.29	1000	120	1.13
v	$a \leq t \leq c$	120.7	120	-	-	-	11.11	-	-	11.11	1000	120	1
vi	$a \leq t \leq c$	120.5	120	-	-	-	-	9.09	-	9.09	1000	120	0.93
vii	$a \leq t \leq c$	120.4	120	-	-	-	-	-	7.69	7.69	1000	120	0.94
viii	$a \leq t \leq c$	121.1	120	8	9	5	-	2	2	13.34	1000	120	0.92
ix	$a \leq t \leq c$	131.3	120	33.33	20.01	14.29	11.11	9.09	7.69	44.5	1000	119.9	3.26
x	$a \leq t \leq c$	84	84	-	-	-	-	-	-	0	1000	119.2	2.16
xi	$a \leq t \leq c$	156	156	-	-	-	-	-	-	0	1000	120.6	1.76
xii	$a \leq t \leq c$	97.33	96	10	11	6.25	-	2.5	2.5	16.68	1000	119.5	1.83
xiii	$a \leq t \leq c$	116.1	115.9	1.78	3.36	1.6	0.19	2.52	1.43	5.12	1000	119.9	0.74
xiv	$a \leq t \leq b$	120	120	-	-	-	-	-	-	0	1000	120	0
	$b \leq t \leq c$	120	120	-	-	-	-	-	-	0	1500	120	0
xv	$a \leq t \leq b$	97.33	96	10	11	6.25	-	2.5	2.5	16.68	1000	119.5	1.83
	$b \leq t \leq c$	97.33	96	10	11	6.25	-	2.5	2.5	16.68	1500	119.4	2.5
xvi	$a \leq t \leq b$	144	144	-	-	-	-	-	-	0	1000	120.4	1.3
	$b \leq t \leq c$	168	168	-	-	-	-	-	-	0	1000	120.9	2.12
xvii	$a \leq t \leq b$	122.4	120	20	-	-	-	-	-	20	1000	120	1.34
	$b \leq t \leq c$	125.3	120	-	30	-	-	-	-	30	1000	119.9	1.96

A.3.1 Normal Grid Condition: Operating scenario i

The first simulation was performed for normal grid operation such as magnitude and THD of source voltage is 120V RMS and zero respectively as shown in Figure A.2. The source voltage is compared to 120V sinusoid reference voltage and error voltage is generated which is zero in this case. Thus, as per control strategy discussed in previous section, bidirectional switches S1S2 and S3S4 remains open while switch S5S6 remains closed and modified AC-DVR synthesizes almost zero voltage at its output terminals as depicted in Figure A.3. This voltage is injected in series with source voltage resulting load voltage and current to be same as source voltage and current as presented in Figure A.4. Hence, it can be verified that under normal grid conditions, modified AC-DVR does not operate and injects almost zero voltage in series with source voltage and load voltage and current are same as source voltage and current with zero THD.

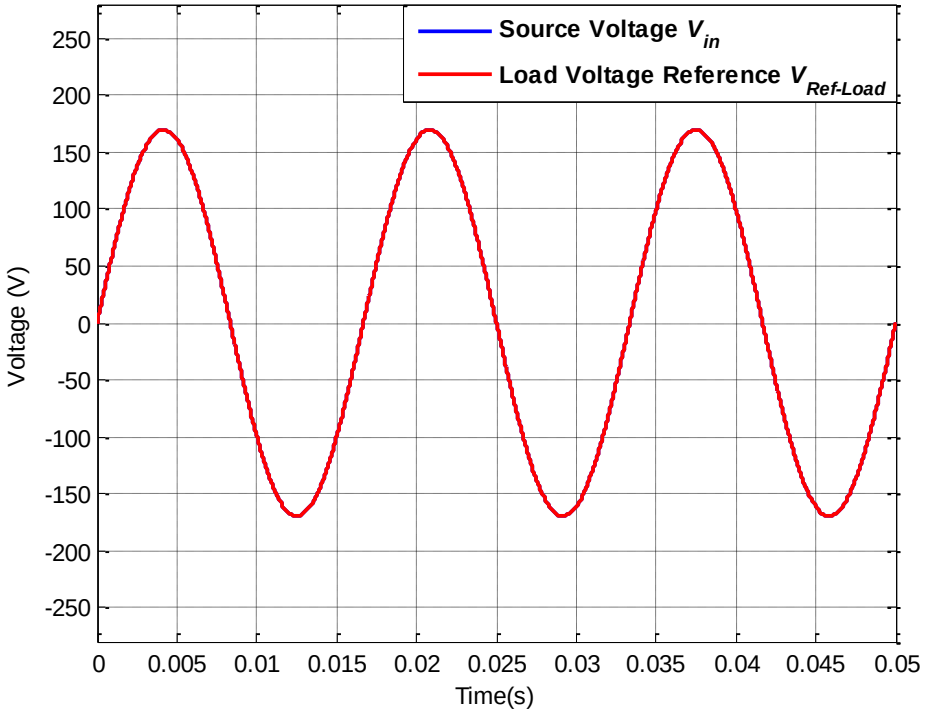

Figure A.2: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario i

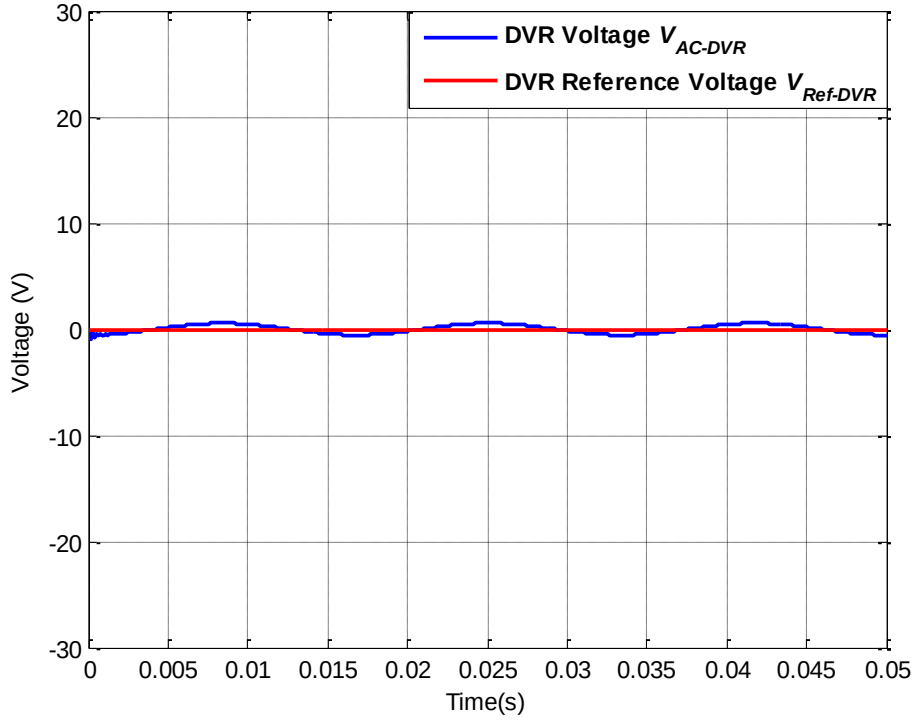

Figure A.3: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario i

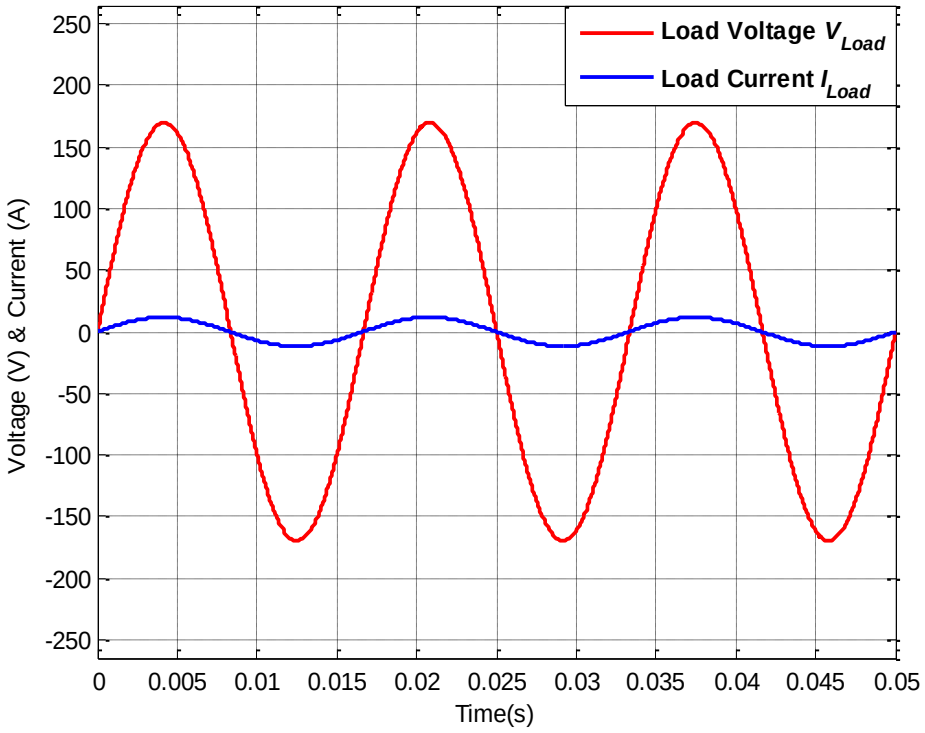

Figure A.4: Load voltage V_{Load} and load current I_{Load} for operating scenario i

A.3.2 3rd Harmonic distortion: Operating scenario ii

In this scenario, the source voltage has a fundamental component of 120V RMS at 60Hz and a 3rd harmonic component of 33.33% with frequency of 180Hz. Thus, RMS and THD of input voltage becomes 126.5V and 33.33% respectively. The modified AC-DVR should inject needed amount of voltage at 180Hz to restore the magnitude and shape of voltage at load side. The control unit of the system senses the source voltage and compares it with 120V sinusoidal load reference as shown in Figure A.5 and generates reference voltage for modified AC-DVR. The modified AC-DVR is supposed to generate 180° out of phase 3rd harmonic voltage with needed amplitude to restore load voltage. As discussed in section A.2, output of modified AC-DVR is always 180° out of phase from its input voltage. Hence, inductors/windings L1 or L2 are switched accordingly to synthesize voltage with positive and negative polarity from source voltage. Note that polarity of source voltage was changed by bidirectional bridge in previously discussed AC-DVR, while the same is achieved by switching inductors/windings L1 and L2 in case of modified AC-DVR. The modified AC-DVR is then switched with dedicated duty cycle, and injection voltage with desired shape, magnitude and phase is synthesized as shown in Figure A.6. The equation for the duty cycle generation is still same as previous AC-DVR as both flyback buck boost and normal buck boost works on the same principle. This voltage is injected in series with source voltage and load voltage is restored to 119.9V RMS with 2.03% THD as depicted in Figure A.6. The inductor currents are divided between L1 and L2 in this case and are depicted in Figures A.10 and A.11. The results for source currents, AC-DVR input currents, capacitor currents and source power are same as previous AC-DVR and are depicted in Figures A.8, A.9, A.12, A.13, A.14.

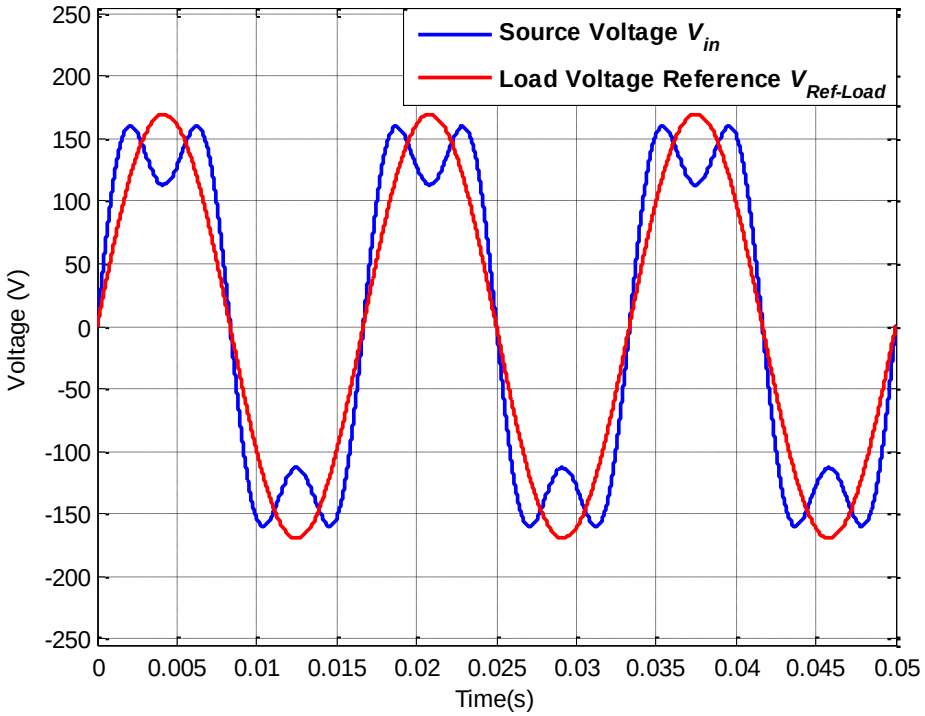

Figure A.5: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario ii

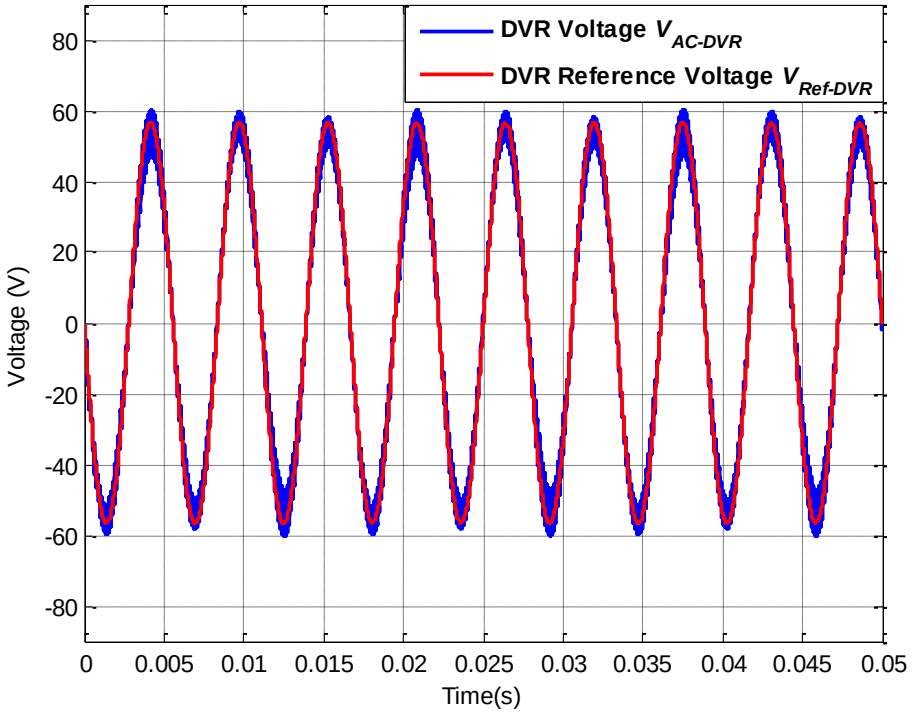

Figure A.6: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario ii

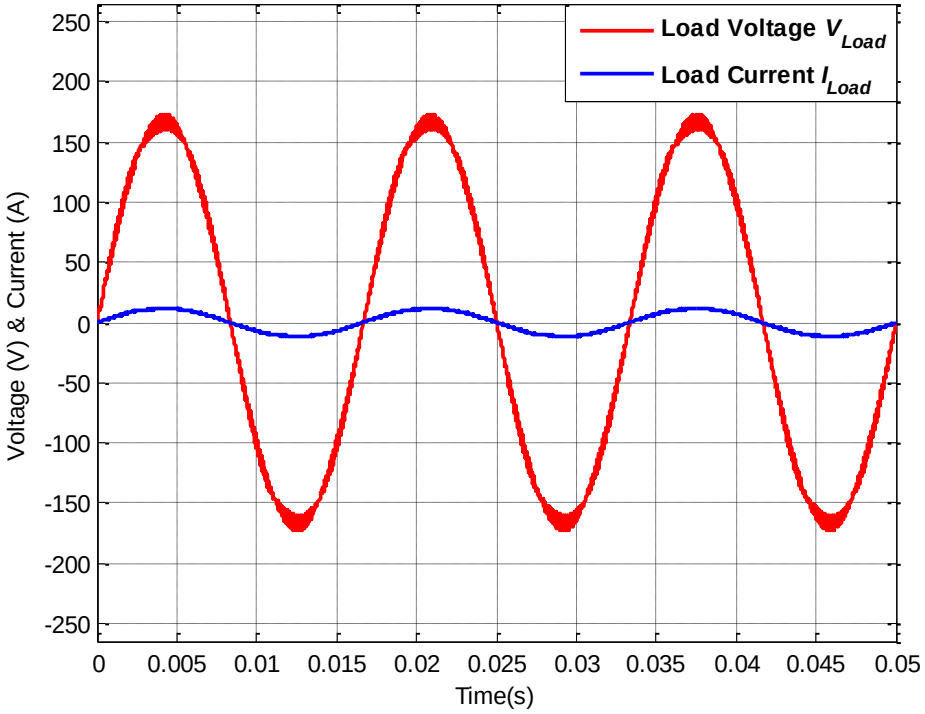

Figure A.7: Load voltage V_{Load} and load current I_{Load} for operating scenario ii

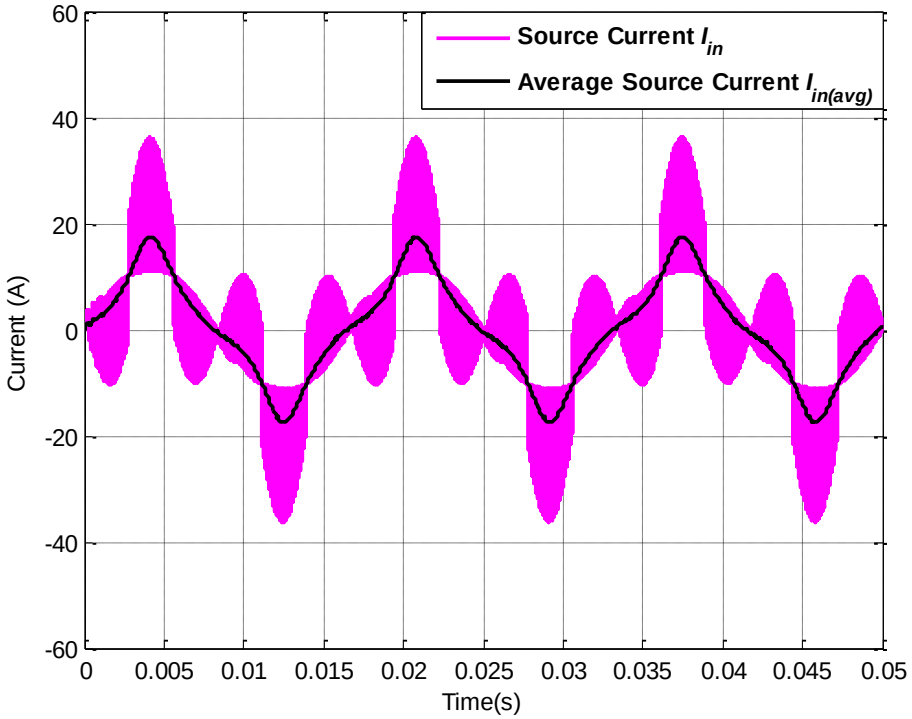

Figure A.8: Actual source current I_{in} and average source current $I_{in(avg)}$ for operating scenario ii

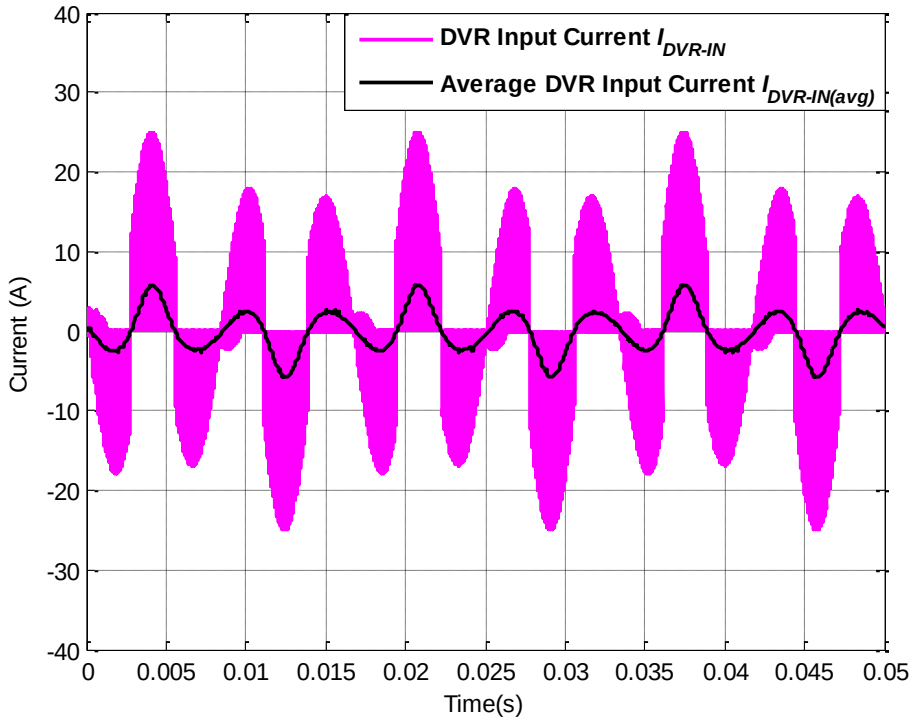

Figure A.9: Actual DVR current I_{DVR-IN} and average DVR current $I_{DVR-IN(avg)}$ for operating scenario ii

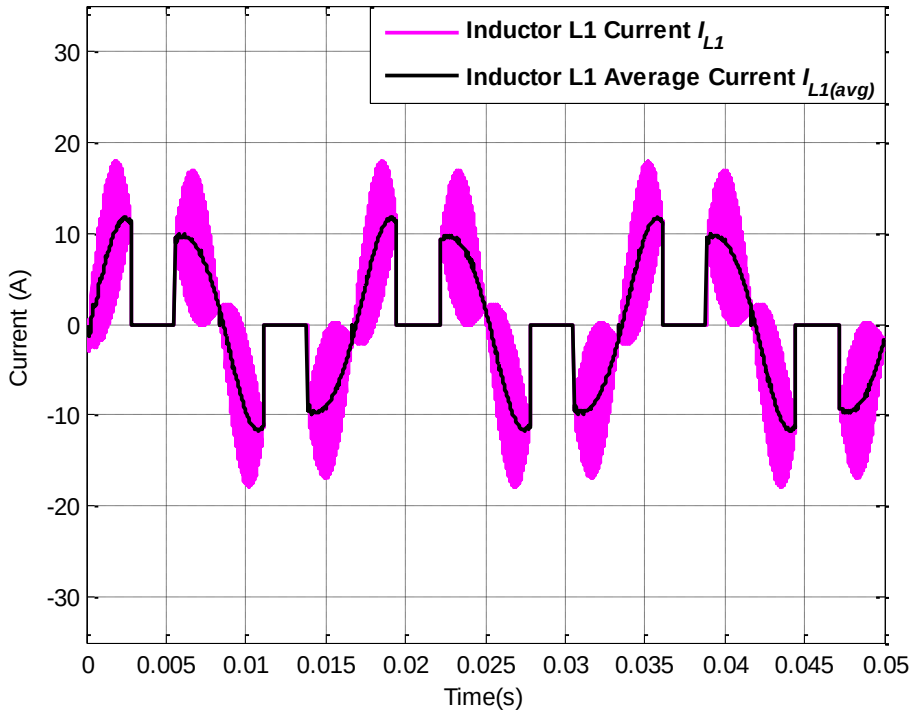

Figure A.10: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario ii

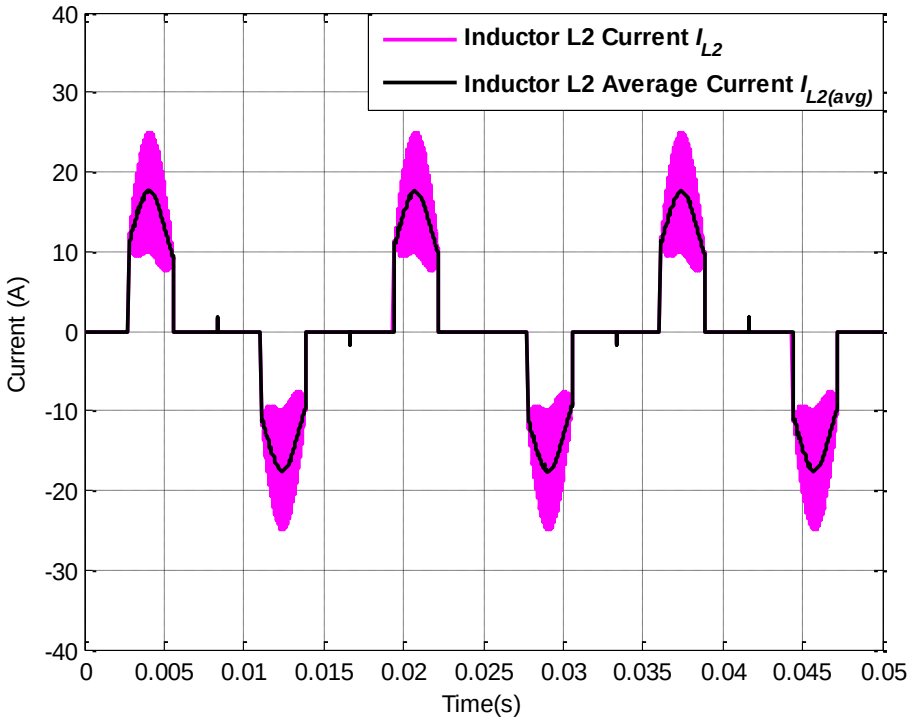

Figure A.11: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario ii

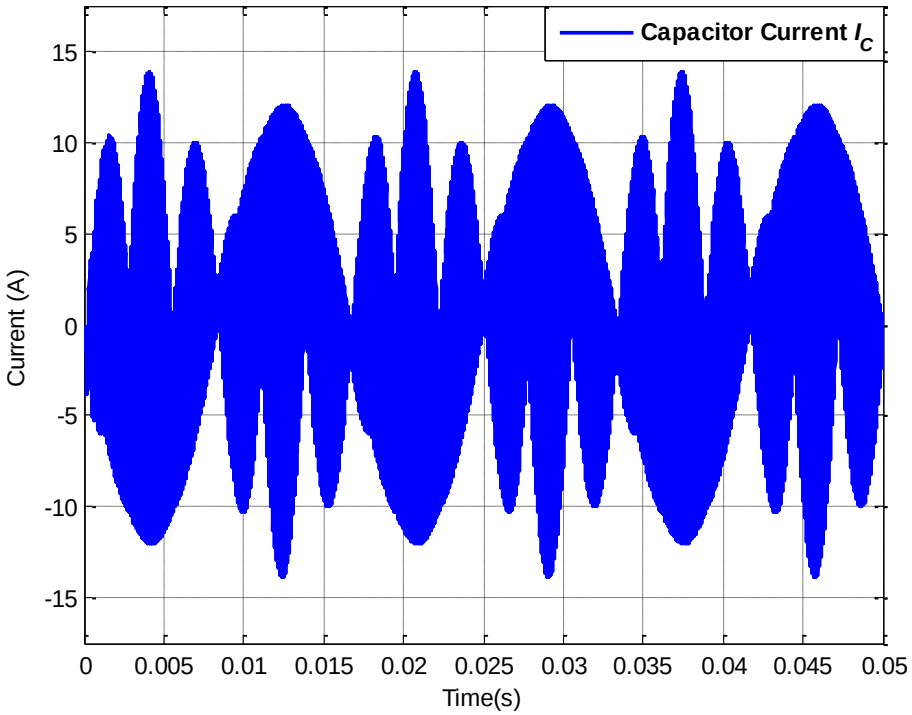

Figure A.12: Actual capacitor current I_C for operating scenario ii

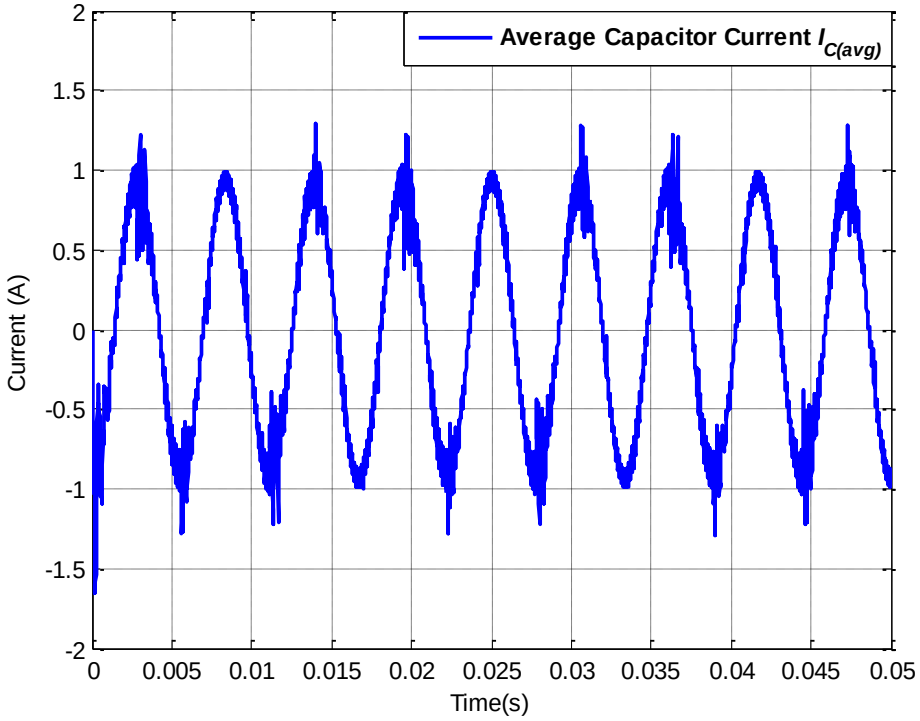

Figure A.13: Average capacitor current $I_{C(avg)}$ for operating scenario ii

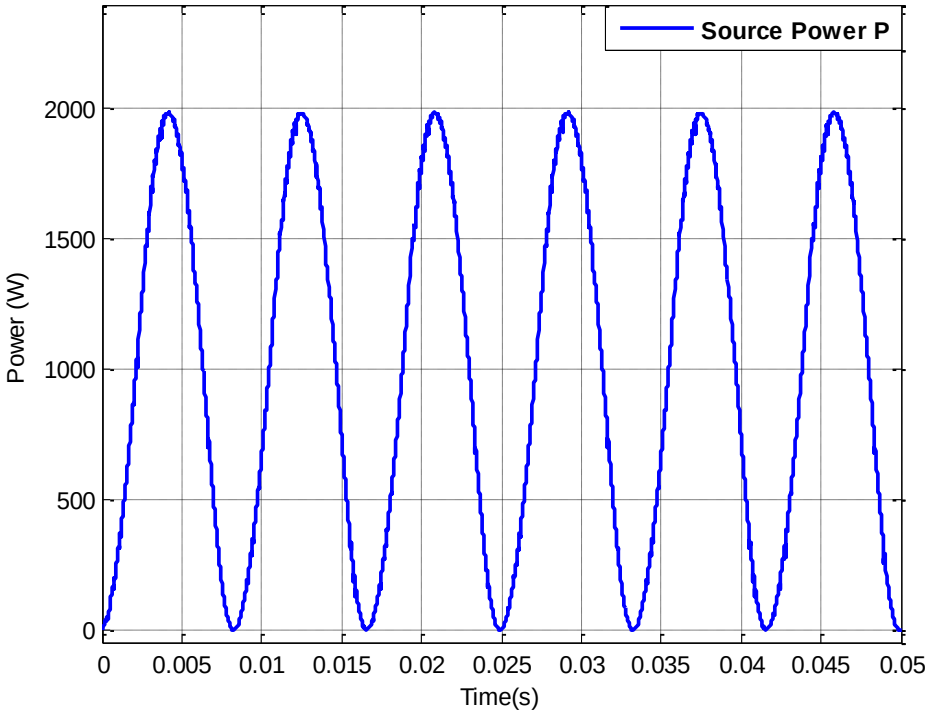

Figure A.14: Grid power for operating scenario ii

A.3.3 5th Harmonic distortion: Operating scenario iii

This operating scenario is like the scenario discussed in previous subsection. The only difference is the harmonic order and its percentage. In this operating condition, source voltage experiences 5th harmonic distortion with harmonic magnitude of 20% resulting input RMS and THD to be 112.4V and 20% respectively. The modified AC-DVR is operated with dedicated control and principle as discussed in section A.2. The simulation was performed for three fundamental cycles such as t=0 to t=0.05 seconds. The source voltage with 5th harmonic distortion and 120V sinusoid load voltage reference is depicted in Figure A.15. The output of modified AC-DVR and its reference voltage are shown in Figure A.16 which is added in series with source voltage. Hence, the load voltage RMS is restored to 119.9V whereas the THD is reduced to 1.41%. The load voltage and load current are presented in Figure A.17.

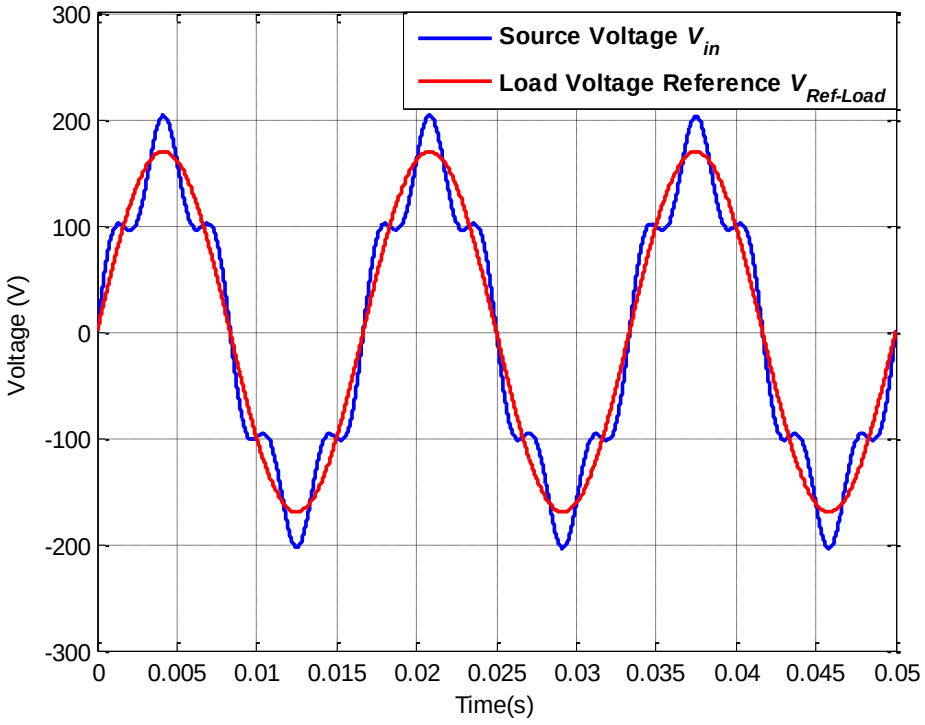

Figure A.15: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario iii

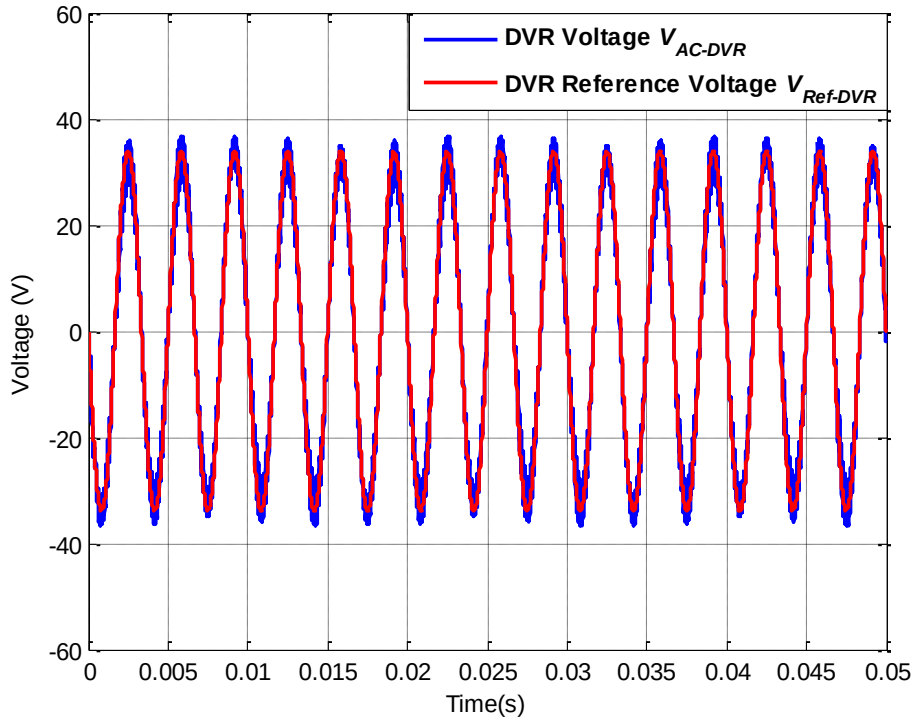

Figure A.16: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario iii

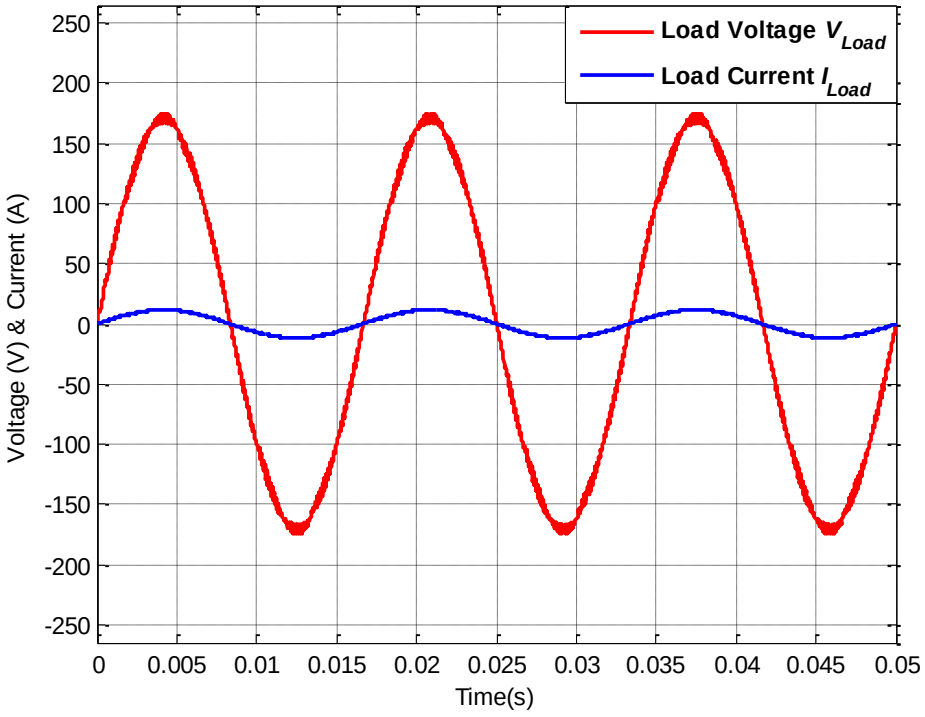

Figure A.17: Load voltage V_{Load} and load current I_{Load} for operating scenario iii

A.3.4 11th Harmonic distortion: Operating scenario vi

The source voltage has 9.09% of 11th harmonic distortion in this scenario which makes input RMS voltage 120.5V. The source voltage is sensed and compared with a 120V RMS sinusoidal reference signal and AC-DVR is operated to synthesize the error voltage which will be 11th harmonic voltage with 9.09% magnitude in this case. The simulation results for source voltage and 120V reference signal are presented in Figure A.18. The modified AC-DVR working as a replacement of both bidirectional bridge and AC-AC buck boost converter, synthesizes the 11th harmonic sinusoid with appropriate magnitude as shown in Figure A.19. This voltage is injected in series with source voltage and load voltage is restored to 120V RMS with 0.93% THD. The results for restored fine sinusoidal load voltage and load current are depicted in Figure A.20.

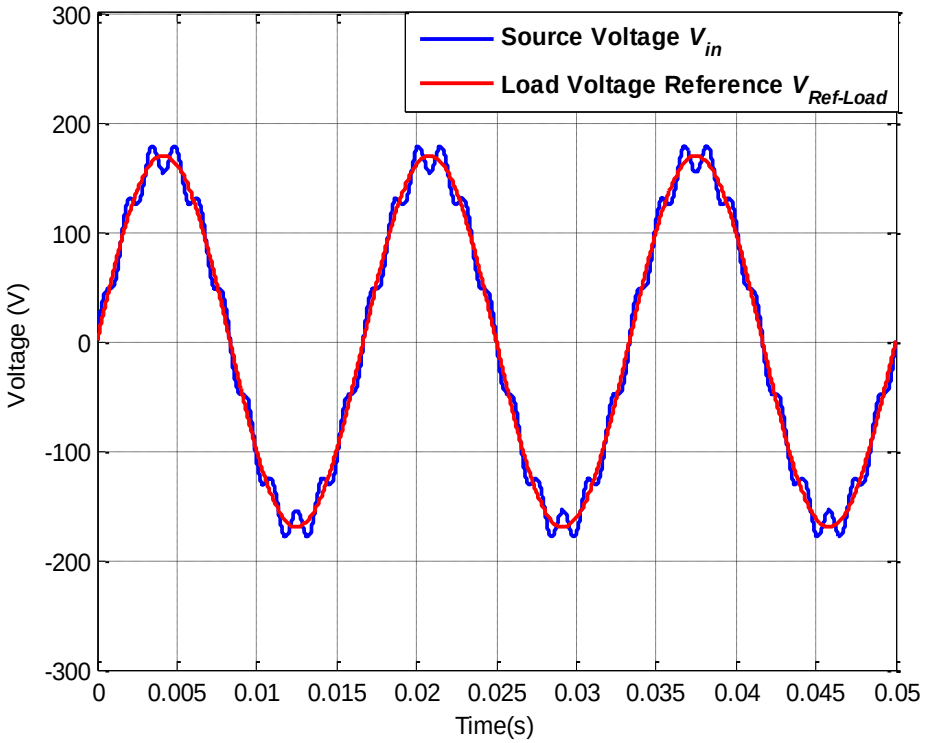

Figure A.18: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario vi

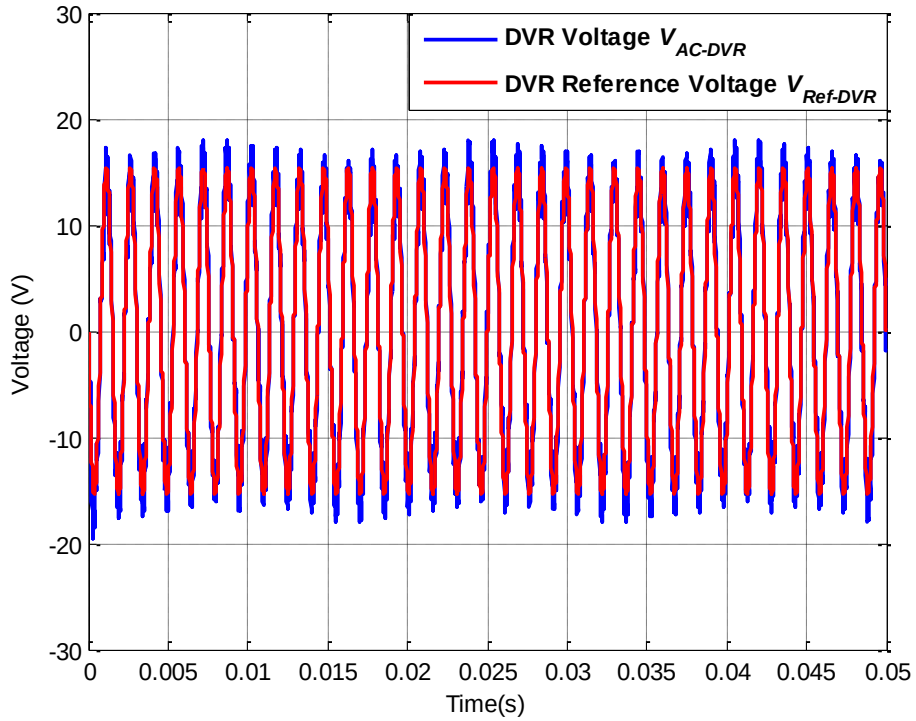

Figure A.19: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario vi

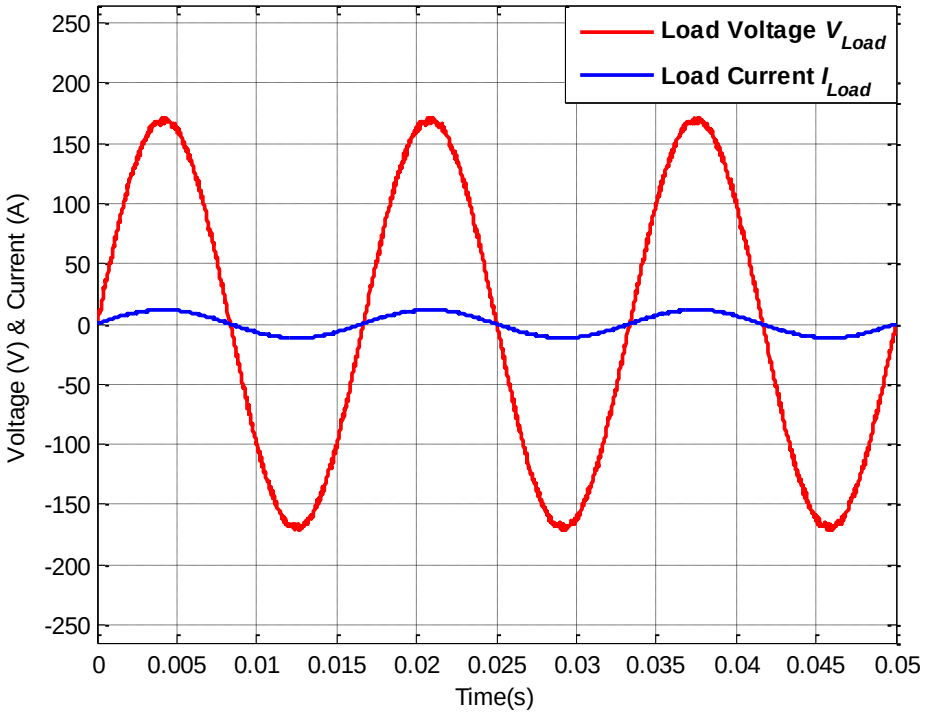

Figure A.20: Load voltage V_{Load} and load current I_{Load} for operating scenario vi

A.3.5 Combined harmonic distortion: Operating scenario viii

Simulations for individual harmonic voltage distortion are discussed and presented in previous scenarios. In this operating condition, performance of modified AC-DVR under combined effect of various harmonic orders will be evaluated. Thus, the source voltage is modelled with harmonic orders of 3^{rd}, 5^{th}, 7^{th}, 11^{th} and 13^{th} with magnitudes of 8%, 9%, 5%, 2% and 2% respectively as shown in Figure A.21. The working of modified AC-DVR is same as working of AC-DVR discussed in subsection 6.3.5 in chapter 3. The polarity of source voltage was changed by means of bidirectional bridge in previous case, while in this case the same is achieved by switching inductors/windings L1 or L2 accordingly. The control unit senses the source voltage and compare it with 120V sinusoidal load voltage reference as shown in Figure A.21. The modified AC-DVR operates with dedicated duty cycle and synthesizes voltage with needed shape, phase and magnitude to restore the load voltage as shown in Figure A.22. This voltage is added in series with source voltage and load voltage is restored to 120V RMS and THD is reduced to 0.92% from 13.34% as depicted in Figure A.23. Inductors/windings L1 and L2 are switched not only to utilize source voltage with different polarities, but they are also charged and discharged via inductor/winding L3 to enable wave shaping of the source voltage. Hence, the inductor currents are same as presented in subsection 6.3.5 but are divided between L1 and L2 for this case and are shown in Figure A.26 and A.27. Moreover, source currents, input currents of modified AC-DVR and capacitor currents follows same equations as discussed for previous AC-DVR and are presented in A.24, A.25, A.28 and A.29 respectively. Due to same working principle, as previous AC-DVR, power extracted from source is almost sinusoidal and does not have any higher frequency oscillations as shown in Figure A.30.

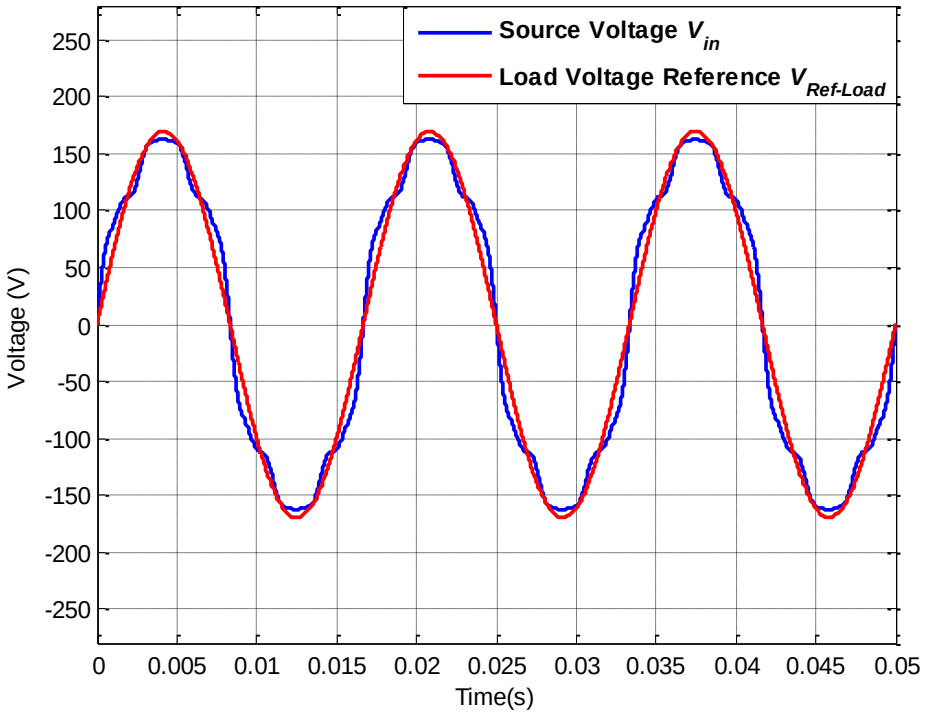

Figure A.21: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario viii

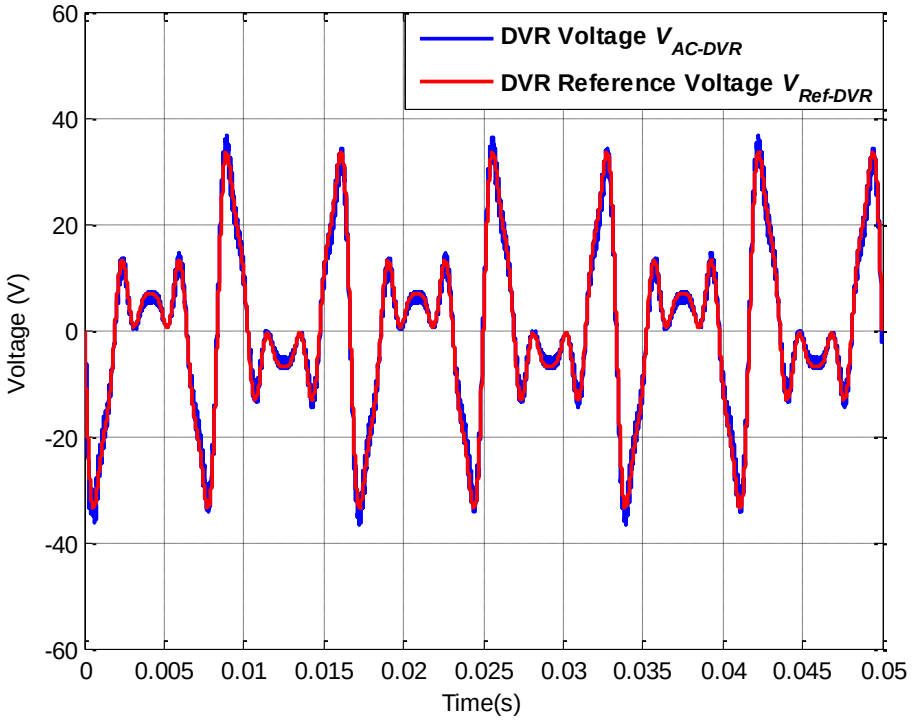

Figure A.22: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario viii

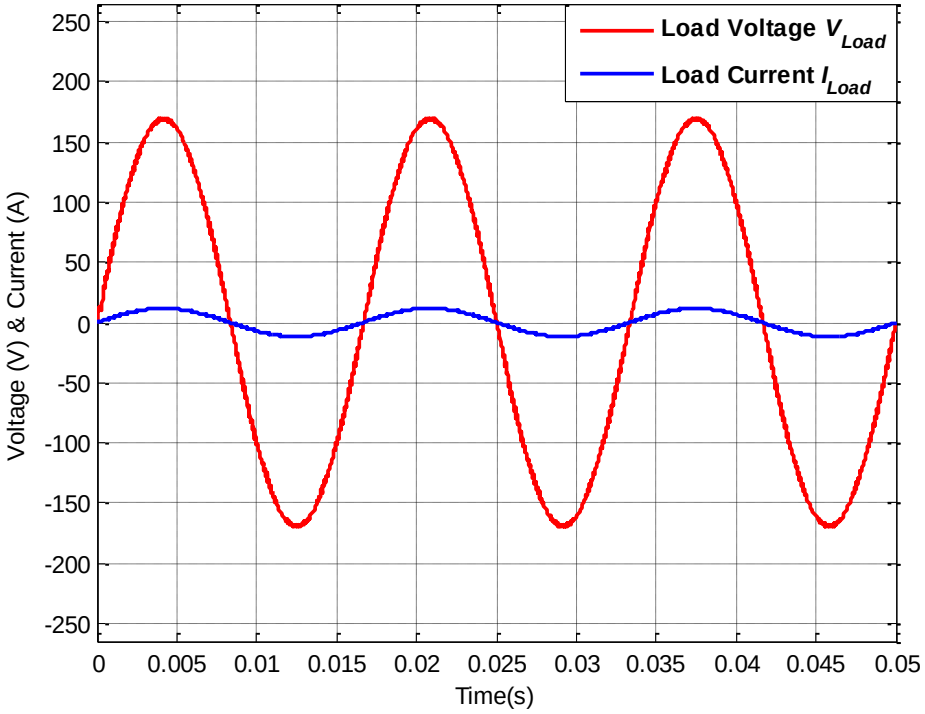

Figure A.23: Load voltage V_{Load} and load current I_{Load} for operating scenario viii

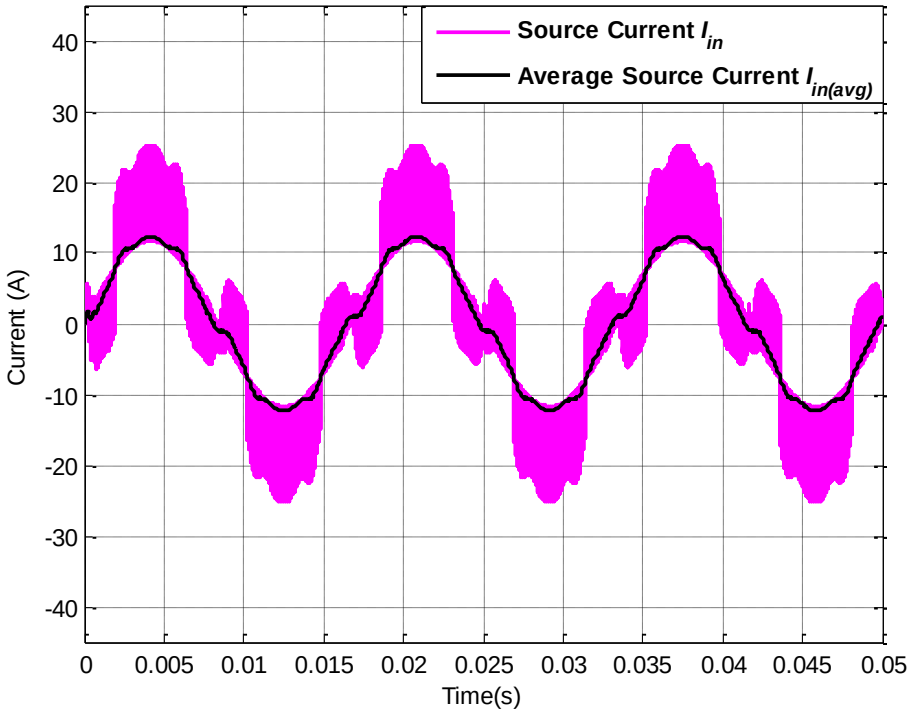

Figure A.24: Actual source current I_{in} and average source current $I_{in(avg)}$ for operating scenario viii

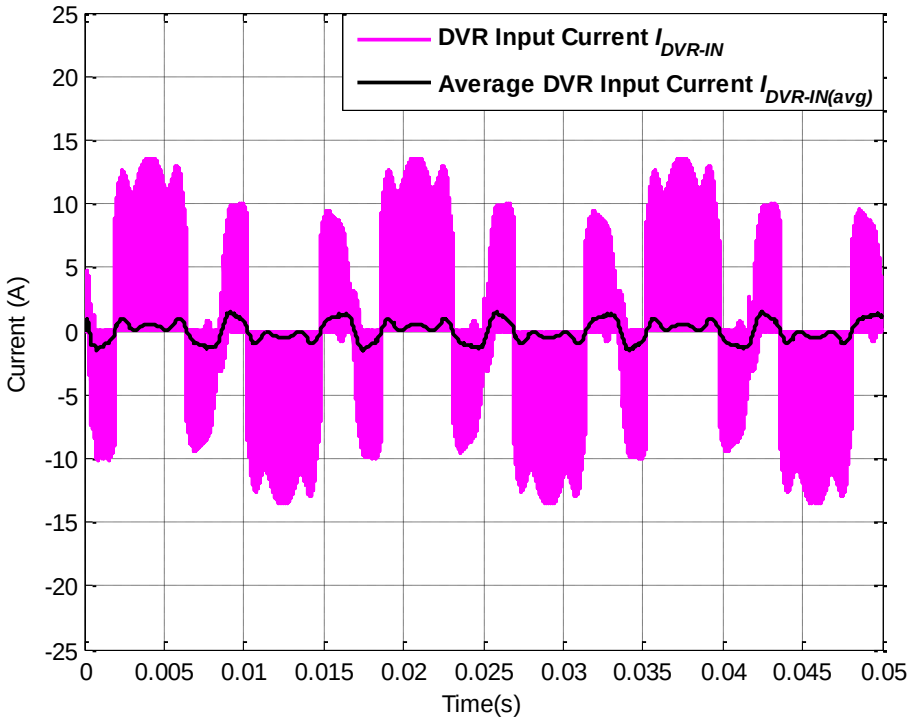

Figure A.25: Actual DVR current I_{DVR-IN} and average DVR current $I_{DVR-IN(avg)}$ for operating scenario viii

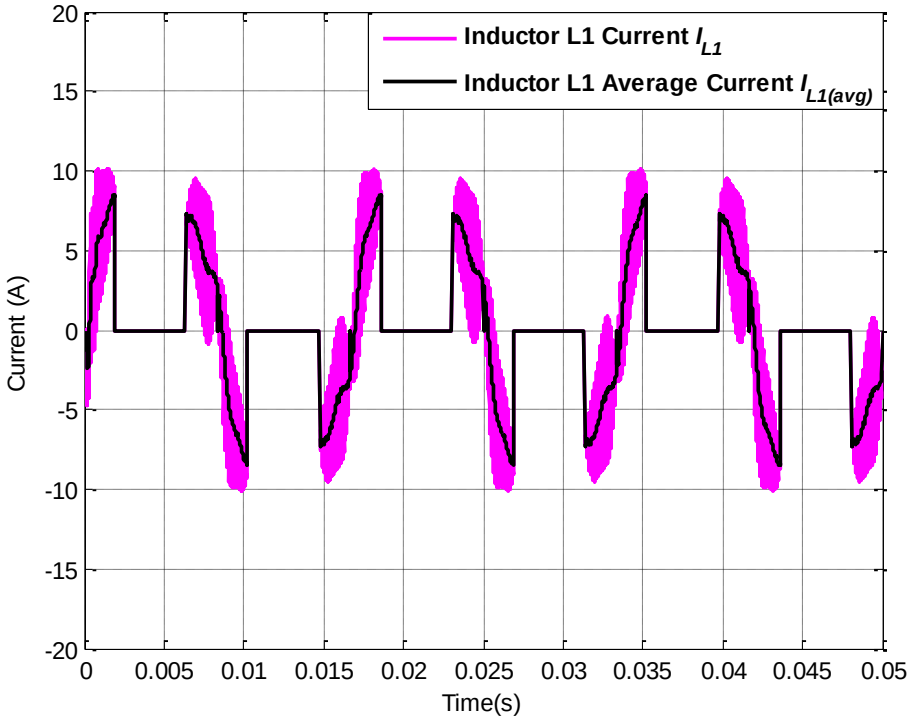

Figure A.26: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario viii

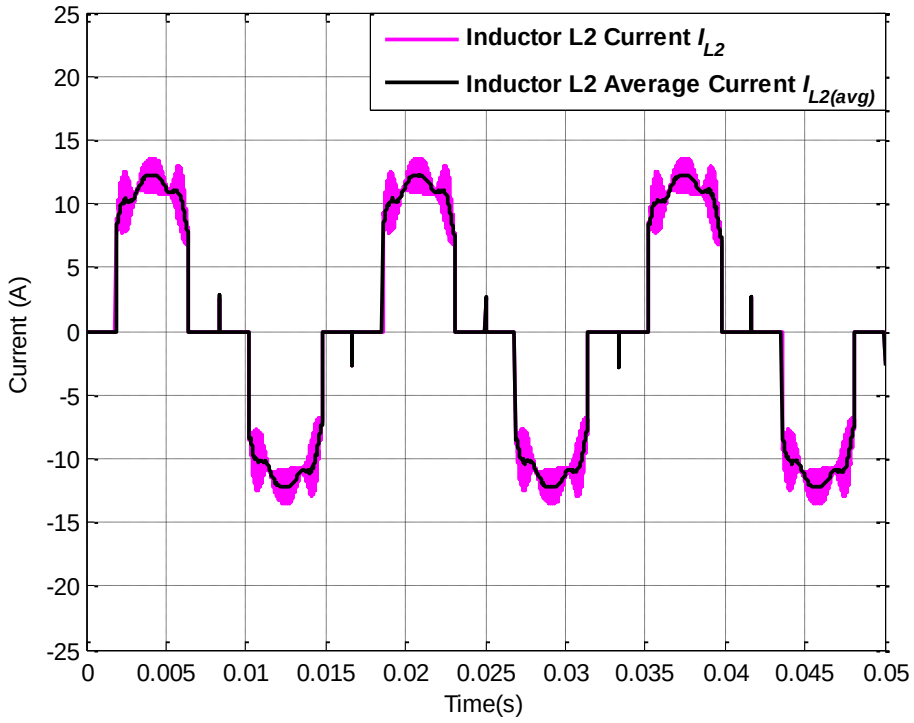

Figure A.27: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario viii

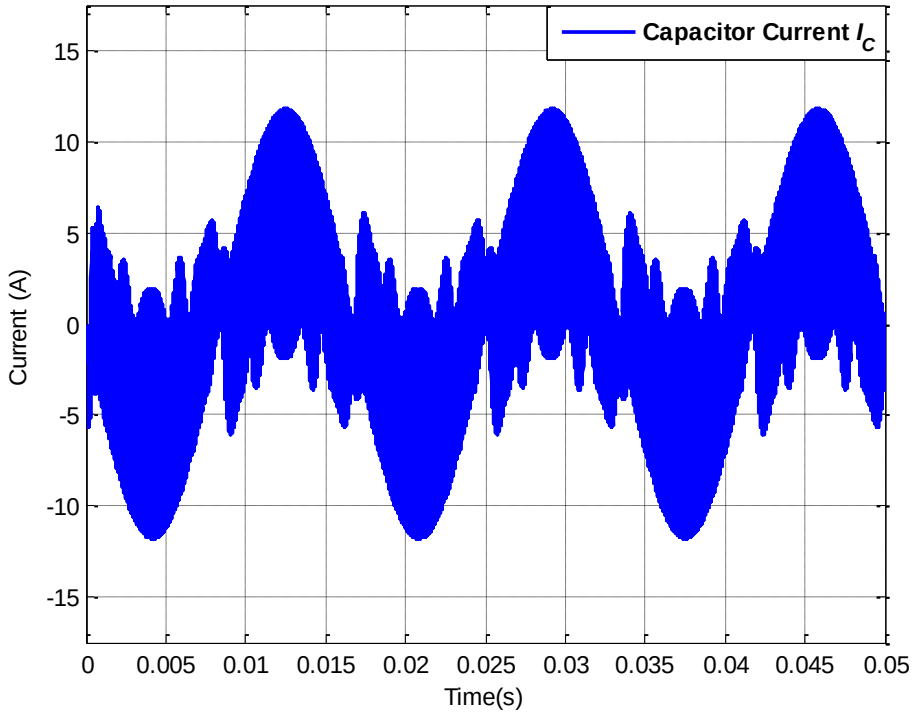

Figure A.28: Actual capacitor current I_C for operating scenario viii

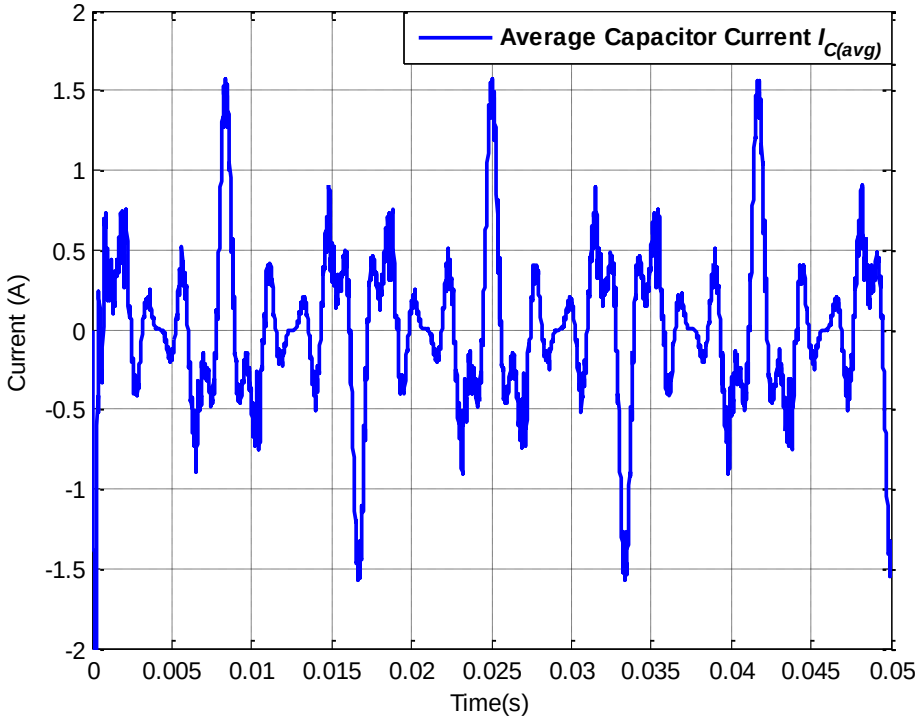

Figure A.29: Average capacitor current $I_{C(avg)}$ for operating scenario viii

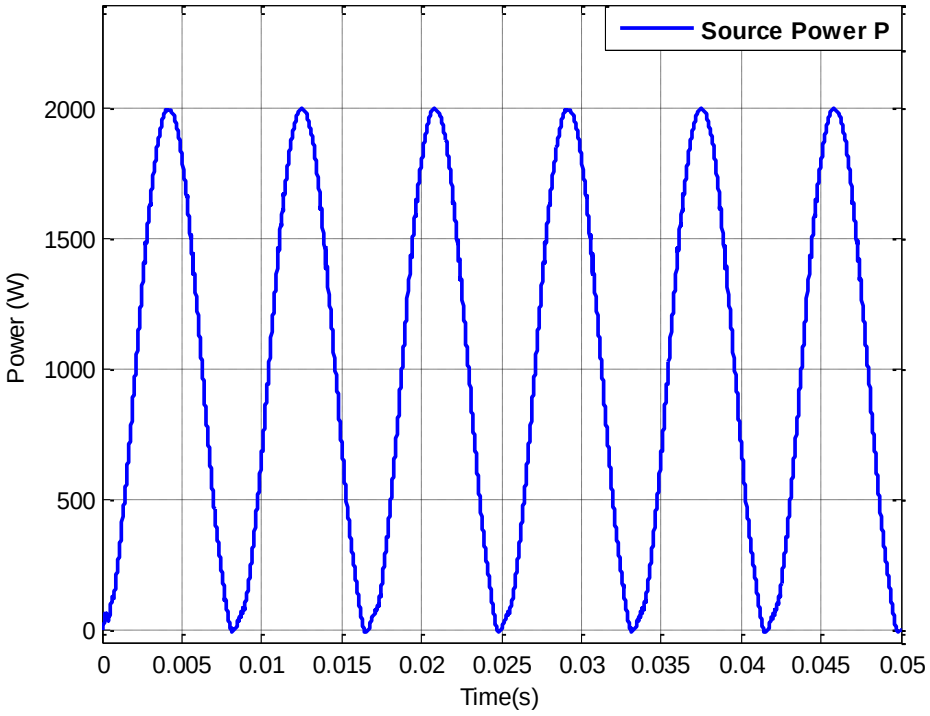

Figure A.30: Grid power for operating scenario viii

A.3.6 Combined harmonic distortion: Operating scenario ix

The performance of AC-DVR is simulated for combined harmonic distortion in source in previous scenario. The simulations for same type of disturbance with different types of harmonic order and their magnitude have been performed in this subsection. The source voltage has 3rd, 5th, 7th, 9th, 11th, and 13th harmonic with 33.33%, 20%, 14.29%, 11.11%, 9.09% and 7.69% magnitude which results in THD of 44.5% and RMS of 131.3V. The inductors/windings L1 or L2 are charged and discharged by L3 and capacitor C to synthesize desired negative and positive portions of error voltage as discussed in section A.2. The voltage synthesized by modified AC-DVR is injected in series with source voltage and load voltage is restored to 119.9V RMS and 3.26% of THD. The simulation results for source voltage, modified AC-DVR output and load voltage and current are presented in Figure A.31, A.32, and A.33 respectively.

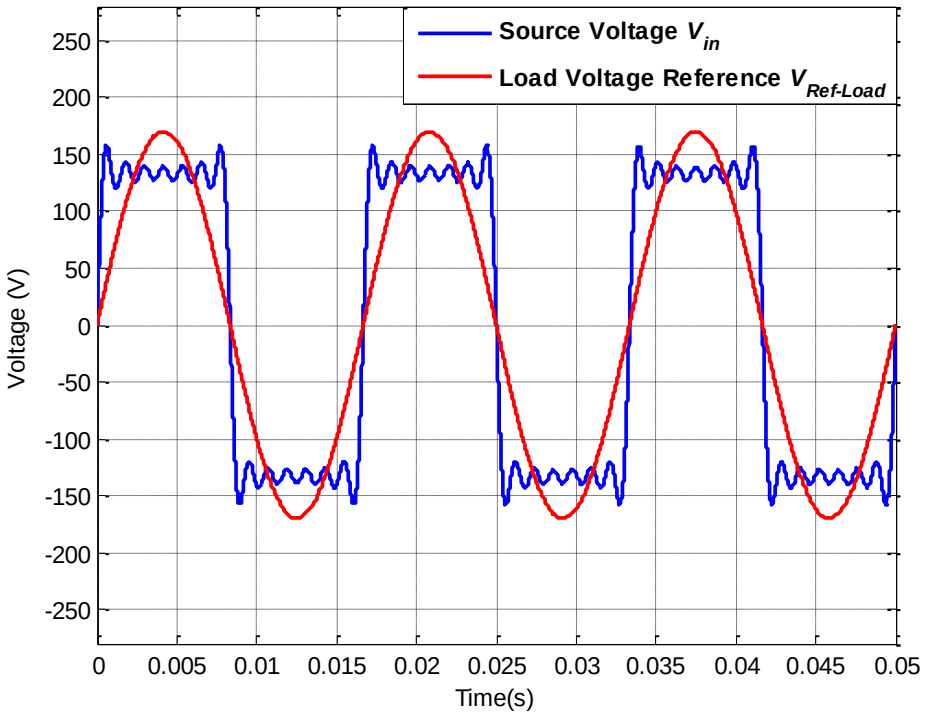

Figure A.31: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario ix

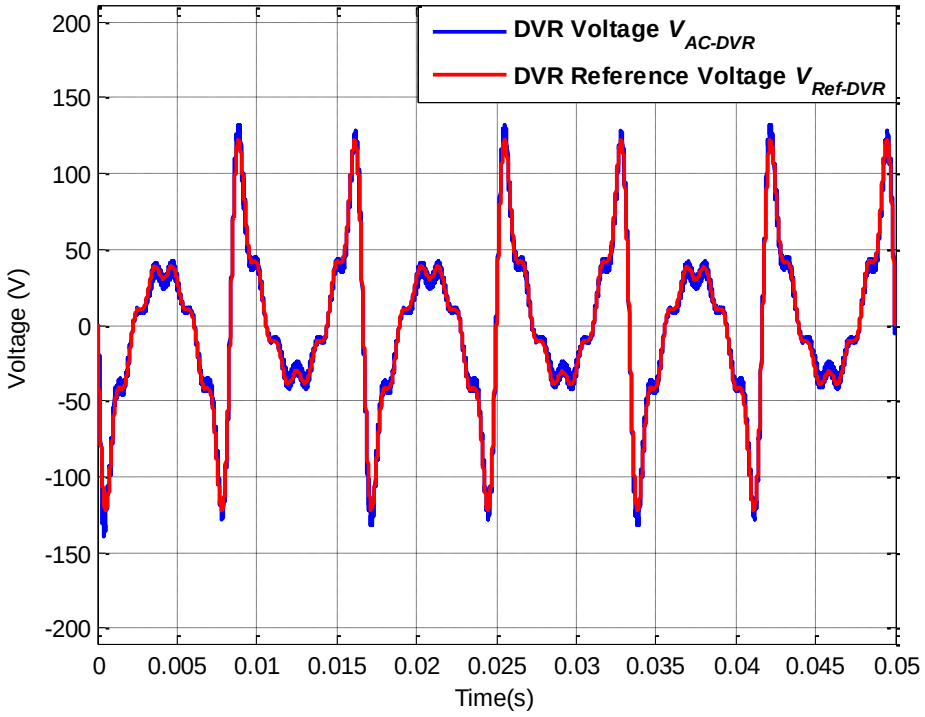

Figure A.32: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario ix

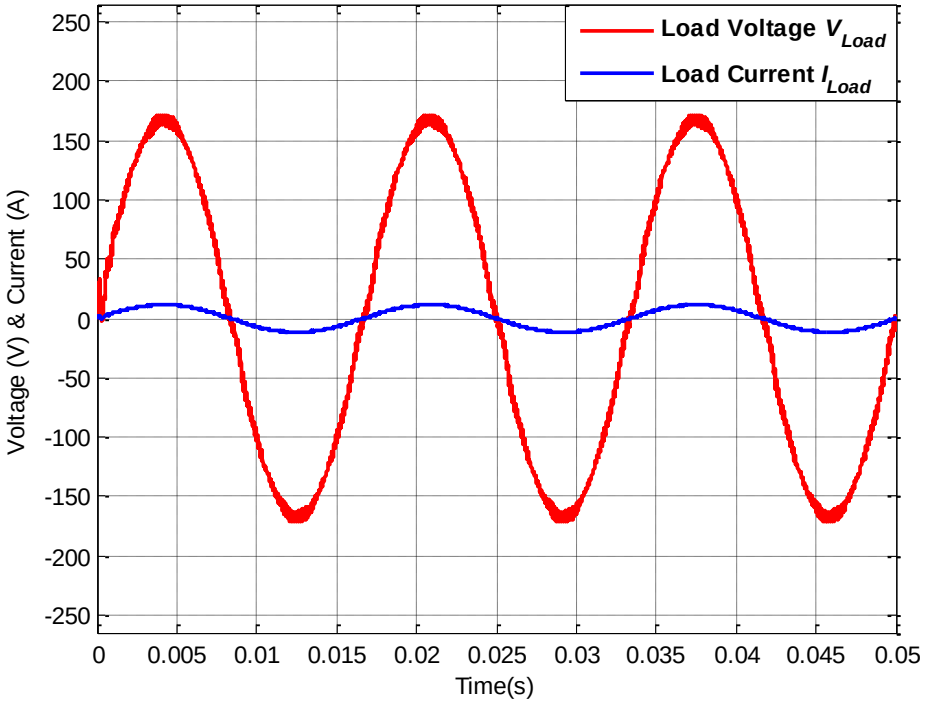

Figure A.33: Load voltage V_{Load} and load current I_{Load} for operating scenario ix

A.3.7 Voltage sag: Operating scenario x

In previous scenarios both individual and combined harmonic disturbances were discussed. In this scenario, the performance of modified AC-DVR under voltage sag condition is validated. The source experiences 30% voltage sag and RMS is reduced to 84V as shown in Figure A.34. Bidirectional switch S3S4 always operates to utilize 180° out of phase source voltage for synthetization of in phase error voltage. Thus, modified AC-DVR provides a voltage with same phase and shape as source voltage but with magnitude which needs to be added with source voltage to restore load voltage at 120V. The simulation results for source voltage and output of modified AC-DVR are depicted in Figure A.34 and A.35 respectively. The voltage synthesized by AC-DVR is added in series with source voltage and load voltage is restored to 119.2V RMS with 2.16% THD. The simulation results for load voltage and current are shown in Figure A.36.

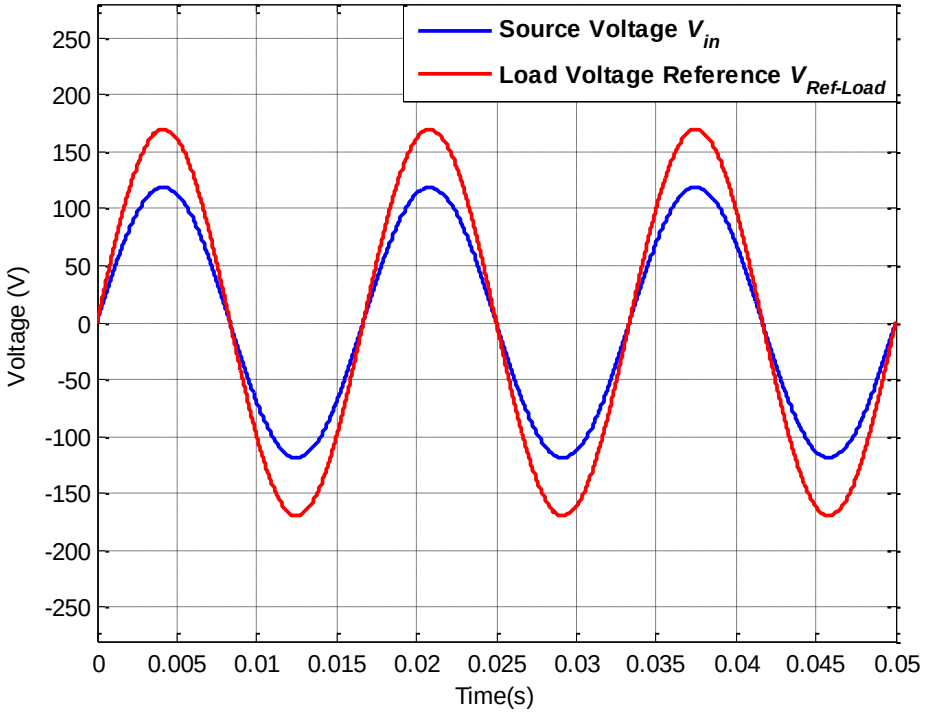

Figure A.34: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario x

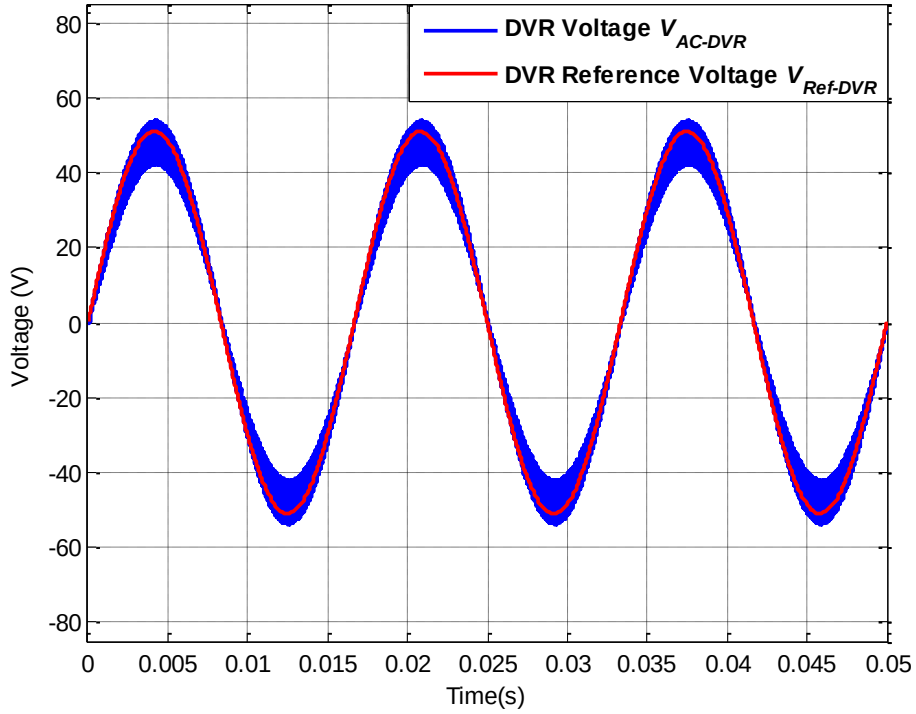

Figure A.35: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario x

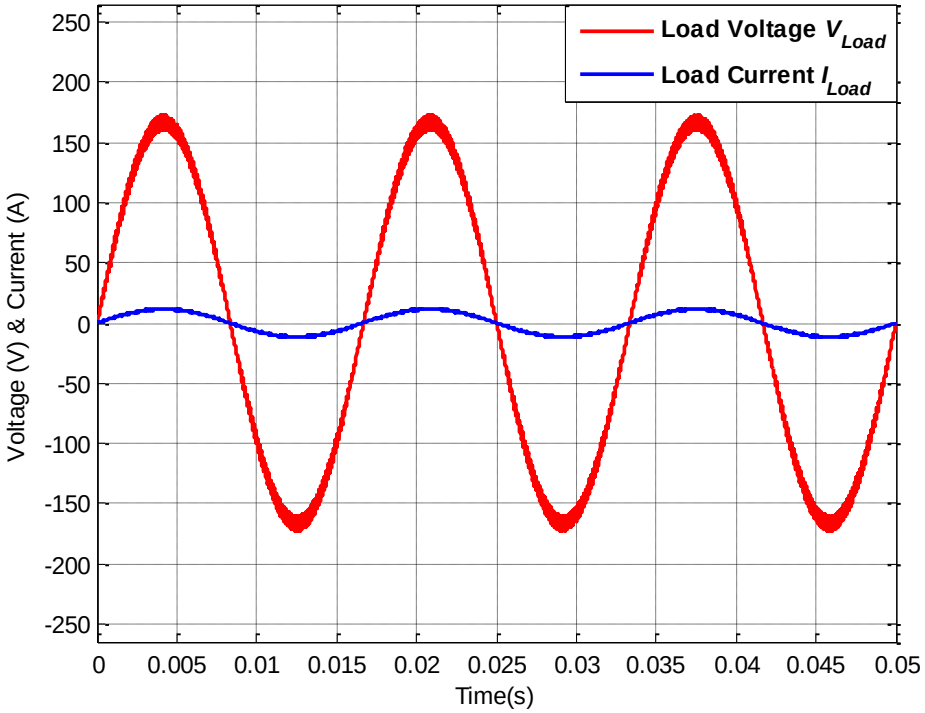

Figure A.36: Load voltage V_{Load} and load current I_{Load} for operating scenario x

A.3.8 Voltage swell: Operating scenario xi

This operating condition has been created to evaluate the performance of AC-DVR under voltage swell or overvoltage type of disturbances. The source voltage contains 30% overvoltage which increases the RMS voltage from 120V to 156V as shown in Figure A.37. Thus, to restore the voltage to 120V RMS, inductor/winding L1 always conducts to utilize the source voltage with its original phase and magnitude. The modified AC-DVR operates with dedicated control discussed in section A.2 and synthesizes 180° out of phase voltage with same shape as source voltage and RMS of 36V. This voltage is added in series with the source and load voltage is restored to 120.6V RMS with 1.76% of THD. Simulation results for source voltage experiencing 30% swell, voltage synthesized by modified AC-DVR and load voltage and current are presented in Figure A.37, A.38 and A.39 respectively.

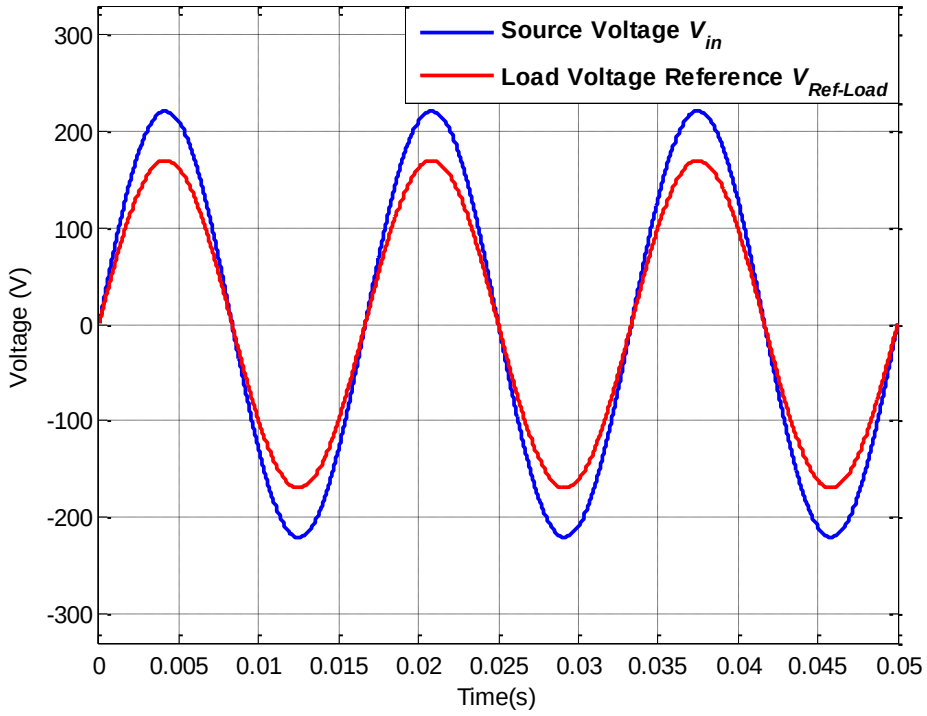

Figure A.37: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario xi

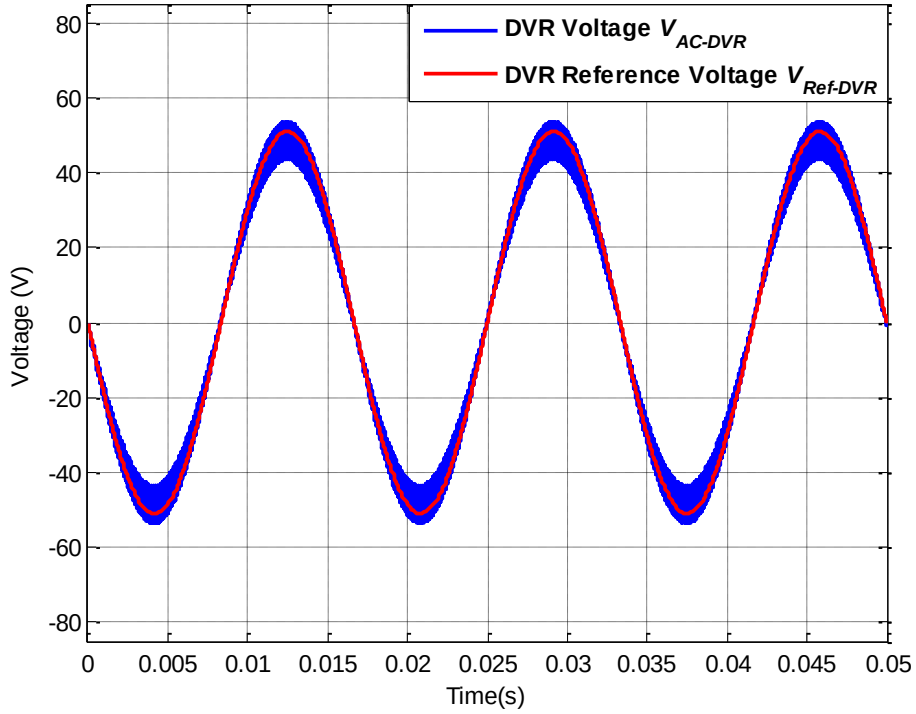

Figure A.38: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario xi

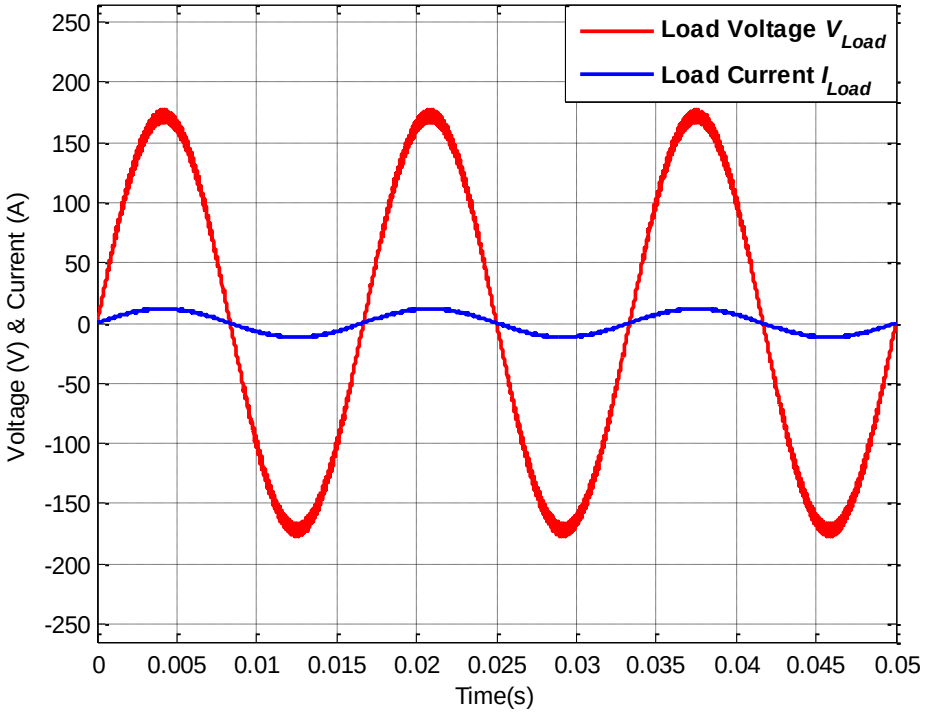

Figure A.39: Load voltage V_{Load} and load current I_{Load} for operating scenario xi

A.3.9 Combined harmonic and voltage sag: Operating scenario xii

In this operating scenario, behavior of AC-DVR is validated for combination of two different types of disturbances which will be harmonics and sag. The source experiences harmonic distortion of same orders as discussed in scenario viii with magnitudes of 10%, 11%, 6.25%, 2.5% and 2.5% with THD of 16.68% and 20% voltage sag as shown in Figure A.40. The source voltage is compared with load voltage reference and reference voltage for modified AC-DVR is generated. The inductors/windings L1 and L2 are switched to utilize source voltage in negative or positive polarities and modified AC-DVR operates with dedicated control to synthesize voltage with desired shape, magnitude and phase as shown in Figure A.41. This voltage is injected in series with source voltage and the load voltage is restored to 119.5V RMS with 1.83% THD as shown in Figure A.42.

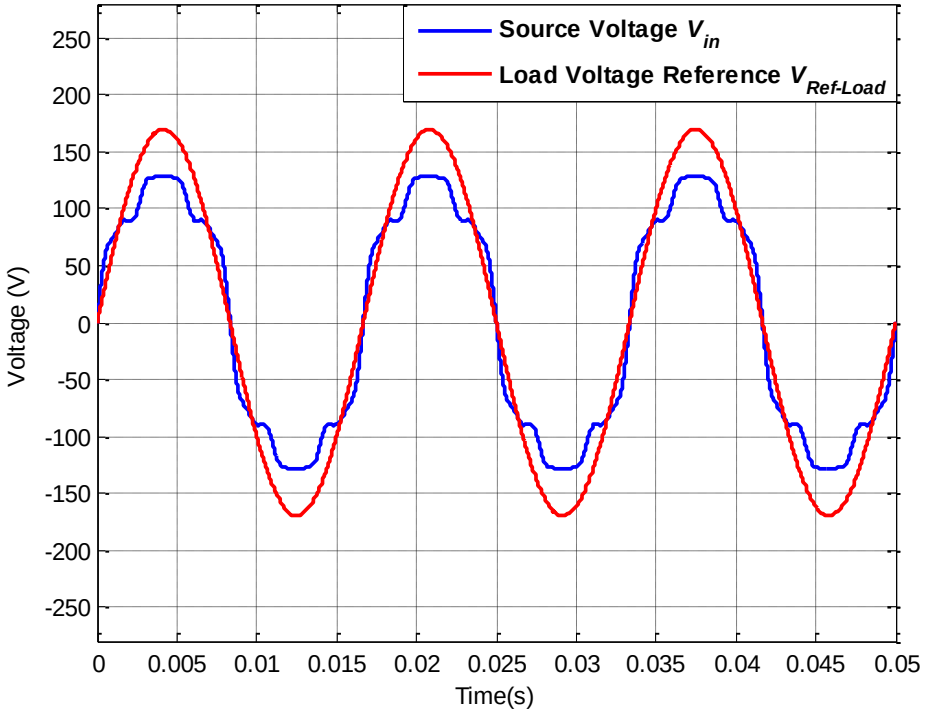

Figure A.40: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario xii

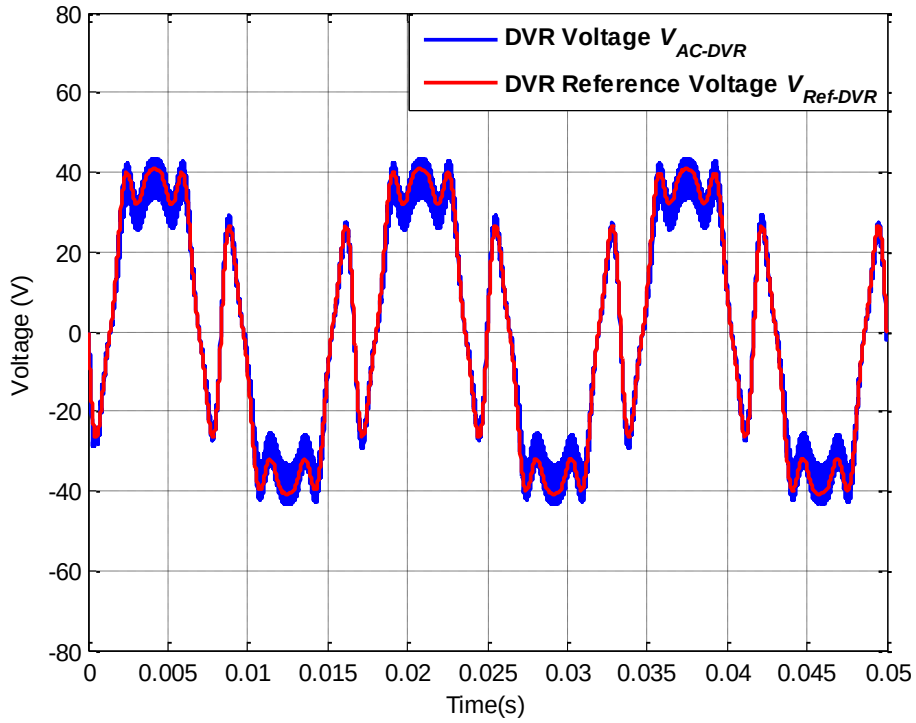

Figure A.41: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario xii

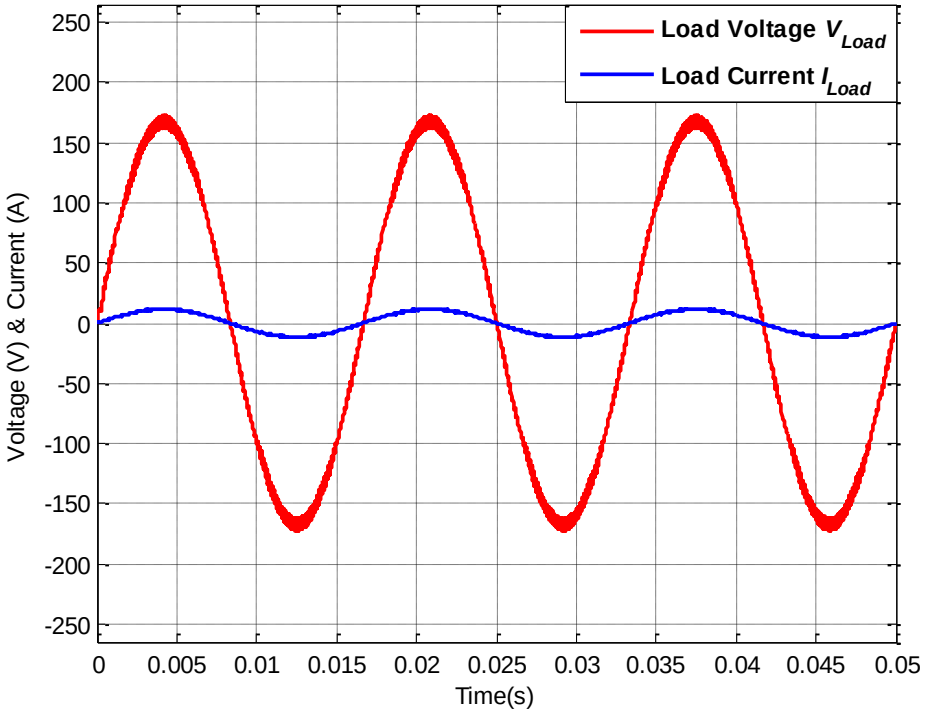

Figure A.42: Load voltage V_{Load} and load current I_{Load} for operating scenario xii

A.3.10 UNC Charlotte service voltage: Operating scenario xiii

In this operating scenario, simulations for behavior of AC-DVR under more realistic grid conditions have been performed. The grid voltage available at 120V power outlet at UNC Charlotte is used for this scenario. The voltage at UNC Charlotte's outlet contains 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th} and 13^{th} order harmonics with magnitudes of 1.78%, 3.36%, 1.6%, 0.19%, 2.52%, and 1.43% with THD of 5.12% and 116V RMS. The source voltage is shown in Figure A.43. The working of modified AC-DVR is same as discussed in previous subsections. Such as, source voltage is compared with load voltage reference and reference voltage for modified AC-DVR is generated. The inductors/windings L1 or L2 are switched to change the polarity of source voltage and modified AC-DVR synthesizes desired voltage with appropriate shape, magnitude and phase. The simulation results for output of modified AC-DVR are presented in Figure A.44. This voltage is injected in series with source voltage and load voltage is restored to 119.9V RMS with 0.74% of THD as shown in Figure A.45. Also, results for modified AC-DVR currents, inductor L1 currents, inductor L2 currents and capacitor currents are presented in Figures A.47, A.48, A.49, A.50 and A.51 respectively. Note that all these currents are same as previous AC-DVR currents and follow the same equations, only difference is that the inductor currents are divided between two inductors in this case. The actual and averaged source currents are presented in Figure A.47. As discussed in previous subsections, this currents are also governed by the same equations which are presented for previous AC-DVR. Thus, as shown in Figure A.52, the power delivered by the source is almost sinusoidal and does not contain any other frequency oscillations except fundamental frequency.

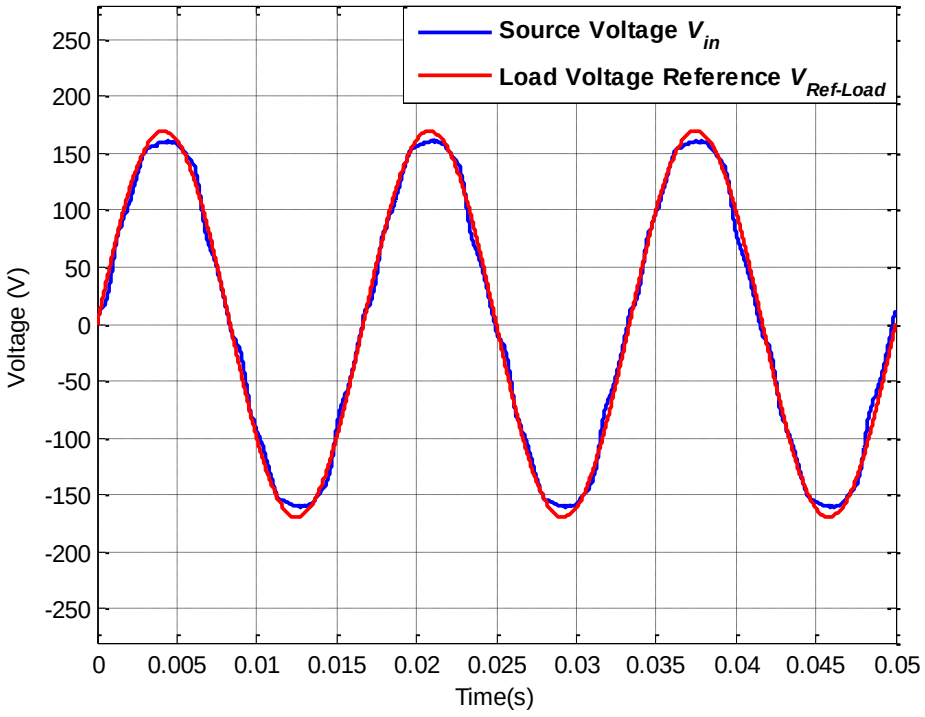

Figure A.43: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario xiii

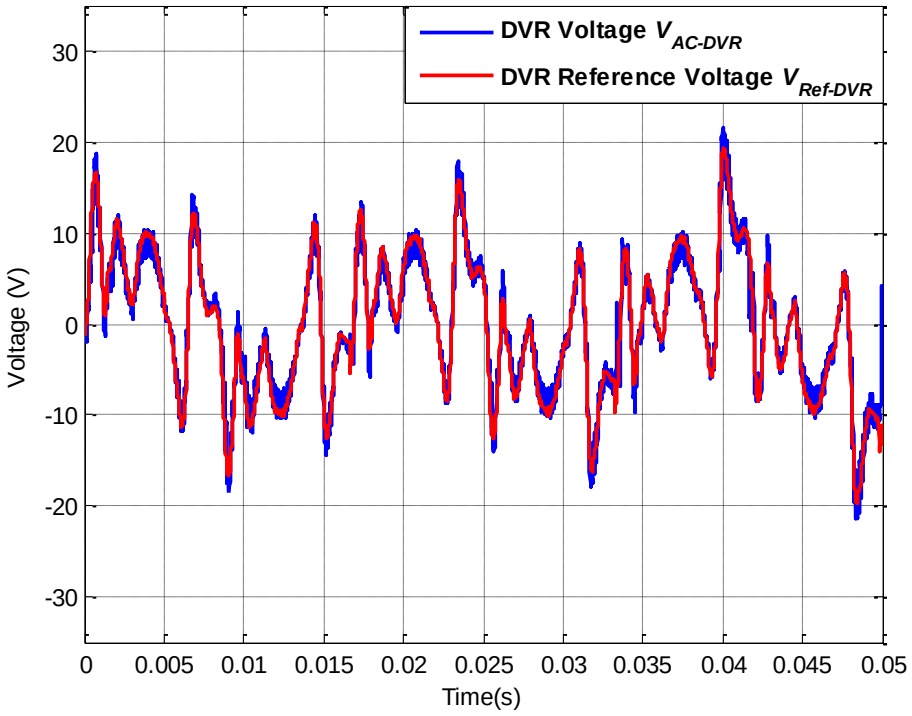

Figure A.44: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario xiii

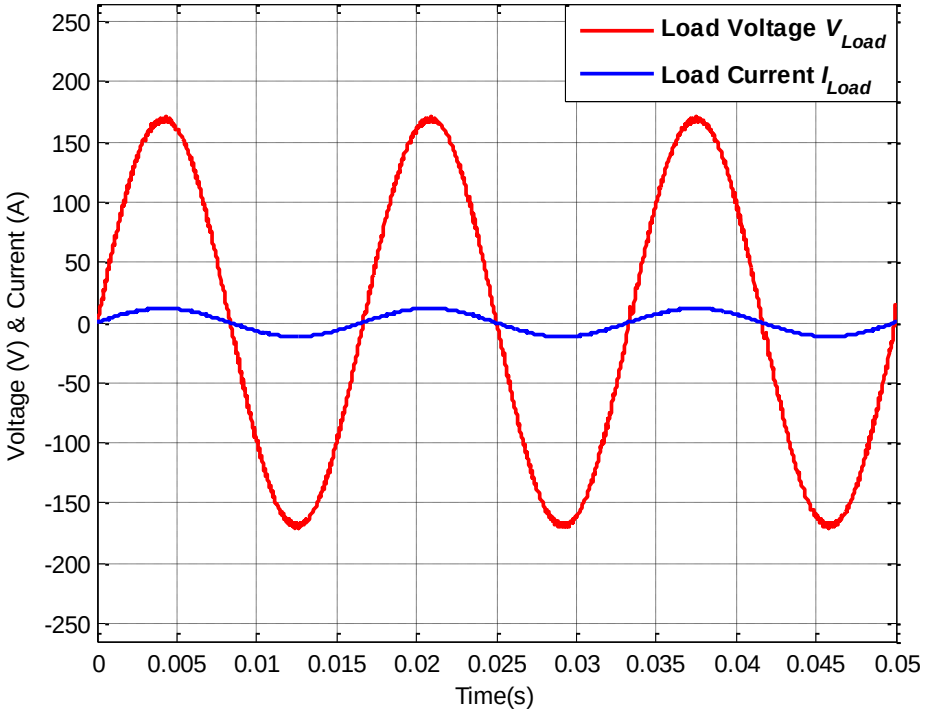

Figure A.45: Load voltage V_{Load} and load current I_{Load} for operating scenario xiii

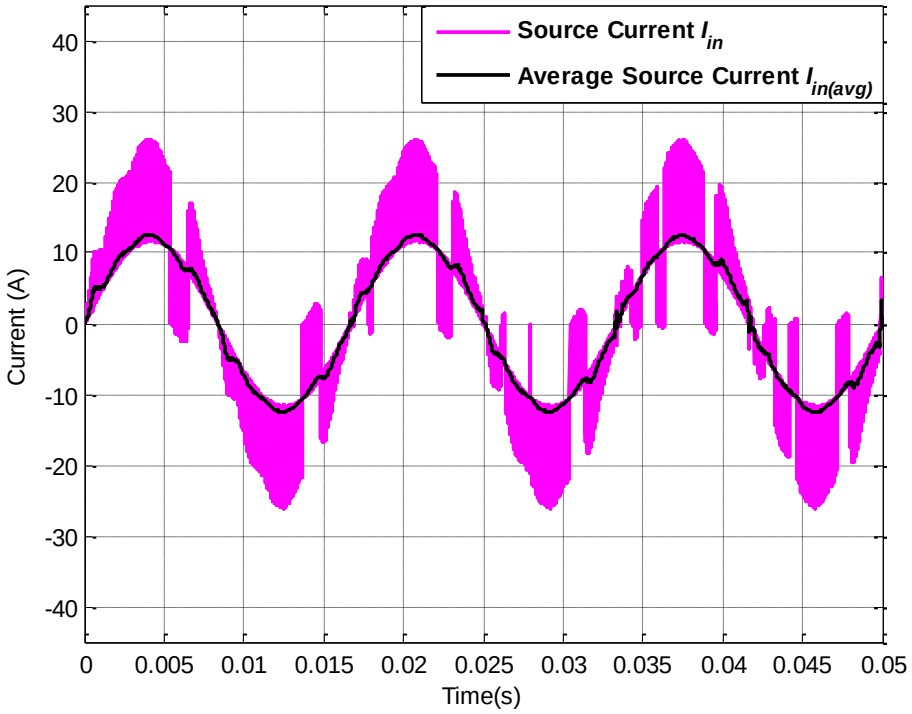

Figure A.46: Actual source current I_{in} and average source current $I_{in(avg)}$ for operating scenario xiii

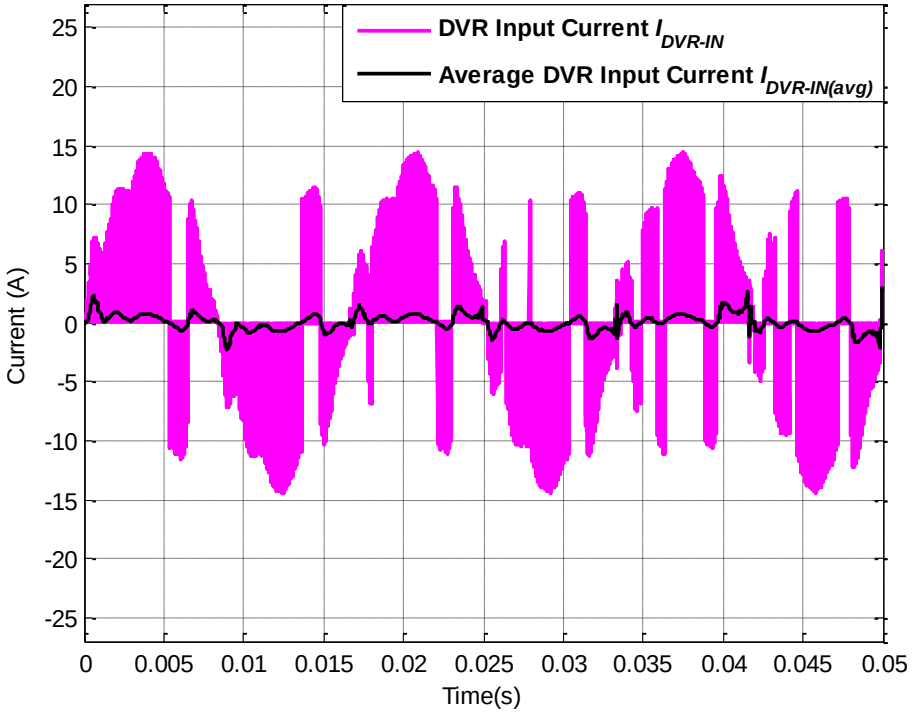

Figure A.47: Actual DVR current I_{DVR-IN} and average DVR current $I_{DVR-IN(avg)}$ for operating scenario xiii

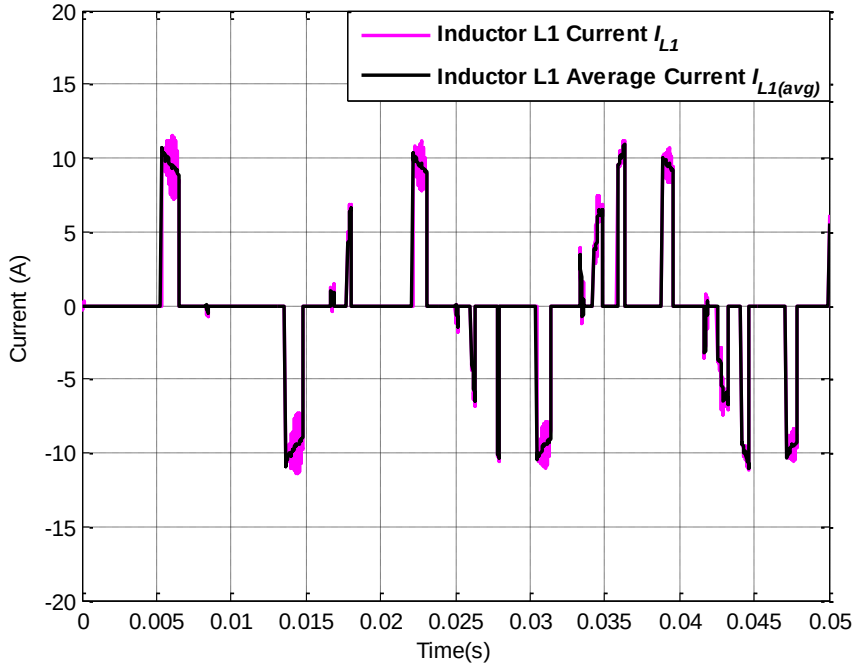

Figure A.48: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario xiii

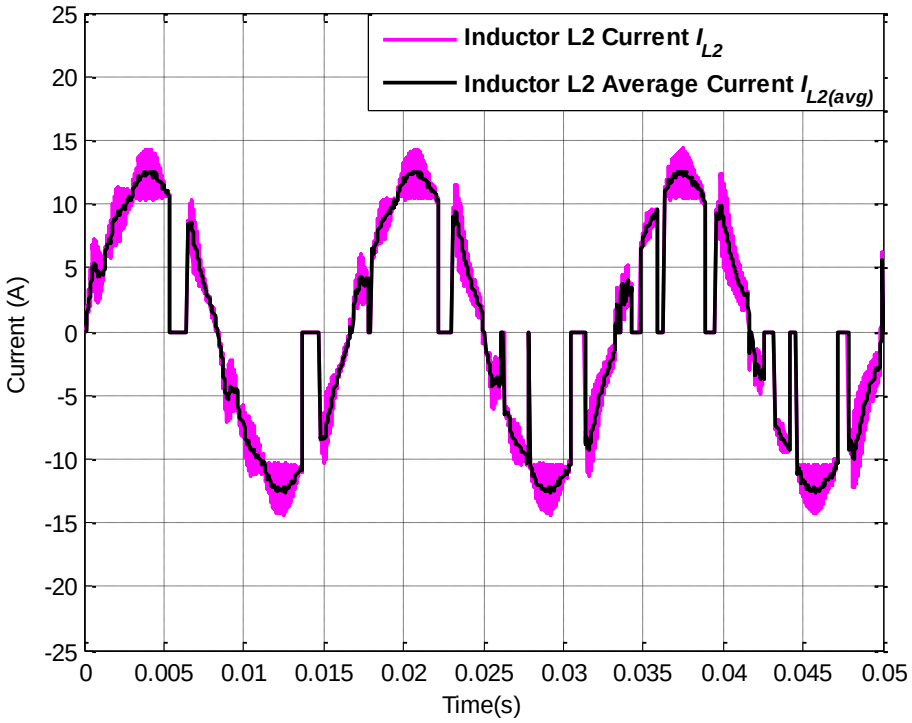

Figure A.49: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario xiii

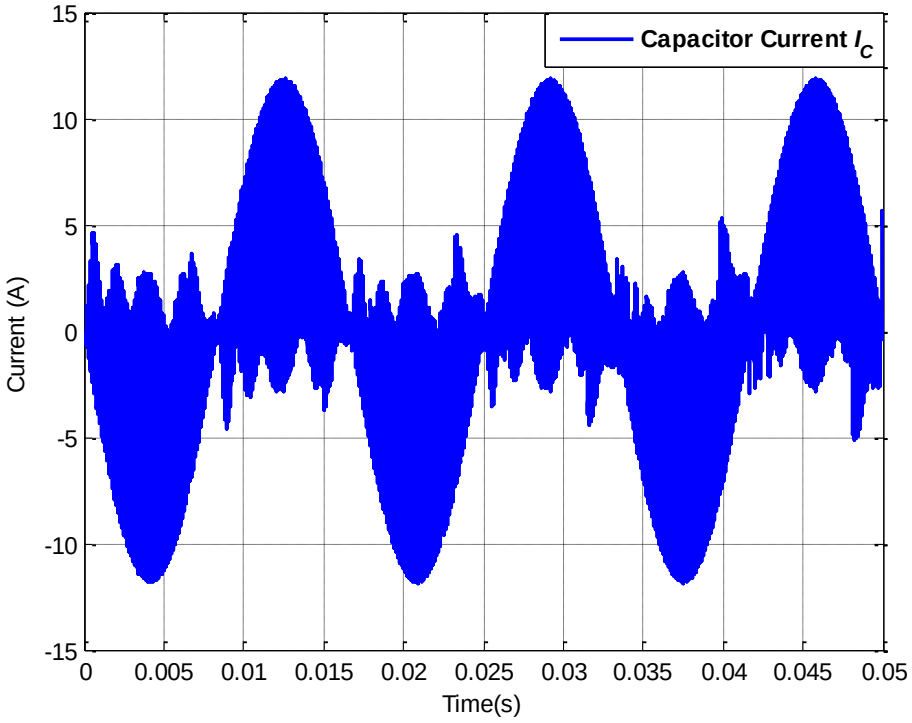

Figure A.50: Actual capacitor current I_C for operating scenario xiii

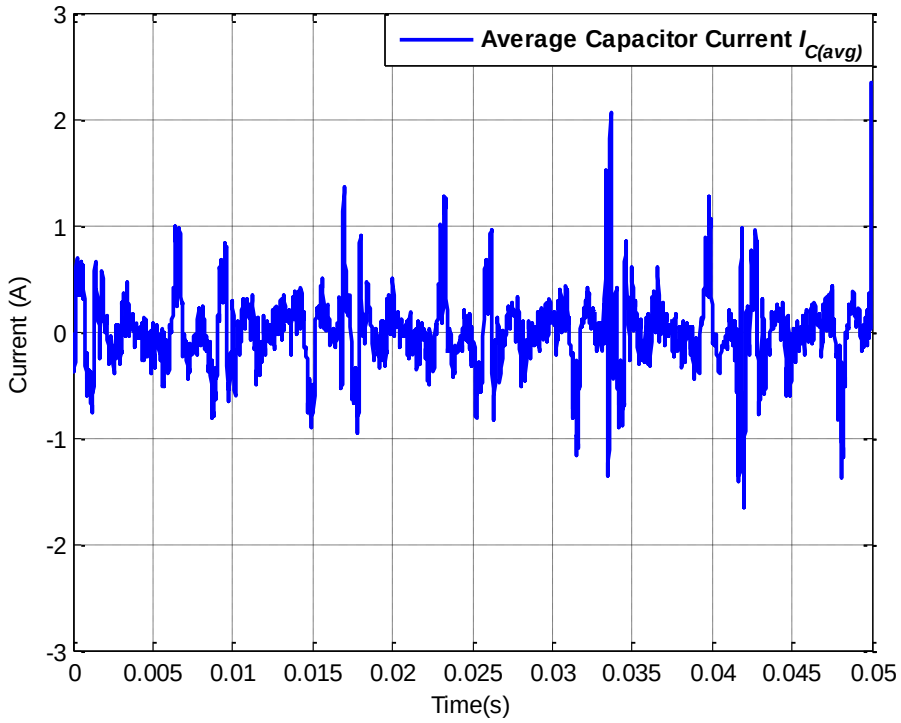

Figure A.51: Average capacitor current $I_{C(avg)}$ for operating scenario xiii

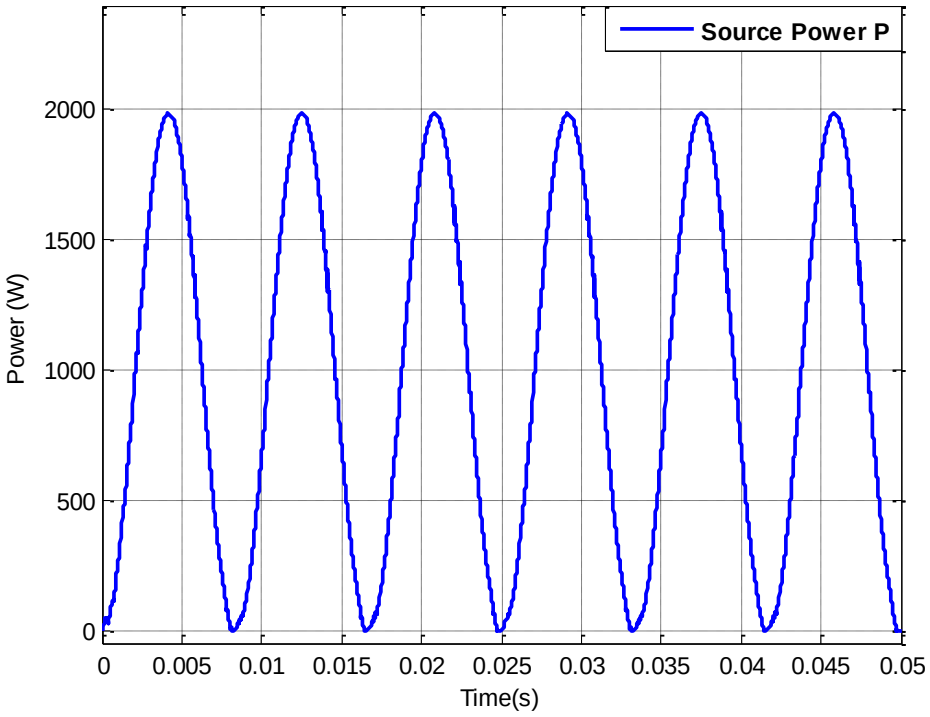

Figure A.52: Grid power for operating scenario xiii

A.3.11 Step change in load under normal conditions: Operating scenario xiv

Effects of step change in load under normal grid conditions are simulated and presented in this operating condition. The source voltage with no disturbance is presented in Figure A.53. The load is 14.4 Ω (1 kW) for time-period $0 \leq t \leq 0.0208$s whereas the load changes to 9.6 Ω (1.5 kW) at t=0.0208 seconds and continues till t=0.05 seconds. The working of modified AC-DVR is same as discussed in subsection A.3.1 such as bidirectional switches S1S2 and S3S4 remains open because duty cycle computed by controller circuit is zero as error voltage is zero for this case. Also, bidirectional switch S5S6 remains closed and thus, modified AC-DVR synthesizes almost zero voltage with some transients at t=0.0208s as depicted in Figure A.54. This voltage is added in series with source voltage, and as it can be seen in Figure A.55 that load voltage is same as source voltage with effects of load change at t=0.0208s.

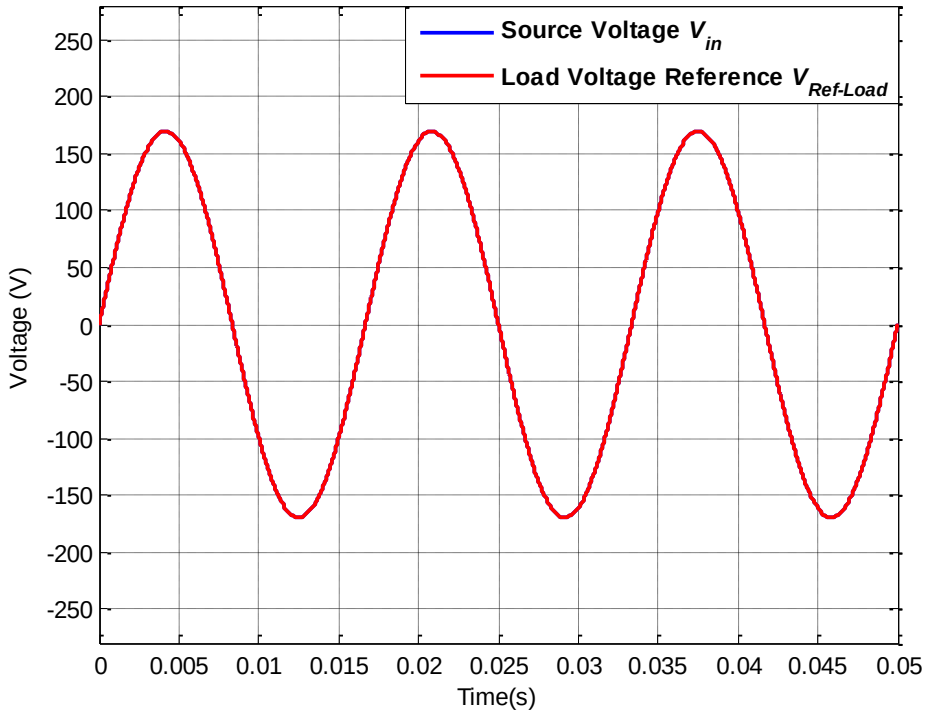

Figure A.53: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario xiv

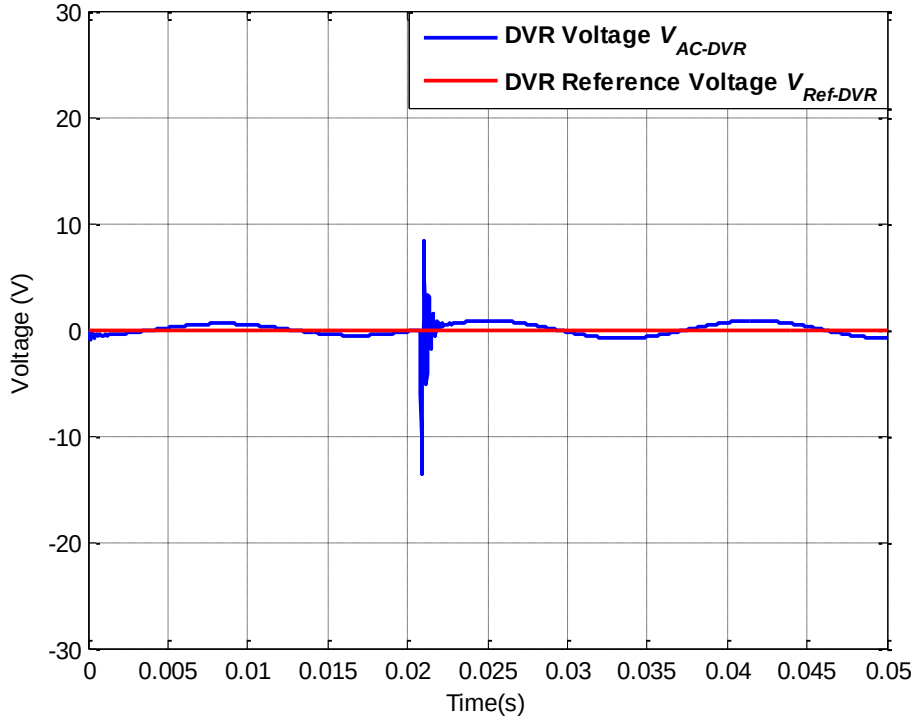

Figure A.54: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario xiv

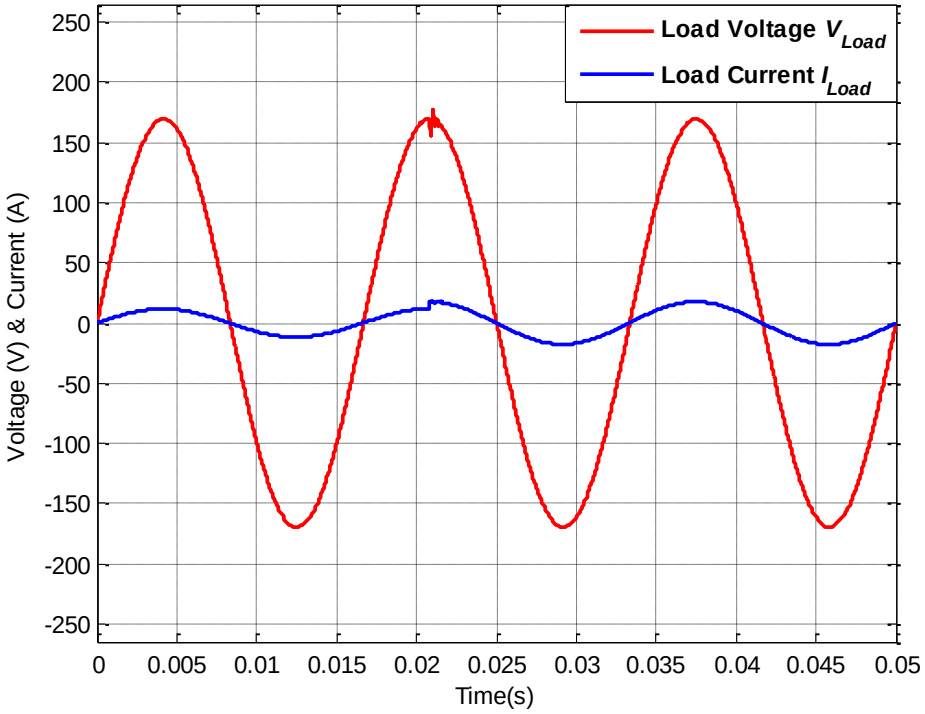

Figure A.55: Load voltage V_{Load} and load current I_{Load} for operating scenario xiv

A.3.12 Step load change under combined harmonic distortion: Operating scenario xv

The behavior of proposed DVR for step change in load under normal grid condition has been discussed and presented in previous scenario. In this operating scenario, performance of proposed DVR for step load change under combined harmonic and sag distortion is discussed and simulation results are presented. The parameters for the grid voltage are same as for scenario xii discussed in subsection A.3.9 such as 20% sag and harmonic voltage distortion at orders 3^{rd}, 5^{th}, 7^{th}, 11^{th} and 13^{th} with magnitudes of 10%, 11%, 6.25%, 2.5% and 2.5% with THD of 16.68%. The load is 14.4 Ω (1 kW) for time-period $0 \leq t \leq 0.0208$ and changed to 9.6 Ω (1.5 kW) at t=0.0208 seconds and continues till t=0.05 seconds. The source voltage is compared to 120V sinusoid reference as shown in Figure A.56 and error voltage is generated. The modified AC-DVR is operated with dedicated duty cycle to synthesize the error voltage and inductors/windings L1 and L2 are switched accordingly to utilize the source voltage in different polarities. The modified AC-DVR thus generates the voltage with desired magnitude and shape. The error voltage and output of modified AC-DVR are presented in Figure A.57. The error voltage generated by modified AC-DVR is injected in series with source voltage and load voltage is restored to 119.5V and 119.4V RMS with 1.83% and 2.5% THD for $0 \leq t \leq 0.0208$s and $0.0208 \leq t \leq 0.05$s respectively as depicted in Figure A.58. The actual and average source currents, AC-DVR input currents, inductor currents and capacitor currents are presented in Figures A.60-A.64. It can be observed that these currents are governed by their respective equations presented in chapter 4 and inductor currents are divided between two inductors L1 and L2. The source power is almost sinusoidal and changes to 1500 kW from 1000 kW at t=0.0208 seconds as shown in Figure A.65.

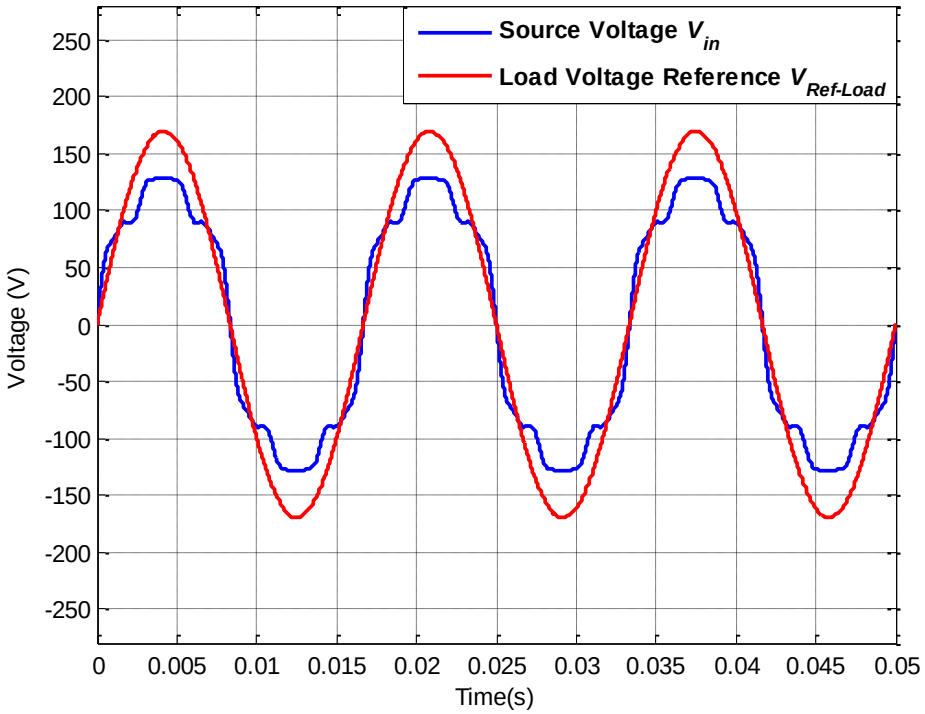

Figure A.56: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario xv

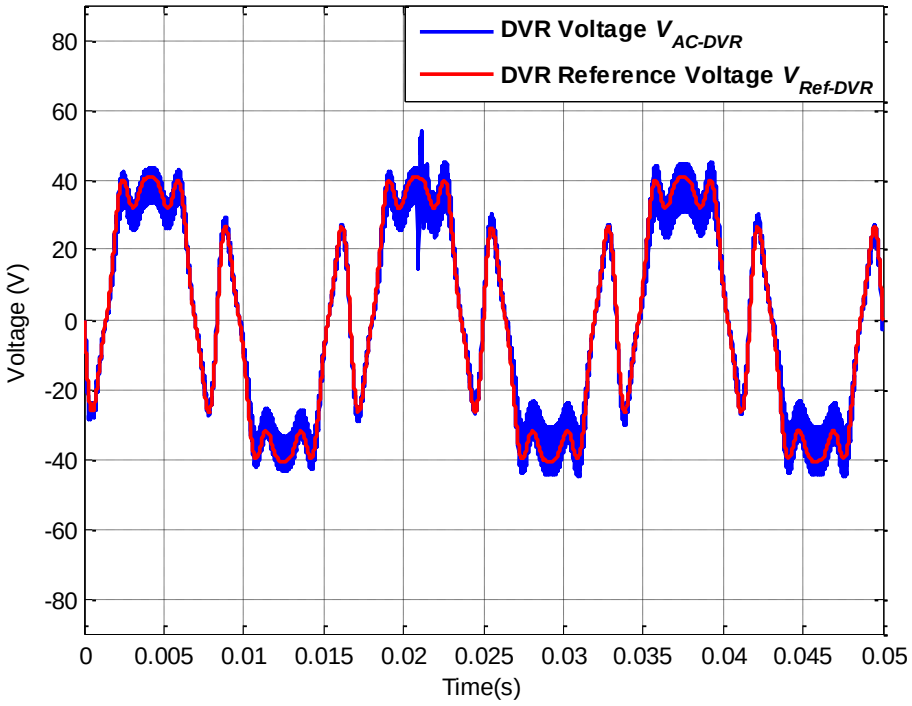

Figure A.57: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario xv

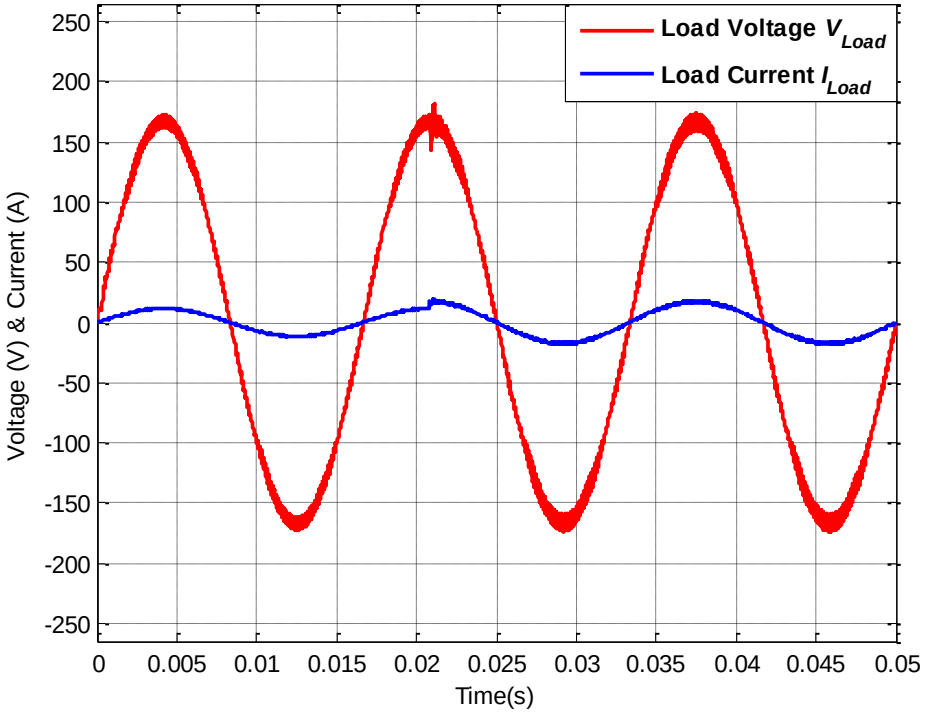

Figure A.58: Load voltage V_{Load} and load current I_{Load} for operating scenario xv

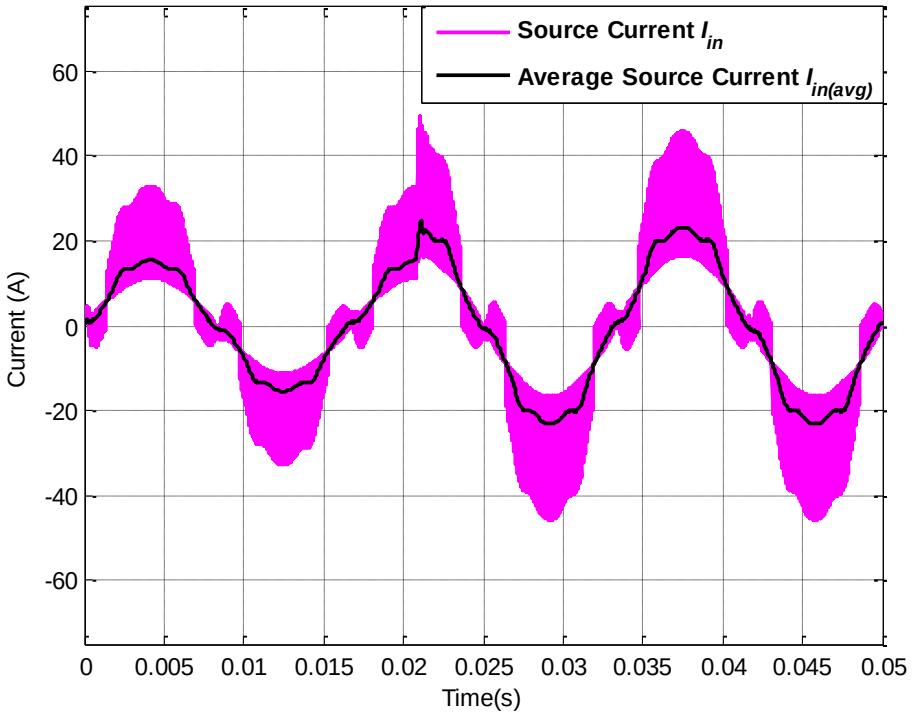

Figure A.59: Actual source current I_{in} and average source current $I_{in(avg)}$ for operating scenario xv

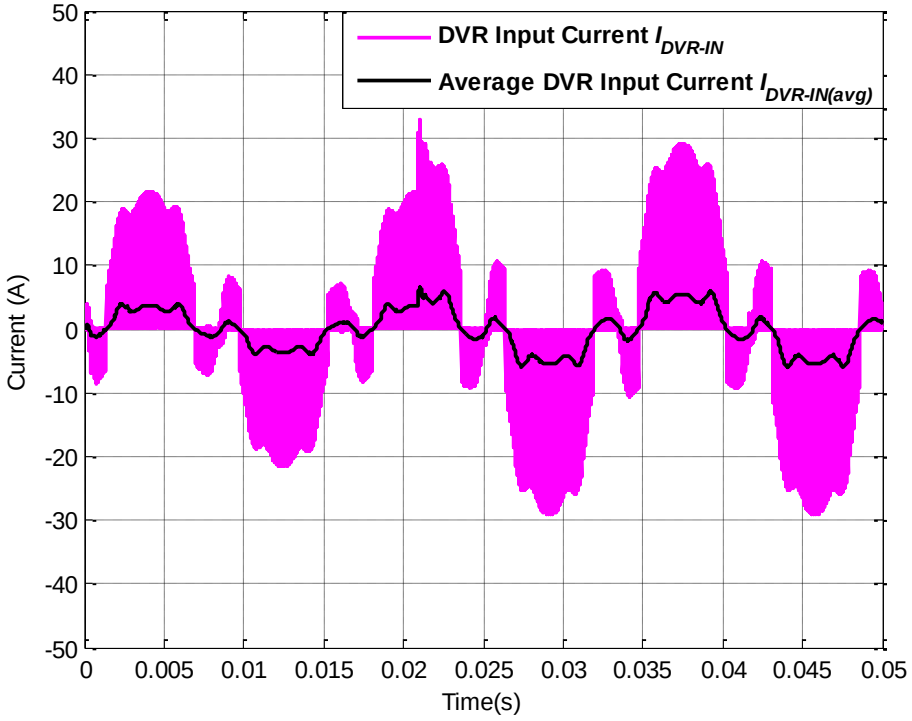

Figure A.60: Actual DVR current I_{DVR-IN} and average DVR current $I_{DVR-IN(avg)}$ for operating scenario xv

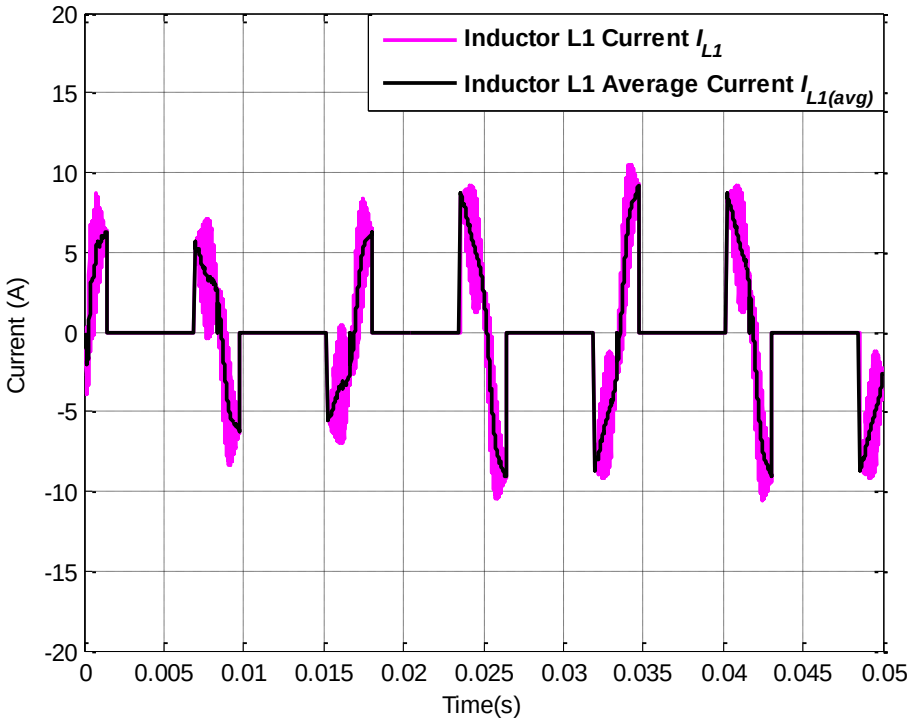

Figure A.61: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario xv

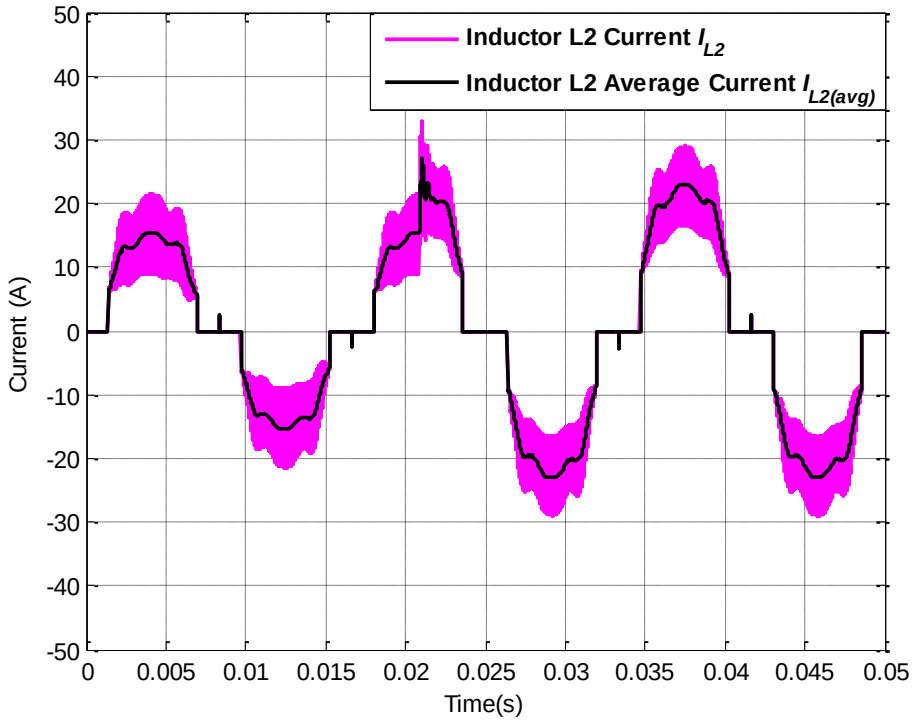

Figure A.62: Actual inductor current I_L and average inductor current $I_{L(avg)}$ for operating scenario xv

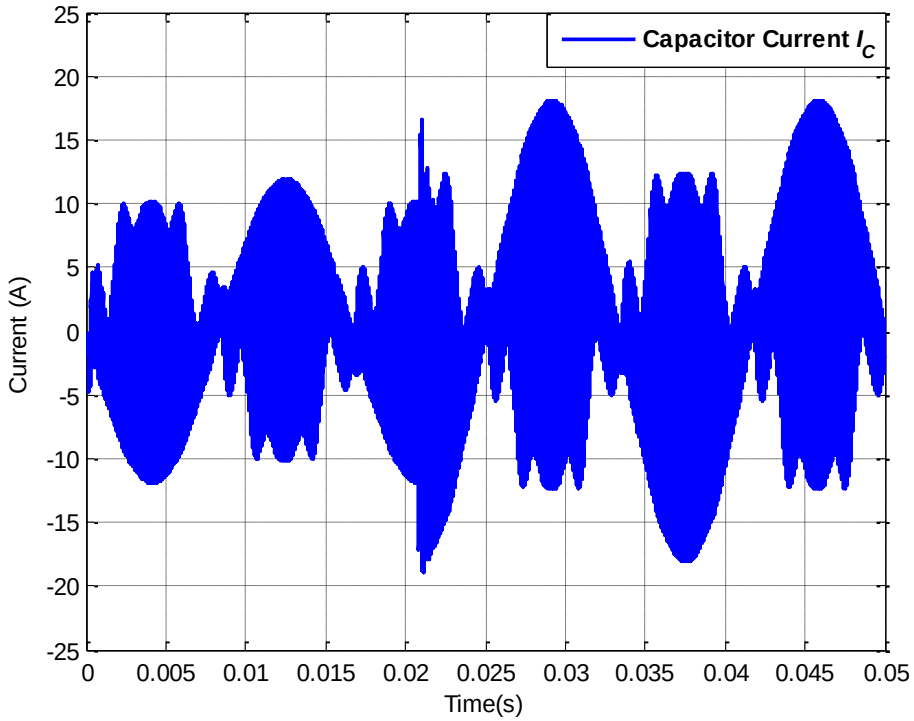

Figure A.63: Actual capacitor current I_C for operating scenario xv

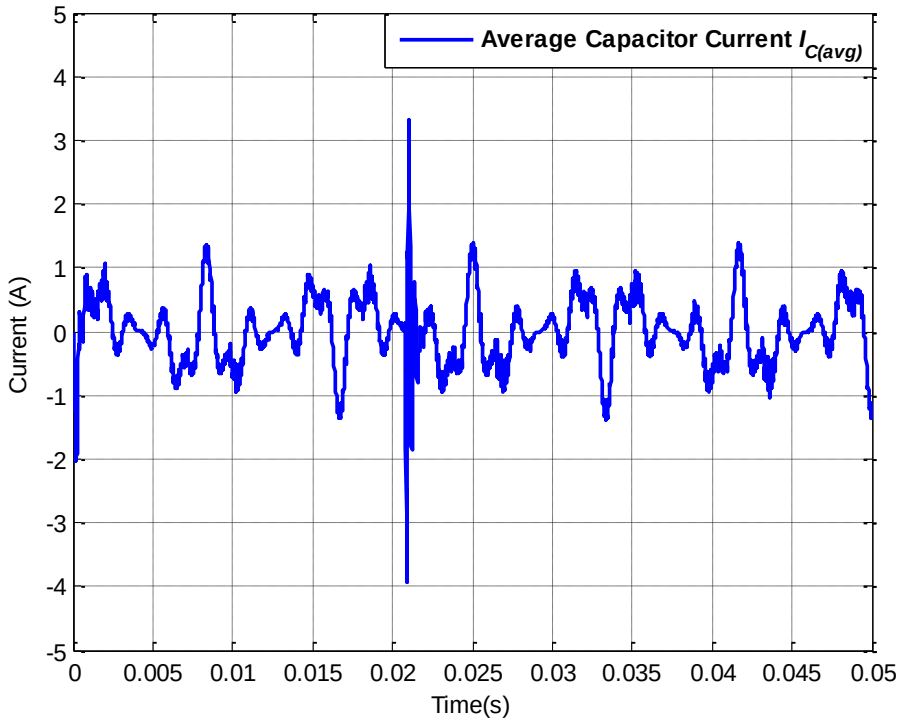

Figure A.64: Average capacitor current $I_{C(avg)}$ for operating scenario xv

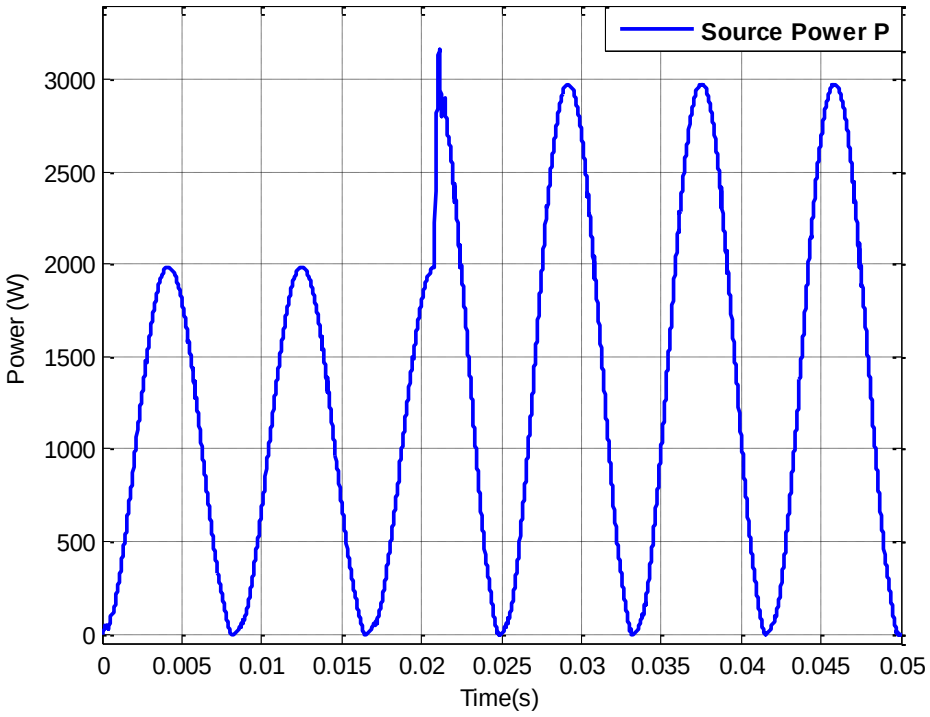

Figure A.65: Grid power for operating scenario xv

A.3.13 Step change in voltage swell: Operating scenario xvi

The simulations of AC-DVR for step change in load under various conditions were discussed and presented in previous scenarios. However, in this scenario simulations for step change in voltage swell have been performed. The source voltage experiences 20% voltage sag for 0 to 0.0208 seconds. At t=0.0208 second the swell is increased to 40% and continues till 0.05 seconds. The working of modified AC-DVR under this operating condition is same as discussed previously in subsection A.3.8. The simulation results for source voltage and modified AC-DVR voltage are presented in Figure A.66 and A.67 respectively. The load voltage is restored to 120.4V with 1.3% THD for $0 \leq t \leq 0.0208$s and 120.9V with 2.12% THD for $0.0208 \leq t \leq 0.05$s after having some transients at t=0.0208 second for couple of milliseconds as shown in Figure A.68.

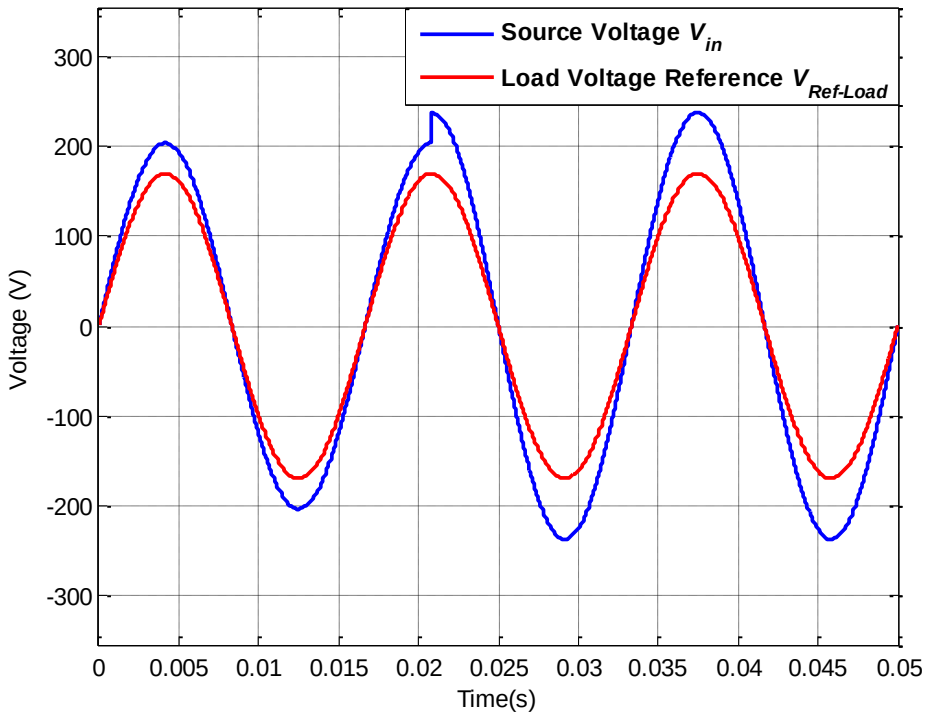

Figure A.66: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario xvi

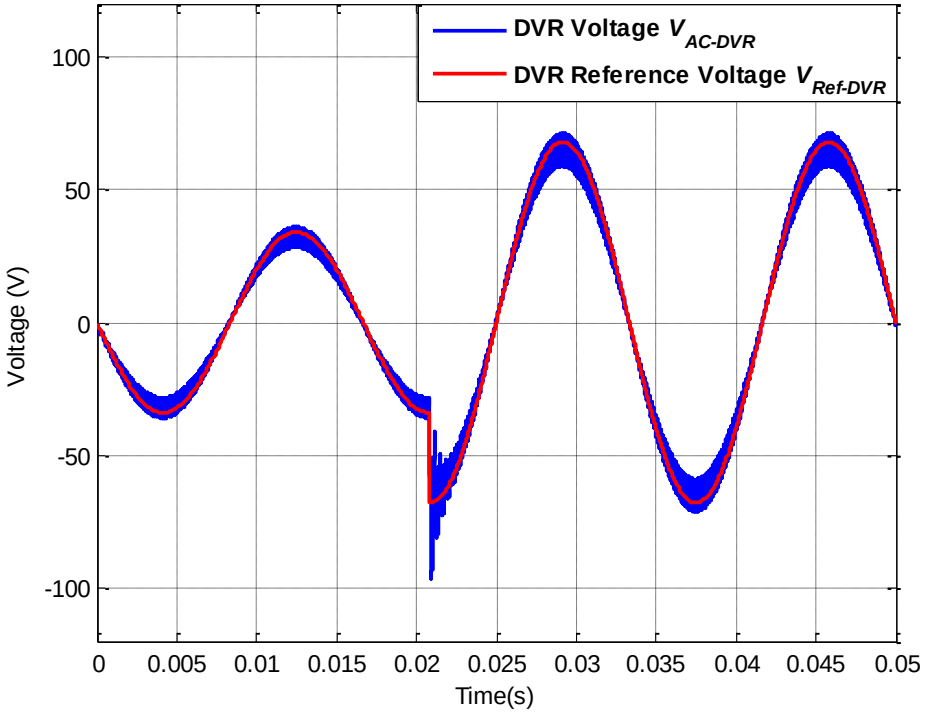

Figure A.67: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario xvi

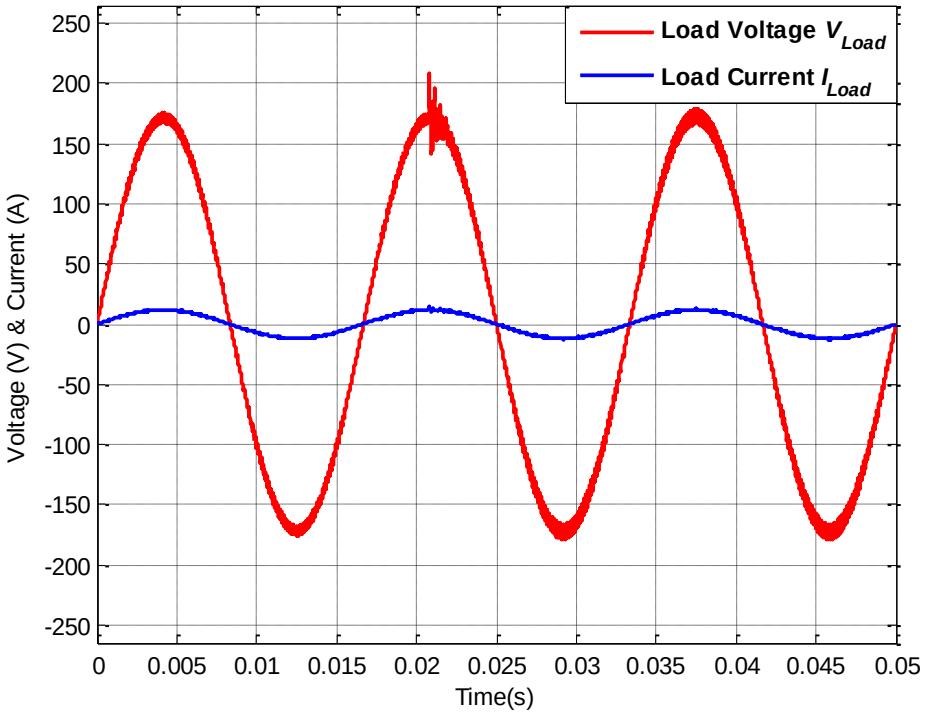

Figure A.68: Load voltage V_{Load} and load current I_{Load} for operating scenario xvi

A.3.14 Step change in harmonic distortion: Operating scenario xvii

Simulations with step change in voltage swell are presented and discussed in A.3.13. Likewise, in this scenario, source voltage comprises of 3rd harmonic voltage of 20% for time-period $0 \leq t \leq 0.0208$s and 5th harmonic voltage of 30% for $0.0208 \leq t \leq 0.05$s as shown in Figure A.69. The working of modified AC-DVR is same as discussed in subsections A.3.2 and A.3.3. The inductors/windings L1 or L2 are operated to utilize in phase or out of phase source voltage and AC-DVR operates under dedicated control to synthesize error voltage with desired magnitude, shape and phase. Simulation result for modified AC-DVR output voltage is depicted in Figure A.70. This voltage is injected in series with source voltage and load voltage is restored to 120V RMS with 1.34% THD for $0 \leq t \leq 0.0208$s and 119.9V RMS with 1.96% THD for $0.0208 \leq t \leq 0.05$s as shown in Figure A.71.

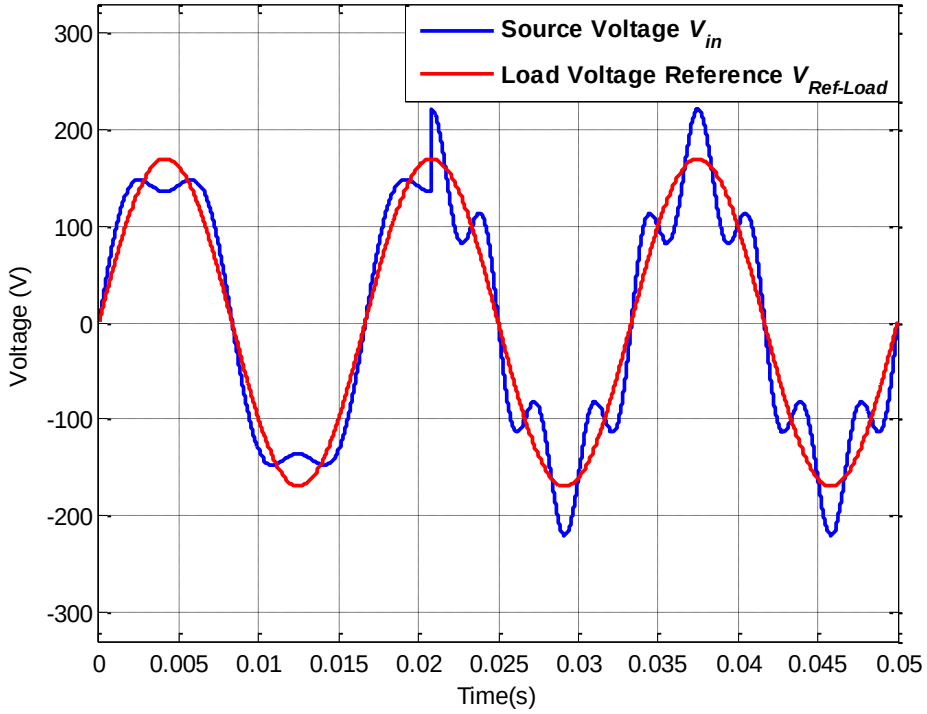

Figure A.69: Source voltage V_{in} and load reference voltage $V_{Ref-Load}$ for operating scenario xvii

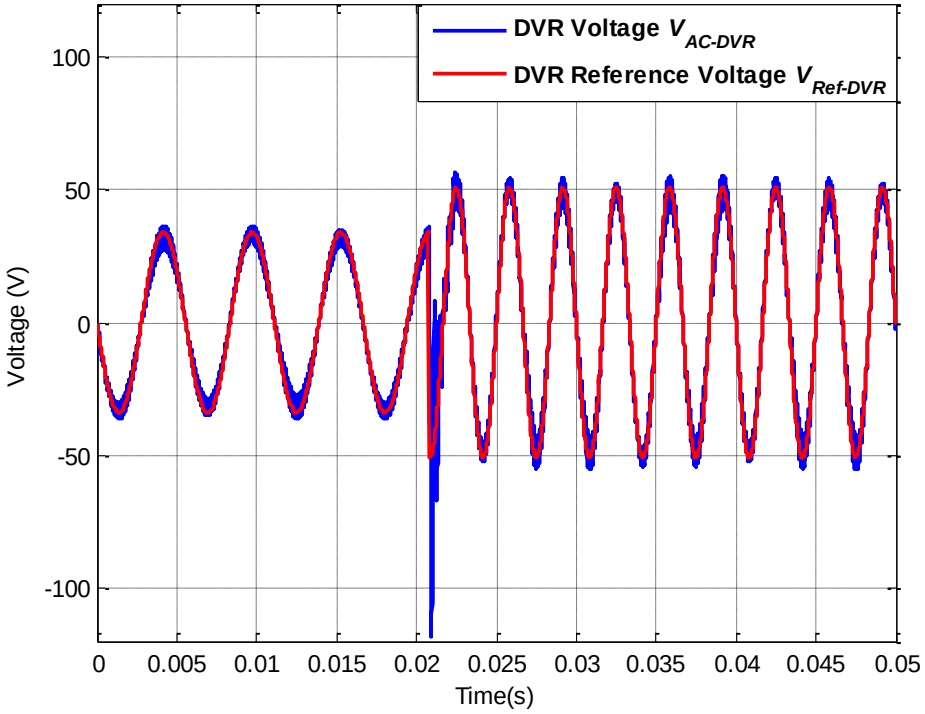

Figure A.70: AC-DVR voltage V_{AC-DVR} and DVR reference voltage $V_{Ref-DVR}$ for operating scenario xvii

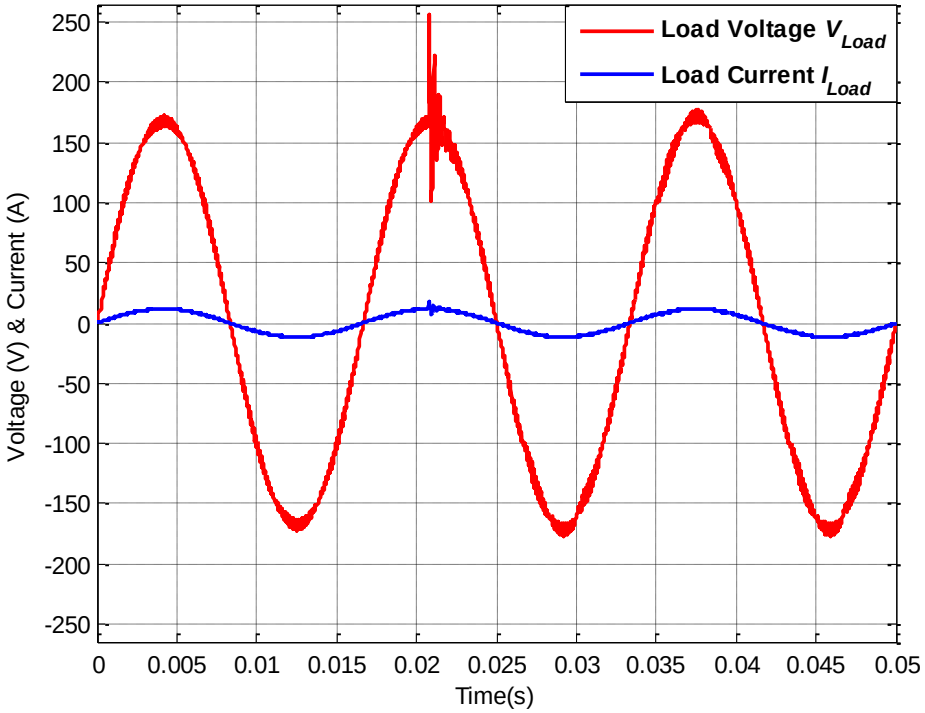

Figure A.71: Load voltage V_{Load} and load current I_{Load} for operating scenario xvii