INVESTIGATIONS, ANALYSIS, AND VALIDATION OF A NOVEL SYNCHRONOUS MACHINE EMULATOR WITH EMBEDDED DROOP CONTROL FOR GRID-FORMING AND GRID-CONNECTED INVERTERS

by

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ABSTRACT

PRITHWIRAJ ROY CHOWDHURY. Investigations, Analysis, and Validation of a Novel Synchronous Machine Emulator with Embedded Droop Control for Grid-Forming and Grid-Connected Inverters.

(Under the direction of DR. MADHAV MANJREKAR)

This dissertation proposes a novel control methodology for voltage (V_{PCC}) and frequency (ω) control at the Point of Common Coupling (PCC) while controlling the active power (P) and reactive power (Q) output of one as well as multiple Grid-Forming (GFM) Inverters. To achieve the goal of becoming self-operable and flexible, Distributed Energy Resources (DERs)-based inverters should be able to supply the power demand to the load as well as control the voltage and frequency at the PCC irrespective of the ambient conditions—the absence of the grid as well as in the grid-connected system. The dissertation presents a brief review of virtual inertia-based controllers, recently reported in the literature, for parallel-connected inverters in islanded systems. A new control topology, Synchronous Machine Emulator with Embedded Droop Control (SME-EDC) is proposed to control parallel-connected grid-forming as well as grid-connected inverters. This is designed to overcome the challenges in the future modern power grid consisting of large numbers of small-scale Distributed Energy Resources (DERs). It is estimated that the modern power grid will lack adequate grid inertia and will not have stiff grid reference for the DERs to follow using the existing methods like Phase-Locked Loop (PLL). The capabilities of the proposed controller are V_{PCC} and ω control of the inverters, auto-synchronization of the phases of the interfacing inverters without communication and without PLL, black starting the inverters without the presence of the grid, operating in the grid-connected system, controlling P and Q of inverter by droop control, and providing virtual inertia. The control philosophy of the proposed controller is established by rigid PCC voltage control by using capacitor current control. Whereas the auto

phase-synchronization is achieved by determining the phase-angle (θ_P) from the power controlling ω/P droop control. Simulation results from MATLAB/Simulink, and experimental results from the Control Hardware-in-the-Loop (CHIL) testbed and hardware experiment are presented to validate the capabilities of the proposed controller under various grid and load test cases.

DEDICATION

I dedicate this thesis to my beloved wife, Kabita, my parents, and my friends, whose unwavering love, support, encouragement, and motivation have been the bedrock of my research journey throughout graduate school. Your presence in my life is a blessing that I deeply treasure.

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LIST OF ABBREVIATIONS AND SYMBOLS

RERs	Renewable Energy Resources
PCC	Point of Common Coupling
SME-EDC	Synchronous Machine Emulator with Embedded Droop Control
CHIL	Control Hardware-in-Loop
ERs	Energy Resources
NRERs	Non-Renewable Energy Resources
PV	Photo Voltaic
V_{PCC}	PCC Voltage
f	Frequency
f_{SW}	Switching Frequency
ω, ω^*, $\omega_{nominal}$	Angular Frequency of the System, Reference Frequency and Nominal Frequency of Voltage
ω_m	Mechanical Speed of Rotor
ω_r	Virtual Rotor's Angular Speed
Θ	Phase Angle
IPC	Indirect Power Control
DPC	Direct Power Control
FPC	Flux Power Control

VISMA	Virtual Synchronous Machine
SMA	Synchronous Machine
CC-VISMA	Current Controlled Virtual Synchronous Machine
VC-VISMA	Voltage Controlled Virtual Synchronous Machine
VSG	Virtual Synchronous Generator
SSG	Static Synchronous Generator
CFC	Capacitor Feedback Current Control
VSI	Voltage Source Inverter
AVR	Automatic Voltage Restorer
SPWM	Sinusoidal Pulse Width Modulation
V_a, V_b, V_c	Three-Phase Voltage of Grid
V_a*, V_b* and V_c*	Reference Three-Phase Voltage of Grid
L_{ga}, L_{gb}, and L_{gc}	Grid Inductances
L	Filter Inductances
C	Filter Capacitance
R	Resistance
X	Reactance
V_{DC}	DC voltage of Battery

E_a, E_b, E_c	Three-Phase Inverter Output Voltages
E_d, E_q	D and Q-Axis Inverter Output Voltages
E_{ref}	Reference Inverter Output Voltages
P_{PCC}, Q_{PCC}	Active and Reactive Power at PCC
P^*, Q^*	Reference Active and Reactive Power
$P_{nominal}$, $Q_{nominal}$	Nominal Active and Reactive Power
I_d, $I_{q,}$	D and Q-Axis Currents
V_d, V_q	D and Q-Axis Voltages
I_d^*, I_q^*	Reference D and Q-Axis Currents
V_d^*, V_q^*	Reference D and Q-Axis Voltages
I_{PCC}	PCC current
PLL	Phase Lock Loop
PI	Proportional Integral
DSP	Digital Signal Processing
ΔP, ΔQ	Error Components of Active and Reactive Power
dp, dq	Binary Error Status in Space Vector
V_0-V_7	Switching Vectors
s_1-s_{12}	12 Sectors in Space Vector

S_a, S_b, S_c	Three phase switch Inverter Legs
S_1- S_6	6 switches of the Inverter
$\tilde{P}$, $\tilde{q}$	Instantaneous Active and Reactive Power
$\|\psi\|$, δ	Flux magnitude and angle in General
$\|\psi_E\|$, δ_E	Inverter Output Flux Magnitude and Angle
ψ_E*, δ_E*	Reference Inverter Output Flux Magnitude and Angle
$\|\psi_V\|$, δ_V	Flux Magnitude and Angle of PCC voltage
δ_p	Power Angle
P_{elect}, T_{elect}	Electrical Output Power and Torque
T_{mech}, T_{mech}*	Mechanical Torque and Reference Mechanical Torque
J	Rotor Inertia
B	Damping Factor for VISMA
D	Damping Factor for SWING-VSG
M_f	Mutual Inductance between the Field Coil
I_C*	Feed-Forward Capacitor Current
iC	Measured Capacitor Current
E_ff	Feed-Forward Voltage
K_C	Proportional Constant for Capacitor Current

K_f	Inner Loop Frequency Droop Constant
K_p	Proportional Constant
K_i	Integral Constant
D_p	ω/P *Droop Constant*
D_q	V/Q Droop Constant

CHAPTER 1: INTRODUCTION

1.1. Introduction

In the era of ever-increasing awareness of climate change and the associated higher penetration of inverter-based renewable resources, a complete and optimally designed control scheme for controlling grid-following [1-4] as well as parallel-connected inverters [5-8] in the islanded system is highly desired. RERs, which are modeled as DC Voltage Sources alongside the conventional AC sources, can be seen in the present and future power grid as in Figure 1.1.

Soon, fossil fuel-powered, and synchronous generator-based power generations might become functionally obsolete because of greenhouse gas emissions and the gradual exhaustion of fuel [9-11]. Consequently, the power grid might not remain in the communication-based centralized structure for long. Instead, it will be distributed in nature and more interoperability and flexibility are expected in the inverter-dominated modern power grid [12] as shown in Figure 1.2. Designing

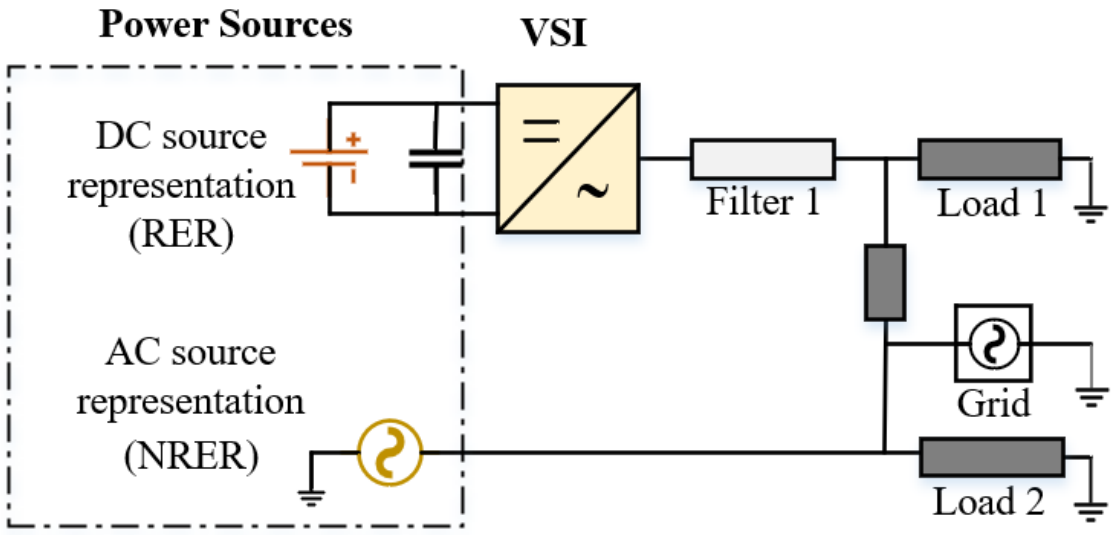


Figure 1.1. Energy resources connected to the grid through the inverter

grids consisting of mostly inherently inertia-less inverters and without rotating machine-based power supply is a current challenge for power electronics engineers. As the Grid-Forming (GFM) inverter [8, 13-15] lacks rotating inertia and damping, it may face transients during disturbances in loads without a proper controller. Furthermore, the PCC voltage may get unstable or the time to reach steady-state might get long which may be critical to some sensitive loads in the system [10].

The future grid (Figure 1.2) will consist of mostly a large number of small scaled DERs [16]. These DERs will form grid, interact with other DERs, operate in islanded mode as well as grid-connected mode. Currently, the voltage and frequency are rigidly maintained at their fixed values by the large synchronous generators powered power system where some connected DERs follow the grid by a PLL and supply excess power or receive required power from the grid.

However, in the future grid, the concept of a fixed frequency and voltage will also be controlled by the DERs in addition to balancing the generated, and load power. In that scenario, the power

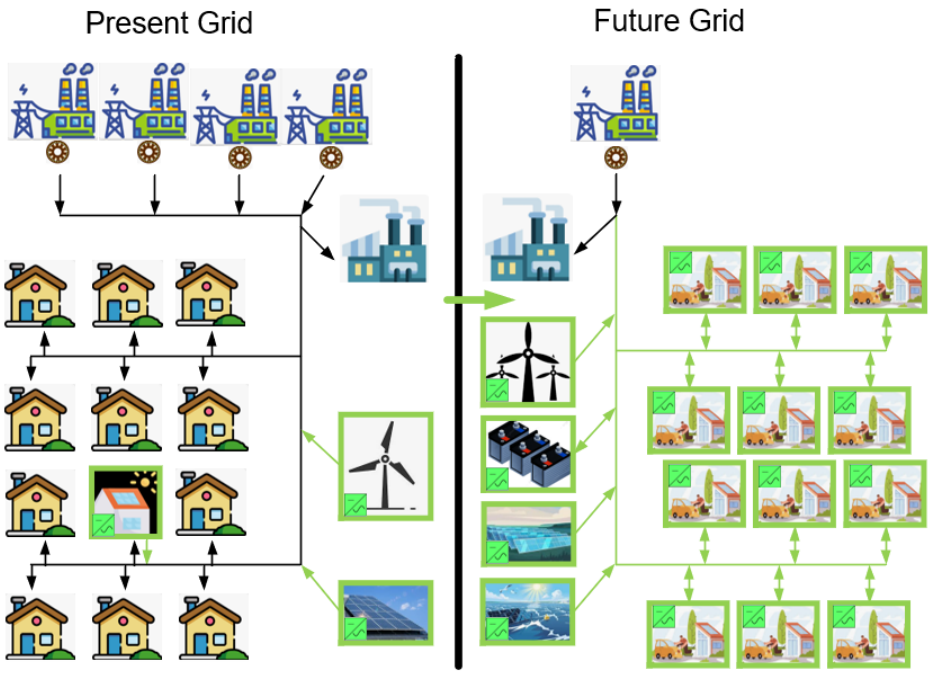


Figure 1.2. Energy resources connected to the grid through the inverter

control architecture by a pre-determined reference frequency and voltage will not be wise. The concept of power control and load share by droop control will be a new norm.

The following 5 terms need to be controlled at any conditions for a stable and flexible system. These are *voltage control*, *frequency control*, *active power control*, *reactive power control* and *phase-synchronization*.

Towards solving these problems, the novel control, Synchronous Machine Emulator with Embedded Droop Controller (SME-EDC) is proposed in this paper to control the 3-phase GFM inverters. Here, the virtual-inertia and damping are integrated just like a Virtual Synchronous Machine (VISMA) controller [17, 18] and Virtual Synchronous Generator (VSG) [19] controller to follow the dynamics of the synchronous generator (SG) by the inverter. By measuring and controlling the filter capacitor current, the PCC voltage can be accurately controlled [20, 21]. Also, by doing so, more resiliency against load disturbances is expected to be achieved [22, 23]. The frequency (*f*) and voltage (*V*) droop characteristics of the load are integrated into the proposed controller to allow it to react to the load changes according to the pre-determined rate. Furthermore, the nominal frequency and voltage references are designed in the droop control loops to operate the controller under the condition of black-start. It is estimated that the controller will be more secure and reliable as it will not have any real-time communication as found in the conventional PLL-based control schemes[24, 25]. Some PLL-less inverter synchronization techniques are shown the literatures [26-28]. The performances of the developed controller are analyzed under various load and grid conditions, including uneven loading, and load disturbance with as well as without the presence of the grid. The objective of the simulations and experiments are to determine if it can satisfy all the desired criteria of a complete GFM inverter controller. Finally, the controller

is validated by Controller in Hardware in Loop (CHIL) [29] and hardware experiments to validate the concept.

1.2. Contribution and Thesis Outline

The following are the thesis contributions.

A. Accurately control the PCC voltage and frequency of the inverters accurately by controlling the capacitor feedback current

B. Auto-synchronize the phase of the voltage of the parallel-connected inverters and grid-connected without communication by implementing virtual inertia

C. Black start the inverters in the absence of other inverters or the grid

D. Seamless transition between grid-forming and grid-connected mode of inverter control

E. Control load sharing in multiple parallel-connected inverters system by droop control

The thesis document is organized in the following manner. In this document, the introduction is presented in “Chapter 1”. The power electronics test setup and review of the controllers for grid-forming and grid-connected inverters are described in “Chapter 2”. “Chapter 3” describes the operating principle of the proposed controller, SME-EDC. “Chapter 4” contains the comparison of the proposed controller with PLL, classical VISMA-based controls, and Droop controls. “Chapter 5” describes the auto phase-synchronization technique by the 3-layered control of SME-EDC. Technical discussions of the simulated and experimental results are included in “Chapter 6”. Hardware results are presented in “Chapter 7”. Finally, “Chapter 8” presents the conclusions and future works of the thesis.

CHAPTER 2: LITERATURE REVIEW OF CONTROLLERS FOR GRID-FORMING INVERTERS

2.1. Description of the Power Electronics Test Setup

The performance of the proposed controller for controlling parallel-connected three grid-forming (GFM) as well as grid-connected inverters is analyzed in the power electronic setup shown in Figure 2.1. In this scheme, each of the 3-leg 3-phase inverters has an ideal voltage source on the DC side and the AC side is connected to the power grid via corresponding LC filters, breakers and line impedances. Here, the grid is represented as a three-phase voltage source in series with grid

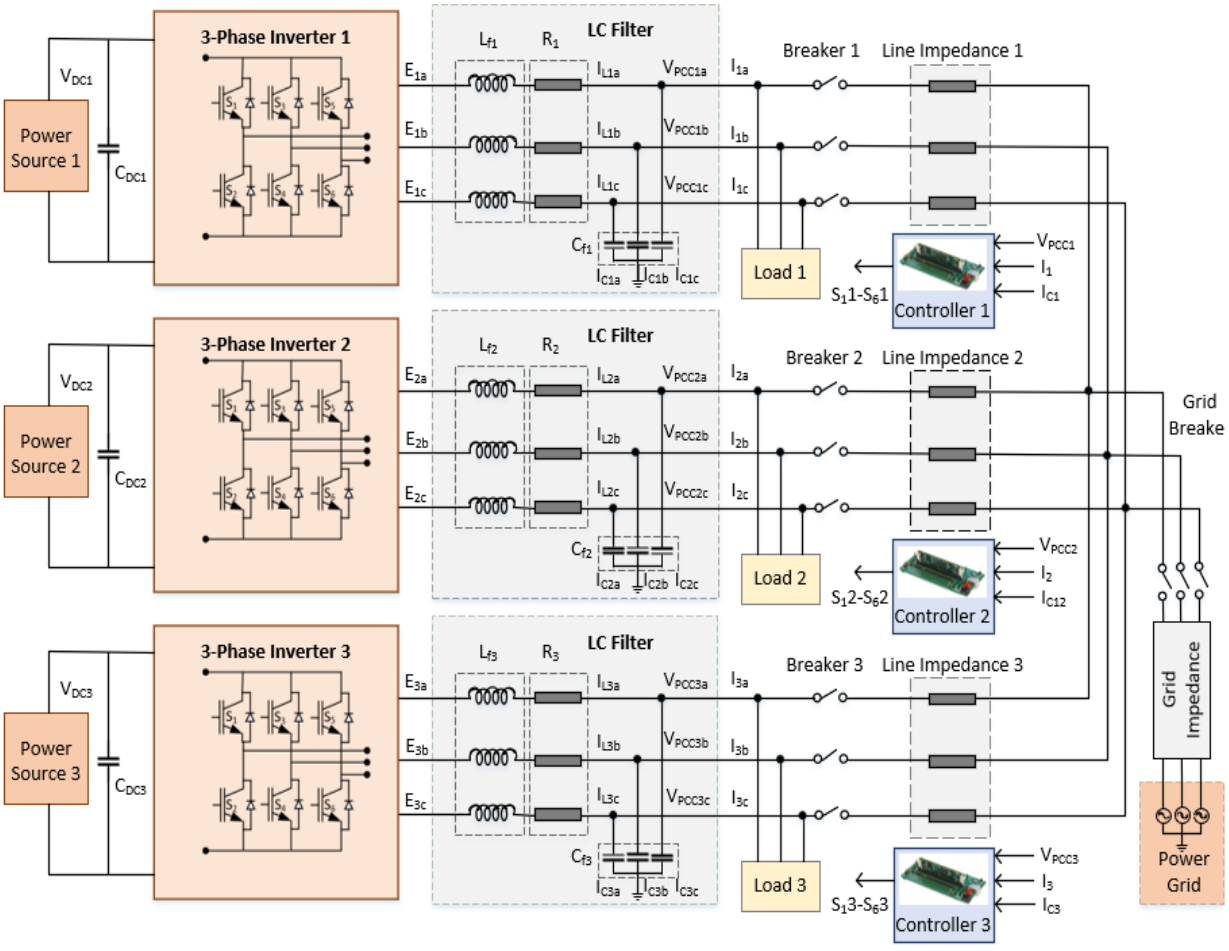


Figure 2.1. Schematic Diagram of the three parallel-connected grid-forming inverters

inductances L_{ga}, L_{gb}, and L_{gc}. Grid-disconnected and grid-connected systems can be built by opening and closing the grid-breaker respectively. Breaker-1, 2 and 3 are kept 'closed' in the base case. Here, magnitudes of grid inductance represent a strong or weak grid. The inverter output voltages are denoted by E_a, E_b, and E_c whereas, the PCC voltages (after filters) are denoted by V_{PCCa}, V_{PCCb}, and V_{PCCc}. The block 'Power Source' represents any DERs such as a photovoltaic array, battery storage systems, etc., and its voltage, V_{DC} is 1000 V. The Loads-1, 2 and 3 are selected such that the active power (P) and reactive power (Q) are 100 kW, and 100 kvar, respectively under the nominal PCC coupling voltage, V_{PCC}=480 $V_{ll,rms,}$ and nominal grid frequency, f=60 Hz. In the parallel-connected inverters system, these nominal values V_{PCC} and f are taken as reference parameters. The filter inductance, L=1 mH, has been chosen (with approximately 0.2 p.u. equivalent impedance). Grid inductance, L_g=0.2 mH (0.03 p.u. impedance), has been chosen. In the islanded system, the filter capacitor, C=25 uF, is chosen. The primary objective in the islanded system is to stabilize the V_{PCC} and f in the PCCs of each inverter while providing the load requirements by the respective controllers.

2.2. Review of Controllers for Grid-Following and Grid-Forming VSIs

2.2.1. Indirect Power Control (IPC)

In the IPC architecture, the current is controlled indirectly as explained in [30] and hence it is named as indirect power control scheme as shown in Figure 2.2. The controller is designed in the synchronous reference frame. Here, the direct axis current (I_d) and voltage (V_d) components and the quadrature axis current (I_q) and voltage (V_q) components are determined based on transformation, as in [31], from the measured PCC voltage (V_{PCC}) and current (I_{PCC}).

Control q-loop and d-loop equations are as follows,

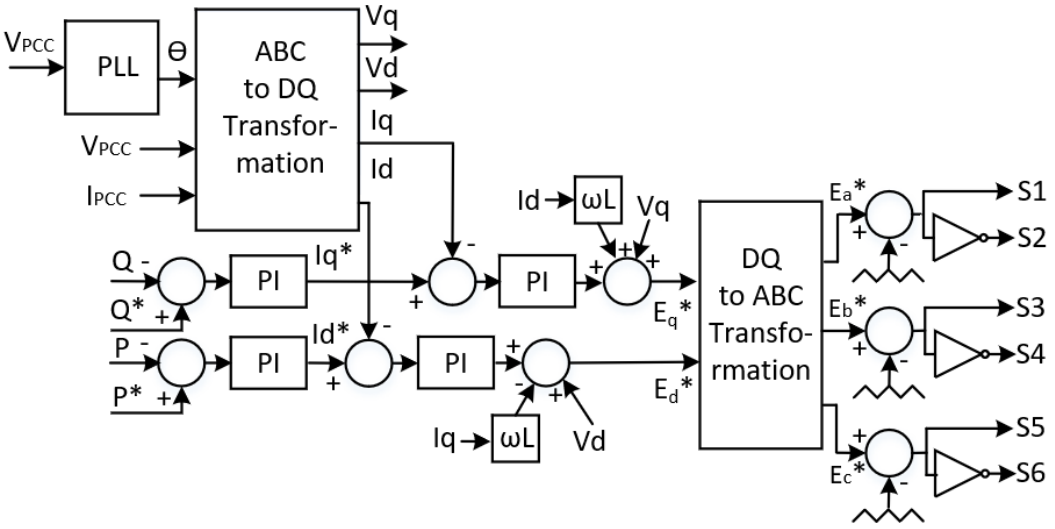


Figure 2.2. Simplified block diagram of IPC

$$V_q^* = V_q + XI_d + [(K_P + K_I \frac{1}{s})(I_q^* - I_q)] . \quad (2.1)$$

$$V_d^* = V_d - XI_q + [(K_P + K_I \frac{1}{s})(I_d^* - I_q)] . \quad (2.2)$$

There are two control loops running in parallel. Each of them contains 1. Outer *P* and *Q* regulation loops that produce reference direct and quadrature axis current I_d* and I_q* respectively from the errors (P*-P_{PCC}) and (Q*-Q_{PCC}), and then feed them to the inner loops; 2. Inner current loops produces control signals V_d* and V_q* from I_d, I_q, I_d*, I_q*, V_d and V_q using equations (2.1) and (2.2). V_d* and V_q* are then transformed into the ABC frame to get reference voltage V_a*, V_b* and V_c*. After that, this reference voltage is compared with a repeating triangular wave (that makes the switching frequency, f_{SW}=10 kHz to generate the PWM signal to drive the inverter switches). As V_{PCC} is a fixed variable in the grid, the power flow through the inverter is inherently controlled by continuously tracked by the Phase Lock Loop (PLL) and controlled by the current magnitude and phase. The transient during the power control is controlled by the PI control inside this controller. This controller undergoes through Digital Signal Processing (DSP) and progresses by one step-

delay in the instantaneous power measurements to account for the controller's impact from the errors calculated in the previous step. This controller design is inspired from the three-layer control architecture [32].

2.2.2. Direct Power Control (DPC)

P_{PCC} and Q_{PCC} are directly controlled via directly deriving the switching states by the switching table (Table I). Hence, the control scheme is named as Direct Power Control (DPC). The DPC scheme was first proposed in [33], as shown in Figure 2.3. Here, 12 space vector sectors, are derived from the V_{PCC} waveform after αβ transformation [34, 35], as shown in Figure 2.4. Error signals ΔP (=P*-P_{PCC}) and ΔQ (=Q*-Q_{PCC}) results in binary error status *dp* and *dq* respectively by hysteresis implementation. In the consequence, the f_{sw} is not constant (<83 kHz). Finally, *dp*, *dq* and the position of the space become the inputs by the switching table as shown in Table I [11]. The objective is to calculate the switching states of all 6 switches of the 3-leg VSI for regulating P_{PCC} and Q_{PCC}.

Here, the numbers, 0 to 7 in the Table I are switching vectors (V_0-V_7), denote the binary switching states of the 3-legs of the inverter in the domain of the space vector as shown in Figure

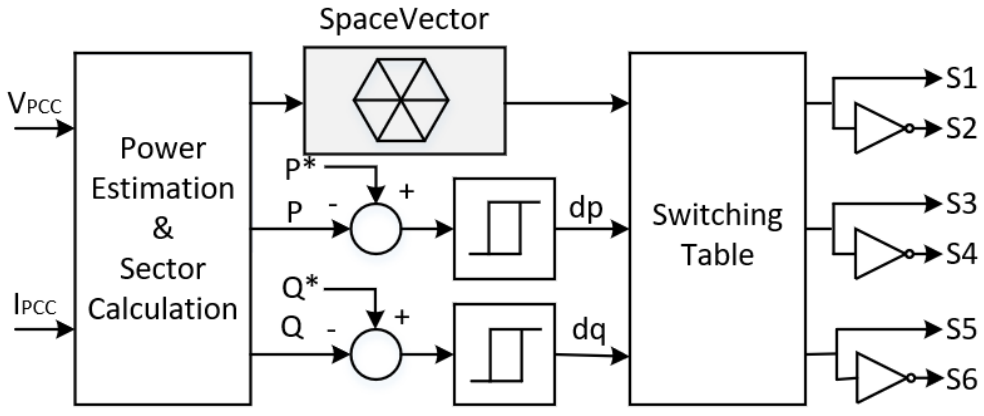


Figure 2.3. Simplified block diagram of DPC

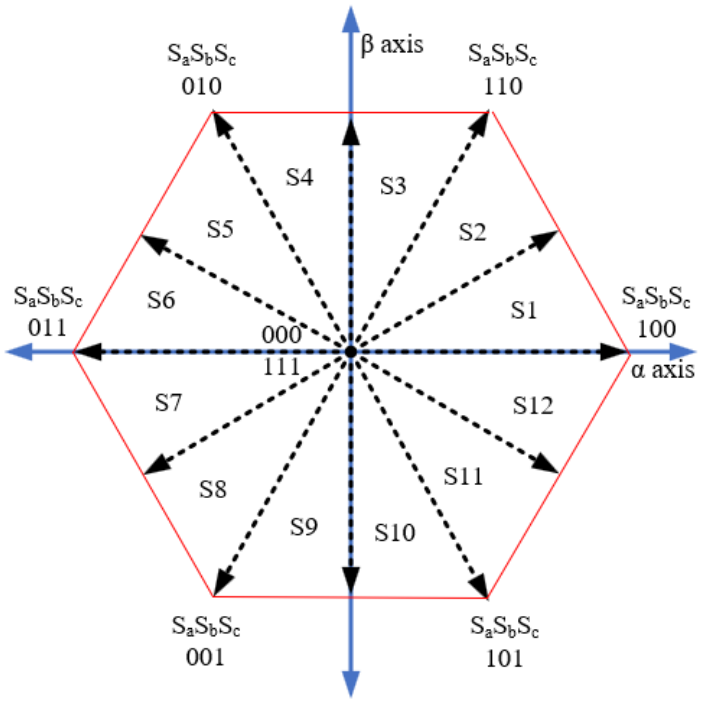


Figure 2.4. Space vector and 12 sectors in the αβ plane

2.4. We have divided the space vector into 12 equal sectors (s_1-s_{12}) instead of 6 sectors to get a double sampling of the instantaneous active and reactive power error *dp* and *dq* respectively so that the steady-state condition is achieved quickly.

TABLE I
SWITCHING TABLE FOR DPC AND FPC

***dp*, *dq* error status**		**Switching status according to the sector location**											
dp	***dq***	***S1***	***S2***	***S3***	***S4***	***S5***	***S6***	***S7***	***S8***	***S9***	***S 10***	***S 11***	***S 12***
1	**0**	6	7	1	0	2	7	3	0	4	7	5	0
1	**1**	7	7	0	0	7	7	0	0	7	7	0	0
0	**0**	6	1	1	2	2	3	3	4	4	5	5	6
0	**1**	1	2	2	3	3	4	4	5	5	6	6	1

Switch legs are denoted by Sa (S_1+S_2), S_b (S_3+S_4) and S_c (S_5+S_6) and it can be either 0 or 1, where 1 means only the upper switch of that leg is closed and 0 means only the lower switch of that leg is closed. So, 1 and 0 signify that positive and negative voltage are provided respectively by that corresponding phase leg at that instant. By the 3-leged 6 switches of the inverter, there are total 2^3=8 numbers of possible switching combinations. Different instantaneous power is injected to the grid according to the positions of the switches. The states, 000 and 111 do not provide useful voltage to the grid but work as 3rd harmonics eliminator in this power control.

The relationship between instantaneous active power, $\tilde{p}$ and switching states of the leg, $S_aS_bS_c$ by this scheme are following.

$$\tilde{p} = L(\frac{dI_a}{dt} I_a + \frac{dI_b}{dt} I_b + \frac{dI_c}{dt} I_c) + p(-1)^n V_{DC} I_x \,. \tag{2.3}$$

Where, n =0, if only one of the binary digits $S_aS_bS_c$ is 1,

=1, elsewhere.

p =0, if S_a=S_b=S_c,

=1, otherwise.

And, I_x =the corresponding phase leg-current (where, x can be a, b or c), also the status of which is dissimilar from the other two phase-legs in the space vector.

The relation between instantaneous reactive power, $\tilde{q}$ and switching states of the legs, $S_aS_bS_c$ are.

$$\tilde{q} = \frac{1}{\sqrt{3}}[3 * L(\frac{dI_x}{dt} I_y - \frac{dI_y}{dt} I_x) + p(-1)^n V_{DC}(I_y - I_x)] \cdot \tag{2.4}$$

Where,

n =0, if only one of the binary digits $S_aS_bS_c$ is 1,

=1, elsewhere.

p =0, if S_a=S_b=S_c,

=1, otherwise.

And, I_y, I_x =the corresponding phase leg's current (where, *x*, *y* can be *a*, *b* or *c*), status of which are the same to each other in the space vector.

Power quality can be improved by applying this controller as experimented in [36] as transients in controlling *P* and *Q* have been effectively controlled in this scheme. And other applications of DPC scheme in renewable power system is validated in [37-39].

2.2.3. Flux-based Power Control (FPC)

The control scheme is named FPC, because the inverter flux is internally calculated in this power control architecture. This control scheme was first proposed in [40] and in [41], as shown in Figure 2.5. This control scheme is somehow similar to DPC, especially regarding sector calculation and switching table development. But, both inverter voltage (*E*) and V_{PCC} are measured and integrated to get the equivalent inverter flux magnitude $|\psi|$ and angle (δ) for both the backend (back emf) and inverter output in this scheme. The power angle δ_p, as in (10), determines the active power flowing through the filter inductor, also it is affected by the fluctuation of *P*. Similarly, the inverter output flux $|\psi_E|$ determines the reactive power injected into V_{PCC}. Two PI controllers generate the reference signals δ_P* and ψ_E* from the calculated errors ΔP (=P*-P_{PCC}) and ΔQ (=Q*-Q_{PCC}) respectively from the generalized equations (2.5) and (2.6). After that, *dp* and *dq* are generated by hysteresis control. And hence, f_{sw} is also constant (<83 kHz) in this scheme. And finally, *dp*, *dq* and the position of the space vector as the input of the switching table (Table I), generates PWM signal

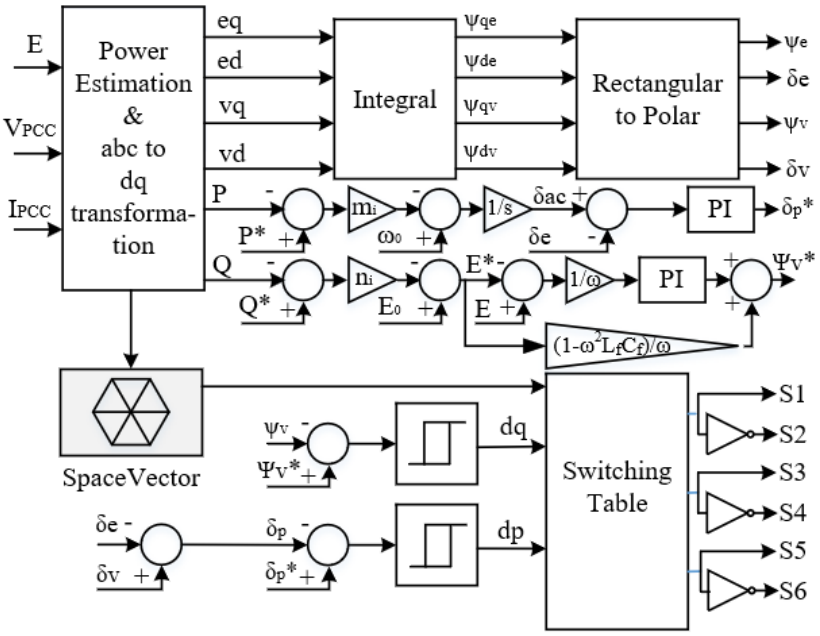


Figure 2.5. Simplified block diagram of the FPC for parallel-connected VSIs

to control the required P_{PCC} and $Q_{PCC.}$ General P-ω droop characteristics and Q-V droop characteristics for k number of parallel inverters are expressed in the equations (5) and (6) respectively as,

$$\omega_k{}^* = \omega_0 - m_1(P^* - P) \ . \tag{2.5}$$

$$V_k{}^* = V_0 - n_k(Q^* - Q) \ . \tag{2.6}$$

The switching choses a zero-switching vector (V_0 or V_7) table if these errors are less than a specified limit (the band of the hysteresis loop). Otherwise, the switching vector, which controls ψ_E and δ_p in the correct direction to force the error (P^*-P_{PCC}) and (Q^*-Q_{PCC}) to zero is initiated instantly. The flux vector ($\vec{\psi}_E$) in the FPC scheme is expressed as,

$$\psi_{dE} = \int_{-\infty}^{t} e_d d\tau \ . \tag{2.7}$$

$$\psi_{qE} = \int_{-\infty}^{t} e_q d\tau \ . \tag{2.8}$$

The magnitude and angle of $\vec{\psi}_E$ are represented as,

$$|\psi_{Ev}| = \sqrt{\psi^2_{dE} + \psi^2_{qE}} \ . \tag{2.9}$$

and $\delta_E = \tan^{-1}\left(\frac{-\psi_{dE}}{\psi_{qE}}\right)$. (2.10)

Similarly, the magnitude and angle of $\vec{\psi}_V$ are represented as,

$$\delta_V = \tan^{-1}\left(\frac{-\psi_{dV}}{\psi_{qV}}\right). \tag{2.11}$$

$$\delta_p = \delta_E - \delta_V \ . \tag{2.12}$$

The active power and reactive power representation by the flux vectors are

$$P = \frac{3\omega}{2L_f}\psi_V\psi_E \sin(\delta_p). \tag{2.13}$$

$$Q = \frac{3\omega}{2L_f}(\psi_V\psi_E \cos(\delta_p) - \psi^2_V). \tag{2.14}$$

In the islanded system version of the control scheme, voltage and frequency of the PCC are controlled by following the V_{PCC}* and *f** in each of the PCCs of the two parallel-connected VSIs as shown in Figure 2.6. The remaining calculation of the switching states of the 3 phase VSI is done by using the switching table by following the original FPC scheme from the calculated *dp*, *dq* and the position of the space vector.

The Load sharing technique is explained in [40, 42] for parallel-connected inverters in the islanded system and many papers [43-46] are based on this method for defining controls in islanded operation.

2.2.4. Current Controlled Virtual Synchronous Machine (CC-VISMA)

The VISMA control method was first proposed in [17]. In comparison with a conventional electromagnetic Synchronous Machine (SMA), a three-phase inverter has neither rotating inertia nor damping effect, to begin with. The intrinsic kinetic energy (rotor inertia) and damping factor (due to mainly electrical losses in stator and mechanical friction) of the conventional bulk SMAs play a significant role in the grid stability. By implementing virtual rotor inertia (*J*) and damping factor (*B*) in the current control-based the CC-VISMA [18] control, the inverter can behalf like an SG to improve the stability and quality of a grid-connected and specially islanded power system. The main objective of analyzing this controller is whether it can control the parallel-connected VSIs by applying virtual inertia and damping factor in the same fashion SGs react to the voltage and frequency unbalances at the PCC.

The governing equations of a conventional SG acting as a power generator are given by

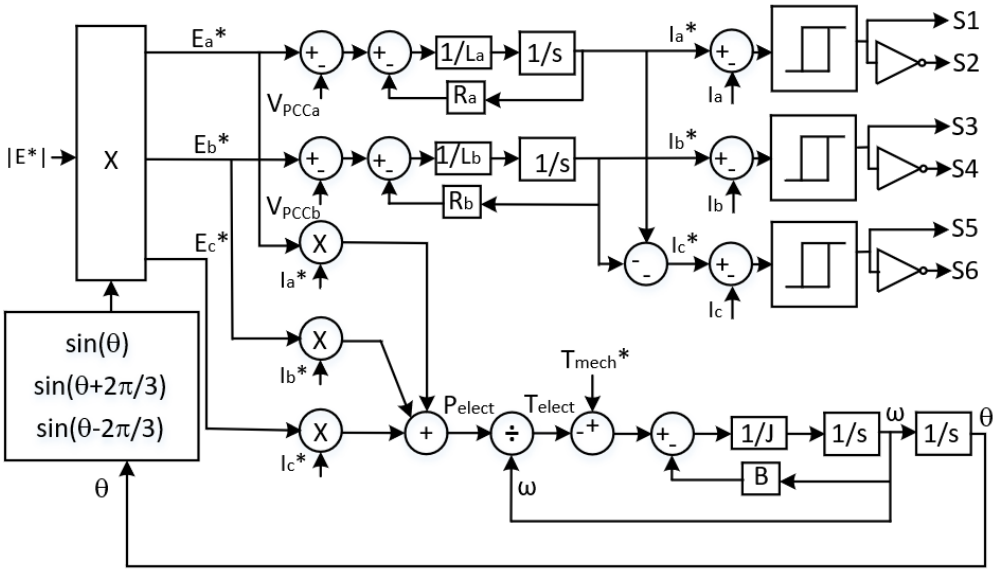


Figure 2.6. Simplified block diagram of CC-VISMA control

$$\bar{e} = \bar{v} + \bar{i}R + L_s \frac{d\bar{i}}{dt} . \quad (2.15)$$

$$P_{elect} = E_a i_a + E_b i_b + E_c i_c . \quad (2.16)$$

$$T_{elect} = (P_{elect}) / \omega . \quad (2.17)$$

$$T_{mech} = T_{elect} + B\omega + J \frac{d\omega}{dt} . \quad (2.18)$$

Based on these equations, CC-VISMA controller, shown in Figure 2.6, is constructed that mimics the operation of the synchronous machine.

Following the governing equation (18), phase angle, Θ is calculated from electrical output power P_{elect}, mechanical torque T_{mech}* (which represents active power setting, P*, in synchronous generator) and chosen parameters of J and B. Based on a reference voltage amplitude ($|E^*|$) (which represents current in excitation winding that regulates Q), reference voltages, (E_a*, E_b* and E_c*) are formed. Whereas PCC voltages (V_a, V_b and V_c) are treated as terminal voltages of this machine. Thus, from the error (E*-V), for a given machine stator resistance (R) and stator leakage inductance (L_s), the reference currents (i_a*, i_b* and i_c*) are constructed (by implementing the equation (2.15) in the controller). These are then compared with the measured current in the PCC (i_a, i_b, and i_c) and the error to generate the PWM signal after hysteresis implementation. Active power can be controlled by setting the value of T_{mech}*.

In the grid-connected system, the controller does not need to be synchronized to the V_{PCC} before starting the control operation to control P_{PCC} and Q_{PCC}.

In the parallel-connected two inverter system, the magnitude of the voltage information is present, but the definition of the nominal frequency (ω_0) is needed to be included in the control

scheme to stabilize the system. Because in the existing CC-VISMA control scheme, ω_0 is not externally provided to form the two parallel-connected VSIs in the islanded system.

The VISMA control architecture does not need the PLL to form grid [26]. Hence, it eliminates the complexity and disadvantages of having a PLL in the controller [47]. Active and reactive power control for a virtual power plant has been demonstrated in [48] using basic VISMA control. An improved damping of VISMA control is shown in [49]. Virtual Impedance design for a VISMA controller in a weak grid is done in [50].

2.2.5. Voltage Controlled Virtual Synchronous Machine (VC-VISMA) Control

In a similar approach, measured PCC currents (i_a, i_b and $i_{c)}$ are employed to determine PCC voltage references (V_a*, V_b* and V_c*) to control the VSI by VC-VISMA control [18] scheme is shown in Figure 2.7. The dynamic property of this scheme was explained in [51]. The improvement of power quality after using this control scheme was proved in [52]. The mathematical design of this virtual inertia controller has been modeled in [53-55].

From the schematic diagram of this controller in Figure 2.7 based on a |E*|, and associated E_a*, E_b* and E_c* (which represent generated back emf voltages of a virtual machine) for a certain given R and L_s, reference references (V_a*, V_b* and V_c*) are generated following the equation (15). Next, these are compared with a 10 kHz carrier triangular waveform to perform PWM of the switches. This generated inverter output voltages (E_a*, E_b* and Ec*) are necessary to emulate reference

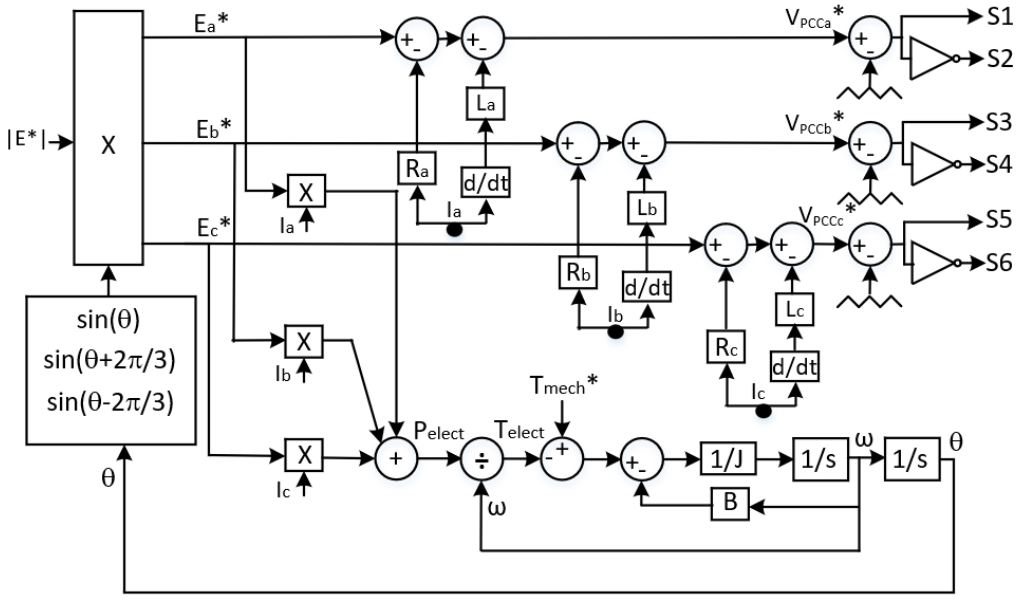


Figure 2.7. Simplified block diagram of VC-VISMA control

terminal voltages of this virtual machine model of the inverter. In the CC-VISMA scheme shown in Figure 2.6, phase angle θ is calculated from the mechanical and T_{mech} and T_{elect} governing the equation (2.18) of the virtual machine. In this control scheme, the dynamic property is the same as the CC-VISMA control scheme but as the switching frequency is constant, there is a possibility to have fewer harmonic contents and lesser noises than the CC-VISMA control scheme.

To form the parallel-connected two inverters system, the definition of the nominal frequency (ω_0) should be included and necessary modifications are needed in the VC-VISMA control scheme to stabilize the system.

This concept of the controller is followed in the following literature [56-60].

A comparative analysis of IPC, DPC and FPC is done in [61]

2.2.6. Classical Droop Control (CDC)

A classical droop controller can be viewed as a VISMA with inertia and damping factors set to zero can be realized in Figure 2.8. The main function of this controller is to stabilize V_{PCC} and f

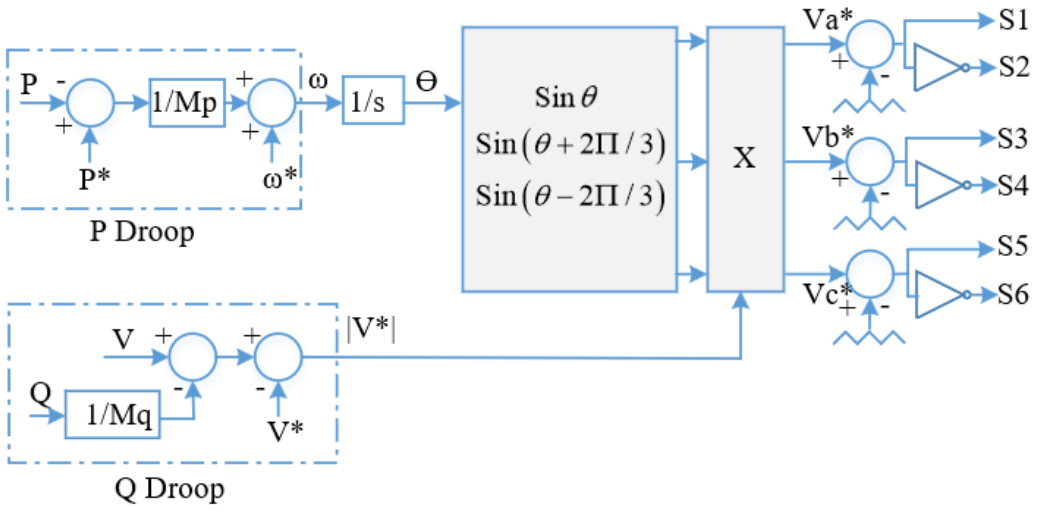


Figure 2.8. Simplified block diagram of droop control

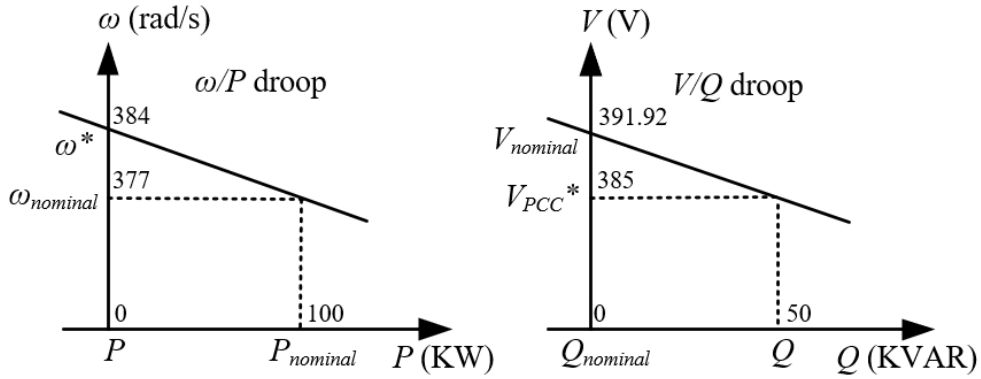


Figure 2.9. Traditional P-f and Q-V droop characteristics of the system

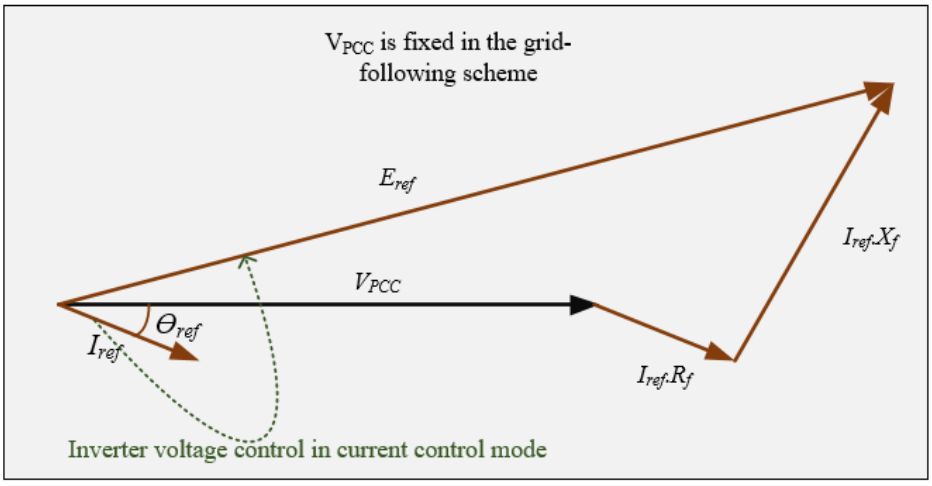


Figure 2.10. The phasor diagram explaining the current control

of the PCC by the following two droop control loops in the parallel-connected VSIs in the islanded

system. Here, P-droop and Q-droop loops create the reference frequency and voltage magnitude to create the PWM signal as an extended current controller. Relation and comparison of droop and other virtual synchronous machines are shown in [6, 56, 62-64].

When voltage decreases in the PCC, the *Q*-*V* droop control loop is triggered and the output *Q* from the inverter is increased to force the V_{PCC} to maintain within the limit as shown in Figure 2.9. Similarly, when frequency droops, output *P* from the inverter increases to force the f_{PCC} back to the stability margin. This behavior of the inverter control is inspired from the Synchronous Generators which have machine inertia. But for the test system in this paper, this simplified droop control is suitable and is expected to control the *V* and *f* as it is a grid-connected system.

As V_{PCC} is fixed in the grid, the power flow through the inverter is inherently controlled by controlling the current magnitude and phase. In this voltage-controlled inverter, E_{ref} is determined from the I_{ref} according to the phasor diagram in Figure 2.10. And the transient during the power control is handled by the PI control inside this controller.

2.2.7. Swing Equation based Virtual Synchronous Generator (SWING-VSG) Control

Synchronous Generator's (SG) swing equation-based VSG control scheme or SWING-VSG is based on the model of a cylindrical-rotor SG and is implemented from [19] and [65]. A detailed survey on VSG and its stability have been done in [66].

The kinetic energy of virtual rotor is expressed as,

$$W = \frac{1}{2} J \omega_m^2 . \tag{2.19}$$

The swing equation for a conventional SG is formed by taking derivative of equation (2.20) as,

$$P_{in} - P_{out} = J \omega_m \frac{d\omega_m}{dt} - Ds . \tag{2.20}$$

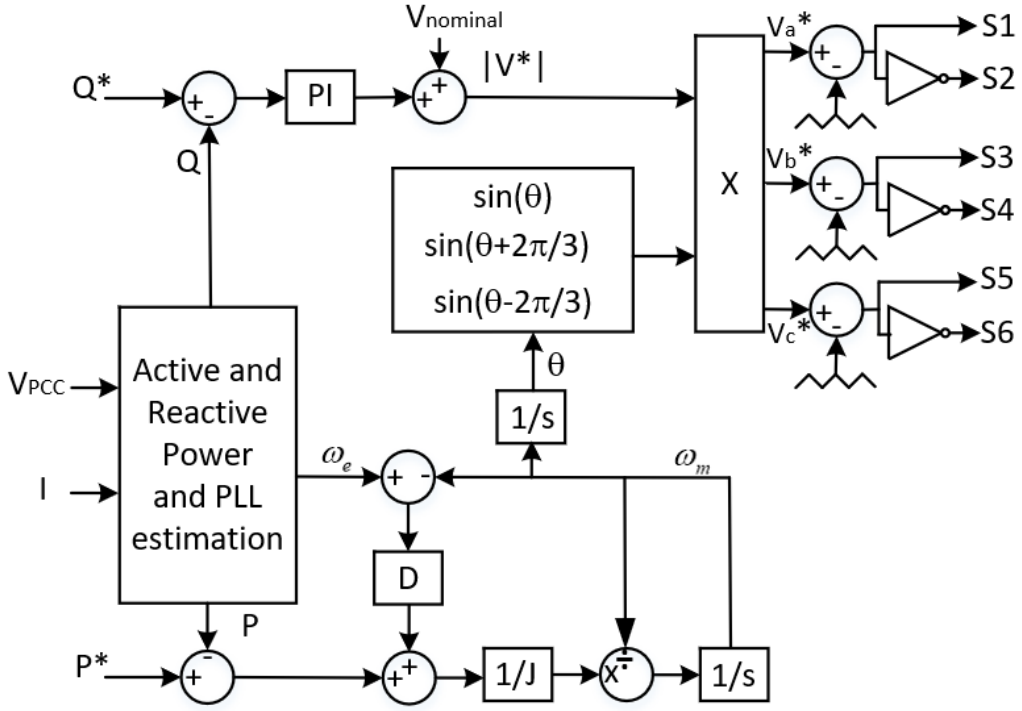


Figure 2.11. Simplified block diagram of SWING-VSG control

Where, J is moment of inertia, ω_m is the mechanical speed, D is the damping factor, and s is slip of the virtual rotor. By implementing this equation, the ω is calculated and by passing through an integrator, the virtual mechanical phase angle (θ) is produced for generating switching pulses in the control scheme in Figure 2.11, shown in [65]. In this figure, the P, Q and f are calculated in the Active and Reactive Power Estimator and PLL block. The f is employed to compute slip, s ($=\omega_e - \omega_m$). Then and then ω_m is calculated by using equation (2.20). Then, this ω_m is integrated to get θ which is then supplied to the sine wave generator to get the reference voltage shape. While the change of reactive power and nominal voltage ($v_{nominal}$) in the PCC creates reference voltage magnitude $|V^*|$. Multiplying the reference shape and $|V^*|$, reference PCC voltage V^* is achieved. And finally, the PWM signal is generated by the sine-triangle PWM modulation method from the V^* signal.

This method is not good for directly controlling P_{PCC} and Q_{PCC} in the grid-connected mode. As V^* is generated by controlling ω_m but it is comparatively rigid in grid-connected system and any effort to change it directly for controlling power will force to create a different value of ω_m by the controller. So, error (s) will not be 0 and the power control will not be a success. A small change in P, Q may be handled by this controller. But load sharing by parallel-connected inverters can be controlled by this method as shown in [67].

However, In the grid-isolated system with some modifications, especially setting the nominal frequency ($\omega_{nominal}$) as reference, SWING-VSG can stabilize V_{PCC} and f in the PCC.

Applications of this control scheme in microgrids and its stability are highlighted in [68-77].

2.2.8. Algebraic Type Virtual Synchronous Generator (AT-VSG) Control

The VSG model using the phasor diagram (Figure 2.12) is called Algebraic Type VSG or just AT-VSG and was proposed in [78] which is called algebraic type VSG. From the phasor diagram, the armature currents I_d^* and I_q^* are expressed as in equation (2.22). These are used to generate the

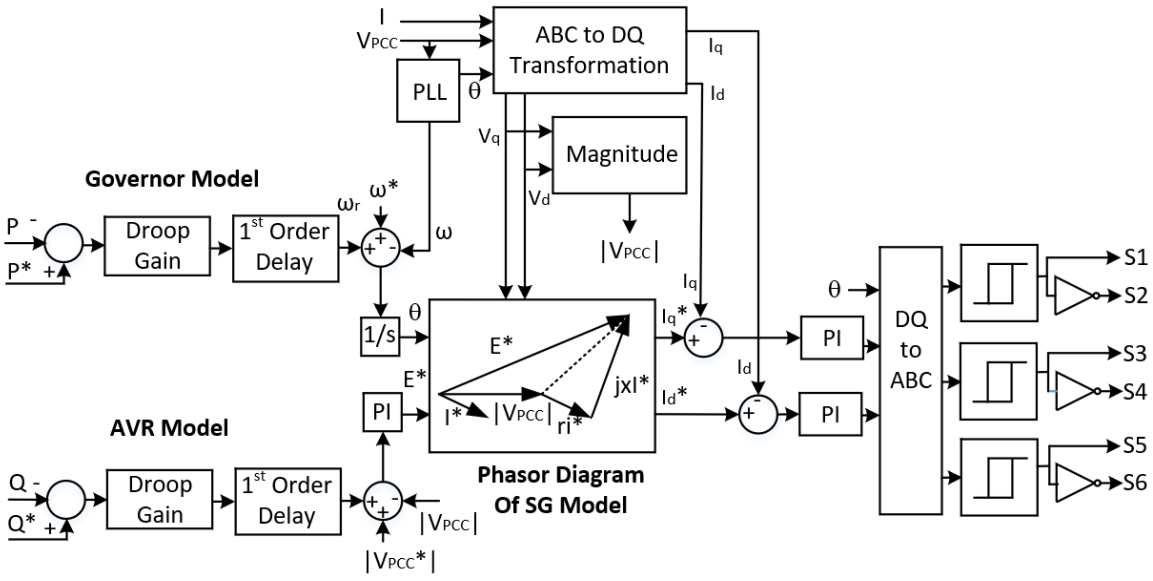


Figure 2.12. Simplified block diagram of AT-VSG control

error after the encounter with I_d and I_q for generating the PWM signal for the inverter as shown in Figure 2.12. The synchronous impedances, R and X of the virtual SG model of the inverter are taken as the constants in the equation (2.23).

$$\begin{bmatrix} E_d \\ E_q \end{bmatrix} = E \begin{bmatrix} \cos(\theta) \\ \sin(\theta) \end{bmatrix}. \tag{2.21}$$

$$\begin{bmatrix} I_d^* \\ I_q^* \end{bmatrix} = Y \left\{ \begin{bmatrix} E_d^* \\ E_q^* \end{bmatrix} - \begin{bmatrix} V_d \\ V_q \end{bmatrix} \right\}. \tag{2.22}$$

$$Y = \frac{1}{R^2 + X^2} \begin{bmatrix} R & X \\ -X & R \end{bmatrix}. \tag{2.23}$$

The magnitude of E^* is specified by the Automatic Voltage Restorer (AVR) model and is calculated by the Q^*, Q, V^* and V signals as shown in the block diagram. The internal phase angle, θ is determined as the time integral of the deviation between the virtual rotor's angular speed, ω_r is provided by the governor model and the system angular frequency, ω is determined by the PLL circuit. The PLL circuit detects the phase angle and angular speed from the generator's terminal voltage which is the PCC voltage from the inverter's terminal.

This VSG control scheme has also been employed in [62, 79-81] for the grid-connected and grid-isolated systems in recent times.

2.2.9. Static Synchronous Generator (SSG) Control

A comprehensive emulation of the static synchronous generator was proposed in [82] in forming a control scheme, named SSG for parallel-connected VSIs is shown in the simplified block diagram (Figure 2.13). The derived equations from the detailed model of an SG for calculating T_{elect}, P, Q and E^* are expressed as,

$$T_{elect} = M_f i_f \langle i, \sin\tilde{\theta} \rangle . \tag{2.24}$$

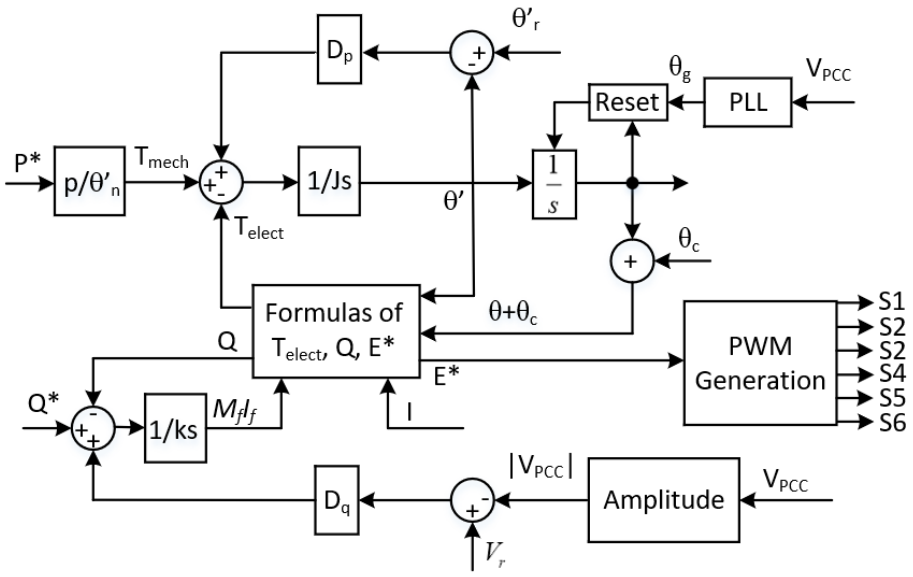


Figure 2.13. Simplified block diagram of SSG control

$$E^* = \dot{\theta} M_f i_f \sin\tilde{\theta} \,. \tag{2.25}$$

$$P = \dot{\theta} M_f i_f \langle i, \sin\tilde{\theta} \rangle \,. \tag{2.26}$$

$$Q = -\dot{\theta} M_f i_f \langle i, \cos\tilde{\theta} \rangle \,. \tag{2.27}$$

These equations are implemented in SSG control is shown in Figure 2.13. Here, $\langle \cdot, \cdot \rangle$ denotes the conventional inner product in R^3. M_f is mutual inductance between the field coil and the stator winding. I_f is the rotor excitation current of the SG and this is represented by the PCC current (i) in the VSI. PWM is generated by the from the reference E* after comparing it with a repeating triangular wave to control the VSI.

The equations calculating the change in θ and other factors of the controller, shown in Figure 2.13 are expressed as,

$$\ddot{\theta} = \frac{1}{J}(T_{mech} - T_{elect} - D_p \dot{\theta}) \,. \tag{2.28}$$

$$D_p = \frac{\Delta T}{\Delta \dot{\theta}}. \quad (2.29)$$

$$D_q = \frac{\Delta Q}{\Delta v}. \quad (2.30)$$

$$J_s = D_p \tau_f. \quad (2.31)$$

And $K_s = D_q \tau_v$. (2.32)

Here, ΔT is the change in torque, $\Delta \dot{\theta}$ is the change in angular frequency, ΔQ is the change is reactive power, Δv is the change is voltage and τ_f and τ_v are time constants in frequency and voltage droop respectively.

This control model is derived from an SG to cover all the dynamics without any assumptions to generate the controlling signals. In the implementation, power regulation and load sharing operations are included in the control scheme. The mathematical model, which can be developed using described equations in this control scheme based on SG can be used to investigate the stability of power systems consisting of parallel-connected inverters the islanded system.

Similar work has been performed with this SSG control in [83]. The detailed model of SG from the SSG was used to evaluate the load sharing among inverters, smart grid integration, operation and transitions in the literatures [84-87]. An improved SSG control scheme was proposed in [88] to bound voltage and frequency near the rated value.

2.2.10. Virtual Synchronous Machine- Static Synchronous Compensator (VISMA-STATCOM) Control

An extended concept of the synchronous machine, a VISMA based STATCOM controller was proposed and a mathematical model was derived in [89]. The simplified block diagram is shown in Figure 2.14 to show the PWM signal generation while stabilizing the PCC voltage at the reference

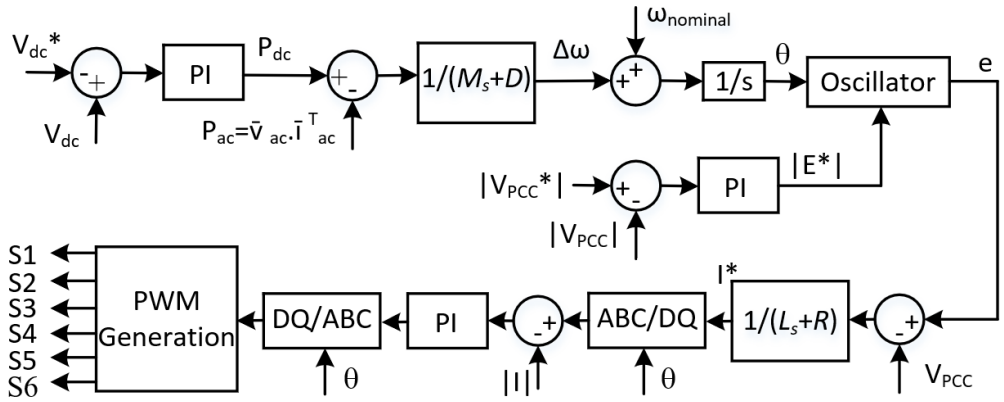


Figure 2.14. Simplified block diagram of virtual synchronous machine based STATCOM control in DQ synchronous frame (current mode)

V_{PCC}*. Here, voltage and frequency are taken as the controlling elements and measured voltage and current from the PCC are measured as the controlled elements. Theoretically, this is a good controller to synchronize parallel-connected inverters.

Practically, it's basic principle of generating the PWM signal is similar to the IPC controller but the θ is internally synced by the virtual inertia. Later this θ is used in the park's transformations in this control scheme. The virtual inertia constants (M and D) and virtual impedances (R and L) decide the overall transfer function of the controller and the stability justification of these values of the constants can be done from the mathematical model [90] and by the bode plot analysis. More analysis and experimental validation of the active and reactive power control by this controller was done in [91-93]

2.3. Simulation Results

2.3.1 Comparison of Power Control by IPC, DPC and FPC

In test case-I, DPC and FPC (Fig. 2.16 and Fig. 2.17 respectively) are faster than IPC (Fig. 2.15) to reach the steady states (within $\pm 5\%$ band) from initial conditions and the changed power-demand conditions which were initiated at 0.1 s [61]. It is because of the PI dynamics in the IPC control loop and unit step delays in the DSP implementation of the controller. The disadvantage

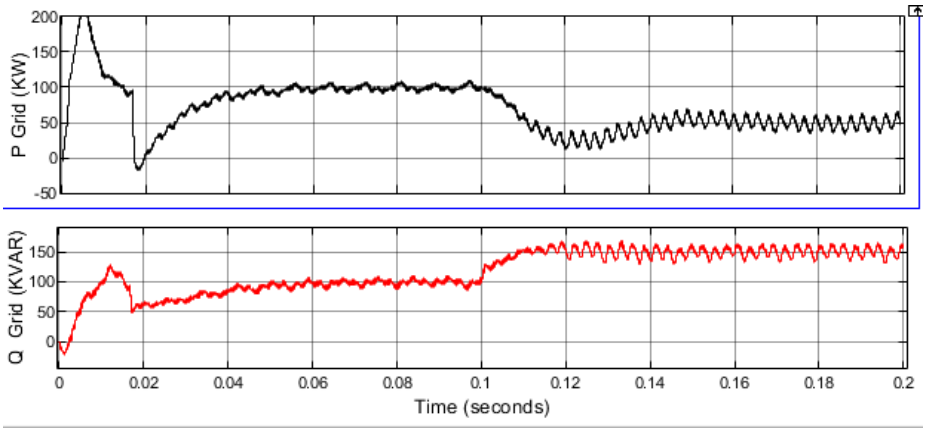


Figure 2.15. Profile of P_{PCC} and Q_{PCC} by IPC (steady state in P at 0.05s and 0.15s, and Q at 0.06s and 0.12s)

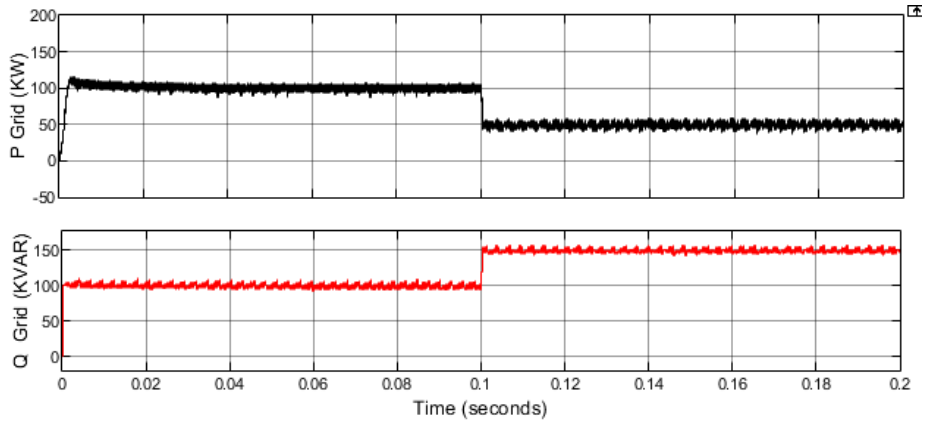


Figure 2.16. Profile of P_{PCC} and Q_{PCC} by DPC (steady state in P at 0.0035s and 0.1004s, and Q at 0.0004s and 0.1004s)

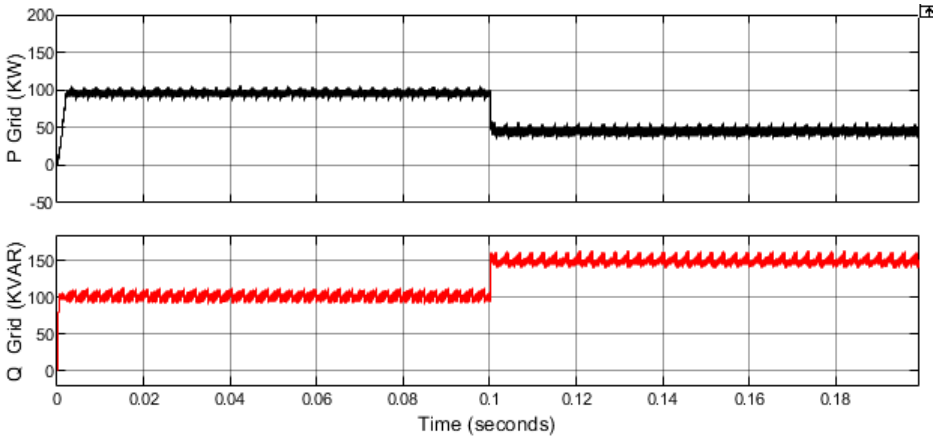


Figure 2.17. Profile of P_{PCC} and Q_{PCC} by FPC (steady state in P at 0.0028s and 0.1003s, and Q at 0.00035s and 0.1002s

of DPC and FPC schemes is that the f_{sw}, generated by these controllers is not specified and it ranges from 83-168 kHz because of the hysteresis implementation.

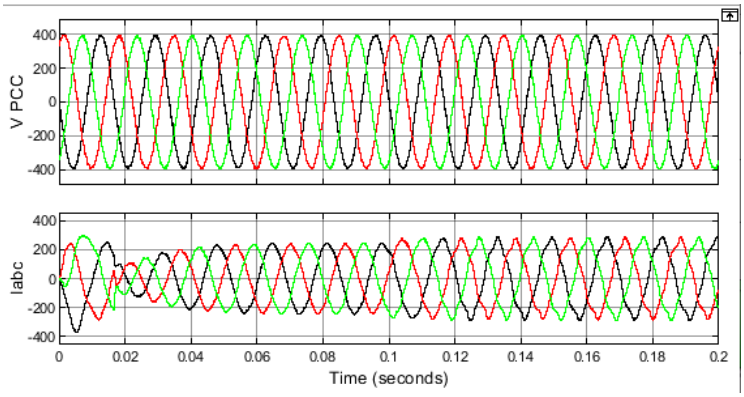


Figure 2.18. Voltage and current by the IPC scheme, where the transient is applied at 0.1 s

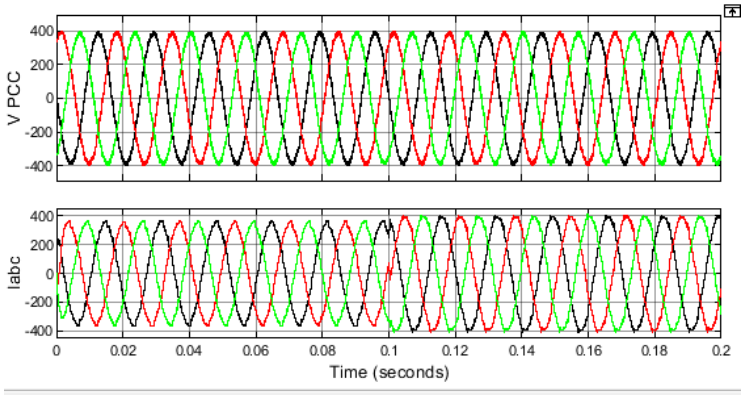


Figure 2.19. Voltage and current by the DPC scheme, where the transient is applied at 0.1 s

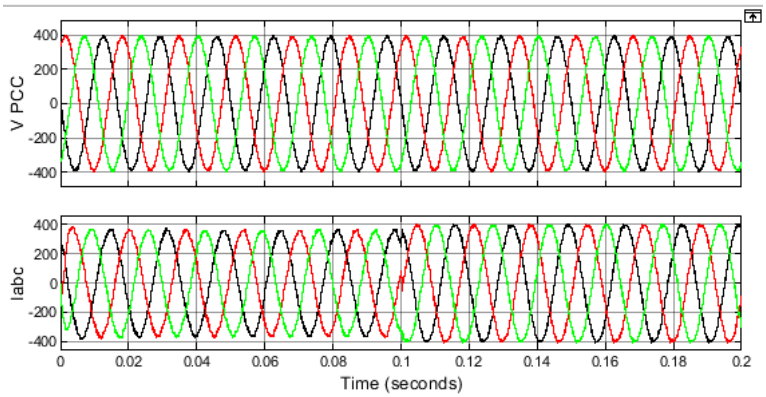


Figure 2.20. Voltage and current by the FPC scheme, where the transient is applied at 0.1 s

From the observation of the profiles of grid voltages and currents (in Figs. 2.18-2.20), the current profile while controlled by the IPC has more harmonic content than that by DPC and FPC scheme and because of that, it looks more distorted. A lower amount of distortion in the grid current profile of the DPC and FPC schemes can be observed in Figs. 2.19, 2.20. This is because of the finite number (12) of sector selections in the switching table design. Improving the smoothness of the current is contingent on adding more sector divisions. FPC shows a slightly lower ripple than DPC in regulating P_{PCC} and Q_{PCC} while achieving a similar fast transient

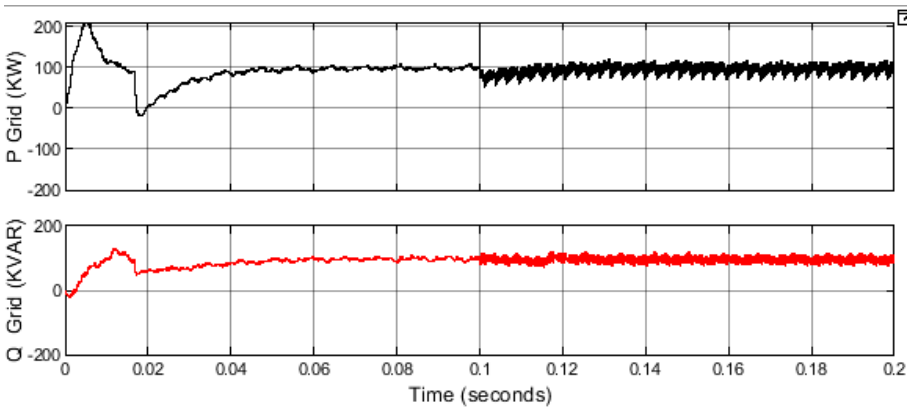


Figure 2.21. Profile of *P* and *Q* by the IPC scheme, where grid inductance is increased from 0.02 mH to 0.2 mH at 0.1 s

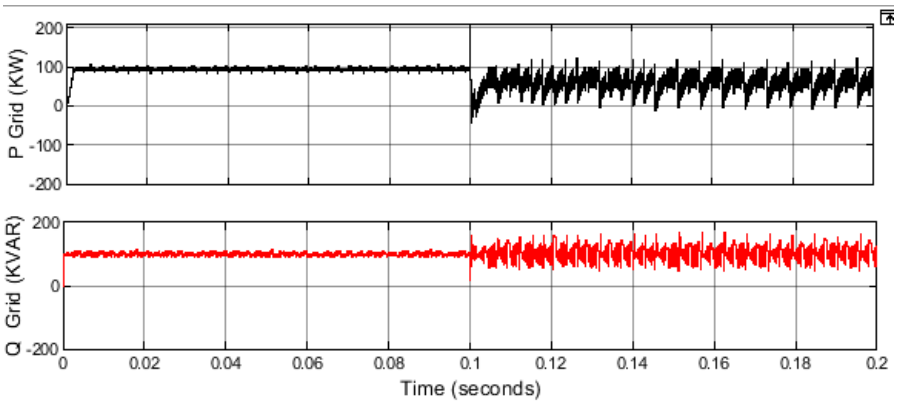


Figure 2.22. Profile of *P* and *Q* by the DPC scheme, where grid inductance is increased from 0.02 mH to 0.2 mH at 0.1 s

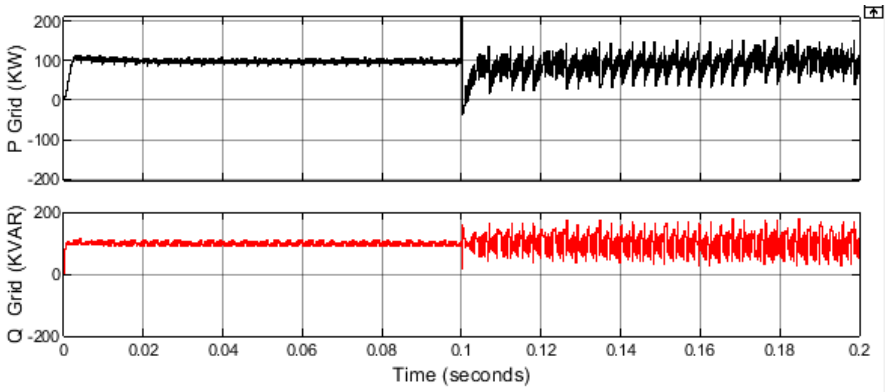


Figure 2.23. Profile of *P* and *Q* by the FPC scheme, where grid inductance is increased from 0.02 mH to 0.2 mH at 0.1 s

response as DPC (in Figs. 2.16, 2.17) because small dynamic changes of *P* and *Q* were taken into consideration in terms of changes in inverter flux magnitude and angle in this control scheme.

In test case-II, because DPC and FPC schemes lack PI control, it produced more steady-state error compared to the IPC scheme while controlling the grid power demand in the 10 times weaker grid at 0.1s (Figs. 2.21-2.23). From the observation in the profiles of grid voltages and currents in Figs. 2.24-2.26, DPC and FPC produced more harmonic contents than IPC while keeping all other parameters unchanged from test case-I.

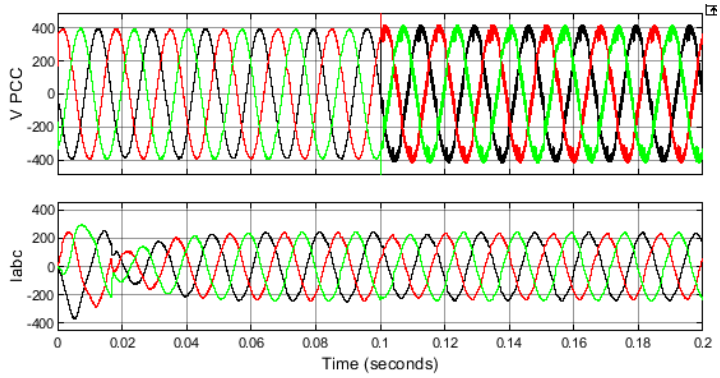


Figure 2.24. Voltage and current by the IPC scheme; the grid is 10 times weaker at 0.1 s

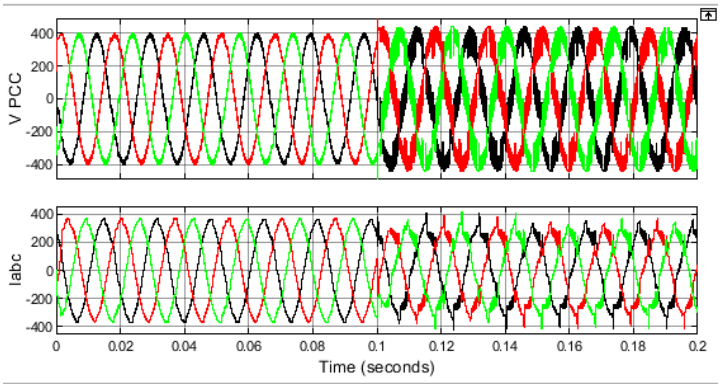


Figure 2.25. Voltage and current by the DPC scheme; the grid is 10 times weaker at 0.1 s

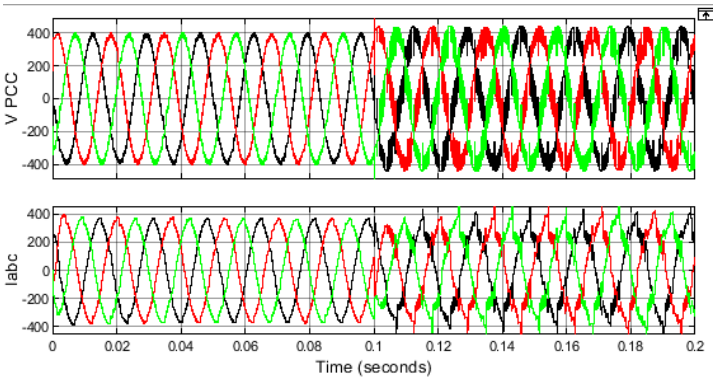


Figure 2.26. Voltage and current by the FPC scheme; the grid is 10 times weaker at 0.1 s

2.3.2 Virtual Synchronous Machine-Based Controllers for Grid-Following Inverters

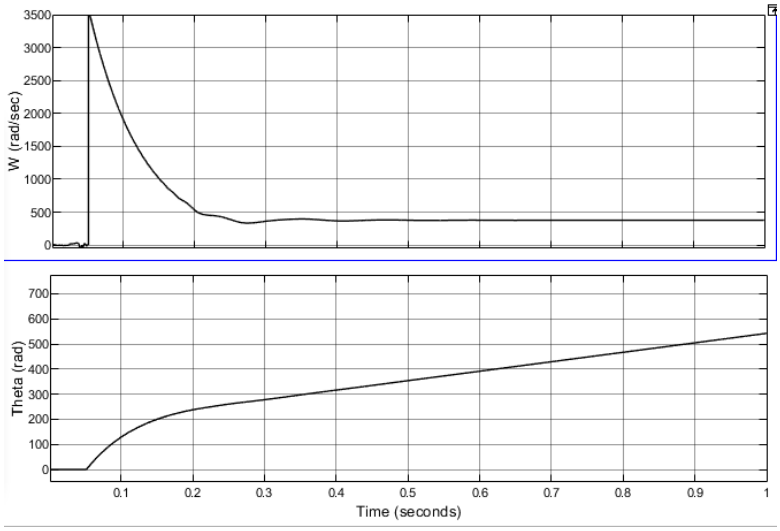


Figure 2.27. Profiles of ω and θ by CC-VISMA for the grid-connected system

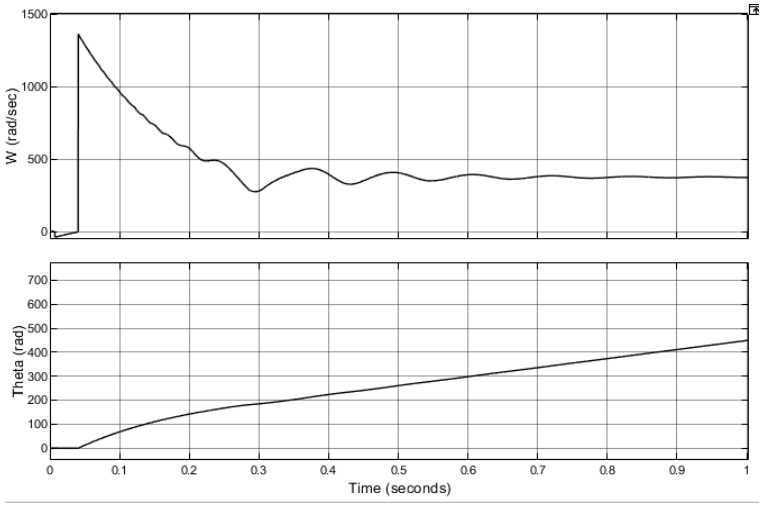


Figure 2.28. Profiles of ω and θ by VC-VISMA for the grid-connected system

The measured frequency (ω) and phase (θ) while controlled by the CC-VISMA control scheme are presented in Fig. 2.27. ω is controlled as 377 rad/sec at 0.2 sec. However, a big transient peak of 3500 rad/sec is observed in the grid-connected system. This peak in frequency can be further controlled by appropriately designing inertia constant and damping factor according to conditions. The measured ω and θ by the VC-VISMA control scheme is presented in Fig. 28 where the

frequency has been stabilized at 0.3 sec. Here the maximum peak value of the frequency is 1400 Hz which is less than that while controlled by the CC-VISMA control scheme.

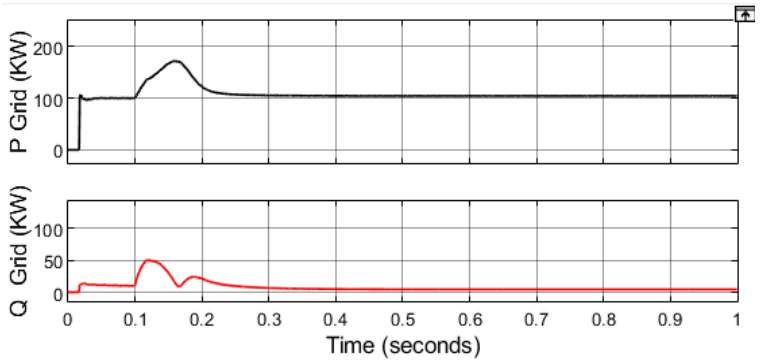


Figure 2.29. Profiles of *P* and *Q* by CC-VISMA for the grid-connected system

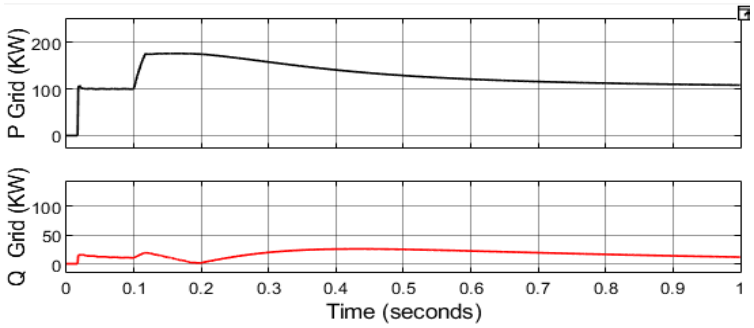


Figure 2.30. Profiles of *P* and *Q* by VC-VISMA for the grid-connected system

The power delivered by the inverter by CC-VISMA and VC-VISMA is presented in Figs. 29 and 30. In this case, controllers can control the *P* and *Q* to the desired 100 kW and 10 kVar but the frequency response is slower in VC-VISMA compared to CC-VISMA as observed in Figs. 27 and 28. As the power is a product of voltage and current, with the change of reactive power, voltage can be changed at PCC. And in consequence, active power can be affected as shown in Figs 29 and 30. Hence a parallel voltage control loop is recommended for this controller to control PCC voltage for controlling frequency and power accurately.

The values of *J* and *B* are chosen as 0.1 kg.m^2 and 0.15 respectively.

2.3.2 Grid-Forming Inverter Controllers in the Grid-Disconnected System

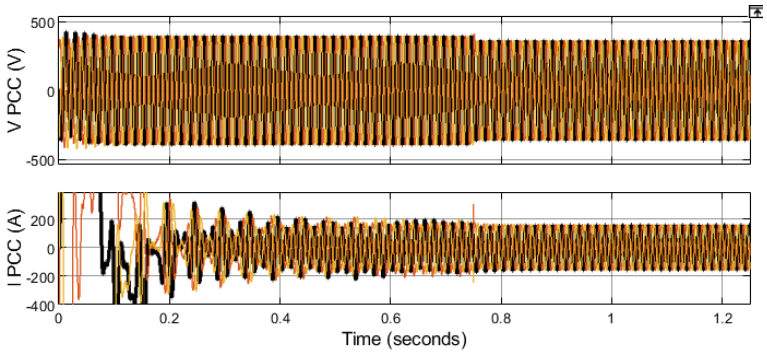


Figure 2.31. Profiles of PCC voltage and current by SWING-VSG controller where at 0.75 sec, the inverter is disconnected from the grid

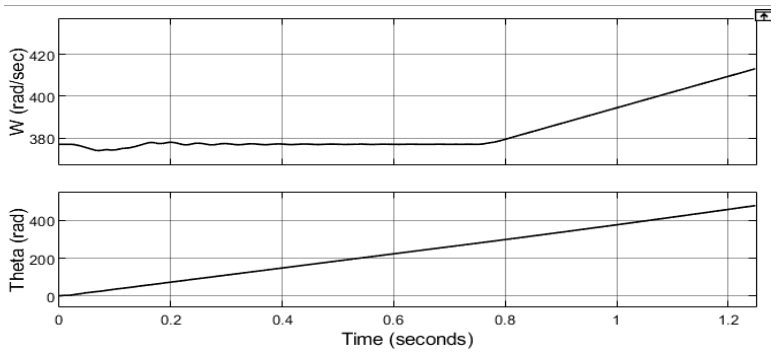


Figure 2.32. Profiles of ω and θ by SWING-VSG controller

In this special case, the inverter is connected to the grid from the start and disconnected from the grid at 0.75 s. The voltage and frequency control capacity of the controllers are compared by initiating this condition of sudden disconnection from the grid.

Fig. 31 shows the profiles of the inverter voltage and current at PCC while it was controlled by the SWING-VSG controller. The profiles of measured ω and θ are shown in Fig. 32. It is observed that after the disconnection from the grid, slowly the frequency diverges from the reference frequency value, 377rad/s as the reference frequency does not exist in this controller.

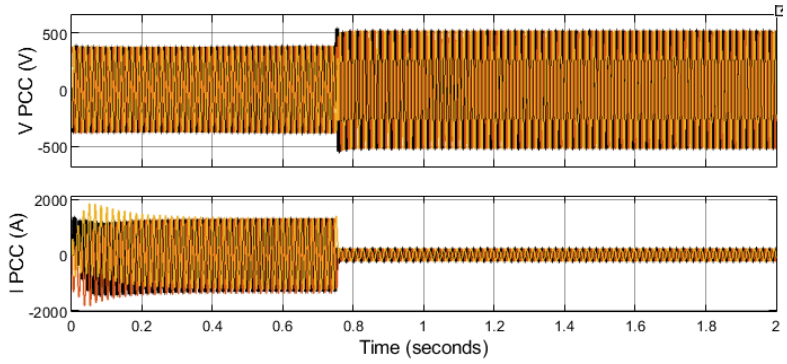


Figure 2.33. Profiles of PCC voltage and current by AT-VSG controller where at 0.75 sec, the inverter is disconnected from the grid

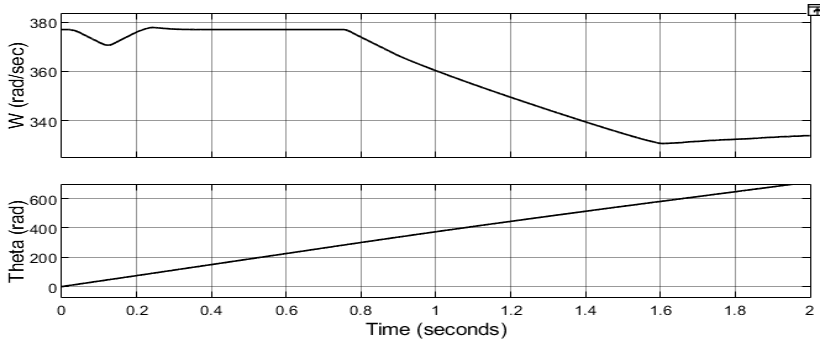


Figure 2.34. Profiles of ω and θ by AT-VSG controller

Fig. 34 presents the profiles of the inverter voltage and current at PCC while it was controlled by the AT-VSG controller. The profiles of measured ω and phase θ are presented in Fig. 34. In the grid connection system, it follows the voltage and frequency but after the disconnection from the grid, it fails to control the voltage and frequency to the reference values.

Fig. 35 presents the profiles of the inverter voltage and current at PCC while it was controlled by the SSG controller. The profiles of measured ω and phase θ are shown in Fig. 36. It is observed that it took approximately 0.7 s to recover the voltage of the inverter to its nominal value after being disconnected from the grid. In both the grid-following and grid-forming modes, it succeeded in controlling the voltage and frequency.

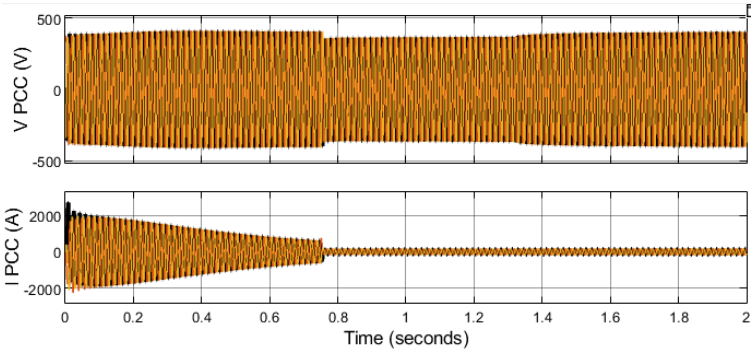


Figure 2.35. Profiles of PCC voltage and current by SSG controller where at 0.75 sec, the inverter is disconnected from the grid

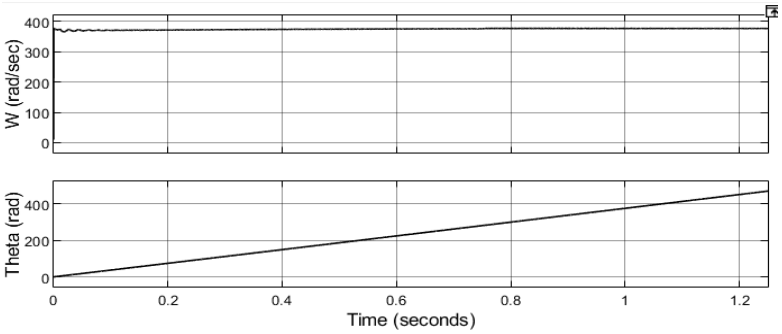


Figure 2.36. Profiles of ω and θ by SSG controller

Fig. 37 presents the profiles of the inverter voltage and current at PCC while it was controlled by the VISMA-STATCOM controller. The profiles of measured ω and phase θ are presented in Fig. 38. It is observed that Both in the grid-connection and disconnected systems, it controlled the voltage and frequency to their desired reference values.

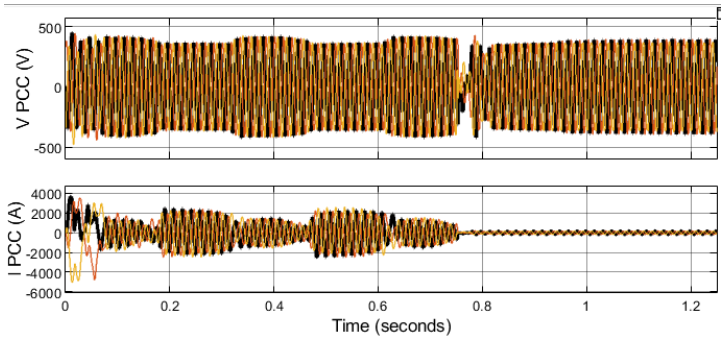


Figure 2.37. Profiles of PCC voltage and current by VISMA-STATCOM controller where at 0.75 sec, the inverter is disconnected from the grid

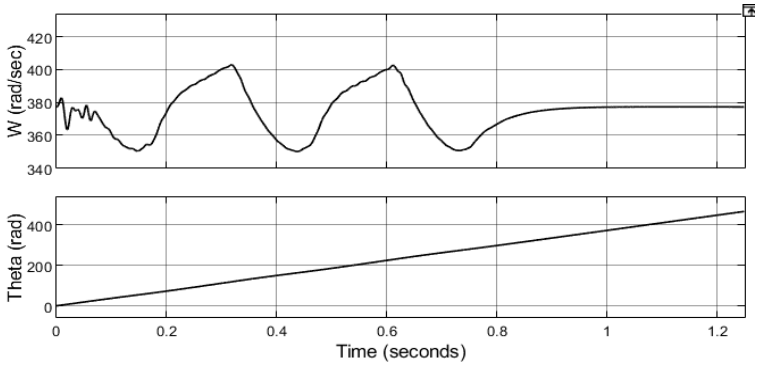


Figure 2.38. Profiles of ω and θ by VISMA-STATCOM controller

2.4. Conclusion

From the study of the existing literature, it can be concluded that VSG controls can compensate for voltage dip during a short circuit (just like an SG injects reactive power to the system during a fault) for a short time. Thus, it is expected that the VSG also can prevent power grid blackouts due to voltage unbalance and can retain safety in fault situations. That is why several literatures [15-17, 38-42, 46-49, 50-53] have considered this VSG control for the grid-forming and grid-connected applications. Table II shows the comparison of the controllers based on their capabilities.

Presently, the main problem is defining a control architecture for the inverters in distributed ERs. There are two options: 1. redesign the whole power system and to change the way it is operated (e.g., establish fast communication lines between generators and possibly central SCADA control) and 2. Finding a way so that these inverters can be integrated into the existing system and behave in the same way bulk SGs do. It is analyzed that the second option is advantageous because it would assure a smooth transition to a grid or no-grid system, dominated by the inverters. And for this, all the virtual implementations of controllers, based on SGs, are preffered by the control engineers. Furthermore, a simple and complete control architecture is in current demand to make

TABLE II
COMPARISON OF CONTROLLERS

Controllers	Grid-Formation	Absence of PLL	Virtual Inertia	Black-Start Capacity	Absence of d/dt	Droop Control
IPC	×	×	×	×	✓	×
DPC	×	✓	×	×	✓	×
FPC	✓	✓	×	×	✓	×
CC-VISMA	×	✓	✓	×	✓	×
VC-VISMA	×	✓	✓	×	×	×
CDC	✓	✓	×	✓	✓	✓
SWING-VSG	×	×	✓	×	✓	✓
AT-VSG	✓	×	×	✓	✓	✓
SSG	✓	×	✓	✓	✓	✓
VISMA-STATCOM	✓	✓	✓	✓	✓	×

the grid-isolated system stable and to make the transition from SG based power system to NRERs based power system smooth.

CHAPTER 3: SYNCHRONOUS MACHINE EMULATOR WITH EMBEDDED DROOP CONTROL (SME-EDC)

3.1. Introduction

From the literature review of the reported controllers for grid-forming and grid-connected inverters, it has been noted that none of the controllers have all the capabilities of an ideal controller for grid-forming inverters. These desired capabilities are:

A. Accurately control the PCC voltage and frequency of the inverters
B. Auto-synchronize the phase of the voltage of the parallel-connected and grid-connected inverters without communication.
C. Black start the inverters in absence of the grid
D. Seamless transition between grid-forming grid-connected mode of inverter control
E. Control load sharing in multiple parallel-connected inverters system

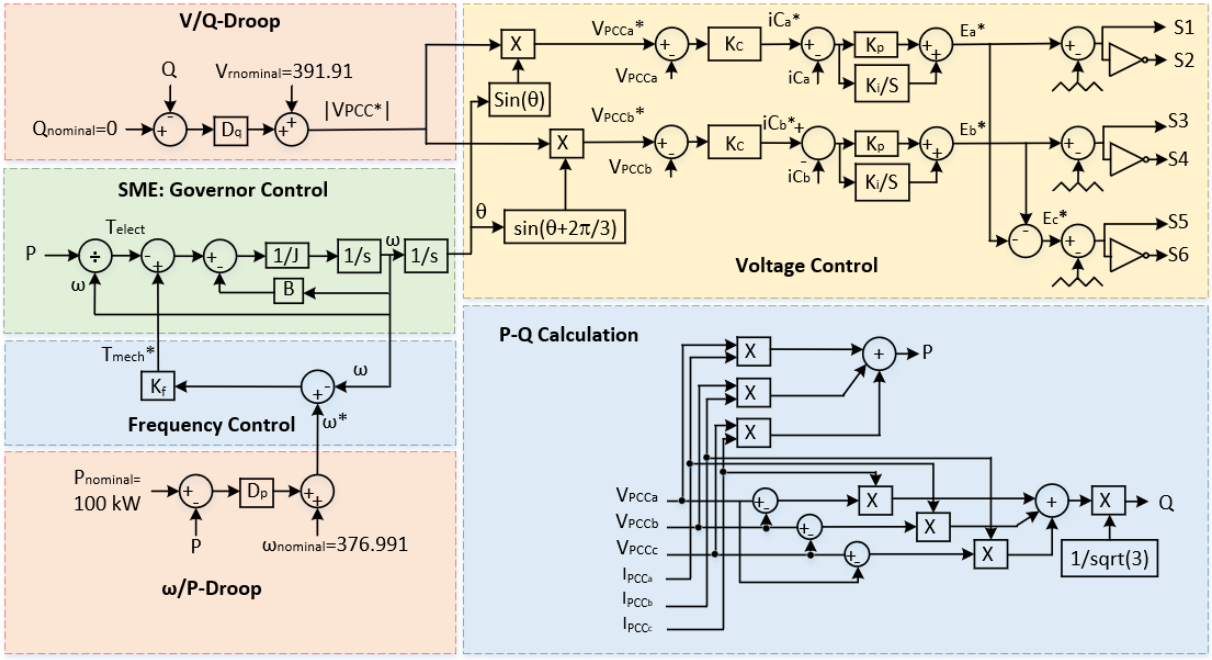


Figure 3.1. Simplified control block diagram of the proposed Synchronous Machine Emulator with Embedded Droop Control (SME-EDC)

3.2. Operating Principle of SME-EDC

For solving the above-mentioned problems in the inverter control, the novel control topology, Synchronous Machine Emulator with Embedded Droop Control (SME-EDC) is proposed. Figure 3.1 shows the simplified block diagram of the proposed SME-EDC. The following are the features of the controller. The controller has four control loops as follows.

3.2.1. Voltage Control Loop

The innermost control loop **or voltage control loop** consists of the filter capacitor (iC) current-controlled reference inverter emf (E_{abc}) generation. K_p, K_i and K_c are the control gains in this control loop. V_{PCC}* is the input of this control loop that comes from the second control loop. In this control loop, after comparing V_{PCC}* with V_{PCC}, the error signal (V_{PCC}-V_{PCC}*) is multiplied by the constant K_C and forms the reference capacitor current iC*. K_C is proportional to the admittance of C_f. Its relation can be determined from the following equations.

$$C_f \frac{dV_C}{dt} = iC^*$$

$$\left(\frac{C_f}{\Delta T}\right)(V_C^* - V_C) = iC^*$$

$$K_C\,(V_{PCC}^* - V_{PCC}) = iC^*. \tag{3.1}$$

In (3.1), the voltage across the C_f is V_C and which is equal to V_{PCC}. Here, $\Delta T = 1/f_{SW} = 10^{-4}$ and the value of K_C can be calculated from this relation:

$$K_C = \frac{C}{\Delta T}. \tag{3.2}$$

Next, the generated iC* is compared with the measured capacitor current (iC) and goes through the PI control loop to control the error and construct the inverter reference voltage (E*).

$$E^* = (iC^* - iC)(K_P + K_I/s) \tag{3.3}$$

By changing the constants of the PI loop, the damping effect of the LC filter and the controller's stability can be increased. Finally, after implementing PWM on the E^*, the switching signals for the inverter are generated. The controller's parametric values are shown in Table III.

3.2.2. Virtual Governor Control Loop

In the second control loop or **virtual governor control loop**, the equations (2.15-2.18) of the SM are implemented. The input signals of this control loop are T_{mech}^* which is derived from the third control loop (Virtual torque control loop) (3.4). Inertia constants J and B are implemented in this control loop as shown in (3.4) for enabling the phase-synchronism capability and virtual inertia property of this controller. Frequency (ω) and phase angle (θ) are calculated in this control loop to finally generate (V_{PCC}^*) for the inner loop.

$$T_{mech*} = T_{elect} + B\omega + J\frac{d\omega}{dt} \tag{3.4}$$

3.2.3. Frequency Control Loop

In the third control loop or **frequency control loop**, T_{mech}^* is generated from the measured and reference frequency as shown in (3.5) and frequency is controlled. The value of the constant K_f generates the required torque in the black-start condition while actively controlling ω and assisting to determine the phase angle. The value of K_f depends on the rating of the inverter and ω.

$$T_{mech}^* = \omega^* - \omega).\ K_f. \tag{3.5}$$

At the black start, $\omega = 0$, and T_{mech}^* becomes $\omega^*.\ K_f$. In the next iterations ω is controlled at 377 rad/s and appropriate T_{mech}^* is generated in the steady state. At steady state, the frequency ripple is controlled by the following relation: $\Delta\omega = T_{mech}^*/K_f$.

3.2.3. Droop Control Loops

In the fourth control loops or **droop control loops**, reference and measured active power ($P_{nominal}$ and P) and reference and measured reactive Power ($Q_{nominal}$ and Q) are taken as input signals. P and Q are calculated from the measured V_{PCC} and I_{PCC} as shown in (3.6) and (3.7) [33].

$$P=V_{PCCa}.\ I_{PCCa} + V_{PCCb}.\ I_{PCCb} + V_{PCCc}.\ I_{PCCc}. \tag{3.6}$$

$$Q=\frac{1}{\sqrt{3}}[(V_{PCCb} - V_{PCCc}).\ I_{PCCa} + (V_{PCCc} - V_{PCCa}).\ I_{PCCb} + (V_{PCCa} - V_{PCCb}).\ I_{PCCc}]. \tag{3.7}$$

P and Q are compared with the nominal values and multiplied with the corresponding droop coefficients (D_P and D_Q) to generate V_{PCC}* and ω* as shown in (3.8) and (3.9).

$$\omega * = \omega_{nominal} + (P_{nominal} - P).\ D_p. \tag{3.8}$$

$$V_{PCC}* = V_{nominal} + (Q_{nominal} - Q).\ D_q. \tag{3.9}$$

In Figure 3.2, the slope of ω/P droop is set in the way so that $\omega_{niominal}$ = 377 rad/s at $P_{nominal}$ = 100 kW and ω* increases to 380.14 rad/s when P = 50 kW. The slope of the V/Q droop is set in the way so that $V_{niominal}$ = 391.92 V at $Q_{nominal}$ = 10 kvar and V_{PCC}* decreases to 385 V when Q = 20 kvar. These slopes define the droop coefficients, D_P = 1/15915.49 rad/s/kW and D_Q =

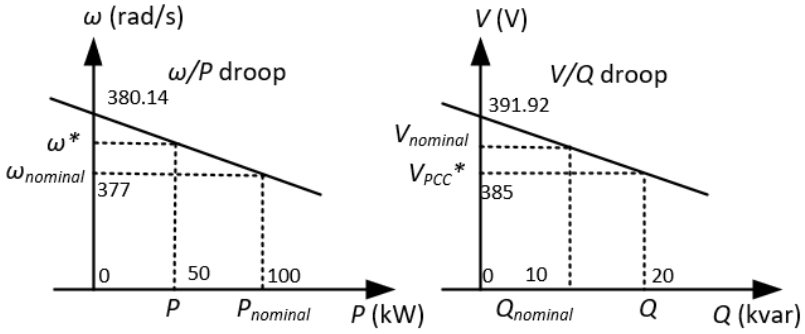


Figure 3.2. Traditional ω/P and V/Q droop characteristics of the system

1/1445.1V/kvar. These droop coefficients in the controller are used as levers to decide the active and reactive power sharing from the parallel-connected GFM inverters system. The parameters of the inverters and controllers are shown in Table III.

3.3. Design and Mathematical Modelling of SME-EDC

The parameter design and the impact of it on stability are described in the following sections.

3.3.1. Design of Voltage Control Loop

The highlighted area in Figure 3.3 is the voltage control loop. From the relation of capacitor current in (3.10), K_C is calculated. ≈

$$iC = C\frac{dV}{dT} \tag{3.10}$$

$$\approx C\frac{\Delta V}{\Delta T} = K_C \Delta V;\ K_C \approx \frac{C}{\Delta T} = \frac{.000025}{.00004}$$

$$K_C = 0.25$$

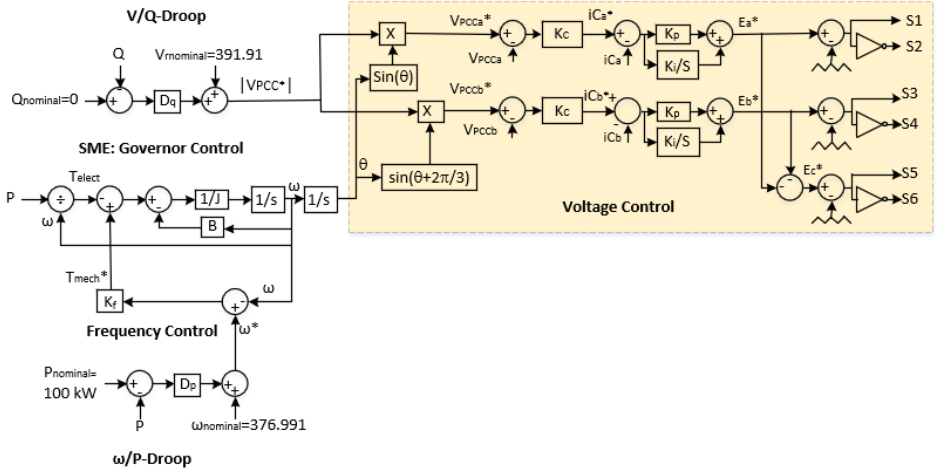


Figure 3.3. Simplified equivalent block diagram of SME-EDC

At corner frequency, f_P, I_L is equal to *iC*. The change in current in the LC filter (loop) is proportional to the change in inductor current. From the relation of inductor voltage in (3.11), K_P is calculated.

$$V_L = L\frac{dI_L}{dT} = L\frac{diC}{dT} \tag{3.11}$$

$$\approx L\frac{\Delta iC}{\Delta T} = K_p\,\Delta iC\ ;$$

$K_P = f_P * L = 1000 * 0.001$

$K_p = 1$

Also, capacitor current can be calculated by integrating the change in capacitor current over time as shown in (3.12).

$$iC = \int \frac{\Delta iC}{\Delta T} dt \tag{3.12}$$

From the relation of capacitor voltage and current (3.13) and (3.12), K_i is calculated.

$$V_C = \frac{iC}{\omega C} \tag{3.13}$$

$$\approx \frac{1}{\omega C}\int \frac{\Delta iC}{\Delta T} dt = \frac{1}{\omega \Delta T C}\int \Delta iC\ dt = K_i \int \Delta iC\ dt;\ K_i = \frac{1}{C} = \frac{1}{0.000025}$$

$K_i = 40000$

The equivalent block diagram of the system and the controller (SME-EDC) is presented in Figure 3.4. The input is the reference voltage (V_{PCC}*) and the output of the system is PCC voltage (V_{PCC}). The simplified transfer function including the physical system, PI control and feed-back capacitor current is $G(s)_2$. The bode plot is shown in Figure 3.5.

$$G(s)_2 = \frac{V_{PCC}(s)}{V*(s)} = \frac{K_c*\left(K_p+\frac{K_i}{s}\right)*\frac{1}{s^2LC+sRC+1}}{1+\left(K_p+\frac{K_i}{s}\right)*\frac{1}{s^2LC+sRC+1}} \tag{3.14}$$

$$= \frac{s*0.25*1+.25*40000}{0.000000025*s^3+0.00000025*s^2+2*s+40000}$$

The transfer function with gain $G(s)_2$ and feedback V_{PCC} is $G(s)_3$. It is shown in Figure 3.6. The bode plot is shown in Figure 3.7

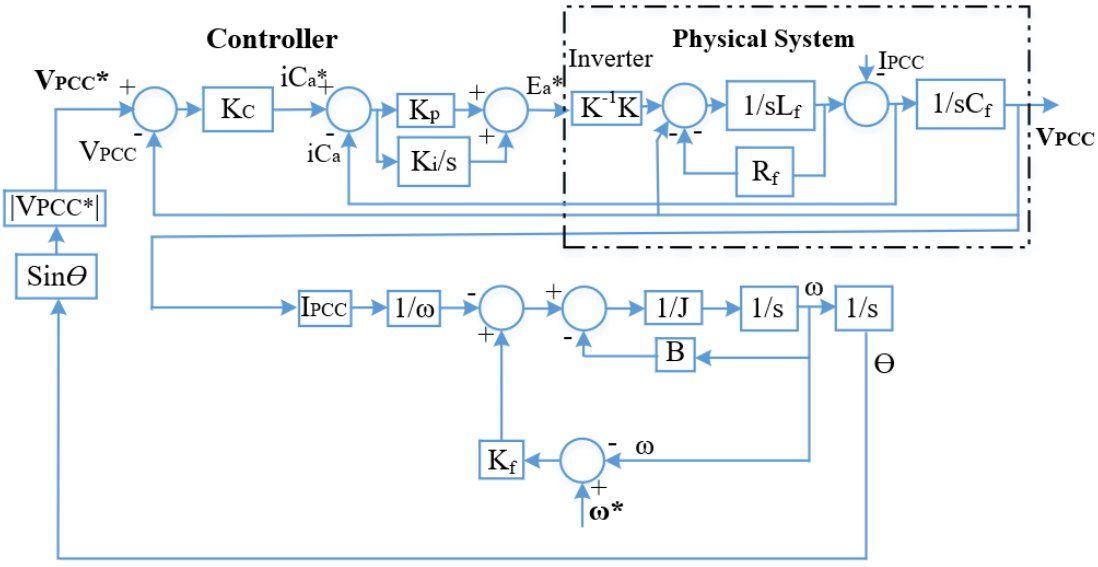


Figure 3.4. Simplified equivalent block diagram of the system (controller and physical system)

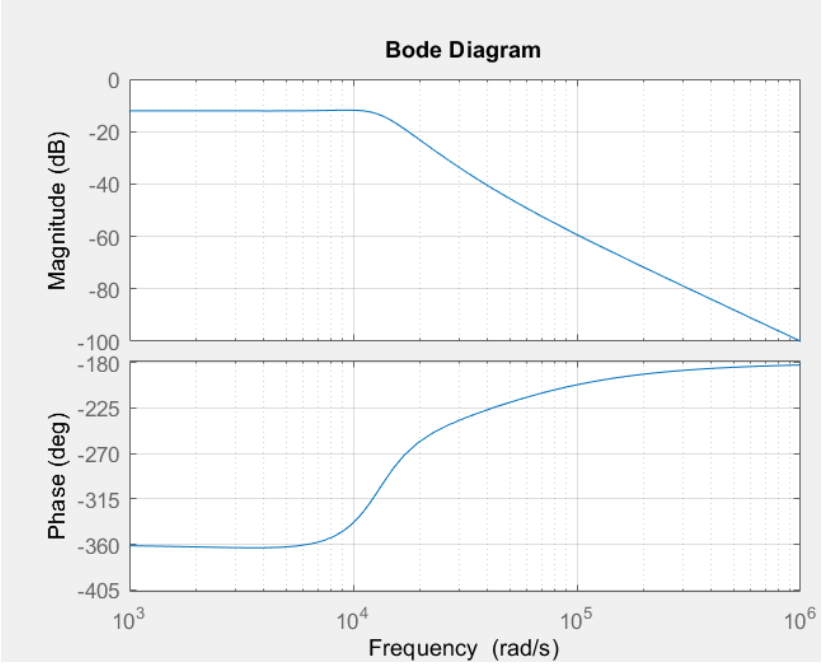


Figure 3.5. Bode plot for $G(s)_2$

$$G(s)_3 = \frac{G(s)2}{1+G(s)2}$$

$$= \frac{s*K_c*K_p+K_c*K_i}{s^3\mathrm{LC}+s^2\mathrm{RC}+s(1+K_p+K_c*K_p)+K_i+K_c*K_i} \quad (3.15)$$

$$= \frac{s*2.5*6.6+2.5*89500}{0.000000025*s^3+0.00000025*s^2+(1+6.6+2.5*6.6)*s+89500+2.5*89500}$$

$G(s)_2$ and $G(s)_3$ are stable because the gain margin is positive, 100 dB (when phase reaches -180^0). If we increase the gain the gain margin still stays positive. We can increase the gain equivalent to 100 dB until it gets unstable.

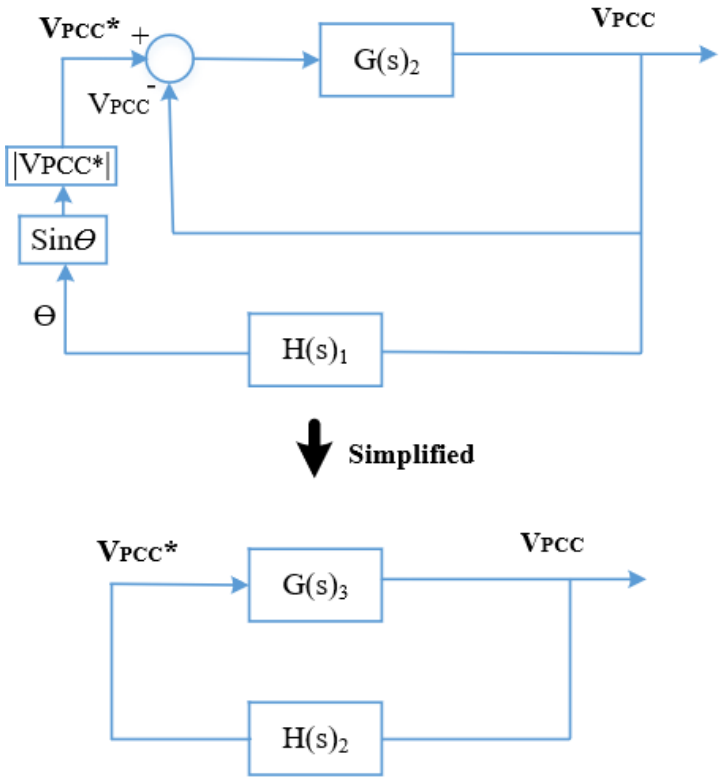


Figure 3.8. Simplified equivalent block diagram of the controller and physical system

From the open loop gain, $G(s)_2$, we can determine the gain of this loop below so that the control loop is stable. So, we can determine the range open loop gain from the relation. Figure 3.8 shows the Simplified block diagram of the system, and controller and physical system.

3.3.1. Design of Virtual Governor Control

The highlighted area in Figure 3.9 is the virtual governor control loop, emulating synchronous machine's operating principle. Here, *J* is virtual inertia constant which can be realized from the following relation.

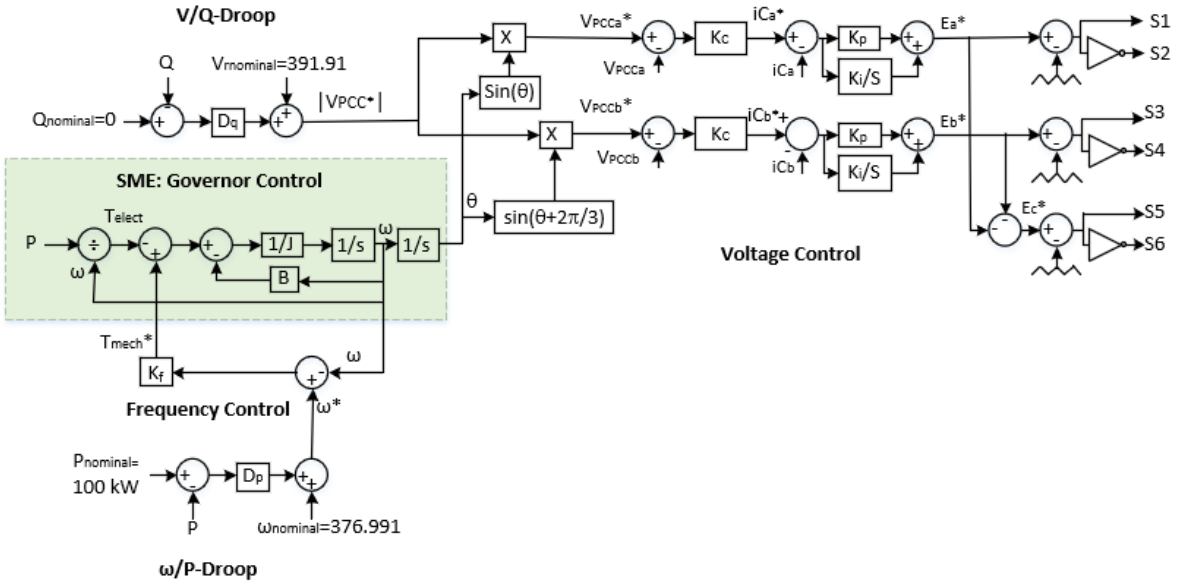


Figure 3.9. Simplified equivalent block diagram of SME-EDC

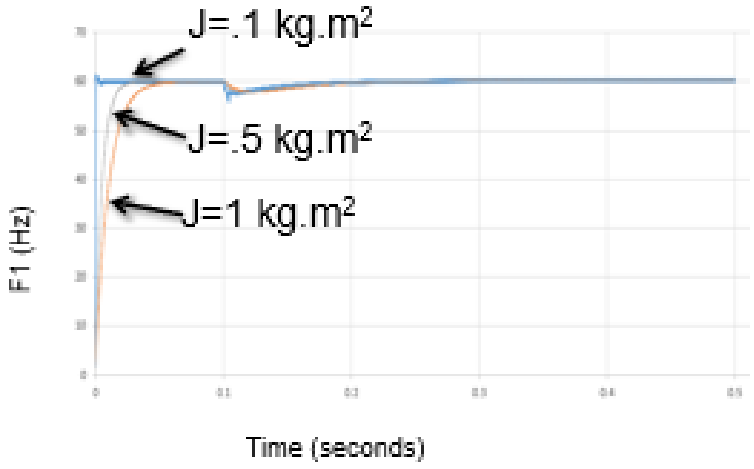


Figure 3.10. Frequency dynamics of SME for various values of *J*

$$J = \frac{1}{2} I r^2 \quad (3.16)$$

Here, For Virtual mass (*I*)=50 Kg, virtual rotor radius (*r*)= 0.2 m, virtual inertia becomes *J*=1 kg.m^2.

Figure 10 shows the frequency response under these variations of *J* =0.1 kg.m^2, 0.5 kg.m^2 and 1 kg.m^2. It is observed that with the increase of its value, the time to reach the steady state increases while increasing the stiffness of the grid under disturbance. Because for *J*=1 kg.m^2, the frequency ripple was minimal during the transient at 0.1 s

$$T_{mech} = T_{elect} + B\omega + J\frac{d\omega}{dt} \quad (3.4)$$

The percentage of damping is considered around 10-20% of the rated torque for a synchronous machine and it follows (3.4). For the SME-EDC, the value of B is chosen as 0.15 which makes the damping, $B\omega$ = 21% of T_{elect}.

The transfer function of the virtual governor control is $H(s)_2$.

$$H(s)_2 = \frac{\theta(s)}{P(s)} = \frac{1}{s\omega(Js+B)} \quad (3.17)$$

From 3.17, the poles are located at 0 and -*B*/*J*.

An increase in the value of *B* will make this controller more stable. For the parameters:

J=1, *B*=0.15, $H(s)_2 = \frac{1}{377*s^2+56.55*s}$

The bode plot of $H(s)_2$ is shown in Figure 3.12. The phase margin is positive; hence it is stable for the chosen parameters.

3.3.3. Design of Frequency Control Loop

The highlighted area in Figure 3.11 is the virtual governor control loop with frequency control loop. The frequency control follows the following relation.

$$T_{mech}* = \omega *- \omega). K_f. \quad (3.5)$$

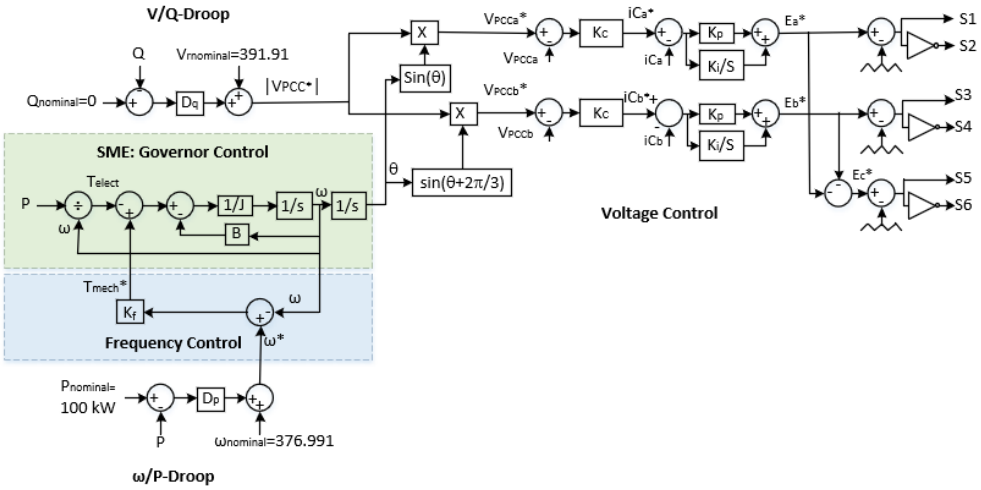


Figure 3.11. Simplified equivalent block diagram of SME-EDC

K_f is chosen as 1000 so that the frequency is controlled at the black-start with allowable frequency ripple = T_{mech}*/K_f= 0.265 rad/s. It generates the appropriate T_{mech}* during transient for the ω /P Droop control.

Considering the frequency control loop, the transfer function for phase-angle determination becomes $H(s)_3$.

$$H(s)_3 = \frac{\theta(s)}{P(s)} = \frac{1}{s\omega(Js+B+K_f)} \tag{3.18}$$

$$= \frac{1}{s^2*377+s*377056}$$

The bode plot of $H(s)_3$ is shown in Figure 3.13. The system is stable as the phase margin is positive and effectively the stability is increased as the pole is shifted further left in the X-axis, i.e., s=0 and s=-1000.15.

3.3.4. Design of Droop Control

The design of droop control is explained in section 3.2.3. The ω/P and V/Q droop relations are shown in (3.8) and (3.9) respectively.

$$\omega * = \omega_{nominal} + (P_{nominal} - P).\ D_p. \tag{3.8}$$

V_{PCC}*= $V_{nominal}$ + ($Q_{nominal}$ - Q). D_q. (3.9)

For a 100 kW 10 kvar inverter the droop coefficients are calculated as D_{P2} = 1/15915.49 rad/s/kW and D_{Q2} = 1/1445.1 V/kvar.

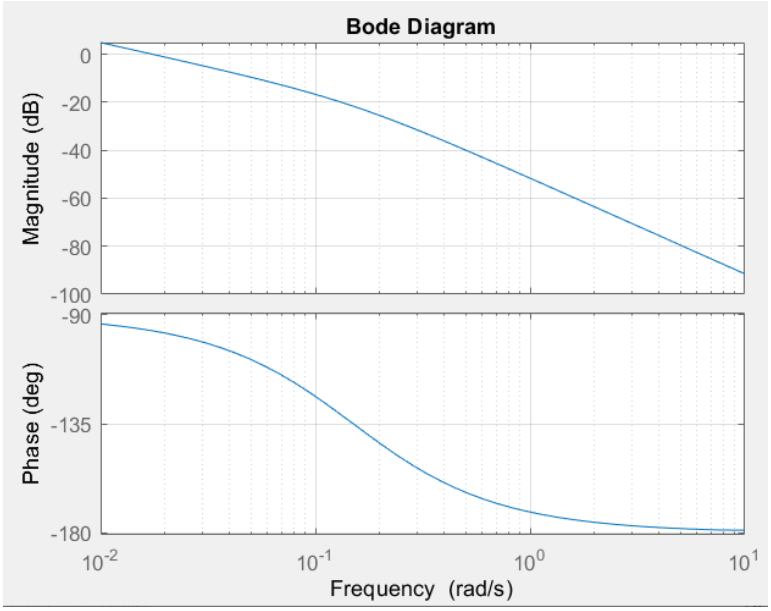


Figure 3.12. Bode plot for $H(s)_2$

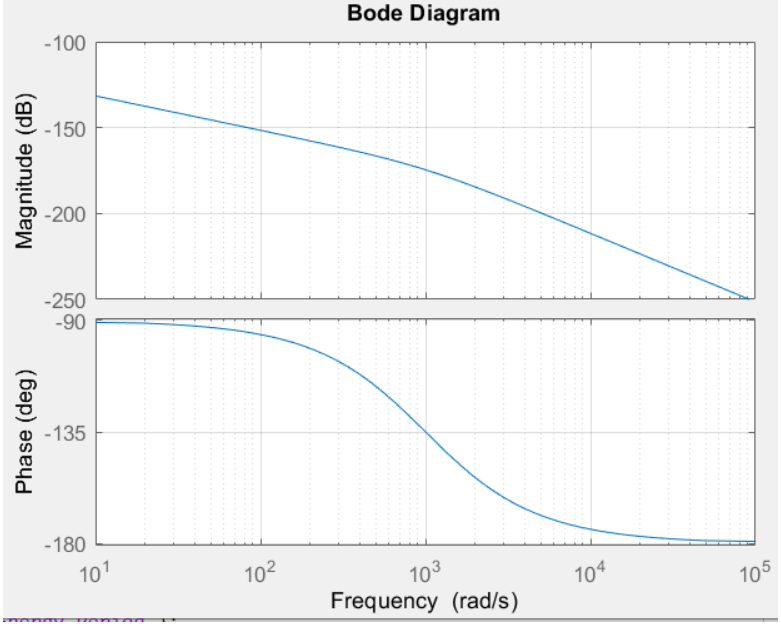


Figure 3.13. Bode plot for $H(s)_3$

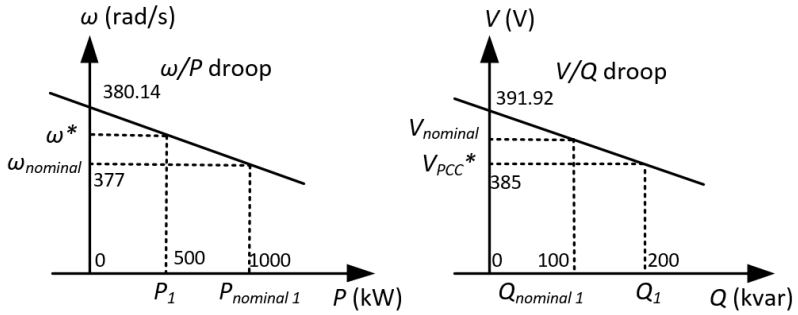


Figure 3.14. ω/P and V/Q droop characteristics for the 1st inverter in the cluster of DERs

For an example cluster of DERs, two inverters have different P and Q ratings (1st Inverter: 1000 kW and 100 kvar; 2nd inverter: 100 kW and 10 kvar) as demonstrated in Figure 3.13.

The inverters follow their corresponding ω/P and V/Q droop characteristics as shown in Figures 3.12 and 3. 14

Following (3.8) and (3.9) and 2nd inverter's droop characteristics, the droop coefficients become, D_{P1} = 1/159154.9 rad/s/kW and D_{Q1} = 1/14451 V/kvar.

It signifies that for the same amount of change of ω, inverter with higher rating will supply higher P.

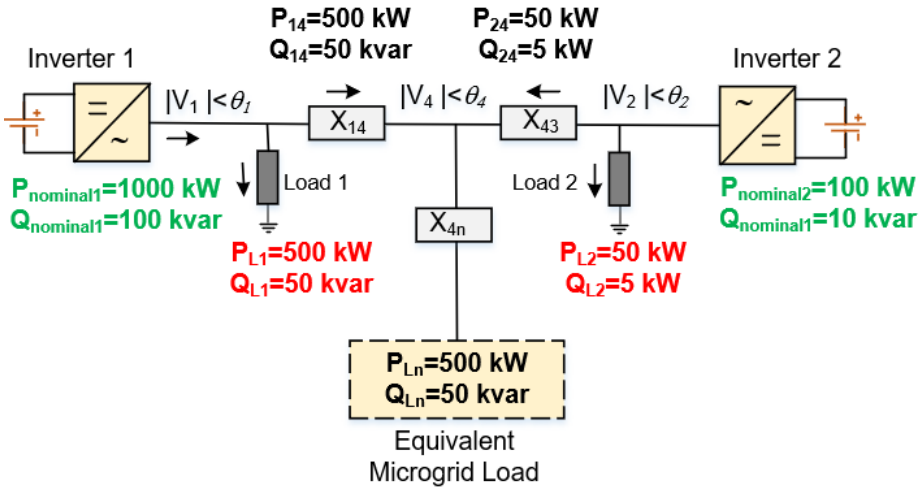


Figure 3.15. A cluster of DERs with two inverters

The general relation of droop and power rating for ‘n’ numbers of inverters are following:

$$P_1D_{P1}=P_2D_{P2}\ldots=P_nD_{Pn} \quad (3.19)$$

$$Q_1D_{Q1}=Q_2D_{Q2}\ldots=Q_nD_{Qn} \quad (3.20)$$

TABLE III
PARAMETERS OF THE INVERTER AND CONTROLLER

Parameter	Values	Parameter	Values
V_{DC}	1000 V	K_C	0.25
$V_{niominal}$	391.92 V	K_f	1000
$\omega_{niominal}$	377 rad/s	K_P	1
L_f	1 mH	K_I	40000
L_g	0.2 mH	J	1 Kg.m^2
C_f	25 uF	B	0.15
R	0.02 Ω	D_P	1/15915.49 rad/s/kW
f_{SW}	10 kHz	D_Q	1/1445.1 V/kvar

CHAPTER 4: COMPARATIVE ANALYSIS OF PHASE-ANGLE DETERMINATION BY PLL, VISMA CONTROLS, DROOP-BASED CONTROLS AND SME-EDC

The comparative dynamic nature of the PLL, VISMA controls and droop-based controls and SME is analyzed in this section

4.1. Operating Principle of PLL

The block diagram of a basic PLL is shown in Figure 4.1 [94]. It consists of a Phase Detector (PD), a low pass filter (LPF), and a Voltage Controlled Oscillator (VCO). From the linearized model of the PLL topology (Figure 4.1), in the closed loop, the calculated phase angle (θ) is compared to the phase angle at PCC (θ_P) to generate the Voltage Error (V_{ER}) in the PD control loop. Filtered signal, V_f is calculated from this error signal in the Low Pass Filter (LPF) control loop. Finally, θ is calculated by integrating the $V_f.K_V$ in the Voltage Controlled Oscillator (VCO) control loop. K_V is an amplification factor. PD can be represented as K_P, LPF can be represented as $\frac{\omega_P}{s+\omega_P}$, VCO can be represented as $\frac{K_V}{s}$. The open loop gain is $G(s)_1$.

$$G(s)_1 = K_P K_V \frac{\omega_P}{s(s+\omega_P)} . \quad (4.1)$$

The following is a detailed study of the various parts of a PLL – The phase detector, Low Pass

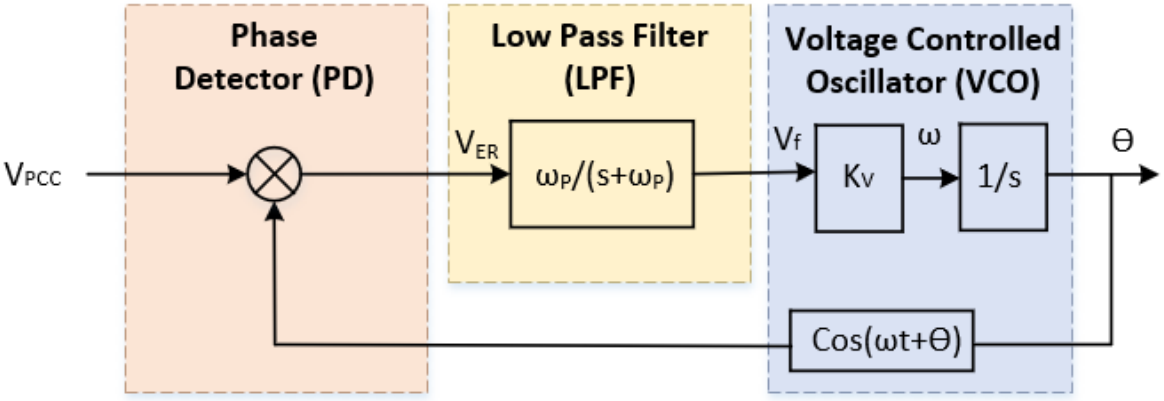


Figure 4.1. Simplified block diagram of PLL topology

Filter and Voltage Controlled Oscillator.

4.1.1. Phase Detector (PD)

The input frequency and the output frequency from VCO are compared by the PD circuit and a DC voltage that is proportional to the phase difference between the two frequencies are generated. PD used in PLLs can be of either analog or digital type. Although most PLL integrated circuits utilize analog phase detectors, it was noted that the majority of discrete phase detectors are of the digital type. One of the most commonly used analog phase detectors is the double-balanced mixer circuit. V_{ER} is the output of this loop as shown below.

$$V_{ER} = V_{PCC}\, Sin(\omega t + \theta_1).\, Cos(\omega t + \theta)$$

$$= \frac{V_{PCC}}{2}(Sin(2\omega t + \theta_1) + Sin(\theta_1 - \theta)) \tag{4.2}$$

4.1.2. Low Pass Filter (LPF)

A LPF is employed in PLLs to eliminate high-frequency components in the output (4.2) of the PD and to filter out high-frequency noise. These attributes render the LPF a crucial element of PLLs, aiding in the management of the circuit's dynamics. These dynamic aspects encompass parameters such as capture and lock ranges, bandwidth, and transient response. The locking range denotes the tracking span within which the PLL's frequency range adjusts to variations in the input frequency, while the capture bandwidth refers to the range in which Phase-Locked Loops achieve phase lock.When the filter bandwidth is reduced, it takes more time to reach the steady state. But this reduces the capture bandwidth. Additionally, it also helps in reducing noise and maintaining the phase-lock through momentary disturbance in signal.

V_f is the output of this loop as shown below.

$$V_f = V_f = \frac{V_{PCC}}{2}(Sin(\theta_1 - \theta) \tag{4.3}$$

4.1.3. Voltage Controlled Oscillator (VCO)

The primary role of the Voltage-Controlled Oscillator (VCO) is to generate an output frequency directly correlated with the input voltage. Consequently, the Phase-Locked Loop (PLL) operates under conditions termed as free-running, capture, and phase lock. The free-running phase was described as the state when no input voltage is applied; however, it was noted that to achieve this state, a reference frequency (ω) must be integrated into the control loop. [95]. Upon the application of the input frequency, the Voltage-Controlled Oscillator (VCO) initiates its adjustment process, resulting in the generation of an output frequency for comparative purposes. This phase is referred to as the capture stage. The comparison of frequencies ceases once the output frequency is aligned to match the input frequency-- a condition termed as the phase-locked state. ω is calculated in the following manner.

$$V_f.K_V = \frac{d\theta}{dt} \tag{4.4}$$

Finally, the phase angle is determined by integrating the frequency. θ is a feedback signal for the phase-angle determination by PLL.

$$\theta = \int V_f \, K_V \, dt \tag{4.5}$$

Finally, the open loop gain of PLL is $G(s)_4$.

$$G(s)_4 = \frac{\theta(s)}{V_{PCC}(s)} = K_V \frac{\omega_P}{s(s+\omega_P)} \tag{4.6}$$

4.2. Phase-Angle Determination by VISMA Control

From the block diagram of VISMA control topology (Figure 4.2), and Laplace Transformation of (4.2), the following representation of θ can be attained.

$$(T_{mech} * - T_{elect}) = J \frac{d\omega}{dt} + B\omega. \tag{4.7}$$

$$\theta = \frac{T_{mech}* - T_{elect}}{Js^2 + Bs}. \quad (4.8)$$

T_{mech}* is the input torque and T_{elect} is the electrical torque. T_{elect} is generated from the measured voltage, current and frequency at the PCC of the inverter in the Electrical Torque Calculator (ETC) control loop. T_{mech}* is a reference in this control loop.

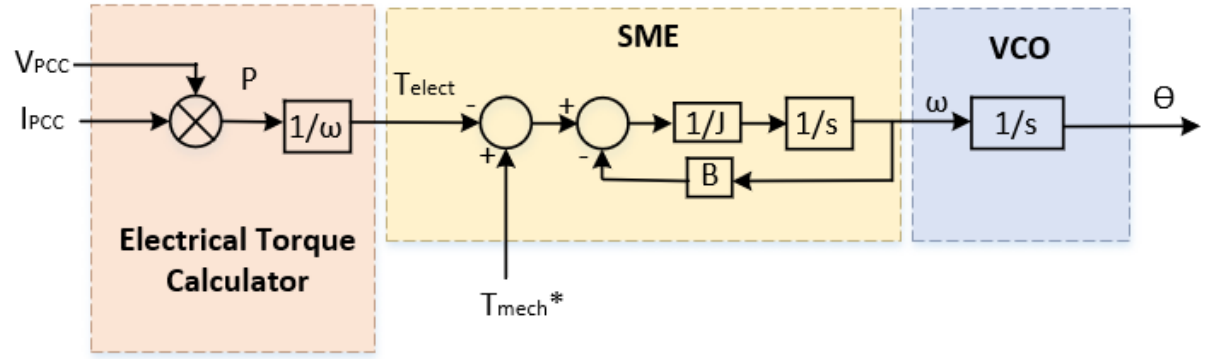


Figure 4.2. Simplified equivalent block diagram of the Virtual synchronous Machine (VISMA) Control

ETC can be represented as $\frac{I_P}{\omega_P}$, SME can be represented as $\frac{1}{Js+B}$, and VCO can be represented as $\frac{1}{s}$. The open loop gain for the SME is $H(s)_2$.

$$H(s)_2 = \frac{\theta(s)}{P(s)} = \frac{1}{\omega.s(Js+B)} \quad (4.9)$$

The used parameters in the control schemes are ω_p=377, J=1, B=0.15, and $|V_{PCC}|$ = 480.

For PLL, the coefficients are ω_P=0.2, K_V=*1*.

Figs. 4.3 and 4.4 show the magnitude and phase response of the open loop gains of the PLL and SME by following (4.6) and (4.9) respectively.

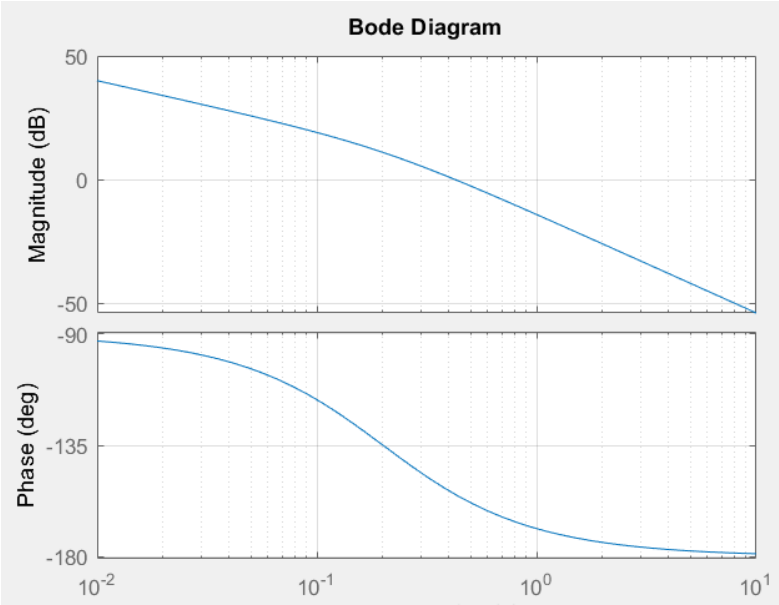


Fig. 4.3. Bode diagram of $G(s)_4$ for PLL topology

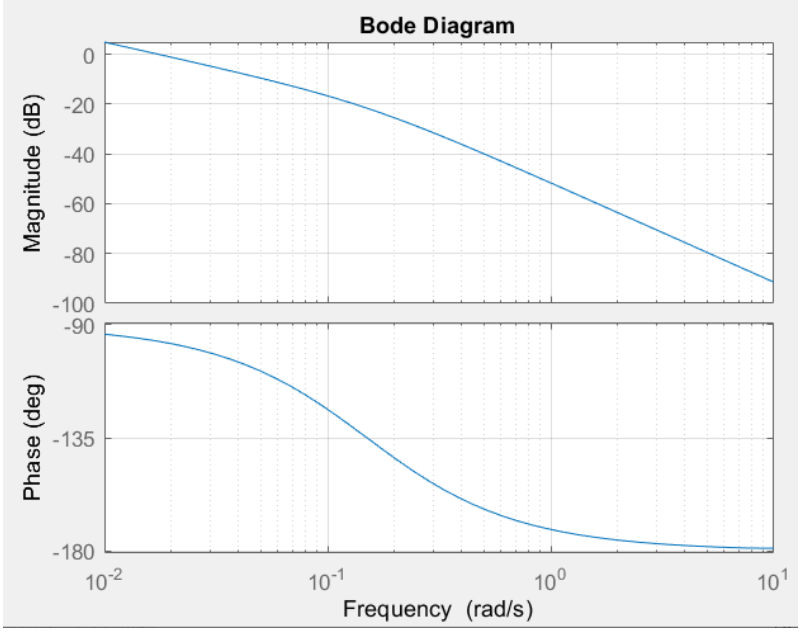


Fig. 4.4. Bode diagram of $H(s)_2$ for VISMA topology

PLL and VISMA give equivalent performance when the following condition is matched:

$$\omega_P = \frac{B}{J} = 0.15 \quad (4.10)$$

and $K_V = \frac{1}{\omega . B} = 0.018$ (4.11)

The key advantages of using SME over PLL in the grid-forming inverters are the following [96].

1. **No Transformation, and No Direct Phase-Angle Control:** PLL uses ABC to DQ transformation whereas SME uses time domain instantaneous value for the phase-angle determination. There is no ABC to DQ transformation, and no direct phase-angle control loop in SME. Hence, it has the capability to provide fast response in phase-synchronization.
2. **Phase-Angle Control by Balancing Torque Equation:** SME uses the torque equation of SM in controlling the ω and determining θ just like a synchronous machine does. The required θ is directly calculated based on the electrical and mechanical torque balancing approach and the required adjustment to the phase-angle is continuously made to maintain the stability of the modern power grid, consisting of large numbers of IBRs.
3. **Distributed Control:** SME-based control does not need a fixed reference of phase-angle. As its operation is fast, it can quickly stabilize the overall system while synchronizing each of the inverters to its corresponding PCC establishing a distributed control architecture. This distributed control architecture will operate without communication, further improving the robustness and security of the grid.
4. **Droop Control Options:** SME has the potential controlling flexibility to further control frequency based on droop characteristics. It has internally generated comparable mechanical torque for control characteristics analysis.

5. **Comparable Dynamic Behavior:** Finally, from the observation of (4.6) and (4.9)-(4.11) and figs. 4.3 and 4.4, SME has a comparable dynamic performance to PLL supporting its capability of determining the phase-angle precisely.

4.3. Frequency Control and Phase-Angle Determination by Mod-VISMA

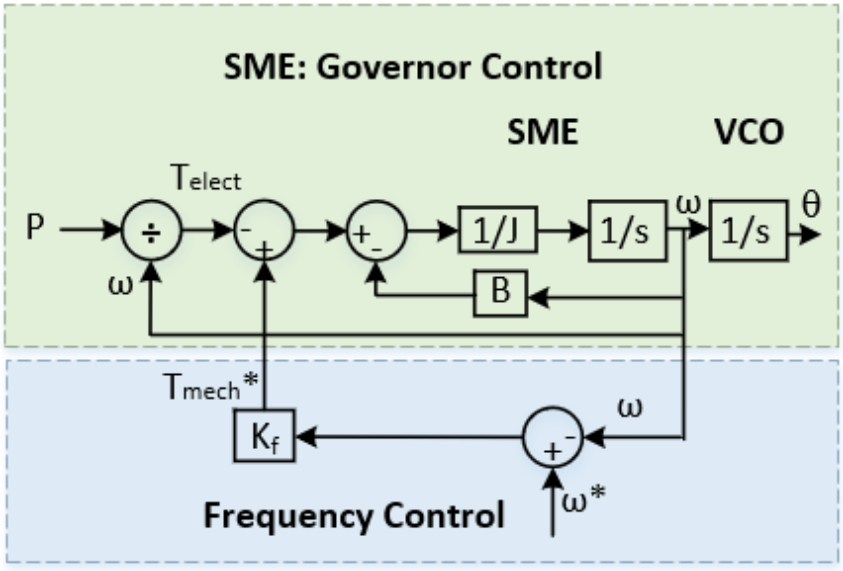


Figure 4.5. Simplified equivalent block diagram of Mod-VISMA with frequency control

The phase-angle is determined by the Mod-VISMA (Figure 4.5) in the same fashion as classical VISMA control does following (4.3). Additionally, *Tmech** is generated in the Frequency control loop by following (4.4). From the principle of an SG, by the approach of balancing these two torques in SME and VCO control loops, the phase-angle, θ is determined.

$$T_{mech}^* = (\omega^* - \omega).\ K_f. \tag{4.4}$$

At the black-start condition, the Frequency control loop generates the reference frequency (ω^*). K_f is the proportional constant. The impact of θ in terms of T_{elect} is controlled to control the phase-angle and stabilize the system.

4.4. Frequency Control and Phase-Angle Determination by SME-EDC

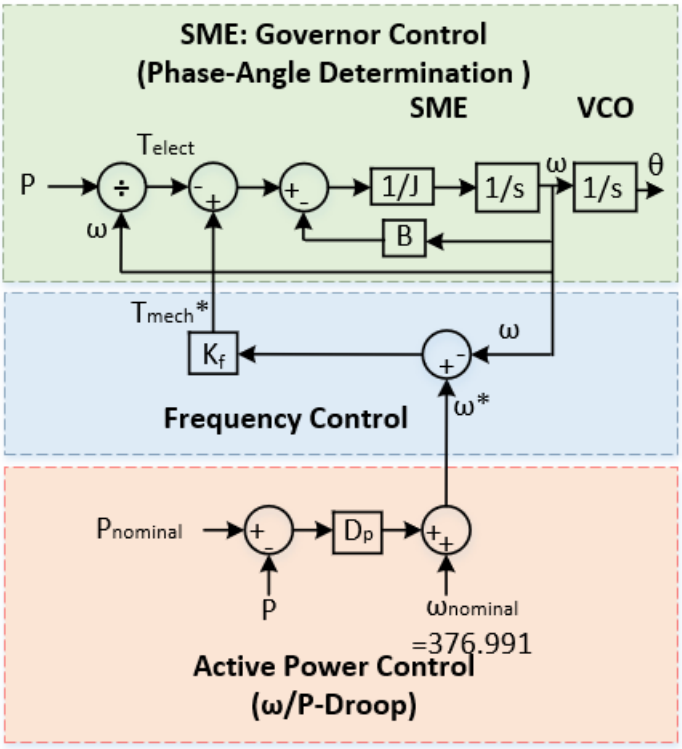


Figure 4.6. Simplified equivalent block diagram of SME-EDC for phase-angle determination (3-layered control)

On top of the phase-angle determination by the SME control loop and frequency control loop, SME-EDC (Figure 4.6) has an active power control loop. ω* is generated by following (3.8) during transient for controlling P. During transient, the consequence of a change in frequency generates T_{mech}* in the frequency control loop. And finally, T_{mech}* controls P and in consequence, phase-angle (θ) is determined.

$$\omega * = \omega_{nominal} + (P_{nominal} - P).\ D_p. \tag{3.8}$$

At steady state, P becomes $P_{nominal}$ and ω* becomes ω_{nominal}.

4.5. Frequency Control and Phase-Angle Determination by Advanced Droop Controls

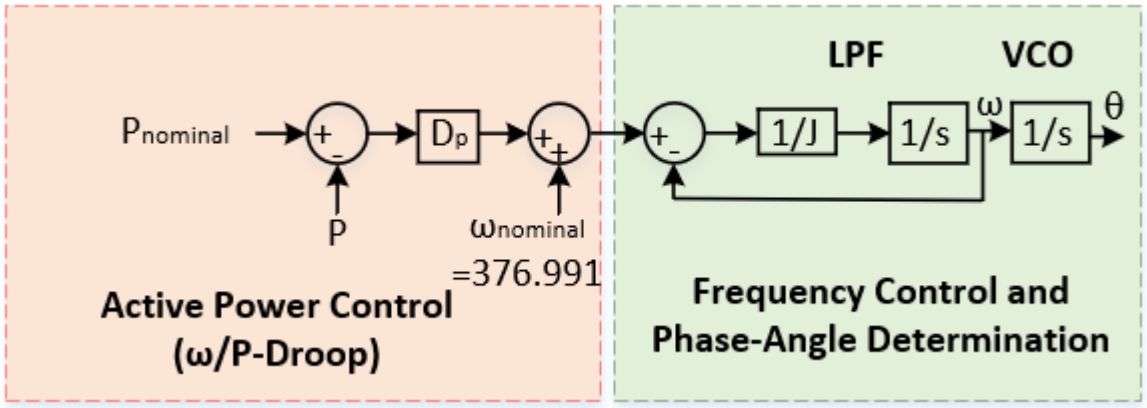


Figure 4.7. Simplified block diagram of an Advanced Droop Control 1

The active power control loop of this droop controller [97] is similar to SME-EDC. However, the 2nd control loop for frequency control and phase-angle determination is dissimilar to SME-EDC.

It controls the frequency at the steady state and controls active power during the transient using the following relation.

$$\omega = \frac{1}{(Js+1)}\,\omega_{nominal} + (P_{nominal} - P).D_P \tag{4.5}$$

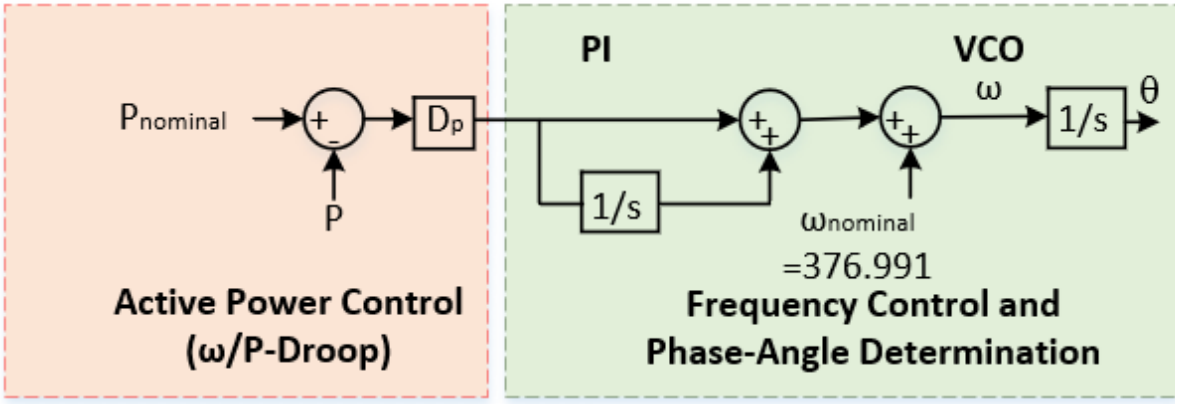


Figure 4.8. Simplified block diagram of an Advanced Droop Control 2

At steady state, $P_{nominal} = P$ and $\omega = \frac{1}{(Js+1)}\,\omega_{nominal}$

Virtual governor control for the phase-angle determination does not exist in this controller.

Another approach of droop control, mentioned in [97] is shown in Figure 4.8. It also has a similar active power control loop compared to SME-EDC. But, instead of virtual governor control in SME-EDC, it has Proportional-Integral (PI) control for frequency control and phase-angle determination.

The droop characteristics of this controller is governed by the following relation.

$$\omega = \omega_{nominal} + (P_{nominal} - P).D_P(1 + \frac{K}{s}) \quad (4.6)$$

Also, because of this, the droop characteristics is non-linear, $D'_P = D_P(1 + \frac{K}{s})$

in compared to SME-EDC.

Table IV shows the summary of Phase-Angle Determination by PLL, VISMA controls, Droop-based controls and SMD-EDC.

TABLE IV
SUMMARY OF CONTROLLERS FOR PHASE-ANGLE DETERMINATION

	Active Power Control (ω/P-Droop)	Frequency Control (ω)	Phase-Angle Determination (θ)
PLL			(1) LPF+ VCO
VISMA	(1)		(2) SME+ VCO
Mod-VISMA		(1)	(2) SME+ VCO
Droop	(1)		
Advanced-Droop	(1)		(2) LPF/PI+ VCO
SME-EDC	(1)	(2)	(3) SME+ VCO

CHAPTER 5: AUTO PHASE-SYNCHRONIZATION BY SME-EDC DURING THE INTERACTION WITH GRID AND OTHER INVERTER

5.1. Active Power Control and Phase-Synchronization Relation

Active Power flow between an inverter and grid can be realized in (5.1). In a test case (Figure 5.1), θ_{12} is 4.93^0 for $P_{nominal1}$=10 kW.

$$P_{12} = \frac{|V_1||V_2|}{X_{12}} \text{Sin}(\theta_{12}) \quad (5.1)$$

But initially, when the inverter is connected to the grid, θ_1 is random (i.e.- θ_{1i}) and it can be greater or less than **4.93^0.** It makes the output power of the inverter, P_1 greater or less than $P_{nominal1}$.

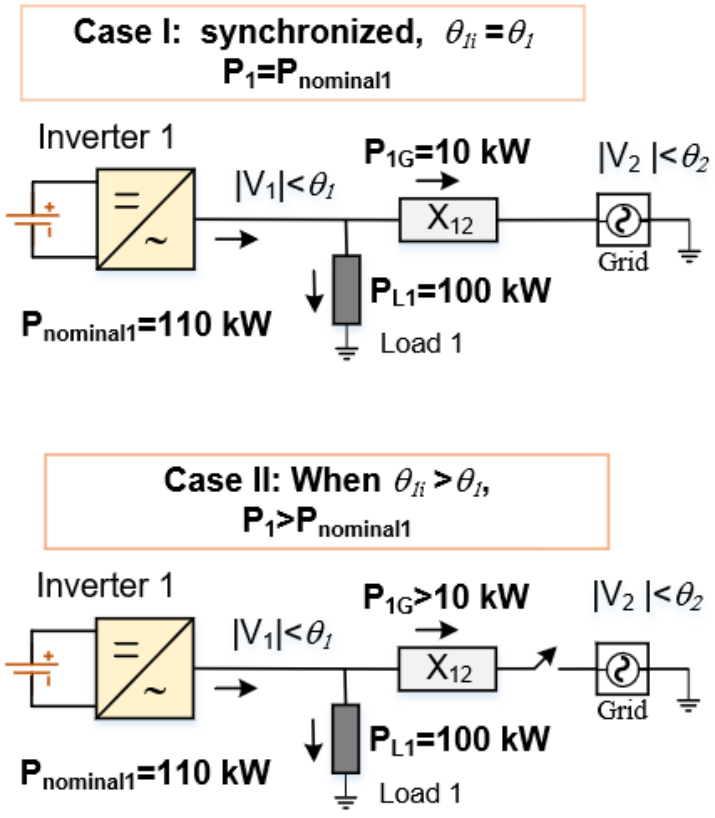


Figure. 5.1. One line diagram of a grid-connected inverter

The objective is to control active power, $P_1 = P_{nominal1}$ and in consequence, synchronize the inverter to the grid, $\theta_{1i} = \theta_1$.

5.2. 3-layered control for phases-synchronization:

The three-layered phase-synchronization by SME-EDC is described below (Fig. 5.2).

At first, in the active power control loop, $\omega *$ is generated for controlling P at transient (3.8). At steady state, $P_{nominal} = P$ and $\omega * = \omega_{nominal}$.

In the frequency control loop, reference virtual torque (T_{mech}*) is generated by $\omega *$ at transient (3.5). At steady state, $\omega = \omega * = \omega_{nominal}$.

In the virtual governor control loop, accelerating torque, T_a ($=T_{mech} * - T_{elect}$) is proportional to angular acceleration ($\frac{d\omega}{dt}$) (3.4).

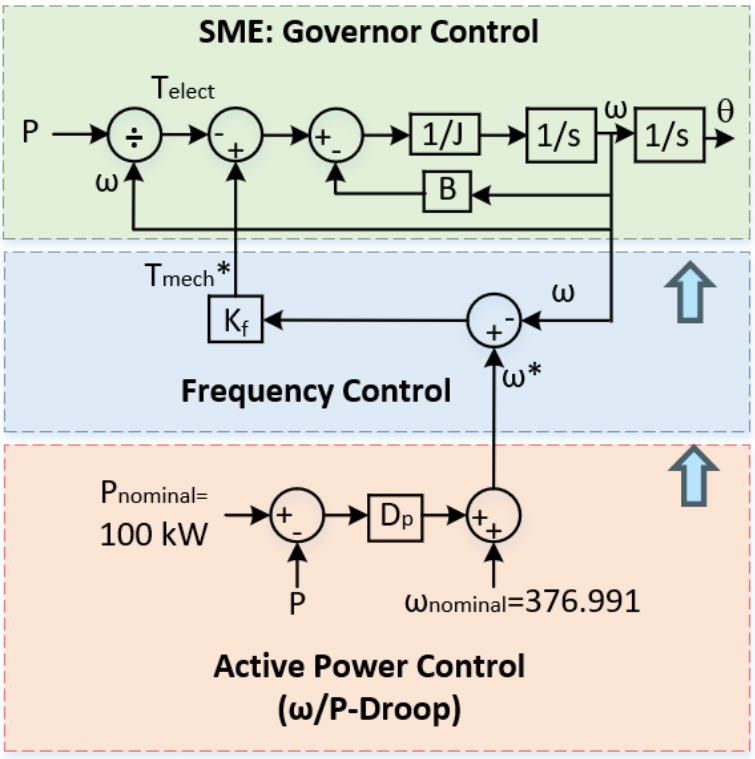
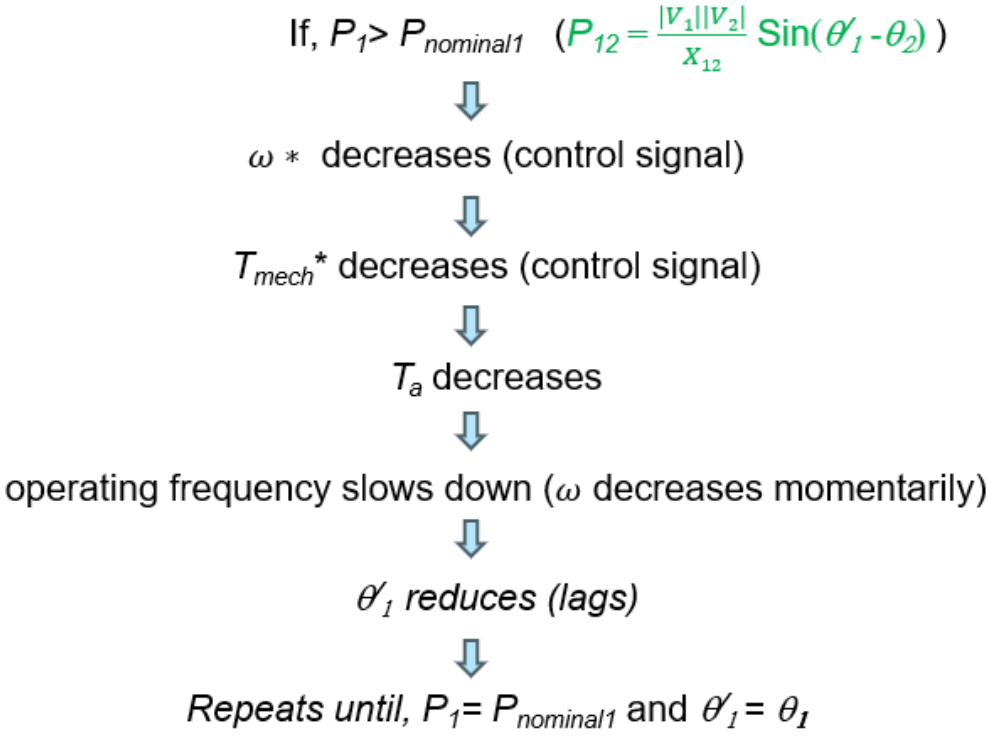


Figure 5.2. Three-layered power, frequency, and phase-synchronization control by SME-EDC

T_{mech}* controls the T_{elect} and in consequence P. In this control loop, based on T_a, the phase-angle (θ) and ω is determined.

For case I (Figure 5.1), the P_{12} is increased at the beginning when the inverter is just connected to the grid as $\theta'_1 > \theta$. i.e. θ'_1 leads θ. In the response, ω* is decreased in the active power control loop in the transient. Next, T_{mech}* is decreased in the frequency control loop and T_a is also decreased in the consequence. As a result, the operating frequency slows down and θ'_1 starts lagging until P_1 is close to $P_{niminal1}$. The summary of the 3-layered control for phase-synchronization is described below.



5.2. Active Power Control and Phase-Synchronization Technique for Multiple Inverters

The nominal power ratings of the inverters in the 3 inverters system are shown in Figure 5.3. The power flow between 1st inverter and bus-4 is P_{14}. And the general power flow between Bus-m and bus-n is P_{mn}.

$$P_{mn} = \frac{|V_m||V_n|}{X_{mn}} \text{Sin}(\theta_m - \theta_n) \tag{5.2}$$

$$P_{14} = \frac{|V_1||V_4|}{X_{14}} \text{Sin}(\theta_1 - \theta_4) = 50 \text{ kW} \tag{5.3}$$

From (5.3), the phase angle of voltage at PCC 1 is $\theta_1 = \text{Sin}^{-1}(.086) = \boldsymbol{25.72^0}$, considering, $q_4 = \mathbf{0^0}$, $|V_1| = ||V_4| = 480$ V, and $X_{14} = 2\ \Omega$.

Following (5.2) , $\theta_2 = \boldsymbol{0^0}$ *and* $\theta_3 = \boldsymbol{-25.72^0}$.

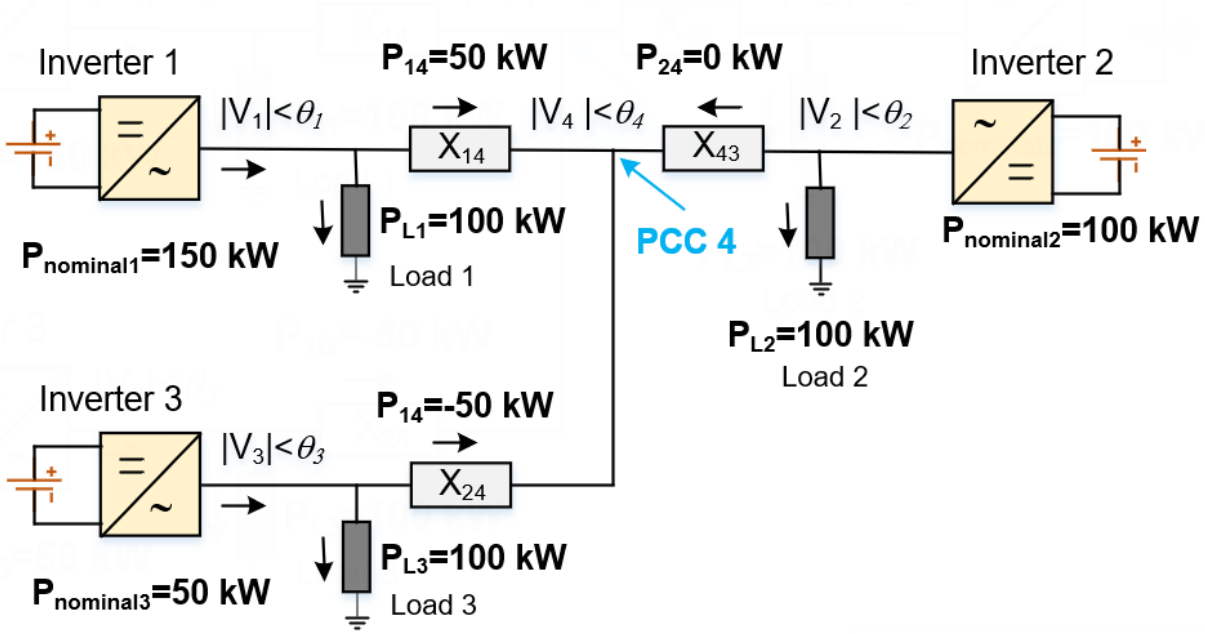


Figure 5.3. Phase-synchronization for 3 inverters system

In conclusion, $(\theta_m - \theta_n)$ for each of the inverters are controlled by controlling control P_{mn} for each inverter. The objective is to control active power of Inverter m is $P_m = P_{nominal\ m}$.

and in consequence, synchronize the inverter to the required phase angle, $\theta_{mi} = \theta$.

CHAPTER 6: MODELING, RESULTS AND TECHNICAL DISCUSSION

In the simulation (MATLAB/Simulink) model, each of the inverters has one designated controller without communication with each other to control the respective V_{PCC} and f. As the inverters and the corresponding controllers are simulated in a single Simulink model, the internal references of the sine function generators (refer to 2nd control loop of SME-EDC) are already synched irrespective of switching the inverters at different instances. For this reason, the initial phases of the internal sine references of the controllers are manually changed to demonstrate the communication-less control capability of the controllers.

6.1. Case I & Case II: Auto-Phase Synchronization in the Grid-Connected Mode

The three-layered control of active power and phase-synchronization as discussed in Chapter 5 (Figures 5.1-5.3) is demonstrated in simulation in Fig. 6.1. It shows the increase of initial inverter output power (P) at 0.1 s when it is connected to the grid in Figure 6.1(a). Figure 6.1(b) shows that

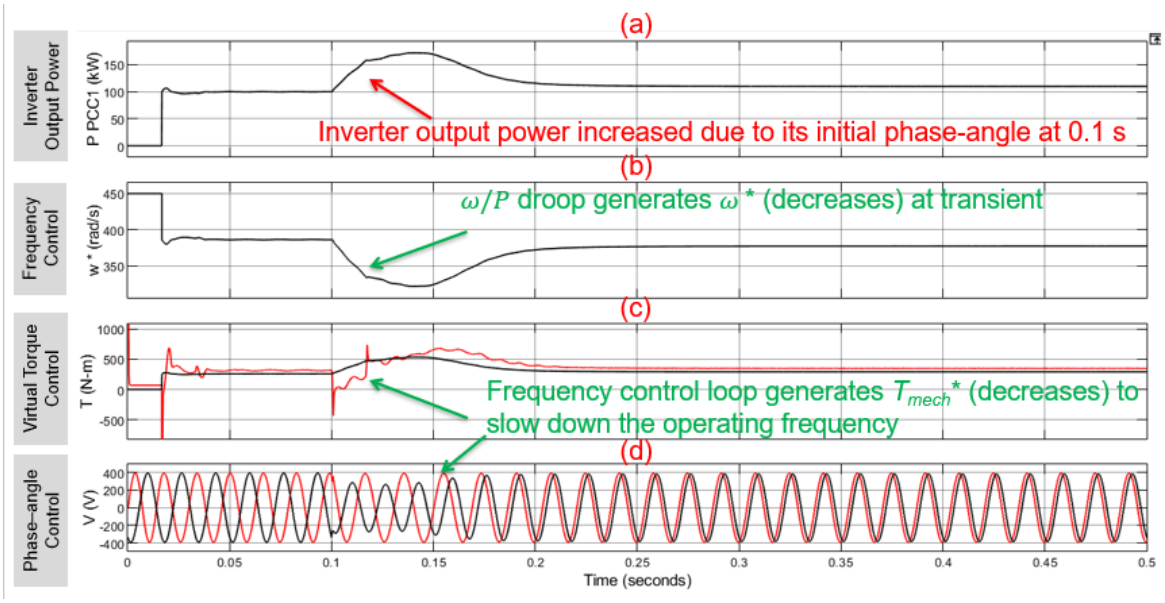


Figure 6.1. Profiles of P_{PCC1}, ω *, T_{mech}*, T_{elect}, V_{PCCa} and V_{ga} of the 1st inverter showing the phase-synchronization mechanism in **Case I** and **Case II**

ω * is decreased during the transient which is the controlled signal by the droop control loop. Figure 6.1(c) shows the control action by the frequency control loop in terms of change in T_{mech}*. At transient, T_{mech}* is decreased momentarily to control T_{elect}, and in consequence inverter output power, P. However, at steady-state, T_{mech}* is bigger than T_{elect} and T_a depends on the control parameter design ($B\omega$). Profiles of V_{PCCa} and V_{ga} of the 1st inverter show the impact of phase-synchronization by SME-EDC in Figure 6.1(d).

6.2. Case III: Grid Formation, Black-Start and Phase-Synchronization Capability for two Inverters

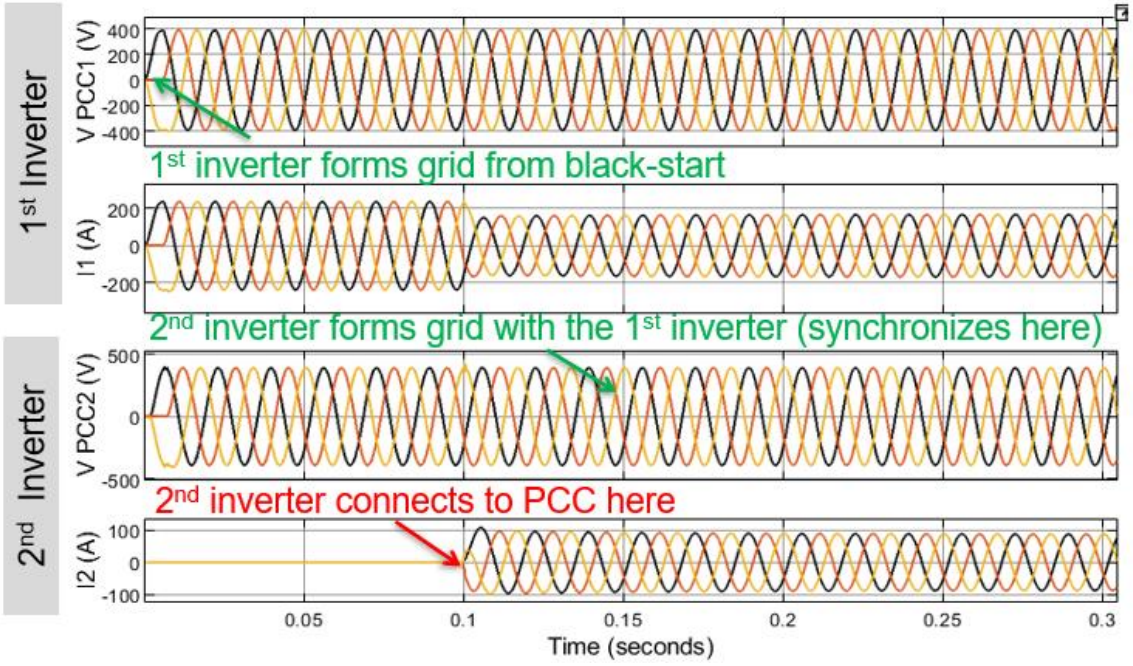


Figure 6.2**.** Profiles of V_{PCC1}, $I1$, V_{PCC2}, and $I2$ from the two parallel-connected GFM inverters while controlled by SME-EDC in **Case III** (Grid formation Black-start and phase-synchronization from 30^0 phase difference)

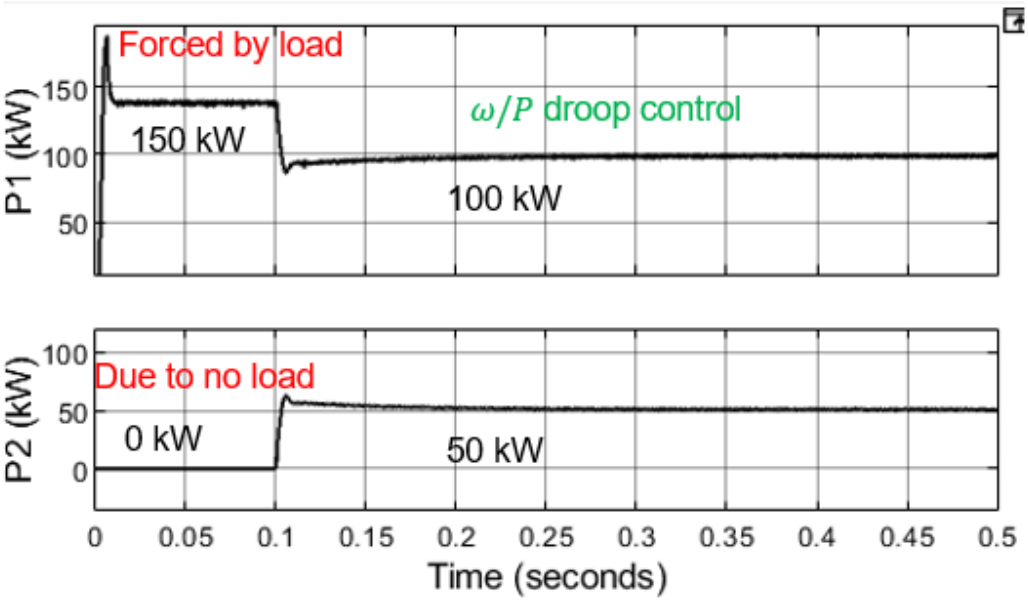


Figure 6.3. Profiles of *P1* and *P2* from the two parallel-connected inverters while controlled by SME-EDC in **Case III**

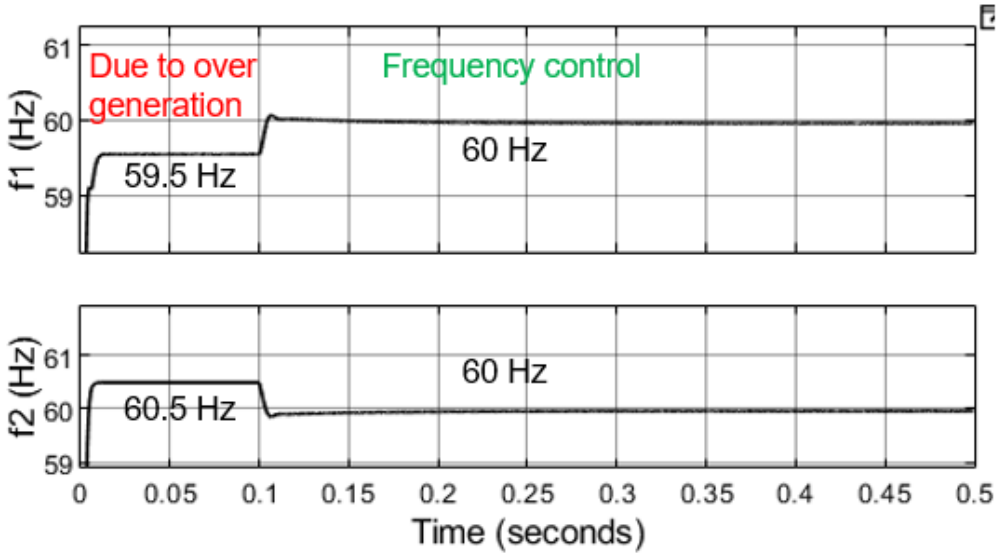


Figure 6.4. Profiles of *f1 and f2* from the two parallel-connected inverters while controlled by SME-EDC in **Case III**

Referring to Figure 2.1, initially, Breakers 1 is 'closed' to form the grid from the black start by the 1st inverter in the two inverters system. Grid Breaker is 'opened'. 2nd Inverter is connected to

the rest of the system at 0.1 s by closing Breaker 2. Load 1 and Load 2 are 100 kW and 50 kW respectively. Figure 6.2 shows how the 1st inverter black starts from 0 s and forms the 3-phase voltage. The internal reference for the sine function generator in the 2nd inverter's controller is 30^0 leading to the 1st inverter's controller. At 0.15 s, both inverters' voltages are synchronized.

6.3. Case III: Power Sharing Capability by the Droop Control

Figure 6.3 shows the profiles of the output power of the inverters (*P1* and *P2*) to fulfill Load 1= 100 kW and Load 2= 50 kW. References of the inverters are $P_{niminal1}$=100 kW and $P_{nominal2}$=50 kW. At 0 s, only the 1st inverter is connected to the loads in the two-inverter system and supplies the total load, 150 kW in Figure 6.3. Following its droop equation (12), its operating frequency becomes 59.5 Hz as shown in Figure 6.4 due to over generation. At 0.1 s, Breaker 2 is closed (Fig. 2), and from 0.15 s the 2nd inverter supplies 50 kW while, 1st inverter supplies 100 kW. After 0.15 s, both inverters operate at the nominal frequency (60 Hz) in Fig. 6.4.

6.4. Case IV: Dynamic Load Condition and Capacitor Current Control

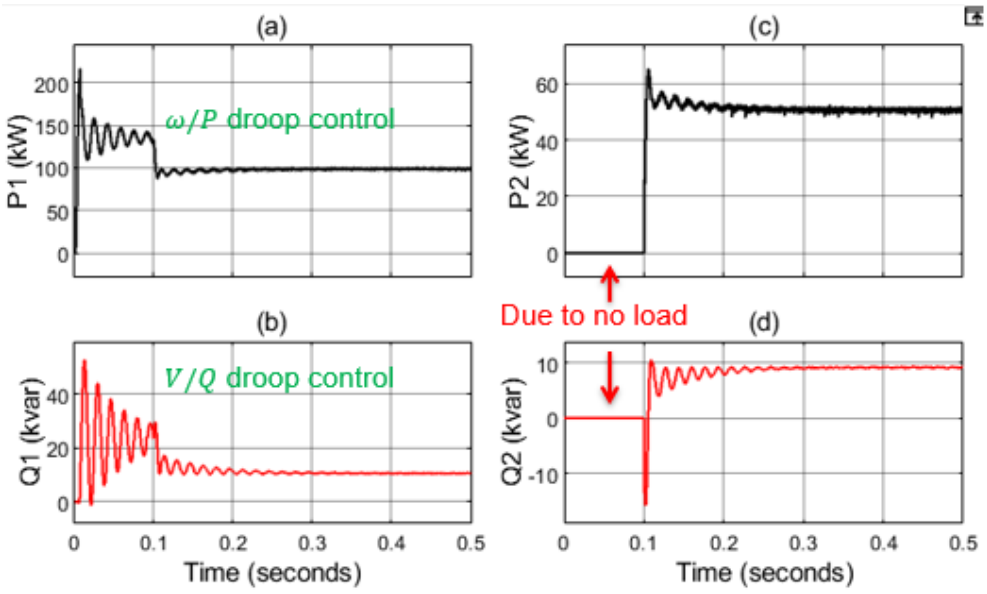


Figure 6.5**.** Profiles of Q*1* and Q*2* from the two parallel-connected inverters while controlled by SME-EDC in **Case IV**

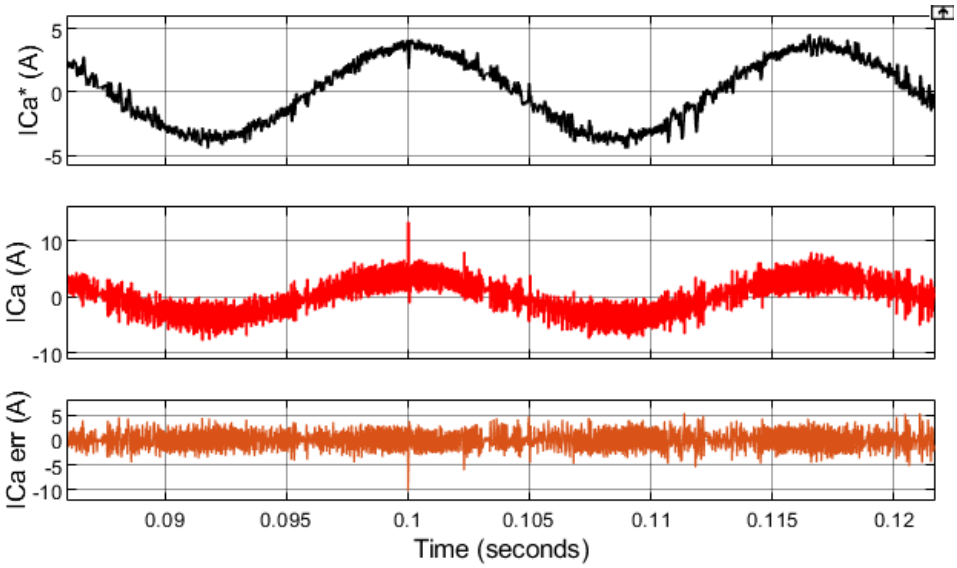


Figure 6.6. Profiles of reference capacitor current, measured capacitor current and error signal of the 1st inverter in **Case IV**

In Case IV, reactive powers 10 kvar is added to each of Load 1 and Load 2 while active powers are maintained as same as shown in Case III. Also, $Q_{nominal}$ for both the inverters is set as 10 kvar. Figure 6.5 shows the active and reactive power shared by the two inverters in this case. It shows that inverters control the reactive powers after 0.2 s.

Figure 6.6 shows the profiles of reference capacitor current, measured capacitor current and error signal during the transient at 0.1 s in Case IV. The filter capacitor current is controlled for accurately controlling the inverter output voltage to overcome the impact of the load changes on the inverter quickly. It enables the inverter to respond more effectively during dynamic loads. It is often termed as dynamic stiffness. However, it has a tolerance of ±3 V (*ICa_err*).

6.5. Virtual Inertia Capability

The virtual moment of inertia, J is varied while keeping other control parameters fixed as in Case I. Figure 6.7 shows the frequency response under these variations of J =0.1 kg.m^2, 0.5 kg.m^2 and 1 kg.m^2. It is observed that with the increase of its value, the time to reach the steady state

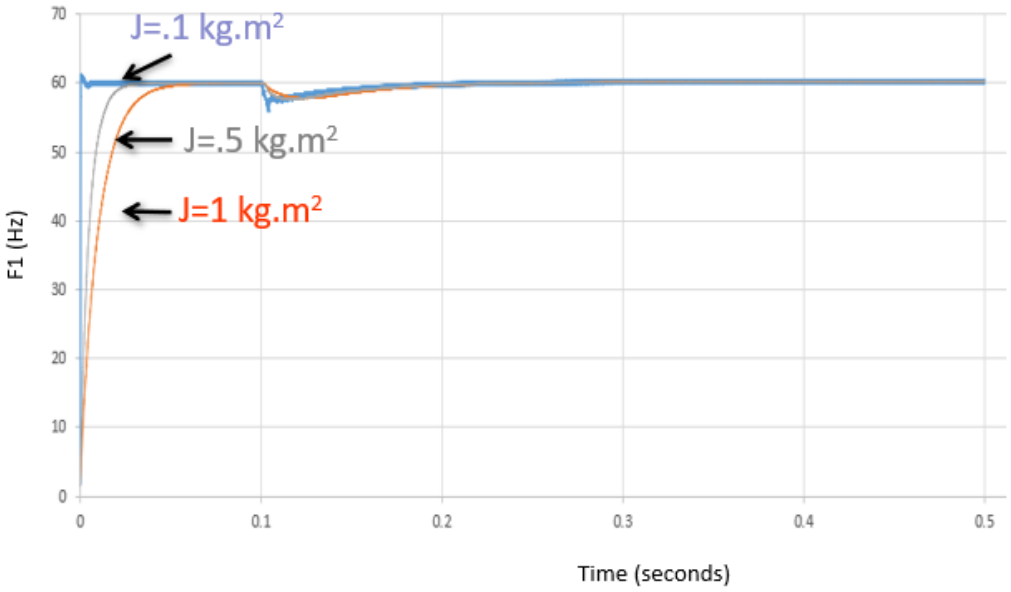


Figure 6.7. Profiles of *f1* under various values of moment of inertia, *J* while controlled by SME-EDC in **Case V (**Virtual inertia capability)

increases while increasing the stiffness of the grid under disturbance. Because for J=1 kg.m^2, the frequency ripple was minimal during the transient at 0.1 s (Fig. 18). However, *J*=.1 kg.m2 provided the fastest transient response for the inverter.

6.6. Voltage Ride-through Capability

In Case VI, consisting of 1st inverter and grid, the inverter is connected to the grid at 0.1 s as shown in Fig. 20. From 0.15-0.25 s, the grid voltage is increased from 480 V to 550 V. Figure 6.8 shows the voltage ride through capability of the proposed controller which is an essential criterion of a grid-forming inverter, connected to the grid according to the current standards. It shows that the inverter output voltage is stable under the short-term voltage disturbance.

6.7. Grid-Connected Three Inverters System

Breakers 1, 2 and 3 are ‘opened’ at the beginning and are ‘closed’ at 0.1 s to connect the three inverters to the grid simultaneously. At that instant, the voltage phases of the inverters were 300 leading from the grid voltage. Figure 6.9 shows that at 0.35 s, the inverters are synchronized to the

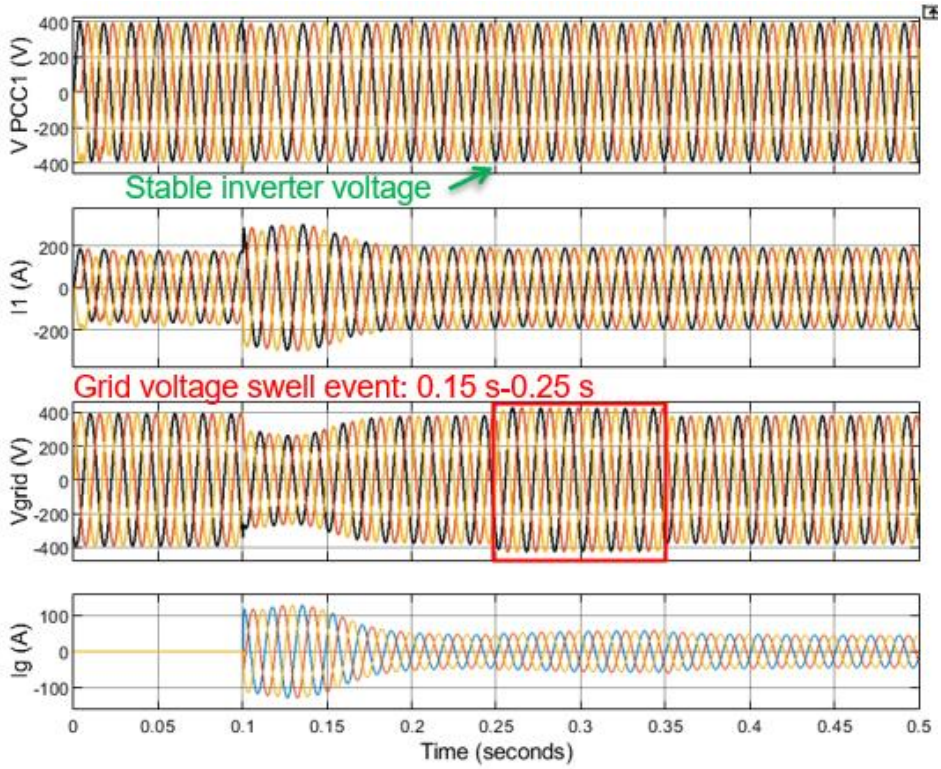


Figure 6.8. Profiles of *f1* under various values of moment of inertia, *J* while controlled by SME-EDC in **Case VI (**Virtual inertia capability)

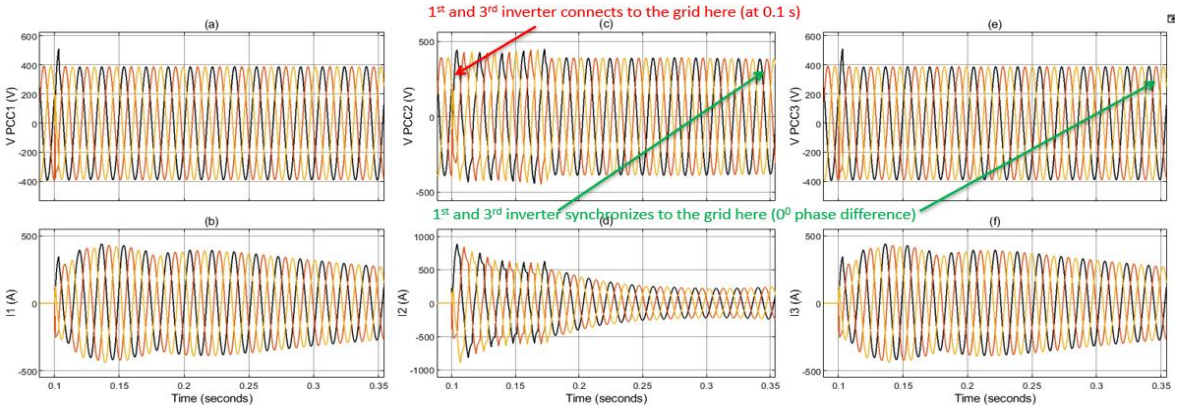


Figure 6.9. Profiles of V_{PCC1}, *I1*, V_{PCC2}, *I2*, V_{PCC3}, and *I3* by the three parallel-connected GFM inverters while controlled bv SME-EDC in **Case VII**

grid voltage and the disturbances are quenched. It is observed that the voltage profile of the 2nd inverter was impacted (shape is distorted) the most as the grid is located closest to it (Fig. 2).

CHAPTER 7: EXPERIMENTAL VALIDATION OF THE SME-EDC

7.1. Experimental Validation by Control-Hardware-in Loop (CHIL) Experiment

In the (Control-Hardware-in-Loop) CHIL experiment, the power electronics components (two parallel-connected inverters, LC filters, breakers, DC power supply) are modeled in the Digital Real-Time Simulator (DRTS), Typhoon HIL 604 [98-100] and the inverters are controlled by two independent controllers which are programmed and operated by two separate computers as shown in Figure 7.1. Configuration: Number of cores in Typhoon HIL 604 is 8. The processing speed is up to 2 MHz. The total number of analog output pins is 32 (±10 V), analog input pin is 32 (±10 V), the total number of digital input pins is 32 (±15 V), and digital output pins is 32 (±5 V)

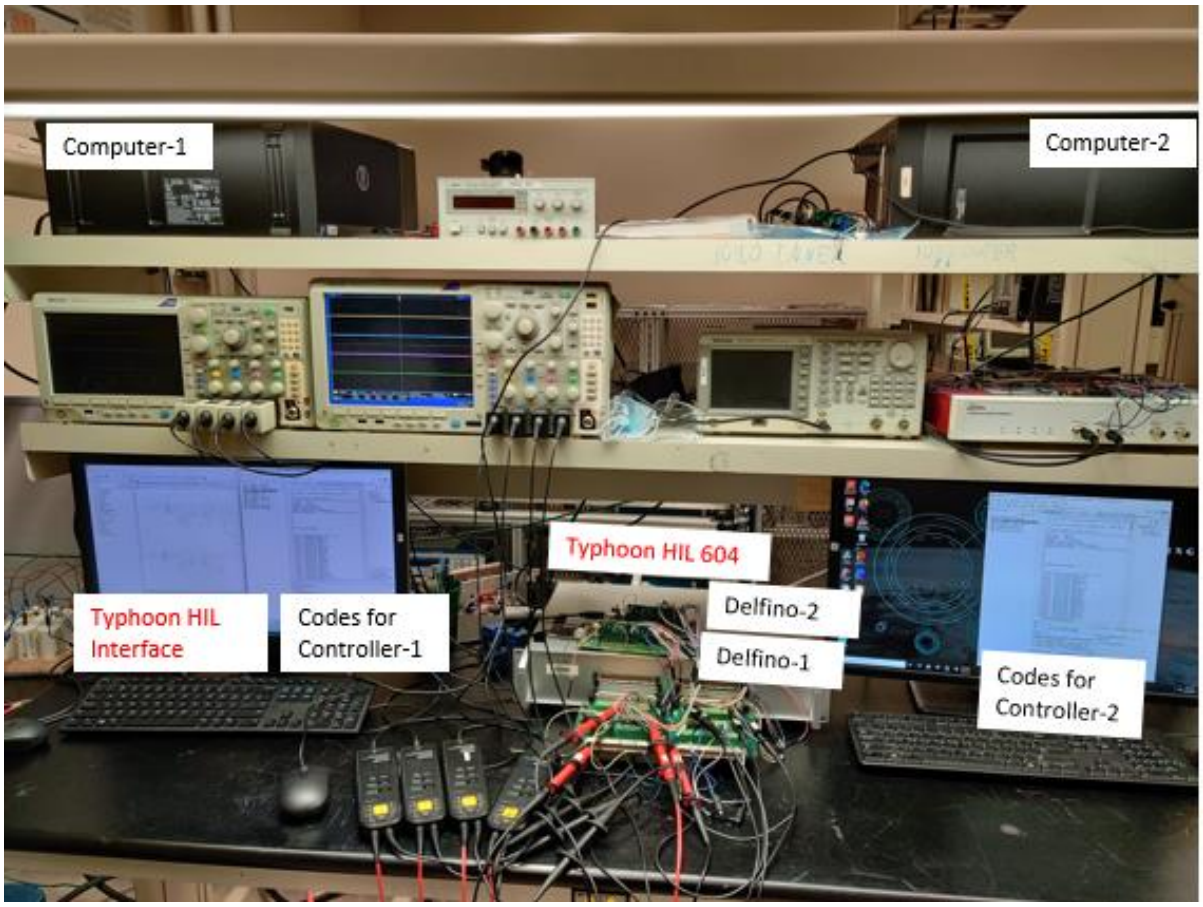


Figure 7.1. Experimental setup with Typhoon HIL 604 and Delfino controllers

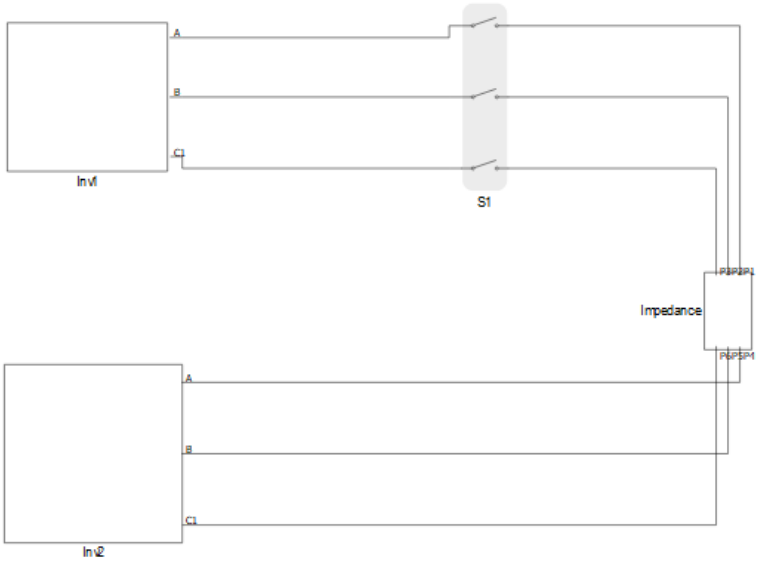


Figure 7.2. Schematic diagram of two parallel connected inverters in Typhoon HIL

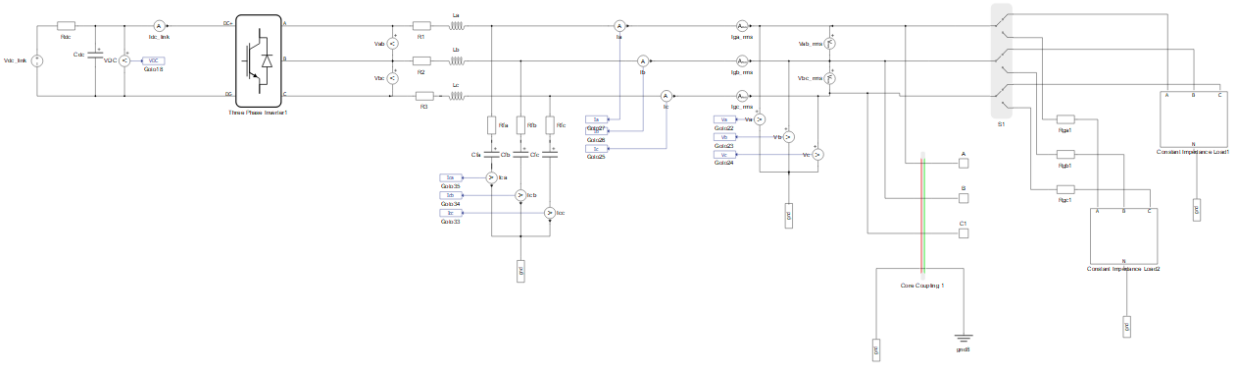


Figure 7.3. Schematic diagram of the 1st inverter in details

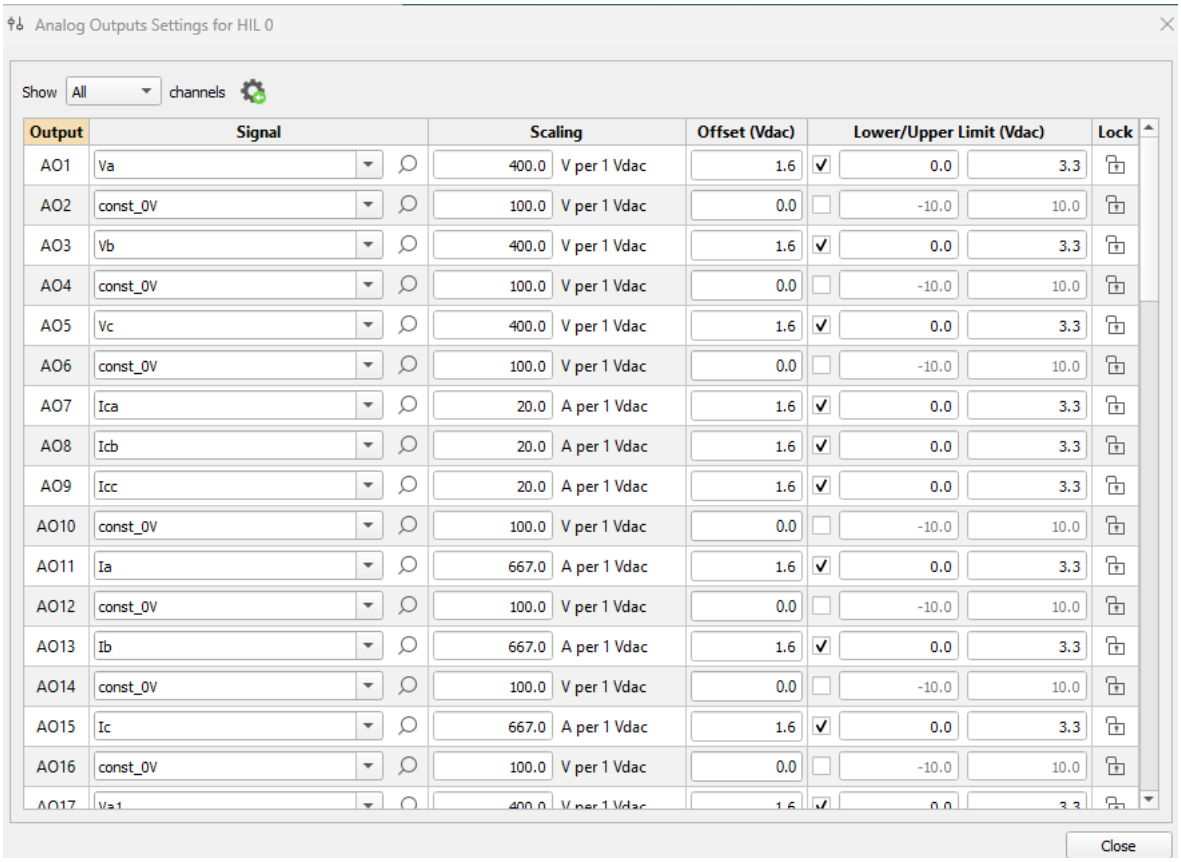
7.1.1. Modeling the Power Stage in Typhoon HIL 604

The power stage, (power electronics components) is modeled in the 'Schematic' interface of the Typhoon HIL software in the 604 setting as shown in Figures 7.2 and 7.3. In addition to two

3-phase inverters, DC power supplies, and LC filters, the model has core-coupling which separates the model to avoid overload in the cores of the Typhoon HIL 604.

7.1.2. Signal Conditioning process and scaling in Typhoon HIL 604

Signal conditioning is part of the electronic data acquisition process which includes scaling and shifting before feeding the analog signal for Analog to Digital Conversion (ADC). ADC samples the analog signal into the digital signal. The measured inverter voltage, current and capacitor current are processed through the signal conditioning in the SCADA panel of the Typhoon HIL as shown in Figure 7.4. The goal of the signal conditioning is to transform the feedback analog signals within the range of 0- 3.3 V so that they can be fed to the DSP controller



Output	Signal	Scaling	Offset (Vdac)	Lower/Upper Limit (Vdac)	Lock
AO1	Va	400.0 V per 1 Vdac	1.6	☑ 0.0 3.3	
AO2	const_0V	100.0 V per 1 Vdac	0.0	☐ -10.0 10.0	
AO3	Vb	400.0 V per 1 Vdac	1.6	☑ 0.0 3.3	
AO4	const_0V	100.0 V per 1 Vdac	0.0	☐ -10.0 10.0	
AO5	Vc	400.0 V per 1 Vdac	1.6	☑ 0.0 3.3	
AO6	const_0V	100.0 V per 1 Vdac	0.0	☐ -10.0 10.0	
AO7	Ica	20.0 A per 1 Vdac	1.6	☑ 0.0 3.3	
AO8	Icb	20.0 A per 1 Vdac	1.6	☑ 0.0 3.3	
AO9	Icc	20.0 A per 1 Vdac	1.6	☑ 0.0 3.3	
AO10	const_0V	100.0 V per 1 Vdac	0.0	☐ -10.0 10.0	
AO11	Ia	667.0 A per 1 Vdac	1.6	☑ 0.0 3.3	
AO12	const_0V	100.0 V per 1 Vdac	0.0	☐ -10.0 10.0	
AO13	Ib	667.0 A per 1 Vdac	1.6	☑ 0.0 3.3	
AO14	const_0V	100.0 V per 1 Vdac	0.0	☐ -10.0 10.0	
AO15	Ic	667.0 A per 1 Vdac	1.6	☑ 0.0 3.3	
AO16	const_0V	100.0 V per 1 Vdac	0.0	☐ -10.0 10.0	
AO17	Va1	400.0 V per 1 Vdac	1.6	☑ 0.0 3.3	

Figure 7.4. Signal Conditioning (Scaling and shifting) in Typhoon HIL PIN configuration

(Delfino). PCC voltages are scaled 1/400, PCC currents are scaled 1.5/1000 and the capacitor currents are scaled 1/20 and then each of them is added to 1.6 V for the signal conditioning.

#Note: The breaker board and the pins connected with the Typhoon HIL machine should not be modified/disturbed when the real-time simulation in the Typhoon HIL is turned on.

7.1.3. Microcontroller

Two Delfino F28335 digital controllers are used as the controllers of the inverters, shown in Figure 7.3. Figure 7.3 shows the connection of the two controllers with the Typhoon 604 machine for the closed-loop control by SME-EDC. The frequency of the ADC clock of the microcontroller is 12.5 MHz. It has 16 analog input pins, which is desirable for the SME-EDC as it needs at least 9 analog input pins for the feedback signals.

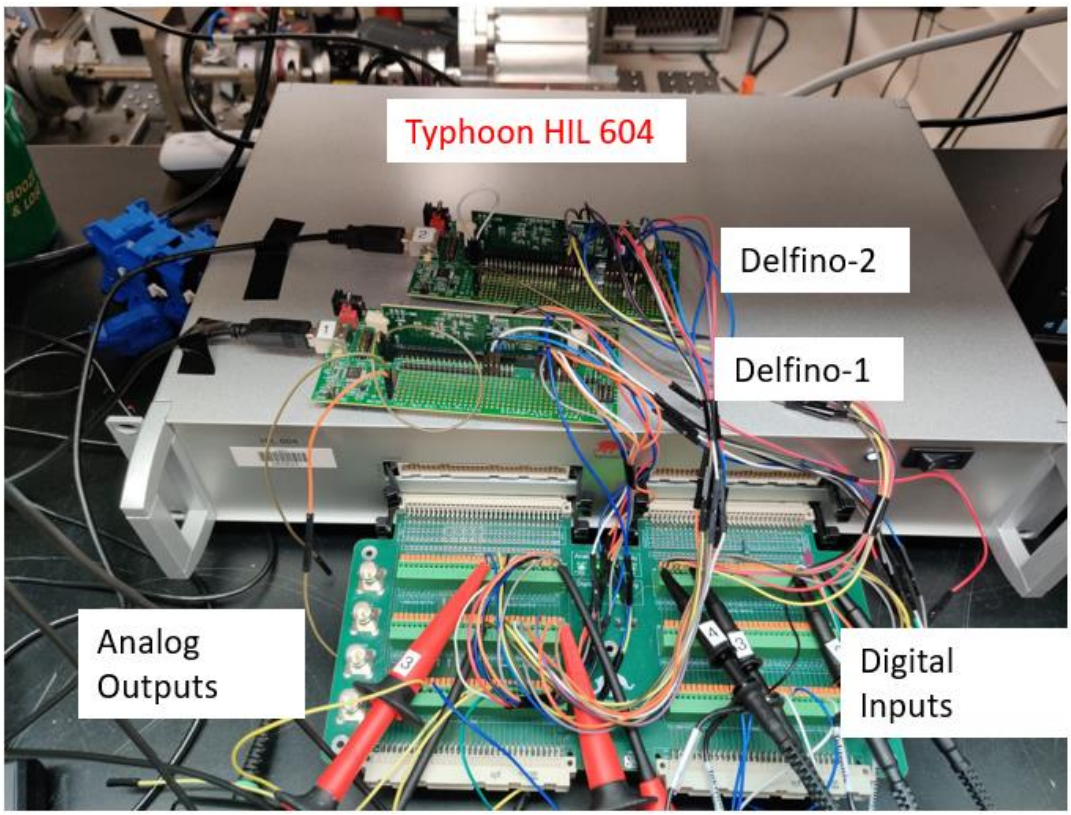


Figure 7.5. Two controllers controlling two parallel-connected inverters

7.1.4. PSIM Code Generation

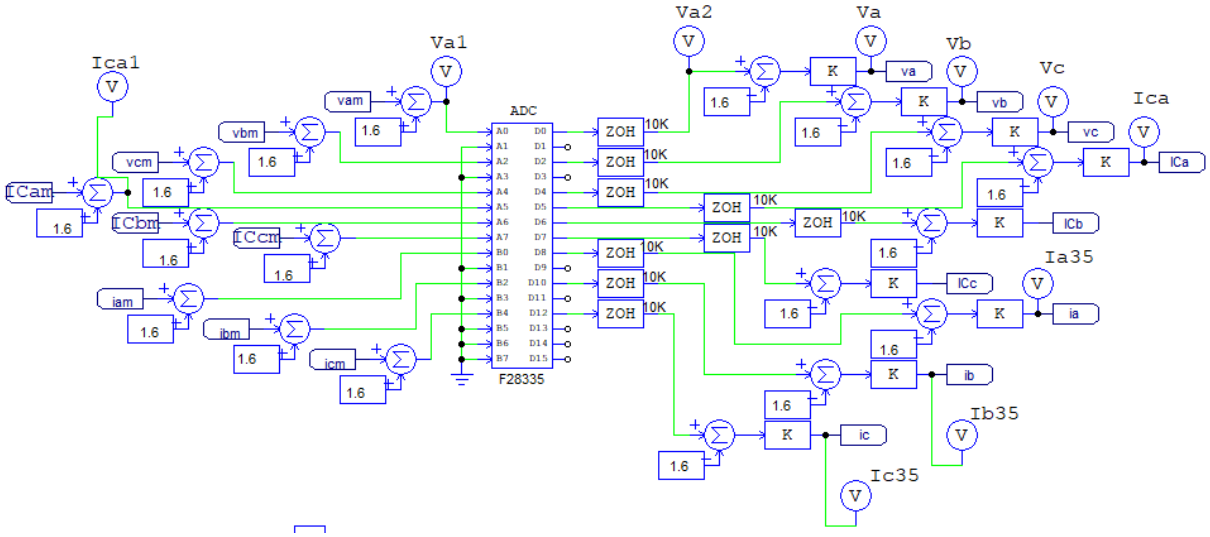


Figure 7.6. ADC and Scaling in PSIM for C code generation

The C code and firmware of the SME-EDC are generated using PSIM software. The firmware consists of Analog to Digital Conversion (ADC) and signal recovery as shown in Figure 7.6. The ADC process consists of sampling the analog signals every $1/f_{SW}$ = 1/10000 s. After this, the sampled signal is first added with 1.6 V and then multiplied with their corresponding scaling factors according to the signal conditioning applied in Typhoon HIL (Figure 7.4). Before generating the code, one 3-phase inverter and controller are again modeled in the PSIM software to validate the gains of the controller. Finally, the C Code can be generated using PSIM.

The analog and digital pins of the microcontroller are managed in Figure 7.5 according to the PIN configuration configured in code generation as shown in Figure 7.6.

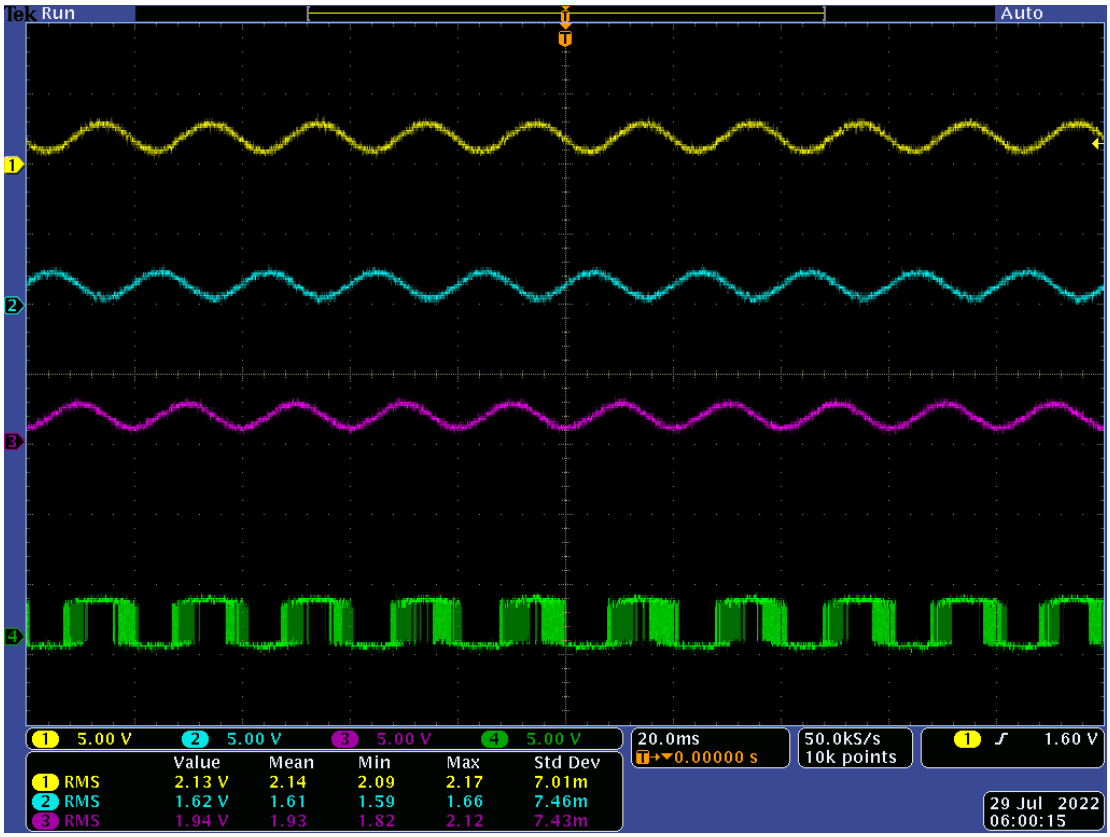


Figure 7.7. Profiles of phase A voltage of inverter-1 and inverter-2, current of inverter-1 and PWM signal for IGBT-1 of inverter-1 while controlled by SME-EDC before closing breaker-2 (before synchronism)

7.1.5. Programming by Code Composer Studio

The generated C code is programmed in the microcontroller using Code Composer Studio (CCS).

CCS needs to be properly configured to the microcontroller (F28335) during creating a project in CCS before programming the C code in the microcontroller. Additionally, the target of the code needs to be configured consistent with the microcontroller's model/series. The microcontroller holds the code as long as it is powered by the USB connector or external 3.3 V power supply.

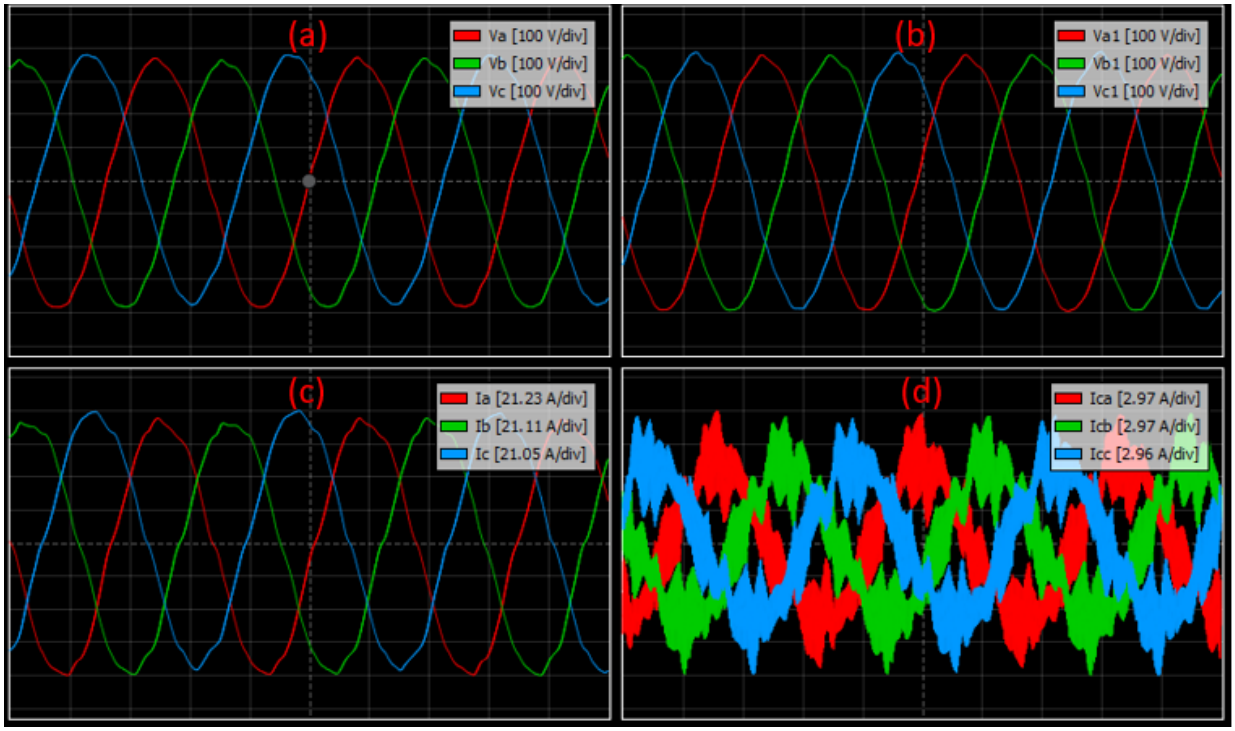


Figure 7.8. Profiles of (a) 1st inverter's voltage, (b) 2nd inverter's voltage, (c) 1st inverter's current and (d) 1st inverter's capacitor current at steady state in Typhoon SCADA panel while controlled by SME-EDC

7.1.6. CHIL Results and Discussions

In the CHIL experiment, two parallel-connected inverters are constructed in Typhoon HIL 604. Referring to Figure 2.1, Breaker-1 is 'closed' and Grid-Breaker is permanently 'Opened'. Only Breaker-2 is operated. Figure 7.7 shows the phase-A voltage of 1st inverter and 2nd inverter before closing Breaker-2 and after applying the signal conditioning. Also, Figure 7.7 shows the Delfino controller generated PWM signal (10 kHz) for IGBT-1 of inverter-1. The SME-EDC controller is programmed into the Delfino after connecting its corresponding digital and analog pins to the Typhoon HIL's breakout board (Figure 7.5) and applying the signal conditioning. Figure. 7.8. shows the phase synchronism of the voltage of 1st inverter and 2nd inverter in the scope in typhoon HIL after closing the Breaker-2 before the signal conditioning and Figure. 7.9 shows the voltage

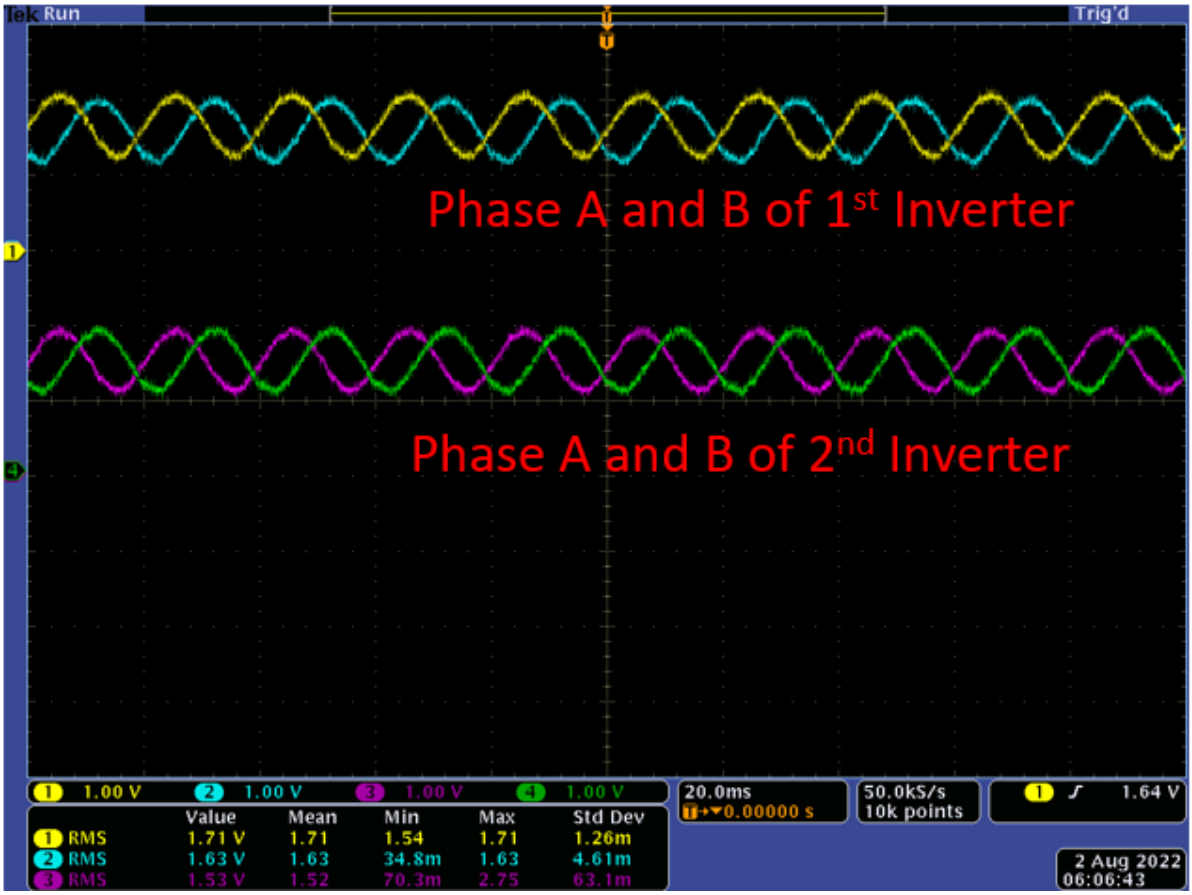


Figure 7.9. Profiles of phase A and phase B voltage of inverter-1 and inverter-2, by SME-EDC after closing breaker-2 (after synchronization)

profiles of the two inverters, measured by an oscilloscope after achieving phase synchronization (after signal conditioning).

7.2. Experimental Validation in Hardware

The hardware setup of the 3-kW inverter is shown in Figure 7.10. The inverter prototype consists of 400 V DC power supply, LC filter, gate driver circuit, signal conditioning circuit, microcontroller (f28335), and resistive load. L=0.25 mH and C=100 uF are chosen as the LC filter which makes the corner frequency= 10006 Hz

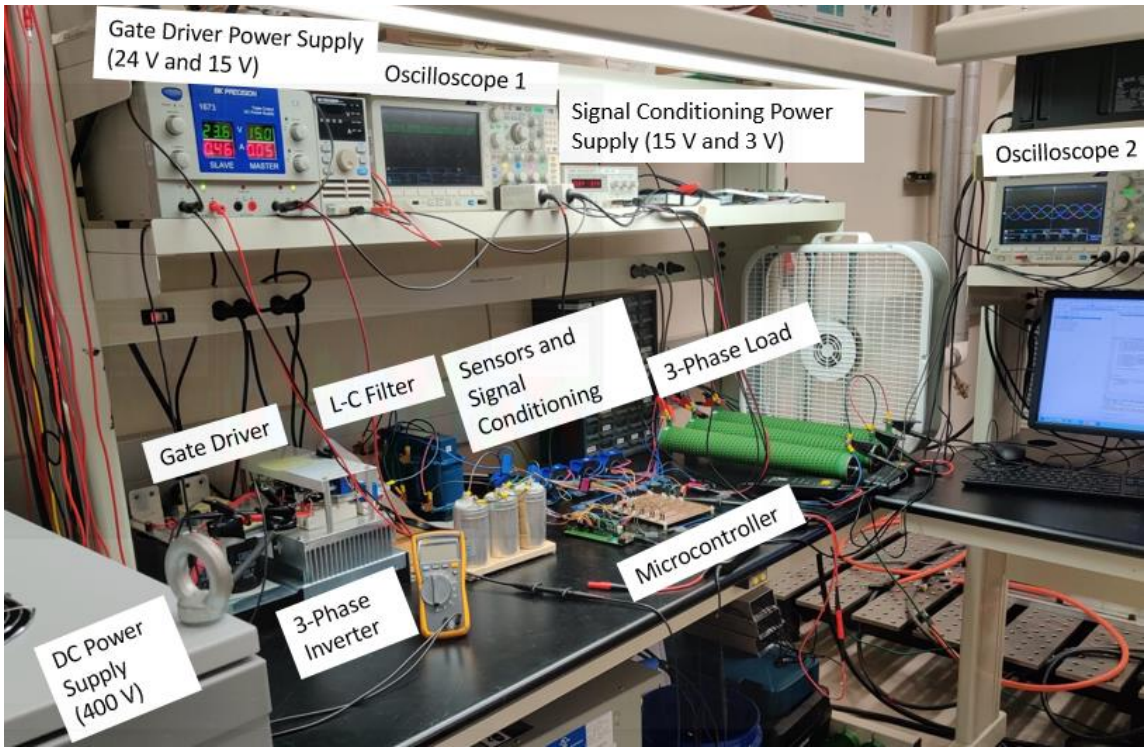


Figure. 7.10. Experimental setup with 3-phase inverter, LC filter, gate driver circuit, signal conditioning circuit, microcontroller, and resistive load

7.2.1. IGBT Modules

The IGBT module is rated for 1000 Vdc, 50 A. The maximum allowable switching frequency is 20 kHz. For the experiment, the prototype is designed for 10 kHz switching frequency and 3 kW resistive load. The turn-on voltage for the IGBTs is 15 V.

7.2.2. Gate Driver Design

The gate driver board consists of three TC1427 gate drivers for converting six 3.3 V modulating signals to 15 V modulating signals for the six IGBTs of the 3-phase inverter. The gate driver board interface and power supplies are shown in Figure 7.11. It requires 15 V DC voltage for powering the gate drivers. Additionally, it requires 24 V DC to activate the overcurrent protection. Figure 7.11 also shows the pin configuration of the inverter for interacting with the microcontroller for open-loop and closed-loop control applications.

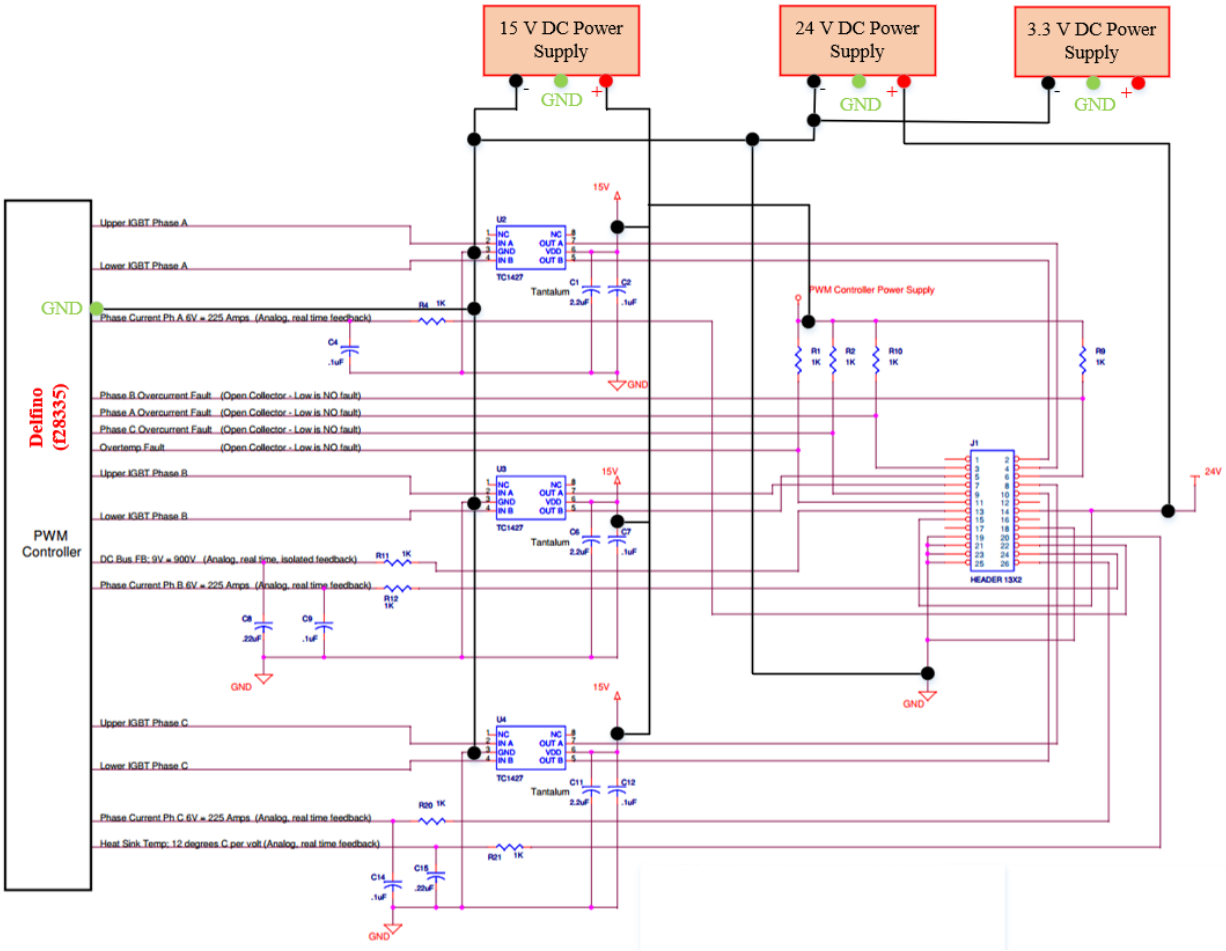


Figure. 7.11. Gate driver board, DC power supplies and pin configuration

7.2.3. Signal Conditioning Board Design

The same signal conditioning principle, that is discussed in section 7.1.2. in the CHIL experiment is utilized in the hardware experiment. The Signal conditioning board layout design is shown in Figure 7.12 and the final board is shown in Figure 7.13 containing the pin connections with the sensors and the inverter prototype. The voltage conditioning follows the design shown in Figure 7.14. By choosing R_2=R_3 =1.8 kΩ, the scaling ratio becomes 1/409 for the voltage sensing. For the current sensing circuit, shown in Figure 7.15, the scaling ratio for inverter output current (I) and capacitor current (iC) becomes 0.064 and 1/15 by following (7.2). For the I am sensing circuit R_4 is 240 Ω whereas for the iC sensing circuit, R4 is 100 Ω.

$$V_o = V_{in}.(R_2 + R_3)/1474k + 1.5 \quad (7.1)$$

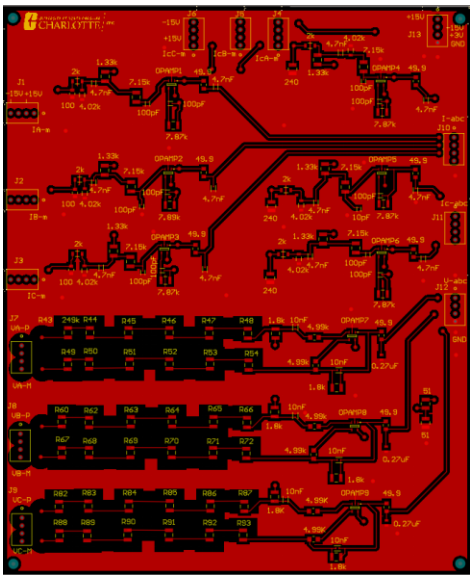


Figure. 7.12. Layout design of the 2-layer PCB design for the signal conditioning for the closed loop control in Altium

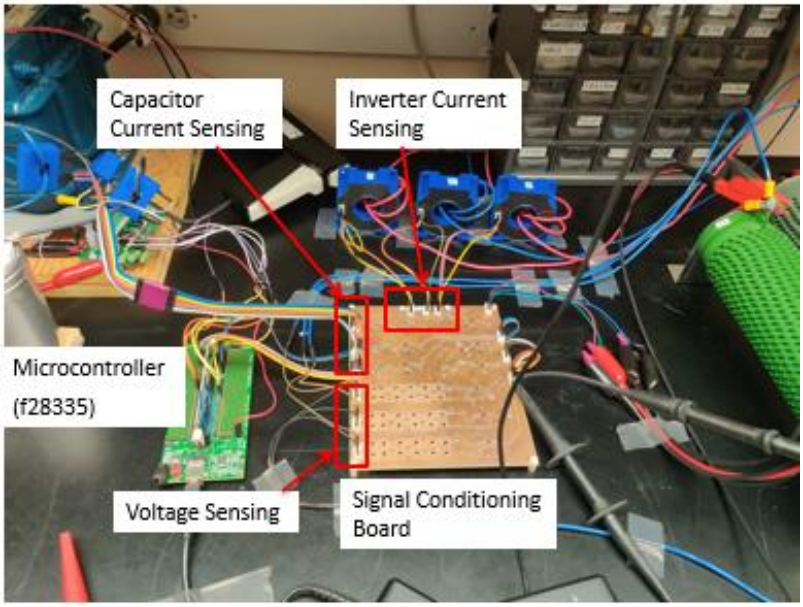


Figure. 7.13. Signal conditioning circuit for inverter output voltage, output current and capacitor current sensing in the closed-loop control

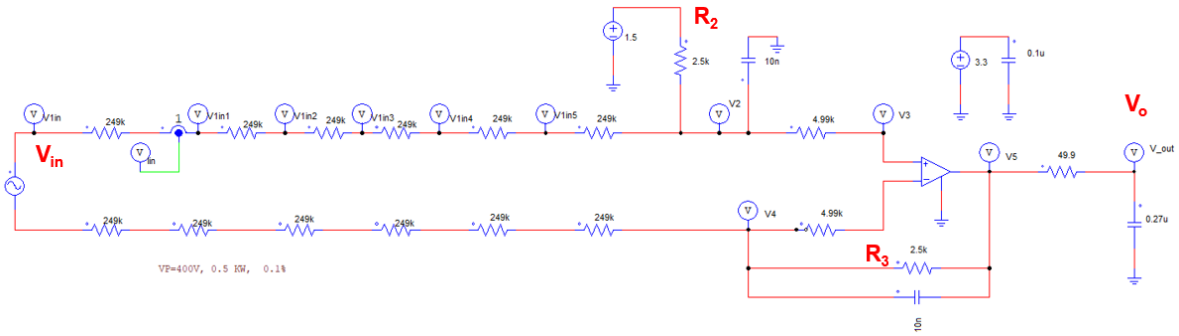


Figure. 7.14. Voltage sensing circuit for the closed loop control

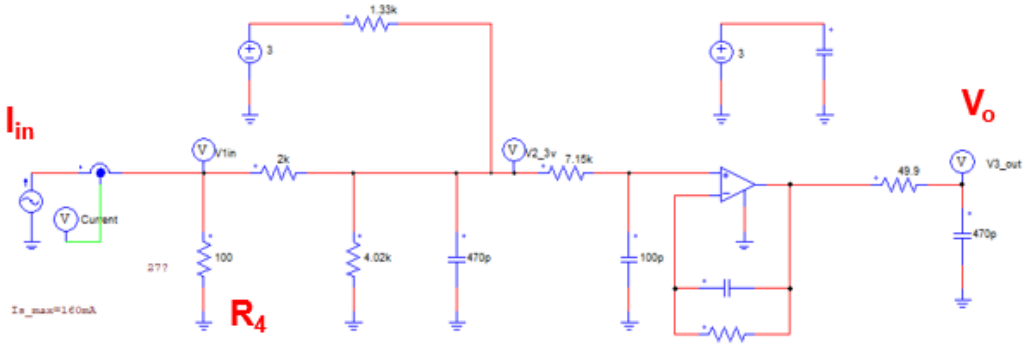


Figure. 7.15. Current sensing circuit for the closed loop control

$$V_o = (I_{in}.R_4)/3 + 1.503 \qquad (7.2)$$

(7.1) and (7.2) are determined by analyzing circuits in Figures 7.15 and 7.15 respectively.

7.2.4. LEM Sensors

LEM Sensors, HAS 100-S and HAS-200 series are used for iC and I sensing respectively which have 1:1000 and 1:2000 turns ratios respectively. These were considered while resigning the signal conditioning circuits for the current sensing.

7.2.5. Load Selection

The selected ceramic resistive loads are constructed by three Y-connected resistive loads each having 10 Ω resistance and 2 kW rating. In the islanded system, the inverter is connected to the load, and the inverter output current is determined by the load resistance and inverter output voltage. For the 3-phase RMS voltage= 173 V, the single-phase RMS voltage is 100 V, single-phase RMS current=10 A, and 3-phase active power becomes 3*100*10= 3kW.

7.2.6. Validation of Closed Loop Control of SME-EDC in Hardware

Figure 7.16(a) shows the feedback voltage (phase C) profiles of the inverter which is input for the microcontroller. Figure 7.16(b) is the 3-phase inverter output voltage, controlled at 173 V_{ll_rms} and 60 Hz by the closed-loop control (SME-EDC). It shows the voltage scaling ratio of 9/3686 which verifies the voltage sensing design in Figure 7.14.

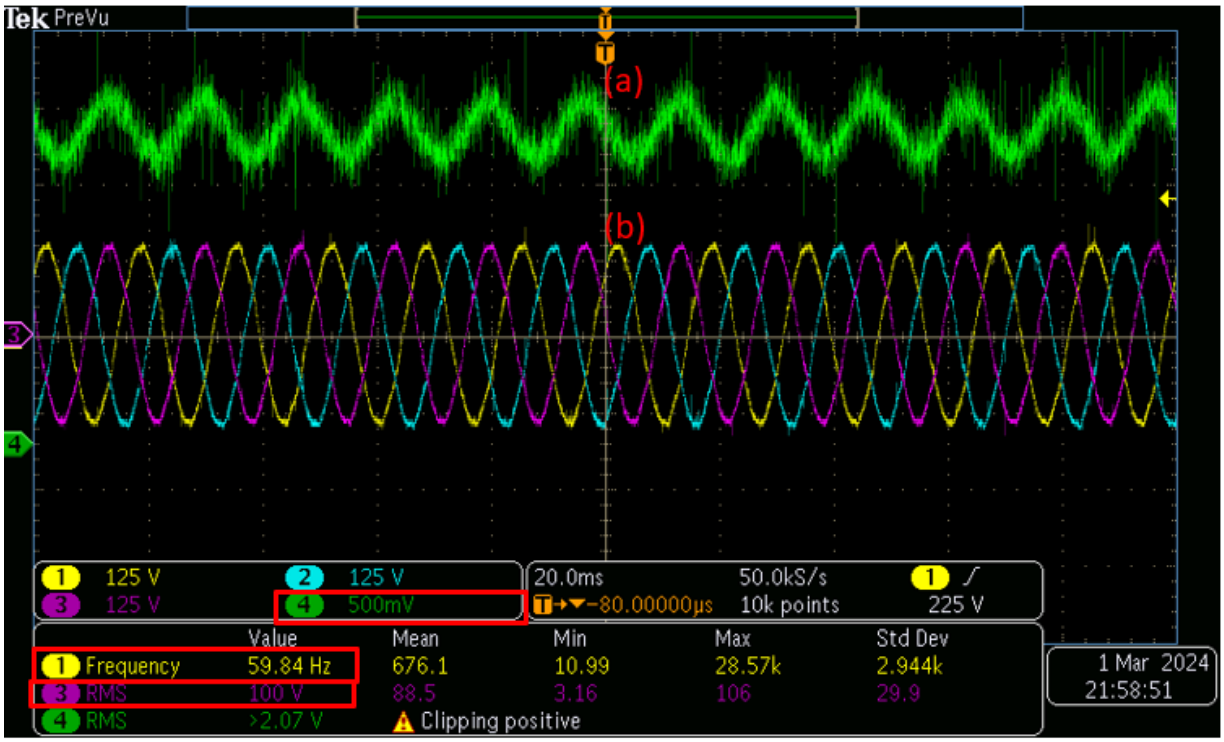


Figure. 7.16. Profiles of (a) inverter's scaled and shifted voltage (V_{mC}) and (b) inverter's filtered output voltage (V_{PCC}) while controlled by SME-EDC in closed loop control

Figure 7.17(a) shows the current (phase C) profiles of the inverter which is input for the microcontroller. Figure 7.17(b) is the phase C inverter output current. From the observation, the scaling is 0.064 which verifies the current sensing circuit design in Figure 7.15.

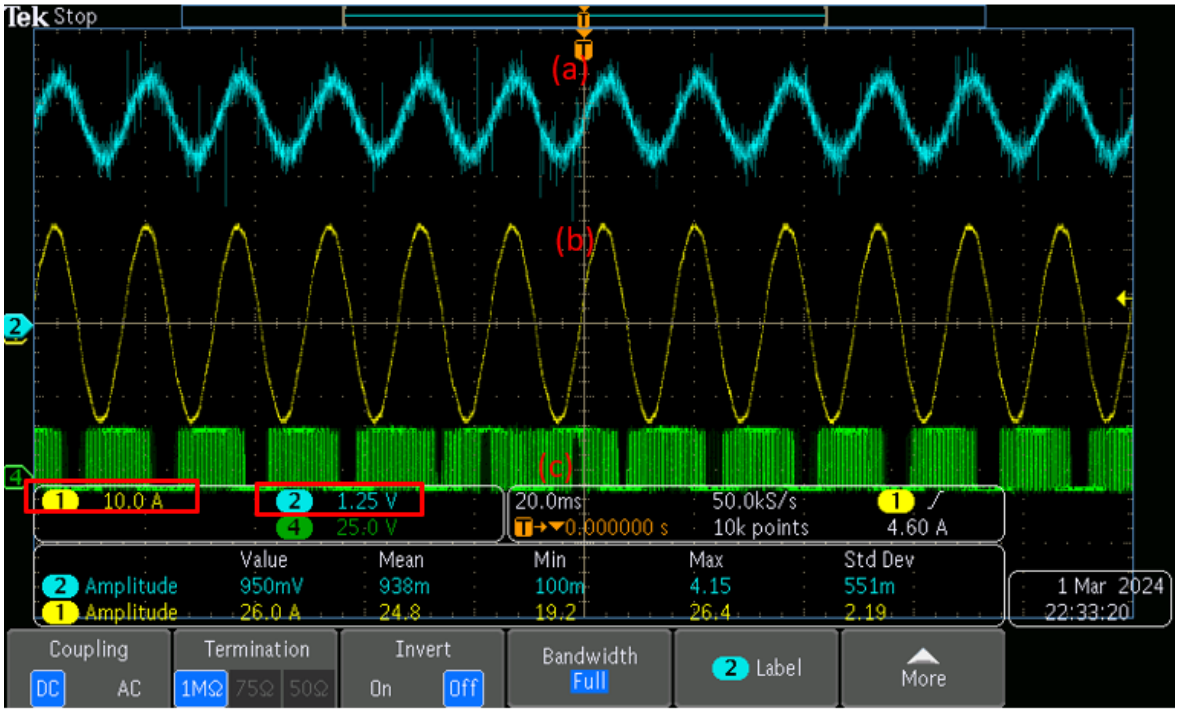


Figure. 7.17. Profiles of (a) inverter's scaled and shifted voltage (V_{mC}) and (b) inverter's filtered output voltage (V_{PCC}) while controlled by SME-EDC in closed loop control

Figure 7.17(c) shows the PWM signal for phase C-, generated by the controller in the closed-loop control. Next, the feedback signals to the microcontroller are turned off and then turned on.

From Fig. 7.18(b), after 7/60 s of applying the feedback signals to the digital controller, the voltage and frequency were controlled to 173 V_{ll_rms} and 60 Hz respectively. It validates the closed-loop control and grid-forming capability of the controller.

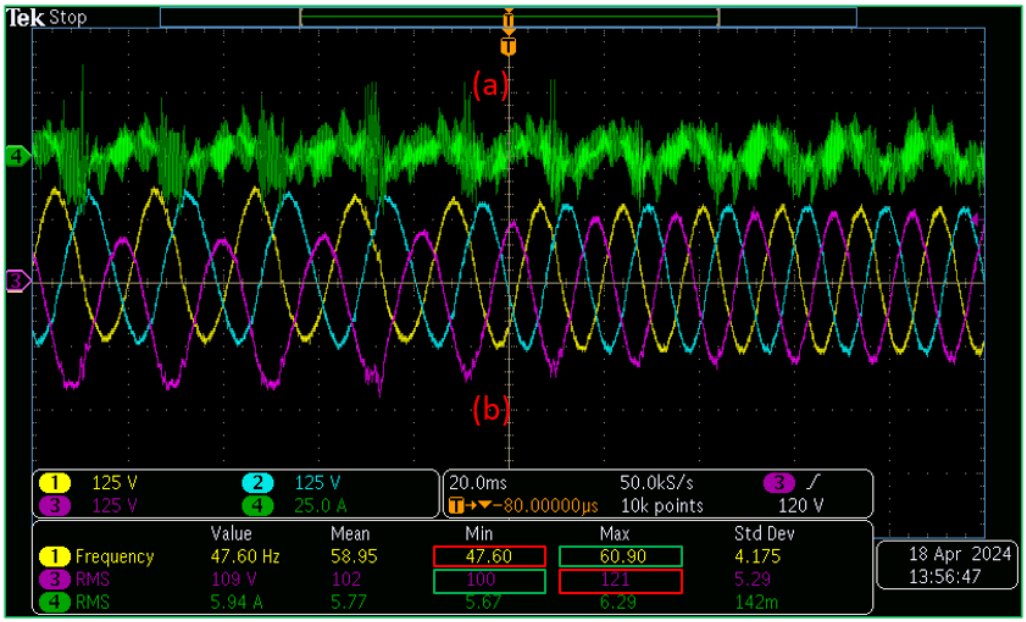


Figure. 7.18. Profiles of (a) capacitor current (phase C), and (b) inverter output voltage

After applying the feedback signal to the controller

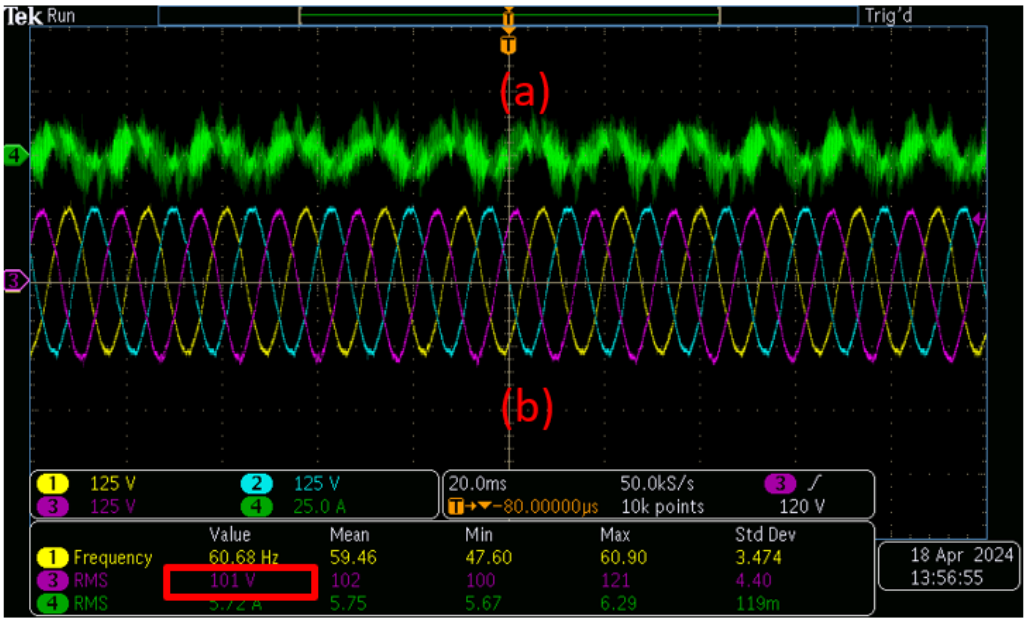


Figure. 7.19. Profiles of (a) capacitor current and (b) Inverter output voltage at steady state

At the start when the feedback voltage and signals were not provided to the digital controller,

the frequency was 47.48 Hz and the voltage was 207 V_{ll_rms} because the digital voltage and current signals after the signal conditioning are greater than rated (V_m=-1.5*409 V, I_m=-1.5*15.52 A, P_m= 42.8 kW). Hence $\omega *$ became 299 rad/s; i.e. f^* = 47.58 Hz by following (3.8) before applying the feedback signals to the digital controller. Fig. 18(a) shows the capacitor current of phase C which is also controlled after 7/60 s to control the voltage 173 V_{ll_rms}.

After applying the control, capacitor current, voltage and frequency are controlled. Before applying the feedback signal to the digital controller, as the internal V_{PCC}* is negative, iC^* and E^* are greater (120 V) than the rated values as shown in Figure 7.18(a) and 7.18(b). It validates the frequency and voltage control relation of the controller.

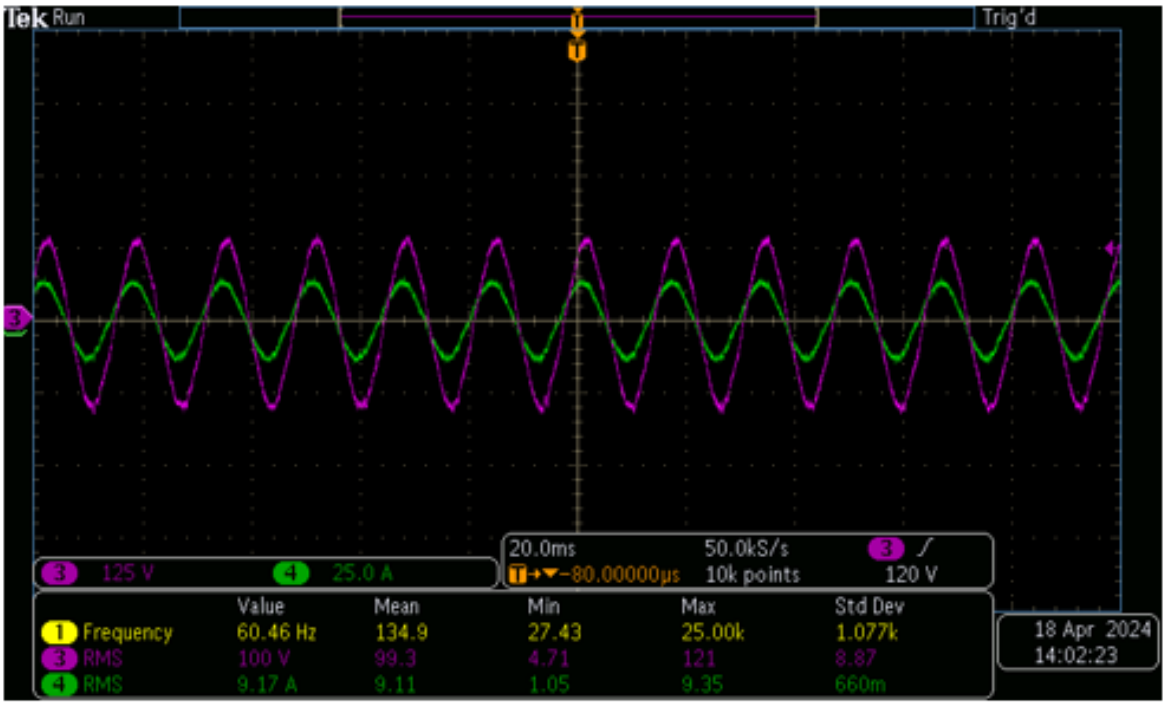


Figure. 7.20. Profiles of (a) capacitor current (phase C), and (b) inverter output voltage

After applying the feedback signal to the controller

$$(\omega * = \omega_{nominal} + (P_{nominal} - P).\ D_p) \quad (3.8)$$

$$K_C\ (V_{PCC}* - V_{PCC}) = iC* \quad (3.1)$$

$$E*= (iC* - iC)(K_P + K_I/s) \quad (3.3)$$

Figure 19 shows the profiles of steady-state capacitor current and inverter output voltage. At steady state, the voltage is 173 V_{LL_rms} and frequency is controlled at 60 Hz. Figure 20 shows the inverter output voltage and current of phase C at steady state.

CHAPTER 8: CONCLUSIONS AND FUTURE WORK

8.1. Special Cases

8.1.1. Case I: Black-Start without any Local Load, and then Phase-Synchronization (10 kW)

The inverter starts without any load at the start as shown in Figure 8.1. Figure 8.1(a) displays the profile of the P_{PCC} of the 1st inverter which is 0 at the beginning and stabilizes to 10 kW after connecting it to the grid. The initial phase difference between the inverter and the grid was 60^0. Because of its droop characteristics, the initial frequency is higher than the rated 377 rad/s. At .01 s, the inverter is connected to the grid and $P_{nominal}$=P= 10 kW is supplied to the grid. The phase of

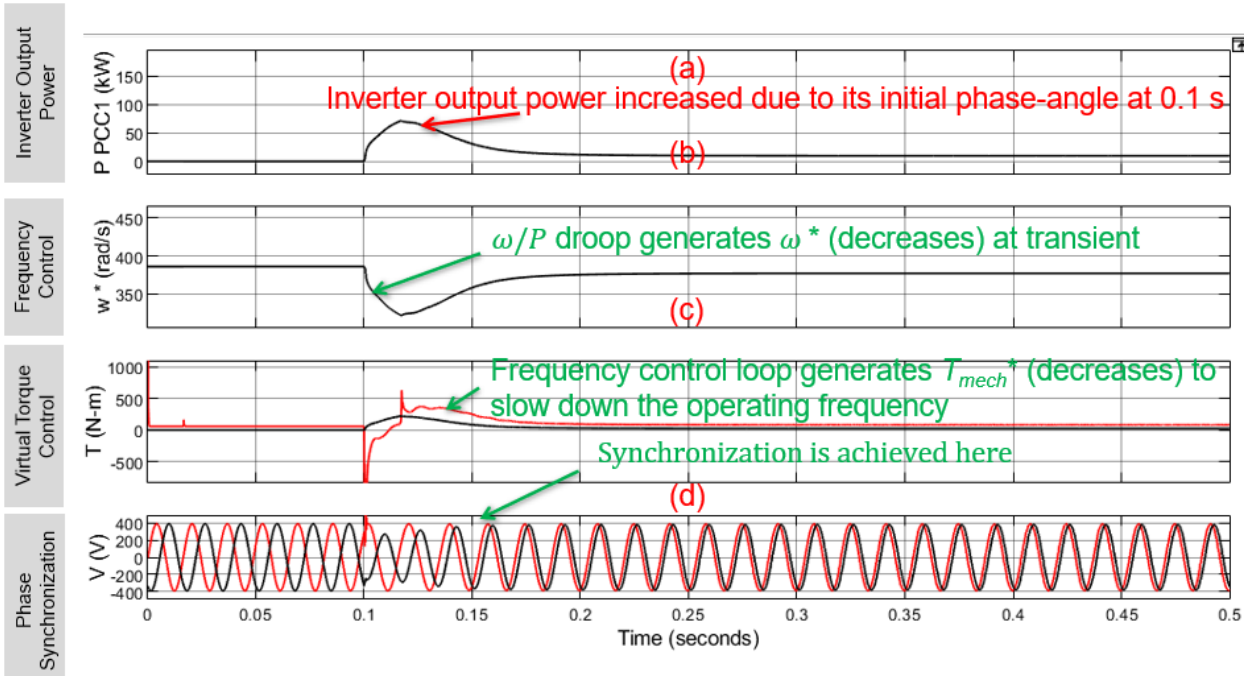


Figure. 8.1. Profiles of P_{PCC1}, ω *, T_{mech}*, T_{elect}, V_{PCCa} and V_{ga} of the 1st inverter showing the Black-start and phase-synchronization mechanism in Case I

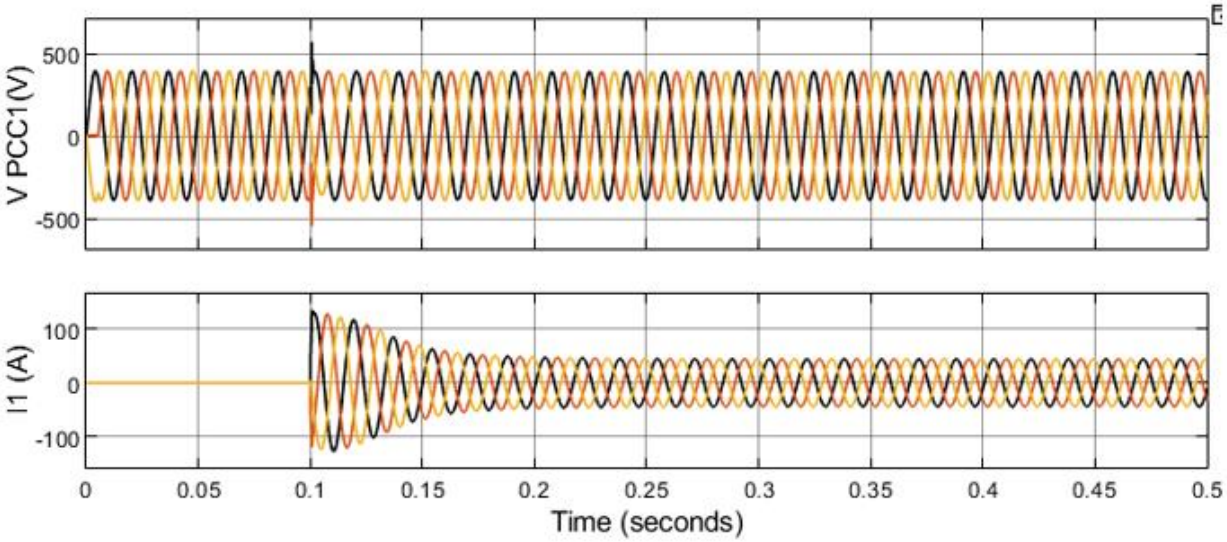


Figure. 8.2. Profiles of voltage and current at PCC 1 before and after connecting the inverter to the grid

the voltage of the inverter is synchronized to that of the grid at 0.2 s. Figure 8.2 shows the profiles of inverter voltage and current. The transient voltage is controlled very fast by the voltage control loop of SME-EDC (0.0062 s) after connecting the inverter to the grid. But it took 0.05 s to control the current and active power in this condition.

8.1.2. Case II: Black-Start without any Local Load, and then Phase-Synchronization (50 kW)

In this condition, $P_{nominal}$ is changed to 50 kW and the inverter is connected to the grid at 0.1 s as shown in Figure 8.3. The initial phase difference between the inverter and the grid was 30^0 and there was no local load.

As the final phase of the inverter voltage is closer to the initial condition (60^0) in comparison with the same in Case I, the phase synchronization action took less time than in Case I. It is synchronized at 0.15 s (After 0.05 s). Figure 8.4 shows the voltage and current profiles of the

inverter in this case. Transient peaks in voltage and current are lesser than that in Case I. Also, the time to control both voltage and current is approximately 0.05 s in this case.

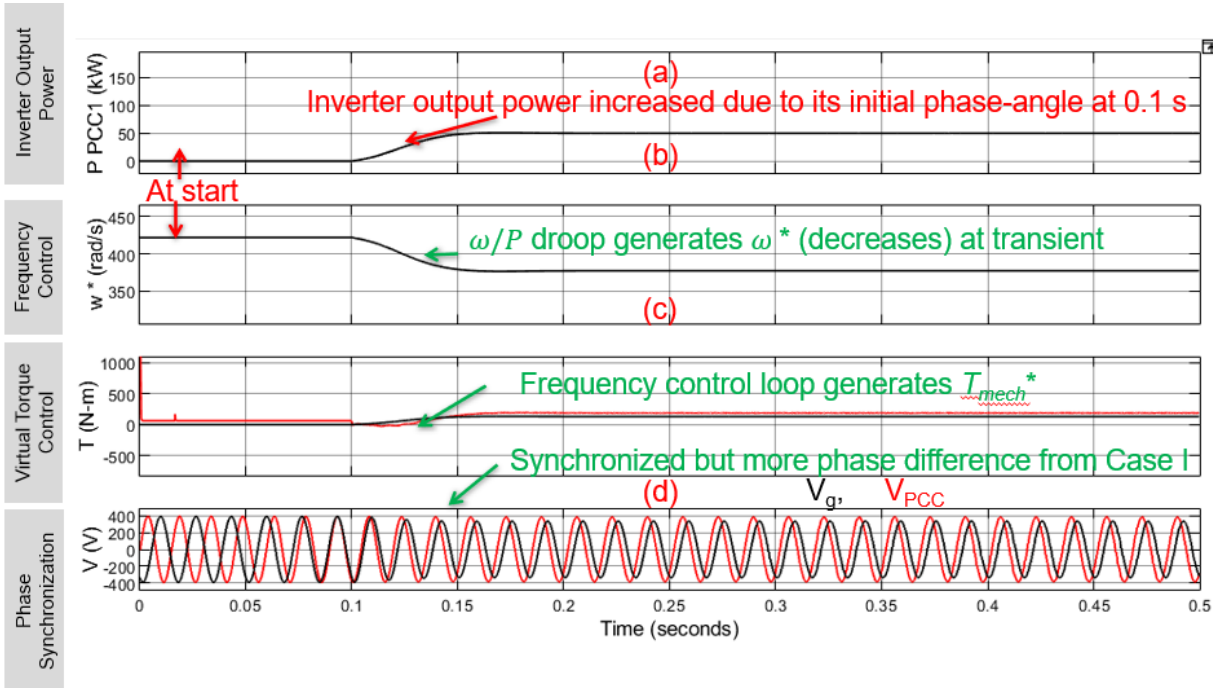


Figure. 8.3. Profiles of P_{PCC1}, ω *, T_{mech}*, T_{elect}, V_{PCCa} and V_{ga} of the 1st inverter showing the Black-start and phase-synchronization mechanism in Case II

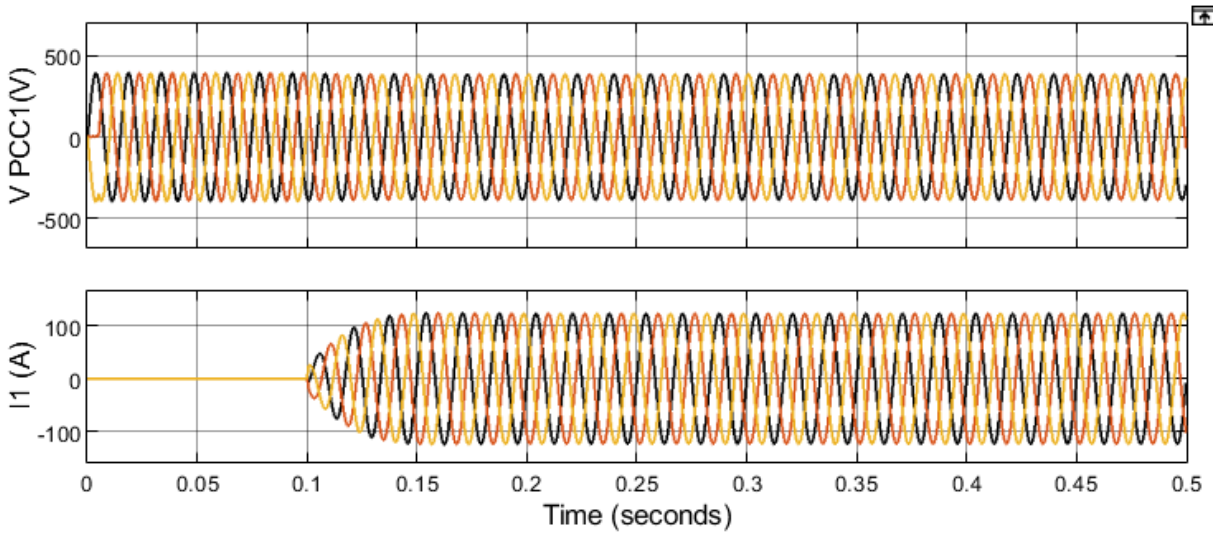


Figure. 8.4. Profiles of voltage and current at PCC 1 in Case II

8.1.3. Case III: Phase-Synchronization with Under Voltage at Grid (V_g = 326 V)

In this test case, the grid voltage is 326 Vpeak whereas the inverter output voltage at PCC is 391.92 Vpeak. Figure 8.5 shows that the inverter was able to control the output power = 10 kW and synchronize to the grid 0.065 s after connecting to the grid.

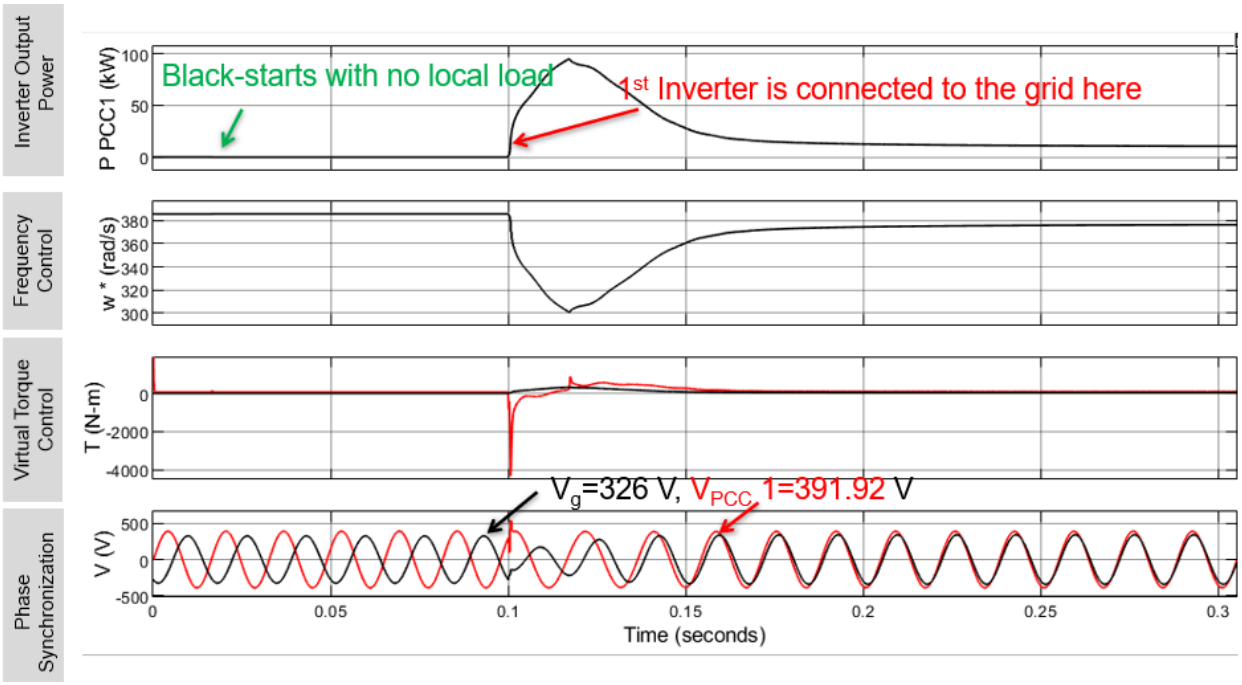


Figure. 8.5. Profiles of P_{PCC1}, ω *, T_{mech}*, T_{elect}, V_{PCCa} and V_{ga} of the 1st inverter showing phase-synchronization with grid, having under voltage in Case III

8.1.4. Case IV: Impact of D_P in Phase-Synchronization (D_P= 1/5000)

In the previous test cases, the value of the droop constant D_P was 1/1111.1. It is changed to 1/5000 in Case IV (Figure. 8.6). It is observed that the controller is able to synchronize the inverter with the grid, but it took approximately 0.3 s to reach the steady state.

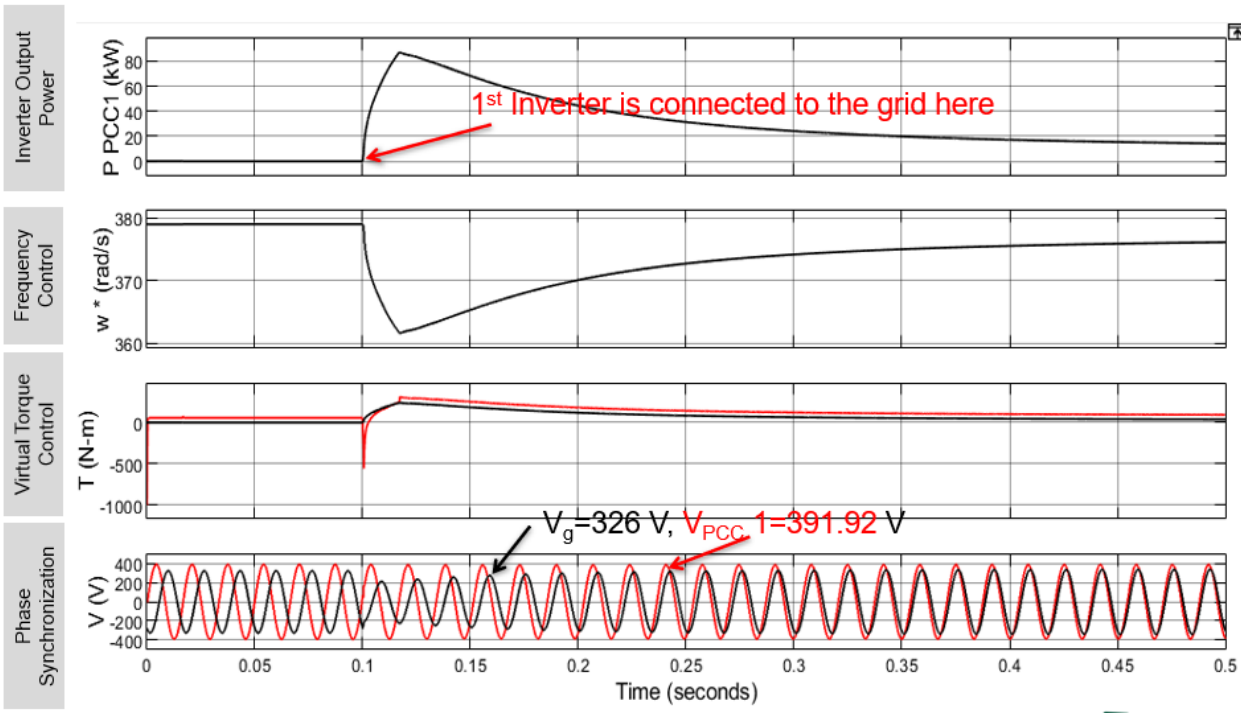


Figure. 8.6. Profiles of P_{PCC1}, ω *, T_{mech}*, T_{elect}, V_{PCCa} and V_{ga} of the 1st inverter showing the Black-start and phase-synchronization mechanism in Case IV

8.2. Conclusions

The objective of the dissertation work is to architect a smart and complete inverter-control system to control the GFM inverters irrespective of the system changes between modes and without any communication signal in the islanded system. This research presents a novel control scheme, namely Synchronous Machine Emulator with Embedded Droop Control is proposed to control the PCC voltage, frequency, and power of one or multiple inverters without any communication among the controllers and without PLL in the grid-connected as well as grid-forming mode. Existing virtual inertia-based controllers do not have all the required capabilities of a complete GFM inverter controller for the future power grid. To overcome the limitations, a new and improved control architecture, SME-EDC has been proposed for the modern power grid in the future where all the inverters will have identical control architecture allowing them to seamlessly operate in islanded mode, parallel-connected mode with other inverters and grid-connected mode. By conducting various experiments, the grid forming capability from black-start, auto-synchronization capability and droop control capability of this controller are validated in the presence of other inverters or the grid. PCC voltage and frequency of multiple inverters were cooperatively controlled by this controller within constraints under various grid and load conditions. However, three extra current sensors are needed for implementing the capacitor current control for accurately controlling the PCC voltage even under sudden load changes. Additionally, this controller showed flexibility to control the load sharing in the multiple inverters system by its droop control. As this controller does not need PLL, the grid synchronization has become independent of the fixed reference-based control in the DERs-dominated modern Power Grid. Instead, phase-synchronization is achieved on the principle of power control by the internal virtual torque control of the controller. Furthermore, it is expected to be more secure and reliable than

conventional communication-based controllers. Based on the simulation and experimental results, the proposed controller has fulfilled all the criteria to become a complete and flexible controller for grid-forming and grid-interacting inverters and appears to be a promising alternative for the modern power grid.

In SME-EDC, P will be $P_{nominal}$ at the steady state, and ω^* will be $\omega_{nominal}$ at that condition. Hence, there will not be any stability problems with phase-synchronization. With a high value of D_P, the response time decreases. Furthermore, it is also observed that even with a slight deviation of $|V_{PCC}^*|$ at any bus, the inverter, controlled by SME-EDC, can synchronize seamlessly.

8.3. Future Works

1. Dynamic Stiffness: Dynamic stiffness is the resiliency of a system under disturbance. In the context of voltage control, it means the strength of the voltage control under load changes during transients. As the proposed controller uses capacitor current control to control inverter output voltage, it has potential to increase the dynamic stiffness of the system.

2. Virtual Impedance, and Virtual Resonator: The objective of the virtual impedance in the inverter control loop is to simulate the current or voltage at the PCC and then apply it in the control loop. By mimicking the behavior of a physical impedance, virtual impedance may allow for better integration of renewable energy sources into the grid. It can help increase the effective output impedance during voltage control and synchronization.

The virtual resonator control loop can dampen harmonics content, improve stability, and filter out undesired harmonics contents from the output.

3. Duality Between DPC, and SME-EDC: In terms of controlling active power and phase-synchronization without PLL, these DPC and SME-EDC have objective similarities. A comparative analysis of these two controllers can help improve the response time, stability, and steady-state error.

4. Bidirectional Power Flow Condition: SME-EDC is designed for emulating an inverter as a synchronous machine for supporting power from the inverter in islanded, grid-connected, and grid-forming conditions. The analysis of bidirectional power flow is another potential research continuation.

8.4. Publications Related to the Thesis

1. P. R. Chowdhury, E. Shoubaki and M. Manjrekar, "Comparison of Power Control Methods for Renewable Energy Resources Operating in a Weak Grid," *2020 52nd North American Power Symposium (NAPS)*, 2021, pp. 1-6, doi: 10.1109/NAPS50074.2021.9449827.
2. P. R. Chowdhury, E. Shoubaki and M. Manjrekar, "Modified Voltage and Frequency Control of Parallel-Connected Grid-Forming Inverters by Virtual Synchronous Machine Controller," *2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2020, pp. 1-5, doi: 10.1109/PEDES49360.2020.9379725.
3. P. R. Chowdhury, E. Shoubaki and M. Manjrekar, "Modified Voltage Controlled-Virtual Synchronous Machine Controller in the application of Parallel Connected Grid-Forming Inverters," *2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2021, pp. 1-5, doi: 10.1109/PEDG51384.2021.9494260.
4. P. R. Chowdhury, and M. Manjrekar, " Capacitor Current Control for the Parallel-Connected Grid-Forming Inverters," *2022 IEEE Energy Conversion Congress & Exposition (ECCE)*, 2022.
5. P. R. Chowdhury, and M. Manjrekar, “Phase-Locked Loop vs Synchronous Machine Emulation: A Comparative Study of Phase-Angle Determination Dynamics”, *2024 IEEE Energy Conversion Congress & Exposition (ECCE)*, 2024. [ACCEPTED]
6. P. R. Chowdhury, and M. Manjrekar, " Synchronous Machine Emulator: A Novel Controller for Grid-Forming and Grid-Supporting Inverters in the Distributed Energy Resources Dominated Future Grid," *IEEE Transactions on Smart grid (TSG)*, 2024. [UNDER REVIEW]

7. P. R. Chowdhury, E. Shoubaki, S. Essakiappan and M. Manjrekar, " A Survay of Control Schemes for Grid-Connected and Islanded Inverters," *2024 IEEE Access*. [UNDER REVIEW]

8.5. Publications Related to the Sponsored Projects

8. A. S. Siddiqui, P. R. Chowdhury, Y. Gui, M. Manjrekar, S. Essakiappan and F. Saqib, "Design of Secure Reconfigurable Power Converters," *2019 IEEE CyberPELS (CyberPELS)*, 2019, pp. 1-6, doi: 10.1109/CyberPELS.2019.8925057.
9. A. S. Siddiqui, P R. Chowdhury, P. Sawant; S. M. Shinde, Y. Gui, M. Manjrekar, S. Essakiappan and F. Saqib, "Implementation of a Grid-Tied Secure Reconfigurable Power Converter," *2020 IEEE CyberPELS (CyberPELS)*, 2020, pp. 1-7, doi: 10.1109/CyberPELS49534.2020.9311537.
10. P. Roy Chowdhury, P. K. Sahu, S. Essakiappan, M. Manjrekar, K. Schneider and S. Laval, "Power Quality and Stability in a Cluster of Microgrids with Coordinated Power and Energy Management," *2020 IEEE Industry Applications Society Annual Meeting*, 2020, pp. 1-7, doi: 10.1109/IAS44978.2020.9334828.
11. P. R. Chowdhury, S. Essakiappan, M. Manjrekar, K. Schneider and S. Laval, "Optimized Dispatch of Distributed Energy Resources for Resiliency and Power Quality Improvements at the Grid-Edge," *2021 IEEE Kansas Power and Energy Conference (KPEC)*, 2021, pp. 1-6, doi: 10.1109/KPEC51835.2021.9446241.
12. S. Essakiappan, P. R. Chowdhury, K. Schneider, S. Laval, K. Prabakar, M. Manjrekar, Y. N. Velaga, N. Shepard, J. Hambrick and B. Ollis, "A Multi-Site Networked Hardware-in-the-Loop Platform for Evaluation of Interoperability and Distributed Intelligence at Grid-Edge,"

in IEEE Open Access Journal of Power and Energy, vol. 8, pp. 460-471, 2021, doi: 10.1109/OAJPE.2021.3103496.

13. R. Itiki, P. R. Chowdhury, F. Kamal, M. Manjrekar, B. Chowdhury and G. G. Bonner, "Method for Estimation of Marine Hydro-Kinetic Power based on High-frequency Radar Data," *OCEANS 2021*: San Diego – Porto, 2021, pp. 1-7, doi: 10.23919/OCEANS44145.2021.9705675.
14. F. Kamal, P. R. Chowdhury, B. H. Chowdhury and M. Manjrekar, "Power Sharing and Stability Assurance using Grid Forming Inverter Control in HVDC Connected Offshore Microgrid Cluster," *2021 North American Power Symposium (NAPS)*, 2021, pp. 1-6, doi: 10.1109/NAPS52732.2021.9654748.
15. P. R. Chowdhury, Y. N. Velaga, S. Essakiappan, M. Manjrekar, K. Prabakar, K. Schneider and S. Laval, "Demonstrating Distribution System Resiliency through Grid-Edge Microgrids, on a Multi-Site Networked Hardware-in-Loop Platform," *2022 IEEE Power Electronics for Distributed Generation Systems (PEDG)*.

8.6. Intellectual Property:

1. M. Manjrekar, P. R. Chowdhury, “Apparatus and Method for Controlling One or More Inverters”, non-provisional US patent application, US Patent App. 18/171,999, February 2023. [SUBMITTED]

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APPENDIX

APPENDIX A: Reactive Power Control: Automatic Voltage Regulator (AVR) Control

An AVR control is used to control the DC excitation (E_f) of SG for holding the voltage within specified limits and consequently controlling the generator's terminal voltage (V_{PCC}) [48].

By increasing the E_f, the rotor of an SG is overexcited. This process is capable to supply the needed reactive power (Q) to the grid. Similarly, by decreasing the DC excitation, the rotor can be made under-excited. And now it absorbs the needed reactive power from the grid. So, E_f is the controlling element to control Q and V_{PCC}. $\Delta V = E_f - V$. The AVR control is operated by the following equations,

$$\Delta Q = -1/R_a . \Delta V \quad (8.1)$$

$$R_a = \Delta V / \Delta Q \quad (8.2)$$

APPENDIX B: Active Power Control: Governor Control

By the governor control, grid frequency (f) is maintained within the specified limit by monitoring the P drops and applying controls.

Output power, P can be controlled by controlling the rotor speed (N_r) by applying mechanical torque T_m. Here, f is dependent on the rotor speed, as

$$f = N_r * \text{poles}/120 \tag{8.3}$$

When power demand increases, f decreases in the grid, making the N_r of SG slow. To make the system stabilized, T_m is applied in the SG to make $N_r=N_s$. by governor control in the frequency-drop method. So, T_m controls the governor (G), G controls N_r, N_r controls f which controls P in steady-state. (ref-droop speed control [48]). So, in this way, T_m controls output P and f. The following equations decide the governor control.

$$\Delta T_m = -1/R_g . \Delta f \tag{8.4}$$

$$R_g = \Delta f / \Delta T_m \tag{8.5}$$