DESIGN OF A TIME-INTERLEVED SAR ANALOG TO DIGITAL CONVERTER IN 45NM CMOS

by

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ABSTRACT

JED SANDER. Design of a time-interleved SAR analog to digital converter in 45nm CMOS. (Under the direction of DR. JEREMY HOLLEMAN)

As wireless communication standards evolve to utilize wider bandwidths and higher order modulation schemes, such as 1024-QAM, careful attention must be placed on the embedded Analog to Digital Converter (ADC). For a modern receiver to meet current IEEE 802.11ax (Wi-Fi 6e) standards, it must be able to transmit a 1024-QAM signal with a bandwidth of 160 MHz. Historically, pipelined architectures have performed well with wide bandwidths and high resolution; however, these pipelined ADC's have poor power to bandwidth tradeoffs. For mobile devices, power consumption is very limited, and the chosen ADC design has a significant impact on overall battery life. Successive Approximation Register (SAR) ADCs have exceptionally low power consumption, but arent able to perform at the desired speeds. Recent works have shown that "Time-Interleaving" several SAR ADCs results in the ability to achieve the desired speeds, while consuming much less power than a traditional pipelined ADC. This method utilizes several SAR ADCs in parallel, with each starting its acquisition at a different time. The resulting outputs from each ADC are then "Interleaved" to produce a collective output at a much faster sampling rate. For example, a 10 bit, 500 Msps ADC can be made from 5 "Interleaved" 10 bit SAR ADCs, each having a sample rate of just 100 Msps.

DEDICATION

To the Father whose design still leaves much to discover. And to the Son whose sacrifice set us free to explore it.

To my parents, who have motivated and supported my academic journey.

TABLE OF CONTENTS

LIST OF TABLES vii

LIST OF FIGURES viii

LIST OF ABBREVIATIONS x

PREFACE xii

CHAPTER 1: INTRODUCTION 1

1.1. Problem Statement 1

1.2. Overview 1

1.2.1. Theory of Operation 1

1.2.2. Binary Search Algorithm 2

1.2.3. Time Interleaving 3

1.3. Scope of Work 4

CHAPTER 2: COMPARATOR DESIGN 5

2.1. Considerations 5

2.1.1. General 5

2.1.2. Input Offset 7

2.1.3. Metastability 8

2.1.4. Input Referred Noise 10

2.1.5. Kickback Noise 10

2.2. Design 11

2.3. Simulation Analysis 11

2.3.1. Input Referred Noise 12

2.3.2. Input Offset 13

CHAPTER 3: CAPACITIVE DAC DESIGN 16

3.1. Considerations 17

3.1.1. General 17

3.1.2. Non Linearity 17

3.1.3. Capacitor Mismatch 18

3.2. Design 19

3.3. Simulation Analysis 21

CHAPTER 4: SAR LOGIC DESIGN 24

CHAPTER 5: COMPLETE ADC DESIGN AND SIMULATION 26

CHAPTER 6: TIME INTERLEAVED DESIGN 30

CHAPTER 7: CONCLUSIONS 34

CHAPTER 8: FUTURE WORK 36

8.1. DAC Design Revisions 36

8.2. Calibration Techniques 36

8.3. Interleaving Error Mitigation 36

REFERENCES 37

LIST OF TABLES

TABLE 7.1: ADC Performance Summary 35

TABLE 7.2: Relevant Works 35

LIST OF FIGURES

FIGURE 1: Modern Receiver Front End xii

FIGURE 1.1: SAR ADC Block Diagram 2

FIGURE 1.2: Binary search based conversion cycle 3

FIGURE 1.3: Time Interleaved Converter Timing Diagram 4

FIGURE 2.1: Comparator input-output relationship 6

FIGURE 2.2: Strong Arm Latch Comparator 7

FIGURE 2.3: Schematic for evaluating Input Referred Noise 12

FIGURE 2.4: Output Noise Spectrum 13

FIGURE 2.5: Schematic for evaluating Input Offset 14

FIGURE 2.6: Input Offset Voltage Relationship 14

FIGURE 2.7: Input Offset Monte Carlo 15

FIGURE 3.1: Basic 4 bit Capdac with bottom plate sampling 16

FIGURE 3.2: 10 bit split differential CAPDAC 18

FIGURE 3.3: PMOS Sample Switch 20

FIGURE 3.4: Bi-lateral SP3T Switch 21

FIGURE 3.5: Block Diagram for evaluating CAPDAC SINAD 21

FIGURE 3.6: CAPDAC Spectrum 22

FIGURE 3.7: CAPDAC SINAD Monte Carlo Simulations 23

FIGURE 4.1: SAR Logic Flow Diagram 25

FIGURE 5.1: Simulation Testbench 26

FIGURE 5.2: ADC Output Spectrum Measurement 27

FIGURE 6.1: Time Interleaved ADC Circuit 31

FIGURE 6.2: ADC Output Spectrum Measurement 32

LIST OF ABBREVIATIONS

ADC Analog to Digital Converter

BER Bit Error Rate

CAPDAC Capacitive Digital to Analog Converter (Charge Redistribution)

CMOS Complimentary Metal-Oxide-Semiconductor

DAC Digital to Analog Converter

DFT Discrete Fourier Transform

DNL Differential Non-Linearity

ECE An acronym for Electrical and Computer Engineering.

ENOB Effective Number of Bits

INL Integral Non-Linearity

IRN Input Referred Noise

LO Local Oscillator

LSB Least Significant Bit

MSB Most Significant Bit

PDK Process Design Kit

QAM Quadrature Amplitude Modulation

RF Radio Frequency

SAR Successive Approximation Register

SFDR Spurious Free Dynamic Range

SINAD Signal to Noise and Distortion Ratio

THD Total Harmonic Distortion

PREFACE

Today's wireless communication systems often employ quadrature modulation to make efficient use of the channel bandwidth. The receiver is often realized as a quadrature direct conversion receiver like the one shown in figure 1. The incoming RF signal is split and directed to two different mixers. One mixer is driven by the LO directly, while the other is driven by a 90 degree phase shifted version of the LO signal. This action breaks the baseband signal into an in-phase component and a quadrature phase component. These baseband signals each represent one half of the channel bandwidth, meaning that each analog to digital converter only needs to have a Nyquist rate of $\frac{1}{2}B_w$. For example, to convert a IEEE 802.11be (Wi-Fi 7) signal with a 320 MHz channel bandwidth, two ADC's, each having a sample rate of 320 MSPS can be used. However, this is the absolute minimum as Nyquist's theorem suggests. For practical applications, the converter's speed must exceed the minimum. This paper will evaluate the Successive Approximation Register (SAR) ADC architecture for suitability in these applications.

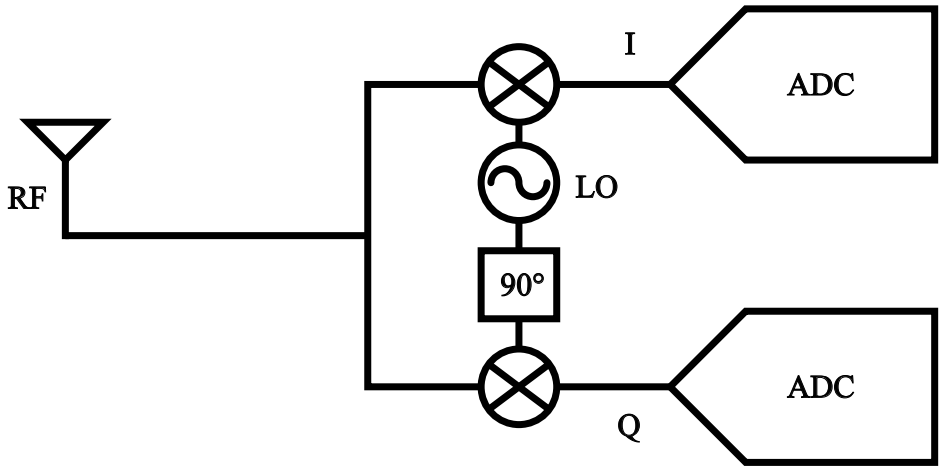

Figure 1: Modern Receiver Front End

CHAPTER 1: INTRODUCTION

1.1 Problem Statement

Modern communications systems rely on the use of data converters to convert digital data to a transmittable analog signal, and to convert a received analog signal to usable digital data. The performance of these data converters proves to be critical as data rates increase. The conversion speeds and resolution needed to accommodate the next generation of wireless standards have been easily achievable for some time; however, the power consumption can be improved for mobile devices. This work will focus on the design of a Time-Interleaved SAR ADC that will meet Wi-Fi 6e specifications. As shown in works [1] and [2], this ADC architecture has the ability to meet the bandwidth and precision specs necessary while consuming much less power than the traditional pipelined or flash converters.

1.2 Overview

1.2.1 Theory of Operation

A SAR Analog to Digital Converter contains four main components as shown in figure 1.1: A sample and hold circuit, a digital to analog converter, a comparator, and the SAR logic circuit. As the name suggests, this type of converter uses a successive approximation algorithm to resolve the digital code that represents the analog input. The analog signal is first sampled and held, this becomes the target value to be converted. The DAC then produces a reference voltage using the digital code supplied by the SAR logic. This reference voltage is compared against the target value from the sample and hold circuit and the results are fed back to the SAR logic, which will create a new reference value for the DAC. This process continues until the

digital code is found. Figure 1.2 in the next section shows an example of a conversion cycle for a SAR converter using a Binary Search Algorithm.

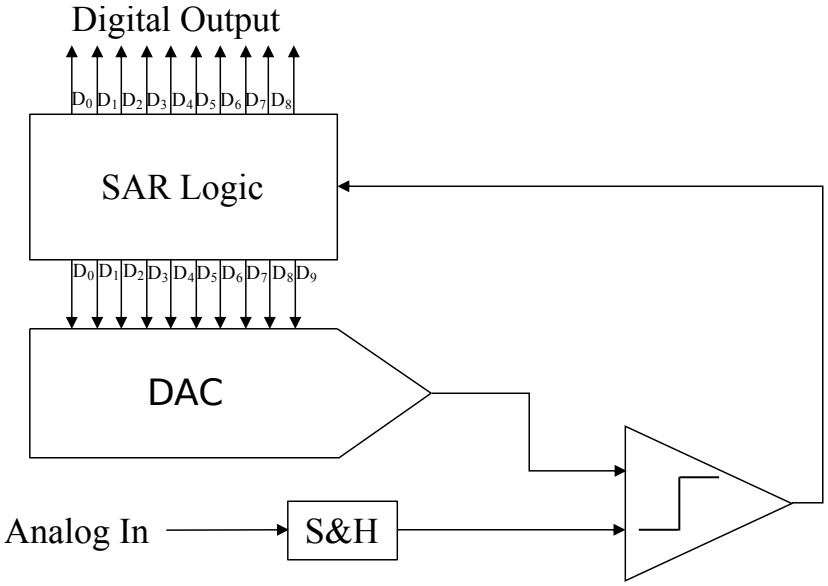

Figure 1.1: SAR ADC Block Diagram

1.2.2 Binary Search Algorithm

Many different algorithms can be employed to resolve the output code, however the Binary Search Algorithm is the predominant choice for SAR converters. This algorithm aims to find the output by testing each bit in an N bit converter. Figure 1.2 shows an example of a conversion cycle using a binary search algorithm. First, the most significant bit (MSB) is tested by setting its value to a 1, and the remaining bits are set to 0. The digital code is then converted to a voltage and compared to the analog input voltage. In the case of the MSB, the analog value is half of the reference voltage. If this value is less than the analog input, then the corresponding output bit is set to a 1. If this value is greater than the analog input, the output bit is set to a 0. Each bit is tested in the same manner, and once the least significant bit (LSB) is tested, the digital code has been found. Therefore, an N bit ADC requires N cycles to complete one conversion using the binary search algorithm. Other search algorithms have been attempted in SAR ADCs such as in [3]; however, they will not be covered

in this work.

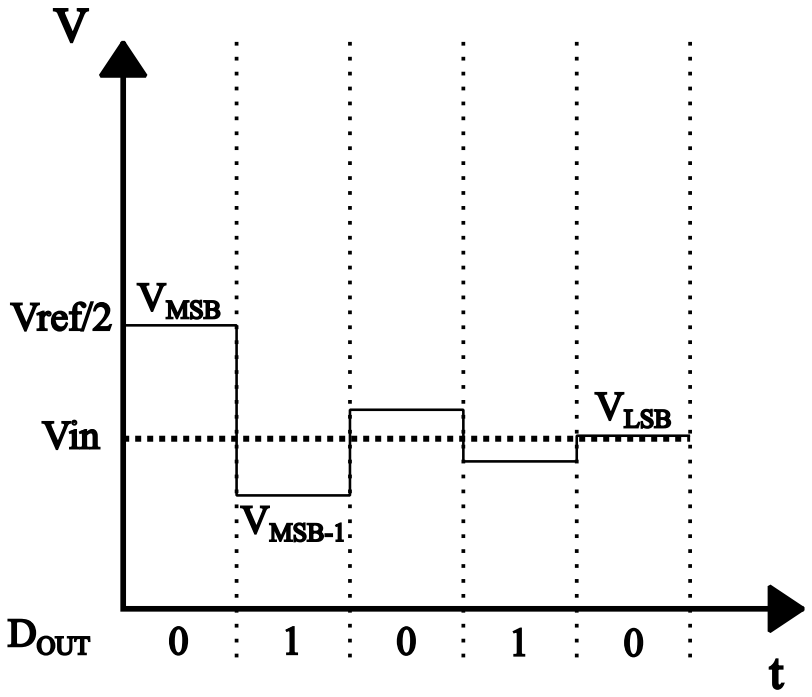

Figure 1.2: Binary search based conversion cycle

1.2.3 Time Interleaving

Since SAR ADCs require N clock cycles to produce one conversion, the bandwidth is typically much lower than other architectures. However, no operational amplifiers are required in a SAR converter, meaning very little quiescent current is necessary for operation. This makes the SAR converter much more power efficient than its pipelined and flash counterparts. The question becomes: how do we make a converter that has the bandwidth of a pipelined converter and the power consumption of a SAR converter? The time interleaving approach has proven to satisfy the needs of a high speed converter while also consuming very little power [4]. In this approach, several SAR ADCs act in parallel, with the start time of each converter being offset. Figure 1.3 shows an example of a 10 bit interleaved converter with 5 ADCs.

Each of the ADCs start their conversion cycles 2 clock cycles after the previous converter. With this method, a new conversion will be available every 2 clock cycles

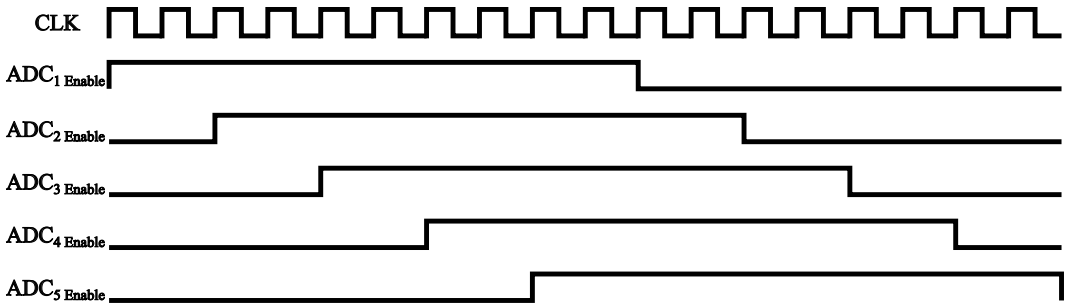

Figure 1.3: Time Interleaved Converter Timing Diagram

rather than every 10 (after waiting for the first conversion cycle to complete). This results in an obvious increase in the converters bandwidth since the sample rate is effectively 5 times faster. Clearly, increasing the number of converters will also increase the total power consumption and space requirements. This work aims to evaluate these metrics and determine if this approach is suitable for current wireless standards.

1.3 Scope of Work

In this thesis, a Successive Approximation Analog to Digital Converter is designed at the component level. The design is implemented in the fictional Cadence Generic 45nm CMOS process and is built using the Cadence Virtuoso design environment. An analysis will be made of the various components in the circuit, and simulations will be performed to the highest level of scrutiny. The 45 nm Generic Process Design Kit (PDK) from Cadence is a decent emulation of modern design kits containing most of the same features as the PDK for a real process.

CHAPTER 2: COMPARATOR DESIGN

The focus is now shifted to the analog comparator design. An ideal comparator exhibits an input-output relationship like that shown in figure 2.1. The comparator circuit accepts two input signals and evaluates which of the two has a larger voltage. In the example, the input voltage is a differential sine wave, and the output is the digital result of the comparison. When the voltage at the positive input terminal is less than the voltage at the negative input terminal, the output is a logical LOW. When the voltage at the positive input terminal is greater than the voltage on the negative input terminal the output is a logical HIGH. As shown in figure 1.1, the comparator must accurately determine whether the sample and hold input is greater than the output of the DAC for each cycle in the binary search. In a realistic design, the comparator must perform well enough to ensure reliable analog to digital conversion. Factors that contribute to the comparators performance are discussed at length in this chapter.

2.1 Considerations

2.1.1 General

The comparator must be carefully designed to ensure accurate and efficient operation of the SAR converter. Some major design concerns include: speed, power consumption, offset, and space. Within a data converter, the comparator must reach a decision and latch the result within each clock period. Though a trivial requirement, the speed imposes a direct tradeoff with almost all other requirements. Power consumption must be weighed, especially for mobile designs. The chosen comparator topology typically has the most impact. A dynamic comparator, like the Strong

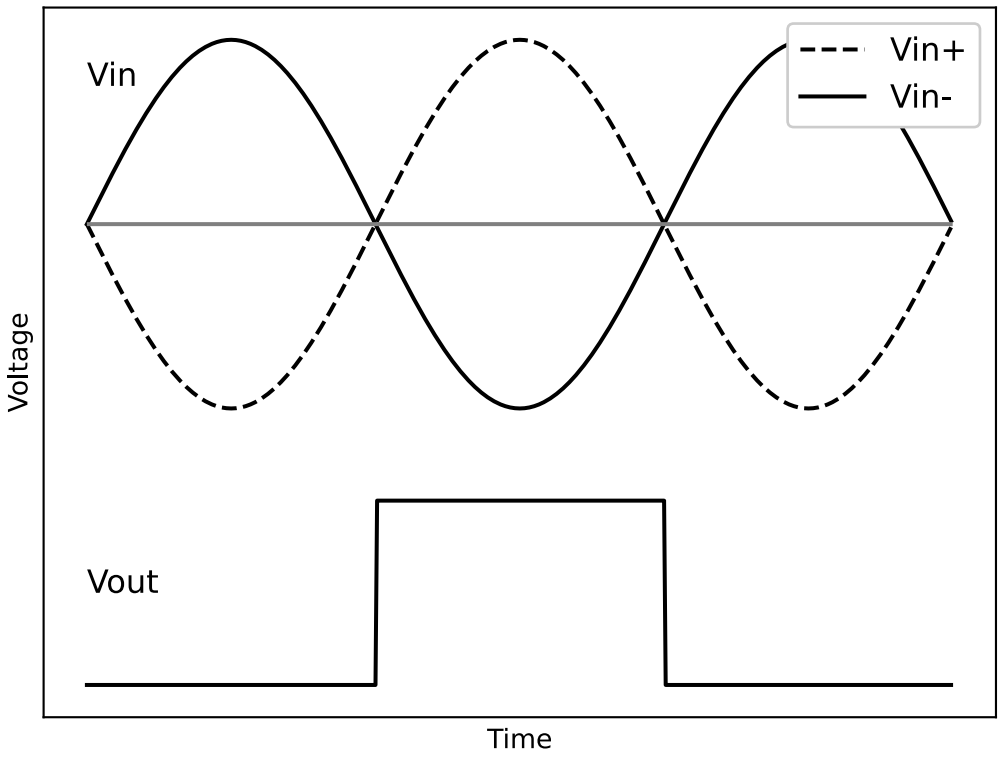

Figure 2.1: Comparator input-output relationship

Arm Latch, only consumes power when the input clock is high. A static comparator requires no input clock and provides an output continuously. Aside from power consumption, the dynamic comparator is also the ideal choice to prevent unwanted noise feedback. As shown later, the input offset and die area also have a direct relationship. Typically, the offset can be reduced by increasing the transistor area, taking more space and more power, and for some devices in the circuit, this can result in lower speed. For this design, a Strong Arm Latch comparator topology is chosen because of its prevalence in similar applications.

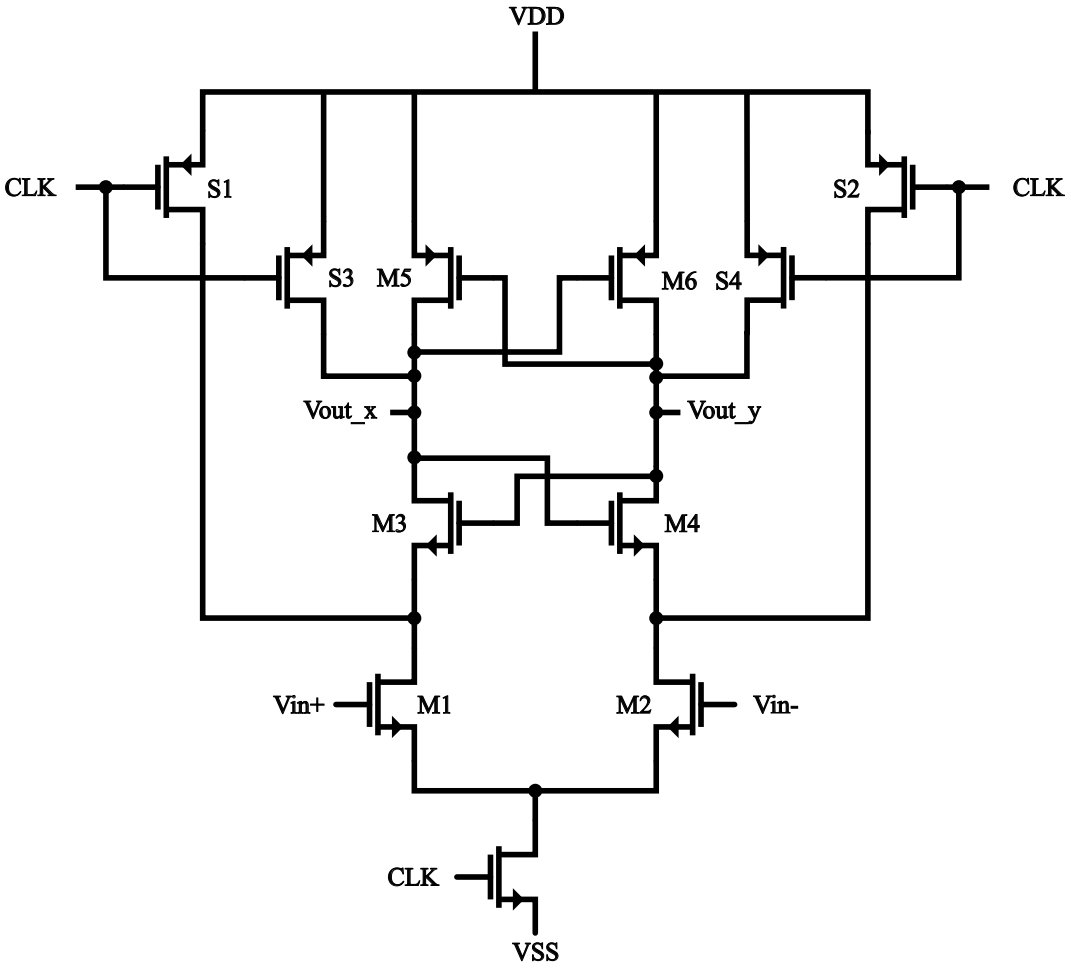

Figure 2.2: Strong Arm Latch Comparator

2.1.2 Input Offset

The input offset of a comparator is simply the input voltage which causes the output to change. In a perfect world, the input offset would be 0V, where any negative voltage difference across the input terminals results in a logic level LOW at the output, and any positive voltage difference causes a logical HIGH. In practice, zero input offset is an impossible challenge due to mismatch imposed by the process. Early in the design, a tolerable input offset voltage must be selected prior to sizing the input devices, M1 and M2. The method detailed in [5] can be used to size these components via equation 2.1.

$$\Delta V_{TH1,2} = \frac{A_{VTH}}{\sqrt{WL}} \tag{2.1}$$

Where the width (W) and length (L) must be selected to minimize the fraction. The length is set to the process minimum, and the width is scaled to provide enough current to drive the output, while minimizing the offset. The value of A_{VTH} is defined for the process and is typically expressed in $\frac{mV}{\mu m}$. $\Delta V_{TH1,2}$ gives the standard deviation of the threshold voltage mismatch. Assuming that the distribution is gaussian, roughly 68% of the produced devices will have less offset than this value. To examine the effect at higher yields, such as 3σ, this value can merely be multiplied by 3.

When sizing the tail device, the width can be chosen to give $V_{DS} = V_{CM} - VGS1$ when the clock source is high. The sizing of the remaining devices is less mathematical and more empirical. For example, M3 and M4 have approximately 1/4th of the effect on the input mismatch, and are often initially chosen to be the same size as M1 and M2 for simplicity. Initially, M5 and M6 are chosen to be very small since the offset contribution is small and the effect on the speed is minimal. These sizes can be increased later if need be. The latch devices, S1-S4 are chosen to ensure they can pull the drain voltage to VDD within a reasonable rise time. Experimentation will need to be done to choose the best value, but a small width often suffices. These choices have very negligible effects on the input offset[5].

2.1.3 Metastability

Metastability in a comparator is analyzed to examine the error caused by the settling delay at the output. For decreasing input differential voltages, the time required for the output to settle is increased. For the comparator, a digital signal level must be reached within the sampling time T_s of the clock pulse. With that in mind, very small differential input voltages (much smaller than the LSB step size) will cause the comparator to enter a "meta-stable" state, meaning that a decision

cannot be made within the sampling time T_s and a bit error occurs[6].

In the context of the whole converter, a meta-stable state is more likely to occur when the code being tested is very near the input voltage. If detection circuitry is added and a meta-stable state is detected, it is likely that the current code being compared to the input is very near the optimal output code. This is only true when the LSB step size is larger than the input voltage difference that causes a meta-stable output. Metastable detection circuits are not discussed in this work but are discussed in [6] and [7].

The effect of the metastability conditions can be observed by obtaining the Bit Error Rate (BER) of the comparator. The BER should be minimized to improve the accuracy of the converter and reduce the number of output errors. The Bit Error Rate is largely driven by the ratio between the latch voltage swing and the latch step size, along with the ratio between the sample period and the latch time constant. The relationship is shown in equation 2.2 where $\frac{V_{Latch}}{V_{LSB}}$ is typically set to 2^N. Small changes to this ratio have very little effect on the BER as the result is dominated by $\frac{T_s}{\tau}$

$$BER \approx \frac{V_{Latch}}{V_{LSB}} e^{-\frac{T_s}{\tau}} \tag{2.2}$$

T_s is the sample period and τ is the time constant of the latch output node. This time constant is largely driven by the transconductance and capacitance of the latch devices and can be modified by changing the device dimensions and current. These parameters are chosen to obtain the acceptable bit error rate. This error rate is also equal to the fraction of the LSB step size (α) that causes the metastability conditions to be met. For example, if a comparator has a BER of 10^{-8}, then a metastable state occurs when the input voltage difference is less than $10^{-8} * V_{LSB}$[6].

2.1.4 Input Referred Noise

Evaluating the input referred noise in a comparator is a necessary step in its design as the presence of noise can result in errant outputs. However, computing the input noise of a comparator is typically much more involved than computing the input noise of an amplifier. With an amplifier, the output noise is measured and referred to the input by dividing by the gain. This method cannot work with a comparator due to it having a digital output. A common method for evaluating the input noise involves evaluating the probabilities of zeros and ones when a well defined input is present. First, inputs V_{ip} and V_{in} are tied together, giving zero offset between them and a noise simulation is performed. The probability of the output being a one or zero is evaluated, and should result in a gaussian distribution. If the comparator is well balanced, there should be equally as many zeros and ones output. A small differential voltage is then applied to the input to evaluate the effect on the output probabilities. The voltage is varied to determine a value that causes the probability of a zero to fall to 16% as the area under a gaussian distribution from $-\infty$ *to* $-\sigma$ is 16%. The total root mean square (rms) input referred noise is approximately equal to this input voltage. The precision of the simulation can be improved by increasing the number of clock cycles for a larger set of data, and the voltage step size should be as small as possible[8][9].

2.1.5 Kickback Noise

Since the input of the comparator can vary drastically in a short period of time, it is likely that many of the devices in the circuit will operate in all regions of operation. Over the sample period, the charges present on each device can vary greatly due to these region changes. These charges are supplied and dissipated through the power supply, thus causing variation in the rail voltages. These charges can be reflected on the input and reference voltages and the comparator's decision can be affected.

This "kick-back" noise is undesired and must be minimized. In converter designs containing multiple comparators, such as the time-interleaved converter discussed, the effect compounds. We also note that this "kick-back" becomes more concerning when it occurs at the same time that a decision is made. The circuit's kick-back noise is largely driven by the dimensions of the input transistors in the Strong Arm Latch topology[5][6].

2.2 Design

The comparator must be designed with the above considerations in mind. The logical first choice to make is the acceptable input referred offset. In this design, the input offset should be minimized, but an offset of 5 mV is set as the initial target. Setting the channel length to the process minimum, equation 2.1 can be solved to find an initial value for the width of the input devices M1 and M2. Knowing that M3 and M4 have a minimal contribution to the input offset, they are made much smaller than M1 and M2 to improve the speed of the comparator. M5 and M6 can also be made small for the same reason. S1-S4 must be made as small as possible to ensure fast switching time. The tail current source is sized to ensure that $V_{CM} - V_{GS1} = V_{DS}$. These devices have negligible results on the input offset. The input referred noise, input offset, and speed are simulated and iterations of device sizes are made to maximize performance.

2.3 Simulation Analysis

The comparator design must be evaluated for to ensure it's suitability for use in this converter. To perform this evaluation, we must simulate both the input referred noise, and the input offset. The combination of these two parameters will account for the majority of the non-idealities relating to the comparator. These simulation results will be used in the final ADC SINAD calculation, and will aid in determining the yield of the design.

2.3.1 Input Referred Noise

To evaluate the input referred noise, the comparator is connected to the test circuit as shown in figure 2.3.

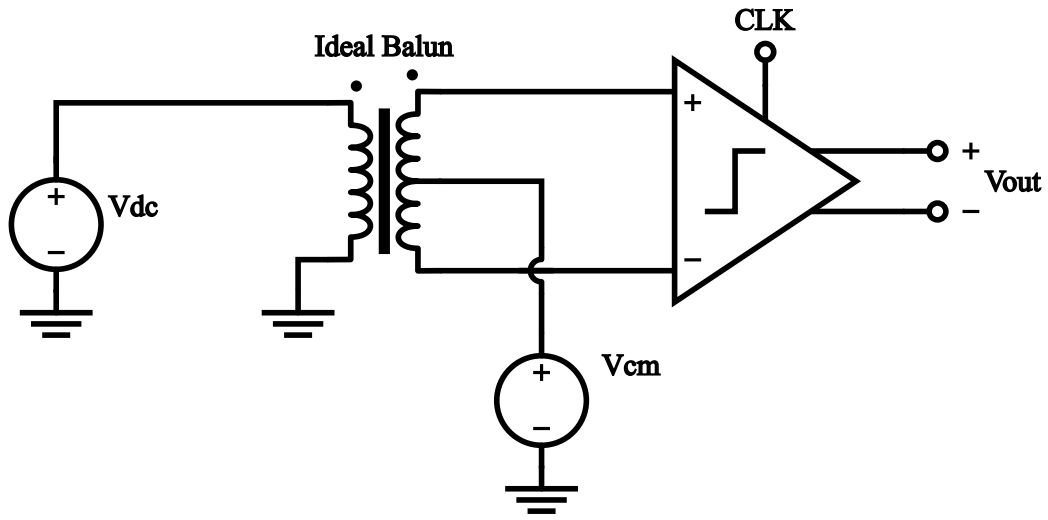

Figure 2.3: Schematic for evaluating Input Referred Noise

The input noise of the comparator has an obvious random effect on the decision of the converter. To mitigate this issue, the noise level must remain below $\frac{1}{2}LSB$. As discussed above, the traditional method for evaluating the comparator's input referred noise requires calibration of the comparators offset, and an analysis of the bit error rate. However, Cadence has included a feature in the PSS analysis that allows sampling the output noise at a specific time. Obtaining this noise spectrum at an instant when the comparator's output is transitioning to a logical high, and dividing by the gain gives a valid input referred noise measurement. This is often the preferred method because the results are fairly accurate and the simulation time is greatly reduced. Figure 2.4 shows the comparator's output noise over frequency. The output noise is integrated and divided by the gain to give a input referred noise of 300 μV_{RMS}, which is significantly less than $\frac{1}{2}LSB$.

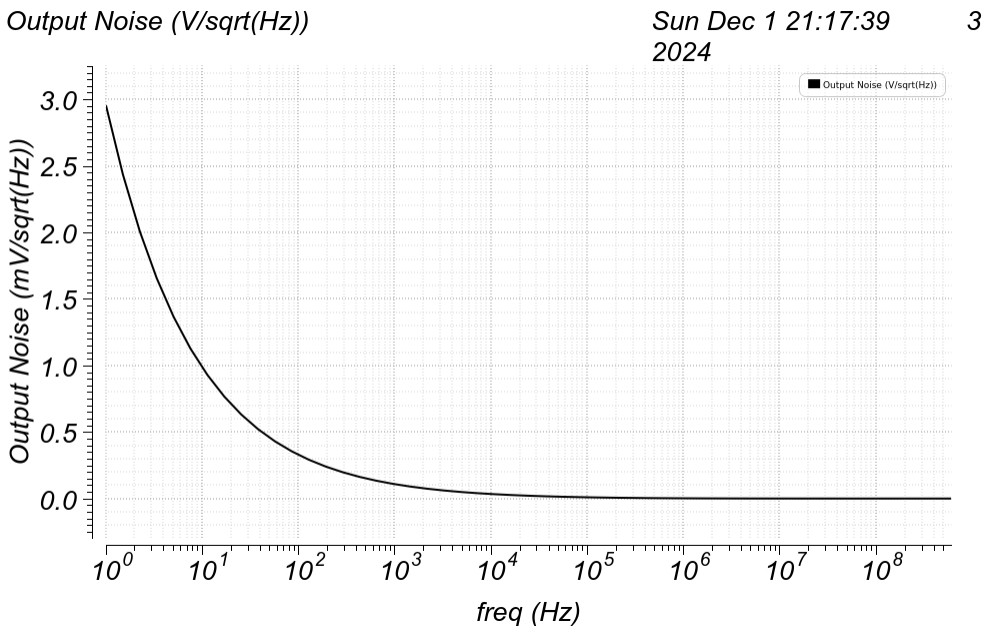

Figure 2.4: Output Noise Spectrum

2.3.2 Input Offset

The test circuit shown in 2.5 is used to determine the input offset voltage. Here, a ramp voltage is applied to the input, and the output is observed for a change in the decision. The input voltage at the instant when the comparators output changes is the input offset voltage. Since the input is a ramp voltage, the accuracy of the simulation relies upon the step size of the ramp. To increase the accuracy, the offset is first measured with the ramp starting at +5mV, and stopping at -5mV, then the ramp is reversed, starting at -5mV and stopping at +5mV. The value of the input is recorded for each crossing at the output, and the average of the two values is recorded.

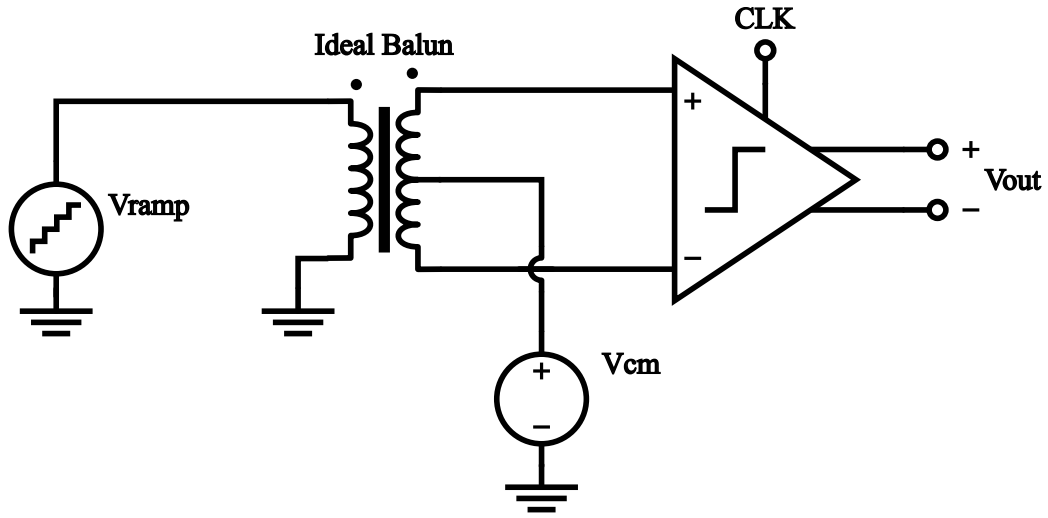

Figure 2.5: Schematic for evaluating Input Offset

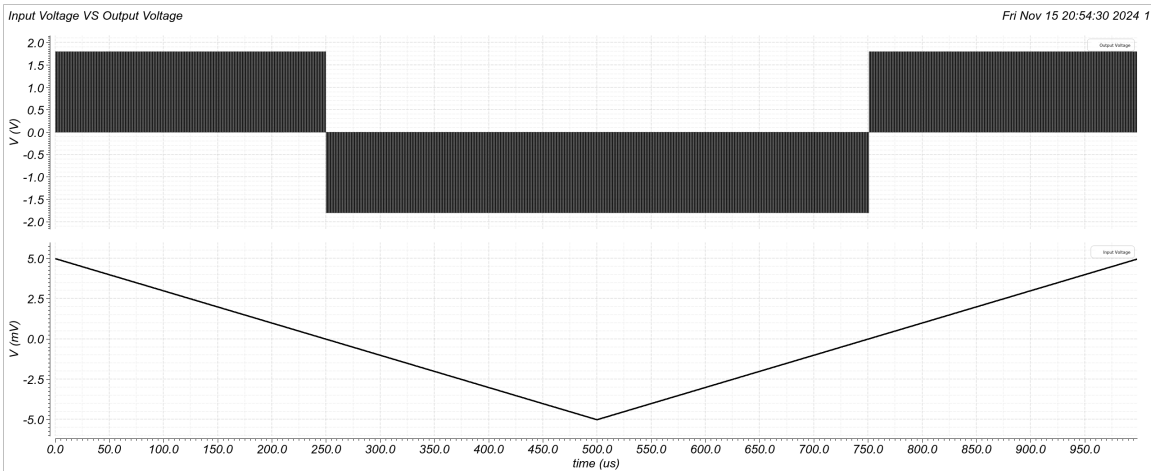

Figure 2.6: Input Offset Voltage Relationship

Figure 2.6 illustrates this simulation. Using this setup, a monte carlo analysis is performed to inspect the effects of process variation on the input offset. For this comparator, the input offset has a mean of -42.5 μV and standard deviation of 1.492 mV, giving a 3σ yield of 4.476 mV. This may seem like a large value in respect to the LSB size; however, this only results in a linear offset in the digital results due to the SAR architecture. For precision applications, some offset calibration techniques have been proposed such as [10] and [11]. In this application, the offset calibration is assumed to be performed in the digital domain and external to the converter.

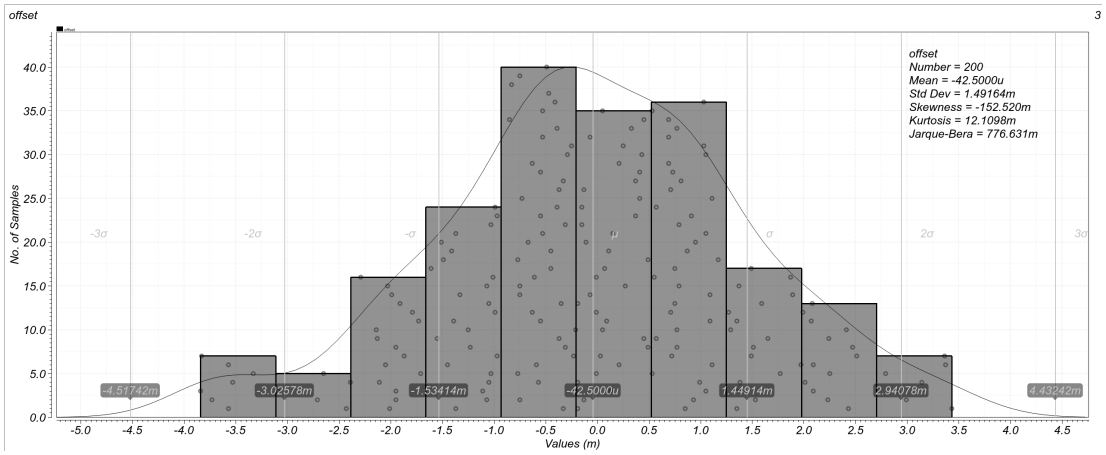

Figure 2.7: Input Offset Monte Carlo

CHAPTER 3: CAPACITIVE DAC DESIGN

In any SAR ADC design, the DAC design requires the most careful attention to ensure maximum performance is achieved. The overall accuracy of the ADC hinges mostly on the accuracy of the DAC. In this design, a capacitive DAC architecture is selected as it is the standard choice for such an application. A basic capacitive DAC is illustrated in figure 3.1 below. This particular version is a 4 bit design, which makes use of bottom plate sampling. With this architecture, the analog input, along with the positive and negative reference voltages, are connected to the bottom plate of each capacitor via a switch. With this topology, the sample and hold (or track and hold) circuitry is integrated into the DAC. By placing a switchable common mode voltage reference on the top plate, a current drain is made available for the analog input during tracking. In comparison to a top plate sampling circuit, this circuit provides improvement over the input range and linearity, with the cost of a slight increase in settling time due to the extra switch.

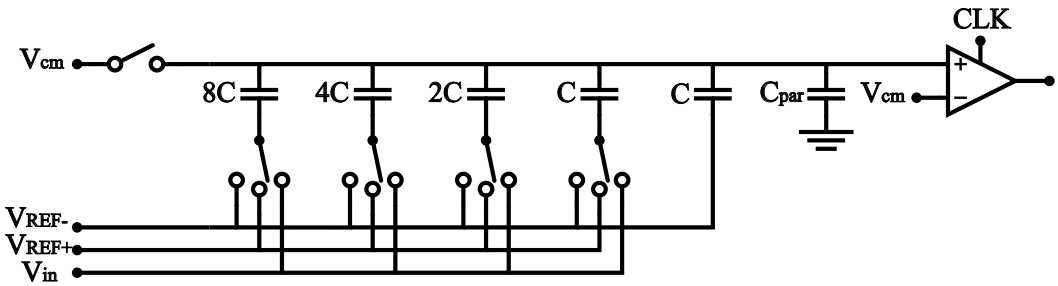

Figure 3.1: Basic 4 bit Capdac with bottom plate sampling

3.1 Considerations

3.1.1 General

When designing a DAC, some considerations need to be made prior to choosing a topology. Some important parameters to observe include the input voltage range, the settling speed, and in some cases, the total space consumed. This paper aims to design a circuit suitable for mobile Wi-Fi data acquisition, thus requiring a very fast, linear, low power, high resolution converter, that consumes very little space. Unfortunately, no topologies are ideal for all of these constraints simultaneously, so some tradeoffs must be considered. Below, figure 3.2 illustrates a bottom plate sampling, differential CAPDAC with a split capacitor array. By splitting the array with a unit capacitor of C, the maximum capacitor size is reduced to 16C in a 10 bit converter. A traditional converter would require a maximum capacitance of 512C, thus creating a large equivalent capacitance on the top plates, and requiring large currents to charge these capacitors at high speed. In addition to increasing the speed and reducing the current, the space consumed by the capacitor array is reduced by adding the splitting capacitor [12]. Another concern of this topology is the use of bottom plate sampling. Typically, bottom plate sampling has some effect on the settling time of the DAC, thus reducing the overall speed of the ADC. For this design, the speed loss due to bottom plate sampling is assumed to be less impactful than the gains in linearity and the input voltage range. Overall, the split differential CAPDAC with bottom plate sampling shows promise for this application where the space, speed, power consumption, linearity, and voltage range are constrained. Below, more detail is provided regarding the design and characterization of the CAPDAC.

3.1.2 Non Linearity

Perhaps the most concerning feature of a DAC is it's ability to convert digital code to an analog signal accurately. To evaluate the accuracy of a DAC, the differential

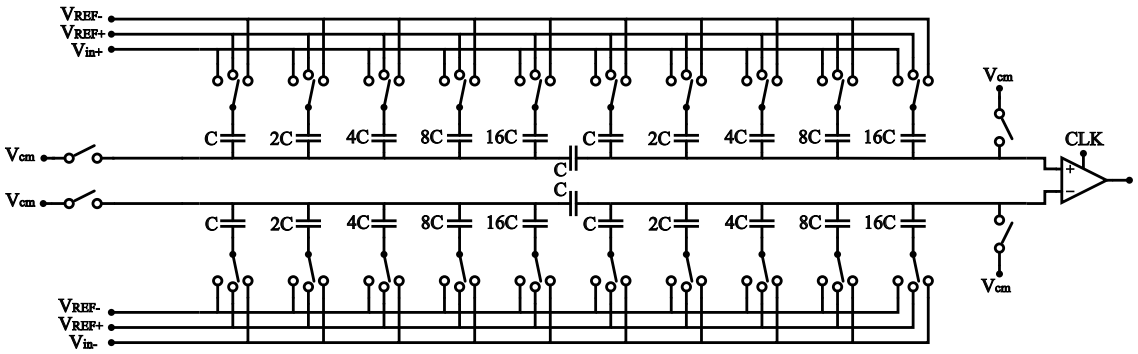

Figure 3.2: 10 bit split differential CAPDAC

non-linearity (DNL) and integral non-linearity (INL) must be observed. DNL is defined as the difference between the measured voltage step size and ideal voltage step size at each output code.

$$DNL(i) = \frac{\Delta v(i) - \Delta v_{ideal}}{\Delta v_{ideal}} \tag{3.1}$$

Integral Non-Linearity describes the maximum difference between the real and ideal output curves. Often, the INL is simply described as the sum of the DNL across all possible input codes. These values are typically exprssed with the LSB as the unit. The maximum DNL acceptable for a DAC in a SAR ADC is $\frac{1}{2}LSB$, meaning for a 10 bit DAC with a 1.8V output range, the output voltage must err no more than $\frac{1}{2} \times \frac{1.8}{1024} = 878\mu V$.

3.1.3 Capacitor Mismatch

The capacitive DAC must be designed such that the process variation negligibly impacts the performance. A unit capacitance must be selected such that the maximum DNL remains below $\frac{1}{2}LSB$ for the vast majority of produced die. Assuming the distribution of capacitance values over a production process is gaussian, the DNL can be computed utilizing the standard deviation. A proper design will ensure that all die having capacitors that match within 3 standard deviations (3σ) will have a DNL of no greater than $\frac{1}{2}LSB$. This will ensure that at least a 99.7% yield is realized.

Equation 3.2 evaluates the standard deviation of the maximum DNL for an N bit DAC given the standard deviation and capacitance of a unit capacitor. One must select a $\frac{\sigma_U}{C_U}$ to ensure that $3\sigma_{DNLmax}$ remains less than $\frac{1}{2}LSB$ (equation 3.3) [12].

$$\sigma_{DNLmax} = \sqrt{2^N - 1}\frac{\sigma_U}{C_U}LSB \tag{3.2}$$

$$3\sigma_{DNLmax} < 1/2LSB \tag{3.3}$$

$$C_{Ud,split} > 9 \times (2^M - 1) \times 2^{2(N-M)}K_\sigma^2 K_C \tag{3.4}$$

3.2 Design

The design process begins by characterizing the capacitor mismatch over process variation. To get a rough idea of the effects, a simple monte carlo simulation is performed to evaluate the capacitors. An S-Parameter analysis is performed to calculate the capacitance of various mim capacitors over the process variation. A unit capacitor is then selected by choosing the smallest capacitance that satisfies equations 3.2 and 3.3. During this design process, a 2.8 fF capacitor had a standard deviation of 12.5 aF, therefore giving:

$$\sigma_{DNLmax} = \sqrt{2^9 - 1}\frac{12.9 * 10^{-18}}{2.8 * 10^{-15}}LSB = 0.145LSB \tag{3.5}$$

$$3\sigma_{DNLmax} \approx 0.435LSB < 1/2LSB \tag{3.6}$$

This unit capacitor provides a good starting point for the design and can be adjusted later to improve either speed or reproducibility.

The switches depicted in figure 3.2, must then be implemented in the CMOS process. The sampling switch, connecting the common voltage reference to the top plate of the capacitors, is implemented using a basic PMOS switch, shown in figure 3.3. These switches are controlled by a single digital control voltage provided by the SAR

Logic circuit.

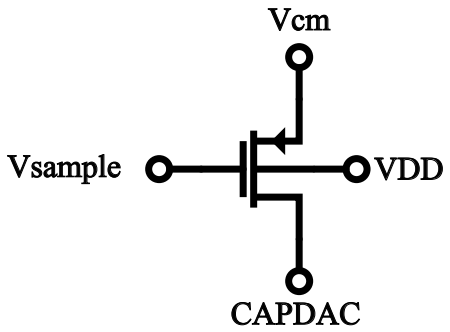

Figure 3.3: PMOS Sample Switch

The bottom plate SP3T switch is a little more complicated however. Additional logic must be added to choose between the 3 switch paths, an additional control voltage is needed to determine which path to enable. Figure 3.4 below shows the schematic of this SP3T switch with V1, V2 and V3 being the control voltages. These transistors must be sized to provide enough current to charge the attached capacitor, but must also be minimized to reduce area consumption. The length of each device is set to the process minimum, and the width is chosen by experimentation. A transient SINAD evaluation is performed while sweeping the width of the devices, and the final width is selected by observing when an increase in width has a negligible impact on the resulting SINAD.

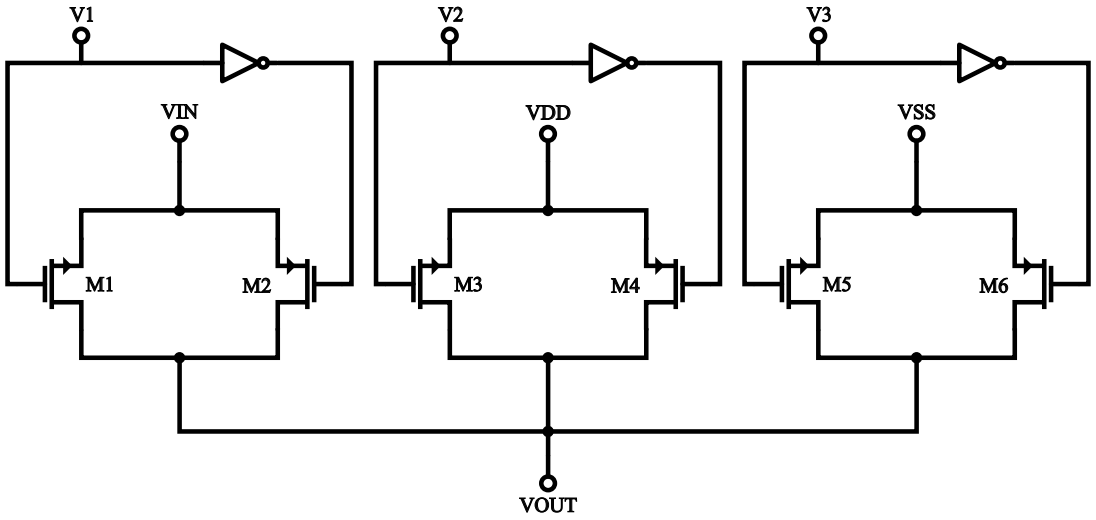

Figure 3.4: Bi-lateral SP3T Switch

3.3 Simulation Analysis

The CAPDAC must be analyzed over process variation to ensure that the performance goals will be met in manufacturing. A monte carlo analysis is performed measuring the SINAD of the DAC over 200 iterations of random mismatch. The resulting mean and standard deviation of the SINAD can be used to determine the impact of the mismatch on the final ADC design. To perform this analysis, the test circuit in figure 3.5 is connected.

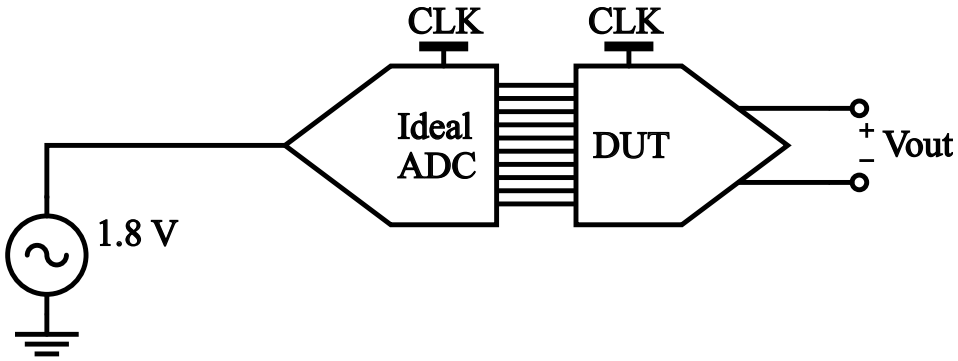

Figure 3.5: Block Diagram for evaluating CAPDAC SINAD

A sine wave is fed into an ideal ADC to create the digital input to the DAC. The sine wave is converted to analog by the DAC and the output is recorded. The SINAD measurement is performed utilizing the built in spectrum measurement function in

Cadence Spectre. This function performs a DFT on the output sine wave and uses the frequency domain information to compute the SINAD. With this same information, the converter's ENOB, SFDR, and THD can be computed. The output spectrum for a typical CAPDAC is shown below in figure 3.6.

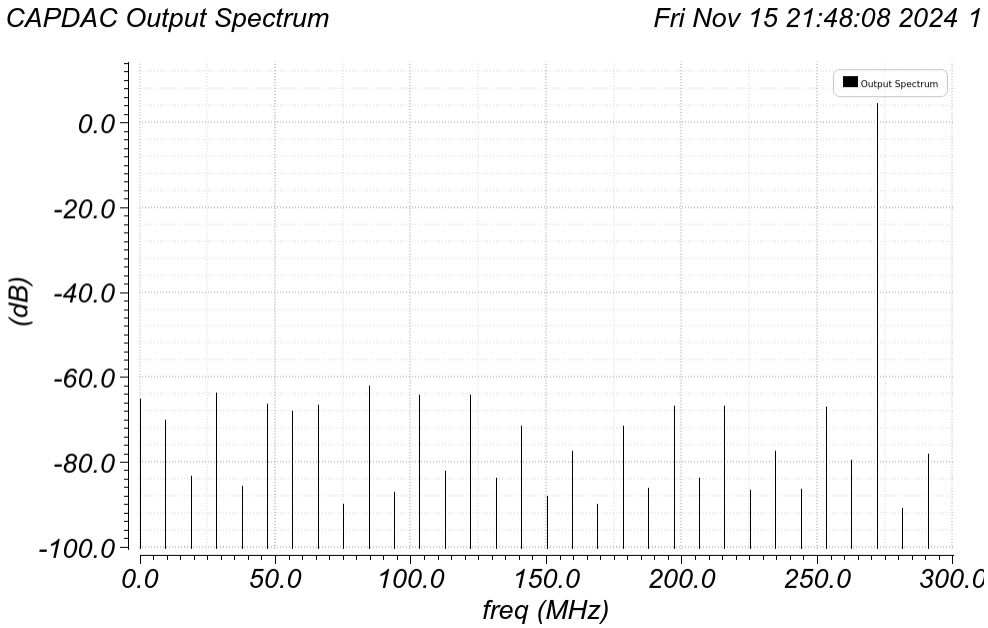

Figure 3.6: CAPDAC Spectrum

The SINAD values are recorded for each iteration of the monte carlo analysis, where the mean and standard deviation can later be extracted. For this design, the mean of the SINAD was 55.9 dB giving a mean ENOB of 8.99. The SINAD standard deviation was 2.37 dB. With a target yield of 3σ, the worst DAC will have a SINAD of 48.79 dB, and an ENOB of 7.8. These results will be factored into the computation for the complete ADC design.

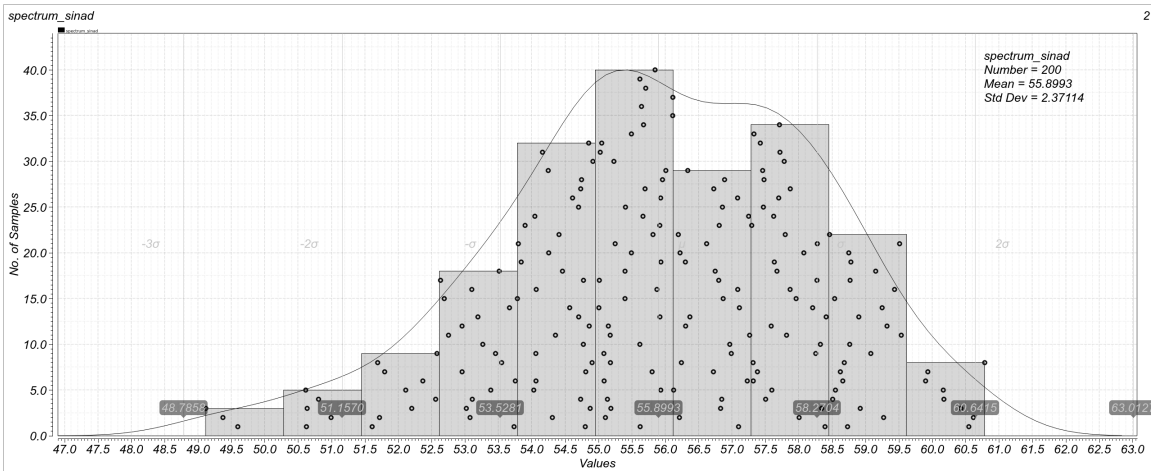

Figure 3.7: CAPDAC SINAD Monte Carlo Simulations

CHAPTER 4: SAR LOGIC DESIGN

The digital control portion of the SAR ADC is implemented utilizing Verilog-A. The script mirrors that of a simple state machine where the state is incremented each clock cycle. The design for this converter utilizes 12 distinct states, starting with 2 sample states, followed 10 states representing each bit test in a binary search. Figure 4.1 shows the flow of the converter's logic design. The converter starts its conversion cycle by outputting the digital results of the last conversion cycle, while setting the sample switch to the closed position. The converter will then begin the sample and hold process by pre-charging the DAC capacitors to a level determined by the analog input, which is connected to the bottom plate. After the two sampling cycles are complete, the controller will switch the input on the bottom plate of the MSB capacitor to VDD. The output from the comparator will then be measured to determine if the stored analog level is greater than 1 MSB. This process is completed 10 times for each bit in an 10 bit converter. If the analog level is greater than the bit under test, the output buffer will store a "1" for that bit. If the analog level is less than the bit under test, a "0" is stored. Once all 10 bits are tested, the conversion is considered complete, and the digital code is ready to output at the beginning of the next conversion cycle.

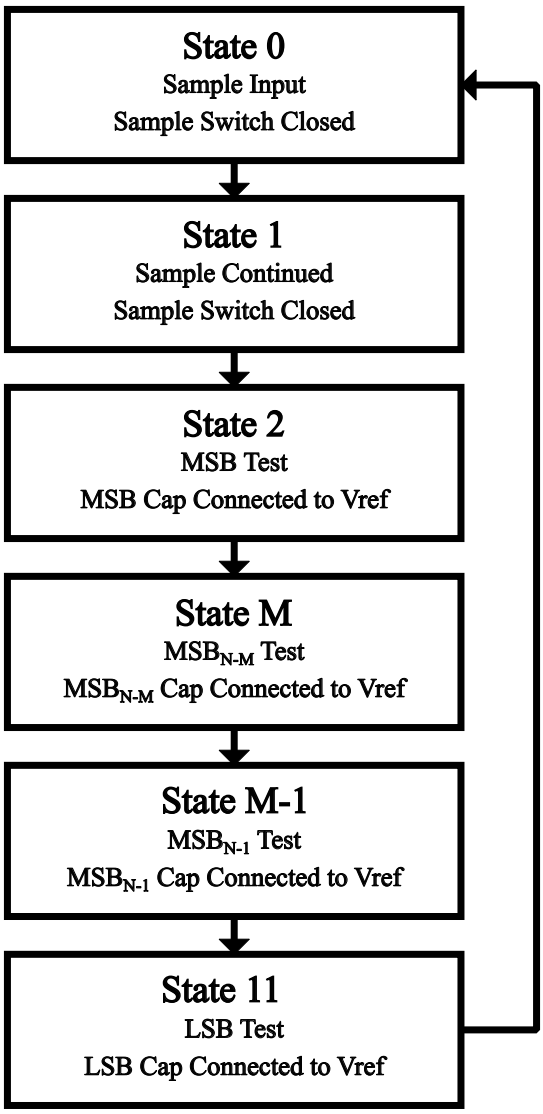

Figure 4.1: SAR Logic Flow Diagram

CHAPTER 5: COMPLETE ADC DESIGN AND SIMULATION

Once the individual components have been designed, they can be combined to create the full ADC circuit shown in figure 1.1. The circuit will now need to be validated for performance through simulation, and the layout process can begin.

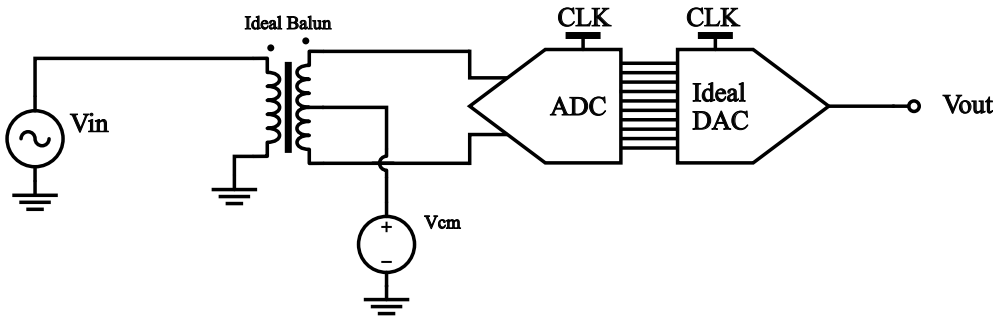

Figure 5.1: Simulation Testbench

To begin, the circuit is connected as shown in figure 5.1 and a transient simulation is performed. From this transient simulation, the SINAD, ENOB, SFDR and THD can be obtained by performing an FFT. To avoid any dependency introduced by windowing, the converter is simulated using coherent sampling as shown in equation 5.1.

$$f_{Input} = \frac{N_{Window}}{N_{Record}} * f_{Sample} \tag{5.1}$$

Where N_{Window} is the number of cycles in the FFT window and should be a prime number. N_{Record} is the number of data points and should be a power of 2. For this design the sampling frequency is 100MSPS, N_{Window} is chosen to be 29, N_{Record} is 64, thus requiring an input frequency of 45.3125 MHz.

Figure 5.2 shows the resulting spectrum of the ADC. The design has a nominal SINAD of 55.71 dB and an ENOB of 8.96. From our simulations from the CAPDAC

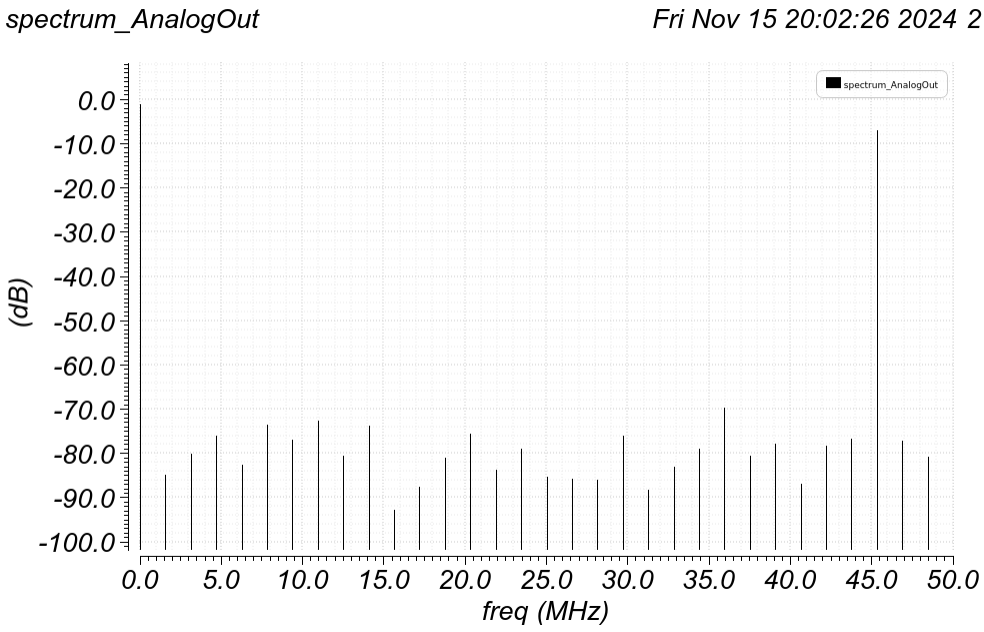

Figure 5.2: ADC Output Spectrum Measurement

and the Comparator, we calculate the minimum 3σ SINAD and ENOB due to the extremely lengthy monte carlo simulation time for the whole converter. A decent approximation can be performed by summing the noise contributions of each component in the circuit to calculate the SINAD.

$$N_{total} = \sqrt{N_{Quantization}^2 + N_{CAPDAC}^2 + N_{Comparator}^2} \tag{5.2}$$

Where the quantization noise is calculated using the input voltage range from the simulation and is given as the LSB step size over $\sqrt{12}$. These simulations were performed with an input AC source with 0.9 vpp, giving $\Delta v = \frac{0.9V}{2^{10}} = 0.88mV$.

$$N_{Quantization} = \frac{\Delta v}{\sqrt{12}} = \frac{0.88mV}{\sqrt{12}} = 254\mu v_{rms} \tag{5.3}$$

The CAPDAC noise contribution can be broken into two components resulting from the SINAD of the nominal CAPDAC and the SINAD from the 3σ mismatched CAPDAC.

$$N_{CAPDAC_{Ideal}} = \sqrt{SINAD^2_{nominal,vrms} - N^2_{Quantization}} \tag{5.4}$$

$$N_{CAPDAC_{Mismatch}} = \sqrt{SINAD^2_{mismatch,vrms} - N^2_{Quantization}} \tag{5.5}$$

Making the total contribution of the CAPDAC:

$$N_{CAPDAC} = \sqrt{N^2_{Capdac_{mismatch}} + N^2_{Capdac_{ideal}}} \tag{5.6}$$

The comparator noise is given directly from the previous simulation and is $300uVrms$. Using the values obtained in the previous sections we obtain:

$$N_{CAPDAC_{Ideal}} = \sqrt{521^2\mu v_{rms} - 254^2\mu v_{rms}} = 455\mu v_{rms} \tag{5.7}$$

$$N_{CAPDAC_{Mismatch}} = \sqrt{1.157^2 m v_{rms} - 254^2\mu v_{rms}} = 1.113 m v_{rms} \tag{5.8}$$

$$N_{CAPDAC} = \sqrt{455^2\mu v_{rms} + 1.113^2 m v_{rms}} = 1.2 m v_{rms} \tag{5.9}$$

With a total noise of:

$$N_{total} = \sqrt{254^2\mu v_{rms} + 1.2^2 m v_{rms} + 300^2 u v_{rms}} = 1.26 m v_{rms} \tag{5.10}$$

And an equivalent SINAD of:

$$SINAD = 20\log\left(\frac{Vin_{rms}}{N_{total,rms}}\right) = 20\log\left(\frac{318 m v_{rms}}{1.26 m v_{rms}}\right) = 48dB \tag{5.11}$$

giving a 3σ ENOB of:

$$ENOB = \frac{SINAD - 1.76dB}{6.02dB} = 7.68Bits \tag{5.12}$$

This is obviously a long way off from the value obtained by simulating the nominal ADC. This calculation concludes that 3σ or 99.7% of the produced die will have a SINAD greater than 48 dB and an ENOB greater than 7.68 bits. Comparing these values to the 3σ SINAD obtained for the CAPDAC (48.79 dB), shows that the ADC's SINAD is mostly impacted by the CAPDAC mismatch. Improvement to nominal CAPDAC linearity could improve the 3σ SINAD, or the unit capacitor size can be increased to reduce the effects of mismatch.

CHAPTER 6: TIME INTERLEAVED DESIGN

Time Interleaving multiple analog to digital converters allows the use of efficient architectures that are typically limited in speed, in high speed applications. In theory, time interleaving multiple ADC's is a simple task, simply place N_{int} converters in parallel, and start the conversions asynchronously to increase the output sampling rate. In practice; however, there will be mismatch between the converters, causing spurs in the frequency domain, which must be accounted for. Some recent works such as [13] include calibration to mitigate the spectrum effects of converters with low interleaving factors (N_{int}). Spurs in the output spectrum often occur at frequencies equal to integer fractions of the sampling frequency. These spurs are mostly caused by DC offsets between each converter. For this design, a 4x interleaving factor is selected, and these spurs are expected at fs/4, fs/2, and 3fs/4. The total power of these spurs is approximately equal to the variance of the DC offset voltage σ^2_{voff} [6].

Since this design implements a 4x interleaving factor, 4 of the above designed ADC's are placed in parallel and are timed to begin converting sequentially. Since the designed 10 bit converter also uses 2 additional clock cycles for sampling, a total of 12 cycles are necessary for each conversion. The sub-ADC's are then timed so that a new conversion begins every 3 clock cycles. These sub-ADC's make use of an additional enable pin, allowing them to be turned on/off by setting this input HIGH or LOW. A simple switching circuit is controlled by a verilog-A block, setting the enable input appropriately. For output multiplexing, another verilog-A model is used to select the appropriate output as each converter completes its cycle. A data-ready pin is available on the sub-ADC's to signal when the conversion is complete. Figure 6.1 shows the schematic of the time-interleaved converter.

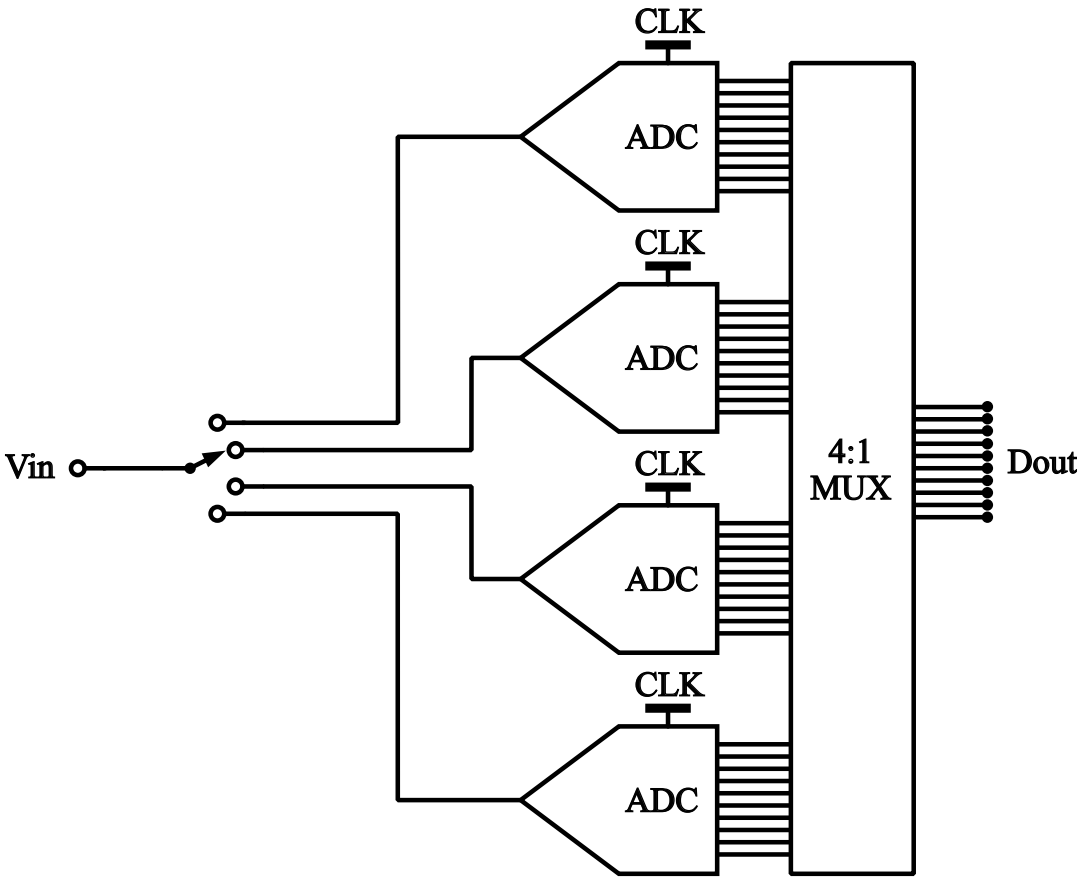

Figure 6.1: Time Interleaved ADC Circuit

The converter is evaluated using the same test circuit shown in figure 5.1, where the sub-ADC is replaced by the time-interleaved converter. A spectrum analysis is performed to evaluate the nominal SINAD, ENOB, and SFDR. With the 4x interleaving factor, the sample rate of the converter is increased to 400 MSPS. The DFT and input parameters are modified to ensure coherence. The window is chosen to be 29, while the sampling frequency is increased to 400. The number of points is reduced to 128 to improve simulation time. Again, a monte carlo analysis will not be performed due to simulation time requirements, so these results do not demonstrate the effects of mismatch. The output spectrum of this nominal converter is shown in figure 6.2.

With this design the nominal SINAD is 51.289 dB, which is less than that of the sub-ADC's. The ENOB is 8.23 bits while the SFDR is 58.8 dB. This degradation in performance is likely due to the analog bandwidth of the CAPDAC and would likely

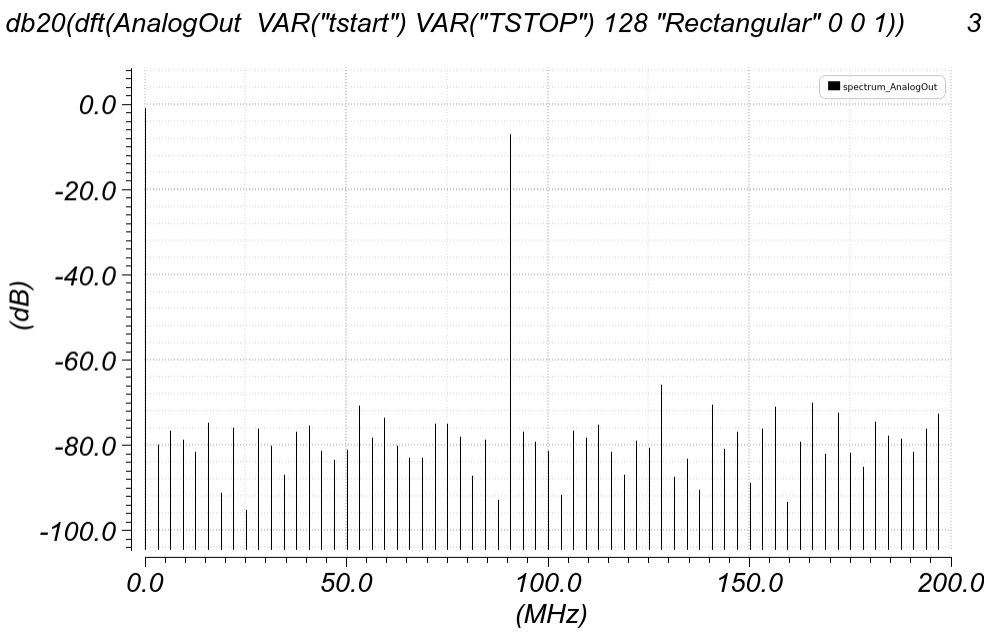

Figure 6.2: ADC Output Spectrum Measurement

be improved in future design revisions.

To evaluate the potential effects of DC mismatch, a calculation is performed to determine the noise contribution. As discussed above, the total power of the interleaving spurs is approximately equal to the variance of the DC offset voltage σ^2_{voff}. In the SAR ADC, the largest contributor to the DC offset is the comparator input offset voltage. Taking the standard deviation from the simulations performed earlier, we can compute the variance by simply squaring σ_{voff}.

$$\sigma^2_{voff} = (1.492mV)^2 = 2.23mV \tag{6.1}$$

Thus giving the total noise voltage as:

$$N_{spur} = \frac{2.23mV}{\sqrt{2}} = 1.58mv_{rms} \tag{6.2}$$

We can then compute the effect on the SINAD by:

$$N_{Total} = \sqrt{N_{Nominal,rms}^2 + N_{spur,rms}^2} \tag{6.3}$$

To compute the noise of the nominal ADC, the quantization noise is removed from the SINAD measurement.

$$N_{Nominal,rms} = \sqrt{SINAD_{Nominal,rms}^2 - N_{Quantization}^2} \tag{6.4}$$

$$N_{Nominal,rms} = \sqrt{866_{\mu vrms}^2 - 254_{\mu vrms}^2} = 828_{uVrms} \tag{6.5}$$

Therefore making the total noise:

$$N_{Total} = \sqrt{828_{uVrms}^2 + 1.58_{mVrms}^2} = 1.78_{mVrms} \tag{6.6}$$

Accounting for the DC mismatch between the sub-ADC's, the SINAD can then be computed:

$$SINAD_{Total,dB} = 20\log\left(\frac{Vin_{rms}}{N_{Total,rms}}\right) \tag{6.7}$$

$$SINAD_{Total,dB} = 20\log\left(\frac{318_{mVrms}}{1.78_{mVrms}}\right) = 45dB \tag{6.8}$$

The resulting ENOB drops to 7.18 bits. Without accounting for noise and mismatch in the sub-ADC, the SINAD is already greatly reduced. A realized design will require DC offset calibration for maximum performance.

CHAPTER 7: CONCLUSIONS

In this work, a time interleaved SAR ADC was designed utilizing the Cadence generic 45nm CMOS process. Though the design could still be improved, this architecture is shown to be a very viable choice in modern wireless systems. Even with larger 1.8v transistors, the design is still relatively small with an approximated area of 0.193 mm^2. The power consumption is 6.63 mW for each of the sub-ADC's, while the power consumption for the complete converter is 25.38 mW. As shown in figure 1, two ADC's are necessary in modern quadrature receivers, therefore doubling the required die area. Still, these converters show promise for use in mobile radio systems. Further evaluation must be performed by the radio system designer to ensure that the negative effects of time interleaving have minimal impact on the specific system. For example, radios using QAM modulation schemes have different requirements than those utilizing QPSK. Table 7.1 summarizes the performance of the converter. Table 7.2 highlights the performance of similar recent works. The Figure of Merit (FOM) is calculated using Walden's method [14]:

$$FOM = \frac{Power}{fs * 2^{ENOB}}[fJ/conversionStep] \tag{7.1}$$

Table 7.1: ADC Performance Summary

Parameter	**Value**	**Units**
Process	Cadence GPDK045	
Bits	10	Bits
Supply Voltage, VDD	1.8	V
Input Voltage Range	900	mVpp
Approx. Area (sub-ADC)	0.048	mm^2
Sample Rate (sub-ADC)	100	MSPS
SINAD (sub-ADC)	48	dB
ENOB (sub-ADC)	7.68	Bits
Power (sub-ADC)	6.33	mW
FOM (sub-ADC)	307	fJ/c.step
Approx. Area (4xTI)	0.193	mm^2
Sample Rate (4xTI)	400	MSPS
SINAD (4xTI)	45	dB
ENOB (4xTI)	7.18	Bits
Power (4xTI)	25.38	mW (avg)
FOM (4xTI)	438	fJ/c.step

Table 7.2: Relevant Works

Parameter	**[15]**	**[16]**	**Units**
Process	16	28	nm
Bits	10	10	Bit
Interleave Factor	4	8	x
Supply Voltage, VDD	0.8	0.9/1.0/1.8	V
Input Voltage Range	1.3	1.4	Vpp
Approx. Area	0.149	0.06	mm^2
Sample Rate	1.67	1.4	GSPS
SINAD	51.1	48.1	dB
ENOB	8.8	7.7	Bit
Power	7.9	24	mW
FOM	16	82.4	fJ/c.step

CHAPTER 8: FUTURE WORK

8.1 DAC Design Revisions

It is noted that the DAC performance hinders the overall ADC performance and should be improved. During revisions, some choices made in the design process can be changed to evaluate the effect on performance. For example: the unit capacitor size can be reduced to trade mismatch for speed. This may degrade the SINAD σ; however, the nominal SINAD should increase. This also has the potential to increase the 3σ SINAD, if the positive effect on the nominal SINAD is greater effects caused by increased mismatch. Additionally, an alternate CAPDAC topology may be considered. Evaluating current domain converters may see an improvement in speed and reduction in mismatch. These converters may also require less die area.

8.2 Calibration Techniques

This work largely ignored comparator offset calibration, which should really be considered in a time interleaved SAR design. Mismatch between each individual converter results in frequency domain spurs, which degrade the SINAD of the converter. With calibration, these effects can be mitigated to some extent, improving the performance and yield.

8.3 Interleaving Error Mitigation

In addition to the SINAD degradation imposed by the DC offset, further evaluation needs to be performed on additional sources of interleaving error. The sources of phase error such as timing and bandwidth differences need to be evaluated. Additionally, the gain differences between the sub-ADC's must be observed. With this information, the converters suitability for use in phase modulated radio systems can be evaluated.

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