# INVESTIGATIONS ON RESONANT GATE DRIVERS FOR POWER MOSFETS

by

Nazmus Sakib

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Approved by:

Dr. Madhav D. Manjrekar

Dr. Abasifreke Ebong

Dr. Badrul Chowdhury

Dr. Yesim Sireli

# ABSTRACT

NAZMUS SAKIB. Investigations on Resonant Gate Drivers for Power MOSFETs
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(Under the direction of DR. MADHAV D. MANJREKAR and DR. ABASIFREKE EBONG)

In recent years, Wide Bandgap (WBG) semiconductor based power devices such as Metal Oxide Semiconductor Field Effect Transistors (MOSFET) have matured rapidly and are playing a significant role in high switching frequency power electronic applications.WBG materials such as silicon carbide (SiC) and gallium nitride (GaN) possess a higher critical breakdown strength than silicon due to stronger atomic bond. It also shows greater thermal conductivity. Due to these properties, WBG semiconductors become a material of choice in different modern power electronic applications. In addition, using these devices result in the overall size reduction of the devices as higher doping levels can be achieved at similar voltage levels. A gate driver is an interface between the control signals and power devices. It plays a significant role in the switching behaviour of WBG devices. To increase the overall efficiency and reduce the footprint of the system high switching frequency operation of the devices is desirable. However, power consumption in the gate driving circuit increases with frequency. A viable strategy to reduce the gate driving power consumption is to use resonant gate driving technique where part of the energy stored in the gate capacitance is recycled. In this dissertation, a novel resonant gate driver (RGD) for WBG devices is proposed, designed and implemented which drives the semiconductor device using quasi-square wave by utilizing higher order harmonics. Firstly, the operating principles of the proposed gate driver circuit is presented. Secondly, a detailed characterization and analysis of power loss of the circuit are provided. Additionally, a comprehensive simulation study of the proposed circuit is introduced. Moreover, a prototype of the

proposed RGD was built and tested. Experimental results demonstrate that the proposed gate driving technique can significantly reduce power consumption in the gate driver circuit in comparison to conventional gate driving techniques.

# ACKNOWLEDGEMENTS

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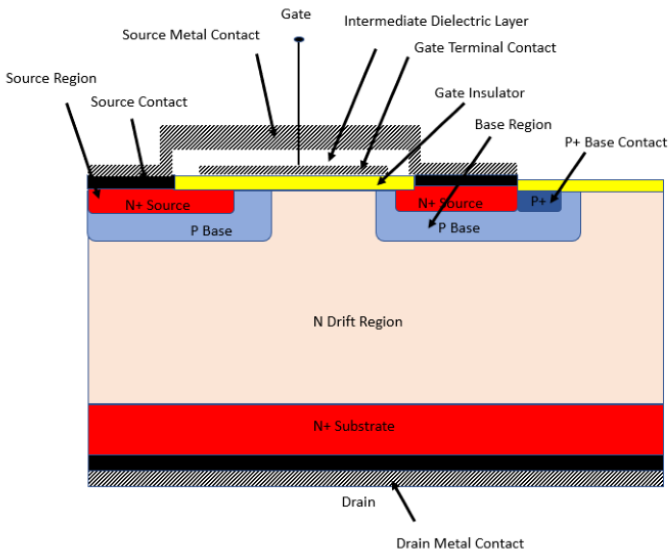
# CHAPTER 1: INTRODUCTION

## 1.1 Power MOSFET transistors Overview

Before the late 1970s, the only available nonlatching power switch was Bipolar Junction Transistor (BJT). Contrary to latching switches like thyristors which lose control of the gate once triggered into conducting state, BJT can be operated in it's on or off state by an input current at base [3]. However, power BJTs lack high speed operation ability, require high base drive currents and subject to thermal runaway and second breakdown. An alternative structure to BJT which has high speed switching capability, high input impedance and without thermal runaway problem is MOSFET [4]. As shown in 2.1(a), a power MOSFET has alternate p-type and n-type doping profile with vertical orientation [5]. This structure is termed as VDMOS or vertical diffused MOSFET. In this structure, the gate is built over the N- drift zone which enables better thermal resistance [6]. The structure is known as enhancement mode n-channel MOSFET. Fig. 2.1(b) shows a physical MOSFET device which has three terminals such as gate, source and drain. On the contrary, a p-channel MOSFET has the opposite doping profile. As shown in the figure, the end layers are labelled as source and drain. The doping of these two layers is large, around $10^{19}$ $cm^{-3}$. The middle layer is p-type where the channel is established and is known as body. The typical doping of this region is around $10^{16}$ $cm^{-3}$. The N- layer is the drift region and is typically doped at $10^{14}$ $cm^{-3}$ [5]. The breakdown voltage of the device mainly depends on this region. When a voltage is applied in gate, it becomes positive with respect to the source and the surface beneath it converts into n-type layer or channel, which connects the source and drain and allows the flow of current. Higher interconnected capacitance and bigger resistance for the gate access are two major drawbacks of this

structure [6]. Also, low channel mobility and high interface trap density are other two disadvantages. Due to this reason, the switching takes much longer time and the frequency performance of the MOSFET decreases.

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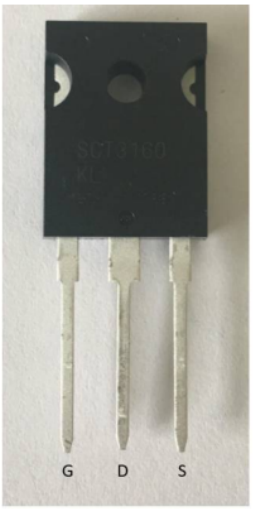



(b)

Figure 1.1: Power MOSFET (a) Device Architecture [2] (b) A photograph of a physical MOSFET from ROHM

A double trench structure is another structure is also useful for different applica-

tions where a trench gate is used. It has increased channel width and provides a higher channel mobility. Also, this structure has the ability to improve channel-resistance and epitaxial current uniformity [7]. For SiC the energy band gap is 3.2 to 3.4 eV as opposed to 1.12 eV in Si. A larger bandgap means less carrier generation in the depletion region which is favourable for reducing the leakage current.

## 1.2 MOSFET Switching

Wide Bandgap (WBG) based devices have unique electrical properties that make them attractive to various power electronic applications. MOSFET is a voltage controlled device. The switching characteristic of a MOSFET can be divided into four regions. In the first step, gate voltage starts to rise and pass the threshold voltage $V_{th}$. During this step a large gate current is supplied from the charge stored in the gate driver input capacitance. In next step, drain voltage remains at its highest level while the body diode is still not its blocking state. In the following stage drain current starts to fall and gate source voltage reaches its final value and the MOSFET becomes fully on.

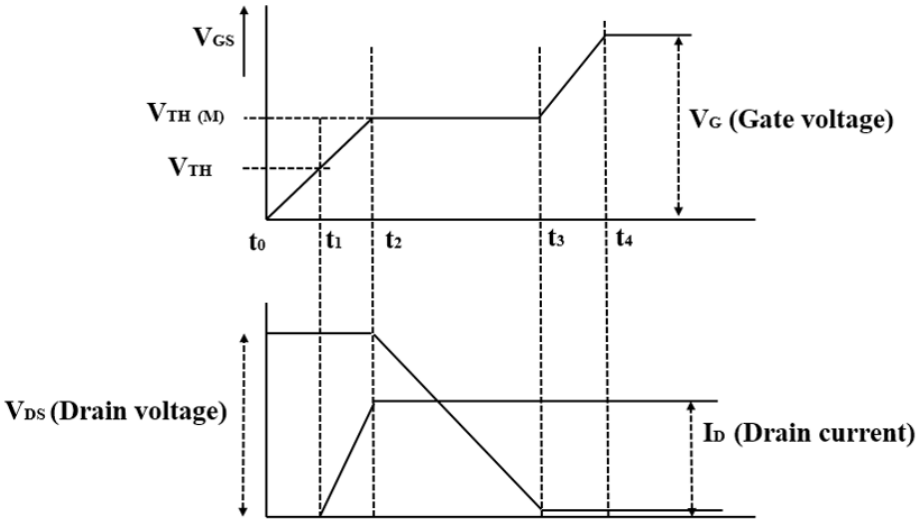



Figure 1.2: Switching waveforms for MOSFETs

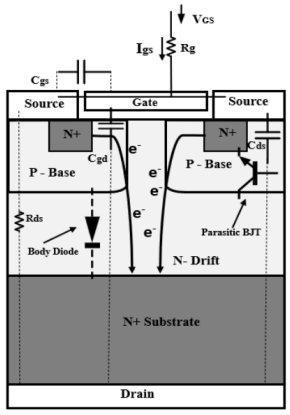
The critical parameters that impact the characteristic of a MOSFET switching

are gate resistance $R_g$, two capacitances gate-source capacitance $C_{gs}$ and gate-drain capacitance $C_{gd}$. Also the gate-source voltage $V_{gs}$ plays an important role. Two other important parameters are switching frequency $F_{sw}$ and on-resistance $R_{dson}$.

Gate power required to drive the MOSFET can be expressed as

$$P_{gate} = V_{gs} \times Q_g \times \frac{1}{T} \tag{1.1}$$

From (1.1) it is evident that the gate power requirement depends on the turn-on and turn-off time of the device. Faster switching time means less gate power requirement.

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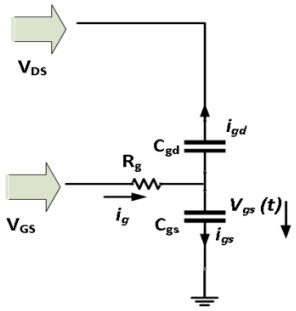
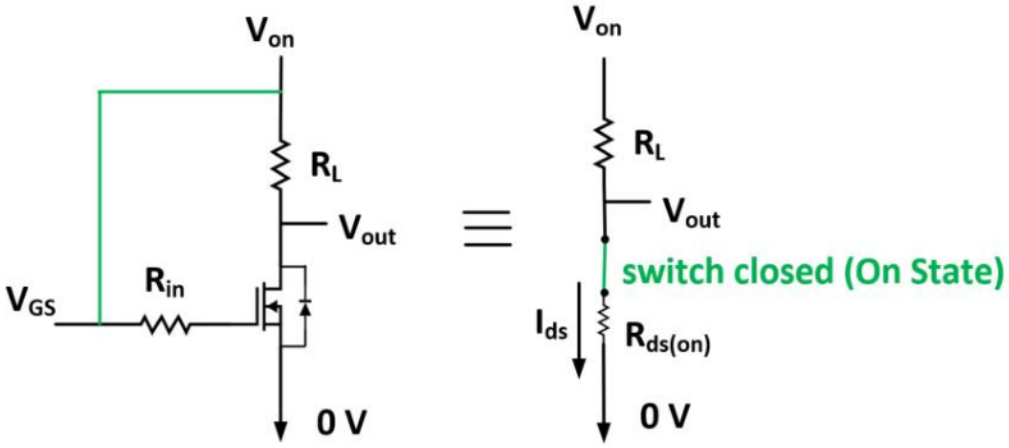



(b)

Figure 1.3: (a) Critical parameters at turn-on event of the MOSFET (b) Equivalent circuit structure of the MOSFET

As seen in Fig. 1.4, in the turn-on event the gate first connected to $V_{on}$. When the gate-source voltage is greater than the threshold voltage level $V_{th}$, the MOSFET starts to conduct. In between source and drain a channel is formed and the drain to source current $I_{ds}$ starts to flow. At this state the MOSFET becomes on and it operates as a low resistance switch.

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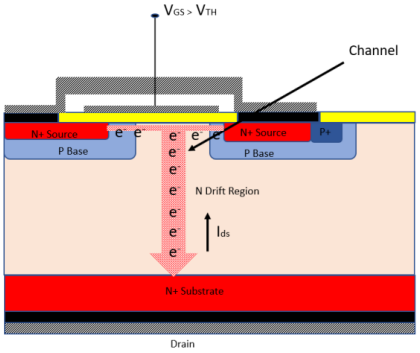
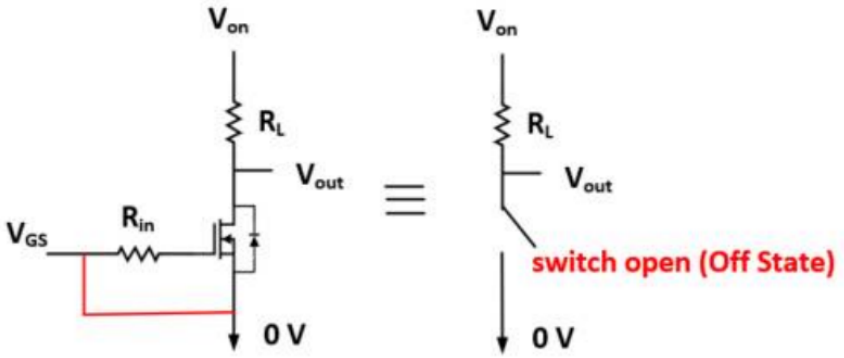



(b)

Figure 1.4: MOSFET turn-on event (a) equivalent circuit (b) MOSFET device in an turn-on event

As seen in Fig. 1.4, in the turn-on event the gate first connected to ground or zero potential. In this case the gate-source voltage drops below the threshold voltage level

$V_{th}$ and the MOSFET ceases to conduct. No drain to source current $I_{ds}$ flows. In this state the MOSFET becomes off and it operates as a very high resistance switch.

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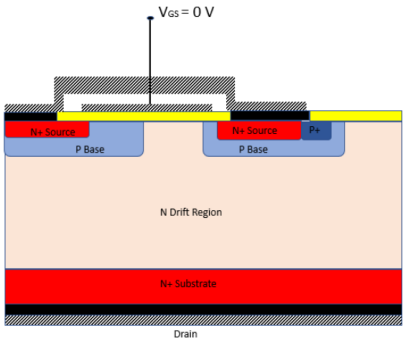


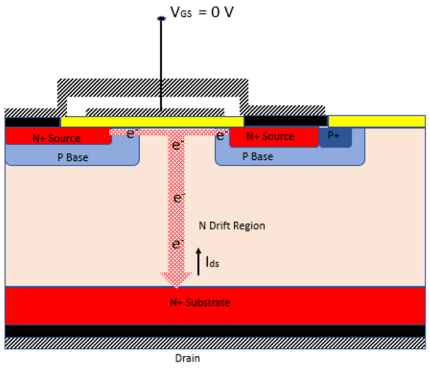

(b)

Figure 1.5: MOSFET turn-off event (a) equivalent circuit (b) MOSFET device in an turn-off event

## 1.3 Motivation of the research

In power electronics, most load circuits are inductive in nature. In inductive switching conditions, when the switch turned off some charges are still present in the channel and a drain to surce current flows in the channel which contributes to the gate power loss. In the case of high speed switching, this loss could be very significant. One way to solve this issue is to apply a small negative gate source voltage in the off state.

This eventually leads to the full turn-off of the MOSFET. Normally, conventional gate drives can only provide unipolar gate voltages which leads to power loss in the gate circuit. In this research resonant gate driving technique is used to generate unequal gate voltage levels to reduce the power loss.

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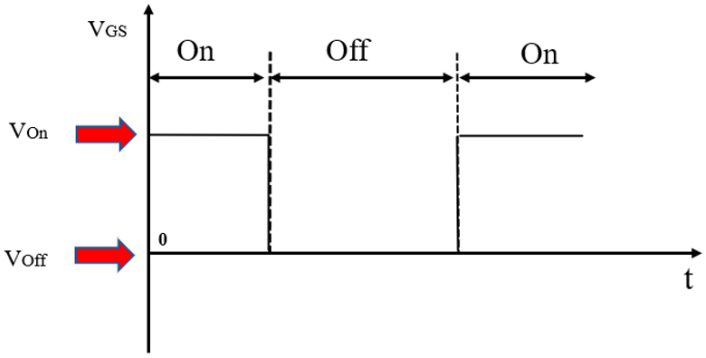


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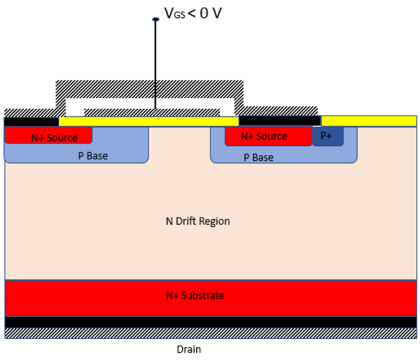
Figure 1.6: (a) At zero voltage MOSFET is not properly turned-off (b) CGD gate-source voltage

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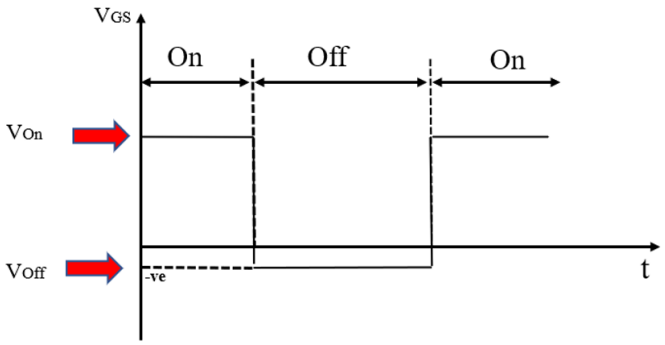



(b)

Figure 1.7: (a) A negative gate voltage turns-off the MOSFET properly (b) Desired gate-source voltage

## 1.4 Gate Driver

A gate drive acts as an intermediate layer which accepts low level signals from controls and amplify the signal to match the requirement of turning on or turning off of a device. The main requirement of a basic gate drive circuit is to be able to supply a sufficiently high voltage to turn on the device. The turn-on operation in a MOSFET normally depends on its gate capacitance in the input terminal. The gate driver needs to supply sufficient charge in the input capacitance and in the turn-off sequence should remove the charge quicky without incurring much loss.

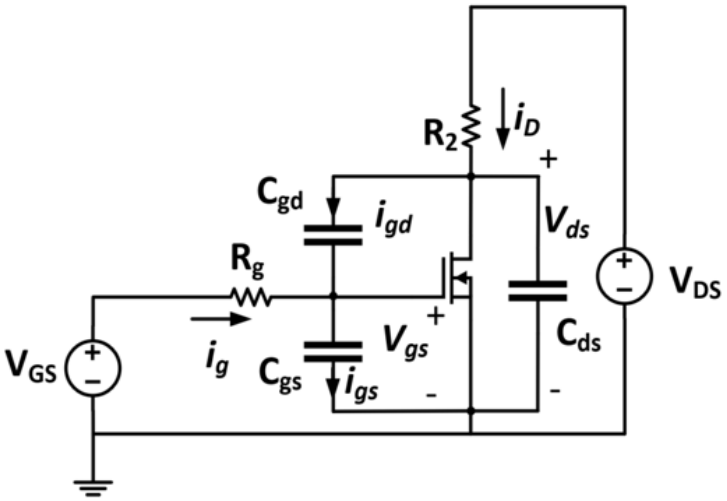
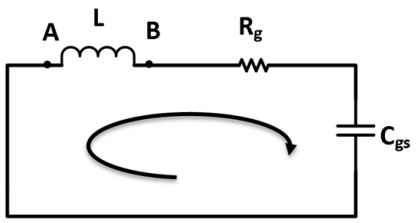



Figure 1.8: A conventional gate drive circuit (CGD) for MOSFET

## 1.5 Resonant Gate Driver

Resonant gate driver is a gate driving technique using LC circuit which is used to recycle and recover part of the dissipated energy in the gate resistance. In the circuit, an inductor is used as a current source to charge and discharge the gate capacitance. As shown in 1.9(a) the transfer of energy can be controlled by using the switching components at the terminals A and B. When the operating switching frequency is very high this technique is very useful to reduce the overall power consumption in the gate drive circuit. Fig. 1.10 shows the resonating inductor connection in series and parallel combinations. The series combination is suitable to drive voltage based devices as this structure provide more control over the voltage of the circuit. On the overhand the current control can be achieved for the parallel architecture. These structures are particularly suitable for RF circuits.

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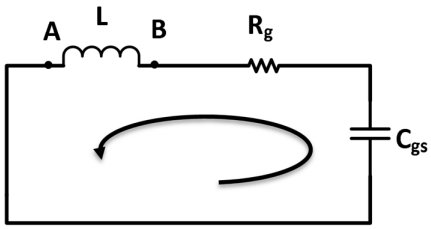


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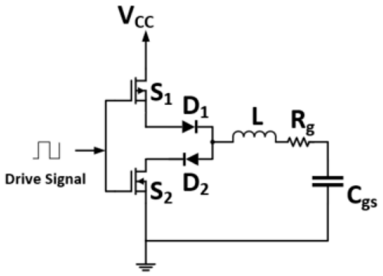
Figure 1.9: (a) RGD equivalent circuit at turn-on transition (b) RGD equivalent circuit at turn-off transition

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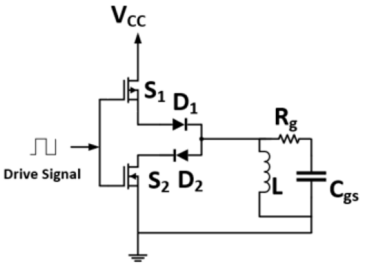



(b)

Figure 1.10: Examples of simple RGD circuits (a) Inductor in series with $C_{gs}$ (b) Inductor in parallel with $C_{gs}$

## 1.6 Outline of the Dissertation

This dissertation is outlined as the following.

Chapter 1: Introduction

Chapter 2: An Overview of Advances in High Reliability Gate Driving Mechanisms for SiC MOSFETs.

Chapter 3: A New Multiresonant Gate Driver Circuit for SiC MOSFETs.

Chapter 4: A High-Performance Resonant Gate Driver Circuit for GaN MOSFETs.

Chapter 5: Conclusion and Future Work

# CHAPTER 2: An Overview of Advances in High Reliability Gate Driving Mechanisms for SiC MOSFETs

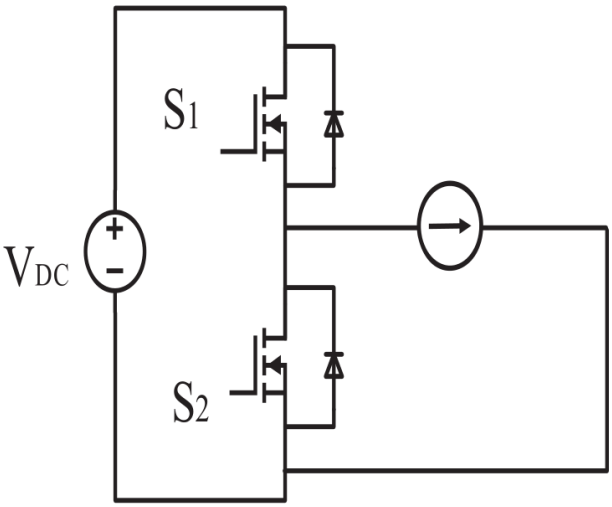
## 2.1 Abstract

SiC power devices exhibit low on-resistance and are capable of processing high switching frequencies at elevated temperatures. When SiC MOSFETs are employed as switch, minimizing switching power losses is crucial. A proper design of gate driving circuit for SiC MOSFET can ensure minimum losses, safe operation of the device and reliable performance. A comparative study of gate drivers for SiC MOSFETs in current literature is presented in this paper.

## 2.2 Introduction

Recently, silicon carbide (SiC) power devices have been established as a promising alternative to silicon based devices in wide range of power electronics applications [8]. SiC power devices feature low on-resistance, high blocking voltage, high switching frequency and high operational temperature [9]. SiC MOSFETs also provide significant improvement in power density for a typical bridge-leg converter configuration [10]. A representative bridge-leg consisting of two SiC MOSFETs as switching devices ($S_1$ and $S_2$ ) with their anti-parallel diodes drawing energy from a DC link and supplying a constant AC current load is shown in 2.1(a). The device under study ($S_2$) is driven by classical gate drive circuit as shown in 2.1(b) and produces switching waveforms as shown in 2.2(a) . When MOSFETs operate as switches, equivalent capacitances in the semiconductor region as shown in 2.2(b) play a significant role. The rate of changes of voltages across the capacitors specify the overall switching performance of these MOSFETs. The equivalent MOSFET model including the three capacitances

connected between the three terminals of the device is shown in 2.3.

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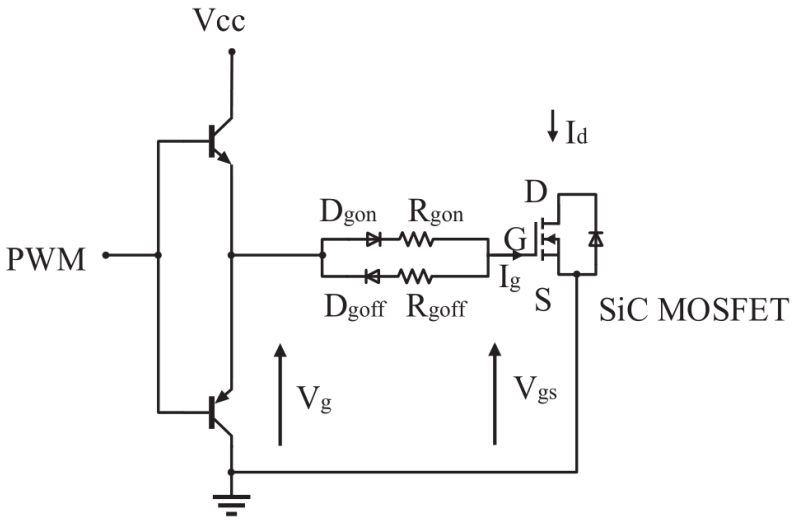


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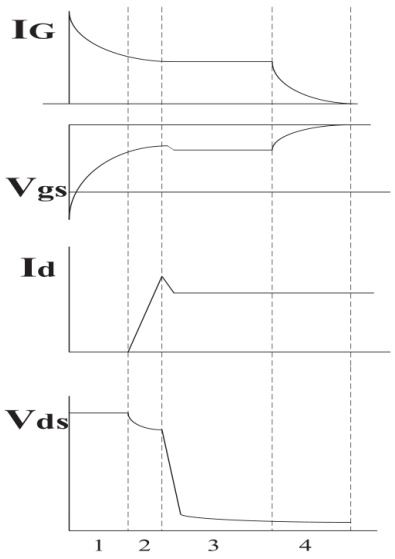
Figure 2.1: (a) Bridge-leg Configuration (b) Classical Gate Drive

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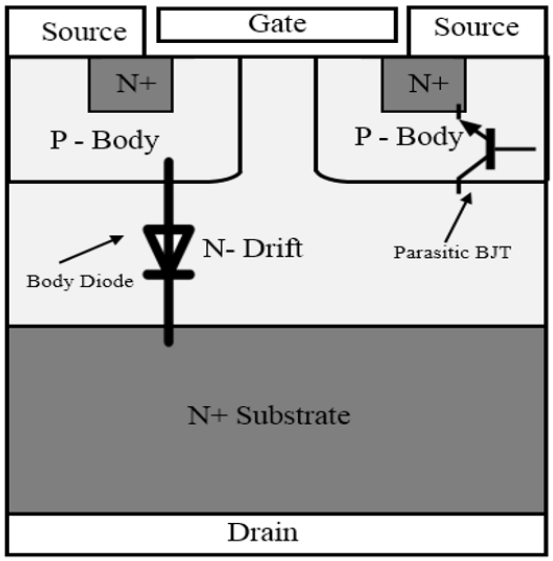



(b)

Figure 2.2: (a) Traditional MOSFET switching waveform (b) MOSFET device architecture

A switching event of the MOSFET can be divided into four intervals as shown in 2.2(a). In the first step, input capacitance starts to build up the charge . A small current is charging the $C_{gs}$ capacitance and current starts to flow in the capacitance. The time interval between this conduction and the beginning of gate pulse is known

as turn-on delay as both the drain current and drain voltage remain unchanged. In the next step, the gate voltage rises from threshold level to a steady level where the current in the device is proportional to the gate voltage. In this stage, the drain-to-source voltage stays at the previous level, however drain current starts to build up. The drain-to-source voltage starts to fall slowly and all the current is transferred into the MOSFET. Discharge of capacitance $C_{gd}$ happens due to rapid voltage change in drain- to-source terminals. During this process, the drain voltage starts to fall. At this time, the gate-to-source voltage stays unchanged. Also the drain current remains unchanged. In the

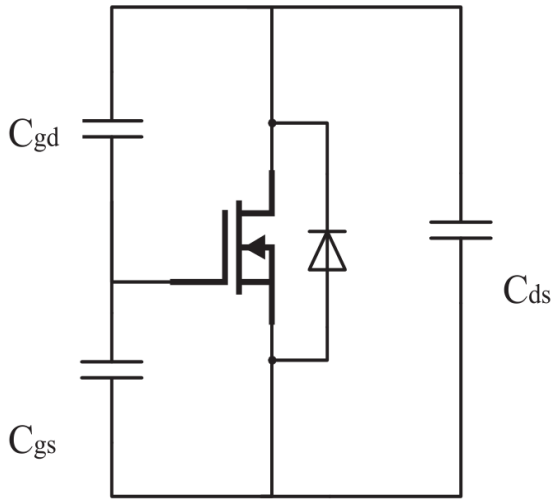



Figure 2.3: Schematic diagram of a MOSFET.

last step, by applying a higher gate voltage, the MOSFET becomes fully on. Gate-to-source voltage reaches its final value. The final on-resistance of the device is determined by the gate-to-source voltage. Both the capacitances $C_{gs}$ and $C_{gd}$ get charged and the current is shared by them. However, the drain current still remains unchanged and the drain-to-source voltage and the on-resistance are reduced. In bridge-leg configuration as shown in 2.1(a), faults can happen due to the decrease in gate-source voltage level. Eventually, $S_2$ can be turned on when it should remain

off [11] A classical gate drive circuit has detectors of gate-to-source voltage to detect switching performance, but it lacks an optimized method to address faults in case of switching noises such as overshoot of voltage and current, oscillation, and fast switching transients [12] Gate driving mechanisms proposed in recent literature focus mainly on addressing issues related to switching noises with optimized performance of the device. This paper presents comparison of various gate driving mechanisms employed to optimize the switching performance of SiC MOSFETs.

## 2.3 Review of Gate Driving Mechanisms

In recent years, different gate driving methodologies for SiC MOSFETs have been reported in the literature [12, 13, 14, 15, 16] When employed in a bridge-leg configuration, existing gate driving techniques primarily focus on two important design aspects. The first one is to provide negative gate voltage in order to guarantee fast turn-off of the switch. The second focus is to mitigate negative gate-source voltage spikes when the complementary MOSFET is turned off [12, 13] Four alternating gate driving mechanisms addressing these two aspects are discussed below.

### 2.3.1 Passively Triggered Gate Drive

SiC MOSFETs can work on high switching frequency with high blocking voltage. However, operating at high switching speed, parasitic components influence the performance of the device and may produce spikes during switching transients. The gate driver proposed in reference [12] is able to generate the required negative gate voltage and eliminate the negative gate-to-source voltage spikes. This is shown in 2.4. Firstly, to generate a negative gate voltage and to speed up the

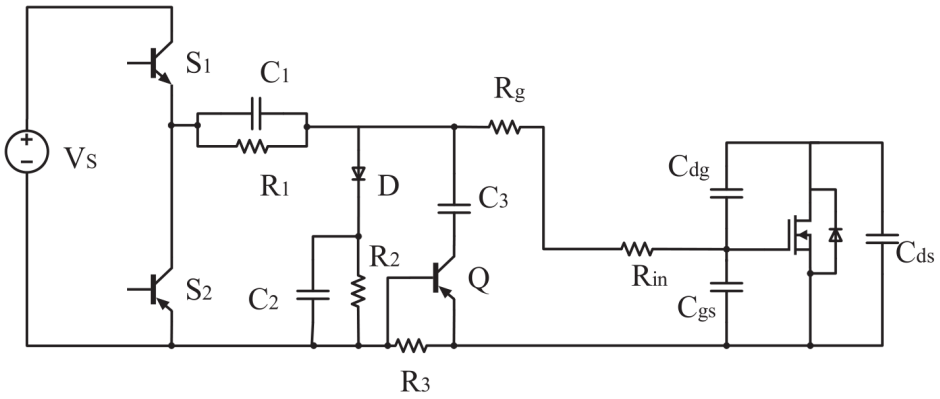



Figure 2.4: A Passively Triggered Gate Drive

turning-off transient, a series divider with resistors $R_1$ and $R_2$ is used. Two capacitors $C_1$ and $C_2$ are employed to attain a steady state gate-to-source voltage. The diode D is used to prevent the current going back to the circuit. The main function of this topology is that it offers another small impedance loop when the negative gate-to-source voltage spike occurs. Another important feature of this circuit is to suppress negative gate voltage spikes with the help of resistor $R_3$ , capacitor $C_3$ and the transistor Q. The small impedance loop for negative gate voltage source is achieved as well with the help of these additional components.

### 2.3.2 Negative Spike Mitigation

The proposed gate driver circuit in reference [12] consists of three resistors $R_1$ , $R_2$ and $R_3$ , two capacitors $C_1$ and $C_2$ , one diode D and a PNP transistor. The capacitor $C_1$ is used to attain steady-state values of negative gate-to-source voltage. Here, $C_1$ is large enough to keep the voltage almost constant. If a negative gate-source voltage spike occurs, a small impedance loop is created by capacitor $C_2$ which is in series with a PNP transistor Q. Resistor $R_3$ controls the transistor passively and when the positive spike happens, the diode D

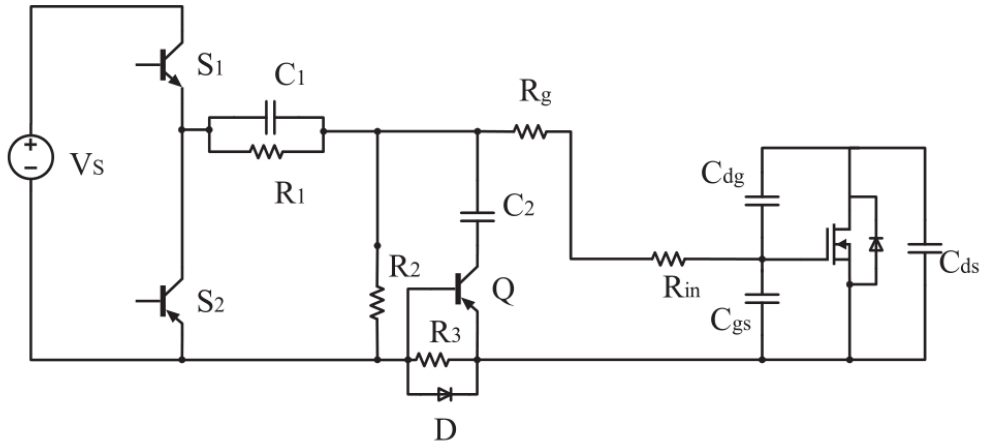



Figure 2.5: Negative Spike Mitigation Gate Drive.

can eliminate adverse effects on positive gate-to-source voltage spikes. Here the auxiliary transistor will connect a series capacitor into the gate circuit to suppress the negative gate voltage spikes. Moreover, this transistor is controlled passively. By employing an RC level shifter, the proposed gate driver can reduce the magnitude of positive gate voltage spikes as well.

### 2.3.3 Crosstalk Prevention

When switching speed is high, due to a smaller gate capacitance, SiC MOSFET switch which is employed in a bridge-leg configuration can get spurious gate voltage. This phenomenon is known as crosstalk. The proposed gate driver in [15] which is shown in 2.6 addresses this issue. The isolation between drive signal and the power MOSFET is achieved by the transformer T and the blocking capacitor $C_b$ . First, a negative voltage clamp circuit which consists of two capacitors, $C_1$ and $C_2$ , two resistors, $R_1$ and $R_2$ and one clamp diode D is used to turn off the SiC MOSFET with negative voltage. Second, the duty ratio compensation circuit, which comprise two series connected transformers $T_M$

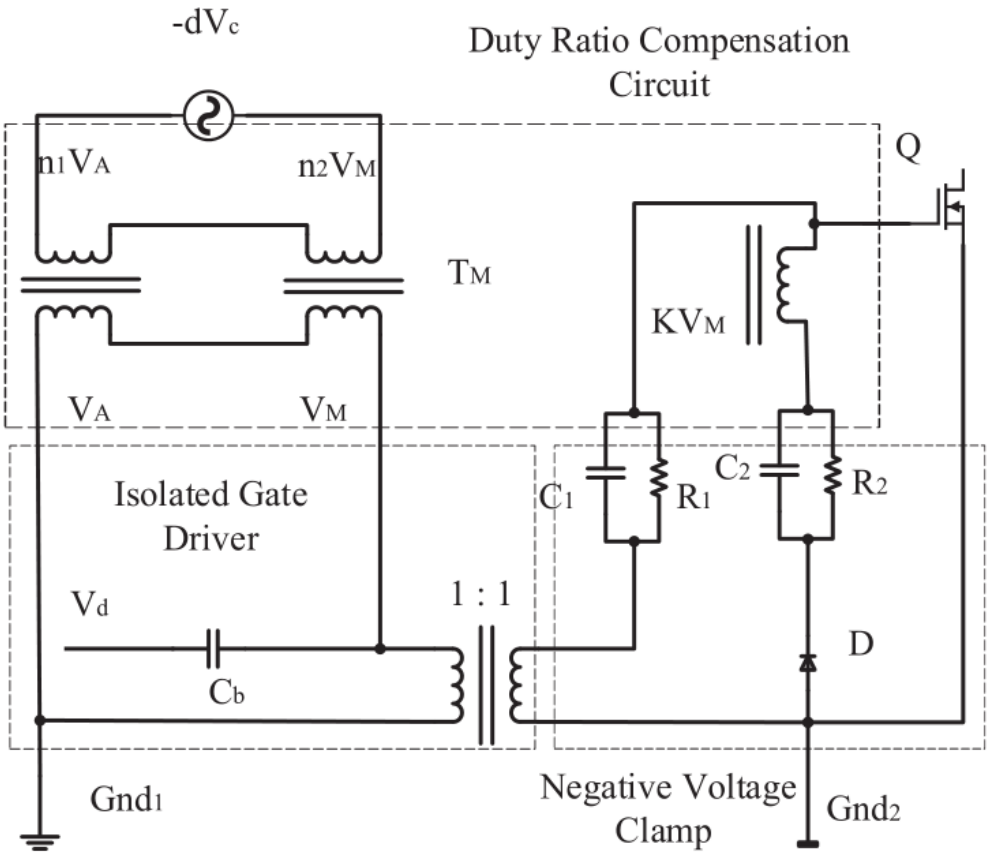



Figure 2.6: Gate Drive with Constant Negative Voltage

and $T_A$ . The purpose of this circuit is to keep the negative voltage constant even when duty ratio varies. The auxiliary voltage source $dV_c$ is directly connected to the series connected transformers and is easily controllable. The variable negative voltage is compensated by the voltage source and when duty ratio changes, the negative voltage also get altered.

### 2.3.4 Resonance and Clamping

A resonant gate drive is proposed in [16] as shown in 2.7. This circuit topology gives reliable performance of switches with reduced power consumption. The switching transition in this circuit is divided into two parts. They are resonance and clamping. Some energy can be recovered by utilizing the principle of resonance which ultimately reduces overall switching power requirement.

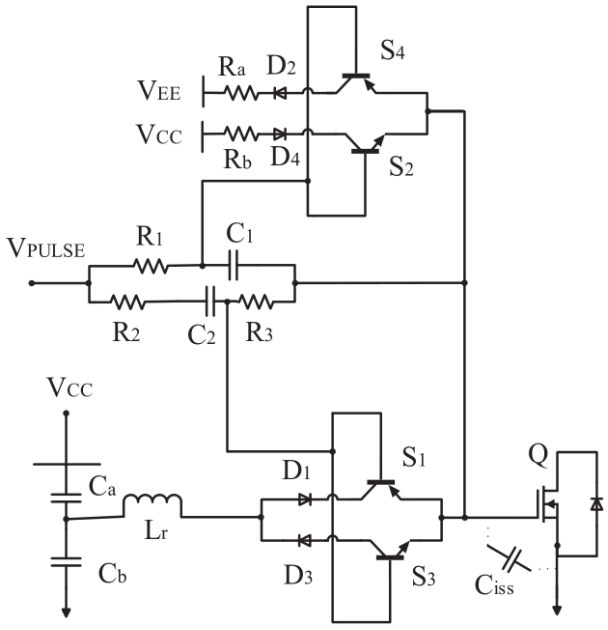



Figure 2.7: A Resonant Gate Drive

First, the small signal BJT, $S_1$ is turned on. Energy starts to transfer between capacitor $C_b$ which is at 7.5 V, $L_r$ , and $C_{iss}$ resulting in voltage transitions from 5 V to +20 V. In practice, however, the gate voltage is less than 20 V, because of the energy losses due to parasitic resistance. This loss can be compensated by clamping the gate source terminals after switching transition, which is achieved by turning off $S_1$ and turning on $S_2$ . The energy needed $g_1$ is supplied by $V_{cc}$ . After charging is finished, $V_{gs}$ is clamped to 20 V through $R_b$ , $D_2$ , and $S_2$ . Both Turn-on transition and turn-off transition are similar.

## 2.4 Comparative Evaluations of Gate Driving Mechanisms

In recent years, different gate driving mechanisms, which address a multitude of design challenges, and novel concepts to suppress false triggers of SiC MOSFETs are investigated. Table 2.1 presents a comparative evaluation of four gate drivers from latest literature.

As seen from Table 2.1, the gate driver in Fig. 2.4 has least negative voltage spike.

However, it has higher turn-on delay time than the gate driver in Fig. 2.5 and Fig. 2.6. Also, its turn-off delay time is significantly higher than the gate driver in Fig. 2.5. Gate driver in Fig. 2.6 has the most turn-on and turn-off time.

Table 2.1: Comparison Between Different Gate Drivers

| Parameters | Fig. 2.4 | Fig. 2.5 | Fig. 2.6 | Fig. 2.7 |
|---|---|---|---|---|
| Turn-on delay time | 107 ns | 35 ns | 700 ns | 120 ns |
| Turn-on time | 52.4 ns | 55.6 ns | 207 ns | 60 ns |
| Positive spike | -1.5 V | -2.0 | -10 V | -1.5 V |
| Negative spike | -7.25 V | -6.7 V | -20 V | 6.5 V |
| Turn-off delay time | 52.4 ns | 29.4 ns | 650 ns | 65 ns |
| Turn-off time | 44.4 ns | 93.8 ns | 193 ns | 50 ns |
| Complexity | Normal | Normal | Complex | Complex |

Also, this circuit topology is more complex than the other gate drivers. Even though gate driver in Fig. 3 has lower turn-on delay time and turn-off delay time, it has significantly higher turn-off time than the gate driver in Fig. 2 and Fig. 5. From these four methods, it is observed that the gate driver which gives best performance on negative voltage spike has comparatively longer turn-on delay time.

## 2.5 Conclusions

This paper has presented an overview and a comparative study of state-of-the-art gate driving mechanisms for SiC MOSFETs. For high switching frequency and high voltage conditions, SiC MOSFETs have low on-state resistance and provide significant improvement in power density. The highly reliable gate drivers are capable of suppressing negative gate voltage spikes. However, with high complex circuitry employed to achieve this objective might slow down the overall switching speed.

# CHAPTER 3: A New Multiresonant Gate Driver Circuit for SiC MOSFETs

## 3.1 Abstract

This paper proposes design and implementation of a new multiresonant gate driver circuit for silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs). The proposed gate driver circuit consumes less power than a conventional gate driver circuit (CGD) at high switching frequency applications. Power consumption in the gate driver circuit is proportional to the operating switching frequency and is significant in higher switching frequency applications. A CGD circuit can provide unipolar gate pulses and all the energy provided to the gate driver is dissipated in the gate resistance. A resonant circuit can be used to recycle part of the energy stored in the gate capacitance and reduce the overall power consumption by the gate driver. For efficient operation of the MOSFET, it is desirable to provide unequal voltage levels during switching operation. In this study, a novel gate driving circuit is presented which provides unequal voltage levels with clamping functionality utilizing higher order harmonics. A detailed analysis of the gate driving power loss is provided. In addition, detailed design procedure, and experimental verification are presented. According to the experimental results, the proposed gate driver can reduce upto 65% of the gate driver power consumption compared to a CGD circuit.

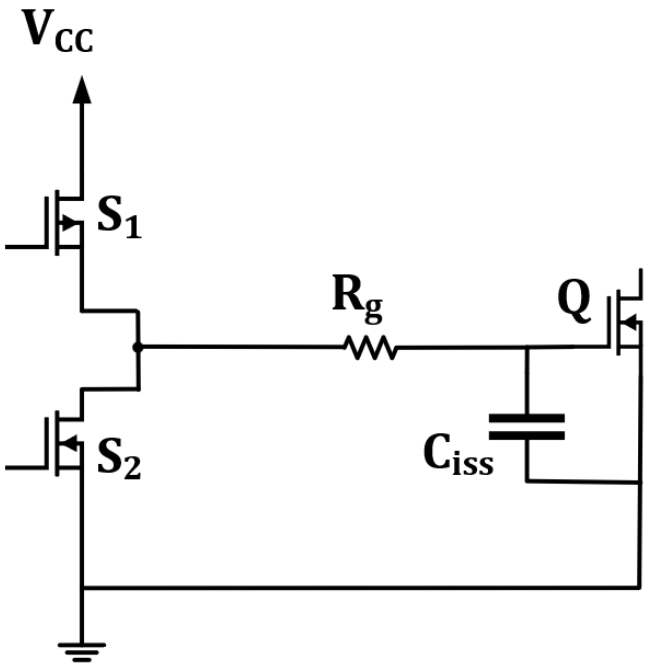
## 3.2 Introduction

In recent years, wide band gap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN) based power devices are playing a significant role in high switching frequency power electronic applications due to their superior characteristics than conventional silicon (Si) based devices.[17, 1, 18]. High speed switching operations

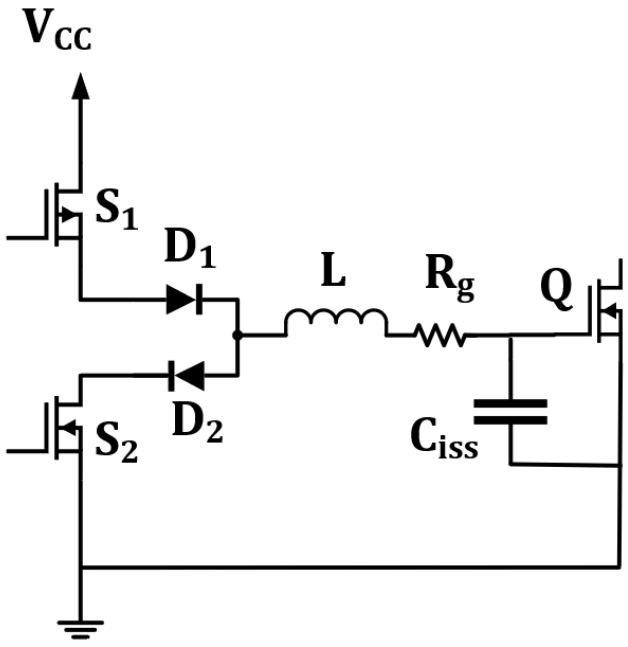
of power converters is advantageous to achieve better power density, compact design and better transient response of the system [19] . With the advancement of WBG materials and related technologies, SiC MOSFETs exhibit low on-state resistance than siliocn MOSFETs [20]. Hence, state-of-the-art converters using SiC MOSFETs are capable of operating at high switching frequencies with better efficiency and reduced losses. [18, 1, 21, 22]. A conventional gate driving circuit supplies energy to the input capacitance of the device in order to turn it on. During the turn on stage gate current charges input capacitance $C_{iss}$ and the MOSFET channel becomes fully enhanced. During the turn-off stage the energy is removed from the capacitance and channel becomes open. Fig. 3.1(a) shows a conventional gate driver circuit. Two MOSFETs $S_1$ and $S_2$ and dc power supply $V_{cc}$ are used to drive the MOSFET $Q$ through the gate resistor $R_g$. For a CGD circuit power consumed for the driving operation can be expressed as

$$P_{gate} = f_s V_{cc} Q_g \tag{3.1}$$

where $f_s$ is the switching frequency, $V_{cc}$ is the supply voltage, and $Q_g$ is the total gate charge of the MOSFET. According to eq:1, in high switching frequency applications power consumption in the gate driver circuit will be significant. A common strategy to reduce the gate driving power consumption is to use resonant gate driving technique [1, 23, 24, 25] Fig. 3.1 shows a common resonant gate driver circuit. In this circuit an additional resonant inductor $L$ is inserted. The resonating inductor $L$ is in series with the MOSFET $Q$ which resonates with $C_{iss}$ and reduce the energy dissipated in the gate resistor $R_g$.




(a)




(b)

Figure 3.1: (a) Conventional Gate Drive (b) Resonant Gate Drive

## 3.3 Literature Survey

The advancement of SiC and GaN power devices allows power converters to switch at higher frequencies for higher power density applications with more efficiency. However, at high frequency applications the gate power requirement can be significantly higher as power loss increases with switching frequency. Resonant gate driving is a conventional technique to reduce the power consumption in the gate driver by recycling energy stored in the gate capacitance. One of the earliest gate driver using resonant techniques was proposed in [26] to reduce power consumption in gate drive circuit. A resonating inductor is used in series with the MOSFET which resonates with gate capacitance and reduce the energy dissipation. This technique enables fast charging and discharging of the MOSFET and increases the overall driving speed. However, one drawback of this technique is voltage swing across the input capacitance during resonance is difficult to control and independent of any variations in the gate power supply. One common way to resolve this issue as proposed in [25] is to use extra clamping devices at the end of resonant period. This RGD circuit utilizes clamping diode to clamp gate source voltage to $V_{cc}$. The RGD circuits in [27] and [28] utilize a similar clamping functionality using body diodes of the MOSFET switches as the clamping device to reduce the overall power consumption . However, a disadvantage of this technique is for high switching frequency significant power loss can occur as SiC based devices exhibit a reduction in threshold voltage level in the blocking state. Therefore, a negative voltage in the gate source terminal is required in the turn-off stage of the switching process [29]. In [30] and [31] four MOSFET switches are used to provide gate voltage transitions between two equal voltage levels. However, in practice, the input capacitance of the MOSFET is charged at a higher gate voltage than when it is discharged through the gate resistor. So in the charging phase more energy is needed than in the discharging phase[32]. RGD circuits proposed in [33, 17, 34] utilizes bipolar voltage with unequal voltage levels to decrease the overall

power consumption.

To improve efficiency in the driver circuit, RGD circuits proposed in [35] and [36] utilizes self oscillation technique. A passive network is added in the gate terminal to achieve self sustain oscillation. However, a disadvantage of this technique is a repetitive adjustments of the phase shifting feedback network is necessary in each switching instant which makes the circuit regulation more difficult.

In [1], a multiresonant gate driver technique is proposed where the MOSFET is driven by a qausi-square wave. The waveform is generated using harmonics of a square wave. However, a limitation of this technique is the energy lost during the recycling stage due to the presence of parasitic resistances or inductances and the voltage drops across the device junctions cannot be recovered. Therefore, $V_{gs}$ can drop below the desired voltage level and constitute more energy losses. A more efficient way is to clamp $V_{gs}$ at the desired unequal voltage levels after the resonant stage is over.

In this article, a new multiresonant gate driver for SiC MOSFETs using higher order harmonics which provide clamping functionality at the desired unequal voltage levels of +15 V and -5 V is proposed. In section III, operating principles and characteristics of the resonant gate driver are presented. A detailed analysis of the power consumption of the gate driver circuit is presented in section IV. In Section V, experimental results are presented and section VI concludes the paper.

## 3.4 Proposed Resonant Gate Driver Circuit

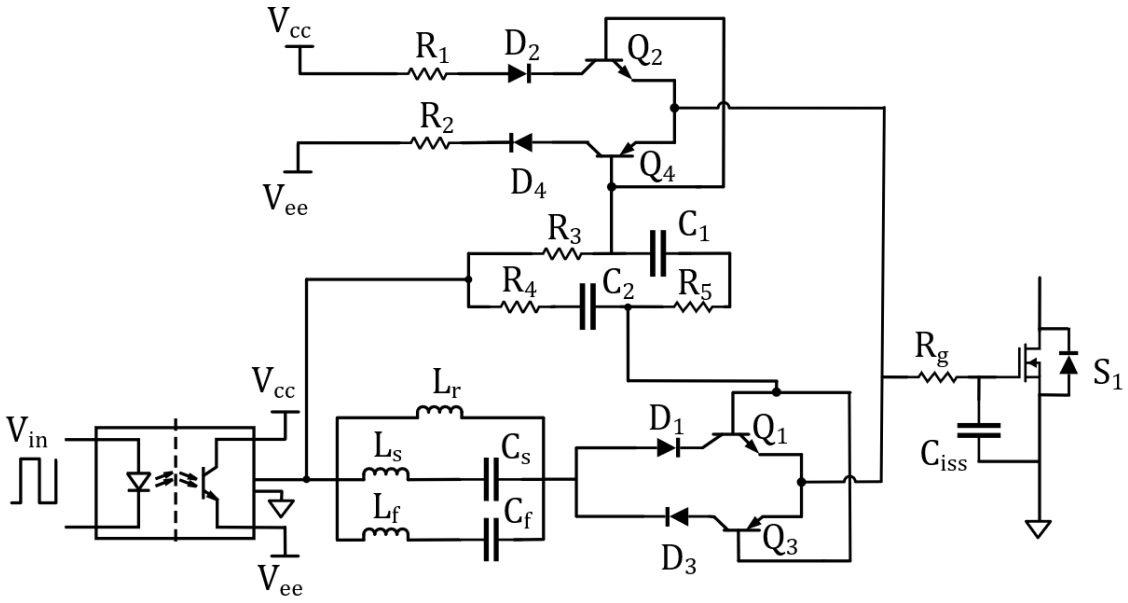



Figure 3.2: Proposed resonant gate driver circuit

The proposed resonant gate driver circuit is illustrated in Fig. 3.2. The resonant elements $L_r$, $L_s$, $C_s$, $L_f$, and $C_f$ form a multiresonant network which acts as filters for the fundamental, third and fifth harmonic components of the square wave and produce a quasi-square wave in the gate terminal of the MOSFET $S_1$. $R_1$, $D_2$ and $Q_2$ are used for clamping functionality during the turn-on stage and $R_2$, $D_4$ and $Q_4$ are used during the turn-off stage. An optocoupler is used to generate a square wave signal.

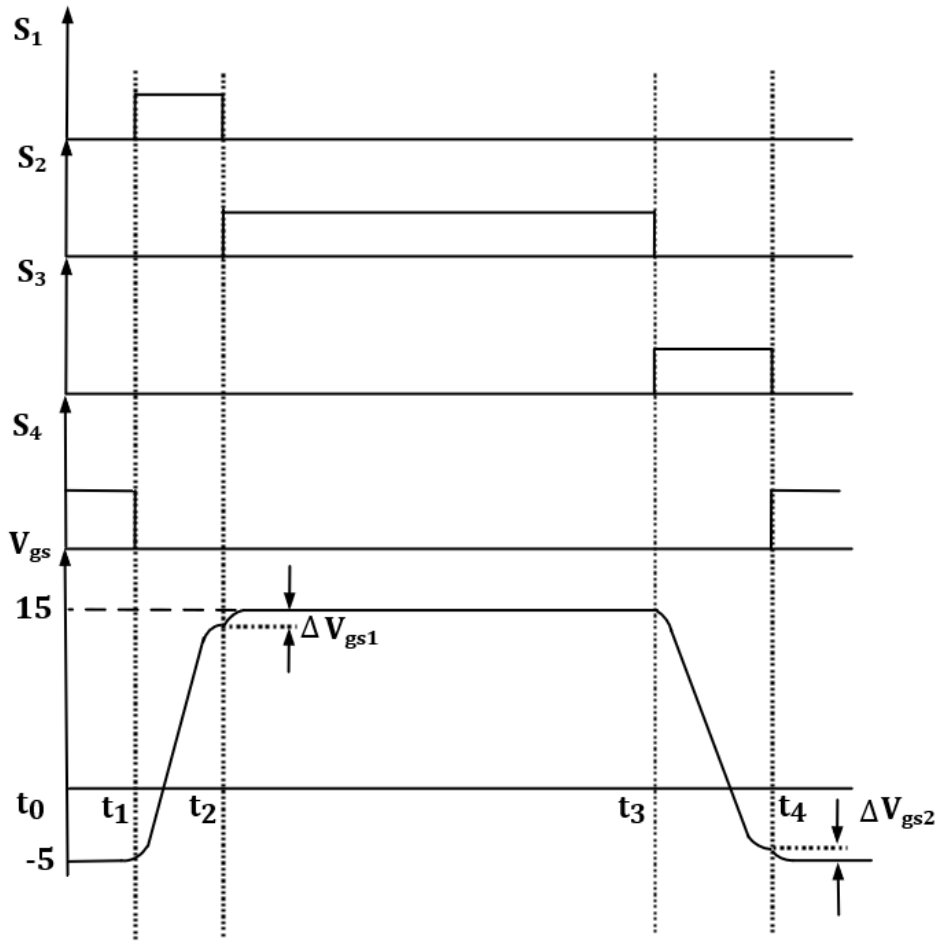



Figure 3.3: Operating waveforms of the proposed resonant gate driver

### 3.4.1 Operation Principle

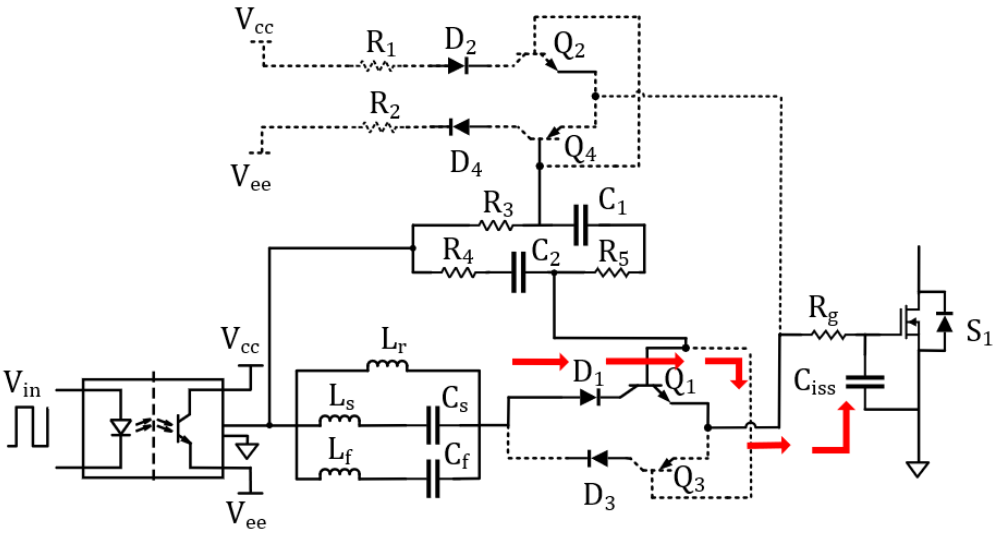
The key waveforms of the RGD circuit is depicted the equivalent circuits of the different steps are shown in Figure. In each switching cycle the gate driver circuit has four steps.

1. *Step 1 $[t_0 - t_1]$:* At time $t_1$, by switching $Q_1$, the turn-on transition is initiated. This enables energy transfer between resonant network and $C_{iss}$. Voltage at $C_{iss}$ starts to transitioning from -5 V to 15 V. All the other switches are remained off at this stage.

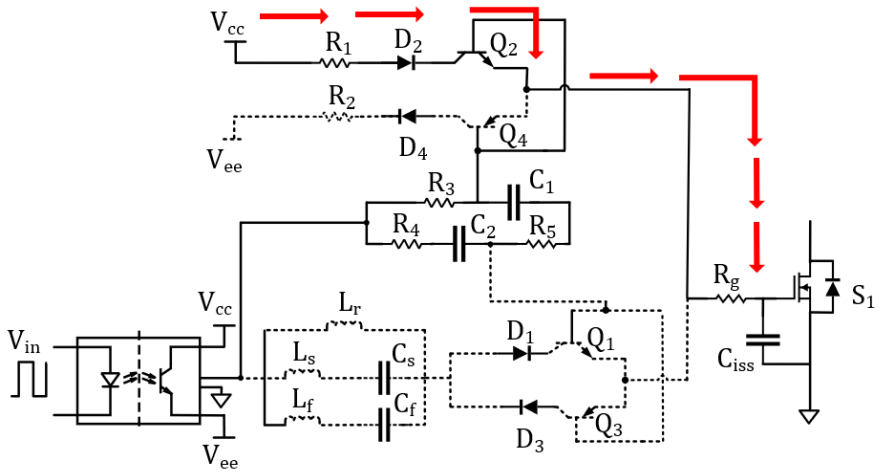
2. *Step 2 $[t_1 - t_2]$:* Normally, as shown in Fig, due to the presence of parasitic

elements in the circuit, voltage drops below the desired level. At time $t_2$, switch $Q_2$ is turned on and $v_{gs}$ is clamped to desired 15 V.

3. *Step 3 $[t_2 - t_3]$:* Switch $Q_3$ is turned on and initiates the turn-off stage of the MOSFET. Energy transfer starts from $C_{iss}$ to the resonant network and Charge in $C_{iss}$ starts to decrease.

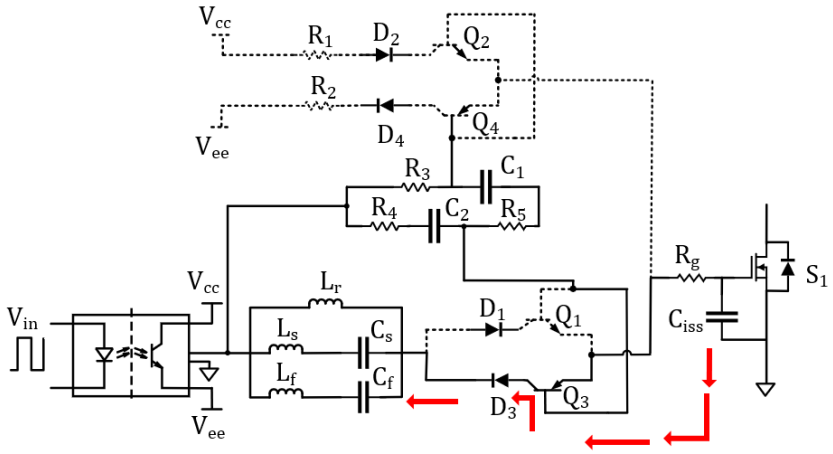



(a)

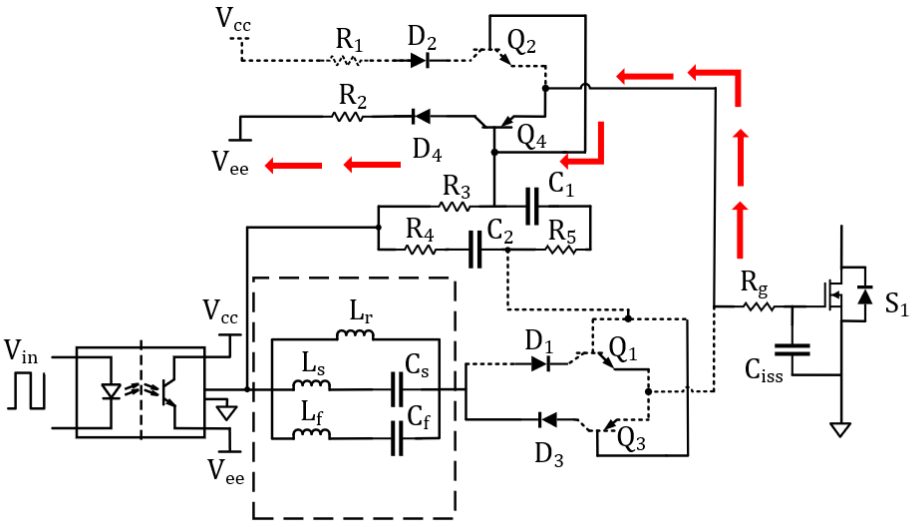



(b)

Figure 3.4: Equivalent circuits of each stage during the operation (a) $[t_0 - t_1]$, (b) $[t_1 - t_2]$




(a)




(b)

Figure 3.5: Equivalent circuits of each stage during the operation (c) $[t_2 - t_3]$, (d) $[t_3 - t_4]$

4. *Step 4* $[t_3 - t_4]$*:* Due to the losses associated with parasitic elements of the circuit $v_{gs}$ drops to a voltage greater than -5 V. Switch $Q_4$ at $t_4$ is turned on to compensate the voltage loss and $v_{gs}$ is clamped to the desired -5 V.

### 3.4.2 Characteristic Analysis

The operating characteristics of the proposed resonant gate driver is mainly determined by the resonant elements present in the circuit. Fig. 3.6(a) displays a simplified circuit model of the multiresonant gate driver and Fig. 3.6(b) displays equivalent input impedance of the circuit when the output is shorted. With the appropriate selection of the gain and it's phase content at different harmonic frequencies, the shape of the quasi-square wave can be adjusted [1]. The input square wave produced by the optocoupler contain only fundamental frequency $f_s$ and it's odd harmonics.

The expression for gain at the fundamental frequency $f_s$ can be obtained as [37]

$$|G_1(j\omega_s)| = \frac{\omega_0^2}{\sqrt{\left(\omega_0^2 - \omega_s^2\right)^2 + \left(\frac{\omega_0}{Q_0} \cdot \omega_s\right)^2}} \tag{3.2}$$

The parameters in (3.2) are defined as

$$\omega_s = 2\pi f_s,\ Q_0 = \frac{\omega_0 L_r}{R},\ \omega_0 = \frac{1}{\sqrt{L_r C_{iss}}}$$

The phase of $G_1(j\omega_s)$ can be obtained as

$$\angle G_1(j\omega_s) = -\arctan\left[\left(\frac{\omega_0}{Q_0}\right)\left(\frac{\omega_s}{\omega_0^2 - \omega_s^2}\right)\right] \tag{3.3}$$

Also, the expression for gain at the third harmonic frequency $3f_s$ can be obtained as

$$|G_3(j\omega_s)| = \frac{\omega_1^2}{\sqrt{\left(\omega_2^2 - 3\omega_s^2\right)^2 + \left(\frac{\omega_1}{Q_1} \cdot 3\omega_s\right)^2}} \tag{3.4}$$

The parameters in (3.4) are defined as

$$Q_1 = \frac{\omega_1 L_s}{R},\ \omega_1 = \frac{1}{\sqrt{L_s C_{iss}}},\ \omega_2 = \frac{1}{\sqrt{L_s C_s}}$$

The phase of $G_3(j\omega_s)$ is

$$\angle G_3(j\omega_s) = -\arctan\left[\left(\frac{\omega_1}{Q_1}\right)\left(\frac{3\omega_s}{\omega_2^2 - 3\omega_s^2}\right)\right] \tag{3.5}$$

In addition, the expression for gain at the fifth harmonic frequency $5f_s$ can be obtained as

$$|G_5(j\omega_s)| = \frac{\omega_3^2}{\sqrt{\left(\omega_4^2 - 5\omega_s^2\right)^2 + \left(\frac{\omega_3}{Q_3}\cdot 5\omega_s\right)^2}} \tag{3.6}$$

The parameters in (3.6) are defined as

$$Q_3 = \frac{\omega_3 L_f}{R},\ \omega_3 = \frac{1}{\sqrt{L_f C_{iss}}},\ \omega_4 = \frac{1}{\sqrt{L_f C_f}}$$

The phase of $G_5(j\omega_s)$ is

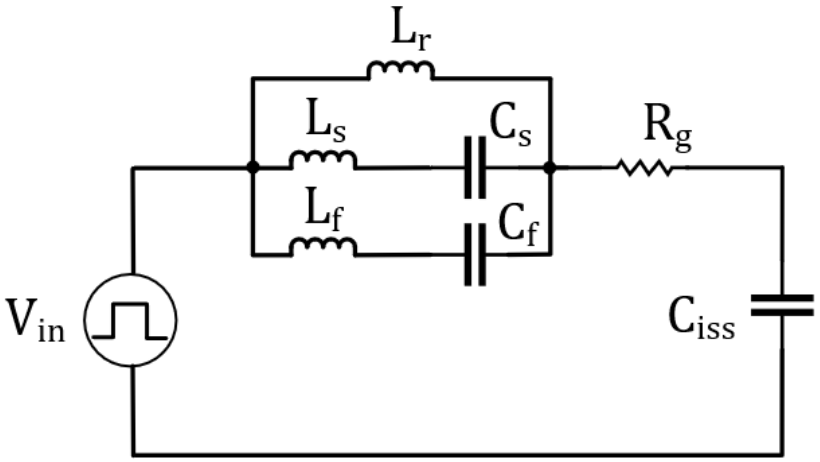
$$\angle G_5(j\omega_s) = -\arctan\left[\left(\frac{\omega_3}{Q_3}\right)\left(\frac{5\omega_s}{\omega_4^2 - 5\omega_s^2}\right)\right] \tag{3.7}$$

Based on (3.2), (3.3), (3.4),(3.5), (3.6), and (3.7) the functionality of the multiresonant filter network can be optimized. The overall input impedance plays an important role in the behavior the circuit at high frequency operations. If the circuit is capacitive at higher frequency, it will reduce the magnitude of total impedance of the circuit. Hence, circulating current will increase and eventually lead to higher losses. The expression for input impedance $Z_{mr}$ when output is shorted is given by

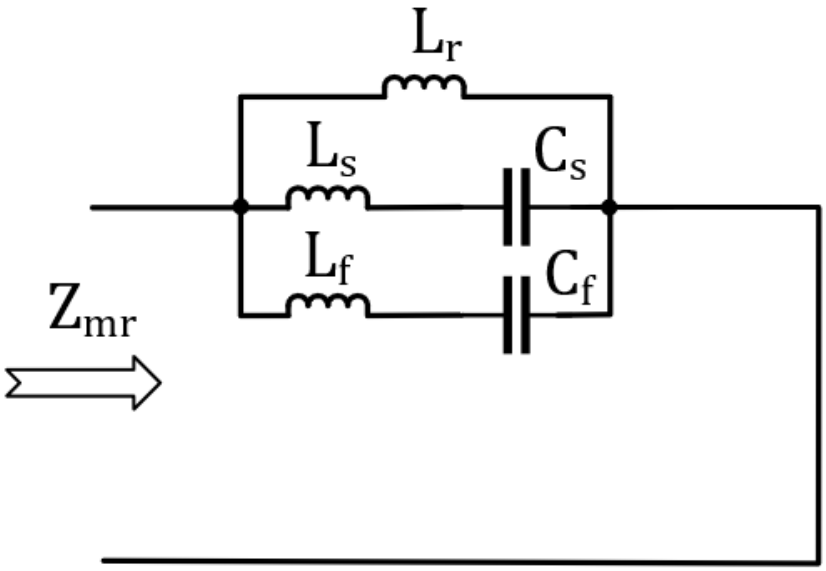
$$Z_{mr}(j\omega_s) = j\omega_s L_r || \left(j\omega_s L_s + \frac{1}{j\omega_s C_s}\right) || \left(j\omega_s L_f + \frac{1}{j\omega_s C_f}\right) \tag{3.8}$$

$$\mathrm{Z}_{mr}(j\omega_s) = \frac{j\omega_s L_r \times \left(j\omega_s L_s + \frac{1}{j\omega_s C_s}\right) \times \left(j\omega_s L_f + \frac{1}{j\omega_s C_f}\right)}{\left\{j\omega_s L_r\left(j\omega_s L_s + \frac{1}{j\omega_s C_s}\right)\right\} + \left\{\left(j\omega_s L_s + \frac{1}{j\omega_s C_s}\right)\left(j\omega_s L_f + \frac{1}{j\omega_s C_f}\right)\right\} + \left\{j\omega_s L_r\left(j\omega_s L_f + \frac{1}{j\omega_s C_f}\right)\right\}} \tag{3.9}$$

Based on (3.8) a expression for the input impedance is given by (3.9).




(a)




(b)

Figure 3.6: (a) Simplified model of the proposed RGD (b) Equivalent input impedance of the circuit at output short

### 3.4.3 Component Selection

o reduce the power consumption in the gate drive circuit, proper selection of the components is important. Diodes and transistors in the proposed circuit are selected with low voltage drop to decrease energy loss.

#### 3.4.3.1 Selection of resonant inductors and capacitors

Inductor $L_r$ and input capacitance $C_{iss}$ resonates at fundamnetal frequency $f_s$. The fundamental frequency is selected as 750 kHz. The selected MOSFET is NVHL040N120SC1 from ON semiconductor which has a $C_{iss}$ of 1781 pF. The initial value of $L_r$ can be determined by

$$L_r = \frac{1}{(2\pi f_s)^2 C_{iss}} \tag{3.10}$$

Using (3.10), the calculated value of $L_r$ is 25 $\mu H$.

$L_s$ and $L_f$ can be calculated by

$$L_s = \frac{1}{(6\pi f_s)^2 C_s} \tag{3.11}$$

$$L_f = \frac{1}{(10\pi f_s)^2 C_f} \tag{3.12}$$

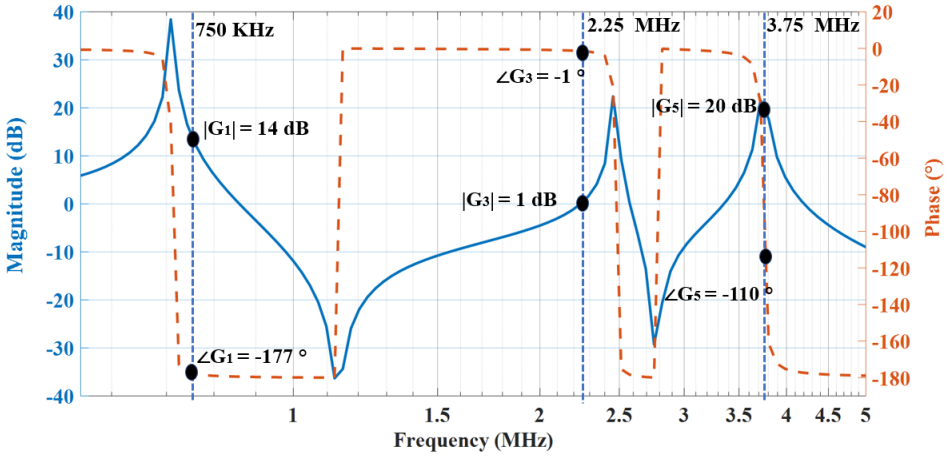
The values of $L_s$ and $L_f$ are calculated to be 15 $\mu H$ and 8 $\mu H$ using (3.11) and (3.12) respectively. $C_s$ and $C_f$ are design parameters and the initial values are selected to be 350 pF and 250 pF.

Table 3.1: Key components of the Proposed Gate Driver

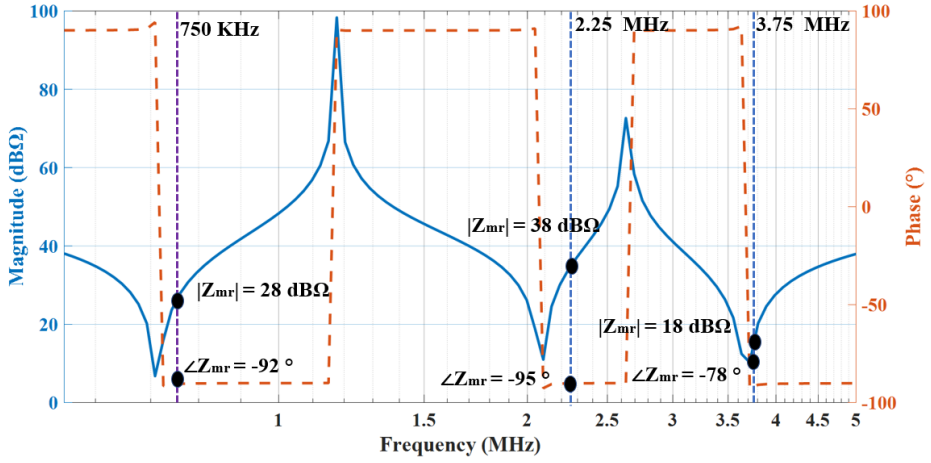
| Component | Value | Part name |
|---|---|---|
| $C_1$ | 15 nF | FG24C0G1H153JNT06 |
| $C_2$ | 0.22 $\mu F$ | FA14X7R1H224KNU06 |
| $C_s$ | 390 pF | FA28C0G1H391JNU06 |
| $C_f$ | 240 pF | C315C241J5G5TA |
| $L_r$ | 25 $\mu H$ | 5702-RC |
| $L_s$ | 15 $\mu H$ | 2303-V-RC |
| $L_f$ | 8 $\mu H$ | SBT-0208 |
| $R_3$ | 1.6 kΩ | CFR-12JB-52-1K6 |
| $R_4$ | 25Ω | RS01A25R00FE12 |
| $R_5$ | 27Ω | FKN5WSJR-73-27R |
| $Q_1$, $Q_2$ | | NPN BJT 2N4401 |
| $Q_3$, $Q_4$ | | PNP BJT 2N2907A |
| $S_1$ | | SiC MOSFET NVHL040N120SC1 |
| Optocoupler | | IR4427PBF |
| $D_1$, $D_2$, $D_3$, $D_4$ | | Schottky diode SB240 |

The square wave provided by the optocoupler is selected to be 10 V. In order to drive the voltage levels of $v_{gs}$ between -5 V to 15 V the gains at $f_s$, $3f_s$, and $5f_s$ are needed to be double or at 6 dB. LTSpice is used to determine the gain values and

the calculated values of $L_r$, $L_s$, $C_s$, $L_f$, and $C_f$ are used. Fig. 3.7(a) and Fig. 3.7(b) shows gain and impedance plot of the resonant network. As shown in Fig. 3.7(a), gain at fundamental frequency is 14 dB. Third harmonic and fifth harmonic gains are 1 dB and 20 dB respectively. However, the target gain is 6 dB for each of these frequencies. Moreover, impedance at fundamental, third harmonic and fifth harmonic are capacitive

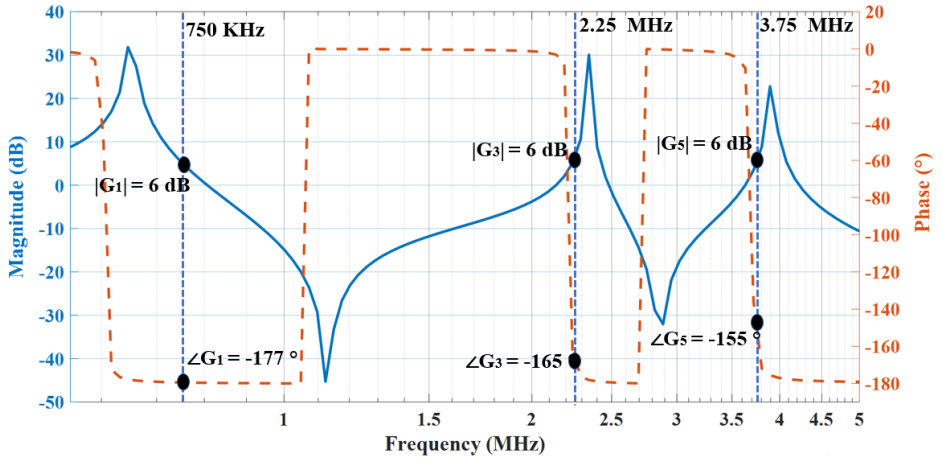



(a)

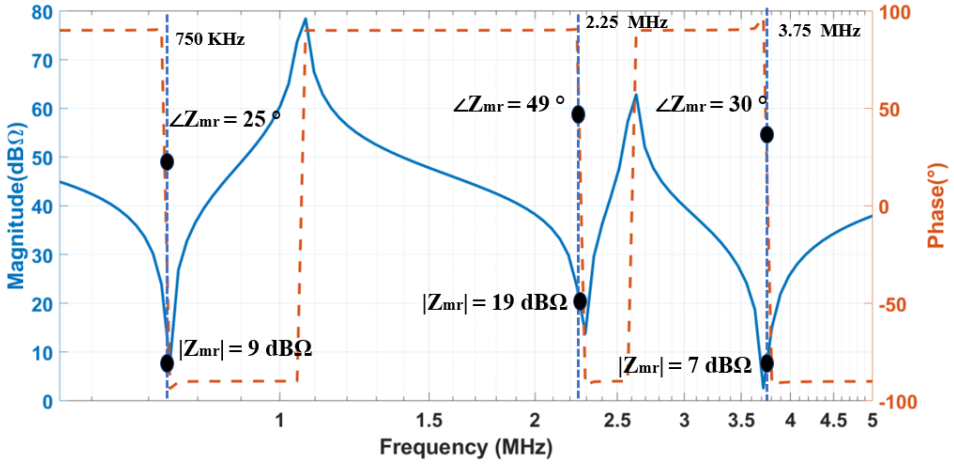



(b)

Figure 3.7: LTSpice simulation (a) Gain at $f_s$, $3f_s$ and $5f_s$ (b) impedance at $f_s$, $3f_s$ and $5f_s$




(a)




(b)

Figure 3.8: LTSpice simulation after update (a) Gain at $f_s$, $3f_s$ and $5f_s$ (b) impedance at $f_s$, $3f_s$ and $5f_s$

in nature. Hence, the values of the components are needed to be updated. Fig.3.8(a) and 3.8(b) shows the new gain and impedance plot of the resonant network. The final selected values of the components are listed in Table 3.1.

#### 3.4.3.2 Clamping Resistances

Resistances $R_1$ and $R_2$ are used to limit the current during the clamping stages. A value of 20 Ω is selected for these resistances.

#### 3.4.3.3 Switching Control Circuit for the BJTs

The combination of $R_4$, $C_2$ and $R_5$ generates the turn-on signal for BJTs $Q_1$ and $Q_3$. In order to avoid oscillation the time constant of $(R_4{+}R_5)C_2$ needs to be less than full transition time of 1.33 $\mu$s. The values of $R_4$ and $R_5$ are selected to be 25 $\Omega$ and 27 $\Omega$. The value of $C_2$ is selected to be 0.22 $\mu$F. In addition, combination of $R_3$ and $C_1$ provides the time delayed turn-on signal for the clamping operation of the BJTs $Q_2$ and $Q_4$. The values of $R_3$ and $C_1$ are selected to be 1.6 k$\Omega$ and 15 nF.

## 3.5 Analysis of Power Consumption

In this section, an analysis of power consumption of the proposed circuit is presented. Through inductive charging/discharging of $C_{iss}$ and recycling part of the energy, the proposed circuit can decrease the required gating power. During MOSFETs turn-on phase half of the energy is stored in $C_{iss}$ [38]. In the turn-off phase the other half is dissipated through gate resistor $R_g$ where gate resistance inside of the MOSFET is the dominant element. In the loss analysis, only the conduction losses are considered while the switching losses are ignored in the analysis as the turn-on and turn-off time intervals $t_1 - t_2$ and $t_3 - t_4$ are much shorter relative to the on and off state of the total circuit operation. The conduction loss across gate resistor $R_g$ due to the current at $\omega_s$ can be calculated as [1]

$$P_1 = \frac{1}{2} \times R_g \times \frac{V_1^2}{R_g^2 + \left(\frac{1}{\omega_s C_{iss}}\right)^2} \tag{3.13}$$

where $V_1$ can be determined by

$$V_1 = \frac{2}{\pi} V_{in}$$

Also, the gate driving power loss due to the current at $3\omega_s$ can be calculated as

$$P_3 = \frac{1}{2} \times R_g \times \frac{V_3^2}{R_g^2 + \left(\frac{1}{3\omega_s C_{iss}}\right)^2} \tag{3.14}$$

where $V_3$ can be determined by

$$V_3 = \frac{2}{3\pi} V_{in}$$

In addition, the gate driving power loss due to the current at $5\omega_s$ can be calculated as

$$P_5 = \frac{1}{2} \times R_g \times \frac{V_5^2}{R_g^2 + \left(\frac{1}{5\omega_s C_{iss}}\right)^2} \tag{3.15}$$

## 3.6 Experimental Results

To support the theoretical analysis of the proposed resonant gate driver and experimentally verify the performance, Dc-Dc boost converter is designed and built and operated in two distinct cases. Firstly, a 15-30 V Boost converter is operated by a conventional gate driver (CGD) and the proposed resonant driver (RGD). Gate driver IC IR4427 from International Rectifier is used as a CGD circuit which is a high speed power MOSFET driver. Secondly, a 30-60 V Boost converter is operated with both the drivers. Lastly, the gate power consumption in each of the cases were measured and compared.

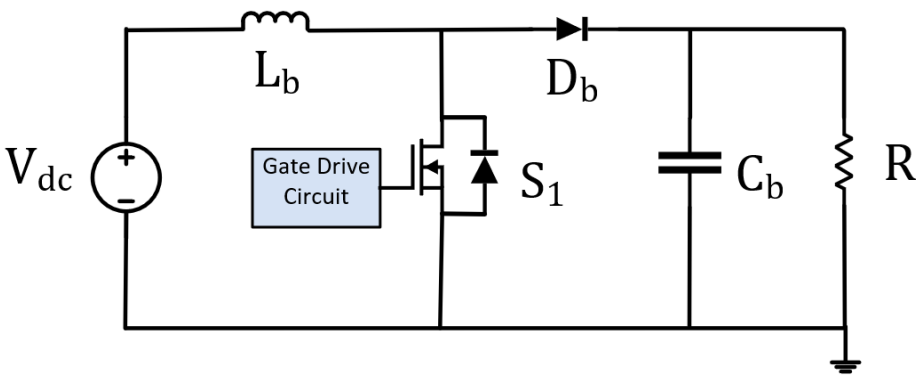



Figure 3.9: Gate driver testing circuit

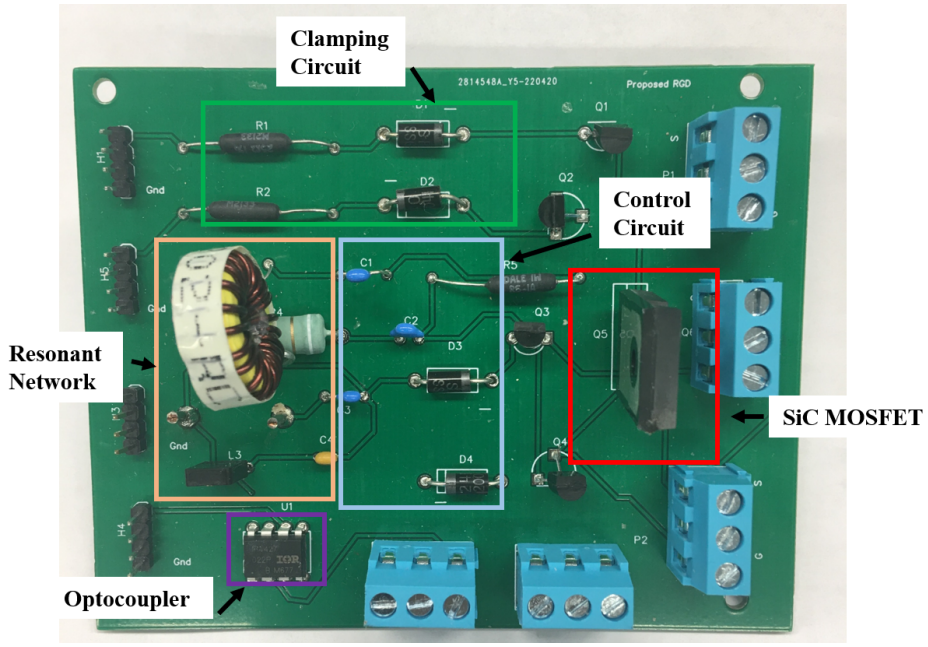


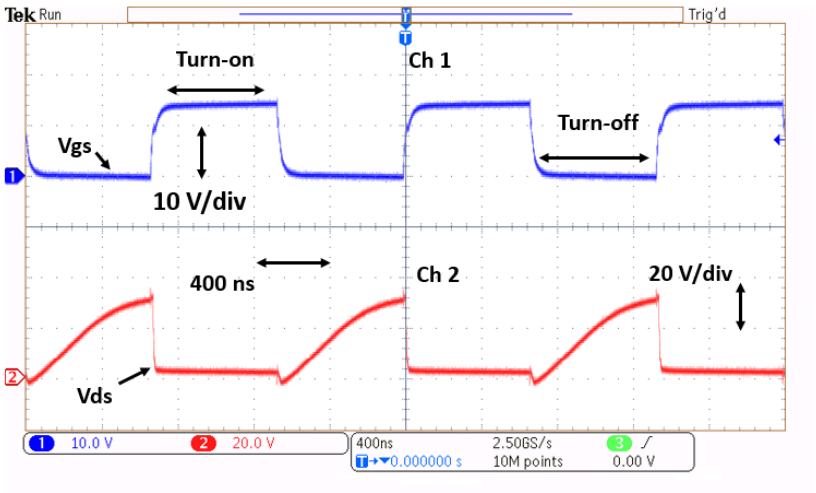

Figure 3.10: Proposed resonant gate driver circuit

Fig. 3.9 shows the diagram of the testing circuit. The switching frequency for the experiment is 750 KHz and the duty cycle is selected to be 50%. The value of the load resistance is 50 Ω. The list of components used for the experiment is shown in Table 3.2. Fig. 3.10 shows the photograph of the proposed gate driver circuit.

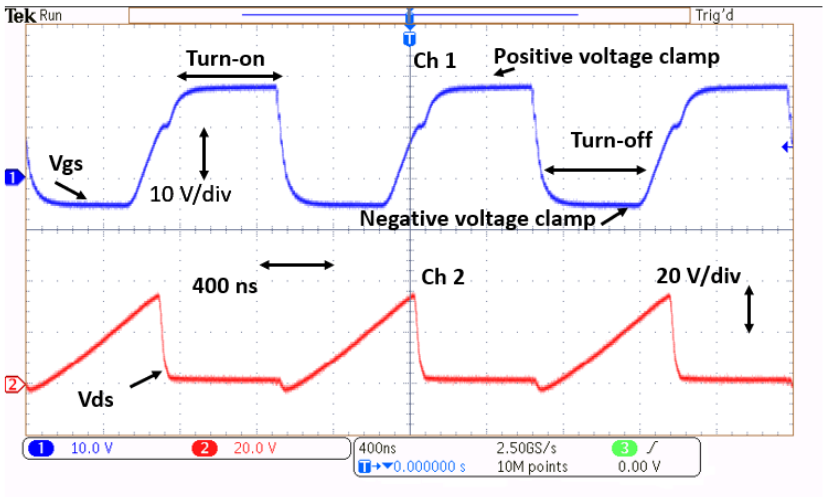
Fig. 3.11(a) and 3.11(b) shows the experimental waveforms of gate to source voltage of the MOSFET ($v_{gs}$) and drain to source voltage of the MOSFET ($v_{ds}$) for the CGD and RGD respectively while driving 15-30 V converter case. The CGD circuit drivng

Table 3.2: Components for experiment

| Component | Value | Part name |
|---|---|---|
| Boost Capacitor $C_b$ | 100 $\mu F$ | 100ZLH100MEFC10X20 |
| Boost Inductor $L_b$ | 25 $\mu H$ | 5702-RC |
| Load Resistor R | 50 $\Omega$ | TEH100M50R0FE |
| Diode $D_b$ | | SB240 |

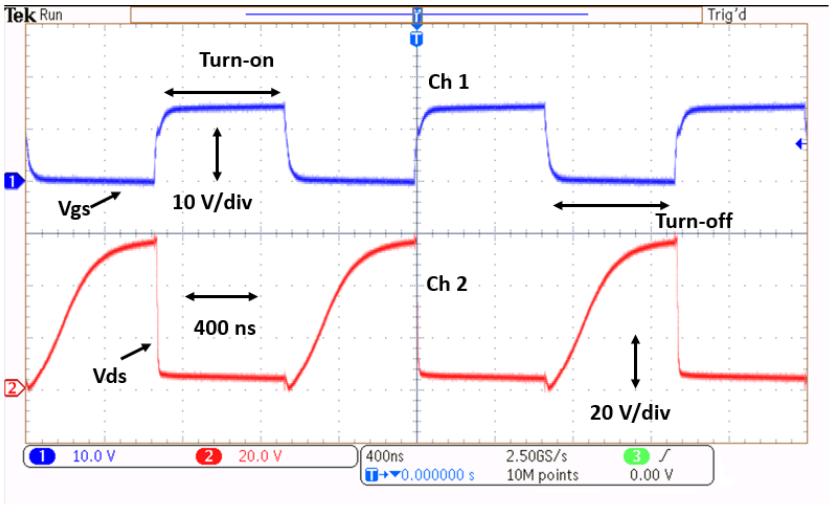



(a)

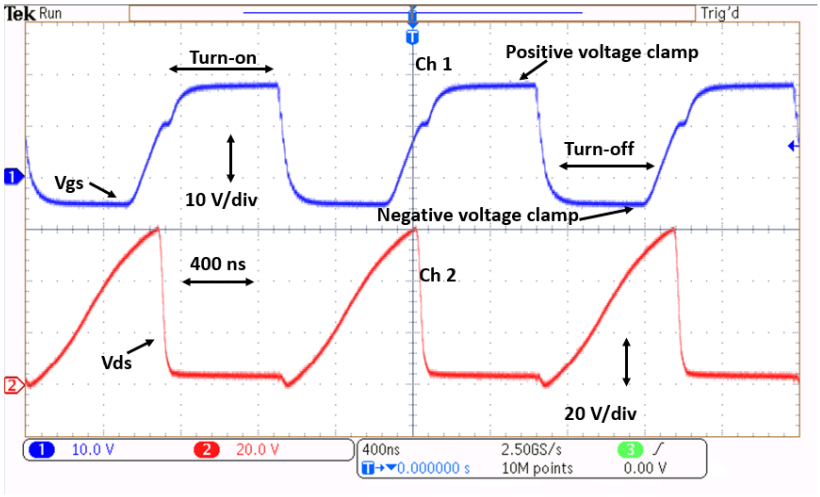



(b)

Figure 3.11: Observed waveforms $v_{gs}$ and $v_{ds}$ at 30 V load voltage (a) Conventional Gate Drive (b) Proposed Resonant Gate Drive




(a)




(b)

Figure 3.12: Observed waveforms $v_{gs}$ and $v_{ds}$ at 60 V load voltage (a) Conventional Gate Drive (b) Proposed Resonant Gate Drive

the MOSFET of the circuit at 15 V during turn-on and at 0 V during turn-off. On the other hand, the RGD circuit clamping the driving signal for the MOSFET at the desired positive and negative voltage levels of 15 V at turn-on and -5 V at the turn-off. Fig. 3.12(a) and 3.12(b) shows $v_{gs}$ and $v_{ds}$ for the 30-60 V converter case. Fig. 3.13 shows the boost testing circuit.

In order to calculate power consumption, a high precision Agilent 34401A digital multimeter is used. The voltage applied to the gate drive circuit and current passing through the circuit is measured using the meter. Then, the product of these two values is calculated as the power consumed by the gate driver circuit.

A comparison of the power consumption among the gate driver circuits for 15-30 V converter is given in Table 3.3. It is found that the power consumed by the proposed RGD circuit is 205 mW. In the case for the CGD circuit it reaches 584 mW. In addition, for the 30-60 V converter case power consumed by CGD is 597 mW while for the proposed RGD circuit it is 196 mW. It is observed that the gate drive power consumption remains almost same irrespective of the power level of the system. The power consumption of the driver circuit mostly depend on the operating switching frequency for a particular system as shown in (3.1).

The gate driver power consumption is reduced by around 65% in comparison to a conventional gate driver. This is due to the recycling of the energy stored in the capacitance and the clamping functionality. In addition, it is observed that the gate drive power consumption remains almost same irrespective of the power level of the system. In the experimental study it is assumed the optocoupler power consumption remains constant and it is excluded from the gate driver power consumption analysis.

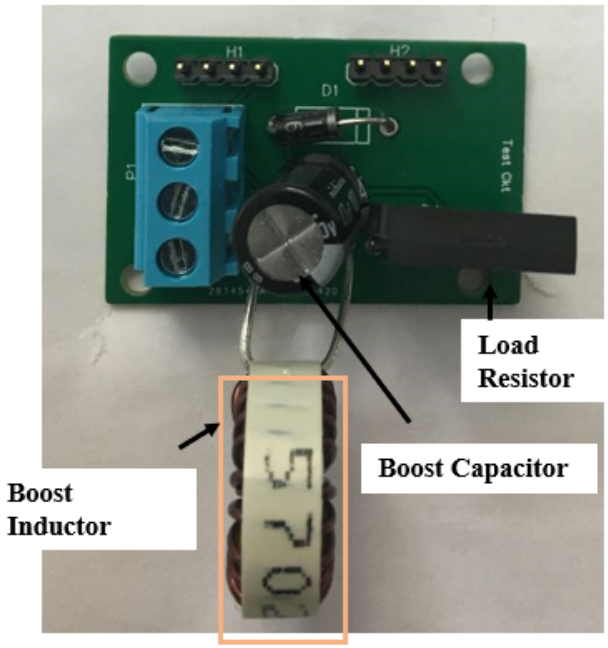



Figure 3.13: Photograph of DC-DC Boost converter testing circuit

Table 3.3: Comparison Between Conventional Gate Driver and Resonant Gate Driver

| | Parameters | CGD | RGD |
|---|---|---|---|
| 15-30 V Converter | $V_{in}$ | 15 V | 15 V |
| | $R_L$ | 50 Ω | 50 Ω |
| | $V_{RL}$ | 30 V | 30 V |
| | Gate supply voltage | 10 V | 10 V |
| | Gate supply current | 58.4 mA | 20.5 mA |
| | Gate Power Consumption $P_{gate}$ | 584 mW | 205 mW |
| 30-60 V Converter | $V_{in}$ | 30 V | 30 V |
| | $R_L$ | 50 Ω | 50 Ω |
| | $V_{RL}$ | 60 V | 60 V |
| | Gate supply voltage | 10 V | 10 V |
| | Gate supply current | 59.7 mA | 19.6 mA |
| | Gate Power Consumption $P_{gate}$ | 597 mW | 196 mW |

## 3.7 Conclusion

In this paper a new multiresonant gate drive circuit is presented with design, analysis and experimental implementation. In this study DC-DC boost converter with 750 kHz switching frequency was built and the gate of the MOSFET was driven by a conventional multiresonant circuit and the proposed gate driver. In addition, the performance of the proposed circuit is compared with a conventional gate driver circuit. The proposed circuit could clamp the gate source voltage to two unequal voltage levels. In addition, it can recycle stored charge in the input capacitance $C_{iss}$. Hence, overall power consumption of the gate driver has significantly reduced. SiC based devices exhibit a reduction in threshold voltage level in the off-state which leads power consumption loss in the driver circuit. A negative clamping in the off-state improves the efficiency of the switching process. In this research, operation principle and a detailed analysis of the power consumption by the proposed resonant gate driver are provided. From the results, it was observed experimentally that the proposed gate driver can reduce power consumption by upto 65% compared to a conventional gate driver circuit.

# CHAPTER 4: A High-Performance Resonant Gate Driver Circuit for GaN MOSFETs

## 4.1 Abstract

This paper proposes a new high performance resonant gate driver for Gallium Nitride (GaN) Metal Oxide Field Effect Transistors (MOSFETs). In order to reduce the power consumption in the gate driver, this paper presents a novel gate driver which utilises higher order harmonics to generate quasi square wave to drive the GaN MOSFET. High switching frequency is a necessary condition in order to achieve reduced footprint of the overall system. However, with high operating switching frequency the power consumption in the circuit increases. In a conventional gate driving circuit all the energy is dissipated in the gate resistance when the turn-on and turn-off sequence occur. A resonant circuit is an efficient way to recycle part of the energy stored in the gate capacitance when one switching event is completed. In this paper, a resonant gate driving circuit is proposed which can reduce the energy loss of the driver circuit than a conventional gate driving circuit.

## 4.2 Introduction

Recently, gallium nitride (GaN) based power devices has been widely utilised for low power converter applications for their better switching capabilities [39]. GaN power devices show lower input capacitances in compare to Silicon and Silicon Carbide based MOSFETs [40]. Particularly, in low power DC-DC converter applications, GaN based devices show better performance in regard to switching and operating voltage levels [41, 42].

A conventional gate driver circuit provides sufficient energy to the input capacitance

in order to turn it on. In addition, during the turn-off stage it removes the charge from the input capacitance. However, during the switching operation, the energy is dissipated through the gate resistance. This dissipated energy is responsible for the heat loss and reduction of the efficiency of the system. One common way to reduce the power consumption in the driving circuit is to utilize resonant gate driving strategy[1, 23]. In this technique, a resonant inductor is placed and designed such a way to form resonance with the gate capacitance. This way part of the energy is recycled and the system efficiency is improved. In [1], a multiresonant gate driving technique is proposed where fundamental and third harmonic content of a square wave is utilized to generate a quasi-square wave and that eventually drive the MOSFET. However, due to the presence of parasitic components in the circuit the voltage level fluctuates from the desired voltage level and it constitue losses in the circuit. Hence, a better strategy would be to clamp the gate-source voltage at a desired negative voltage and a positive voltage.

## 4.3 Proposed Gate Driver

Many resonant gate drivers are proposed in the literature for silicon, silicon carbide and gallium nitride based devices [42, 28, 43]. One of the common technique that is utilized is providing bipolar voltage levels with equal value [30, 31]. However, as pointed out in [1, 17, 29], a more desirable gate-source voltage signal would be to drive the device using unequal voltage levels. The proposed resonant gate driver is depicted in Fig. 4.1. The resonant elements $L_r$, $L_s$ and $C_s$ form a multiresonant network which produces a quasi-square wave in the gate terminal of the MOSFET $S_1$. The circuit operates in the following four steps. At first, $Q_1$ is turned on which eventually initiates the energy trasfer from the resonating network. In the following step, the clamping function is achieved by turning on $Q_2$. Due to the presence of parasitic elements, the circuit losses some energy. This energy is supplied by the external voltage source. At the next step, $Q_3$ is turned on and the charge in the capacitance starts to fall. At the

last step, $Q_4$ is turned on, and due to losses incurred by the parasitic components are fulfilled by the other voltage source $V_{ee}$

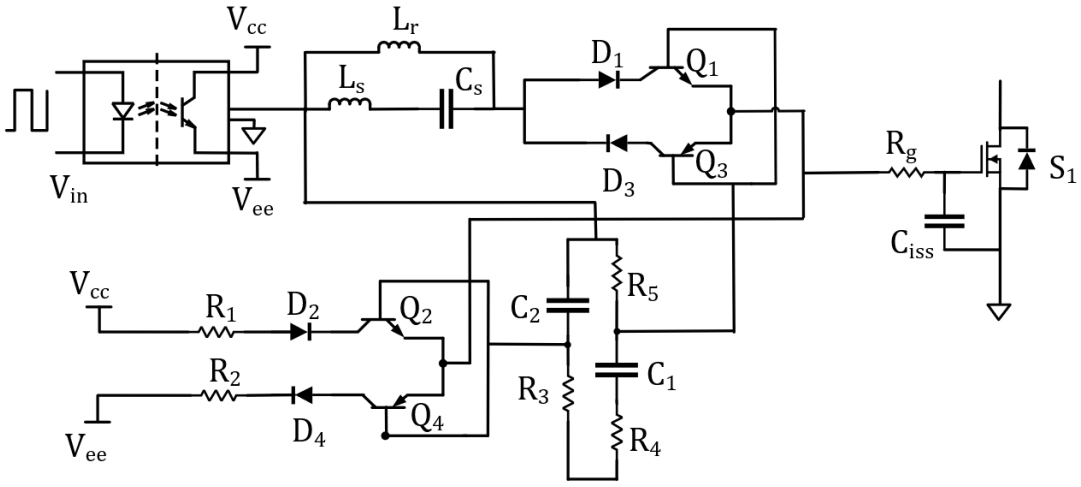



Figure 4.1: Proposed Gate Driver

## 4.4 Characteristic Analysis

The resonating elements present in the circuit plays the central role in determining the characteristics of the proposed circuit. The shape of the quasi-square wave largely depend on the gain at different harmonic frequencies. Input impedance of the overall circuit when output is short plays a significant role in circuit characteristics. The load in this case is the capacitance $C_{iss}$, hence it is desirable to have inductive driver circuit in order to achieve a resonance. In addition, for a capacitive circuit impedance is reduced for higher switching frequency operations. It can lead to higher circulating current in the circuit which eventually can lead to higher losses in the system. (4.1) is the impedance expression for the proposed circuit.

$$Z_{mr}\left(j\omega_s\right) = j\omega_s L_r || \left(j\omega_s L_s + \frac{1}{j\omega_s C_s}\right) \tag{4.1}$$

The on state switching energy loss is important to analyse the performance of a

gate driver. It can be calculated as

$$E_{on} = \frac{1}{2} \times V_s I_{Amax} \times t_{on} \tag{4.2}$$

$$E_{off} = \frac{1}{2} \times V_s I_{Amax} \times t_{off} \tag{4.3}$$

From these equations it is evident that the on-state energy loss and off-state energy loss depend mostly on the rising and falling time of the switching signal.

## 4.5 Simulation Analysis

The simulation study on the proposed circuit is performed using LTSpice simulation platform. The selected GaN device is GAN063-650 from Nexperia. The key parameters of the device is provided in Table 4.1. The drain-source voltage $V_{DS}$ is 650 V and maximum allowable drain current $I_D$ is 34.5 A. This GaN device has a maximum gate-drain charge $Q_{GD}$ of 4 nC.

Table 4.1: Key Parameters of GaN

| Parameter | Symbol | Value |
|---|---|---|
| Drain-source voltage | $V_{DS}$ | 650 V |
| Drain current | $I_D$ | 34.5 A |
| On-state resistance | $R_{DSon}$ | 50 mΩ |
| Gate-drain charge | $Q_{GD}$ | 4 nC |

Table 4.2: Components for the Testing Circuit

| Parameter | Symbol | Value |
|---|---|---|
| Inductor | $L_1$ | 25 $\mu H$ |
| Capacitor | $C_1$ | 50 $\mu$ F |
| Diode Schottky | $D$ | SB2100TA |
| GaN MOSFET Nexperia | $S_1$ | GAN063-650 |

A 36-18 V DC-DC buck converter is designed in the study. The duty cycle is selected as 50%. Fig. 4.2 shows the schematic of the testing circuit. Two separate gate drivers are used to drive the GaN MOSFET switch. Initially, a conventional gate driver is implemented and the MOSFET switch in the testing circuit is driven. Second, the proposed gate driver is implemented and the same MOSFET switch is driven using the proposed driver. The value of the load resistance is selected to be 50 Ω. In this case, inductor $L_1$ is selected to be 25 $\mu H$ and capacitor $C_1$ is selected to be 50 $\mu$F. Table 4.2 shows the selected component list of the testing circuit.

The energy loss in a switching event largely depend on the rising time and falling time of the gate-source voltage. Also it plays a crucial part in the determination of the power consumption in the circuit. To reduce energy consumption component selection plays a significant role. For the selected GaN device $C_{iss}$ is 1000 pF. This capacitance resonates with the inductance of the proposed gate driver. The resistances are selected to be limiting the current in the case of clamping stage. The control circuit uses resistance and capacitance with required time constants to avoid any false triggering.

Gate-source voltage for the both cases are shown in Fig. 4.3. As seen in Fig. 4.3 (b) gate-source voltage for the proposed driver the positive and negative voltage levels are clamped in to the desired voltage levels of a small off-state negative voltage and a large on-state positive voltage.

In this analysis, three distinct cases were selected. In the first stage for 250 KHz switching frequency the turn-on and turn-off switching energy were measured. As shown in Table 4.3, the $t_{on}$ for the gate driver in [1] is 97.8 ns while for the proposed RGD circuit it is 81.3 ns. The $t_{off}$ for the proposed circuit is 80.6 ns. The turn-on loss and turn-off loss is calculated. For the gate driver in [1] turn-on loss is 2.93 $\mu J$. For the proposed circuit it is found out to be 2.45 $\mu J$. The total energy loss calculated from (4.2) is 5.83 $\mu J$ for the gate driver in [1]. For the proposed gate driver this energy loss is 4.86 $\mu J$ which is around 17 % energy loss reduction. In the case of 500 KHz, the $t_{on}$ for the gate driver in [1] is 73.2 ns while for the proposed RGD circuit it is 56.5 ns. The $t_{off}$ for the proposed circuit is 53.58 ns. For the proposed RGD total energy loss is 3.42 $\mu J$ which is around 21 % energy loss reduction. For 750 KHz case the $t_{on}$ for the gate driver in [1] is 48.5 ns while for the proposed RGD circuit it is 32.7 ns. The $t_{off}$ for the proposed circuit is 31.6 ns. The calculated turn-on loss and turn-off loss for the proposed RGD circuit case is found to be 1.04 and 0.93 $\mu J$ respectively. For the proposed RGD total energy loss is calculated as 1.97 $\mu J$. The energy loss reduction is around 30 %.

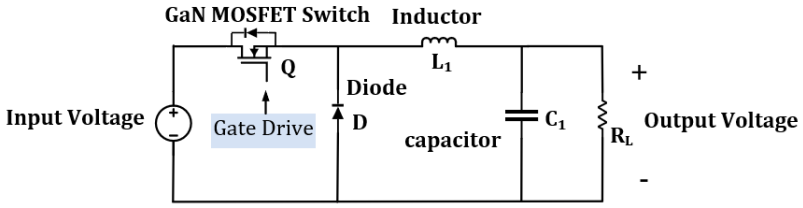
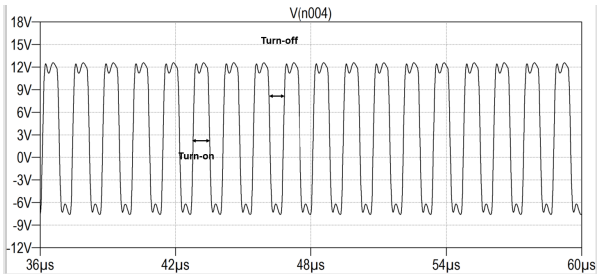
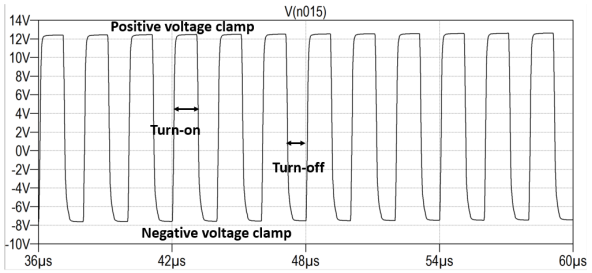



Figure 4.2: Gate driver testing circuit




(a)




(b)

Figure 4.3: (a) Simulation waveform $v_{gs}$ for the RGD [1] (b) waveform $v_{gs}$ for proposed RGD

Table 4.3: Comparison Between RGD in [1] and Proposed Resonant Gate Driver for 250 KHz

| Parameters | RGD in [1] | Proposed RGD |
|---|---|---|
| $t_{on}$ | 97.8 ns | 81.3 ns |
| $t_{off}$ | 96.5 ns | 80.6 ns |
| $t_{on_{Loss}}$ | 2.93 $\mu J$ | 2.45 $\mu J$ |
| $t_{off_{Loss}}$ | 2.90 $\mu J$ | 2.41 $\mu J$ |
| F | 250 KHz | 250 KHz |
| T | 4000 ns | 4000 ns |
| Total Switching energy loss | 5.83 $\mu J$ | 4.86 $\mu J$ |

Table 4.4: Comparison Between RGD in [1] and Proposed Resonant Gate Driver for 500 KHz

| Parameters | RGD in [1] | Proposed RGD |
|---|---|---|
| $t_{on}$ | 73.2 ns | 56.5 ns |
| $t_{off}$ | 71.6 ns | 53.58 ns |
| $t_{on_{L}oss}$ | 2.19 $\mu J$ | 1.81 $\mu J$ |
| $t_{off_{L}oss}$ | 2.14 $\mu J$ | 1.61 $\mu J$ |
| F | 500 KHz | 500 KHz |
| T | 2000 ns | 2000 ns |
| Total Switching energy loss | 4.33 $\mu J$ | 3.42 $\mu J$ |

Table 4.5: Comparison Between RGD in [1] and Proposed Resonant Gate Driver for 750 KHz

| Parameters | RGD in [1] | Proposed RGD |
|---|---|---|
| $t_{on}$ | 48.5 ns | 32.7 ns |
| $t_{off}$ | 46.3 ns | 31.6 ns |
| $t_{on_{L}oss}$ | 1.45 $\mu J$ | 1.04 $\mu J$ |
| $t_{off_{L}oss}$ | 1.30 $\mu J$ | 0.93 $\mu J$ |
| F | 750 KHz | 750 KHz |
| T | 1333.33 ns | 1333.33 ns |
| Total Switching energy loss | 2.75 $\mu J$ | 1.97 $\mu J$ |

As shown in Fig. 4.4, in low switching frequency applications the energy saving is around 17%. However, the proposed RGD circuit can save significantly more energy and thus more efficient in the high switching frequency applications. For very high switching frequency this energy saving can be upto 30 %.

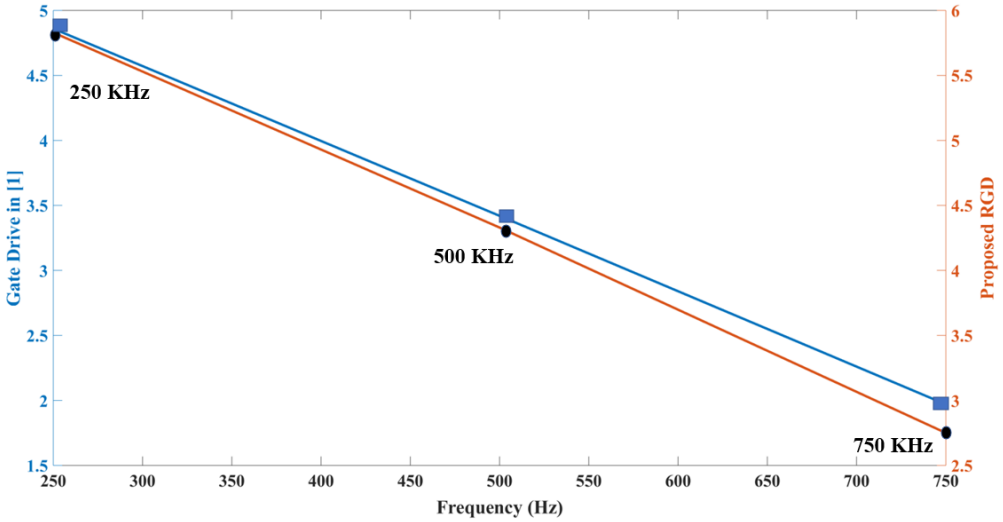



Figure 4.4: Comparison of switching energy losses for the gate drivers

## 4.6 Conclusion

In this article a new resonant gate drive circuit is presented for GaN devices. The switching energy loss of the device depend on the rising and falling time of the gate-source voltage. A simulation study is presented. The drivers are tested with a 36-18 V Buck converter. It is shown from the results in increasing switching frequency the proposed gate driver can save more energy than a resonant circuit and can save switching energy upto 30% in high speed switching operations.

# CHAPTER 5: Conclusion and Future Work

## 5.1 Conclusion

Gate driving circuit is the key component in any power electronic converter applications. Gate driver works as an amplifier circuit and an intermediate layer between controller signal and main power circuit. For a Metal-Oxide Field Effect Transistor (MOSFET) the driving signal is a voltage pulse. Hence, the main objective of a gate driver circuit in a MOSFET based architecture is to source sufficient voltage to teun-on the MOSFET. In addition, it should have the capability to sink the charge in the off-state. The main sequence of event in a switching is governed by the charge and discharge of gate capacitance by the gate voltage. In this dissertation a novel multiresonant gate drive (RGD) circuit for Wide Bandgap based power MOSFETs has been proposed which can clamp the gate-source voltage in desired unequal voltage levels. The main limitation of a conventional gate driving circuit is it only can provide unipolar gate pulses. In high switching frequency applications, particularly in off state, the charges present in the channel needs to be removed instantly in order to operate with less loss. In the case of conventional gate driver circuit this objective is not fulfilled. Hence, a gate driver design is required for the MOSFET which can swiftly turn-off the device with a negative gate pulse. A negative gate pulse can reduce the losses and power consumption in gate driver circuitry as the discharging of the gate happens faster in that case.

First, in the case of SiC MOSFETs it is desirable to clamp the gate voltage to a high positive voltage and a relatively small negative voltage. Typical values for these two voltages are 15 V and -5 V respectively. In this dissertation this objective was achieved. The proposed gate driver circuit can clamp the gate-source voltages to the

desired unequal voltage levels. Compared to a conventional gate driver the proposed RGD can reduce power consumption in the gate driver for upto 65 %.

Detailed design procedure of the RGD is presented. The components were selected based upon the inductive characteristic. Impedance characteristic plays a significant role as the gate driver is to behave as an inductive circuit. If that is not the case the resonance cannot occur as the main driving load is capacitive in nature.

Detailed mathematical analysis with characterization of the proposed RGD is presented. The gain and phase of the harmonics at certain frequencies plays a crucial role in the characteristic of the circuit. It is desirable to have the proper gain at certain key frequencies. The important frequencies are the odd harmonics of the fundamental. As the input to the gate is a square wave signal, only the odd harmonics are present when a Fourier analysis is done. All the even harmonics are become zero. Hence, by tuning the capacitance and inductance values it was possible to get the desired gain and phase of the circuit.

In addition, a resonant circuit is proposed for GaN MOSFETs. It is observed from the analysis and result that the proposed circuit can reduce the energy loss of the gate driver and for high frequency applications this can be upto 30 % switching energy saving.

## 5.2 Future Work

Resonant gate driving (RGD) technique is an useful way to reduce the power consumption in a gate driver circuit. In this technique an inductor is used in series with the gate capacitor for the resonance which eventually can lessen the power consumption of the circuit. Multiresonant gate driving (RGD) technique is a subsection of RGD technique where more than one resonating elements are present in the circuit. This technique primarily is utilized for low voltage applcations in this research. How ever, this could be utilized for high voltage power electronic applications.

Proposed RGD technique could be implemented in very high frequency switching

applications such as RF circuits. In very high frequency designs the inductor and capacitor size is reduced and hence the heat dissipation is easier for these type of circuit. However, higher frequency constitute more power loss in the device as in each switching instant a particular amount of energy is lost in the gate terminal. This technique could be a potential solution for this issue.

The proposed RGD could be further developed to address false triggering issue and cross talk issue of device switching. When devices are operated in a bridge-leg configuration, in order to perform the assigned task by the converter, one switch of the leg needs to be on and other one needs to be off at any moment in time. If two of the devices turned on at a particular moment at the same time, a short circuit situation may arise which can eventually lead to very high current and destruction of the system due to very high heat. On the other hand, in the same bridge-leg configuration, in very high switching operation, due to electromagnetic interference, other switch can accidentally turn-on. This situation can create very high current in the circuit as well.

In addition voltage overshoot or very high rate of change of voltage and current is a major cause of device failure. Sudden changes create stress on the device structure and create an enormous amount of heat which eventually can break the inner structure of the device and ultimately lead to the complete destruction and even creation of fire. Negative spikes are also a serious issue where a sudden decrease of the voltage or current in a very short span of time can create destruction of the device. These can be mitigated conjunction with the proposed circuit.

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