“SI IGBT AND SIC MOSFET” HYBRID SWITCH FOR VOLTAGE SOURCE CONVERTERS

by

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ABSTRACT

HAICHEN LIU. “Si IGBT and SiC MOSFET” Hybrid Switch for Voltage Source Converters. (Under the direction of DR. TIEFU ZHAO)

The SiC devices have been a strong competitor than the conventional Si devices due to the superior characteristics of high operating voltage, low forward voltage, fast switching speed, and high operating temperature. However, the maturity of SiC technology is still in the progress of catching up with the Si devices, the device cost for SiC MOSFET is still much higher than the Si devices. In addition, the maximum current rating of the available SiC devices are still lower than the Si devices, this also limits the utilization of SiC device in high-power applications. In order to combine the Si IGBT’s advantages of low cost and high overload capability and the SiC MOSFET’s advantages of low switching loss. The Si IGBT and SiC MOSFET are connected in parallel as a new switching unit. In this dissertation, the Si IGBT and SiC MOSFET hybrid switch (Si/SiC HyS) in the application of voltage source converters is investigated. The main works are as follows:

Firstly, the configuration, conduction characteristic, and switching characteristic of Si/SiC HyS are introduced. The unique dynamic current sharing process and loss modeling for the Si/SiC HyS are analyzed and proposed. The conduction and switching performance are characterized experimentally.

Secondly, the operation optimization including the Si and SiC device current rating selection, gate delay time selection, and active thermal control for the Si/SiC HyS are investigated. By using the proposed Si and SiC current rating optimization method, the most cost-effective Si/SiC HyS pairs are obtained for the Si/SiC HyS converter. The optimization of the gate delay time reduces the total semiconductor loss for the Si/SiC HyS

and improves the converter efficiency. In order to overcome the thermal unbalance between the Si IGBT and SiC MOSFET, two active thermal control algorithms, named “conduction time variation active thermal control” and “switching sequence dispatch active thermal control”, are proposed to reduce the thermal stress of SiC MOSFE. Experimental results validated the effectiveness of the proposed ATC algorithms.

Thirdly, the performance of Si/SiC HyS-based converter is improved by the proposed multi-objective operation control. In the light load condition, the converter operates with the conventional gate driving sequence, while in the heavy load condition, the converter’s maximum output power is improved by using the proposed active thermal control algorithms. The experimental results show that the maximum output power of Si/SiC HyS-based buck converter is improved by 5.9%. In addition to the maximum output power improvement, the proposed active thermal control for the Si/SiC HyS can also enhance the converter’s reliability. The reliability enhancement evaluation was investigated based on the UPS inverter application. A mission profile-based converter reliability enhancement evaluation is conducted to assess the yearly accumulated damage reduction on the device bond wire by using the active thermal control. The analysis results show that the yearly accumulated damage on the SiC MOSFET is reduced by 80% by using the proposed active thermal control. Thereby, the useful lifetime of Si/SiC HyS-based converter is extended.

Finally, two types of Si/SiC HyS-based three-level active neutral-point-clamped (3L-ANPC) inverter are proposed for high efficiency and low device cost. The proposed Si/SiC HyS-based 3L-ANPC inverters are compared with the full Si IGBT, full SiC MOSFET, and Si with SiC devices-based hybrid 3L-ANPC solutions on the inverter

efficiency, power capacity, and device cost. It is shown that compared with the full Si IGBT 3L-ANPC solution, the inverter efficiency improvement by using Si/SiC HyS is 2.4% and 1.8% at light load condition and heavy load condition, respectively. Compared to the full SiC MOSFET solution and 2-SiC MOSFET hybrid scheme, the device cost of 2-Si/SiC HyS-based 3L-ANPC is reduced by 78% and 50% with 0.28% and 0.21% maximum inverter efficiency sacrifices. The testing results show that the proposed Si/SiC HyS-based 3L-ANPC inverter is a cost-effective way to realize high inverter efficiency. Between the two proposed Si/SiC HyS-based 3L-ANPC inverters, the 2-Si/SiC HyS-based 3L-ANPC inverter has lower device cost which makes it more suitable for cost-sensitive and high efficiency applications. While the 4-Si/SiC HyS-based 3L-ANPC inverter has higher output power capacity, making it a better candidate for high power density, high power capacity, and high efficiency applications. Based this work, a 50kW 2-Si/SiC HyS-based 3L-ANPC battery inverter is proposed as a cost-effective and high efficiency solution for the energy storage industry. The design process and testing results are presented.

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LIST OF ABBREVIATIONS

Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
Si/SiC HyS	Si IGBT and SiC MOSFET Hybrid Switch
GaN	Gallium Nitride
GTR	Giant transistor
GTO	Gate Turn-off Thyristor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
PT	Punch Through
NPT	Non-Punch Through
FS	Filed Stop
VDMOS	Vertical Diffusion Metal-Oxide Semiconductor
JFET	Junction Field Effect Transistor
3L-ANPC	Three-Level Active Neutral Point Clamped
BOM	Bill of Material
DSP	Digital Signal Processor
UPS	Uninterruptable Power Supply
AC	Alternating Current
DC	Direct Current
DSP	Digital Signal Processor

mH	Millihenry
ms	Millisecond
J	Joule
PCB	Printed Circuit Board
s	Second
SiC	Silicon Carbide
V	Volt
W	Watt
Ω	Ohm
ATC	Active thermal control

CHAPTER 1: INTRODUCTION

1.1 Motivation

Power electronics has been widely used in the power conversion, power system protection, national defense, and many other applications. The high-power density and high efficiency power supplies are in demanding in different areas including electrical vehicles, energy storage systems, renewable energy microgrids, etc. In the power conversion process, semiconductor devices have significant impact on the performance of power electronic systems [1]-[10].

Currently, the power electronic system is in facing of the transition from Si material semiconductor devices to the wide bandgap devices due to the superior performance on the high operation voltage and high frequency switching, as shown in Figure 1-1. For the SiC material-based devices, they can operate at higher temperatures, higher operation voltage, and higher switching frequency due to the SiC material's better properties [11].

Among the third-generation wide bandgap devices, SiC MOSFET is a typical device that has been widely utilized in the high power density and high efficiency scenarios. The comparisons considering conduction loss, switching loss, and device cost between the

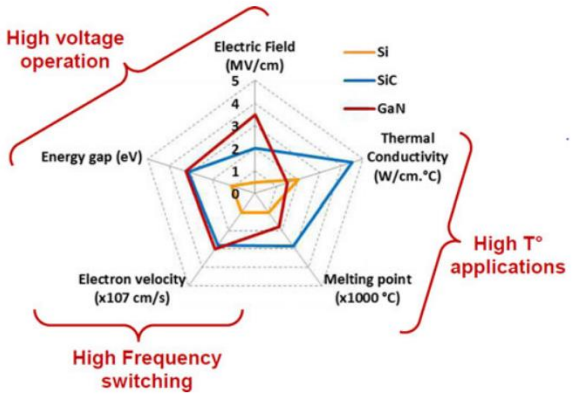


Figure 1-1 Si, SiC, and GaN material properties [11].

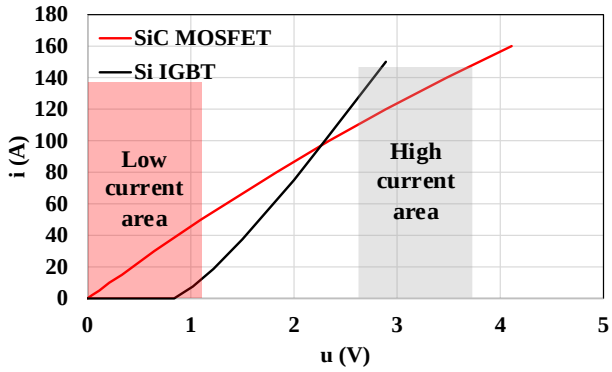


Figure 1-2 Conduction loss comparison between SiC MOSFET and Si IGBT.

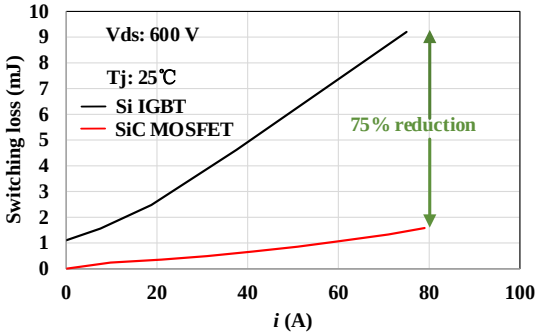


Figure 1-3 Switching loss comparison between SiC MOSFET and Si IGBT.

Si IGBT and SiC MOSFET are made and depicted from Figure 1-2 to Figure 1-4. In Figure 1-2 and Figure 1-3, the comparisons are made based on the selected devices Infineon 1200 V / 75 A Si IGBT IKY75N120CH3 [12] and Wolfspeed 1200 V / 74 A SiC MOSFET C3M0021120K [13]. The data used in the comparison is from the manufacturer's datasheets.

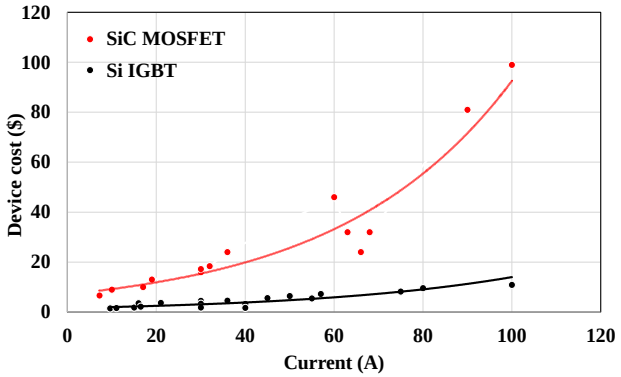
As shown in Figure 1-2, at the low current area, the SiC MOSFET has significant advantage in conduction characteristics. This is because that SiC MOSFET can be seen as an on-state resistance during its conduction, whereas, the Si IGBT has a threshold voltage. In the high current area, the Si IGBT has advantage over the SiC MOSFET. The

conductivity modulation effect of Si IGBT contributes to a very low conduction voltage for the Si IGBT at high current. The low conduction voltage increases the overload capability for the Si IGBT. Through the comparison, it is noted that the SiC MOSFET and Si IGBT has complementary conduction characteristics: SiC MOSFET has advantage in conducting low current while Si IGBT has advantage in conducting high current.

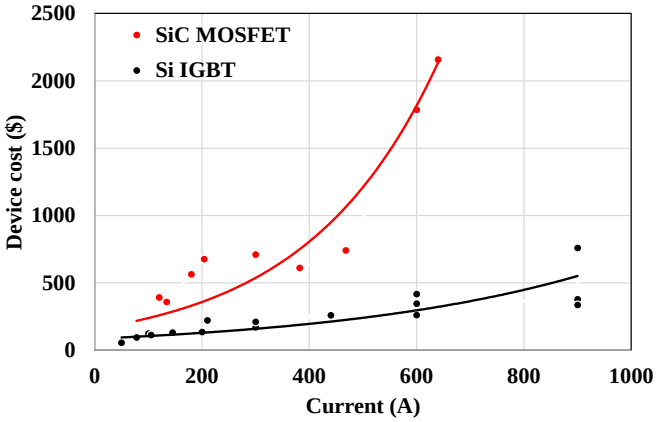
In Figure 1-3, the switching loss of selected Si IGBT and SiC MOSFET are compared. It is shown that compared to the Si IGBT, the SiC MOSFET has significantly lower switching loss. With the increase of load current, the switching loss difference increases. At the load current of 80 A, the Si IGBT has a 75% higher switching loss. Through the comparison, another complementary characteristic on the switching loss is found.

The device cost comparison between the Si IGBT and SiC MOSFET for the discrete devices and power modules are made and depicted in Figure 1-4 (a) and (b). The device cost is from Digi-key on a bulk order more than 2000 units. The 1.2 kV SiC MOSFET devices include the off-the-shelf products from Wolfpeed, Rohm, and Onsemi. The Si IGBT devices include the products from Infineon and IXYS. It is shown that the SiC MOSFET has a much higher device cost both on discrete devices and power modules. With the increase of current rating, the device cost increases significantly. It is noted that the third complementary characteristic is on the device cost.

Based on the above analysis, the Si IGBT and SiC MOSFET has complementary characteristics on the conduction loss, switching loss, and the device cost. It is nature to consider combing the advantages of the two types of semiconductor devices. Thus, the Si/SiC HyS is proposed. As illustrated in Figure 1-5, the Si/SiC HyS consists of a high



(a) Discrete device cost comparison



(b) Power module cost comparison

Figure 1-4 1.2kV device cost comparison between the Si IGBT and SiC MOSFET.

current rated Si IGBT and low current rated SiC MOSFET connected in parallel. The Si/SiC HyS has the following advantages than the individual Si IGBT or SiC MOSFET:

1) Better conduction characteristics than the pure Si IGBT or SiC MOSFET. Compared to the individual Si IGBT, the Si/SiC HyS has no threshold voltage due to the paralleled SiC MOSFET, thus having low conduction voltage at low current. At high current, compared to the individual SiC MOSFET, the Si/SiC HyS has higher current carrying capability and lower conduction voltage due to the paralleled Si IGBT. Thereby, the overload capability is improved.

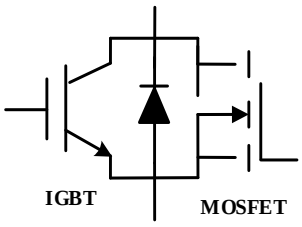


Figure 1-5 Si/SiC HyS configuration.

2) Lower switching loss and higher switching frequency than the pure Si IGBT. Because of the paralleled configuration, the SiC MOSFET can help the Si IGBT to realize zero voltage switching by turning on first and turning off last in every switching cycle. Thus, the switching loss of Si IGBT is significantly reduced. The switching loss and switching frequency of the Si/SiC HyS is significantly improved.
3) Lower device cost than the pure SiC MOSFET. In the Si/SiC HyS configuration, only a small current rated SiC MOSFET is needed. So, the device cost for the Si/SiC HyS is reduced compared to a full current rated SiC MOSFET.

Through the analysis and comparison, the motivation to investigate the Si/SiC HyS and its application in power electronic converters is: a cost-effective way to realize high efficiency and high power density for power electronic systems.

1.2 Development of Semiconductor Devices

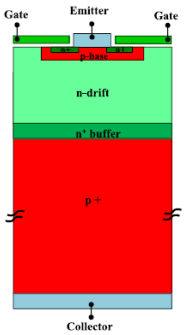
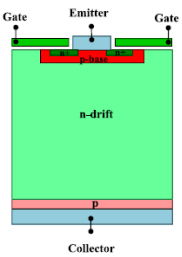
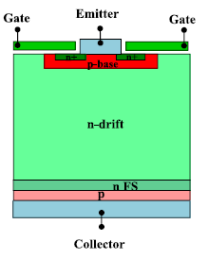
From the point of first semiconductor devices crystal detector was developed by Karl Ferdinand Braun at 1874, different kinds of semiconductor device, such as the transistors, GTR, GTO, MOSFET, and IGBT has been developed and used in the power electronics systems. In this part, the development of the most widely used semiconductor device Si IGBT and the emerging SiC MOSFET are introduced.

1.2.1 Development of Si IGBT

The Si IGBT, as a superior alternative to bipolar power transistors in 1980s, has been widely applied to most power electronic applications, especially medium and high-power scenarios, such as the ac drive, UPS, renewable energy systems [14], [15]. Table 1-1 shows the three design concepts of Si IGBT technology between PT, and NPT IGBT and FS IGBT [15], [16].

The early stage of Si IGBT technology was the PT-IGBT, the collector is highly doped with P+ layer which introduces the PN junction injection mechanism. The

Table 1-1 Comparison of the different IGBT concepts [15], [16]

	PT-IGBT	NPT-IGBT	FS-IGBT
p-emitter	very high efficient	low efficient	low efficient
n-draft	thin	medium	thin
additional n-layer	buffer layer =highly doped to reduce the very high emitter efficiency to stop the electrical field low (lifetime killing)	no	filed stop layer = weakly doped to stop only the electrical field
carrier lifetime	low (lifetime killing)	high	high
structure			

conduction voltage is greatly reduced compared to the VDMOS. But PT-IGBT has a large tail current which is caused by the long recovery of holes and electrons restored in the N-region. Thus, the turn-off loss is greatly increased. The NPT-IGBT, which is lightly doped and only has the P layer, reduced the tail current when IGBT is turned off. Thereby the turn-off loss is reduced. Compared to the PT-IGBT, the NPT-IGBT is more thermally stable. The turn-off loss is less temperature sensitive and its on-state resistance voltage is strongly positive which makes it suitable for parallel operation for high power applications. However, the NPT-IGBT has a thick n-drift layer which increases conduction voltage in high voltage devices. This is the main disadvantage of the NPT-IGBT. The FS-IGBT was invented by *Laska et al*. [15] around the year of 2000. The thickness of n-drift region is reduced, and a thin field stop layer was added to stop the electric field and increase the voltage blocking capability. As a result of this, the forward voltage can be decreased.

Currently, the Si IGBT products has been manufactured from 600 V to 6500 V for different applications. The current level is from several amperes to 3600 A. The related off-the-shelf products are shown in Figure 1-6. With the increased requirement for the

(a) Infineon 6500 V / 750 A Si IGBT power module (FZ750R65KE3NOSA1)

(b) Infineon 1200 V / 3600 A Si IGBT power module (FZ3600R12HP4HOSA2)

Figure 1-6 High power rating Si IGBT modules.

power electronic system on the power density and efficiency, the Si IGBTs gradually fail to meet the new requirements. The main limit for the Si IGBT is the high switching loss. When the Si IGBT is used in the high frequency, not only the converter efficiency will

drop but introduce thermal unstable issue [17]. To reduce the switching loss and increase the Si IGBT switching frequency, the researchers proposed different soft-switching circuits or PWM methods for the Si IGBT-based converter [18]-[26], but the soft switching circuits will increase the number of passive components that result in higher system complexity, weight, and volume also reduce the reliability. The PWM methods that have the soft-switching capability is only suitable for specific topologies and will increase the complexity of control side. Thereby, the use of soft switching methods to increase the Si IGBT switching frequency is limited.

1.2.2 Development of SiC MOSFET

The SiC material, which is one of the third-generation semiconductor materials, was suggested to use in the power devices such as MOSFET in 1989 [27]. Since the first 750 V 6H-SiC-MOSFET and 1100 V 4H-SiC-MOSFET were published in 1997 [28],[29], the research about the SiC MOSFET to reduce the on-resistance while a high blocking voltage start to be widely investigated. Compared to the Si IGBT, the SiC MOSFET has the following advantages [30], [31].

1) SiC MOSFET has faster switching speed and thus having much lower switching loss. The switching frequency of SiC MOSFET can achieve up to several megahertz.
2) The body diode of SiC MOSFET has neglectable reverse recovery current than the antiparallel diode of Si IGBT. The recovery loss and the high-frequency noise caused by the recovery process are significantly reduced.
3) The SiC MOSFET has higher operation temperature limit. This makes it suitable for high temperature applications.

4) The SiC MOSFET has higher breakdown voltage due to the wide bandgap of SiC material.

Currently, although the SiC MOSFET and the SiC MOSFET-based converters has so many advantages over the conventional Si IGBT solutions, the SiC MOSFET still cannot replace the Si IGBT in the high power, high voltage applications. The main obstacles to realize such transformation are listed as follows.

1) The current handling capability of commercially available SiC MOSFET is still lower than the Si IGBT. In the high-power applications, several SiC MOSFETs need to be connected in parallel to handle the high load current.
2) The device cost for SiC MOSFET is still much higher than the Si IGBT, it can be seen from Figure 1-4 that with the increase of current rating, the device cost for SiC MOSFET increases drastically. A full SiC MOSFT-based power electronic system will significantly increase the system cost.
3) The fast-switching characteristic of SiC MOSFET will cause severe EMI problem. The SiC MOSFET-based power electric systems need to pay more attention to the EMI suppression. This increases the design difficulty of the power electronic system.

1.2.3 Development of Hybrid Devices

As shown in the roadmap of hybrid device Figure 1-7, the concept of "hybrid device" is not new. In 1980s, several hybrid concepts which utilize MOS and bipolar device are proposed [32]. The characteristics of hybrid device was tested and presented. In the 1990s, the Si IGBT and Si MOSFET hybrid switch was utilized in power converters. From 1993 to 1997, some research groups implemented the Si IGBT and Si MOSFET hybrid switch-

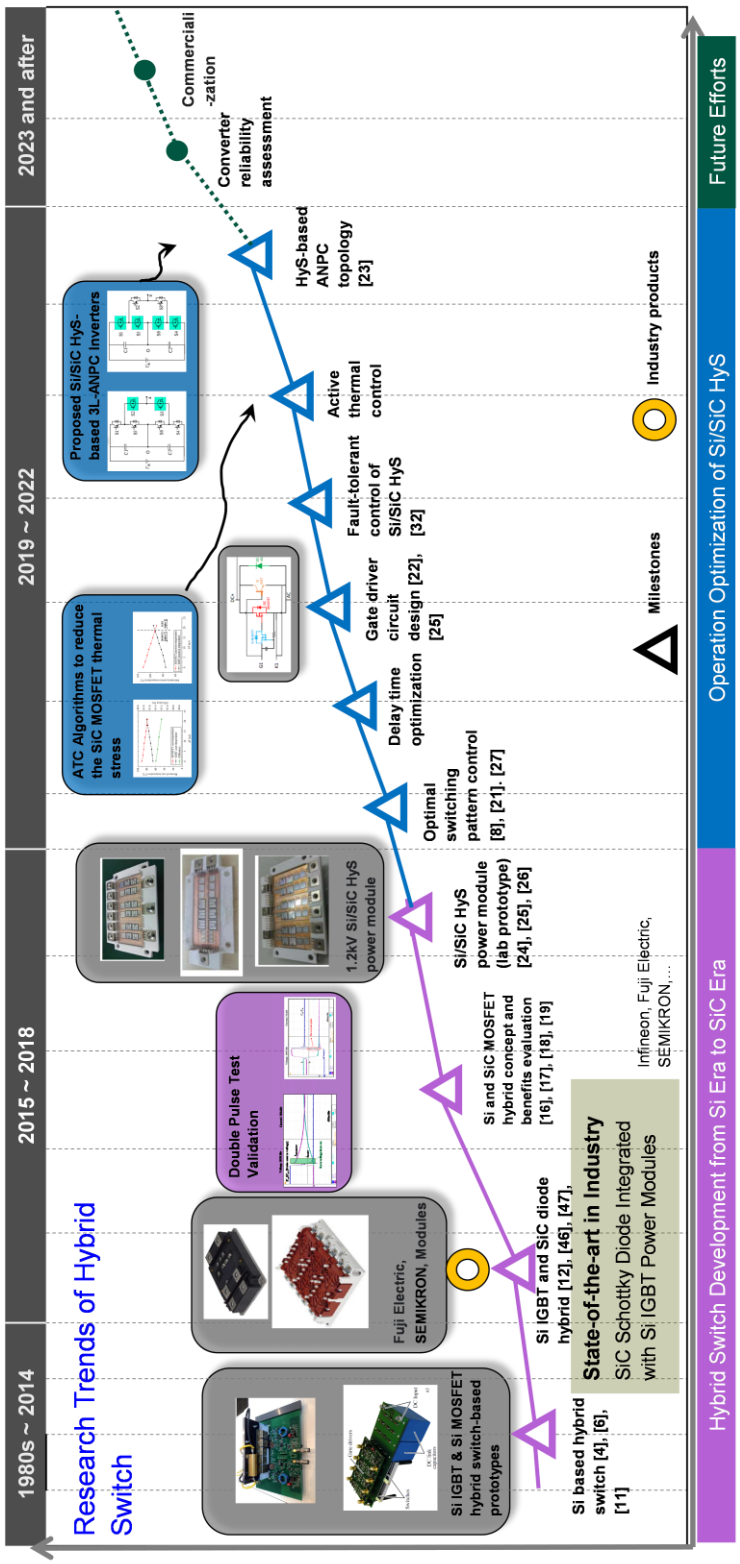


Figure 1-7 Roadmap of the hybrid switch.

based power converters to validate the benefits of the hybrid concept [33], [34]. Later, the Si IGBT and Si MOSFET hybrid switch-based converter prototypes were implemented for high-frequency power electronic systems, such as resonant converters and motor drives [35]-[39]. Some research groups also tried to make hybrid device power modules for better electric performance [38]-[40]. But the main limit of Si-based hybrid devices is the low device voltage of Si MOSFET. So, most of the Si IGBT and Si MOSFET hybrid switch is only used in low voltage applications. The emerging commercially available SiC device has lower on-resistance with higher device voltage. Some researchers integrated the SiC diode with the Si IGBT for better device reverse conduction characteristic [41]. Some semiconductor device manufactures released their products that have the Si IGBT and SiC diode packaged together [42], [43]. Then, the Si IGBT and SiC MOSFET hybrid switch was proposed with the configuration of high current-rated Si IGBT in parallel with the low current-rated SiC MOSFET [44]. Si/SiC HyS-based converter prototypes and related research topics start to be investigated.

1.3 Literature Review

1.3.1 Gate Driving Redundance

Due to the different device characteristics between the Si IGBT and SiC MOSFET, the gate driving sequence of the Si/SiC is highly related to the device's performance. Based on the switching sequence of Si IGBT and SiC MOSFET, there are six gate driving sequence combinations can be applied to the Si/SiC HyS. The six gate driving sequences are depicted in Figure 1-8. For the switching sequences (a) to (d), both Si IGBT and SiC MOSFET will be turned on to conduct current and produce the conduction losses. But only the earliest turned-on device will produce the switching losses. The other device will be

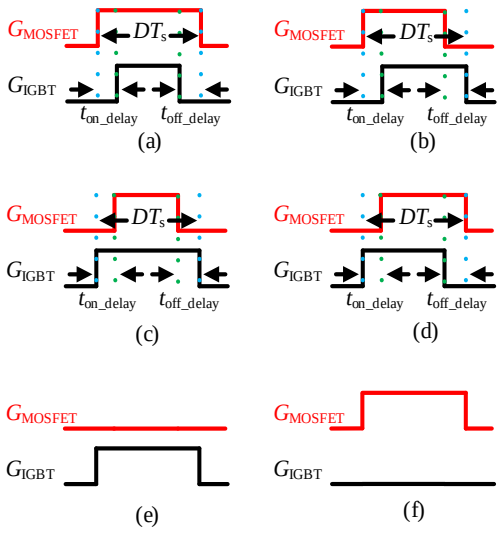


Figure 1-8 Gate driving sequences for the Si/SiC HyS.

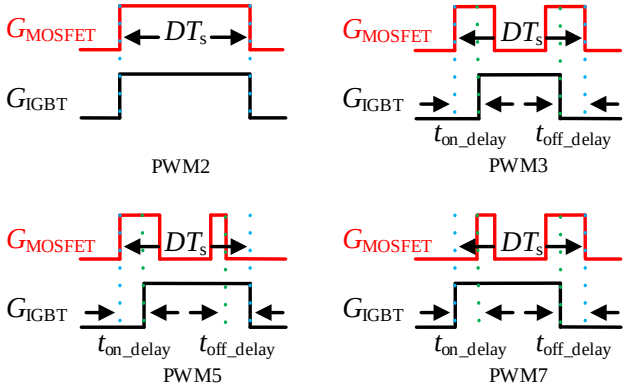


Figure 1-9 Gate driving sequences proposed in [51].

turned on by ZVS. For the switching sequences of (e) and (f), only one device is turned on and produce all the semiconductor losses.

In literature [45] and [50], the investigations of gate driving sequences are mainly focused on the switching sequences (a) and (c), it is concluded that compared with the pure Si IGBT-based converter, the Si/SiC HyS-based converter can achieve higher switching frequency, higher efficiency, and higher power density under the gate driving sequence (a). Compared to the pure SiC solution, in addition to the device cost reduction, the Si/SiC

HyS-based converter has larger overload capability under the gate driving sequence (c) due to the IGBT's better conduction characteristics at large current condition.

In article [51], the research group from Zhejiang University utilized the Si/SiC HyS in the three-level T-type NPC grid inverter. Seven PWM strategies are studied and compared regarding to the inverter efficiency. In addition to the six gate driving sequencies depicted in Figure 1-8, four PWM strategies which are shown in Figure 1-9 are proposed. All the PWM strategies are tested based on a 20kW grid inverter with a 1:2.4 current ratio for the Si and SiC devices. The experimental results show that the gate driving sequence of SiC MOSFET turns-on first and turns-off last is preferred for the efficiency advantage in heavy load, while Si IGBT turns-on first and turn-off first are better for the efficiency advantage in light load and half-load. This conclusion is interesting because it is shown that the Si IGBT turns-on first have larger efficiency advantage in the partial load condition. But all the conclusions are based on the selected topology, turn-on delay time, turn-off delay time, and device current ratings in the article [51]. A different topology, delay time on the gate side, or device current ratings may cause different result. But, in addition to the efficiency improvement validation presented, the proposed PWM3, PWM5, and PWM7 strategies in this work also show the redundancy in designing the SiC MOSFET conduction time and its potential effects on the inverter efficiency change.

The research group from Hunan University presented a variable-frequency current-dependent switching strategy for the inverter efficiency and SiC MOSFET thermal stress trade-off in [52]. Gate driving sequences (a) and (c) are selected as the candidates. When the inverter operates at partial load condition, only gate driving sequence (a) is used. In a sinusoidal current period, with the increase of load current, the switching frequency

changes. At the peak current, the switching frequency is 26kHz. When the inverter operates at the full load condition, gate driving sequences (a) and (c) are utilized together to reduce the thermal stress of SiC MOSFET. The novel variable-frequency current-dependent switching strategy aims at improving the converter reliability of the Si/SiC HyS without reducing the inverter efficiency.

1.3.2 Current Ratio Optimization

In the previous introduction, it is shown that the Si/SiC HyS has great advantage in both device characteristics and device cost. But, to fully utilize those benefits, it is also important to select a proper current ratio between Si IGBT and SiC MOSFET. A lower Si/SiC current ratio will result a higher device cost for the SiC device. A higher Si/SiC current ratio might bring reliability issues because of the heavy thermal stress on the SiC MOSFET. Thus, the current ratio optimization is important for the system design.

Many research groups have investigated the current ratio optimization for a cost-effective, efficient, and reliable Si/SiC HyS pair [49], [53], [54]. The optimization process in those literatures can be summarized in Figure 1-10. The first step of the optimization process is to calculate the total current rating and voltage class of the Si/SiC HyS for the specific applications. Then, the next step is to select the Si IGBTs and SiC MOSFETs with different current ratings based on the commercially available devices. After this step, many Si/SiC HyS pairs with different Si and SiC current ratios can be obtained. The third step is the SiC MOSFET junction temperature estimation for each candidate pair. In this step, the power loss models and thermal models at the device level and system level are needed. The power loss model and thermal model should be based on the specific application or converter topology and operating conditions. Once the thermal profile, power loss model,

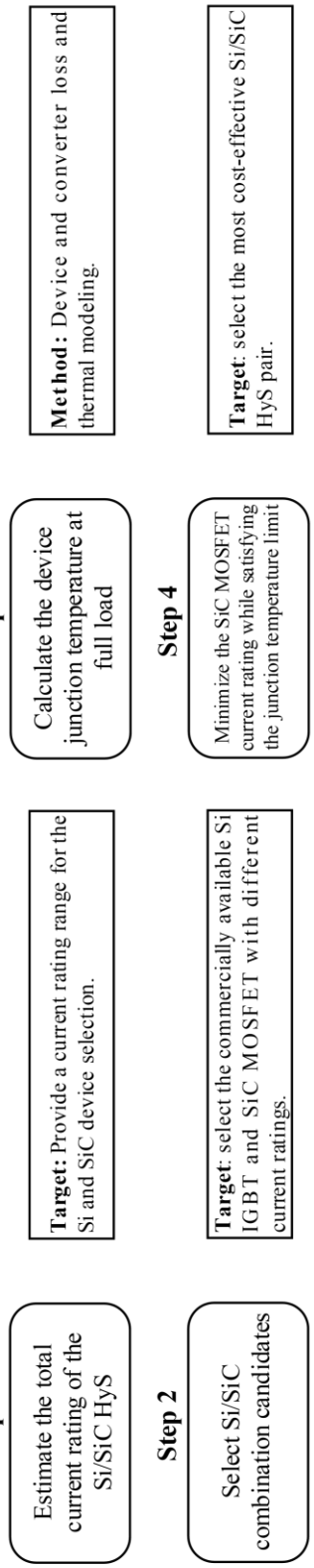


Figure 1-10 Current ratio optimization process summary.

and thermal model are obtained, the junction temperatures of SiC MOSFETs for each combination candidate can be estimated. The final step is to select the most cost-effective Si/SiC HyS combination that satisfies the junction temperature limit. Then, a cost-effective and efficient Si/SiC HyS pare for the specific application is obtained.

This strategy can provide a recommendation on how to form a Si/SiC HyS for a specific application. To achieve a more accurate SiC MOSFET junction temperature estimation, accurate power loss and thermal models are very important. But, currently, due to the lack of high resolution and high frame rate thermal camera and opened Si/SiC HyS module in most research groups, the accuracy of this strategy cannot be validated by the direct junction temperature measurement. It is still an electric and thermal model-based open loop way. From the engineering perspective, to avoid a failure on the Si/SiC HyS selection result from a SiC MOSFET overheat failure, a proper current rating margin of SiC MOSFET or a stricter SiC MOSFET junction temperature limit should be considered when designing the Si/SiC HyS.

1.3.3 Inverter Prototypes

With more and more researchers being attracted to the Si/SiC HyS, several Si/SiC HyS-based power converter prototypes were implemented in the lab. The corresponding research groups and their prototype information are summarized in Table 1-2.

The research group from General Electric (GE) utilized 1:3 current ratio Si/SiC HyS which is formed by one 1200 V / 10 A SiC MOSFET and one 1200 V / 30 A Si IGBT in a 15kW H-bridge inverter [50]. The test was conducted under 600 V Dc voltage and 10 kHz switching frequency and realized a 0.71% inverter efficiency improvement at 25%

Table 1-2 Efficiency performance summarize of Si/SiC HyS-based prototypes

Research group	Topology	Power rating	Switching frequency	Efficiency improvement
GE [50]	H-bridge	15kW	10kHz	0.7%@3.8kW
NUAA [56]	Buck	4kW	50kHz	7.5%@0.8kW, 2.5%@4kW
Hunan University [55]	Boost	9kW	20kHz	0.9%@1kW, 0.8%@4kW
University of Arkansas [54]	A-NPC	20kW	50kHz	0.5%@1kW, 1.3%@20kW
UNC Charlotte [57]	T-NPC	2.5kW	40kHz	4.9%@0.25kW, 2%@2.5kW

load condition compared to the full Si IGBT solution. At full load, the efficiency improvement is not obvious. In Nanjing University of Aeronautics and Astronautics, the researcher developed a 4 kW buck converter using the Si/SiC HyS [56]. The Si/SiC HyS was formed by a 1200 V / 25 A Si IGBT. The efficiency testing shows that compared to the conventional Si IGBT-based buck converter, the converter efficiency is improved by 7.5% at 20% load and 2.5% at full load. It is noted that at light load condition, the Si/SiC HyS solution has much higher efficiency since the Si/SiC HyS has better performance not only on the switching loss but also the conduction loss. In literature [55], Dr. Jun Wang and his group investigated the efficiency improvement by the Si/SiC HyS which is formed by a 1200 V / 12 A SiC MOSFET and a 1200 V / 40 A Si IGBT on a boost converter. The boost converter was tested to have a 0.9% and 0.8% efficiency improvement at 1kW and 4kW output power respectively. In University of Arkansas, Dr. Alan Mantooth and his

research group presented a Si/SiC HyS-based 3L-ANPC inverter which utilized the 1200 V / 22 A SiC MOSFET and the 600 V / 30 A Si IGBT as the combination of Si/SiC HyS. Only two Si/SiC HyS are used for each inverter leg, the other switches use the 600 V / 50 A Si IGBT. The testing results show that 0.5% and 1.3% inverter efficiency improvement can be achieved at the switching frequency of 50kHz [54]. The researchers in UNC Charlotte shows a Si/SiC HyS-based 3L-TNPC inverter in [57]. The hybrid switch was formed by a 1200 V / 12 A SiC MOSFET and a 1200 V / 15 A Si IGBT. The inverter efficiency was tested and compared with a full Si IGBT-based inverter. The results show that the inverter efficiency was improved by 4.9% and 2% at 10% load and full load respectively.

The prototypes from different research groups have validated the efficiency improvement bring by the Si/SiC HyS. The testing results shows a very promising future for the power converters to achieve high converter efficiency at a cost-effective way.

1.3.4 Gate Driving Circuit and Power Module Design

With the increasing popularity of the Si/SiC HyS, more and more researchers are attracted to the electric and thermal performance optimization for the Si/SiC HyS. Power module prototypes with very low parasitic loop inductance are implemented in the labs and presented in the related papers [58]-[60]. 1700 V / 300 A half bridge modules, as shown in Figure 1-11, consists of two Si IGBT dies and one SiC MOSFET die with a Si/SiC current ratio of 6:1 at each switch position was proposed in [58]. A wire bond-less, high-reliability silver clips are employed for the interactions in the module. 12.38nH overall power loop inductance is achieved. In the design presented in [58], a novel metal-encapsulated thermal pyrolytic graphite baseplate is used to decouple the thermal interaction between the Si dies

Figure 1-11 The fabricated power module in [58].

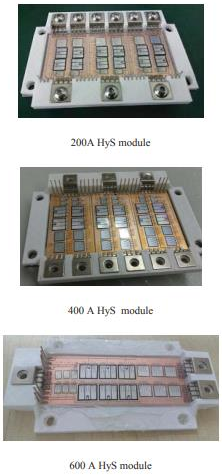


Figure 1-12 1200 V, 200 A / 400 A / 600 A three phase SiC/Si HyS modules in [59].

and SiC die. This design allows junction temperature of the SiC die to be higher than the Si dies to fully utilize the high temperature operation characteristics of SiC. In literature [59], 1200 V / 200 A / 400 A / 600 A Si/SiC HyS modules, as shown in Figure 1-12, are prototyped, and tested in the lab. Just like the hybrid switch formed by discrete devices, the power modules mentioned above need separate gate driver circuits for the Si IGBT and SiC MOSFET. But in literature [60], a novel gate driver circuit, as shown in Figure 1-13, was proposed to use only one gate driver circuit for the Si/SiC HyS. The RC components and low voltage (LV) MOSFET are utilized to realize turn-off delay time in an analog way. The gate driving circuit was integrated with a 1200 V / 200 A Si/SiC HyS power module as shown in Figure 1-14.

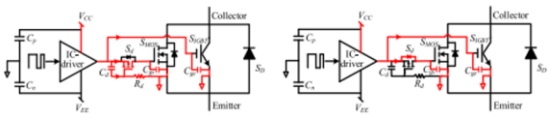


Figure 1-13 Turn-on current paths of the proposed single gate driver circuit [60].

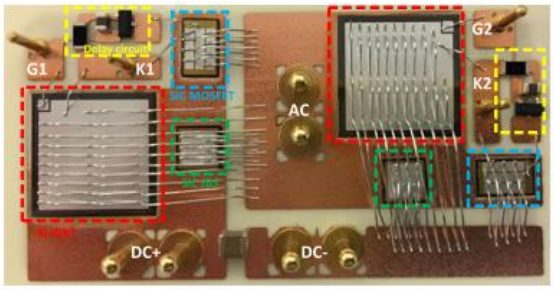


Figure 1-14 Packaged 1200 V / 200 A Si/SiC HyS half-bridge module with the gate driver circuit integrated [60].

1.4 Summary

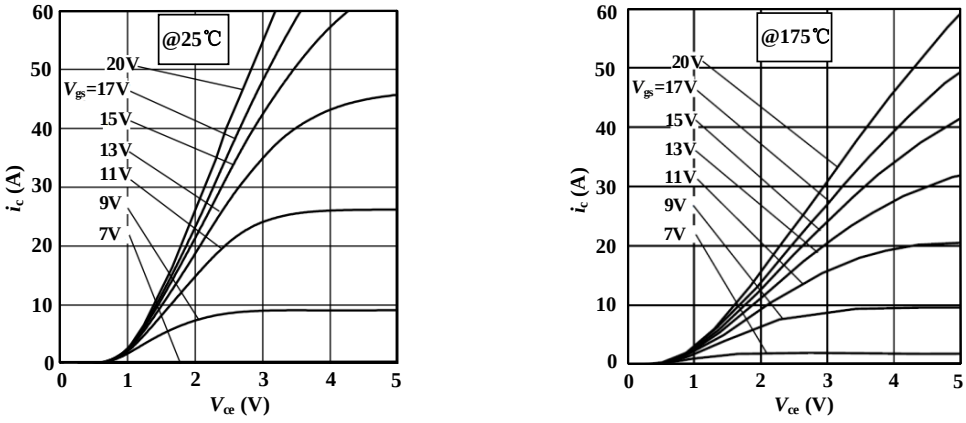
In this chapter, the motivation of proposing the Si/SiC HyS is introduced. By using the parallel connection of a high current rated Si IGBT and a low current rated SiC MOSFET, the low cost and high overload capability advantages of Si IGBT are combined with the SiC MOSFET's advantage of low switching loss and offering a transformative way to provide high efficiency and low-cost solution for power electronic systems. A literature review on the Si/SiC HyS is presented as well as the roadmap of the hybrid switch which shows the development of the hybrid switch from the Si era to the SiC era. The prospect and potential of this technology from the lab to the industry is depicted.

CHAPTER 2: CHARACTERIZATION OF HYBRID SWITCH

Different from the individual Si IGBT or SiC MOSFET device, the Si/SiC HyS is in a parallel configuration. So, its conduction and switching characteristics are different from any of the individual devices. In this chapter, the conduction and switching characteristics between Si IGBT and SiC MOSFET are compared. Then, the characteristics of Si/SiC HyS is introduced. The devices selected for the comparison are from Infineon 1200 V / 30 A @25ºC Si IGBT IKW15N120T2 and Wolfspeed 1200 V / 32 A @25ºC SiC MOSFET C3M0075120D. The data for each device is from the manufacturer's datasheets [12], [13].

2.1 Conduction Characteristic Comparison of Si IGBT and SiC MOSFET

Figure 2-1 shows the conduction characteristics of the Si IGBT. It is shown that Si IGBT has a threshold voltage which is around 0.7 V at 25℃. The on-resistance is negatively related to the gate voltage. When the current is low (0~3 A), the Si IGBT forward voltage shows a negative temperature coefficient. This is mainly because the threshold voltage reduces with the increase of temperature. When the current is higher, the Si IGBT forward

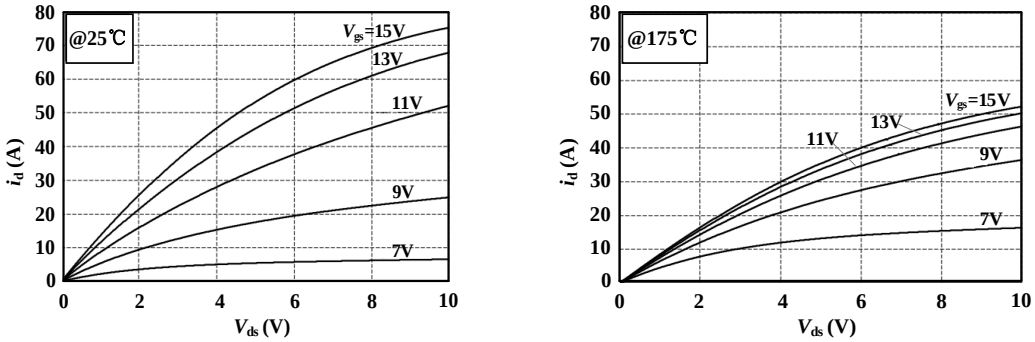


(a) At 25℃ (b) At 175℃

Figure 2-1 Conduction characteristic of Si IGBT IKW15N120T2 [12].

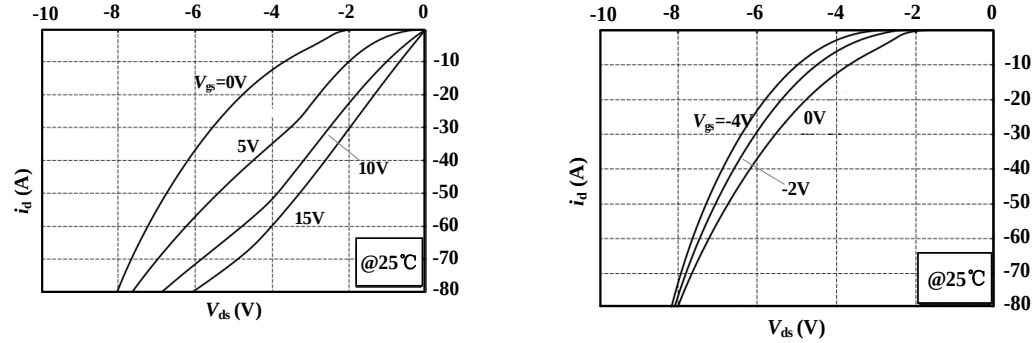
voltage shows a positive temperature coefficient. This characteristic makes the Si IGBT easy to operate in parallel. It is also noted that the Si IGBT can only conduct the positive current which means that the load current can only flow from the collector to the emitter. The current cannot flow reversely.

Different from the Si IGBT, when the SiC MOSFET gate is biased "high", the SiC MOSFET can conduct the current in both directions. The conduction characteristic of SiC MOSFET is shown in Figure 2-2. It is noted that the SiC MOSFET channel on-resistance decrease with the increase of gate bias voltage. The SiC MOSFET on-resistance also shows a positive temperature coefficient. Figure 2-3 shows the reverse conduction characteristics.



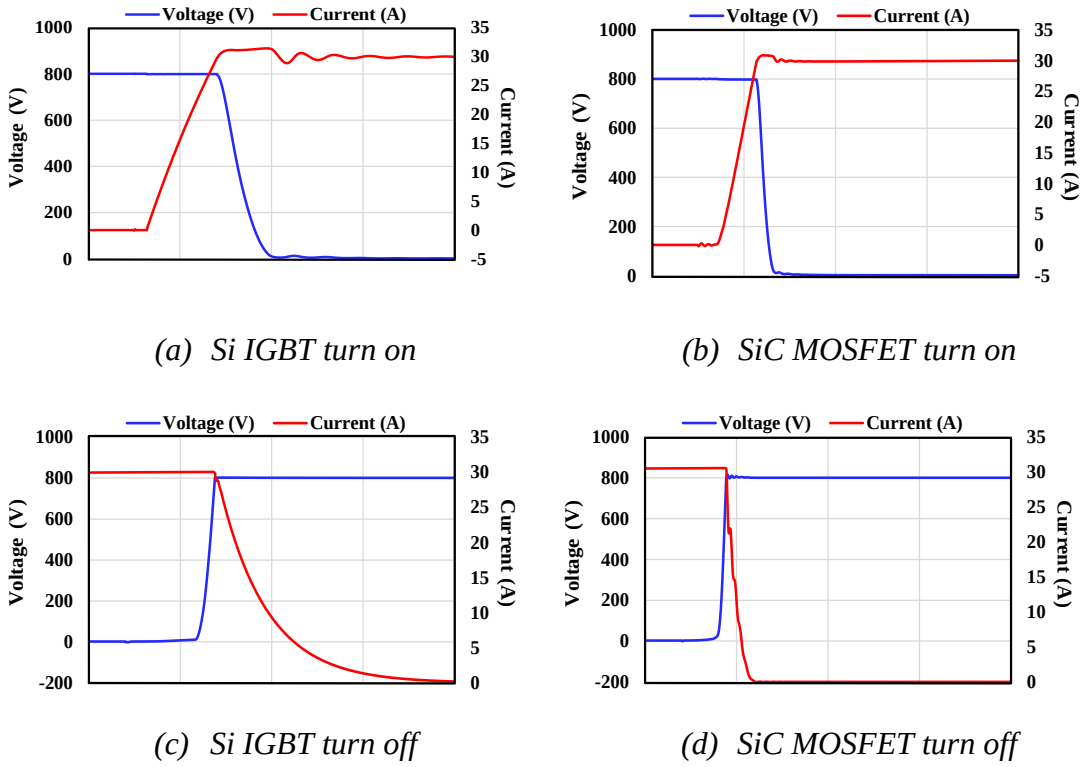
(a) At 25°C (b) At 175°C

Figure 2-2 Conduction characteristic of SiC MOSFET C3M0075120D [13]



(a) Third quadrant (c) Body diode

Figure 2-3 Reverse conduction characteristic of SiC MOSFET C3M0075120D [13.]



(a) Si IGBT turn on

(b) SiC MOSFET turn on

(c) Si IGBT turn off

(d) SiC MOSFET turn off

Figure 2-4 Typical switching waveforms of Si IGBT and SiC MOSFET.

It is noted that the SiC MOSFET can always conduct current reversely no matter the gate voltage is positive, zero, or negative. When the gate is biased “positive”, the body diode and the MOSFET channel both will conduct current. When the gate is biased “negative”, that MOSFET channel will be turned off, while the body diode conduction path still exists. So, it is impossible to “turn off” the SiC MOSFET in both directions. In some applications such as the solid-state circuit breakers that needs to control the SiC MOSFET from both directions, the common source connection of SiC MOSFETs is needed.

2.2 Switching Characteristic Comparison of Si IGBT and SiC MOSFET

The typical switching waveforms of Si IGBT and SiC MOSFET is shown in Figure 2-4. Through the comparison, it is shown that the SiC MOSFET has faster switching speed than the Si IGBT. In the turn on transient, the input capacitor of Si IGBT is larger than the

SiC MOSFET, so the SiC MOSFET will respond to the gate signal faster than the Si IGBT and smaller turn on loss is produced. In the turn off transient, the fast-switching advantage of SiC MOSFET becomes more significant. Not only the larger input capacitor reduces the turn off speed of Si IGBT, the tail current which is caused by the minority carriers recombination process will also increase the turn off time of Si IGBT. Thereby increases the turn off loss significantly.

2.3 Conduction Characteristics of Hybrid Switch

In order to combine the advantages of Si IGBT and SiC MOSFET, the Si/SiC HyS is proposed. In this section, the conduction and switching characteristic of Si/SiC HyS is investigated and introduced.

2.3.1 Dynamic Current Sharing Process

Different from the pure Si IGBT and SiC MOSFET, there is a dynamic current sharing process after the Si IGBT and SiC MOSFET being turned on. The dynamic current sharing process under different power loop parasitic inductance ($L_c + L_e + L_d + L_s$, shown in Figure 2-5) is depicted in Figure 2-6. With the increase of the parasitic inductance, the

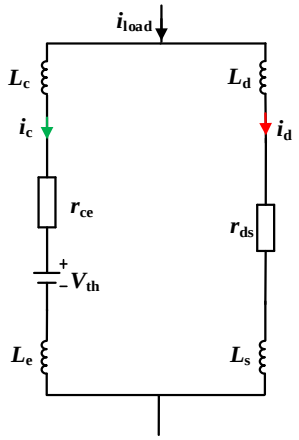


Figure 2-5 Si/SiC HyS equivalent conduction model with parasitic inductance.

speed of dynamic current sharing process decreases. It is also noted that the influence of external parasitic inductance on the current sharing speed is not significant.

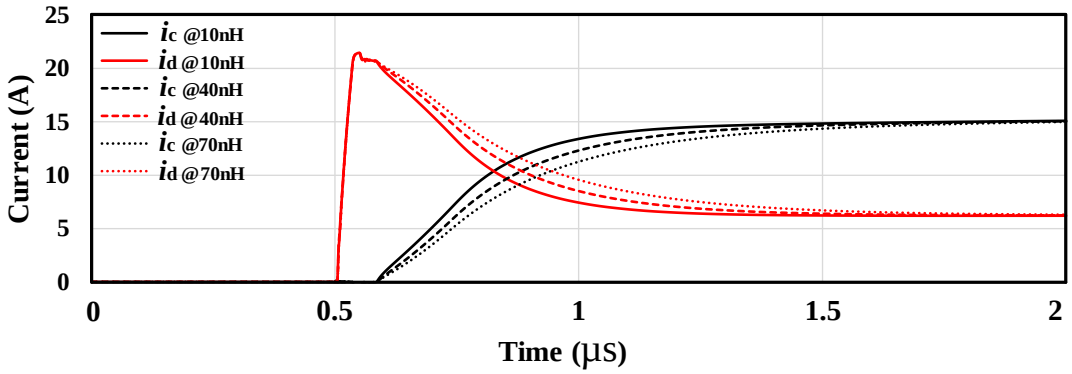


Figure 2-6 The dynamic current sharing process under different power loop parasitic inductance.

2.3.2 Steady State Current Sharing

In the Si/SiC HyS steady state conducting period, the Si IGBT and SiC MOSFET share the load current and have the same forward voltage. The steady state conduction model is depicted in Figure 2-7. The SiC MOSFET can be modeled as an on-resistance r_{ds} and the Si IGBT can be modeled as an on-resistance r_{ce} in series with a voltage source which represents the threshold voltage V_{th}. The idea diode prevents the circulation current.

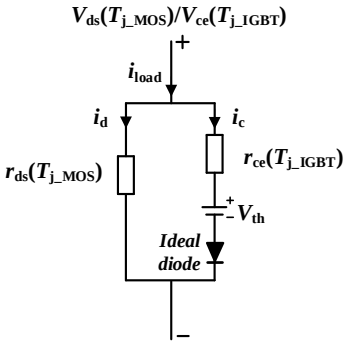


Figure 2-7 Steady state conduction model of Si/SiC HyS.

Based on the steady state conduction model, the conduction voltage of the Si/SiC HyS can be expressed by:

$$V_{ce}(T_{j\_IGBT}) = i_c \times r_{ce}(T_{j\_IGBT}) + V_{th}(T_{j\_IGBT})$$
$$V_{ds}(T_{j\_MOS}) = i_d \times r_{ds}(T_{j\_MOS}) \quad (2\text{-}1)$$

and

$$V_{ds}(T_{j\_MOS}) = V_{ce}(T_{j\_IGBT})$$
$$i_{load} = i_d + i_c \quad (2\text{-}2)$$

Where $V_{ds}(T_{j\_MOS})$ and $V_{ce}(T_{j\_IGBT})$ are the conduction voltage of SiC MOSFET and Si IGBT at their junction temperature.

The on-resistance of Si IGBT and SiC MOSFET and the threshold voltage of Si IGBT are influenced by the device junction temperature. Considering the device junction temperature, the conduction model parameters can be expressed by:

$$r_{ce}(T_{j\_IGBT}) = r_{ce}(25^oC) + \alpha(T_{j\_IGBT} - 25)$$
$$r_{ds}(T_{j\_MOS}) = r_{ds}(25^oC) + \beta(T_{j\_MOS} - 25) \quad (2\text{-}3)$$

Where $r_{ce}(25℃)$ and $r_{ds}(25℃)$ represent the values of the parameters at 25℃. α, β, and η are their respective temperature coefficients. Their values can be calculated by:

$$\alpha \text{ or } \beta = \frac{r(T_{j\_max}) - r(T_{j\_min})}{T_{j\_max} - T_{j\_min}} \quad (2\text{-}4)$$

Where T_{j_max} and T_{j_min} are the maximum and minimum device junction temperature. Those values can be obtained from the manufacturer's datasheets. Since the on resistance of paralleled Si IGBT and SiC MOSFET have positive temperature coefficient, α and β have positive values.

Considering the device junction temperature, the load current shared by Si IGBT and SiC MOSFET can be expressed as:

$$\begin{aligned} i_{\mathrm{c}} &= \frac{i_{\mathrm{load}} r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}}) - V_{\mathrm{th}}}{r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}}) + r_{\mathrm{ce}}(T_{\mathrm{j\_IGBT}})} \\ i_{\mathrm{d}} &= \frac{i_{\mathrm{load}} r_{\mathrm{ce}}(T_{\mathrm{j\_IGBT}}) + V_{\mathrm{th}}}{r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}}) + r_{\mathrm{ce}}(T_{\mathrm{j\_IGBT}})} \end{aligned} \tag{2-5}$$

When the load current is too small to turn on the Si IGBT, $i_{\mathrm{c}}=0$, and $i_{\mathrm{d}}=i_{\mathrm{laod}}$. So, the steady state current sharing model Si/SiC HyS for full current range of is:

$$i_{\mathrm{c}} = \begin{cases} 0 & , i_{\mathrm{load}} < \dfrac{V_{\mathrm{th}}}{r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}})} \\ \dfrac{i_{\mathrm{load}} r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}}) - V_{\mathrm{th}}}{r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}}) + r_{\mathrm{ce}}(T_{\mathrm{j\_IGBT}})} & , i_{\mathrm{load}} > \dfrac{V_{\mathrm{th}}}{r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}})} \end{cases} \tag{2-6}$$

$$i_{\mathrm{d}} = \begin{cases} i_{\mathrm{load}} & , i_{\mathrm{load}} < \dfrac{V_{\mathrm{th}}}{r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}})} \\ \dfrac{i_{\mathrm{load}} r_{\mathrm{ce}}(T_{\mathrm{j\_IGBT}}) + V_{\mathrm{th}}}{r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}}) + r_{\mathrm{ce}}(T_{\mathrm{j\_IGBT}})} & , i_{\mathrm{load}} > \dfrac{V_{\mathrm{th}}}{r_{\mathrm{ds}}(T_{\mathrm{j\_MOS}})} \end{cases} \tag{2-7}$$

Equations (2-6) and (2-7) are the steady state current sharing model of the Si/SiC HyS in the forward conduction. When the Si/SiC HyS reversely conduct the current, the load current will be shared by the Si IGBT antiparallel diode and the SiC MOSFET. The SiC MOSFET can still be equivalent to an on-resistance and the diode can be equivalent to an on-resistance in series with a voltage source which represent the threshold voltage of diode. So, the steady state current sharing form is unchanged. The form of equations (2-6) and (2-7) can still be used. The related parameters can be obtained by the third quadrant conduction characteristic curve of SiC MOSFET and the antiparallel diode conduction characteristic curve of Si IGBT from the datasheets.

2.4 Gate Driving Sequence and Switching Characteristic

The switching characteristics of Si/SiC HyS is closely related to the gate switching sequences for the Si IGBT and SiC MOSFET. Based on the sequences of turn-on and turn-off, there are four types of gate driving sequences for the Si/SiC HyS. As depicted in Figure 2-8, the Si/SiC HyS has four basic switching patterns. Figure 2-8 (a) shows the gate sequence of SiC MOSFET turns on first and turns off last. Under this gate sequence, all the switching loss will be produced by the SiC MOSFET. The Si IGBT will only have zero voltage switching. This gate sequence aims at reducing the switching loss. Figure 2-8 (b) shows the gate sequence of Si IGBT turns on first and turns off last. Under this gate driving sequence, the Si IGBT will produce all the switching loss and SiC MOSFET will experience zero voltage switching. This gate driving sequence allows the high pulse current during the turn on and turn off delay time to be conducted by the Si IGBT. Benefit from the high overload capability of Si IGBT, the overload current capability of Si/SiC HyS is improved by using this switching sequence. The gate driving sequence shown in Figure 2-8 (c) and Figure 2-8 (d) shows the other two types of gate driving sequences which can be

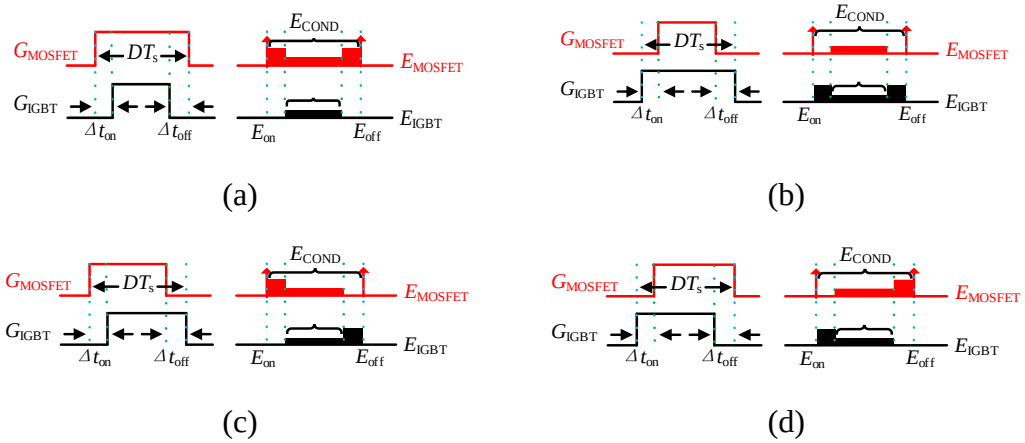


Figure 2-8 Si/SiC HyS switching sequences.

Table 2-1 Double pulse experiment parameters

Item	Parameter
Si IGBT	IKW15N120T2 (1200 V / 15 A)
SiC MOSFET	C2M0280120D (1200 V / 7.5 A)
Dc voltage	400V
Current	20A
Inductor	1mH
Dc capacitor	1.5mF
R_g of SiC MOSFET	7.5Ω
R_g of Si IGBT	20Ω
Gate drive voltage	+18/-5

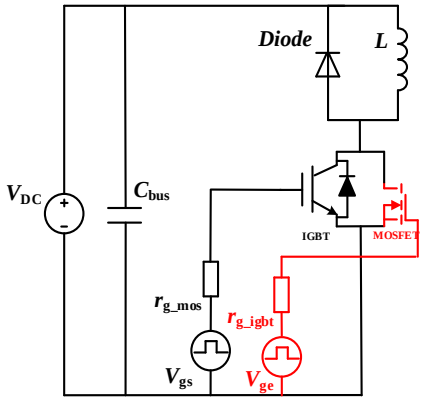
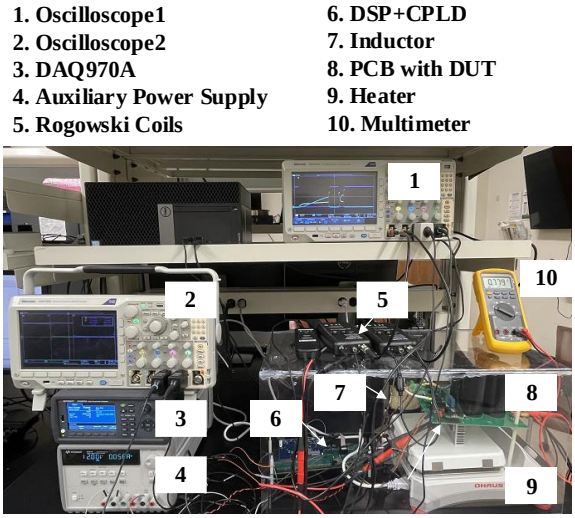


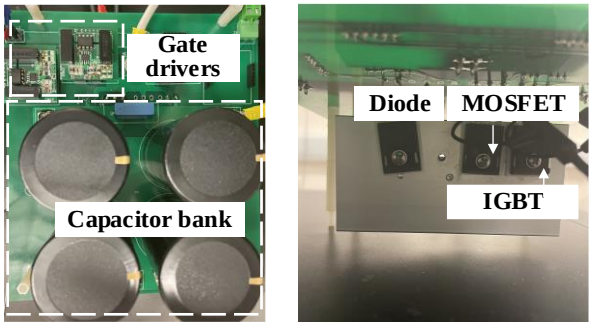
Figure 2-9 Schematic of the double pulse test.

utilized to balance the switching loss distribution among the Si IGBT and SiC MOSFET to regulate the junction temperature distribution of Si IGBT and SiC MOSFET.

To further investigate the Si/SiC HyS switching characteristic under different gate sequences, the double pulse test is conducted to characterize the switching process. The test parameters are listed in Table 2-1. The double pulse test schematic is depicted in Figure 2-9. The double pulse test experimental set up is shown in Figure 2-10. In Figure 2-10 (a), the Ti DSP 28379d and Intel EPM240 series CPLD are utilized to generate the double pulse and add the turn on and turn off delay time. The Rogowski coils are used to measure the device current.

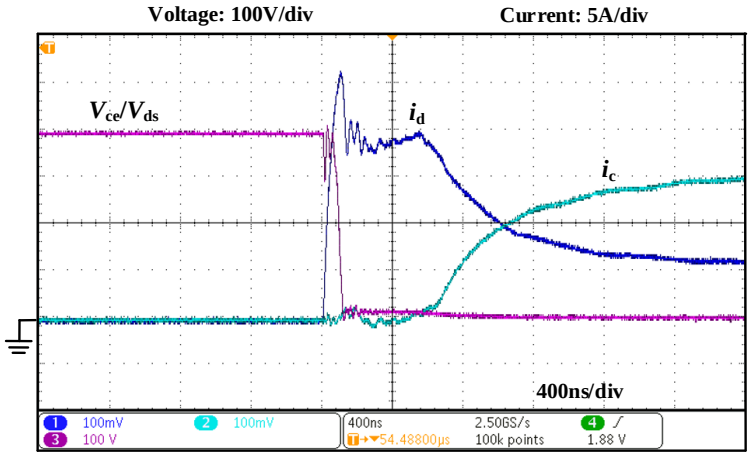


(a) Experimental setup

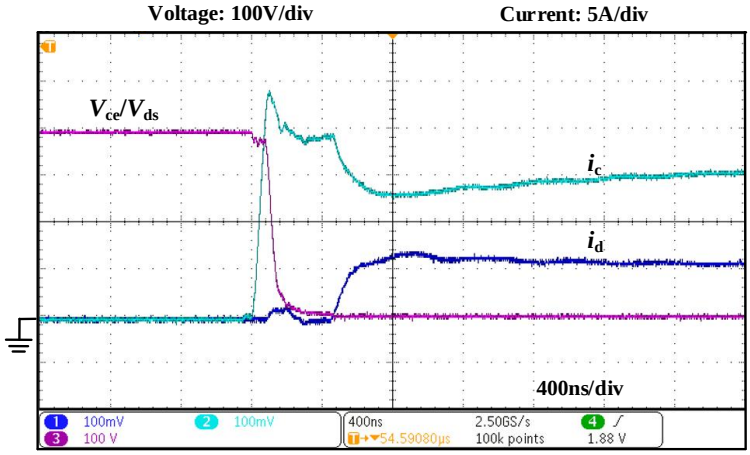


(b) PCB with DUT

Figure 2-10 Double pulse test experimental setup.



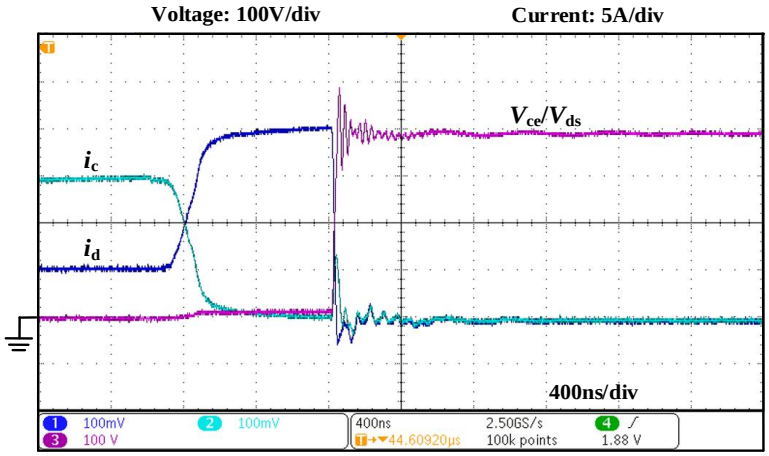
(a) SiC MOSFET turns on first



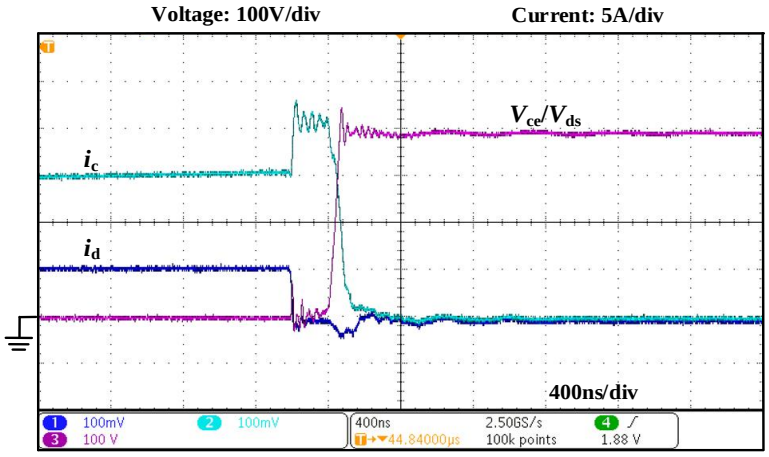
(b) Si IGBT turns on first

Figure 2-11 Turn on process of Si/SiC HyS.

The turn on process is depicted in Figure 2-11. In Figure 2-11 (a), the SiC MOSFET is turned on first. All the load current is commuted by the SiC MOSFET. After the turn on delay time, the Si IGBT is turned on. Then the load current start to be transferred from the SiC MOSFET to Si IGBT. After the dynamic current sharing process, the current conducting of Si/SiC HyS reaches steady state. The turn on process of "Si IGBT turns on first" is shown in Figure 2-11 (b). It is noted that the Si IGBT is turned on ahead of SiC



(a) Si IGBT turns off first



(b) SiC MOSFET turns off first

Figure 2-12 Turn off process of Si/SiC HyS.

MOSFET. All the load current is commutated by the Si IGBT After the turn on delay time, the SiC MOSFET is turned on. Then the SiC MOSFET start to share the load current.

The turn off process is depicted in Figure 2-12. In Figure 2-12 (a), the Si IGBT is turned off first. During the turn off delay time. All the load current is conducted by the SiC MOSFET, the conduction voltage increases a bit. After the turn off delay time, the SiC MOSFET is turned off. At the transient of SiC MOSFET turning off, a current spike in Si IGBT can be observed. The current spike is caused by the residual carriers' recovery within

the Si IGBT. The high di/dt at the turn off transient extract and accelerate the recovery process of the residua carriers, thereby forming the current spike. The influence of the residual current spike on Si IGBT to the system is discussed in Chapter 3 section 3.2.

In Figure 2-12 (b), the SiC MOSFET is turned off ahead of the Si IGBT. After the SiC MOSFET is turned off, all the load current is forced to the Si IGBT. During the turn off delay time, all the load current is conducted by the Si IGBT. After the turn off delay time, the Si IGBT is turned off. It shows a slower turn off speed.

2.5 Loss Modeling for Hybrid Switch

2.5.1 Conduction Loss Modeling

As shown in Figure 2-8 in section 2.3.2, the conduction loss distribution varies with under different gate driving sequence and gate delay time. The conduction loss model can be calculated separately under different gate driving sequences.

1) $\Delta t_{on}>0$ and $\Delta t_{off}>0$

$$P_{con\_HyS\_igbt}(n)=\begin{cases} f_s\left(\frac{D(n)}{f_s}-\Delta t_{on}-\Delta t_{off}\right)\left(i_c(n)r_{ce}+V_{th}\right)i_c\ , & \frac{D(n)}{f_s}>t_{delay} \\ 0 & , \frac{D(n)}{f_s}\le t_{delay} \end{cases} \tag{2-8}$$

$$P_{con\_HyS\_mosfet}(n)=\begin{cases} f_s\left\{\left(\frac{D(n)}{f_s}-\Delta t_{on}-\Delta t_{off}\right)i^2{}_d(n)r_{ds}+(\Delta t_{on}+\Delta t_{off})i_{load}{}^2(n)r_{ds}\right\} & \\ & , \frac{D(n)}{f_s}>t_{delay} \\ D(n)\cdot i_{load}{}^2(n)r_{ds} & , \frac{D(n)}{f_s}\le t_{delay} \end{cases} \tag{2-9}$$

2) $\Delta t_{on}>0$ and $\Delta t_{off}<0$

$$P_{con\_HyS\_igbt}(n)=\begin{cases} f_s\left(\frac{D(n)}{f_s}-\Delta t_{on}\right)\left(i_c(n)r_{ce}+V_{th}\right)i_c+\Delta t_{off}\left(i_{load}(n)r_{ce}+V_{th}\right)i_{load} \\ \qquad\qquad , \ \frac{D(n)}{f_s}>t_{delay} \\ 0 \qquad\qquad , \ \frac{D(n)}{f_s}\le t_{delay} \end{cases} \tag{2-10}$$

$$P_{con\_HyS\_mosfet}(n)=\begin{cases} f_s\left\{\left(\frac{D(n)}{f_s}-\Delta t_{on}-\Delta t_{off}\right)i_d^{\,2}(n)r_{ds}+\Delta t_{on}\,i_{load}^{\,2}(n)r_{ds}\right\} \\ \qquad\qquad , \ \frac{D(n)}{f_s}>t_{delay} \\ D(n)\cdot i_{load}^{\,2}(n)r_{ds} \qquad , \ \frac{D(n)}{f_s}\le t_{delay} \end{cases} \tag{2-11}$$

3) $\Delta t_{on}<0$ and $\Delta t_{off}<0$

$$P_{con\_HyS\_igbt}(n)=\begin{cases} f_s\left(\frac{D(n)}{f_s}\right)\left(i_c(n)r_{ce}+V_{th}\right)i_c+(\Delta t_{on}+\Delta t_{off})\left(i_{load}(n)r_{ce}+V_{th}\right)i_{load} \\ \qquad\qquad , \ \frac{D(n)}{f_s}>t_{delay} \\ 0 \qquad\qquad , \ \frac{D(n)}{f_s}\le t_{delay} \end{cases} \tag{2-12}$$

$$P_{con\_HyS\_mosfet}(n)=\begin{cases} f_s\left\{\left(\frac{D(n)}{f_s}-\Delta t_{on}-\Delta t_{off}\right)i_d^{\,2}(n)r_{ds}\right\} \quad , \ \frac{D(n)}{f_s}>t_{delay} \\ D(n)\cdot i_{load}^{\,2}(n)r_{ds} \qquad , \ \frac{D(n)}{f_s}\le t_{delay} \end{cases} \tag{2-13}$$

4) $\Delta t_{on}<0$ and $\Delta t_{off}>0$

$$P_{con\_HyS\_igbt}(n)=\begin{cases} f_s\left(\frac{D(n)}{f_s}-\Delta t_{off}\right)\left(i_c(n)r_{ce}+V_{th}\right)i_c+\Delta t_{on}\left(i_{load}(n)r_{ce}+V_{th}\right)i_{load} \\ \qquad\qquad , \ \frac{D(n)}{f_s}>t_{delay} \\ 0 \qquad\qquad , \ \frac{D(n)}{f_s}\le t_{delay} \end{cases} \tag{2-14}$$

$$P_{con\_HyS\_mosfet}(n)=\begin{cases} f_s\left\{\left(\frac{D(n)}{f_s}-\Delta t_{on}-\Delta t_{off}\right)i^2{}_d(n)r_{ds}+\Delta t_{off}i_{load}{}^2(n)r_{ds}\right\} \\ \qquad\qquad , \ \frac{D(n)}{f_s}>t_{delay} \\ D(n)\cdot i_{load}{}^2(n)r_{ds} \qquad , \ \frac{D(n)}{f_s}\le t_{delay} \end{cases} \tag{2-15}$$

where D(n) is the duty ratio of nth switching cycle. i_c(n), i_d(n), and i_{load}(n) are the current shared by Si IGBT, SiC MOSFET and the inductor current in n_{th} switching cycle. $P_{con\_HyS\_igbt}$ and $P_{con\_HyS\_mosfet}$ are Si/SiC HyS average conduction loss distributed to the IGBT and MOSFET in n_{th} switching cycle. When the current reversely flow through Si/SiC HyS, the diode shares load current with the SiC MOSFET which operates under synchronous rectification mode. The SiC MOSFET body diode will not conduct current in steady state due to its high conduction voltage. The conduction power loss for the diode and SiC MOSFET can be estimated similarly to (2-12) and (2-13) since the diode has the same conduction equivalent circuit as Si IGBT. The Δt_{on} and Δt_{off} refer to the deadtime in the reverse conduction.

2.5.2 Switching Loss Modeling

The switching loss of the semiconductor devices can be calculated by using the curve fitting and the behavioral loss model as follows

$$E_{\text{Switch}} = \begin{cases} E_{\text{on}}\left(i,\ T_{\text{j}}\right)\dfrac{V_{\text{ds\_test}}}{V_{\text{ds\_rated}}} \\ E_{\text{off}}\left(i,\ T_{\text{j}}\right)\dfrac{V_{\text{ds\_test}}}{V_{\text{ds\_rated}}} \end{cases} \tag{2-16}$$

Where E_{on} and E_{off} are the turn on and turn off loss data obtained either by double pulse test or the manufacturer's datasheet and they are dependent on the conduction current i, device junction temperature T_{j} and the drain-source voltage in the test $V_{\text{ds\_test}}$.

It is assumed the switching is f_{s}, the average switching loss in the n_{th} switching cycle can be calculated by

$$P_{\text{Switch}}(n) = \begin{cases} P_{\text{on}}(n) = f_{\text{s}} E_{\text{on}}\left(n\right)\dfrac{V_{\text{ds\_test}}}{V_{\text{ds\_rated}}} \\ P_{\text{off}}(n) = f_{\text{s}} E_{\text{off}}\left(n\right)\dfrac{V_{\text{ds\_test}}}{V_{\text{ds\_rated}}} \end{cases} \tag{2-17}$$

Where P_{on}(n) and P_{off}(n) are the average turn on and turn off power losses.

With the proposed loss model for the Si/SiC HyS, the thermal related works, for example the converter efficiency estimation, can be investigated.

2.6 Summary

In this chapter, the conduction and switching characteristics of the Si/SiC HyS are investigated. For the conduction characteristic, the dynamic current sharing process and steady state current sharing model are analyzed. The switching process under different gate driving patterns is characterized by massive double pulse tests. The experimental results

validated that under the gate driving sequence of “SiC MOSFET turns on first and turns off last”, the Si IGBT will switch under zero voltage condition which significantly reduces the IGBT switching loss. Finally, the loss model for the Si/SiC HyS is proposed for the thermal related works that will be investigated in the next parts of this dissertation.

CHAPTER 3: OPERATION OPTIMIZATION FOR HYBRID SWITCH

3.1 Si and SiC Current Rating Optimization for Hybrid Switch

To implement a cost-effective, high power density, and high efficiency Si/SiC HyS-based converter, the Si and SiC current rating optimization is important to achieve such a goal. If the current rating of the selected SiC MOSFET is too small, the thermal stress of SiC MOSFET will be very high that will limit the converter output capacity and reduce the system reliability. If the current rating is too large, the device cost for SiC MOSFET will increase. In this part, a current rating optimization algorithm that is based on the commercially available discrete Si IGBT and SiC MOSFET devices is introduced.

As depicted in Figure 3-1, the algorithm starts with several selected Si and SiC devices that can form the full current rated Si/SiC HyS for a specific application. Several Si/SiC HyS combination candidates are obtained. Then, based on the selected Si/SiC HyS

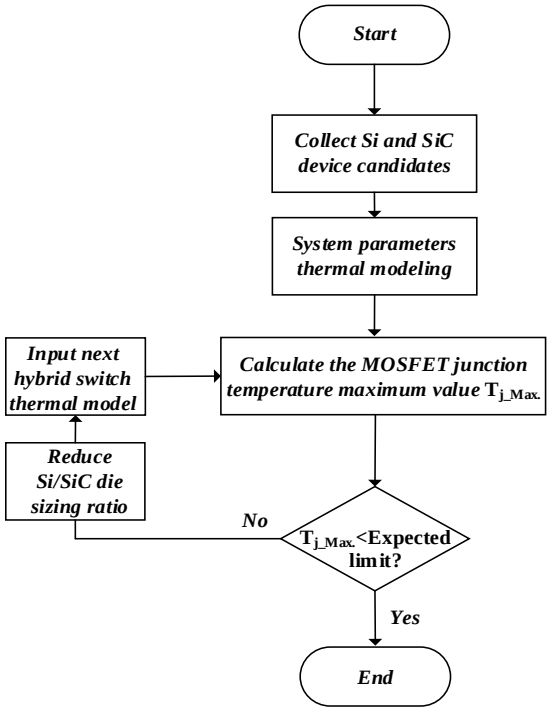


Figure 3-1 Proposed Si and SiC current rating algorithm.

candidates, the thermal simulation is conducted to estimate the device's maximum junction temperature. After this step, the combinations of whose maximum junction temperature exceed the safe operation limit will be discarded. Then, from the rest of the Si/SiC HyS combinations, the most cost-effective combination can be selected. A step-by-step example of how to select a proper Si/SiC HyS for a 40 kW 3L-ANPC inverter with 1500 V dc voltage is presented below.

Step 1. Select the potential Si/SiC HyS candidates based on the commercially available discrete devices. In the Table 3-1, four pairs of 1200 V / 100 A Si/SiC HyS combination are selected for this application. The device cost is from the Mouser Electronics on a bulk order of more than 1000 units. It is observed that with the increase of SiC MOSFET's current rating, the device cost increases.

Step 2. The device maximum junction temperature for each pair is estimated using the thermal simulation tool, such as PLECS. The simulation parameters are listed in Table 3-2. The simulation results for the most heated device SiC MOSFETs are shown in the Figure 3-2.

Table 3-1 1200 V / 100 A Si/SiC HyS combinations

	Configuration	Si/SiC ratio	Cost/$
Pair1	IKQ75N120CT2+C2M0160120D	6.3:1	23.3
Pair 2	IKQ75N120CT2+C3M0075120D	3.8:1	26.3
Pair 3	IKQ75N120CT2+C2M0080120D	3.1:1	31.3
Pair 4	IKQ50N120CT2+C2M0040120D	1.3:1	45.6

Table 3-2 Simulation parameters

Parameters	Value
DC input voltage	1500 V
Output voltage	480 V_{rms}
Rated power	40kW
Switching frequency	18 kHz
Turn on delay	1 μs
Turn off delay	1 μs

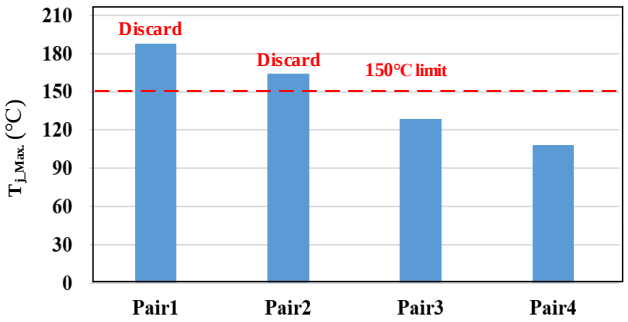


Figure 3-2 Device maximum junction temperature comparison of different Si/SiC HyS pairs.

Step 3. It is noted that pair 1 and pair 2 cannot meet the device junction temperature requirement. The SiC MOSFET maximum junction temperature exceed the limit 150℃. So, pair 1 and pair 2 are discarded. For the pair 3 and pair 4, they both satisfy the junction temperature requirement. While pair 4 has a higher device cost and a higher inverter efficiency. For the cost-sensitive applications, pair 3 would be a better Si/SiC HyS candidate and for those high efficiency and high-power density applications, pair 4 would be a better choice.

3.2 Optimization of Gate Delay Time

3.2.1 Turn on Delay Time Optimization

The turn on process loss analysis of Si/SiC HyS under the gate sequence of SiC MOSFET turns on first and turns off last is shown in Figure 3-3. It is shown that during the turn on process, two types of loss are depicted: hybrid switch turn on loss $E_{\text{on\_HyS}}$ which consists of the turn on loss of SiC MOSFET and turn on loss of Si IGBT.

$$E_{\text{on\_HyS}} = E_{\text{on\_MOSFET}} + E_{\text{on\_IGBT}} \tag{3-1}$$

The second type of loss is the extra conduction loss $E_{\text{on\_extra\_on}}$ is caused by the turn on delay time. This part of loss will be significant and not neglectable if a very large turn on delay is applied to the Si/SiC HyS since the small current rated SiC MOSFET will produce a very high conduction voltage when conducting the all the current within the delay time. The total loss in the turn on process can be calculated by

$$E_{\text{on\_total}} = E_{\text{on\_HyS}} + E_{\text{on\_extra\_con}} = E_{\text{on\_MOSFET}} + E_{\text{on\_IGBT}} + E_{\text{on\_extra\_con}} \tag{3-2}$$

The Si/SiC HyS turn on waveforms at different Δt_{on} is shown in Figure 3-4. In Figure 3-4 (a), it is shown that the Δt_{on} is -0.5μs, the Si IGBT is turned on 0.5μs ahead of

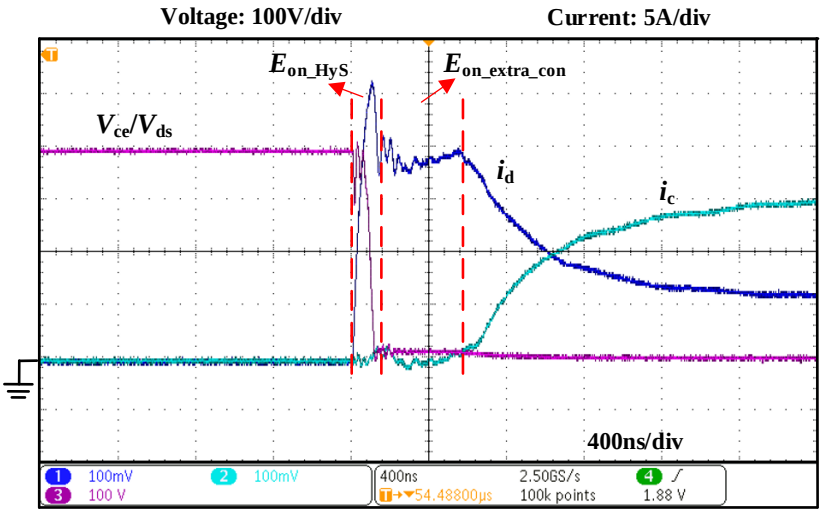
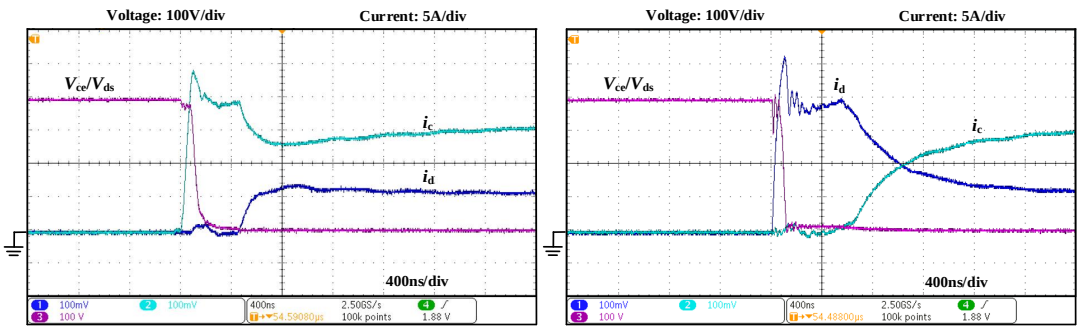


Figure 3-3 Si/SiC HyS turn on loss analysis.



(a) Δt_{on}=-0.5μs (b) Δt_{on}=0.5μs

Figure 3-4 Si/SiC HyS turn on waveforms at different Δt_{on}.

SiC MOSFET. It is shown that the Si IGBT has a hard turn on and SiC MOSFET experiences a soft turn on. In Figure 3-4 (b), the turn on delay time is 0.5μs which means the turn on gate signal of SiC MOSFET is 0.5μs ahead of Si IGBT. Under this gate delay time, the Si IGBT has a soft turn on and SiC MOSFET has a hard turn on. It is shown that the value of Δt_{on} will affect the switching loss E_{on_HyS} by having different device to do the hard switching. In addition, the value of Δt_{on} will also affect the extra conduction loss $E_{on\_extra\_con}$. In Figure 3-4 (a), the value of $E_{on\_extra\_con}$ will be much smaller than that in Figure 3-4 (b) because of the lower conduction voltage of Si IGBT when conducting the full load current.

From the analysis, it is noted that the total turn on loss of the Si/SiC HyS can be affected by the selecting of different value of Δt_{on}. In order to investigate the relationship between E_{on_total} and Δt_{on}, double pulse tests are carried out under different Δt_{on}. The delay from CPLD output to the gate driver output is tested before conducting the double pulse test. The results shown in Figure 3-5 indicate that this part of delay is less than 1ns which is neglectable during the test.

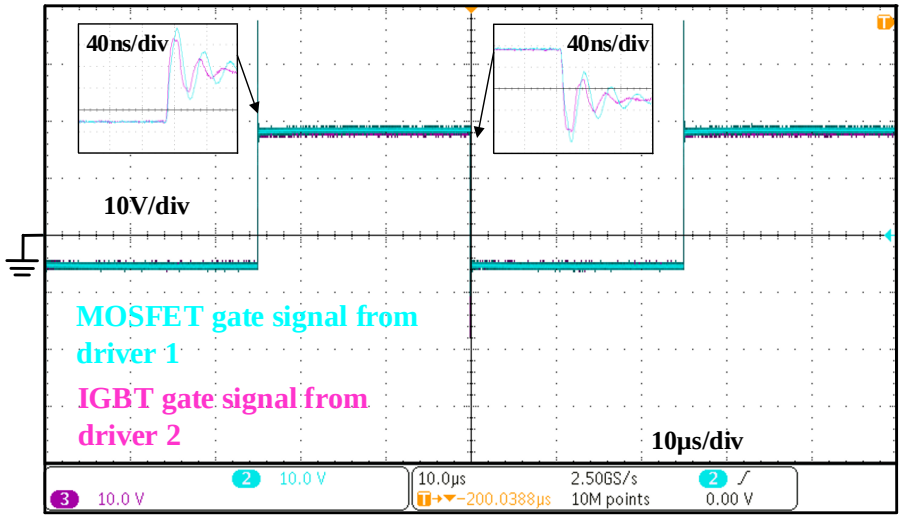


Figure 3-5 Gate signal delay check.

The test results of the dependency between the total turn on loss and Δt_{on} are depicted in Figure 3-6. It is depicted that when the delay time is smaller than -0.5µs, which means that the Si IGBT turn on gate signal is 0.5µs earlier than the turn on gate signal of SiC MOSFET, the Si IGBT will do the hard switching and produces the hard switching loss in turn on process. The SiC MOSFET will have a soft turn on with neglectable turn on loss. With the increase of turn on delay time, both the Si IGBT and SiC MOSFET channels will conduct the turn on current and produce the turn on loss. When the turn on delay is 0.04µs, which means the Si IGBT turn on gate signal is 0.04µs later than the SiC MOSFET, the SiC MOSFET will produce the hard turn on loss and Si IGBT will experience a soft turn on with neglectable turn on loss. It is also noted that with the increase of Δt_{on}, the extra conduction loss increases, especially when the turn on delay is a positive value. The optimal turn on delay time for the Si/SiC HyS is either -0.04µs or -0.06µ. The total turn on loss is 296.4µJ. The Figure 3-7 shows the turn on process of Si/SiC HyS at Δt_{on}=-0.04µs.

The optimal turn on delay time at different current levels is also tested and summarized in the Table 3-3. From Table 3-3, it is noted that the optimal turn on delay time is -0.04μs and -0.06μs for different current level. It is optimal to use different turn on delay time at different current level, but it would increase the control complexity a lot.

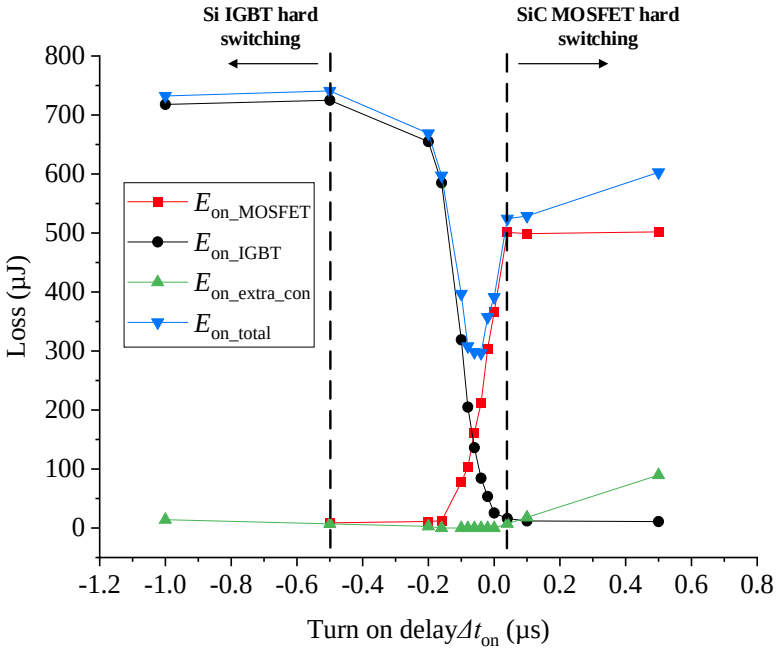


Figure 3-6 Si/SiC HyS turn on loss vs. different turn on delay.

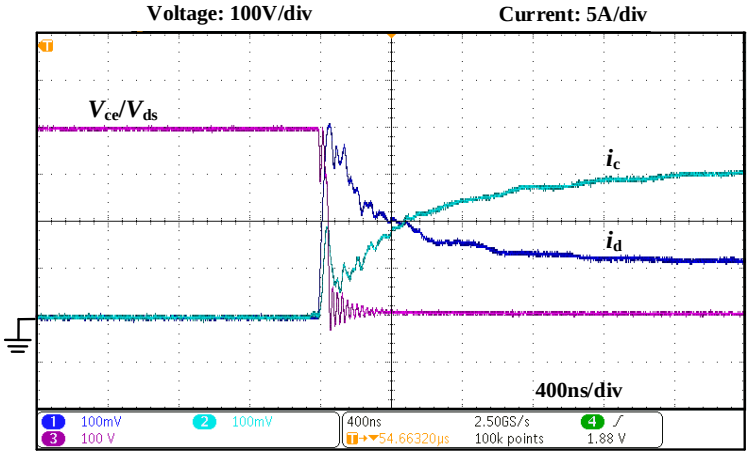


Figure 3-7 Si/SiC HyS turn on process at Δt_{on}=-0.04μs.

From the engineering perspective, using a constant turn on delay time will make the control system more efficient.

The fourth and fifth rows of Table 3-3 show the turn on loss increase of using a constant turn on delay -0.04μs or -0.06μs. It is shown that for the current level 15A, and 18A, when using the constant Δt_{on} -0.04μs, the turn on loss increases 8.9%, and 7.2%. If using a constant turn on delay time of -0.06μs, the turn on loss of Si/SiC HyS will increase 30.8% and 7.2% at current levels of 7A and 10A. The selection on the constant turn on delay time could vary for different applications. For example, if using the Si/SiC HyS in a UPS converter that has a mission profile with light load at most of its operation, the constant turn on delay time of -0.04μs may be a better choice since it has lower turn on loss at low current. If using the Si/SiC HyS in a power converter that has a mission profile with middle or heavy load at most of its operation, the constant turn on delay time of -0.06μs would be better since it has lower turn on loss in the middle and high current level.

3.2.2 Turn off Delay Time Optimization

Table 3-3 Optimal turn on delay time at different current levels

Term	Value					
i_{load} (A)	7	10	13	15	18	20
Optimal Δt_{on} (μs)	-0.04	-0.04	-0.04	-0.06	-0.06	-0.06
Total turn on loss (μJ)	117.4	147.9	185.5	194.2	243.3	296.4
Loss increase of using -0.04μs	0	0	0	8.9%	7.2%	0
Loss increase of using -0.06μs	30.8%	7.2%	0	0	0	0

The Si/SiC HyS turn off process loss analysis under the gate sequence of Si IGBT turns off first is depicted in Figure 3-8. It is noted that the turn off process of Si/SiC HyS has three types of semiconductor loss. The first type of loss is the extra conduction loss during the turn off process. This part of loss is caused by the very high conduction voltage of SiC MOSFET.

$$E_{\text{off\_extra\_con}} = (V_{\text{ds\_full current}} \times i_{\text{load}} - V_{\text{ds\_steady state}} \times i_d) \times \Delta t_{\text{off}} \quad (3\text{-}3)$$

Where $V_{\text{ds\_full current}}$ is the conduction voltage of SiC MOSFET when conducting the all the current within the turn off delay Δt_{off}. i_{load} is the full load current. $V_{\text{ds\_steady state}}$ is the SiC MOSFET conduction voltage in steady state. Δt_{off} is the turn off delay time.

The second type of loss is the turn off loss of Si/SiC HyS that can be calculated by

$$E_{\text{off\_HyS}} = E_{\text{off\_MOSFET}} + E_{\text{off\_IGBT}} \quad (3\text{-}4)$$

Where $E_{\text{off\_MOSFET}}$ and $E_{\text{off\_IGBT}}$ are the turn off loss of SiC MOSFET and Si IGBT.

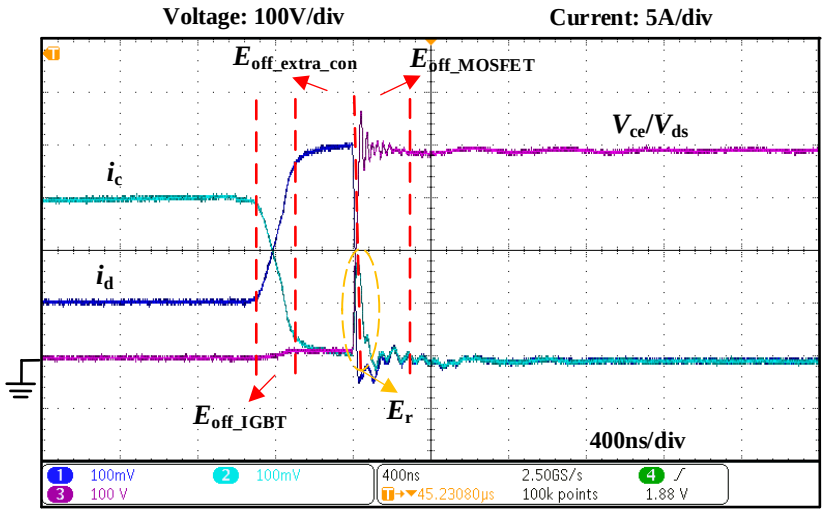
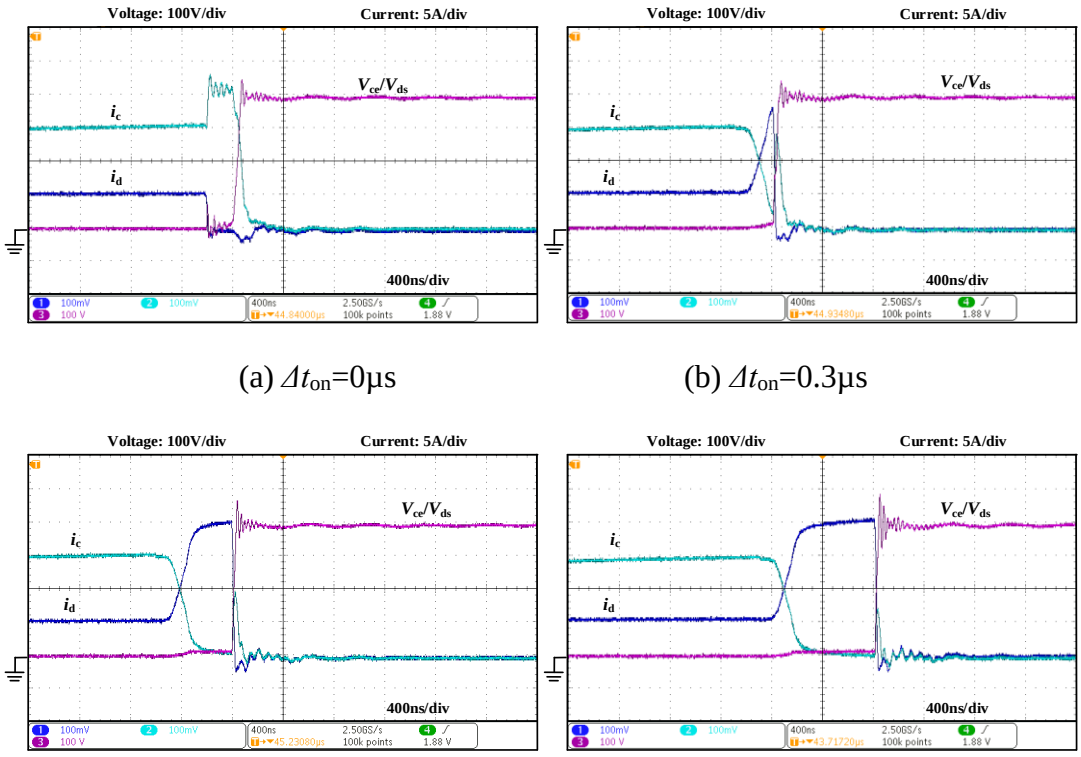


Figure 3-8 Si/SiC HyS turn off loss analysis.



(a) Δt_{on}=0μs (b) Δt_{on}=0.3μs

(c) Δt_{on}=0.6μs (d) Δt_{on}=0.9μs

Figure 3-9 Si/SiC HyS turn off process under different turn off delay.

The third type of semiconductor loss is the Si IGBT residual loss E_r which is produced by the residual carriers restored in Si IGBT. The residual carriers are extracted at the turn off transient. The total loss of the Si/SiC HyS turn off process can be expressed as

$$E_{\text{off\_total}} = E_{\text{off\_MOSFET}} + E_{\text{off\_IGBT}} + E_{\text{off\_extra\_con}} + E_r \tag{3-5}$$

Figure 3-9 shows the turn off processes under different Δt_{off}. In Figure 3-9 (a), the turn off delay time is 0. It is noted that the SiC MOSFET is turned off by ZVS. The Si IGBT has the hard turn off and produces the hard turn off loss. From Figure 3-9 (b) to Figure 3-9 (d), the turn off delay time Δt_{off} is increased from 0.3μs to 0.9μs. It is shown that the Si IGBT has a soft switching at turn off transient and the SiC MOSFET experiences

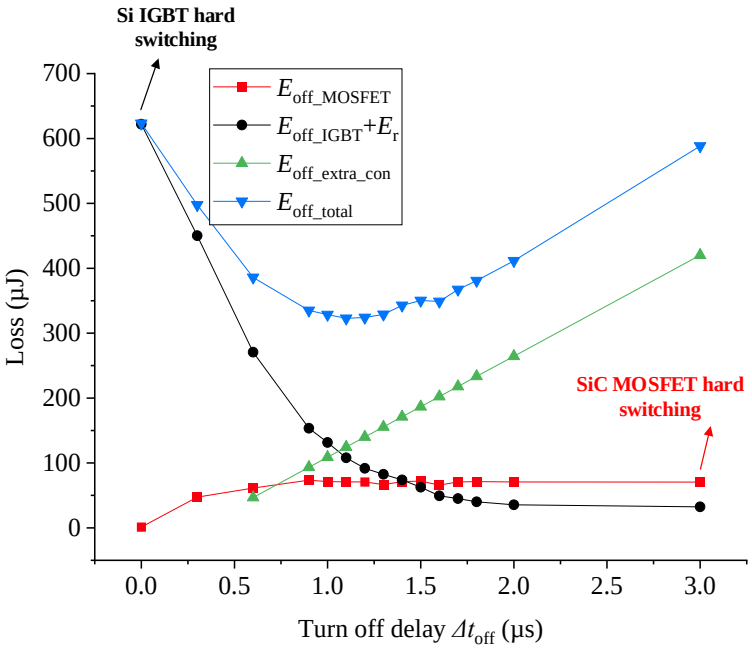


Figure 3-10 Si/SiC HyS turn off loss vs. different turn off delay.

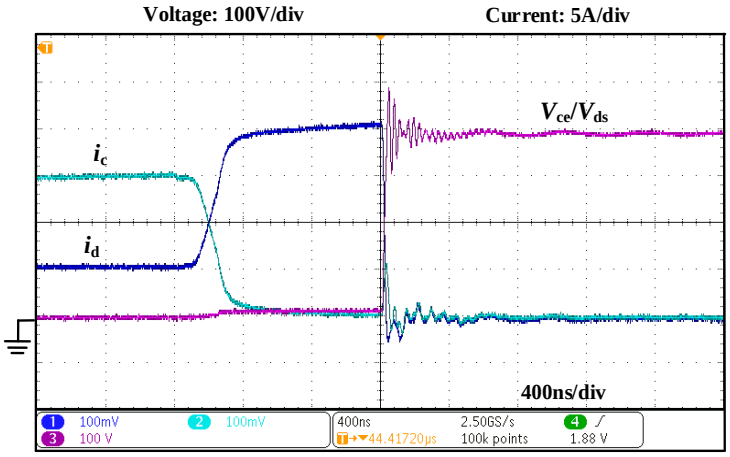


Figure 3-11 Si/SiC HyS turn off process at Δt_{off}=1.2μs.

the hard switching. It is also noted that the residual loss of Si IGBT reduces with the increase of the Δt_{off}. Thus, the turn off delay time will affect the turn off loss distribution and total turn off loss. The turn off loss breakdown and total turn off loss under different turn off delay time is depicted in Figure 3-10.

It is illustrated in Figure 3-10 that when the turn off delay time is 0, the Si IGBT has the hard switching turn off loss. With the increase of turn off delay time, the sum of Si IGBT's turn off loss and residual loss reduces gradually. The SiC MOSFET's turn off loss increases to the hard switching value. The extra conduction loss keeps increasing linearly. The optimal turn off delay time for the Si/SiC HyS is 1.2μs. The turn off waveform of the Si/SiC HyS under 1.2μs turn off delay time is depicted in Figure 3-11.

Table 3-4 Optimal turn off delay time at different current levels

Items	Value					
i_{load} (A)	7	10	13	15	18	20
Optimal Δt_{off} (μs)	1.6	1.6	1.4	1.5	1.3	1.2
Total turn off loss (μJ)	22.5	65	111	159.1	232.2	302.5

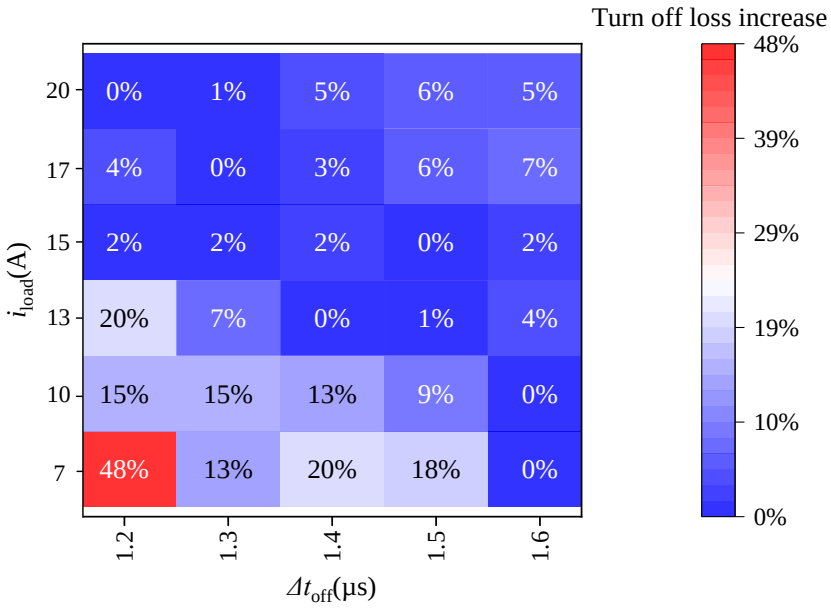


Figure 3-12 Turn off loss increase under different constant Δt_{off}.

The optimal delay time at different current levels is tested and summarized in Table 3-4. From Table 3-4, it is observed that the optimal turn off delay time varies for different current level. But they are all within the range from 1.2μs to 1.6μs. It is optimal to use different turn off delay time at different current level considering the converter efficiency, but from the engineering perspective, using a constant turn off delay time is usually more efficient considering the control system design complexity. Figure 3-12 shows the turn off loss increase under different constant turn off delay time compared to the optimal turn off delay time at each current level. It is shown that with the increase of current level, using the optimal turn off delay time contributes less to the loss reduction. Based on Figure 3-12, a constant Δt_{on} 1.6μs can be selected for the full current range since the loss increase at any current level is below 10%.

It needs to mention that using the optimal delay time is always the best choice considering the power losses. But a constant delay time will reduce the system control complexity while sacrifices little efficiency. For different system, the principle of delay time selection may vary.

3.2.3 Gate Delay Time Optimization Impact

In this section, the system efficiency and thermal performance of the Si/SiC HyS under different gate delay time are investigated based on a buck converter. The experimental parameters are listed in Table 3-5.

The converter efficiency and thermal performance change under different turn on delay time (turn off delay time is constant at 1μs) is shown in Figure 3-13. It is shown that when the Δt_{on} is -0.06μs, the Si/SiC HyS has a lowest total turn on loss at 15A. The efficiency curve indicated in the green line shows that the converter efficiency increases

Table 3-5 Experimental parameters

Parameters	Value
DC input voltage	400 V
Output voltage	200V
Output current	15A
Switching frequency	20 kHz

with the Δt_{on} changes from -0.5μs to -0.06μs. When using the turn on delay time between -0.06μs and -0.02μs, the converter efficiency reaches the highest value which is around 93.77%. Increasing the turn on delay time to 0μs, the converter efficiency decreases. It is shown that when the converter was operating under the optimal delay time (-0.06μs), the converter has the highest efficiency. Compared to using the delay time 0, the converter efficiency is improved by 0.07% at 20kHz. Assuming the conduction loss is unchanged at different switching frequencies, the efficiency improvement will be more significant at high switching frequencies. 0.35% converter efficiency can be improved at 100kHz.

In addition to the efficiency improvement, the device temperatures also vary under different Δt_{on}. When the Δt_{on} is increased from -0.5μs to 0, the MOSFET case temperature keeps increasing and the IGBT case temperature keeps decreasing. This is because the MOSFET will produce more switching loss and extra conduction loss and IGBT generates less switching loss with the increase of turn on delay time. The thermal images of Si IGBT and SiC MOSFET under different turn on delay time are shown in Figure 3-14.

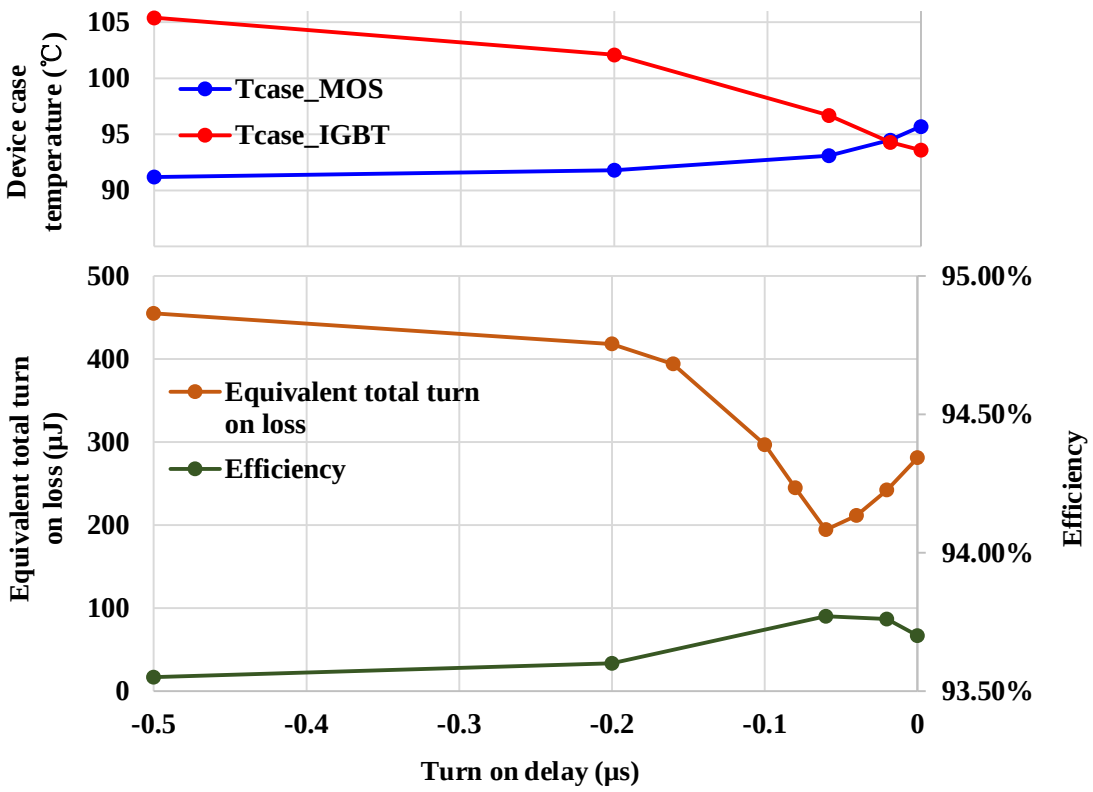


Figure 3-13 Converter efficiency and thermal performance vs. Δt_{on}.

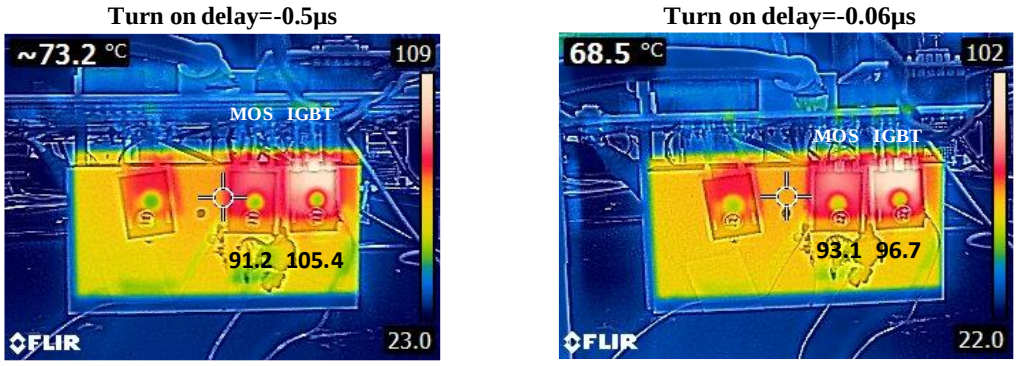


Figure 3-14 The thermal images of Si IGBT and SiC MOSFET.

Figure 3-15 shows the impact of Δt_{off} on the converter efficiency and device thermal performance. The turn on delay time was fixed at 0.

It is shown in Figure 3-15 that the equivalent total turn off loss decreases with the increase of turn off delay time from 0 to 1.5μs. The optimal Δt_{off} for the Si/SiC HyS at 15A

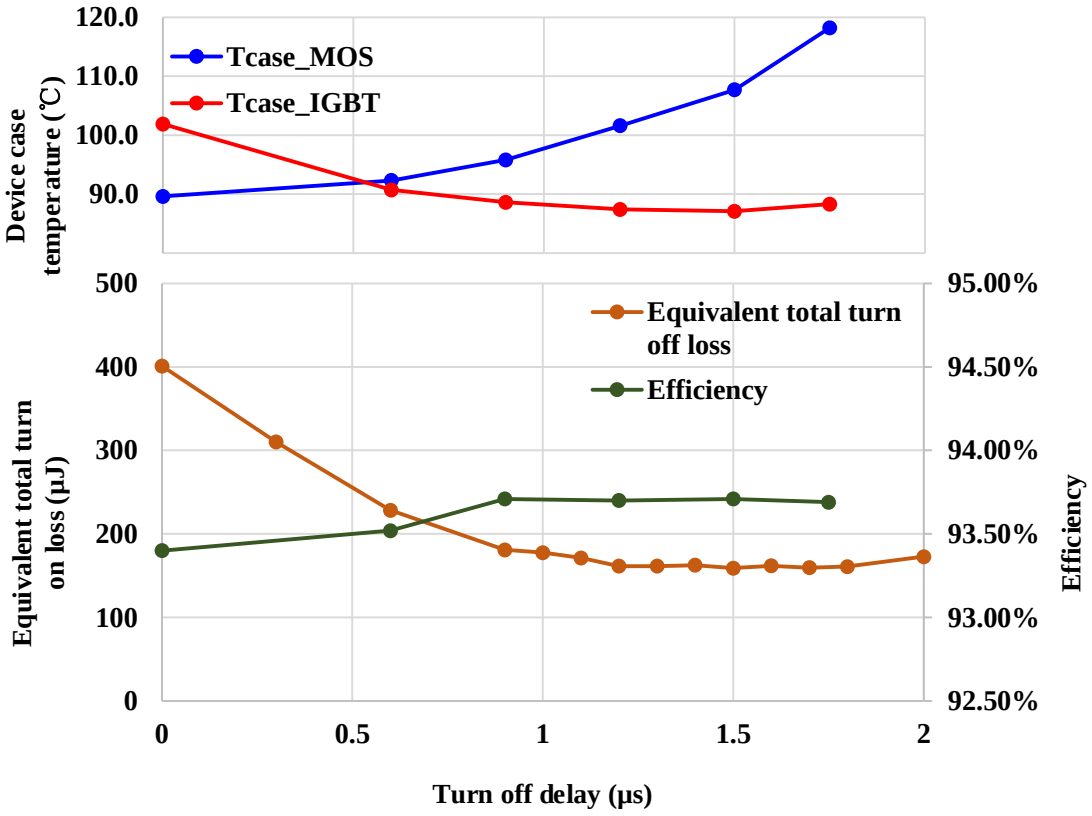


Figure 3-15 Converter efficiency and thermal performance vs. Δt_{off}.

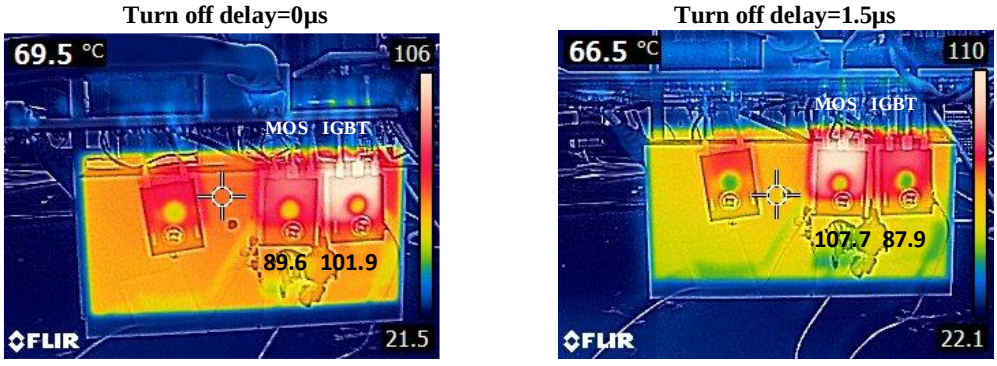


Figure 3-16 The thermal images of Si IGBT and SiC MOSFET.

is 1.5μs while the converter efficiencies are almost the same when using the turn off delay time from 0.9μs to 1.75μs. The small mismatch between the efficiency and loss curve could be caused by the device junction temperature change. Even though the mismatch is observed, the trend of efficiency curve can still validate that the converter efficiency will be affected by the turn off delay time and using the optimal turn off delay time will help to improve the converter efficiency. According to the results shown in Figure 3-15, the device temperatures of Si IGBT and SiC MOSFET can also be affected by the turn off delay time. It is shown that with the increase of turn off delay time, the MOSFET case temperature increase and the IGBT case temperature increases. This is because that with the increase of Δt_{off}, the IGTB residual loss decreases and the MOSFET extra conduction loss increases. The thermal images of Si IGBT and SiC MOSFET are presented in Figure 3-16.

3.3 Active Thermal Control for Si/SiC HyS

Currently, the most commonly used switching sequence for the Si/SiC HyS is SiC MOSFET turn on first and turn off last to minimize the device switching loss and improve the system efficiency. But under this switching characteristic, the small current rated SiC MOSFET will produce all the switching losses and conduction losses. In addition, the small current rated SiC MOSFET usually has a smaller die size and higher thermal resistance. Thus, SiC MOSFET has higher junction temperature than the Si IGBT. The junction temperature unbalance within the Si/SiC HyS will limit the converter output capacity and may reduce the system reliability. To solve this problem, two active thermal control (ATC) algorithms are proposed in this section.

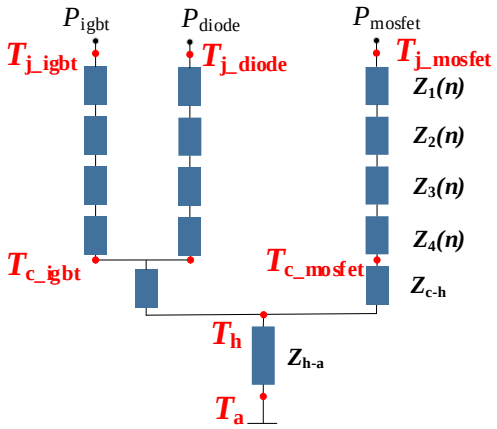


Figure 3-17 Si/SiC HyS thermal model.

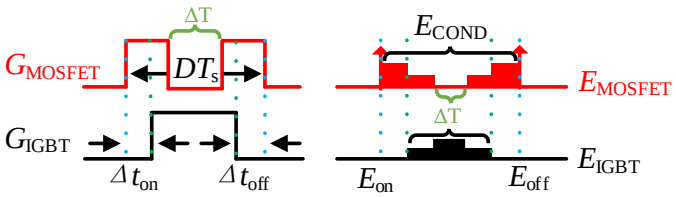


Figure 3-18 Proposed conduction time variation-based ATC algorithm.

3.3.1 Thermal Modeling for Si/SiC HyS

In order to estimate the Si IGBT and SiC MOSFET device junction temperature, the thermal model for the Si/SiC HyS is proposed. As depicted in Figure 3-17, four layers Foster-type RC network representing thermal model from device junction to case is utilized to model the semiconductor devices. With a proper assumed initial temperature of heatsink, case, or ambient and the thermal parameters provided by manufacturer's datasheets, the device's junction temperature can be estimated by

$$T_j = P_{loss}\sum_{m=1}^{4} Z_m + T_c = P_{loss}\sum_{m=1}^{4}\frac{R_m}{\tau_{ms}+1} + T_c \tag{3-6}$$

Where T_j, P_{loss}, and T_c are respectively the junction temperature, pulse power loss profile, and case temperature.

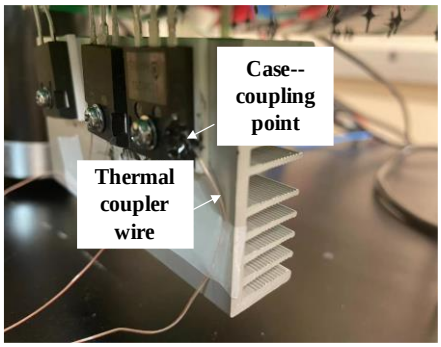


Figure 3-19 The thermal coupler and device case coupling method

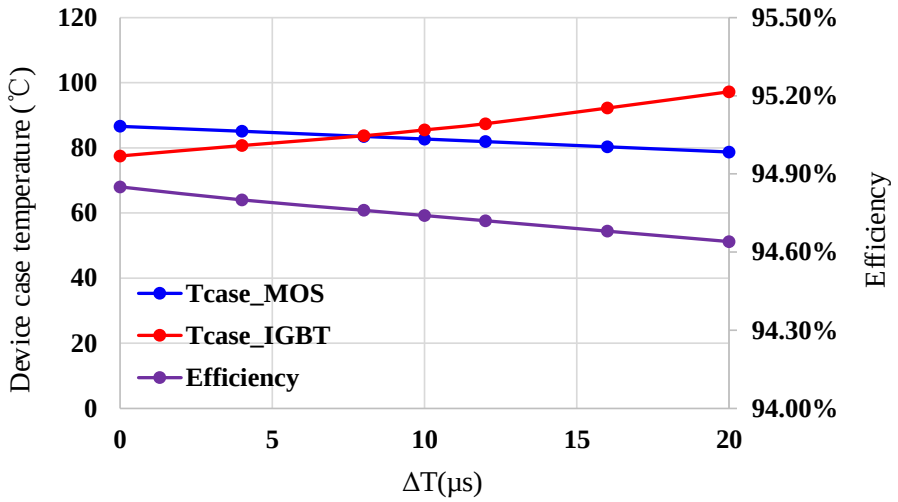


Figure 3-20 Measured device case temperature and converter efficiency under different ΔT

3.3.2 Conduction Time Variation-Based Active Thermal Control

Figure 3-18 briefly shows the proposed conduction time variation-based ATC algorithm for the Si/SiC HyS. During the period ΔT, the SiC MOSFET is turned off actively. All the load current will flow through the Si IGBT, thereby reducing the conduction loss produced by the SiC MOSFET as well as the total loss. The regulated semiconductor loss distribution can be expressed as

$$E_{\mathrm{MOSFET\_R}} = E_{\mathrm{MOSFET}} - \Delta E_{\mathrm{con\_MOS}} \tag{3-7}$$

$$E_{\mathrm{IGBT\_R}} = E_{\mathrm{IGBT}} + \Delta E_{\mathrm{con\_IGBT}} \tag{3-8}$$

Where ΔE_{con_MOSFET} and ΔE_{con_IGBT} are the conduction loss decrease of SiC MOSFET and conduction loss increase of Si IGBT. The zero-voltage switching loss of SiC MOSFET is neglected.

To validate the effectiveness of the proposed ATC algorithm, experiments were conducted on a buck converter that utilized the Infineon Si IGBT IKW15N120T and Wolfspeed SiC MOSFET C2M0280120D as the Si/SiC HyS. The buck converter operated under the proposed conduction time variation-based ATC algorithm with different ΔT. As illustrated in Figure 3-19, the device case temperature was measured by the thermal coupler that attached to the device case. The thermal coupler and device case was bonded by the high temperature and high conductivity epoxy. The Keysight DAQ970A data acquisition system was used to analyze the data and transfer it to temperature. Converter efficiency was measured by the Power Analyzer PA3000.

Figure 3-20 shows the measured device case temperature and converter efficiency when the parameter ΔT changes. It is shown that when ΔT increases from 0 to 20μs, the MOSFET case temperature decreases because the conduction loss it produces decrease. Since the IGBT produces more conduction loss with the increase of ΔT, the IGBT case temperature increase. The converter efficiency also decreases since the total conduction loss will increase with the increase of ΔT. when ΔT=0, the SiC MOSFET and Si IGBT device case temperature are 86.5 ^{o}C and 77.5 ^{o}C, respectively.

Based on the thermal model and the loss profile extract from the double pulse test and manufacturer's datasheet. The device junction temperature can be estimated. Figure 3-21 show the device junction temperature change under different ΔT. It is validated that the

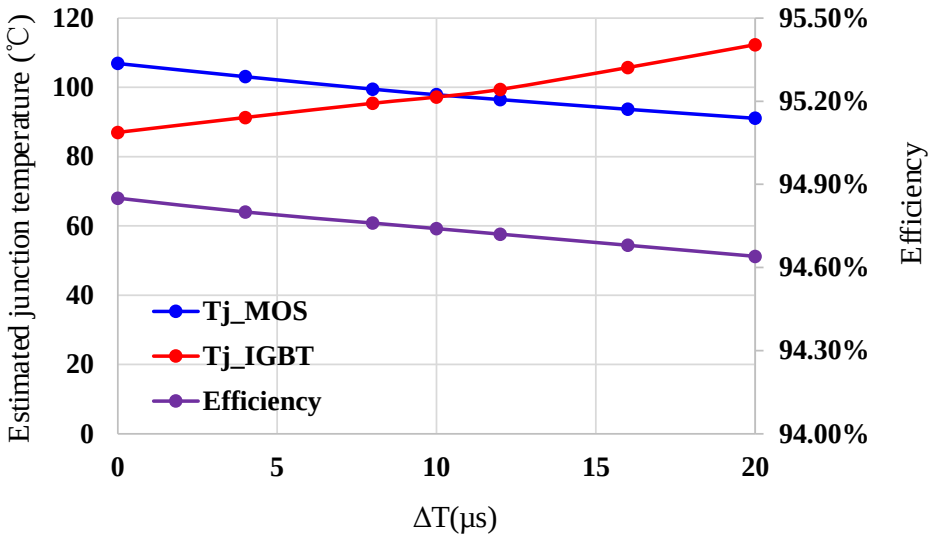


Figure 3-21 Estimated device junction temperature under different ΔT.

device junction temperature can be regulated by the proposed conduction time variation-based ATC.

With the proposed ATC method, the thermal stress of the most heated device SiC MOSFET will be reduced. So, the buck converter maximum output power can be improved. It is worth noting that the Si IGBT and SiC MOSFET have different maximum operating junction temperatures. The balance of device junction temperature can be defined as:

$$\frac{T_{\text{j\_balanced\_MOS}}}{T_{\text{j\_balanced\_IGBT}}} = \frac{T_{\text{j\_max.\_MOS}}}{T_{\text{j\_max.\_IGBT}}} \tag{3-9}$$

Where $T_{\text{j\_balanced\_MOS}}$ and $T_{\text{j\_balanced\_IGBT}}$ are the balanced junction temperatures of SiC MOSFET and Si IGBT which are proportional to their maximum allowable device junction temperatures $T_{\text{j\_max.\_MOS}}$ and $T_{\text{j\_max.\_IGBT}}$, usually 175°C for SiC MOSFET and 150°C for Si IGBT. While in this paper, the SiC MOSFET C2M0280120D maximum operating junction temperature is 150 °C, therefore, a 1:1 junction temperature distribution will be seen as a balanced state.

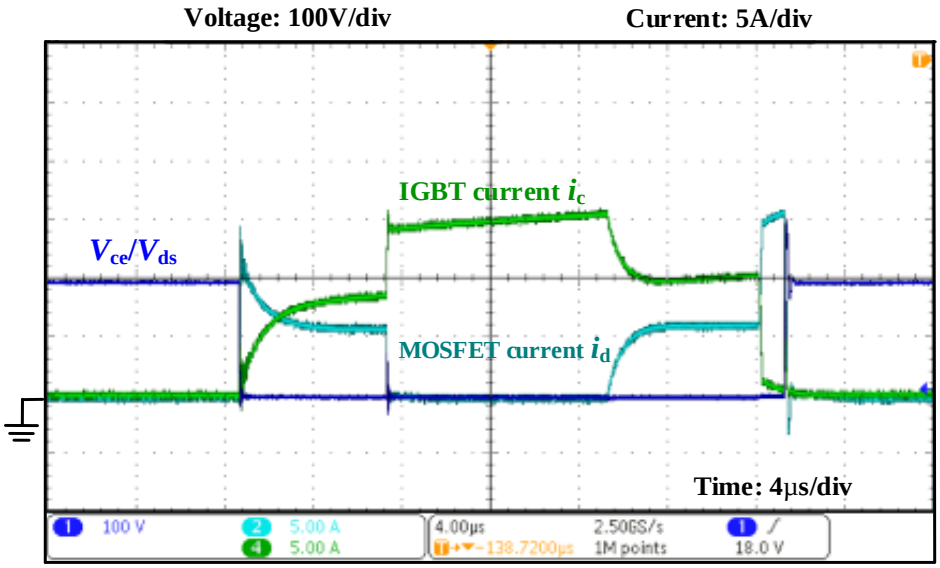


Figure 3-22 Device voltage and current waveforms at ΔT=10μs.

In Figure 3-21, when ΔT=10μs, the junction temperatures of Si IGBT and SiC MOSFET reach the balanced state which are both around 98 ºC. The device voltage and current waveforms are shown in Figure 3-22. It is noted that the additional switching of SiC MOSFET is under the zero-voltage condition, so there is no additional switching loss produced. During the period ΔT, all the load current is only conducted by the Si IGBT.

The experimental results validate the effectiveness of the proposed conduction time variation-based ATC algorithm. By using the conduction time variation-based ATC algorithm, the device junction temperature can be regulated and reach a balanced device junction temperature.

3.3.3 Switching Sequence Dispatch-Based Active Thermal Control

As analyzed in previous chapters, different switching sequences will result in different loss distributions. Using the “Si IGBT turns on first and turns off last” switching sequence, the switching loss will be produced by the Si IGBT. While using the “SiC MOSFET turns on first and turns off last” switching sequence, the switching loss will be

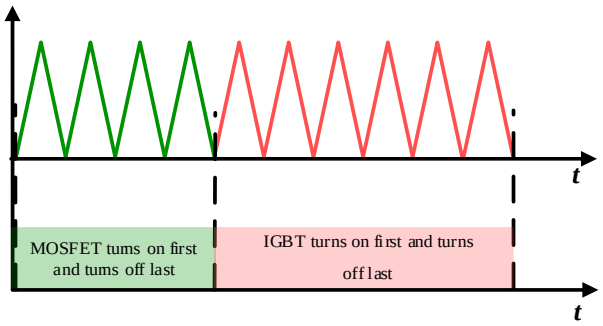


Figure 3-23 Illustration of switching sequence dispatch-based ATC algorithm.

produced by the SiC MOSFET. Based on this idea, the switching sequence dispatch-based ATC algorithm can be illustrated in Figure 3-23.

As shown in figure 3-23, every ten switching cycles are divided into two parts. In the first part, the switching sequence of "MOSFET turns on first and turns off last" will be applied to the Si/SiC HyS. In part two, the switching sequence of "IGBT turns on first and turns off last" is applied to the Si/SiC HyS. The switching loss distribution can be regulated by the ratio of each switching sequence.

Experiments were carried out to validate the effectiveness of the proposed switching sequence distribution-based ATC algorithm. The experimental platform and testing parameters are the same as that used in section 3.3.2.

The testing results are shown in Figure 3-24, it is shown that when the ratio of "IGBT turns on first and turns off last" switching sequence is 0, which means that all the switching losses are produced by the SiC MOSFET, the SiC MOSFET case temperature is around 86℃ and Si IGBT case temperature is around 77℃. The converter efficiency is about 94.85%. With the increase of the ratio of "IGBT turns on first and turns off last" switching sequence, Si IGBT case temperature increases and SiC MOSFET case temperature decreases. The converter efficiency also decreases. When the ratio is 1 which

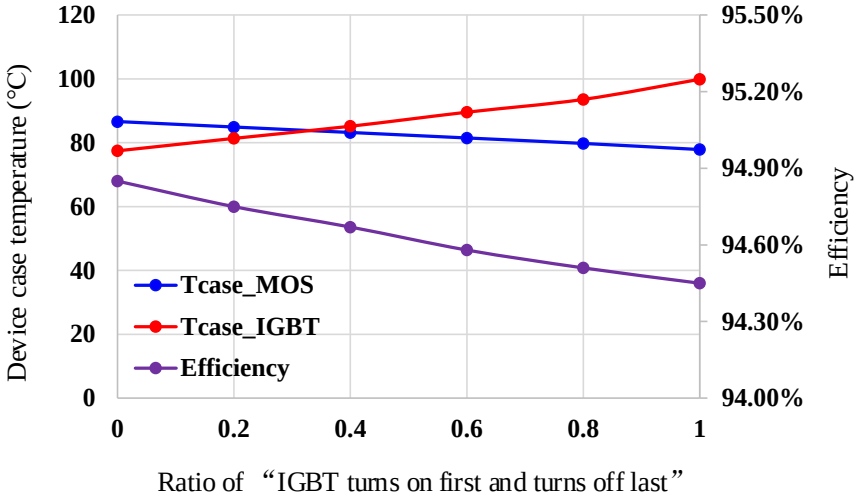


Figure 3-24 Measured device case temperature and converter efficiency vs. ratio of "IGBT turns on first and turns off last" switching sequence.

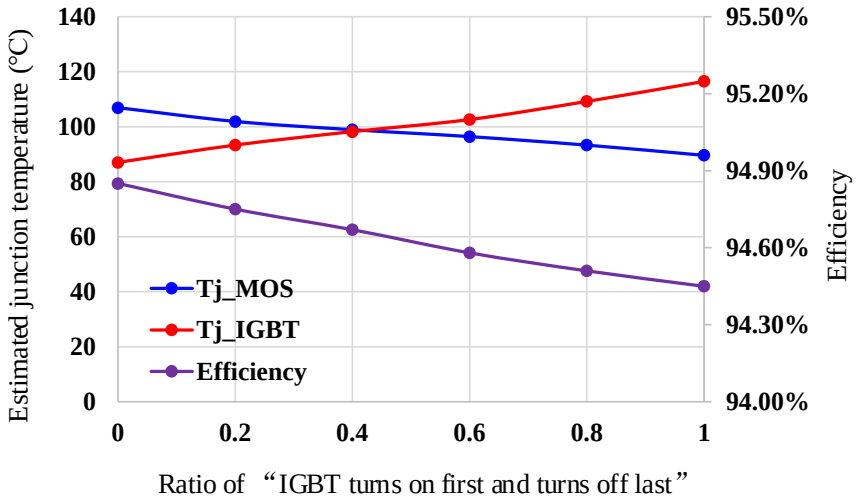


Figure 3-25 Estimated device junction temperature vs. ratio of "IGBT turns on first and turns off last" switching sequence.

means that all the switching losses are generated by the Si IGBT, the converter has the lowest efficiency which is about 94.45%

The estimated device junction temperature change under different ratio of "IGBT turns on first and turns off last" switching sequence is depicted in Figure 3-25. It is noted that when the ratio is around 0.4, the device junction temperatures are balanced which are both around 99℃ and the efficiency is about 94.67%.

The gate signals of Si IGBT and SiC MOSFET are shown in Figure 3-26. The green line in the waveform is the control signal of gate driving sequence dispatch. When the control signal is “low”, the gate driving sequence of “IGBT turns on first and turns off last" is utilized. When the control signal is “high”, the gate driving sequence of “MOSFET turns on first and turns off last” is applied to the Si/SiC HyS.

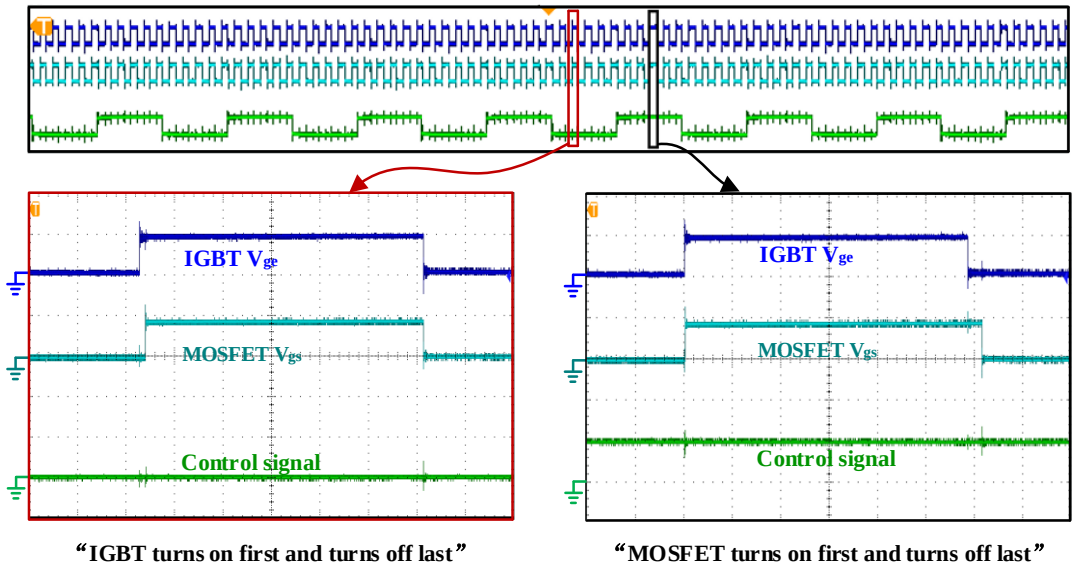


Figure 3-26 Gate driving signals of SSD-ATC.

The experimental results validate the effectiveness of the proposed switching sequence dispatch-based ATC algorithm. By using this algorithm, the device junction temperature can be actively regulated.

3.4 Summary

In this chapter, the operation optimization of Si/SiC HyS including the current ratio selection, optimal delay time selection, and the active thermal control are investigated. The experimental results show that the Si/SiC HyS semiconductor loss can be reduced by using the optimal gate delay time. The proposed CTV-ATC and SSD-ATC can effectively affect the loss distribution within the Si/SiC HyS thus regulating the device junction temperature.

In the next chapter, the converter maximum output power improvement and reliability improvement by using the proposed ATC algorithms will be investigated.

CHAPTER 4: OPERATION OPTIMIZATION OF HYBRID SWITCH-BASED CONVERTER

In section 3.3, two active thermal control methods are proposed to reduce the thermal stress of SiC MOSFET and improve the thermal performance of Si/SiC HyS. In this chapter, from the converter control level, the two active thermal control methods are utilized to improve the converter operation performance by realizing multi-objective control algorithm and improving useful lifetime. In the last part of this chapter, the converter reliability enhancement by the proposed active thermal control is evaluated.

4.1 Multi-Objective Operation Control for Hybrid Switch-Based Converter

Two control objectives are shown in Figure 4-1. When the converter output power or output current is below the threshold value, the converter will be operated in the "energy efficient mode" for high efficiency. When the converter has a heavy load or over load need, the converter will be operated in the "thermal balance mode" to increase the converter maximum output power. In the "thermal balance mode", the active thermal control methods proposed in Chapter 3 will be utilized.

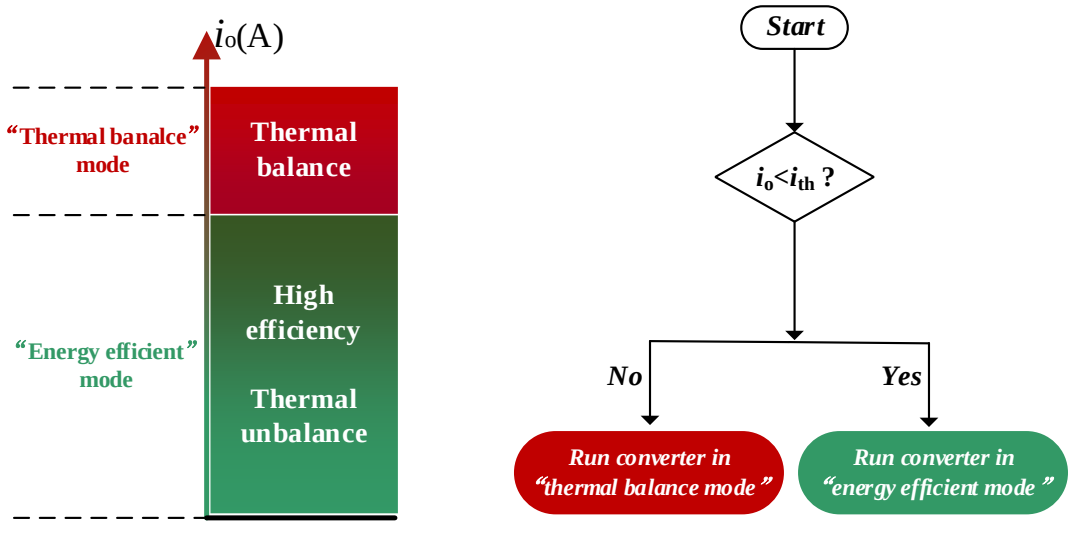


Figure 4-1 Control objectives depending on the output current.

For the DC/DC applications, for example a buck converter, the duty ratio in each switching cycle can be expressed by:

$$D = \frac{V_{out}}{V_{in}} \tag{4-1}$$

Where V_{out} and V_{in} refer to the converter output and input voltage. It is noted that the duty ratio in each switching cycle will not change in a wide range in the full power range. It is easy to implement the CTV-ATC algorithm in the digital signal processors.

The CTV-ATC method is utilized in the buck converter to realize the thermal balancing operation. Experiment was conducted to validate the proposed multi-objective control for the buck converter. The testing parameters are listed in Table 4-1. In the testing

Table 4-1 Testing parameters

Parameters	Value
Input voltage	200V
Output voltage	100V
Switching frequency	20kHz
Filter inductor	1.2mH
Output capacitor	1700μF
SiC MOSFET	C2M0280120D
Si IGBT	IKW15T120
Current threshold i_{th}	17A

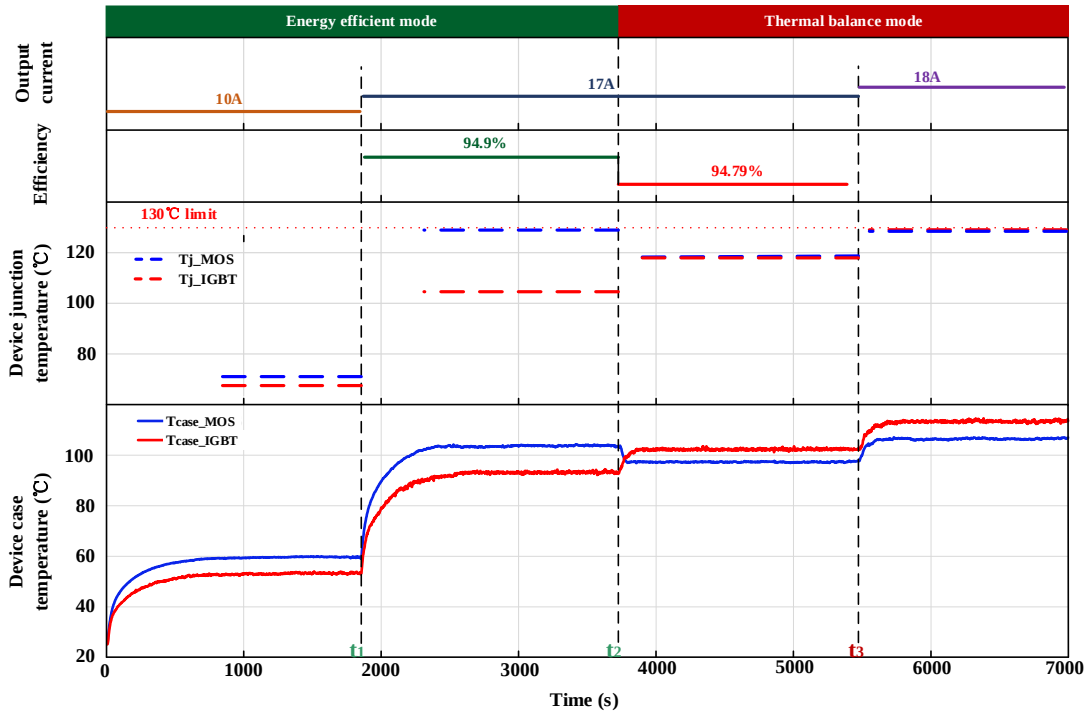


Figure 4-2 Experimental result of multi-objective operation control.

the maximum allowable device junction temperatures are limited to 130°C for both the SiC MOSFET and Si IGBT.

The testing results are shown in Figure 4-2. In the test, the device case temperatures were recorded by the data acquisition system DAQ 970A from 0 to 7000 seconds. From 0~t_2, the buck converter was operated in the "energy efficient mode". From 0~t_1, the output current is 10A. It is noted that the SiC MOSFET has the higher thermal stress and the measured case temperature of SiC MOSFET is around 60°C, the corresponding junction temperature is below 120°C. The Si IGBT junction temperature is lower. At t_1, the output power of buck converter is increased to 17A, the measured device case temperatures are about 105°C and 92°C. The junction temperatures of SiC MOSFET and Si IGBT are about 130°C and 101°C, respectively. The efficiency is 94.9%. At t_2, the control objective of the buck converter is changed to "thermal balance mode". The SiC MOSFET case temperature

decreases and the Si IGBT case temperature increases. The junction temperatures of Si IGBT and SiC MOSFET are balanced at about 108°C. The converter efficiency drops to 94.79%. At t_3, the converter output current is increased to 18A, the junction temperature of SiC MOSFET and Si IGBT both reach the 130°C limit. It is noted that under the "thermal balance mode", the buck converter maximum output power is increased by 5.9%.

4.2 Reliability-Oriented Active Thermal Control for UPS Inverter Application

In this section, to evaluate the impact of ATC on system reliability, the mission profile-based reliability enhancement evaluation for the Si/SiC HyS-based inverter in uninterruptable power supply (UPS) application is conducted. Converter reliability is affected by many factors, such as the package-level failure on bond wires and solder layers, chip-level failure on the gate oxide or body diode, and the DC-link capacitor failure [74]. In the Chapter, the SiC MOSFET bond wire remaining useful lifetime, mainly affected by the power cycling, is analyzed to evaluate the Si/SiC HyS reliability improvement by using the proposed ATC methods.

4.2.1 Reliability-Oriented Active Thermal Control

For the UPS inverter application, the duty ratio in each switching cycle can be expressed as:

$$D = M\sin(\omega t + \theta) \tag{4-2}$$

Where M is the modulation index. It is noted that the duty ratios in each switching cycle are different. So, the SiC MOSFET conduction time in each switching cycle are different. It is very complicated to implement the CTV-ATC method in a digital controller. So, for the DC/AC applications, the SSD-ATC method is used for the active thermal control.

Table 4-2 lists the system parameters of a 30kW UPS inverter simulation system, the inverter has two output power levels: 25% load and full load. When the inverter

Table 4-2 Simulation parameters

Parameters	Value
Input voltage	900V
Output voltage	480V
Switching frequency	20kHz
Filter inductor	3mH
Filter capacitor	5μF
SiC MOSFET	C3M0075120D
Si IGBT	IGW40N120H3
Rated power	30kW

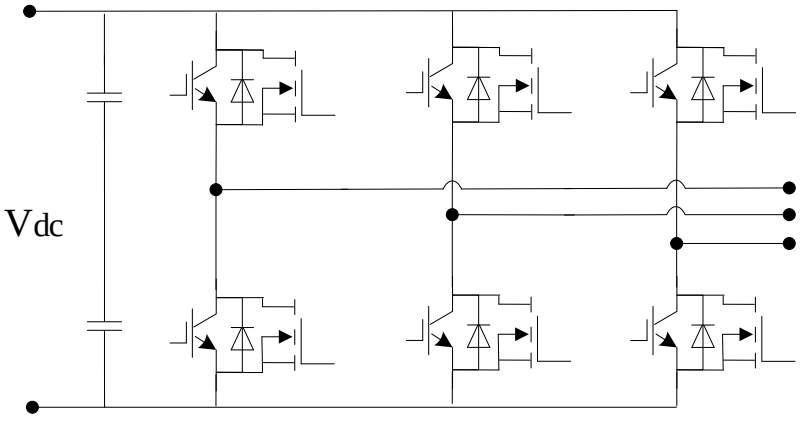
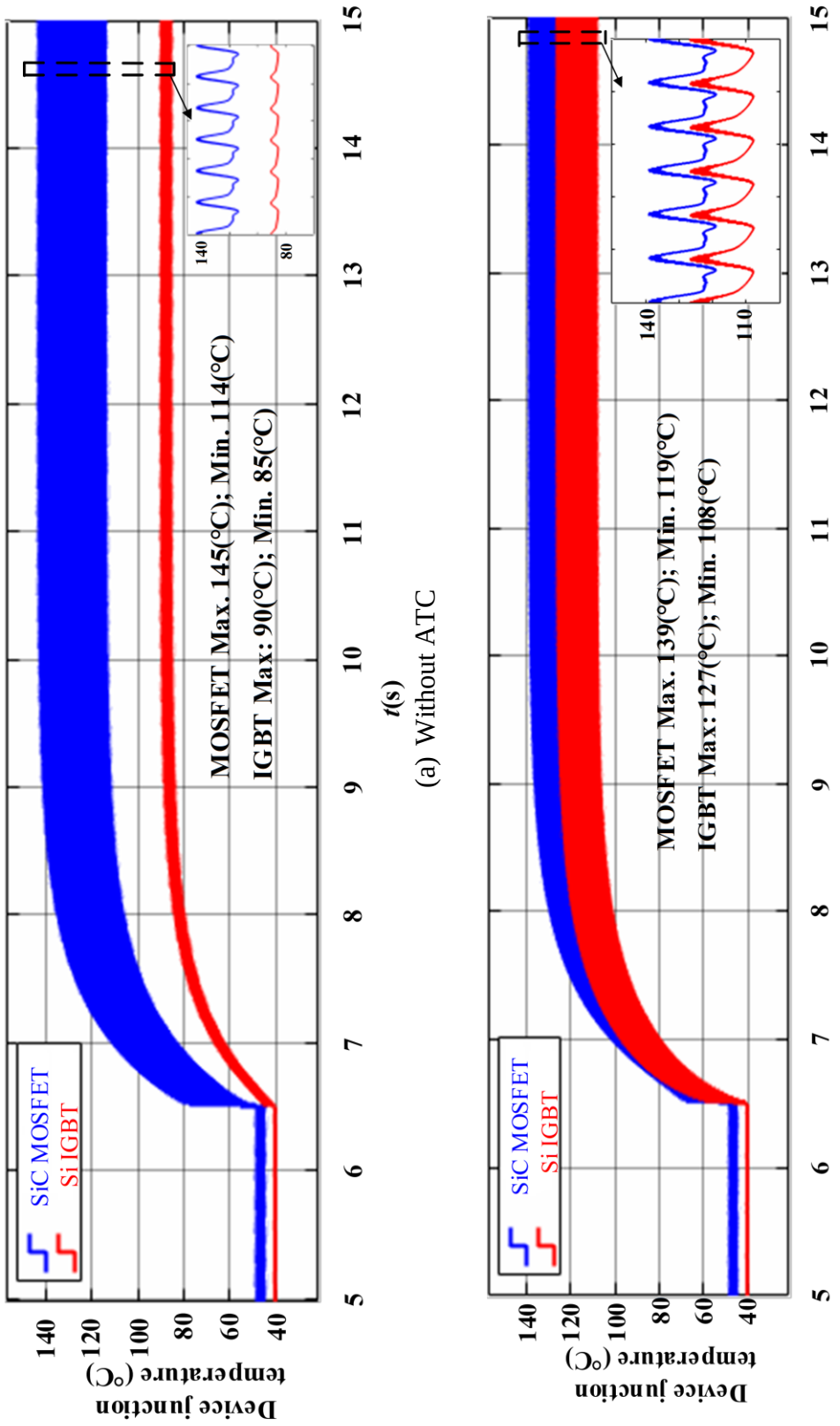


Figure 4-3 Topology of the UPS inverter.



(a) Without ATC

(b) With ATC

Figure 4-4 The device junction temperature comparison.

operates at full load, the SSD-ATC will be used to reduce the thermal stress of SiC MOSFET. The inverter topology is shown in Figure 4-3.

The simulation results of device junction temperature are shown in Figure 4-4. It is noted that when the inverter operates without the ATC, the SiC MOSFET maximum junction temperature can reach 145^{o}C and the junction temperature swing is 31^{o}C. The device junction temperature simulation results with ATC at full load are shown in Figure 4-4 (b). It is depicted that with the ATC, the SiC MOSFET maximum junction temperature is reduced from 145^{o}C to 139^{o}C and the junction temperature swing decreases from 31^{o}C to 20^{o}C. The Si IGBT junction temperature maximum value and swing are increased. In order to evaluate the impact of ATC on the inverter reliability, the device bond wire lifetime prediction-based inverter reliability assessment is investigated.

4.2.2 Bond Wire Lifetime Modeling and Damage Accumulation

The SiC MOSFET device failure modes are summarized in the Table 4-3. According to the failure positions, the SiC MOSFET device failure can be divided into two categories: chip-level failure and package-level failure.

Table 4-3 SiC MOSFET device failure modes summary

Failure position	Chip-level		Package-level	
	Gate oxide	Body diode	Bond wires	Solder layers
Failure cause	• Short circuit stress [61]-[63] • High electric filed and high temperature [64]	• High forward voltage [65]-[67]	• Thermal cycling [68]-[69]	• Thermal cycling [70]-[72]

The device failure on the SiC MOSFET gate oxide and body diode are the two common chip-level failures. Compared to the Si devices, the SiC MOSFET has higher gate voltage which results in a high electrical filed. Moreover, the SiC MOSFET has higher operating temperature which also makes the gate oxide more vulnerable [73]. Another type of chip-level failure is the body diode degradation under the high forward voltage bias stress [65]-[67]. The bond wire fatigue and solder layer degradation are the two major package-level device failures. The bond wire fatigue failure is caused by the coefficient of thermal expansion mismatch between the bond wire copper and die, as well as ohmic self-heating effects [74]. The solder layer degradation is commonly caused by the coefficient of thermal expansion mismatch between die and solder material, shear stress gradually generates the cracks and voids in the solder layer [75]. It is noted that the package-level device failure is highly affected by long-term thermal cycling profiles of the device while the chip-level failure is less affected by the long-term thermal cycling profiles. In this chapter, the active thermal control (ATC) algorithm will affect the device thermal cycling profiles, thus the package-level device failure is more suitable for the evaluation metric of the converter reliability improvement by the ATC.

For the two mostly studied package-level failures, higher junction temperature swings lead to more severe package-level failures and the bond wires degraded prior to the solder layer under the high junction temperature swing [76]. Therefore, this work focuses on the bond wire fatigue.

In literature [77]-[87], the Si IGBT bond wire remaining useful lifetime prediction has been extensively investigated. The IGBT lifetime models, for example Coffin-Manson model [87] and Bayerer's model [84], are proposed to calculate the number of cycles to

failure under a certain thermal stress condition. For the SiC MOSFET, there is no lifetime models at the moment. In some studies, the Si IGBT lifetime models were utilized for the lifetime estimation of SiC MOSFET [88]-[90]. In the recently published studies [91], [92], it is shown that neither the models can properly reflect the number of cycles to failure of SiC power devices at low-temperature swings. The SiC MOSFET lifetime could be overestimated by those models. Before a new lifetime model is proposed to accurately estimate the number of cycles to failure for SiC MOSFET, the absolute lifetime estimation for SiC MOSFET cannot be provided. But currently, those models can be used to evaluate the relative lifetime improvement by the proposed ATC algorithms, rather than an accurate lifetime estimation.

In this chapter, the Bayerer's model is used for the number of cycles to failure calculation. The number of cycles to failure is expressed as:

$$N_f = A \cdot (\Delta T_j)^{-\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{j\_\min} + 273}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot d^{\beta_6} \tag{4-3}$$

Where N_f is the number of cycles to failure. ΔT_j and T_{j_min} represent the device junction temperature swing and minimum value. t_{on}, I, V, and d represent the pulse duration, current per bond wire, voltage class, and diameter of the bond wire. The other parameters A and $\beta_1 \sim \beta_6$ are empirical and derived from curve fitting [94].

The bond wire thermal stress has two origins: the high frequency (HF) thermal cycling which comes from the 60Hz line frequency load variations and low frequency (LF) thermal cycling because of the ambient temperature change [78]. For the LF thermal cycling counting that is below 60s, it contributes to the IGBT bond wire degradation.

Typically, LF thermal cycles that is longer than 60s contribute to the baseplate solder degradation rather than bond wire degradation [78], [94].

The device accumulated damage is estimated by Miner's rule expressed in (4-4). This model assumes that the damage on the semiconductor devices is independent of the stress experienced during its life cycle [88].

$$AD = \sum_i \frac{n_i}{N_{f\_i}} \tag{4-4}$$

Where n_i is the number of thermal cycles and N_{f_i} is the corresponding cycles to failure under the n_i thermal stress.

4.2.3 Mission Profile-Based Lifetime Prediction for Si/SiC HyS

The analysis flow chart for the lifetime prediction for Si/SiC HyS is shown in Figure 4-5. The analysis process has four steps as illustrated below.

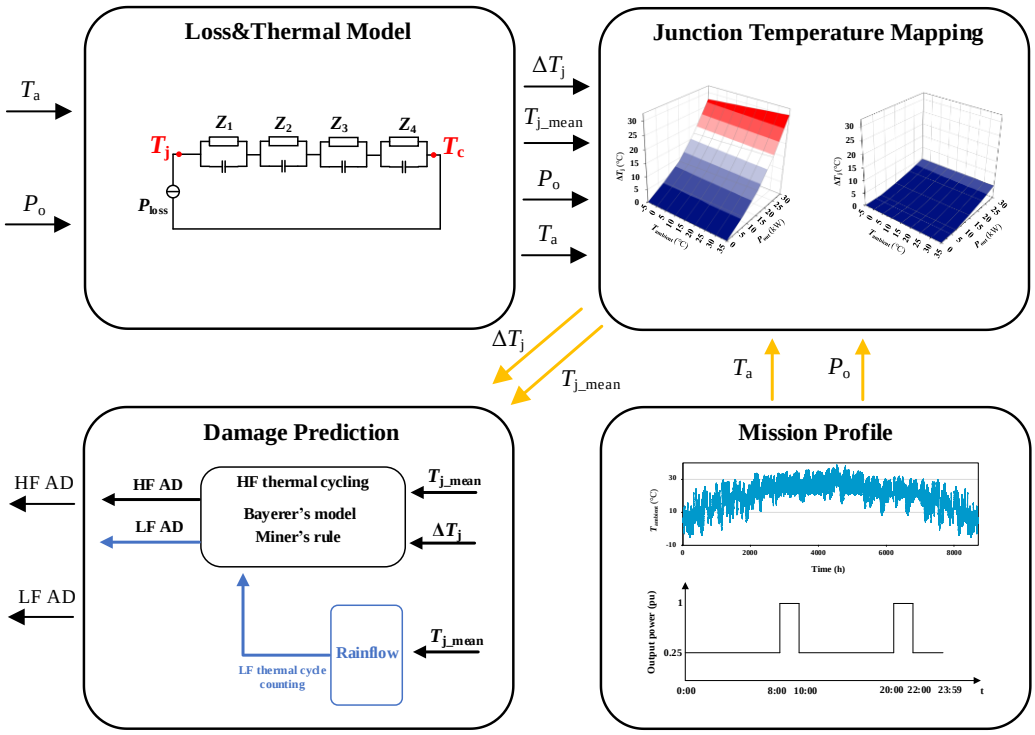


Figure 4-5 Lifetime prediction steps.

1) Step 1: junction temperature calculation. Based on the loss and thermal model for the Si/SiC HyS-based converter, the device junction temperature is calculated under different power profile and ambient temperature profile.
2) Steps 2: junction temperature mapping. 3-D look up tables including the dependency of ΔT_j on output power and ambient temperature, and the dependency of T_{j_mean} on output power and ambient temperature is generated.
3) Step 3: mission profile translation. According to literature [88], reducing the mission profile resolution from the second level to 1-2 hours does not significantly influence the damage prediction for HF thermal cycling, while drastically reducing the simulation time. Therefore, for the damage accumulation due to the HF thermal cycling, the mission profile resolution is reduced to 100s for shorter simulation time. While for the LF damage prediction, the mission profile resolution is not reduced.
4) Step 4: accumulated damage calculation. Yearly accumulated damage on the bond wire can be calculated by using the Bayerer's model and Miner's rule under the specified mission profile.

4.2.4 Mission Profile and Junction Temperature Mapping

As shown in Figure 4-6, the repetitive daily power mission profile for the UPS application is used for this work [80]. It is shown that for the UPS application, the converter will operate in light load condition in most of the day. The converter will also operate at heavy load conditions in two short intervals.

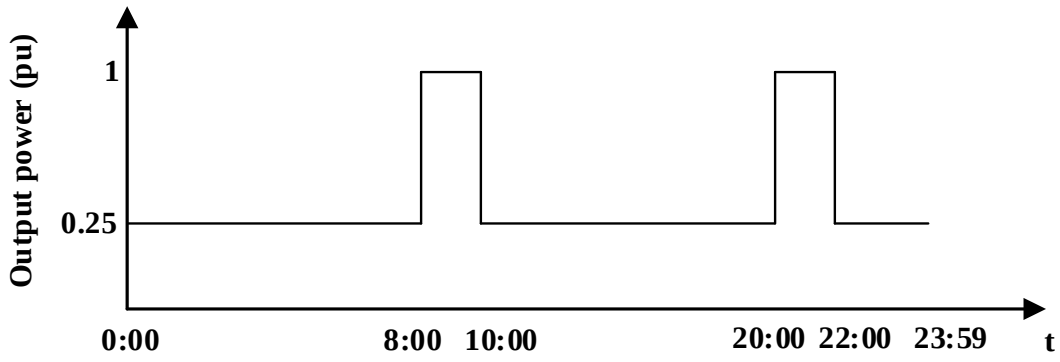


Figure 4-6 Repetitive daily power mission profile for UPS applications.

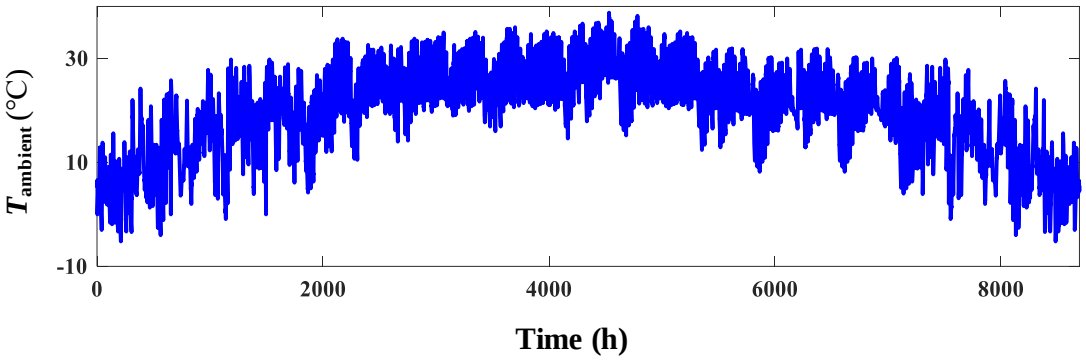
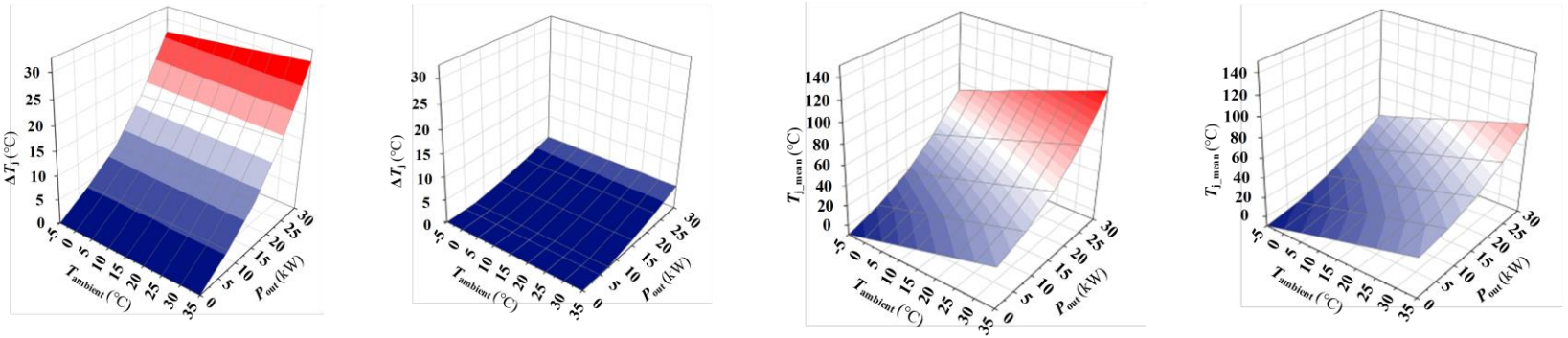


Figure 4-7 Yearly ambient temperature profile.

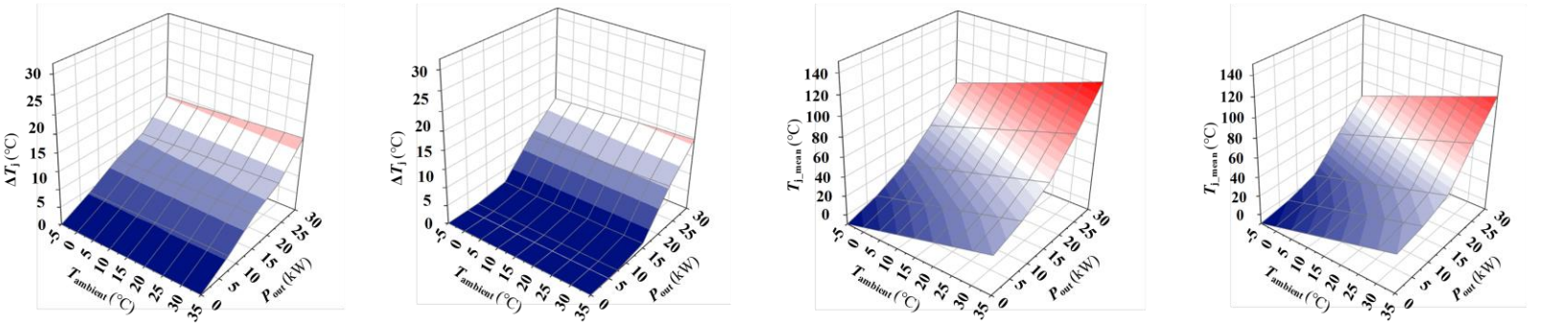
A yearly ambient temperature profile, as shown in Figure 4-7, is used for the lifetime prediction. The device ΔT_j and T_{j_mean} mapping regard to the ambient temperature and output power change is depicted in Figure 4-8. It is found that compared to not using the ATC, the device junction temperature swings ΔT_j and mean temperature T_{j_mean} become more balanced.

The yearly ΔT_j and T_{j_mean} of SiC MOSFET and Si IGBT under the mission profile are depicted in Figure 4-9 and Figure 4-10, respectively. It is shown in Figure 4-9 that the range of SiC MOSFET junction temperature swing is reduced with the proposed ATC. On the other hand, the ΔTj range of Si IGBT is increased. In Figure 4-10, the Si IGBT junction



SiC MOSFET　　Si IGBT　　SiC MOSFET　　Si IGBT

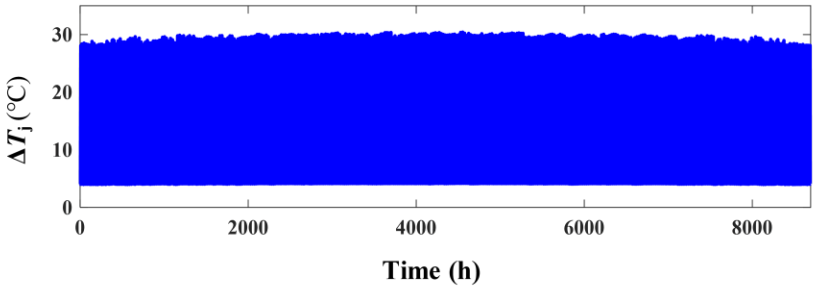
(a) Without ATC



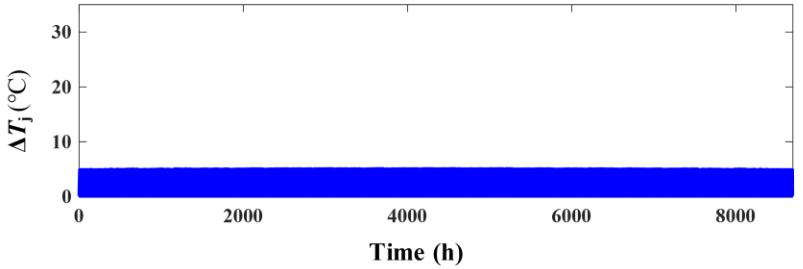
SiC MOSFET　　Si IGBT　　SiC MOSFET　　Si IGBT

(b) With ATC

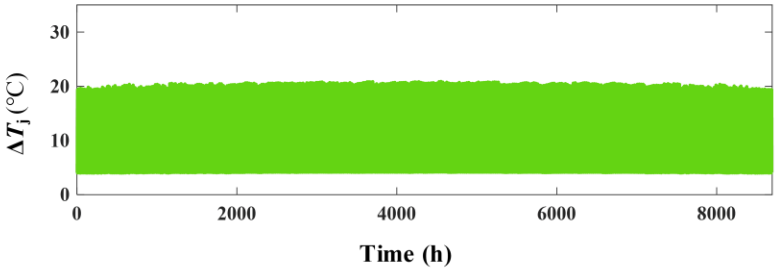
Figure 4-8 Si IGBT and SiC MOSFET ΔT_j and T_{j_mean} mapping.



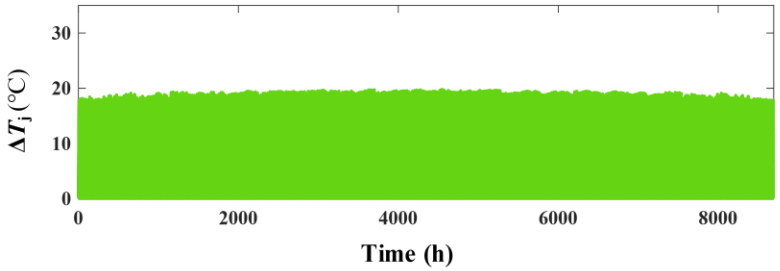
(a) SiC MOSFET yearly ΔT_j without ATC



(b) Si IGBT yearly ΔT_j without ATC

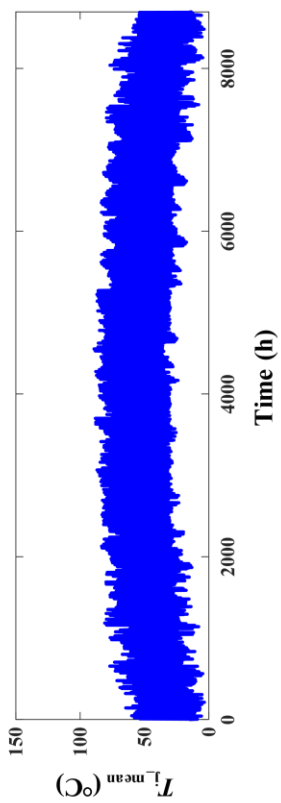


(c) SiC MOSFET yearly ΔT_j with ATC

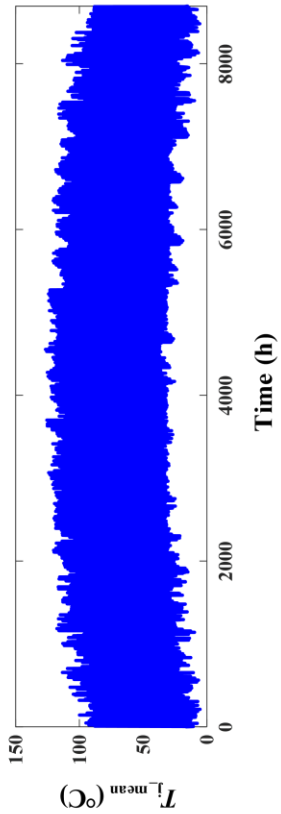


(d) Si IGBT yearly ΔT_j with ATC

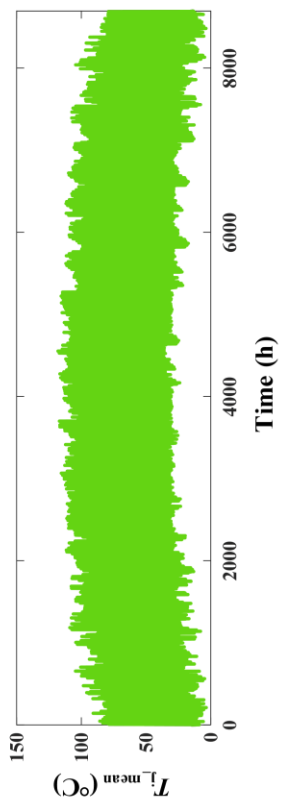
Figure 4-9 Yealy ΔT_j of Si IGBT and SiC MOSFET.



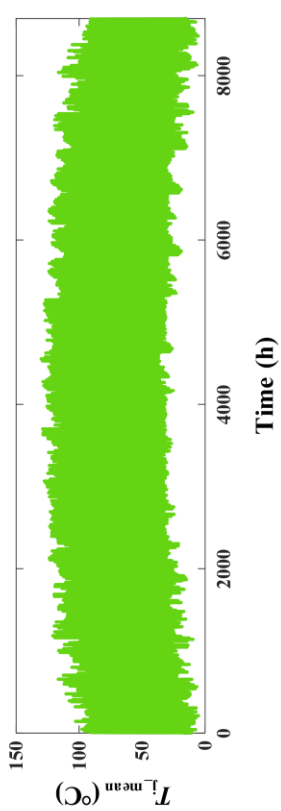
(a) SiC MOSFET yearly T_{j_mean} without ATC



(b) Si IGBT yearly T_{j_mean} without ATC



(c) SiC MOSFET yearly T_{j_mean} with ATC



(d) Si IGBT yearly T_{j_mean} with ATC

Figure 4-10 Yealy T_{j_mean} of Si IGBT and SiC MOSFET.

temperature mean value T_{j_mean} shows a significant increase compared to the values without the ATC.

4.2.5 Damage Prediction

According to (4-3) and (4-4), the yearly accumulated damage is calculated and depicted in Figure 4-11. It is shown that the LF damage contribute much less than the HF damage on the bond wire. When the ATC is not used, the yearly AD of SiC MOSFET and Si IGBT shows a significant unbalance. The system useful lifetime is limited by the SiC MOSFET. When the Si/SiC HyS operates with the ATC algorithm, it is shown that the yearly AD of SiC MOSFET is significantly reduced. Although the yearly AD of Si IGBT increases due to the high junction temperature swing, the yearly AD becomes more balanced. By using the proposed ATC algorithm, the yearly AD on the SiC MOSFET bond wire is reduced by 80%. It can be concluded that the useful lifetime of Si/SiC HyS-based inverter is extended.

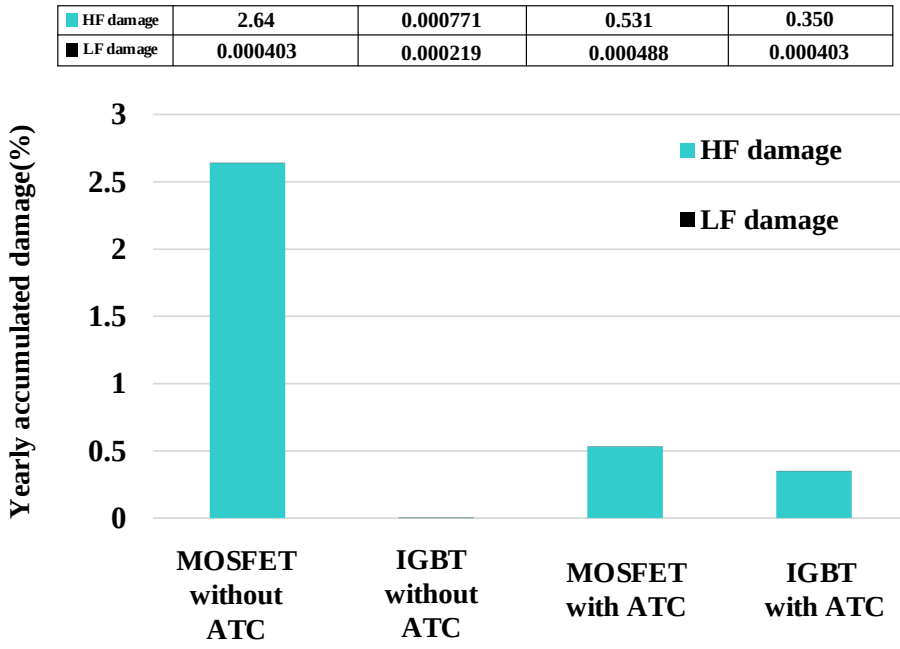


Figure 4-11 Comparison of device yearly accumulated damage between using ATC and not using ATC.

4.4 Summary

In this chapter, the multi-objective control of Si/SiC HyS-based converter was proposed. The experimental result validated that by using the proposed algorithm, the converter can operate in “energy efficient” mode for high efficiency an also can operate in “thermal balance” mode for higher output power. The converter maximum output power is improved by 5.9% by the proposed algorithm. The reliability improvement of the Si/SiC HyS-based converter was evaluated based on the bond wire damage prediction. The analysis shows that with the proposed ATC, the useful lifetime of Si/SiC HyS-based inverter is extended.

CHAPTER 5: HYBRID SWITCH-BASED 3L-ANPC INVERTER

Power inverters have been widely used in electrical vehicles (EV), photovoltaic (PV), and traction systems which play an important role in converting dc-ac powers [95] - [100]. Multilevel inverters have been a good choice for high-voltage and high-power applications. Among the multilevel inverter topologies, three-level (3L) topology is one of the most widely used solutions. Compared to the two-level (2L) inverters, the 3L inverters can operate under higher voltage and have better output power quality [101], [102]. In addition to the benefits on itself, from a system level, the positive impacts on the passive components make the 3L inverters a competitive alternative to the 2L inverters even in low-voltage applications [103].

The three-level neutral-point-clamped (3L-NPC) topology is a well-established solution for the high-voltage and high-power inverters. Among those NPC topologies, the diode clamped NPC topology has been widely used in different applications. But it suffers from the uneven loss distribution and the resulting unsymmetrical semiconductor junction temperature distribution inside the topology, which limits the inverter's switching frequency and power output capacity [104] - [106]. To resolve this problem, the three-level

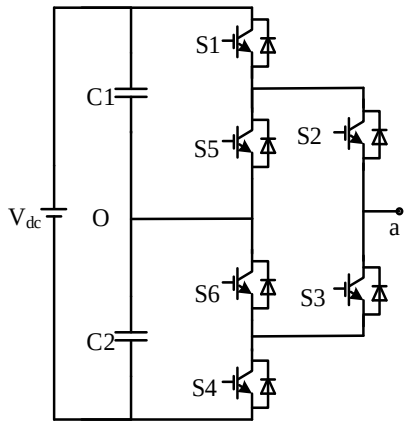
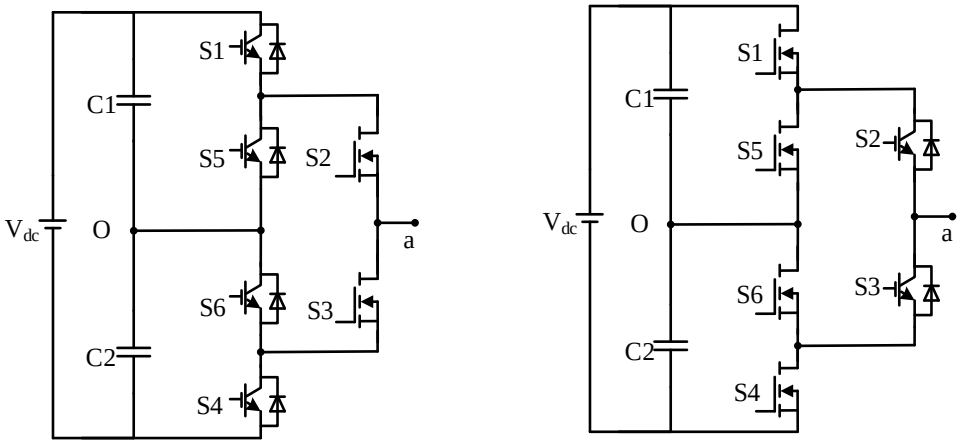


Figure 5-1 One-leg 3L-ANPC topology.

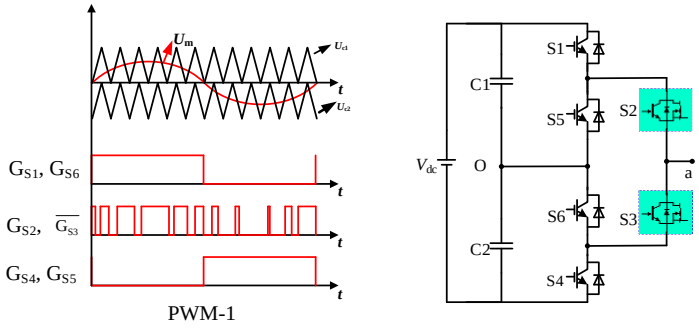
active neutral-point-clamped (3L-ANPC) topology, depicted in Figure 5-1, is derived. The clamping diodes of the diode clamped NPC topology are replaced by two active switches to obtain more midpoint clamping paths. Thus, more degrees of freedom are provided to design the inverter commutation characteristics and adjust the power loss distribution [107] - [110]. In literature [108], adjustable loss distribution (ALD) strategy which combines the loss distribution mechanism of two PWM strategies presented in [107] is proposed to regulate the high frequency switching losses between the inner and outer switches. The ALD strategy improved the thermal balance of the 3L-ANPC inverter, but Si IGBTs still generate all the switching losses. So, the inverter efficiency is not improved.

To achieve better inverter performance on the inverter efficiency, power density, and output power quality, SiC MOSFETs are utilized in the power inverters [111] – [113]. For the 3L-ANPC structure, each inverter leg consists of six active switches. A full SiC MOSFET-based 3L-ANPC inverter will significantly increase the device cost. In order to utilize the SiC benefits in 3L-ANPC structure, Si IGBT and SiC MOSFET (Si&SiC) hybrid 3L-ANPC topologies have been proposed [114], [115]. A cost-effective Si&SiC hybrid scheme for 3L-ANPC, shown in Figure 5-2 (a), is proposed in [114]. Only two active switches in each leg are replaced by SiC MOSFETs for the high frequency switching. The inverter efficiency is greatly improved by reducing the switching losses. In literature [115], 2-SiC MOSFETs and 4-SiC MOSFETs Si&SiC hybrid 3L-ANPC, depicted in Figure 5-2 (a) and Figure 5-2 (b) respectively, are proposed. The inverter efficiency, device cost, and thermal performance of the two Si&SiC hybrid schemes are analyzed and compared experimentally. The device cost has been reduced by the proposed Si&SiC hybrid schemes,

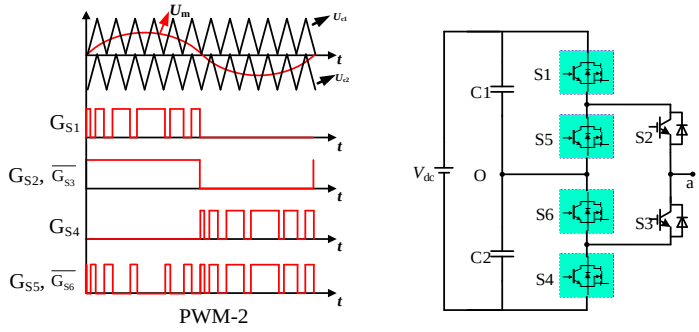


(a) With 2 SiC MOSFETs (b) With 4 SiC MOSFETs

Figure 5-2 Two types of Si&SiC hybrid 3L-ANPC topology.



(a) 2-Si/SiC HyS-based 3L-ANPC and PWM method



(b) 4-Si/SiC HyS-based 3L-ANPC and PWM method

Figure 5-3 Proposed two types of Si/SiC HyS-based 3L-ANPC inverter.

but compared to the full Si IGBT solution, the device cost for large current-rated SiC MOSFETs is still high, especially for the 4-SiC hybrid scheme.

In this chapter, two types of Si/SiC HyS-based 3L-ANPC inverter are proposed to improve the inverter efficiency while further reducing the device cost. The topology and PWM methods are illustrated in Figure 5-3. Comparisons are made between the proposed two types of Si/SiC HyS-based 3L-ANPC inverter. The inverter efficiency improvement is evaluated experimentally.

5.1.2-Si/SiC HyS-Based 3L-ANPC Topology

The 2-Si/SiC HyS-based 3L-ANPC inverter, as illustrated in Figure 5-3 (a), utilizes PWM-1 modulation strategy. When the inductor current is positive, the commutation process is demonstrated in Figure 5-4 and introduced below.

1) During the "P" state, S1 and S2 are turned on to output $+V_{dc}/2$. S6 is also turned on to clamp the blocking voltage of S3 and S4 to $+V_{dc}/2$. At this state, the SiC MOSFET of S2 is turned on first to commutate the inductor current. After the turn-on delay time, the Si IGBT of S2 is turned on by ZVS and shares the current with SiC MOSFET. At the end of "P" state, the Si IGBT of S2 is turned off first through ZVS. As a result, all the current is forced to the SiC MOSFET of S2. After the turn-off delay time. The SiC MOSFET of S2 is turned off. The SiC MOSFET of S2 produces switching losses.

2) During the deadtime, the current is commutated by S6 and the diode of S3.

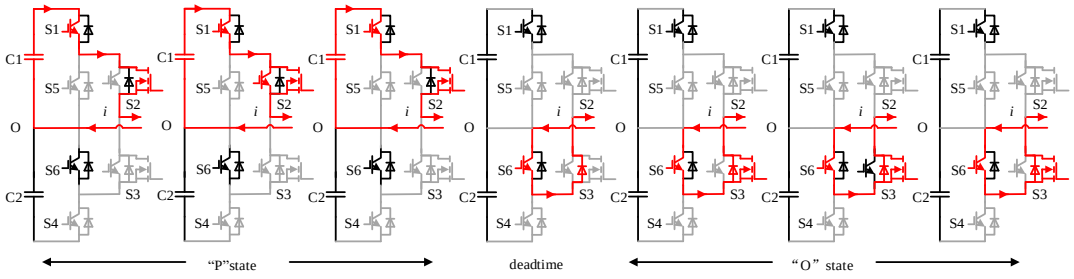


Figure 5-4 Commutation analysis of 2-Si/SiC HyS-based 3L-ANPC inverter from "P" state to "O" state at positive inductor current.

3) During the “O” state, the SiC MOSFET of S3 is turned on first and operates at synchronous rectifier mode. After the turn-on delay time, Si IGBT of S3 is turned on. Since the Si IGBT cannot conduct current reversely, the current distribution is unchanged till the S2 is turned off. The diode of S3 generates recovery losses.

When the inductor current is negative, the commutation process is demonstrated in Figure 5-5.

1) At “P” state, the SiC MOSFET of S2 is turned on first and operates at synchronous rectifier mode to share the current with the diode of S2. After the turn-on delay time, the Si IGBT is turned on, but it will not conduct current. When S2 is about to be turned off, the Si IGBT is turned off first. Then, the SiC MOSFET of S2 is turned off after the turn-off delay time. All the current is forced to the diode of S2.
2) During the deadtime, the current is commutated by the diodes of S2 and S1. At the end of deadtime, the diode of S2 produces recovery losses.
3) During the “O” state, the SiC MOSFET of S3 is turned on first. After the turn-on delay time, Si IGBT of S3 is turned on through ZVS to share the current with SiC MOSFET of S3. At the end of the “O” state, Si IGBT of S3 is turned off

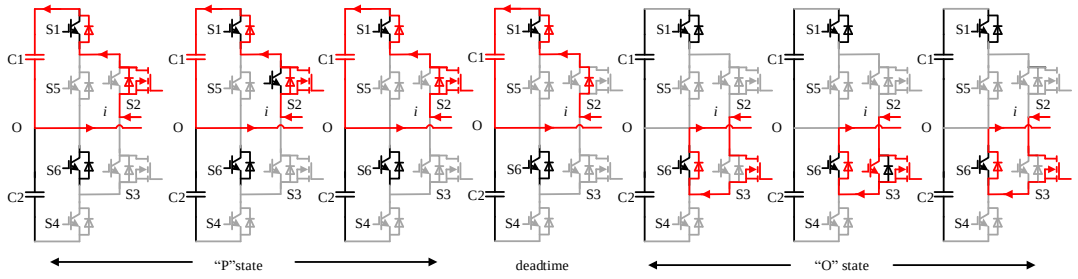


Figure 5-5 Commutation analysis of 2-Si/SiC HyS-based 3L-ANPC inverter from “P” state to “O” state at negative inductor current.

by ZVS. Then, the SiC MOSFET of S3 is turned off after the turn-off delay time. SiC MOSFET of S3 generates switching losses.

5.2.4-Si/SiC HyS-Based 3L-ANPC Topology

As depicted in Figure 5-3 (b), the 4-Si/SiC HyS-based 3L-ANPC inverter utilizes PWM-2 modulation strategy. When the inductor current is positive, the commutation process is demonstrated in Figure 5-6 and introduced below.

1) During the "P" state, S1 and S2 are turned on to output $+V_{dc}/2$. S6 is also turned on to clamp the blocking voltage of S3 and S4 to $+V_{dc}/2$. At this state, the SiC MOSFET of S1 is turned on first to commutate the inductor current. After the turn-on delay time, the Si IGBT of S1 is turned on through ZVS and shares the current with SiC MOSFET. At the end of "P" state, the Si IGBT of S1 is turned off first by ZVS. All the current is forced to the SiC MOSFET of S1. After the turn-off delay time. The SiC MOSFET of S1 is turned off and produces switching losses.
2) During the deadtime, the current is commutated by S2 and the diode of S5.
3) During the "O" state, the SiC MOSFET of S5 is turned on first and operates at synchronous rectifier mode. After the turn-on delay time, Si IGBT of S5 is

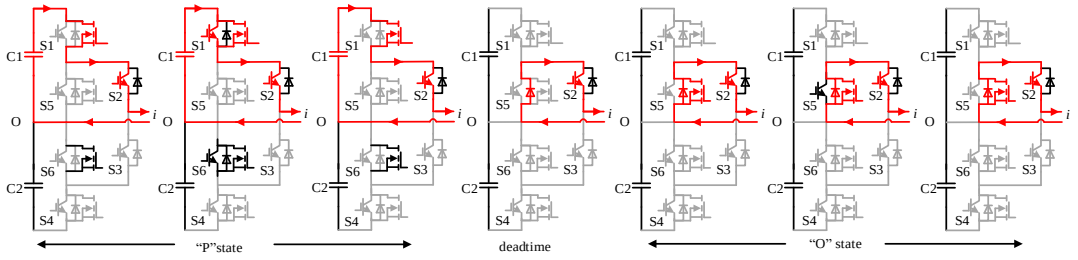


Figure 5-6 Commutation analysis of 4-Si/SiC HyS-based 3L-ANPC inverter from "P" state to "O" state at positive inductor current.

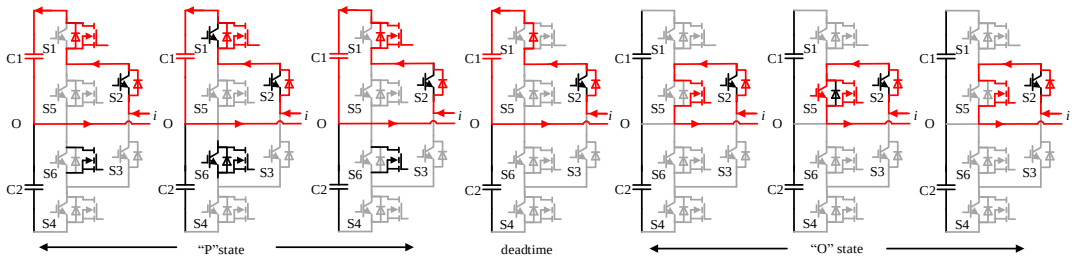


Figure 5-7 Commutation analysis of 4-Si/SiC HyS-based 3L-ANPC inverter from "P" state to "O" state at negative inductor current.

turned on but does not conduct current. The current distribution is unchanged till the S5 is turned off. The diode of S5 produces recovery losses.

When the inductor current is negative, the commutation process is demonstrated in Figure 5-7.

1) At "P" state, the SiC MOSFET of S1 is turned on and operates at synchronous rectifier mode to share the current with the diode of S1. After the turn-on delay time, the Si IGBT is turned on, but it will not conduct current. When S1 is about to be turned off, the Si IGBT is turned off first. After the turn-off delay time, the SiC MOSFET of S1 is turned off. All the current is forced to the diode of S1.
2) During the deadtime, the current is commutated by the diodes of S1 and S2. When the deadtime period ends, the diode of S1 produces recovery losses.
3) During the "O" state, the SiC MOSFET of S5 is turned on first. After the turn-on delay time, Si IGBT of S5 is turned on through ZVS and shares the current with SiC MOSFET. At the end of "O" state, Si IGBT of S5 is turned off through ZVS. After the turn-off delay time, The SiC MOSFET of S5 is turned off and produces switching losses.

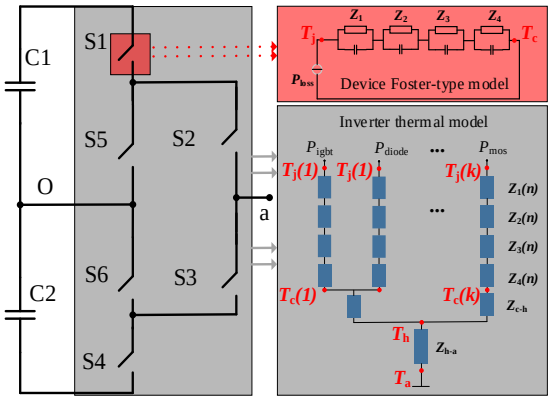


Figure 5-8 Thermal model structure for the 3L-ANPC inverter.

5.3 Thermal Modeling

Based on the Si/SiC HyS loss model, the 3L-ANPC inverter total loss can be calculated by:

$$P_{loss}(n) = \sum_{m=1}^{6} P_m\,(n) = \sum_{m=1}^{6}\left[P_{m\_switch}(n) + P_{m\_con}(n)\right] \tag{5-1}$$

$$P_{\text{loss\_ave}} = \frac{f_{\text{line}}}{f_s}\sum_{n=1}^{\frac{f_s}{f_{line}}} P_{\text{loss}}(n) \tag{5-2}$$

Where $P_{\text{loss(n)}}$ is the total inverter loss in the n_{th} switching cycle. $P_{\text{m\_switch}}$(n), $P_{\text{m\_con}}$(n), and P_{m}(n) are the average switching loss, average conduction loss, and average total loss of switching device S_{m} in the n_{th} switching cycle. To precisely estimate the device junction P_{m}(n) should be used as the device loss profile. In equation (5-2) $P_{\text{loss\_ave}}$ is the inverter average loss in the line frequency scale. f_{s} and f_{line} refer to the switching frequency and line frequency.

The thermal model for the 3L-ANPC inverter is presented in the Figure 5-8. Four layers Foster-type RC network representing the thermal model from device junction to case is utilized to model the semiconductor devices. The Foster model only consists of lumped RC values and no physical meanings. In the system thermal model, each device has one

more layer from device case to the heatsink $Z_{c\text{-}h}$, which represents the thermal impedance of thermal pad and the thermal grease. The antiparallel diode is packaged along with the Si IGBT, thus they share one device case and have one $Z_{c\text{-}h}$.

With a proper assumed initial temperature of heatsink, case, or ambient and the thermal parameters provided by manufacturer's datasheets, the device's junction temperature can be estimated by

$$T_j = P_{loss} \sum_{m=1}^{4} Z_m + T_c = P_{loss} \sum_{m=1}^{4} \frac{R_m}{\tau_{ms}+1} + T_c \tag{5-3}$$

Where T_j, P_{loss}, and T_c are respectively the junction temperature, pulse power loss profile, and case temperature.

5.4 Inverter Performance Evaluation

Based on loss and thermal models, the inverter loss breakdown between the two types of Si/SiC HyS-based 3L-ANPC can be obtained. In this section, the semiconductor loss comparison is firstly made between the full Si IGBT-based 3L-ANPC inverter, 2-Si/SiC HyS-based 3L-ANPC inverter, and 4-Si/SiC HyS-based 3L-ANPC inverter. Then,

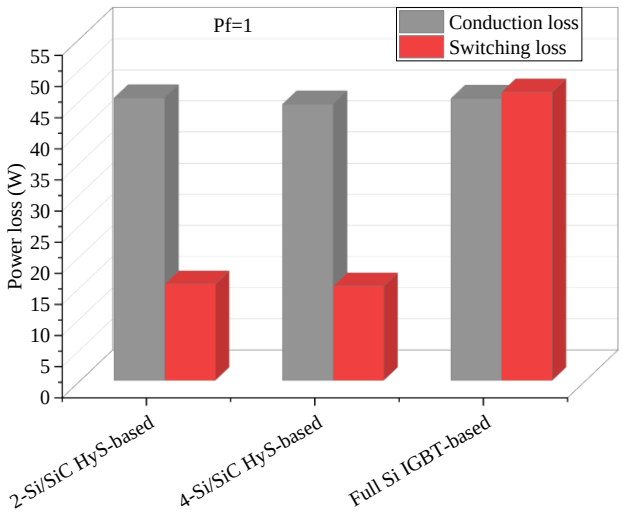


Figure 5-9 Loss comparison of different 3L-ANPC inverter solutions.

Table 5-1 System parameters

Parameter	Value
Dc voltage, V_{dc}	750V
Switching frequency, f_s	40kHz
Output ac voltage V_o	220V/50Hz
Output power, P_o	4.4kW
T_{on_delay}, T_{off_delay}	1μs, 1μs

the semiconductor loss breakdowns are analyzed. Next, the power output capability is evaluated and compared between the two types of Si/SiC HyS-based 3L-ANPC inverters.

The comparisons are made under the system parameters shown in Table 5-1. In the comparison, the Si/SiC HyS is formed by one Rohm SiC MOSFET SCT3120AL (650 V / 15 A) and one Infineon Si IGBT IKW20N60T (600 V / 28 A). The full current-rated Si IGBTs utilized in the 3L-ANPC is Infineon IKW30N60T (600 V / 39 A).

Figure 5-9 shows the semiconductor loss comparison between the 2-Si/SiC HyS-based 3L-ANPC, 4-Si/SiC HyS-based 3L-ANPC, and the full Si IGBT-based 3L-ANPC inverters. It is illustrated in the figure that the conduction losses are almost the same between the three inverters. This is decided by the V-I characteristics of the semiconductor devices. Benefiting from the fast-switching characteristic of SiC MOSFET, the switching losses of the Si/SiC HyS-based 3L-ANPC inverters are much lower than the full Si IGBT-based solution. For the two Si/SiC HyS-based 3L-ANPC inverters, all the switching losses are produced by the Si/SiC HyS, thereby they have the same switching losses.

The loss breakdown for the 2-Si/SiC HyS-based 3L-ANPC inverter is shown in Figure 5-10. Since the 3L-ANPC inverter operates symmetrically between the top devices

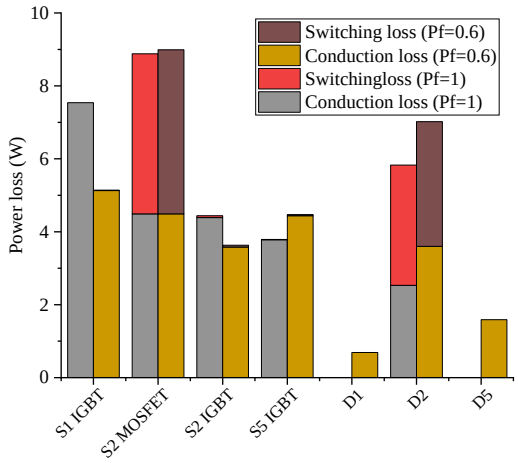


Figure 5-10 Loss breakdown for 2-Si/SiC HyS-based 3L-ANPC inverter.

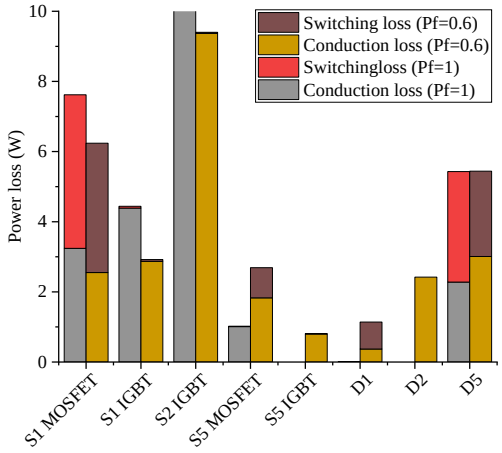


Figure 5-11 Loss breakdown for 4-Si/SiC HyS-based 3L-ANPC inverter.

S1, S2, S5, and the bottom device S4, S3 S6, only the top three devices' losses are calculated and presented. It is noted that all the switching losses and recovery losses are produced by the SiC MOSFETs and the antiparallel didoes of S2, respectively. The other four Si IGBTs only produce conduction losses. When the power factor changes from 1 to 0.6 (lagging), the conduction losses produced by S1 IGBT decrease, and the conduction losses generated by the diodes increase. The switching losses are still produced by the middle two switches S2 and S3. For the loss breakdown of 4-Si/SiC HyS-based 3L-ANPC

inverter, shown in Figure 5-11, when inverter operates at unity power factor, all the switching losses and recovery losses are produced by the SiC MOSFET in S1 and the diode of S5. When it operates at a lower power factor, the switching losses are distributed between the SiC MOSFETs of S1 and S5. The recovery losses are also shared by D1 and D5. The theoretical loss calculation validates that the proposed PWM strategies effectively concentrate all switching losses to the SiC MOSFETs in the Si/SiC HyS-based 3L-ANPC topology.

Based on the loss breakdown analysis of the two types of Si/SiC HyS-based 3L-ANPC inverters, it is also noted that for the 2-Si/SiC HyS-based 3L-ANPC inverter, S1 IGBT, S2 MOSFET, and D2 have higher thermal stress than other devices. In the 4-Si/SiC HyS-based 3L-ANPC inverter, S1 MOSFET, S2 IGBT, and D5 have higher thermal stress than other devices. Thermal performance is an important factor for power inverters. Unbalanced thermal distribution will not only affect the inverter reliability but limit the inverter output capacity. In order to compare the power output capability of the two Si/SiC HyS-based 3L-ANPC inverters, the device junction temperatures are estimated and compared based on the thermal and loss model.

From the device's datasheet, the maximum allowable junction temperature for both the Si IGBTs and the SiC MOSFET are 175 ℃. The inverter maximum output capacity can be found at the point of the most heated device in the topology reaching the 175 ℃ limit. Assuming the heatsink temperature is 80 ℃, the device junction temperatures can be estimated with the power loss profile for each semiconductor devices.

The junction temperature of the two types of Si/SiC HyS-based 3L-ANPC inverter under different power levels are calculated and depicted in Figure 5-12. It is shown that the

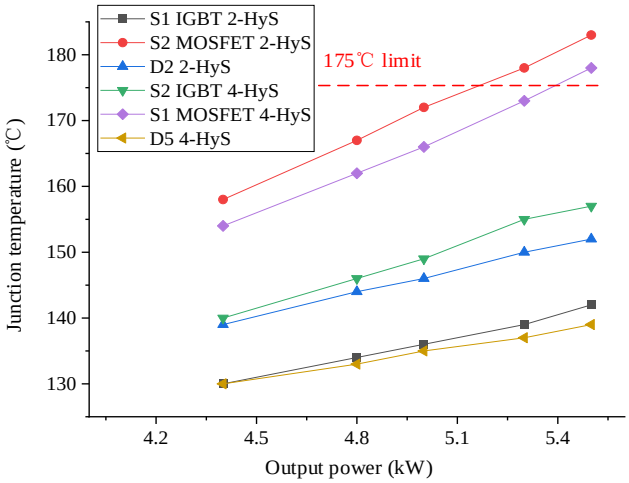


Figure 5-12 Device junction temperature estimation under different output power.

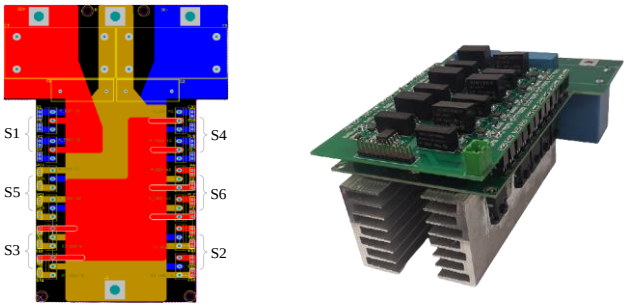


Figure 5-13 Single-phase universal 3L-ANPC experimental prototype.

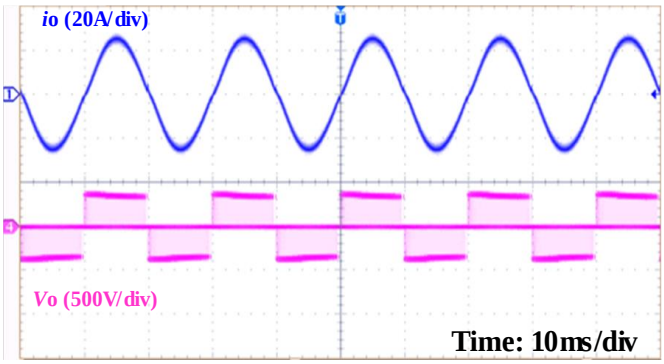
SiC MOSFETs are always the most heated devices in the two hybrid schemes. With the increase of inverter output power, the 2-Si/SiC HyS-based 3L-ANPC reaches the limit firstly with the output power of 5.17kW. While the maximum output power for 4-Si/SiC HyS-based 3L-ANPC is 5.4kW which is limited by S1 SiC MOSFET. The results show that the 4-Si/SiC HyS-based 3L-ANPC inverter has a higher power output capacity. It is more suitable for high power density applications.

To validate the efficiency benefits from the Si/SiC HyS and further investigate the switching and conduction characteristics of the Si/SiC HyS in the continuous inverter operation, a single-phase universal 3L-ANPC inverter, as shown in Figure 5-13 was

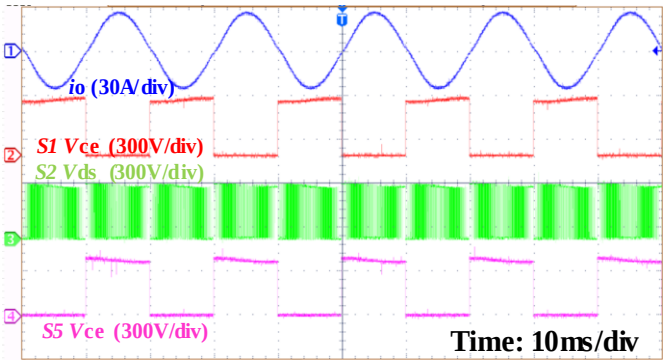
developed to evaluate the feasibility of the proposed Si/SiC HyS-based 3L-ANPC inverters. The testing parameters are listed in Table 5-2. The inverter efficiency was measured with Tektronix power analyzer PA3000. Rogowski coil current sensor TRCP0300 was utilized to measure the Si IGBT and SiC MOSFET drain-source current.

The normal operation of the Si/SiC HyS-based 3L-ANPC inverters are tested and the waveforms are shown in Figure 5-14. The three-level output voltage and current, depicted in Figure 5-14 (a), show that the inverter output voltage has three levels: $+V_{dc}/2$, 0, $-V_{dc}/2$ and the inverter has sinusoidal output current. It is noted that the inverter output voltage and current are unrelated to the 3L-ANPC hybrid schemes and the modulation methods. The drain-source voltage of S1, S2, and S5 for the two types of Si/SiC HyS-based 3L-ANPC inverter are shown in Figure 5-14 (b) and Figure 5-14 (c), respectively. In Figure 5-14 (b), it is noted that S1 and S5 switch at the line frequency (50Hz). The inner switch S2 switches at high frequency. In Figure 5-14 (c), although the gate signal of S1 and S2 are kept constant low in the negative half cycle, the drain-source voltage of S1 and S2 still have two levels. This is because, in the negative half cycle, S5 switches in high frequency with S4. When S4 is turned on, S1 and S2 are clamped to block the voltage $+V_{dc}/2$. When S5 is turned off, S5 and S2 are connected in parallel and in series with S1 to block the voltage $+V_{dc}/2$. Thus, the voltage of $+V_{dc}/2$ is divided based on the off-state equivalent RC networks of S1, S2, and S5.

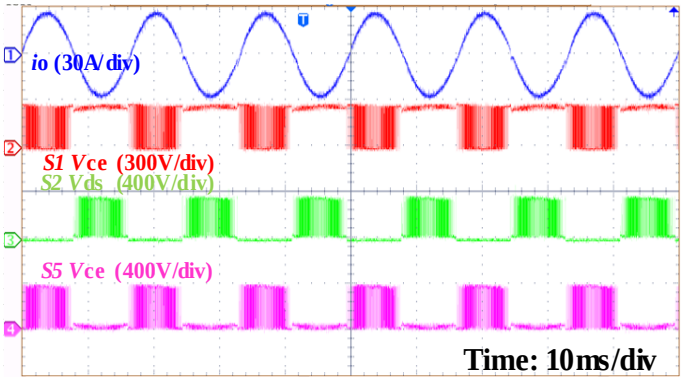
The Si/SiC HyS switching waveforms of forward conduction are depicted in Figure 5-15 (a). The inductor current flows forward through the Si/SiC HyS. It is noted that during the turn-on process, the SiC MOSFET is turned on first. After the 1μs turn-on delay time, the Si IGBT is turned on under the SiC MOSFET's conduction voltage which can be seen



(a) Inverter output voltage and current



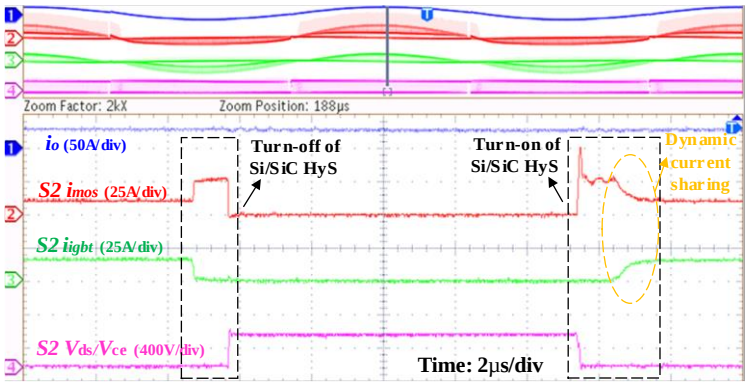
(b) 2-Si/SiC HyS-based 3L-ANPC



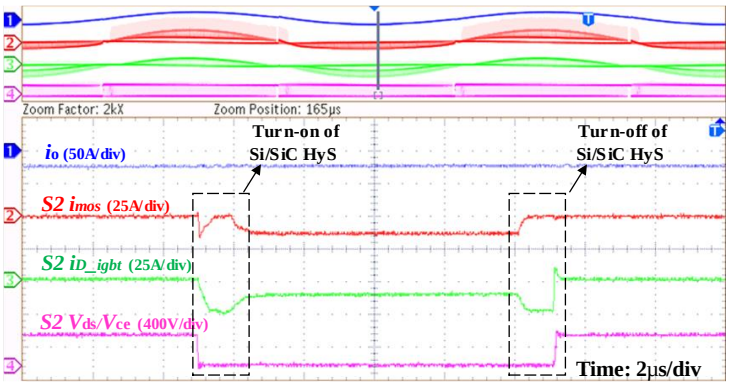
(c) 4-Si/SiC HyS-based 3L-ANPC

Figure 5-14 Inverter normal operation waveforms.

as a zero-voltage turn-on. After the Si IGBT's turn-on, a dynamic current sharing process which is caused by the parasitic inductance in the internal power loop of Si/SiC HyS is observed. In Figure 5-15(a), the dynamic current sharing process takes about 1.2μs. During



(a) Forward conduction



(b) Reverse conduction

Figure 5-15 Si/SiC HyS switching waveforms.

the turn-off process, Si IGBT is turned off first. After 1µs turn-off delay time, the SiC MOSFET is turned off.

The switching waveforms of reverse conduction are shown in Figure 5-15 (b). The inductor current flows through the Si/SiC HyS in the reverse direction. In the turn-on transient, the SiC MOSFET body diode and the antiparallel diode of Si IGBT commutate the inductor current. Then, due to the low conduction voltage of the antiparallel diode of Si IGBT, the current shared by the antiparallel diode increases and the current shared by body diode of SiC MOSFET decreases. After the dead time, SiC MOSFET is turned on, and the MOSFET channel starts to share current with the antiparallel diode of Si IGBT. In

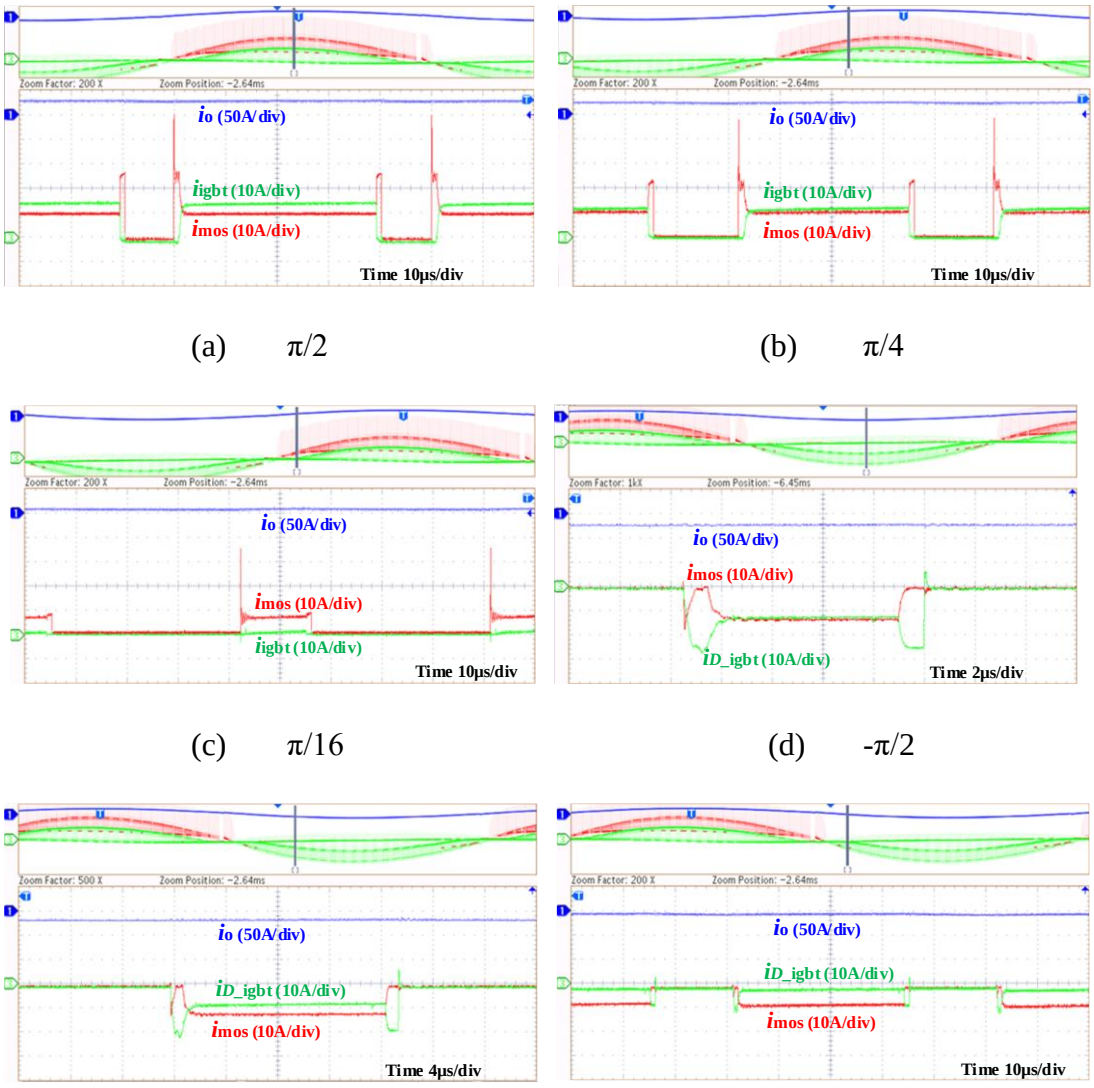


Figure 5-16 Steady state current sharing of the Si/SiC HyS.

the turn-off process, SiC MOSFET is turned off and all the current is commutated by the antiparallel diode during the dead time. Recovery losses are produced by the antiparallel diode.

The steady state current sharing of Si/SiC HyS is shown in Figure 5-16. The forward conduction current sharing waveforms at π/2, π/4, and π/16 of the output current are shown in Figure 5-16 (a), (b), and (c) respectively. It is noted that at the peak point of

the output current, Si IGBT shares more current than the SiC MOSFET. At π/4, the current ratio shared by Si IGBT decreases. At π/16, all the current is conducted by SiC MOSFET. The Si IGBT will not conduct since the conduction voltage is lower than the Si IGBT threshold voltage. Figure 5-16 (d), (e), and (f) show the current sharing in the reverse conduction of Si/SiC HyS. The antiparallel diode shares current with the SiC MOSFET during the conduction. Like the forward conduction, at high current, the diode shares more current. With the decrease of load current, the current ratio shared by SiC MOSFET increase. The results shown in Figure 5-16 validate the advantage of Si/SiC HyS in conduction characteristics. It is noted that the Si/SiC HyS has no threshold voltage when conducting low currents. This will help to improve the inverter light load efficiency. When conducting high current, Si IGBT will share more current and thus reducing the conduction voltage. This will help to improve the inverter overload capability.

The inverter efficiencies are tested under the parameters listed in Table 5-2. Figure 5-17 demonstrated the inverter efficiency improvement by the Si/SiC HyS for the 3L-ANPC inverter. It is shown that the efficiencies of the two Si/SiC HyS-based 3L-ANPC inverters are very close in the full load range, but their efficiencies are both much higher than the full Si IGBT solution. Especially when the switching frequency increases, the Si IGBT solution shows a more significant efficiency drop. At 40 kHz switching frequency, the inverter efficiency improvement by the Si/SiC HyS is 2.4% and 1.8% at light load and heavy load conditions, respectively.

Figure 5-18 shows the inverter efficiency comparison between the all SiC MOSFET 3L-ANPC solution, SiC MOSFET hybrid 3L-ANPC solution which is shown in Figure 5-2 (a) and Figure 5-2(b), and the proposed Si/SiC HyS-based 3L-ANPC solution.

Table 5-2 Testing parameters

Parameter	Value
Dc voltage, V_{dc}	750V
Output ac voltage V_o	220V/50Hz
Output power P_r	4.4kW
Switching frequency f_s	20kHz, 40kHz
Filter inductor L_f	1mH
Filter capacitor C_f	5μF
T_{on_delay}, T_{off_delay}	1μs, 1μs
R_g for SiC MOSFET	7Ω
R_g for Si IGBT	10Ω
V_{gs} for SiC MOSFET	+18V/0V
V_{ge} for Si IGBT	+15V/-9V
Si/SC HyS	SCT3120AL (650 V / 15 A)+ IKW20N60T (600 V / 28 A)
Full Si IGBT	IKW30N60T (600 V / 39 A)
Full SiC MOSFET	SCT3030AL (650 V / 49 A)

It is shown that all SiC MOSFET solution has the overall highest inverter efficiency. While the Si/SiC HyS-based 3L-ANPC solutions have the lowest efficiency, especially in the heavy load condition. A larger efficiency drop is observed in the heavy load condition. Small current-rated SiC MOSFET is used as the switching device in the Si/SiC HyS solution. The thermal stress of SiC MOSFET in the Si/SiC HyS solutions will be much higher than the full current-rated SiC MOSFETs at the thermal steady state. Thus, the conduction and switching losses increase of the small current-rated SiC MOSFET is larger.

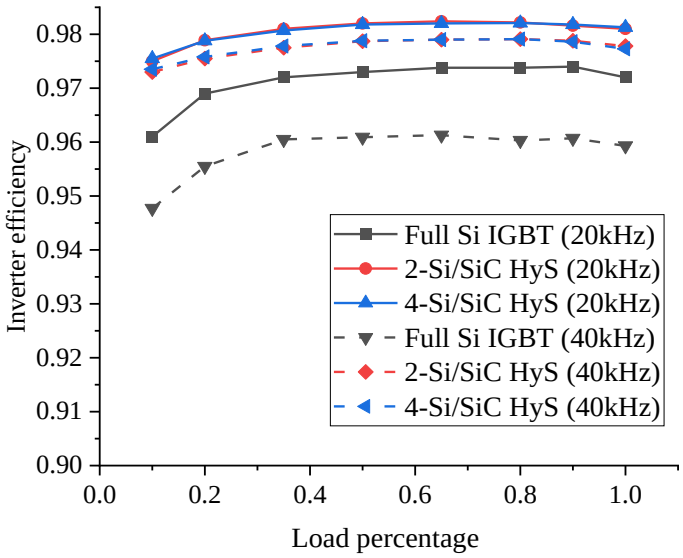


Figure 5-17 Inverter efficiency improvement evaluation.

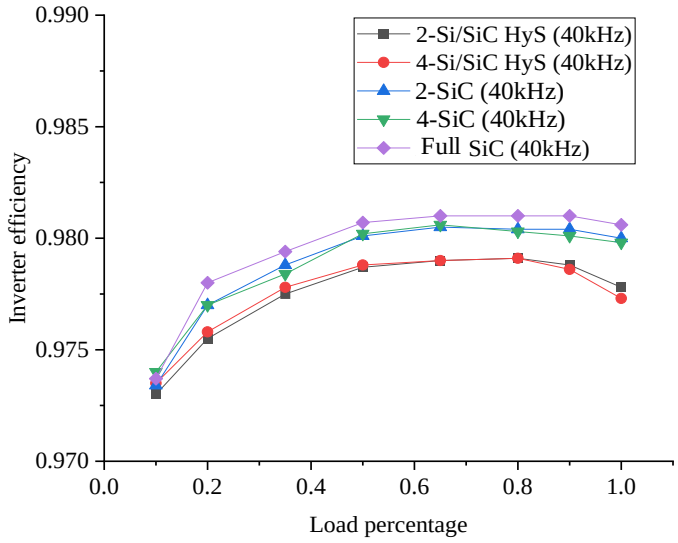


Figure 5-18 Inverter efficiency comparison between different 3L-ANPC solutions.

In addition, in the Si/SiC HyS 3L-ANPC solution, the recovery losses of Si diode will also increase a lot due to the temperature rise. While for the other three solutions, full current-rated SiC MOSFETs are utilized. Usually, the SiC MOSFET with a higher current rating

has a lower junction to case thermal resistance. For the example in this paper, the SiC MOSFET used in Si/SiC HyS is SCT3120AL (650 V/15 A), which has a junction to case thermal resistance of 1.12℃/W and the full current-rated SiC MOSFET used in the comparison is SCT3030AL (650 V/49 A), which has a junction to case thermal resistance of 0.44℃/W. The thermal stress of the larger SiC MOSFET will be lower than the SiC MOSFET in the Si/SiC HyS. Thus, the power loss increased by the rise of temperature is lower. In addition, the SiC MOSFET body diode commutates the load current during the dead time and will not produce any recovery losses.

The device cost comparison between different 3L-ANPC solutions is made and presented in Table 5-3. The device costs are from Mouser Electronics on a bulky order of 1000 pieces. It is shown that the full Si IGBT solution has the lowest device cost and the full SiC MOSFET solution has the highest device cost which is about 6.5 times the full Si IGBT solution. Compared to the 2-SiC hybrid scheme, the 4-SiC hybrid 3L-ANPC has a

Table 5-3 Device cost comparison between different 3L-ANPC solutions

Configuration	Per leg cost / Pu
Full Si IGBT (IKW30N60T)	$17.9 / 1
Full SiC MOSFET (SCT3030AL)	$116.6 / 6.5
2-SiC hybrid	$50.8 / 2.8
4-SiC hybrid	$83.7 / 4.7
2-Si/SiC HyS scheme	$25.8 / 1.4
4-Si/SiC HyS scheme	$33.8 / 1.9

Table 5-4 Comparison two Si/SiC HyS-based 3L-ANPC solution

	Full Si IGBT 3L-ANPC (benchmark)	2-Si/SiC HyS-based 3L-ANPC	4-Si/SiC HyS-based 3L-ANPC
Inverter efficiency	94.7% at light load, 95.6% at heavy load	2.4% improvement at light load, 1.8% improvement at heavy load	2.4% improvement at light load, 1.8% improvement at heavy load
Power capability	4kW	5.17kW	5.4kW
Device cost/kW	4.48$/kW	4.99$/kW	6.26$/kW
Features	Most cost effective, lower efficiency and power density	Cost effective and high efficiency	High power density, high power capacity, and high efficiency

1.7 times device cost while only showing an almost identical inverter efficiency. Compared to the full current-rated SiC MOSFET hybrid solution, the proposed Si/SiC HyS-based 3L-ANPC inverter shows a significantly lower device cost. The 2-Si/SiC HyS scheme only has 1.4 times device cost compared to the full Si IGBT solution.

5.5 Summary

In this chapter, two Si/SiC HyS-based 3L-ANPC hybrid schemes are proposed. The inverter commutation characteristics, loss and thermal model, device cost, efficiency, and thermal performance comparison are investigated and presented. The evaluation results are concluded in Table 5-4 and illustrated as follows.

1) The inverter efficiency of the two proposed Si/SiC HyS-based 3L-ANPC inverters are very close in the full load range. Compared to the full Si IGBT-based 3L-ANPC inverter, the two types of Si/SiC HyS-based 3L-ANPC inverter both have a much higher inverter efficiency, especially when switching frequency increases. At 40kHz switching frequency, the inverter efficiency improvement by the Si/SiC HyS can achieve 2.4% and 1.8% at light load and heavy load condition respectively. Meanwhile, the device cost/kW for 2-Si/SiC HyS-based 3L-ANPC inverter is only 1.11 times of full Si IGBT solution.
2) Compared with the full SiC MOSFET solution, the device cost of 2-Si/SiC HyS scheme has been reduced by 78% while the maximum inverter efficiency sacrifice is only 0.28%. Compared with the 2-SiC MOSFET hybrid 3L-ANPC, the device cost is reduced by 50% with 0.21% maximum inverter efficiency drop at heavy load. The 2-Si/SiC HyS-based 3L-ANPC inverter shows great potential in improving the 3L-ANPC inverter's efficiency while maintaining a low device cost. This makes it a great candidate for cost-sensitive applications.
3) Compared to the 2-Si/SiC HyS-based 3L-ANPC inverter, the 4-Si/SiC HyS scheme has a higher power output capability, making it a better candidate for high power density applications.

5.6 Application Example -- 2 Si/SiC HyS-Based 3L-ANPC Battery Inverter for Energy Storage Integration

PV array and energy storage voltages have increased from 600 V to 1000 V with some up to 1500 V. The PV industry is facing significant need to integrate energy storage to mitigate the solar intermittence and provide load peak shaving and solar generation

shifting. The 1500 V voltage enables a higher voltage DC distribution, thus significantly reduce the conductor size and lower distribution losses. The higher DC voltage trend places increased demands on performance, functionality, and efficiency of battery inverters. The energy storage industry has significant need to develop a 1500 V battery inverter with high efficiency at wide load range, smaller form factor while still maintain cost competitive

For the 1500 V DC voltage application, the semiconductor device can be selected from the 3300 V (two-level topology), and 1200 V (three-level or higher) candidates. It is obvious that the 3300 V device for 1500 V voltage class is oversized on the breakdown voltage. Thus, the three-level topology with 1200 V devices is the optimal solution. Based on the comparison made in Table 5-3, the most cost-effective and high efficiency topology 2 Si/SiC HyS-based 3L-ANPC is selected.

5.6.1 Inverter Design

To implement a high-power density and high-efficiency Si/SiC HyS-based 3L-ANPC inverter, practical considerations including the semiconductor device selection, Si/SiC die-size optimization, DC bus-bar design, and thermal design are investigated.

As shown in Figure 5-19, the one-phase topology consists of four pure Si IGBTs and two Si/SiC HyS devices. To realize a high efficiency inverter design with high power

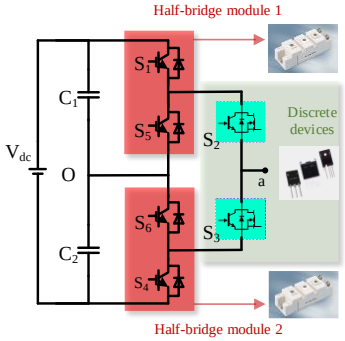


Figure 5-19 Semiconductor device selection.

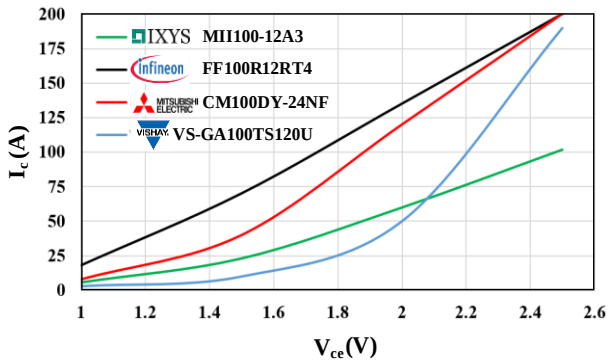


Figure 5-20 Conduction loss comparison between the half-bridge IGBT modules.

density, half-bridge Si IGBT modules are used for the upper two switches S1, S5, and the lower two switches S4, S6. Discrete Si IGBTs and SiC MOSFETs are utilized to form the hybrid switches S2 and S3.

The V_{ce}-I_c characteristics are compared among the four 1200V/100A Si IGBT module candidates, including MII100-12A3 [116] from IXYS, FF100R12RT4 [12] from Infineon, CM100DY-24NF [117] from Mitsubishi, and VS-GA100TS120U [118] from Vishay. As shown in Figure 5-20, the Infineon half-bridge module FF100R12RT4 has the lowest conduction loss. It is to be noted that the switching losses of the four Si IGBT modules are not considered in this analysis since they will not produce high frequency switching losses in this topology. The Si/SiC HyS is designed according to the algorithm proposed in Chapter 3. The discrete devices selected here are: Infineon 1200 V / 75 A Si IGBT IKQ75N120CT2 and Wolfspeed 1200 V / 24 A SiC MOSFET C2M0080120D.

Four 900 V/310 µF film capacitors are connected in a 2×2 configuration to form the 1500 V/310 µF DC capacitor bank. The PCB-based busbar, as shown in Figure 5-21, has four layers. The “DC-” bus is connected to the Si IGBT half-bridge modules in the top layer. Next, the mid-layer 1 and mid-layer 2 connect the neutral point “O” and Si IGBT half-bridge modules. Finally, the bottom layer is used for the “DC+” connection. In Figure

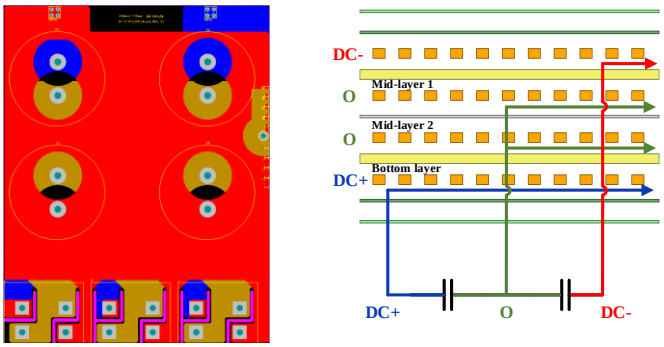


Figure 5-21 PCB-based DC busbar.

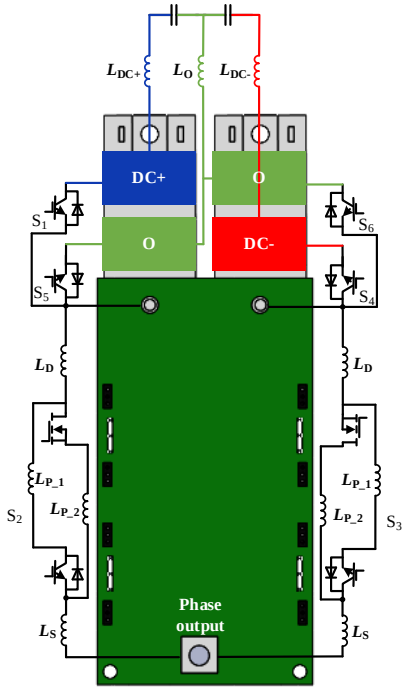


Figure 5-22 One-phase connection between the Si IGBT half bridge modules and the Si/SiC HyS half bridge board.

5-22, a two-layer PCB is designed to implement the Si/SiC HyS half-bridge S2 and S3. In Figure 5-22, L_{DC+}, L_O, L_{DC-}, L_D, L_{p_1}, L_{p_2}, and L_s represent the stray inductance in the power loop.

As shown in Figure 5-23, two separate heatsinks named “Heatsink_IGBT” and “Heatsink_HyS” are used to dissipate the heat produced by IGBT modules and Si/SiC HyS

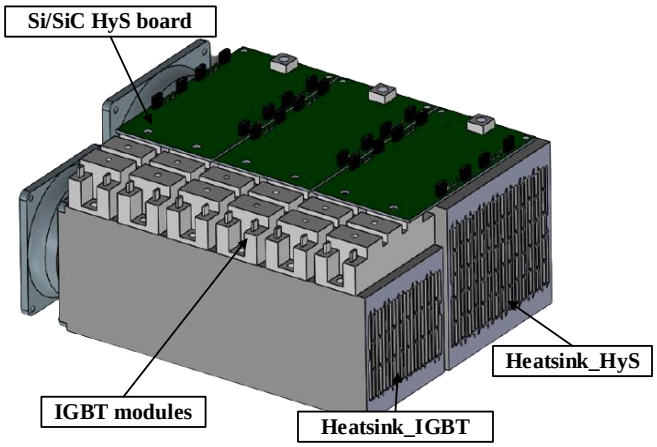


Figure 5-23 Power block with heatsinks.

Table 5-5 Simulation parameters

Parameters	Value
DC input voltage	1500 V
Output voltage	480 V_{rms}
Switching frequency	18 kHz
Turn on delay	1 µs
Turn off delay	1 µs

devices respectively. In the proposed Si/SiC HyS-based 3L-ANPC inverter, the SiC MOSFETs are the most thermal stressed devices due to the designed PWM strategy and gate driving sequence of the Si/SiC HyS. Therefore, the thermal parameters of "Heatsink_HyS" should be carefully designed to ensure the safe operation of SiC MOSFETs. The SiC MOSFET junction temperatures are estimated based on the thermal simulation tool PLCES with the simulation parameters listed in Table 5-5. In the simulation, the power device is modeled as a four layers Foster-type RC thermal model, from the junction to case, and one layer of the case to heatsink. Each layer of the RC impedance only consists of the lumped RC values and has no physical meaning. The power device thermal impedance of case to junction and the case to heatsink (thermal grease and thermal

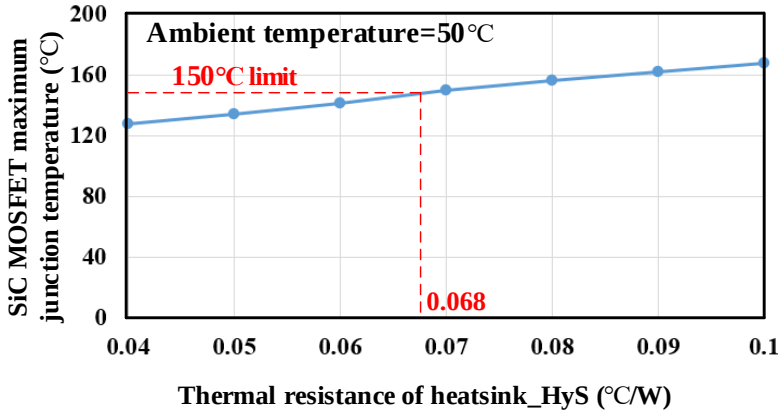


Figure 5-24 Relationship between thermal resistance and the SiC MOSFET maximum junction temperature.

pad) and heatsink to ambient are considered. The four layers Foster-type RC thermal model parameters are from the transient thermal impedance provided by the manufactures' datasheets.

Under the parameters listed in Table 5-5, the simulation results are shown in Figure 5-24. It is noted that with the increase of thermal resistance of "Heatsink_HyS", the SiC MOSFET maximum junction temperature also increases. When the thermal resistance of "Heatsink_HyS" is 0.068 ºC/W, the SiC MOSFET junction temperature reaches its maximum allowable value 150 ºC. Therefore, to ensure the SiC MOSFETs operate safely, the thermal resistance of the selected "Heatsink_HyS" should be smaller than 0.068 ºC/W.

Based on the analysis above, two heatsinks with thermal resistance 0.055℃/W and 0.085℃ /W are used for the Si/SiC HyS board and Si IGBT modules. In order to validate the effectiveness of the thermal design, the simulations are carried out. The thermal simulation results shown in Figure 5-25 show that the SiC MOSFET has the highest device junction temperature which is 139 ºC. The Si IGBT modules have lower device thermal stress. All the devices' maximum junction temperatures are under the 150 ºC limit. It is

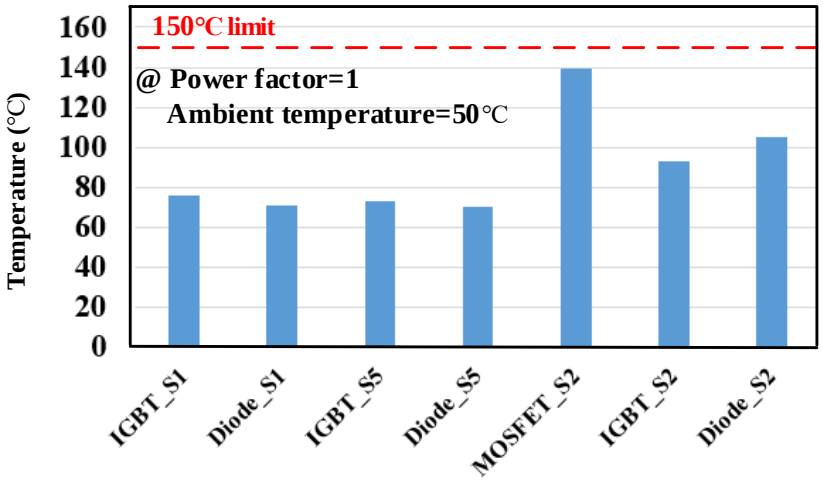


Figure 5-25 Device junction temperature simulation results.

Table 5-6 Testing parameters

Parameters	Value
DC input voltage	900 V ~ 1200 V
Output voltage	480 V_{rms}
Output current	5 kW ~30 kW
Load inductance	1 mH
Turn-on delay	0
Turn-off delay	1 µs
Switching frequency	18 kHz

verified that the thermal design for the inverter can successfully keep all the semiconductor devices junction temperature under the limit value when the inverter operates at rated power and frequency.

5.6.2 Experimental Test

The implemented 40 kW three-phase HyS-based 3L-ANPC inverter prototype is shown in Figure 5-26. The dimensions of the prototype are 18.1 inches long, 11.3 inches wide, and 5.4 inches tall. The experimental setup is shown in Figure 5-27. The controller board for the platform consists of the Texas Instruments (TI) 28379 controlCARD and

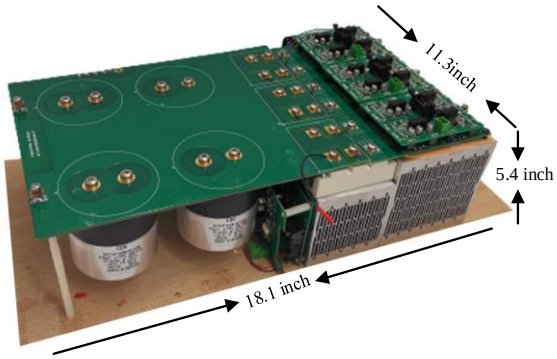


Figure 5-26 Implemented 40kW three-phase Si/SiC HyS-based 3L-ANPC inverter prototype.

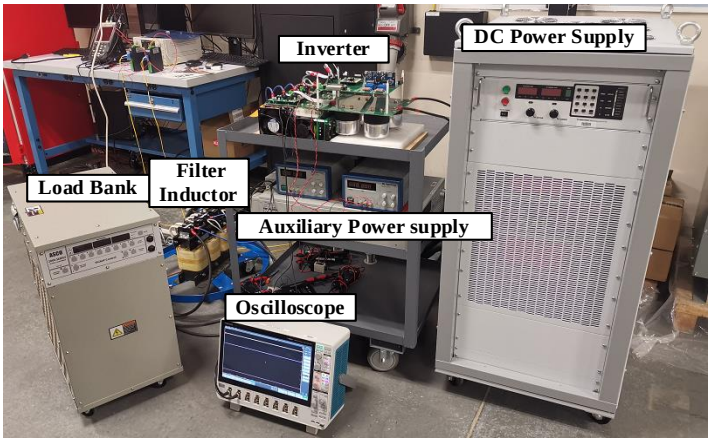


Figure 5-27 Experimental setup.

Altera CPLD EPM240T100I5N. Gate signals which are generated by the TI 28379 controlCARD are sent to the CPLD to add the turn-on and turn-off delay for the Si/SiC HyS. The testing parameters are summarized in Table 5-6.

The experimental current and voltage are measured by the 8-channel Tektronix oscilloscope. As shown in Figure 5-28, the second waveform from the bottom of the figure shows the five-level line to line inverter output voltage. The three-phase line voltage and current on the load side are shown in the first two waveforms in the figure. The line voltage and the phase current have a 30^{o} phase shift.

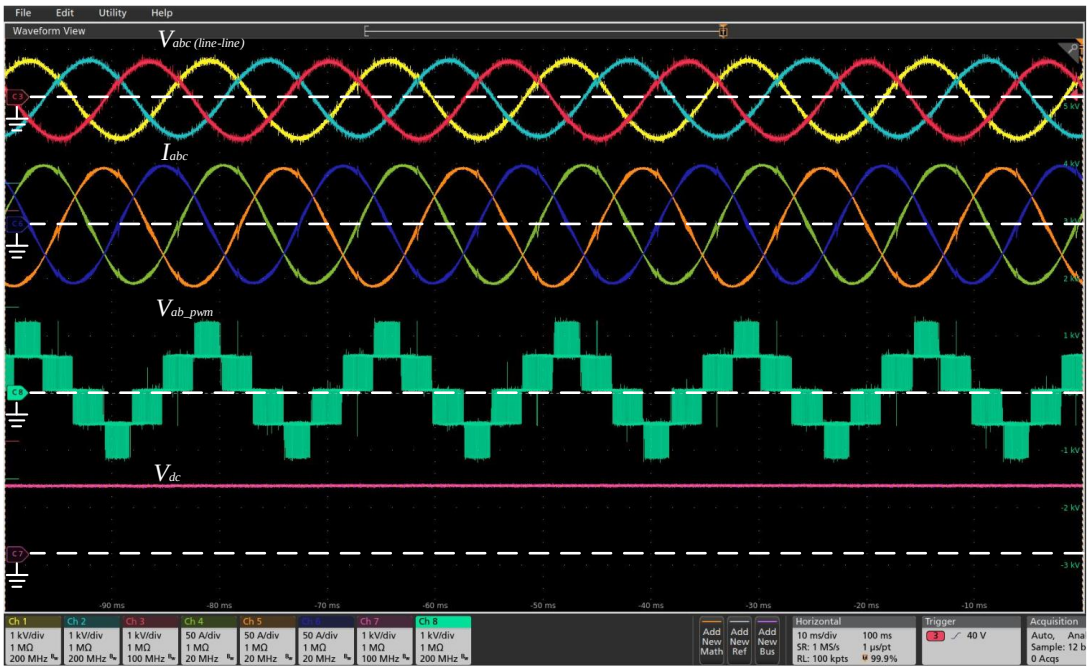


Figure 5-28 Output voltage and current waveforms of 3L-ANPC inverter utilizing Si/SiC HyS.

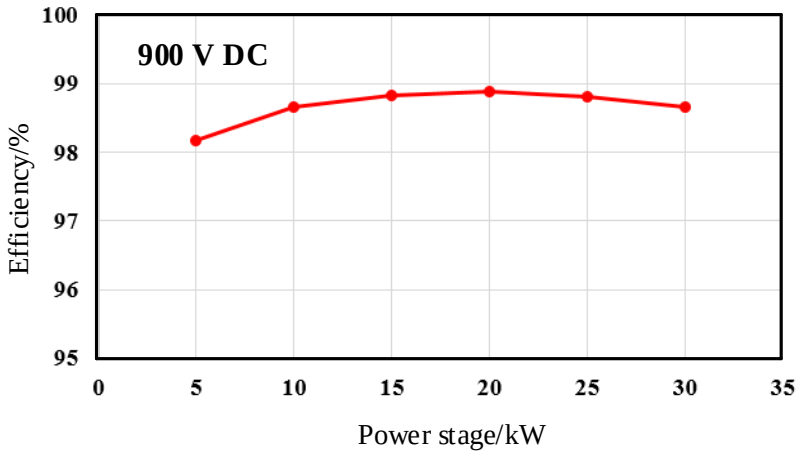


Figure 5-29 Si/SiC HyS-based 3L-ANPC inverter power stage efficiency.

The inverter efficiency test was carried out with RL load. The voltages and currents are measured by the high voltage differential probes Tektronix THDP0100 and current probes Tektronix TCP0150. Then, the efficiency was calculated using the voltage and current data restored in the 8-channel oscilloscope. At each power stage, three-phase load voltage, load

current, voltage, and current of DC side were measured and the inverter efficiency was calculated based on the voltage and current data. It is important to mention that in order to have accurate efficiency results, at least 15 times of line voltage period data were restored and utilized to calculate the inverter efficiency. The efficiency testing results of the implemented Si/SiC HyS-based 3L-ANPC inverter power stage are shown in Figure 5-29. It is shown that the proposed Si/SiC HyS-based 3L-ANPC inverter achieves a 98.9% peak efficiency

CHAPTER 6: CONCLUSIONS AND FUTURE WORKS

6.1 Conclusion

The “Si IGBT+SiC MOSFET” hybrid switch (Si/SiC HyS) is investigated in this work. The Si/SiC HyS combines the Si IGBT’s advantage in conducting high current and the SiC MOSFET’s advantage of low switching loss. The device cost for the Si/SiC HyS is also reduced compared to a full SiC MOSFET. The main works in this dissertation are summarized as follows.

1) The conduction and switching characteristics are investigated and the power loss model is proposed. For the Si/SiC HyS design process, the Si and SiC devices current rating optimization algorithm is proposed to achieve a cost-effective Si/SiC HyS selection and provide a tool to help evaluate the tradeoff between device cost, SiC MOSFET thermal stress, and system efficiency. To realize a more efficient operation of Si/SiC HyS, the delay time optimization method is proposed.
2) Two active thermal control algorithms, named “Conduction Time Variation-Based Active Thermal Control” (CTV-ATC) and “Switching Sequence Dispatch-Based Active Thermal Control” (SSD-ATC), are proposed to reduce the SiC MOSFET thermal stress and enhance the system reliability. The CTV-ATC and SSD-ATC algorithms realize the device junction temperature regulation by redistributing the conduction loss and switching loss, respectively. The effectiveness of the two proposed ATC algorithms is validated on a buck converter experimental platform.

3) The performance of Si/SiC HyS-based converter is improved by the proposed multi-objective operation control. In the light load condition, the converter operate with the conventional gate driving sequence, while at heavy load condition, the converter maximum output power is improved by using the active thermal control algorithms. The experimental results show that the maximum output power of Si/SiC HyS-based buck converter is improved by 5.9%. For the UPS application, a mission profile-based converter reliability enhancement evaluation is conducted to assess the yearly accumulated damage reduction on the device bond wire.
4) two types of Silicon (Si) IGBT and Silicon Carbide (SiC) hybrid switch (Si/SiC HyS) based three-level active-neutral-point-clamped (3L-ANPC) inverter are proposed for high efficiency and low device cost. The proposed Si/SiC HyS-based 3L-ANPC inverters are compared with the full Si IGBT, full SiC MOSFET, and Si with SiC devices-based hybrid 3L-ANPC solutions on the inverter efficiency, power capacity, and device cost. It is shown that compared with the full Si IGBT 3L-ANPC solution, the inverter efficiency improvement by Si/SiC HyS is 2.4% and 1.8% at light load condition and heavy load condition, respectively. Compared to the full SiC MOSFET solution and 2-SiC MOSFETs hybrid scheme, the device cost of 2-Si/SiC HyS-based 3L-ANPC is reduced by 78% and 50% with 0.28% and 0.21% maximum inverter efficiency sacrifices.

The following conclusions are made:

(1) The proposed delay time optimization method can reduce the total semiconductor loss of Si/SiC HyS. The converter efficiency can be improved by using the optimal delay time. In addition, with the increase of switching frequency, the efficiency improvement will become more significant.

(2) The proposed two ATC algorithms can effectively regulate the junction temperature of Si IGBT and SiC MOSFET. The maximum output power of the Si/SiC HyS-based buck converter prototype is increased by 5.9%. For the Si/SiC HyS-based UPS inverter application, by using the ATC algorithm, the yearly AD on the SiC MOSFET bond wire is reduced by 80%. The useful lifetime of Si/SiC HyS-based UPS inverter is extended.

(3) The proposed Si/SiC HyS-based 3L-ANPC inverter is a cost-effective way to realize high inverter efficiency. Between the two proposed Si/SiC HyS-based 3L-ANPC inverters, the 2-Si/SiC HyS-based 3L-ANPC inverter has lower device cost which makes it more suitable for cost-sensitive and high efficiency applications. While the 4-Si/SiC HyS-based 3L-ANPC inverter has higher output power capacity, making it a better candidate for high power density, high power capacity, and high efficiency applications.

6.2 Future Works

The following works will be performed to enhance the current contributions.

(1) A mathematical characterization for the Si/SiC HyS turn on and turn off transient is not investigated in this work. To have better understanding the impact of delay time on the Si/SiC HyS switching loss, the mathematical way

to characterize the Si/SiC HyS switching process ought to be investigated in the future.

(2) In this work, the Si/SiC HyS is formed by the discrete TO-247 devices. The output power is limited. To fully utilize the high current carrying capability advantage of Si IGBT within the Si/SiC HyS, the investigation on the high current-rated Si/SiC HyS power module will be investigated in the future.

6.3 Main Publications

[1] H. Liu, T. Zhao and X. Wu, "Performance Evaluation of Si/SiC Hybrid Switch-Based Three-Level Active Neutral-Point-Clamped Inverter," in *IEEE Open Journal of Industry Applications*. (early access)

[2] H. Liu, T. Zhao, J. Gafford, S. Essakiappan and M. Manjrekar, "Design of a 1500V Si IGBT/SiC MOSFET Hybrid Switch-Based Three-Level Active NPC Inverter," 2021 *IEEE Energy Conversion Congress and Exposition* (ECCE), 2021, pp. 168-173.

[3] H. Liu and T. Zhao, "Optimal Gate Driving Strategy for Si/SiC Hybrid Switch-Based 3L-ANPC Inverter with Improved Output Capacity," 2021 *IEEE Applied Power Electronics Conference and Exposition* (APEC), 2021, pp. 741-74.

[4] H. Liu and T. Zhao, "Performance Evaluation of Si/SiC Hybrid Switch-Based Three-Level Active NPC Converter," 2021 *IEEE Applied Power Electronics Conference and Exposition* (APEC), 2021, pp. 2058-2064.

[5] H. Liu, T. Zhao and X. Wu, "Efficiency Improvement Evaluation and Loss Modeling of a Hybrid Switch-Based T-NPC Inverter," 2019 *IEEE 7th Workshop on Wide Bandgap Power Devices and Applications* (WiPDA), 2019, pp. 6-11.

[6] H. Liu and T. Zhao "Conduction Time Variation-Based Active Thermal Control Method for Si and SiC Hybrid Switch," 2022 *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022. (accepted)

[7] H. Liu and T. Zhao " Si and SiC Hybrid Switch-Based Solid-State Circuit Breaker," 2022 *IEEE Energy Conversion Congress and Exposition* (ECCE), 2022. (accepted)

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