LITHOGRAPHY-FREE GROWTH OF SILICON MICROWIRES VIA ATMOSPHERIC PRESSURE CHEMICAL VAPOR DEPOSITION FOR OPTOELECTRONIC APPLICATIONS

by

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ABSTRACT

ESHA THAKUR. Lithography-Free Growth of Silicon Microwires via Atmospheric Pressure Chemical Vapor Deposition for Optoelectronic Applications.
(Under the direction of DR. MICHAEL G. WALTER)

Realizing the next-generation electronic devices with added features, i.e., flexibility, smaller dimension, higher density (transistors per unit area), lightweight, and low-power consumption, would require extensive work to optimize the processing conditions that would yield high-quality Si wires (microwire/nanowire) with optimum device performance at an affordable price. The standard photolithography process used to pattern the catalyst seed layer for the vapor-liquid-solid (VLS) growth of Si wires provides highly ordered, epitaxial Si wires. However, this process is not scalable owing to the high cost involved; hence there is a need to explore alternate routes to grow Si wires using cost-effective strategies.

To this end, we employed a cost-effective lithography-free de-wetting technique to fabricate the seed layer for the growth of highly ordered Si microwires (Si MWs). There are several reports on VLS growth of Si wires that study the growth kinetics and effect of growth parameters like gas flow rate and growth temperature on Si wire growth rate. However, a quantitative and qualitative analysis of the impact of various growth parameters on Si wire size and quality is still lacking. Herein, we report the quantitative analysis of the effect of different growth parameters on Si MW growth rate and size (length and diameter) using the lithography-free growth technique and the influence of growth parameters on Si MW quality and device performance.

An exponential dependence of MW growth rate is observed, similar to that in thin-film growth rate, and is reported for the first time for a wire configuration. This has important implications in device fabrication as the optoelectronic properties in one-dimensional (1D) structures are strongly affected by size and growth conditions.

The electrical transport properties of as-grown Si MW have been extracted via two-probe and three-probe measurements. The FET characterization of as-grown intrinsic Si MW demonstrated p-type behavior. The temperature-dependent I-V measurement on as-grown and passivated Si MW has been done to determine the impact of trap states on the Si MW properties.

Lastly, we demonstrate the fabrication of Si MW Near-infrared (NIR) photodetector via a solution-processable route with optimum photoresponse at a low applied bias of 0.1 V and incident power density of 1.24×10^{-4} W/cm^2 with a responsivity of 3.05 A/W, T_{on}/T_{off} of 0.308 s / 0.363 s, external quantum efficiency (EQE) of 421%.

This study will enable a clear understanding of the impact of the various growth parameters on Si MW quality and allow us to utilize that knowledge to fabricate Si MW device with improved performance. Overall, the motivation for this dissertation is to develop a comprehensive understanding of the Si MW growth environment on its transport properties for optoelectronic device applications.

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DEDICATION

To my family

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

1D	One-dimensional
APCVD	Atmospheric pressure chemical vapor deposition
CMOS	Complementary-metal-oxide-semiconductor
EQE	External quantum efficiency
FET	Field effect transistor
IC	Integrated circuit
MACE	Metal-catalyzed chemical etching
MOSFET	Metal oxide semiconductor field effect transistor
MSM	Metal-semiconductor-metal
MG law	Mott-Gurney law
NP	Nanoparticle
NIR	Near-infrared
PEDOT: PSS	Poly(3,4-ethylenedioxythiophene)-poly(styrene sulfonate)
SEM	Scanning electron microscopy
Si MW	Silicon microwire
Si NW	Silicon nanowire

Si wire	Silicon nanowire or microwire
SCLC	Space charge limited current
VLS	Vapor-liquid-solid

CHAPTER 1: INTRODUCTION

1.1 Historical background

Inorganic semiconductor materials are intriguing as their electrical conductivity can be easily modulated by doping it with different dopants. This exciting feature of semiconductors finds application in integrated circuits (IC's), also known as microchips, used in computers, mobiles, and other electronic devices.[1, 2] A single chip of 1 cm^2 consists of millions of tiny transistors and other electronic components. The first transistor was fabricated and tested using germanium (Ge) at Bell Telephone Laboratories and soon replaced with Si.[2] As compared to other semiconductor materials, Si forms an excellent thermal oxide (SiO_2) on its surface that finds application as field oxide in metal-oxide-semiconductor field-effect transistors (MOSFET's).[2, 3] Additionally, Si is much cheaper and is the second most abundant material in the earth's crust.[4] Although Ge has higher intrinsic mobility than Si,[3] the above-listed advantageous features of Si make it a dominant material in the semiconductor industry.

Over several decades, the miniaturization of transistors led to increased integration density, improved device performance, and cost reduction.[5] The reduction in the size of the transistor below a certain limit leads to the degradation of device performance due to increased leakage current, and the use of expensive fabrication steps required to achieve those dimensions adds up to its manufacturing cost.[6] One-dimensional structures such as Si wires as building blocks for emerging electronic devices can help overcome these technological challenges, provided a cost-effective solution can be developed for large scale implementation.[7]

1.2 Si one-dimensional structures

Si one-dimensional (1D) structures exhibit unique optoelectronic properties due to the confinement of their dimension in two directions. Si wires have a high aspect ratio, high mobility, enhanced light absorption, stability, and flexibility.[4, 8, 9] The small dimensionality and its compatibility with complementary-metal-oxide-semiconductor (CMOS) processing are the added features that make Si wires attractive for the emerging electronic device applications, i.e., solar cells,[10-12] field effect transistors (FETs),[13-15] batteries,[16, 17] and photodetectors,[4, 18, 19] with prospects of integration of nanophotonic devices on chip[20] as well as for the next-generation flexible/wearable electronics.[12, 15, 21, 22]

1.2.1 Solar cells

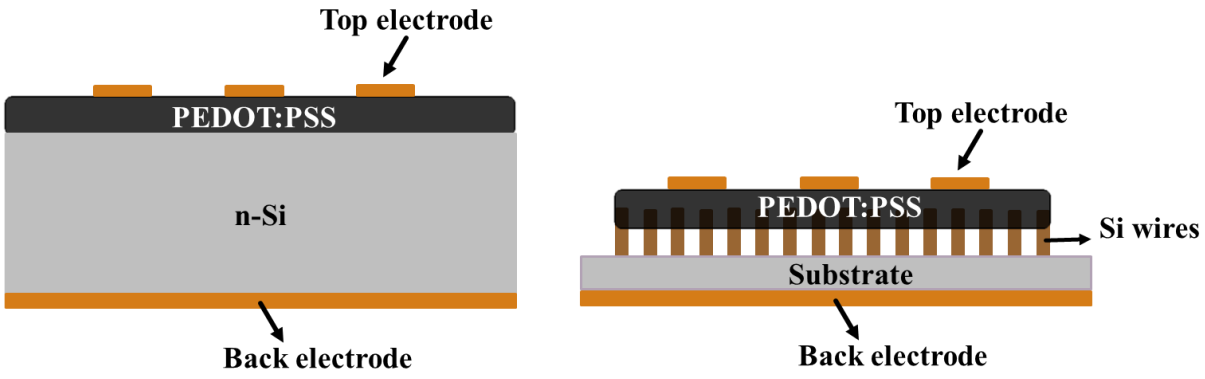


Figure 1.1 Bulk Si vs. Si wire hybrid solar cell configuration

Most of the current photovoltaic technology (90%) is based on Si, and efforts have been made to reduce its cost for large-scale applications resulting in extensive research to explore the cost-effective configurations like textured or pyramidal structures, Si wire (microwire and nanowire) arrays, and hierarchical structures.[23, 24] In a photovoltaic device, the wire configuration allows orthogonalization of light absorption and charge carrier separation, such that the charge

carriers can be separated effectively across the wires, while the light is absorbed along the wire length. This allows for a higher tolerance for impurity in Si wires such that we can use a material with lower minority carrier diffusion lengths in a radial wire configuration.[10, 25-27]

Recently, hybrid (inorganic-organic) Si wire-Poly (3,4-ethylenedioxy thiophene): polystyrene sulfonate (PEDOT: PSS) materials have also gained interest due to their flexibility, easy processing steps, and cost-effectiveness. Their low cost is due to their solution processibility compared to conventional p-n Si solar cells, which require expensive and complex processing steps and higher temperature for doping and junction formation.[28-30] PEDOT: PSS is a conducting polymer, where PSS acts as a p-type dopant and provides the stability to the structure, whereas PEDOT helps in the charge transfer. The conductivity of PEDOT: PSS can be enhanced by chemical treating it with materials like ethylene glycol (EG), dimethyl sulfoxide (DMSO), etc. In a hybrid Si-PEDOT: PSS configuration, the conductive polymer is used as a hole selective contact, which results in a junction formation with n-Si. The charge carriers move towards their respective electrodes, with electrons moving towards the cathode and holes moving towards the p-type PEDOT: PSS, and in this way, the photogenerated charge carriers are separated.[31 32]

The device physics modeling shows that a SMW-based radial solar cell with a minority carrier diffusion length of 1 μm is equally efficient compared to its planar counterpart.[26] However, the higher density of defect states and surface roughness in a wire configuration increases the recombination rate and hence degrades the device performance.[4, 24] Surface/interface engineering is thus essential for reducing charge carrier recombination. Passivation with a methyl group or oxide layer reduces surface recombination and enhances device performance.[33, 34] Wide bandgap semiconductors like MoO_x,[35-38] VO_x,[35], WO_x,[35] have been used as passivating layer and hole

selective contact, and TiO_2,[35, 38-40] Cs_2O_3,[40] ZnO[38] have been used as electron selective layer in planar and textured Si-PEDOT: PSS solar cells.

1.2.2 Biosensors

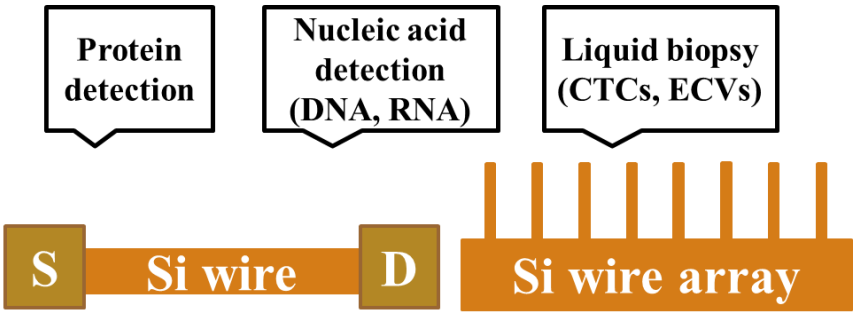


Figure 1.2 Schematic showing different bio-components that can be detected using functionalized single wire FET or Si wire arrays.

Si nanowires (Si NWs) have been reported to detect protein and nucleic acids and have demonstrated the ability to detect genetic cancer biomarkers with a limit of detection in femtomoles. The large surface area to volume ratio of NWs makes them suitable for sensing applications as a small charge on its surface can significantly affect the charge transport. The first Si NW-FET-based biosensor was reported in 2001, where the bio-receptors were attached to the Si NW surface via functionalization for stable binding of the analyte.[41] First, a linker molecule with a functional group (amine, thiol, aldehyde) was attached to the native oxide surface, then the bioreceptor was conjugated to this linker molecule. The Si NW FET sensitivity was observed to be inversely related to the Si NW diameter and directly related to the doping density. In addition to the intrinsic property of the Si NWs, the bioreceptor size and density at the surface also alter the sensitivity of the Si NW FETs.[41]

Any change at the surface of the Si NW, e.g., target analyte binding at the surface, results in a change in the physio-chemical properties (surface charge), which can then be measured to determine the amount of the target analyte without using conventional enzymatic or fluorescent labeling techniques. Depending upon the charge on the target analyte and type of dopant in Si NWs, the conductance of the Si NWs increases or decreases. If the analyte is positive, the conductance of p-type Si NWs decreases, and for the n-type Si NWs, the conductance increases.[41, 42] The Si NW-based biosensors are label-free, highly sensitive, highly specific, and have a fast response time. However, the Si NW-based biosensor's sensitivity at a high salt concentration such as whole blood and serum is substantially reduced or non-existent due to the Debye screening effect. Currently, efforts are underway to overcome the Debye screening effort to incorporate Si NW FET biosensors in clinical practice.[43]

1.2.3 Photodetectors

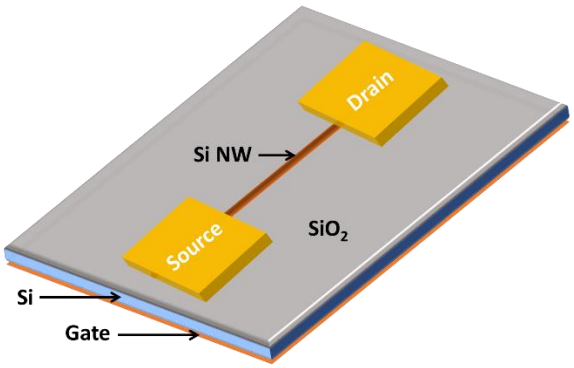


Figure 1.3 Schematic showing metal-oxide-field-effect transistor (MOSFET) based Si NW phototransistor.

Photodetectors have been widely used in various settings like defense, industry, telecommunication, biomedical applications, and find applications in night surveillance, image sensing, environment monitoring, food quality control, optical communication, and non-invasive

blood glucose measurement.[44-48] There are several types of photodetectors like photodiodes, phototransistors, and photoconductors. Photodetectors convert the optical signal into an electrical signal. The incident light generates charge carriers which are collected at the external circuit by applying an electric field between the metal contacts.[49, 50]

Typically, GaN, Si, and InGaAs-based photodetectors have been used for ultraviolet (UV), visible (VIS), and near-infrared (NIR) photodetection for wavelengths ranging from 250-400 nm, 450-800 nm, and 900-1700 nm, respectively.[45] Recently, Si-based photodetectors have been used to detect a wide range of wavelengths from UV-VIS (ultraviolet-visible) to short NIR (near-infrared) regime.[45, 51-54] n-ZnO/p-Si heterojunction photodetectors employing Si wire[55] or planar Si configuration[51, 52] have been mainly used for UV-VIS detection. Han-Don Um et al. reported enhanced UV and visible responsivity in ZnO-Si NW heterojunction photodiode. The visible light is transmitted through ZnO, which is mainly absorbed in the depletion region of the p-type Si NW. The photogenerated electron-hole pair generates the current under reverse bias, and the photocurrent saturates as the depletion width increases beyond the penetration depth of the incident visible light. Alternatively, due to shorter penetration depth, most of the UV light is absorbed by ZnO, and the heterojunction photodiode exhibits UV photoresponse under forward bias.[52, 55] Apart from the heterojunction configuration, junctionless Si NW phototransistors (MOSFETs) have also been reported to exhibit high responsivity, and detectivity in the short-wavelength NIR region.[53, 54] Si-based photodetector with ultra-fast detection, high responsivity, sensitivity, and detectivity is desirable for its integration with VLSI technology for a large scale application in image sensing, food monitoring, and other bio-medical applications.

1.3 Si wire fabrication

The two most popular techniques that are currently being explored for the low-cost production of high-quality Si wires are top-down metal-catalyzed chemical etching (MACE) of Si and bottom-up Vapor-Liquid-Solid (VLS) growth of Si wires via chemical vapor deposition (CVD) technique.[56] MACE is a simple wet chemical etching process that can be easily done under ambient conditions and does not require high-end vacuum setups. In comparison, the VLS-assisted CVD is a much more versatile technique that is applicable to a wide range of semiconductors with the feasibility of in-situ doping with p-type or n-type materials and heterostructure growth. The VLS-grown wires can also be easily scraped, ultrasonicated, or embedded in a polymer for possible application in flexible electronics.[4]

1.3.1 Top-down metal-assisted chemical etching (MACE) technique

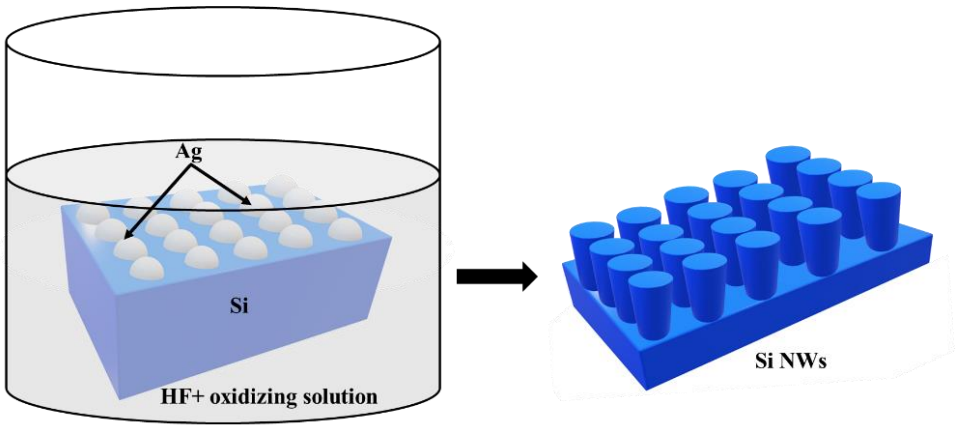


Figure 1.4 Schematic showing MACE technique for fabrication of Si NWs via chemical etching.

In the MACE technique, etching the Si substrate in the presence of a metal in an aqueous HF solution result in the formation of porous Si or Si NWs.[30, 57] Si NW fabrication by electroless etching of Si substrate using aqueous HF/$AgNO_3$ solution was reported by Peng et al.[8] in 2002.

The Ag nanoparticles act as a catalyst that aids in metal-induced local oxidation. Depending upon the crystal orientation of the Si substrate, the oxidized Si is anisotropically etched in HF solution.[8]

There have been reports of the presence of Ag catalyst at the bottom, while other reports indicate the catalyst to be located on top after the chemical etching of Si substrate. Thus, the role of Ag as a catalyst or a protective layer has been controversial. Abouda-Lachiheb et al.[58] proposed a model based on charge transfer at the Si-Ag interface to explain this dual behavior of the Ag. They stated that there are two different ways to achieve Si NWs via electroless etching: either using a one-step process wherein the Ag deposition and Si etching are done simultaneously, or via a two-step process wherein the Si etching is done after Ag nanoparticles are deposited. Depending upon the process used, i.e., one-step or two-step process, Ag either acts as a protective layer or as a catalytic site, respectively.[58]

1.3.2 Bottom-up Vapor-Liquid-Solid (VLS) mechanism

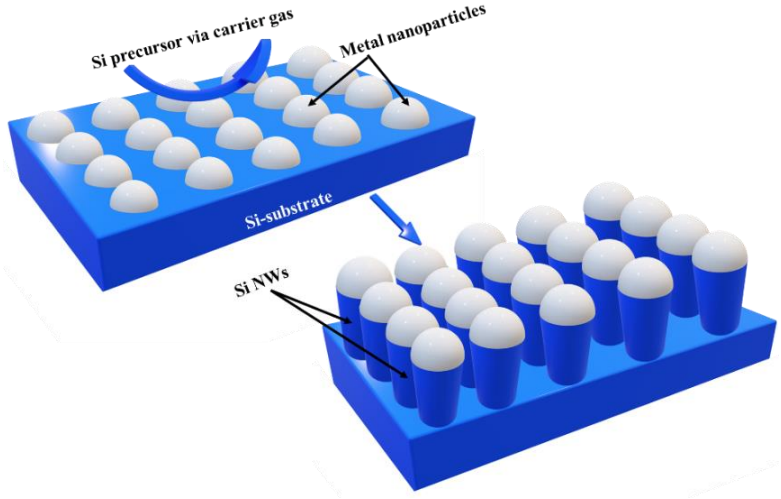


Figure 1.5 Schematic showing growth of Si NWs via VLS mechanism

Vapor-liquid-solid (VLS) mechanism was first introduced by Wagner et al. for the growth of Si whiskers using the Au catalyst and $SiCl_4$ precursor.[59] VLS-assisted chemical vapor deposition (CVD) is a widely used bottom-up technique for the growth of high-quality, single-crystalline Si NWs. Si NW size is strongly dependent on the catalyst seed layer that acts as the sink wherein Si precursor is reduced to Si and adsorbed. On supersaturation of the seed layer (metal-Si alloy) with incident Si, the precipitation occurs at the liquid-solid interface, and in this way, the Si NW growth proceeds.[60, 61] The growth temperature of Si wires should be sufficient to form metal-semiconductor alloy at the eutectic point and lower than the temperature where the nanoparticle desorbs from the substrate.[62] Au-Si forms a single, whereas Cu-Si forms multiple eutectic points in the phase diagram resulting in the different growth temperature and phase of Si wire. The growth of Si wire is a three steps process (a) incorporation of precursor, (b) diffusion of the precursor (c) crystallization of the Si at a solid-liquid interface. The growth rate of Si wire depends on the slowest step among the three listed above. Si vapors will get incorporated into the liquid droplet resulting in the formation of alloy (AuSi and Cu_5Si). An increase in the concentration of Si in the Cu-Si alloy changes its phase from (Cu_5Si to Cu_3Si), and subsequently, it supersaturates to form a solid surface below the liquid droplet.[63] In addition, the silicon crystal growth orientation can be directed by the crystal face of the underlying substrate.

Although there have been several reports on Si wire growth and various optoelectronic applications, several other aspects need to be explored before Si wires can be incorporated into the industry for any commercial applications. This includes, and is not limited to, extensive quantitative as well as qualitative analysis of the as-grown wires for control over Si wire size and quality, understanding the effect of growth conditions on Si wire quality and ways to reduce the

defects and traps, improving metal-semiconductor contacts for better charge transfer, and finding a solution-processable or other alternative methods to make the Si wire fabrication a scalable process without significantly degrading its performance.

1.4 Thesis outline

This work focuses on the growth of Si microwires (MWs) via a cost-effective lithography-free VLS mechanism in atmospheric pressure chemical vapor deposition (APCVD) system. A catalyst thin film is evaporated and annealed in-situ for the nanoparticle formation (de-wetting/agglomeration technique), followed by the epitaxial growth of Si MWs. This study aims to understand the effect of growth conditions on the size as well as the quality of the VLS grown Si MWs and its optoelectronic properties.

Chapter 2 focuses on the growth of Si MWs and includes a quantitative analysis of the impact of various growth parameters on Si MW dimensions. Growth parameters like Cu thin film thickness, gas flow rates, the position of the sample, and growth time were varied to study their effect on Si MW diameter and growth rate, and the rate-limiting step was determined.

Chapter 3 includes the electrical transport characterization using two-probe and three-probe measurements at room temperature. The charge carrier mobility of the as-grown Si MW has been extracted using two-probe measurement via the space charge limited current (SCLC) mechanism. Three-terminal measurement of Si MW was done by fabricating a back-gated Si MW Field Effect Transistor (Si MW-FET), and its output and transfer characteristics have been reported.

The effect of the surface passivation of Si MW on the trap state has been reported in Chapter 4. Low-temperature I-V measurement was done to determine the trap state density and the trap energy levels of the H-terminated and CH_3-terminated Si MWs.

Chapter 5 is dedicated to the optoelectronic device application of the CH_3-terminated Si MWs. A solution-processable, low-powered NIR-based Si MW photodetector has been fabricated using CH_3-terminated samples. Its figure of merit has been extracted at various applied voltages and incident power.

Lastly, Chapter 6 includes the summary and outlook.

CHAPTER 2: LITHOGRAPHY-FREE GROWTH OF SI MWS VIA VAPOR-LIQUID-SOLID (VLS) MECHANISM

2.1 Introduction

Vertically oriented wire growth, with control over its dimension (i.e., diameter, length) and periodicity is highly desirable for enhanced optoelectronic device performance. The wire dimensions and pitch (spacing between the wires) influence the photocurrent density and the efficiency of the device and needs optimization to achieve the best device performance.[12, 64-67] Si wire (nano and MWs) size and pitch can be modulated by tuning the size and distribution of the catalyst seed layer. In the case of the photolithography-assisted process of catalyst seed layer formation, the size and periodicity of catalyst nanoparticles (NPs) depend on the pattern of the mask.[68] Though it provides highly-ordered nanostructures with controlled size and distribution, it is not viable for large-scale production due to the high manufacturing cost. Herein, we utilize a lithography-free de-wetting or agglomeration technique for the NP formation and demonstrate a cost-effective method to fabricate highly ordered Si MWs and tune their size and growth rate via optimizing various growth parameters.

There are numerous reports on the Si wire growth using the de-wetting technique to form the NPs on the substrate wherein Si wire sizes of the order of nanometers and micrometers have been grown using silane[69-71] and silicon tetrachloride[72-75] precursors, respectively. The effect of various growth parameters, i.e., growth temperature[72, 73], precursor gas flow rates as well as their partial pressure[72-74], and wire diameter[71, 75, 76] on Si wire growth rate and orientation with Au as a

dominant catalyst[71, 72, 74, 75] is well reported in the literature. Some reports contradict the dependence of growth rate on partial pressure[9, 72, 73] and wire diameter[73, 75, 77]. Eichfeld et al.[73] reported a critical partial pressure ($P_{critical}$) below or above which the growth rate increases or decreases, respectively. Schmidt et al.[76] reported that growth rate varies with diameter depending upon the incorporation and crystallization velocities w.r.t the supersaturation. Dhalluin et al.[71] proposed a semi-empirical model using Schmidt et al.'s approach and incorporating delay in growth time to explain the decrease in growth rate for larger diameters. Although there have been several reports on the growth kinetics of Si wires, the quantitative analysis of the effect of various growth parameters on Si wire dimensions (diameter and length/growth rate) is lacking. This study is important as the optoelectronic properties are strongly dependent on the size as well as the quality of the as-grown wires. Understanding the impact of various growth parameters on Si wire size and quality can help us control the Si wire growth allowing to achieve optimum device performance.

Herein, we optimize the growth parameters for the growth of vertically oriented Si MWs by varying growth temperature, gas flow rate, and Cu film thickness. The effect of various growth parameters on Si MW morphology, areal density, diameter, and length have been explored. An exponential decrease in the growth rate of the Si MWs with a distance similar to that in the case of thin-film deposition via the CVD process has been reported here. Additionally, uncatalyzed deposition on Si MW sidewalls has been suggested to cause the increase in Si MW diameter with growth time.

2.2 Experimental method

2.2.1 Thin film deposition

The n^+ Si (111) substrate (ρ=0.001-0.005 Ω-cm) was used for the growth of the Si MWs. The substrate was cut into 1x0.5 cm^2 pieces and pre-cleaned before the deposition of the catalyst thin film. The substrate was pre-cleaned by ultrasonicating it in acetone and isopropyl alcohol for 10 min, followed by a 30-min piranha etch (H_2SO_4:H_2O_2::3:1) to remove any organic contamination. The oxide layer was removed by dipping the piranha etched Si substrate in buffered HF. After each processing step, the substrate was rinsed with DI water and blow-dried with N_2. The freshly cleaned Si substrate was then loaded in the thermal evaporator (MB EVAP) to deposit the thin film of Cu (20-40 nm). The system was pumped down to $6x10^{-6}$ mbar, and the thickness of Cu thin film was controlled using an SQC-310 deposition controller with a deposition rate of ~0.3 Å/s.

2.2.2 Si MW growth in atmospheric pressure chemical vapor deposition (APCVD) system

The Si MWs were grown via the VLS mechanism in a home-built APCVD system shown in Fig. 2.1. The samples were loaded in the quartz tube of 1-inch outer diameter, at D_4, D_5, and D_6, corresponding to the substrate position being 4, 5, and 6 inches away from the heater end. The reaction chamber was pumped down to a base pressure of about 8 mTorr using a rough pump. After pumping down the system, the reaction chamber was filled with Ar and H_2 until the pressure reached 760 Torr. The reaction chamber was then heated to the required temperature for in-situ annealing of Cu thin film leading to de-wetting/agglomeration. De-wetting/agglomeration is a thermally activated process wherein the thin film cracks up at elevated temperatures and forms island-like structures or seed layers. At eutectic temperature T_e (about 800 °C), Cu alloys with Si

and forms Cu-Si seed layer. A separate line of Ar gas is used to carry $SiCl_4$ precursor to grow Si MWs at the growth temperature of 1000 °C.

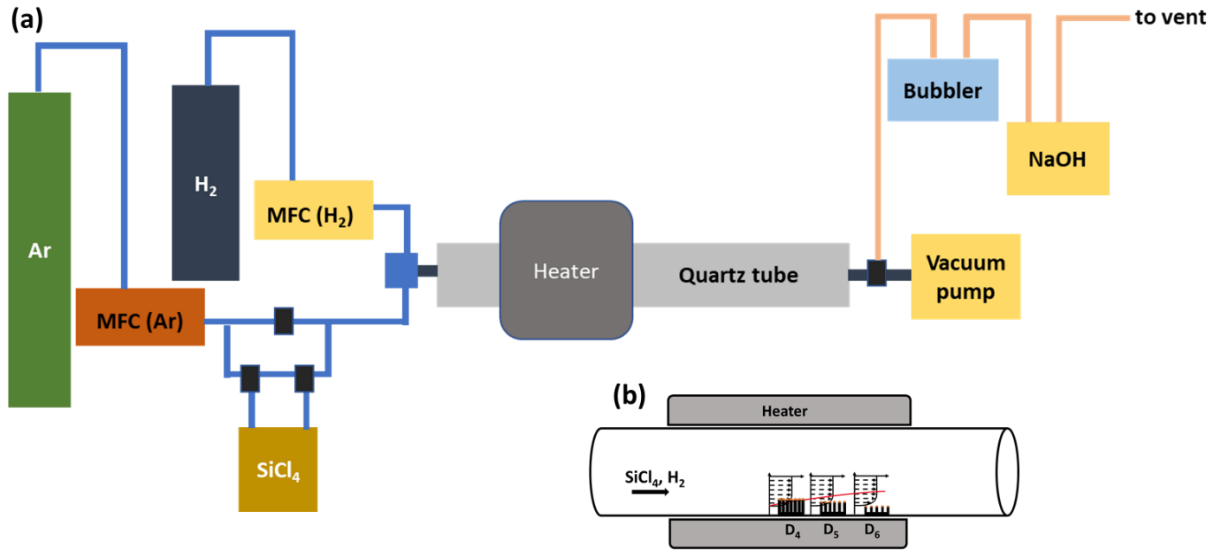


Figure 2.1 (a) Block diagram of APCVD setup and (b) Schematic showing the position D_4, D_5, and D_6, corresponding to the position of substrate 4, 5, and 6 inches away from the heater end in a quartz tube, respectively.

2.3 Results and discussion

2.3.1 Effect of growth parameters on Si MW morphology and areal density (Ar: H_2::3:200 sccm)

The as-deposited 20 nm Cu film was annealed in situ using 3:200 sccm Ar: H_2 flow rate. The growth conditions were optimized by varying growth temperature, growth time, and position of sample w.r.t. heater to obtain kink-free vertically oriented Si MWs.

2.3.1.1 Effect of growth temperature on Si MW morphology

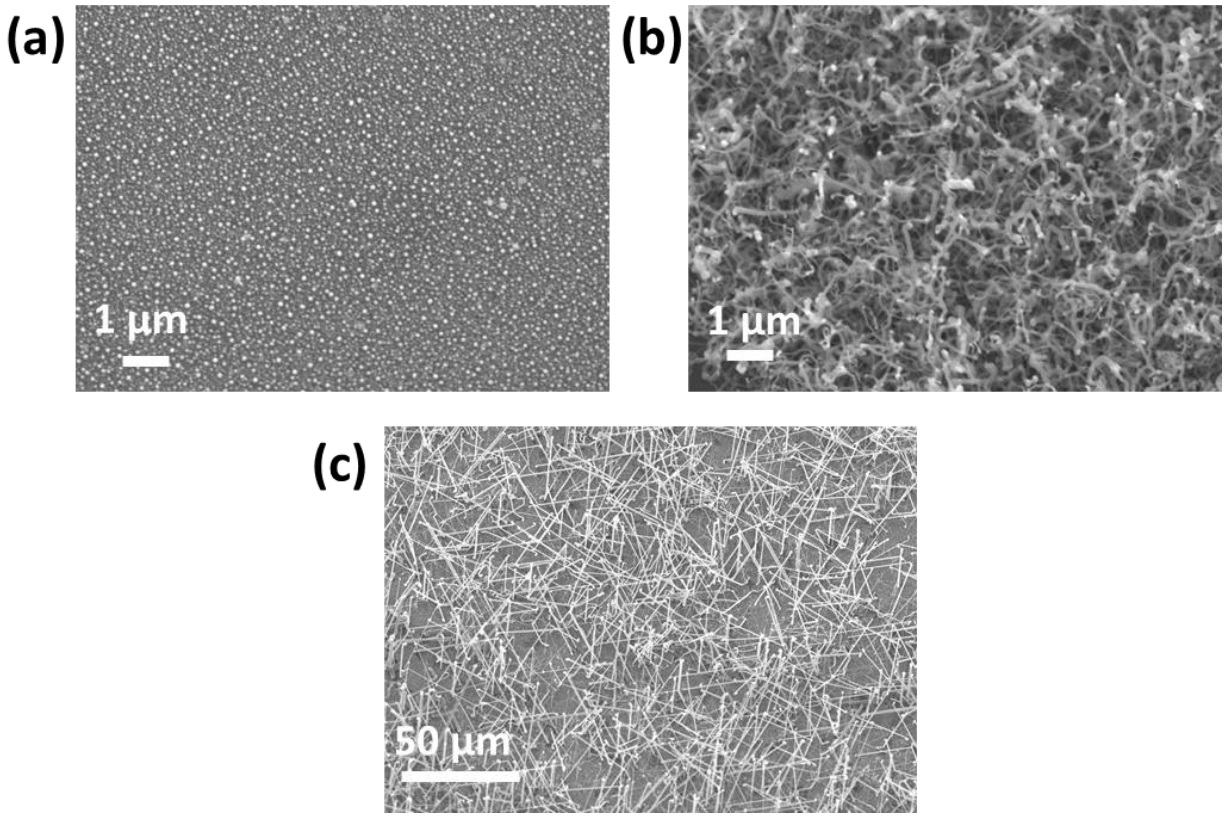


Figure 2.2 Growth of Si MWs at a) 700 °C, (b) 850 °C, (c) 1000 °C, respectively using 3:200 sccm Ar:H_2.

The as-deposited Cu film on n^+-Si (111) substrate was annealed in-situ for 5 min at three different growth temperatures, followed by growth for 1.5 min at 700 °C, 850 °C, and 1000 °C, respectively. It was observed that the growth temperature had a significant effect on Si MW growth and morphology. No growth was observed at 700 °C, as seen in Fig. 2.2 (a); a worm-like growth of Si MWs was observed at 850 °C, as seen in Fig. 2.2 (b), and cylindrical wires with random orientation were observed at 1000 °C as seen in Fig. 2.2 (c). No growth of Si wire was observed at 700 °C since $SiCl_4$ reacts with H_2 between 800-1000 °C to form Si and HCl vapors.[78, 79]. At a lower growth temperature (i.e., 850 °C), diffusion of Si through the liquid alloy is slow and

inhomogeneous, resulting in different deposition rates of Si along the interface, and hence the worm-like structure is formed.[63] Since the MWs grown at 850 °C are curly, and growth is dense as compared to the one grown at 1000 °C, the former will absorb more light; however, there will be more surface recombination of charge carriers. Thus, increasing growth temperature from 850 °C to 1000°C changes the Si MW morphology from worm-like to cylindrical wires.

2.3.1.2 Effect of growth time on Si MW morphology

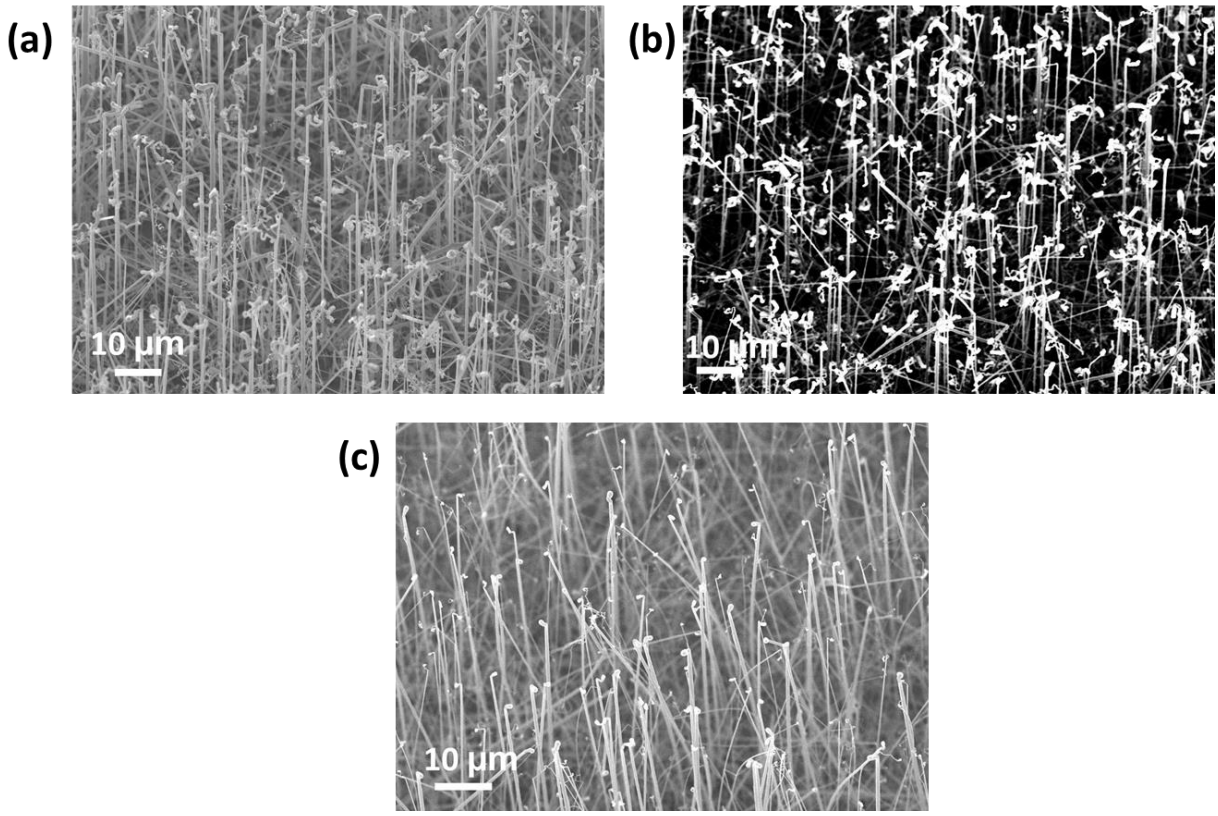


Figure 2.3 Growth of Si MWs at 1000 °C, 3:200 sccm Ar: H_2 flow rate, for (a) 5 min, (b) 3 min, (c), and 2 min, respectively, at D_4.

The as-deposited 20 nm Cu thin film was annealed in-situ at the growth temperature of 1000 °C for 10 min, and Si MWs were grown for 2 min, 3 min, and 5 min, respectively, using 3:200 sccm Ar: H_2 gas flow rate. Most of the Si MWs were observed to grow in the vertical

direction, with kinking at the MW tip, as seen in Fig. 2.3 (c). The kinking is often related to the instability of the liquid alloy droplet due to the abrupt change in the temperature at the liquid-solid interface.[80] When the Si MWs were grown for a longer time, i.e., 3-5 min, as compared to 2 min, no catalyst was observed at the MW tip, and the growth at the tip was haphazard as compared to the bulk of the Si MW below the tip as seen in Fig. 2.3 (b) and (c). The random growth at the tip of the Si MW can be associated with the consumption of Cu catalyst during the growth process, and this disturbance at the growth interface could result in such growth. Decreasing the growth time to 2 min significantly reduces the worm-like tip; however, slight kinking at the MW tip was still observed.

2.3.1.3 Effect of annealing conditions on Si MW areal density

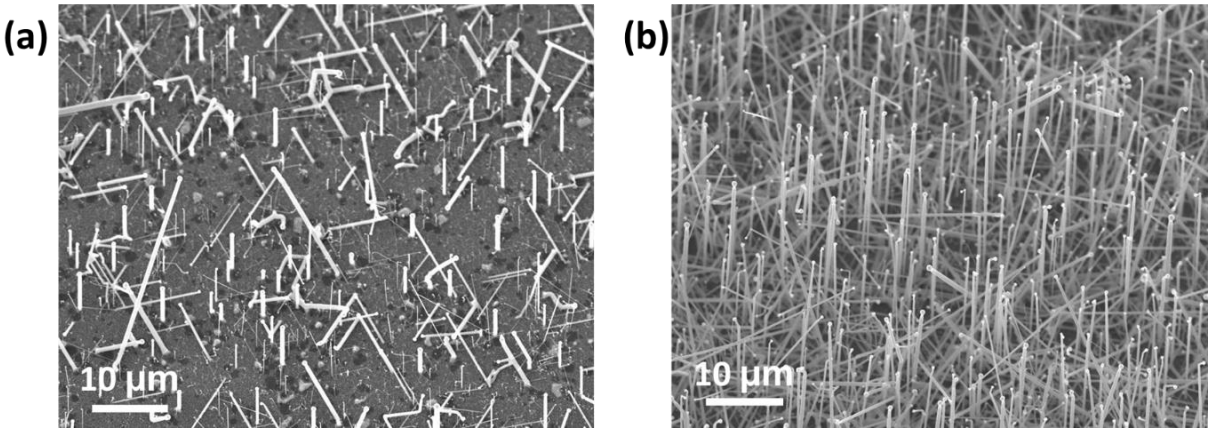


Figure 2.4 Growth of Si MWs at 1000 °C, at D_6 w.r.t heater for 1.5 min by annealing pre-growth at 700 °C, 40 min in (a) 3:200 Ar: H_2 ambiance (b) vacuum.

Si MWs were grown for 1.5 min after annealing 20 nm Cu thin film in 3:200 sccm Ar: H_2 and in vacuum at 700 °C, 40 min, respectively. Samples annealed in vacuum gave a higher yield of Si MWs as compared to the one annealed in Ar: H_2 (3:200 sccm) ambiance, as seen in Fig. 2.4. When Cu thin film is annealed in a vacuum as compared to the annealing in Ar: H_2 ambiance, the

residual oxygen in the chamber may oxidize Cu, affecting the NP size and distribution, thus, affecting Si MW yield.

2.3.1.4 Effect of position w.r.t heater on Si MW diameter (Ar:H_2::3:200 sccm)

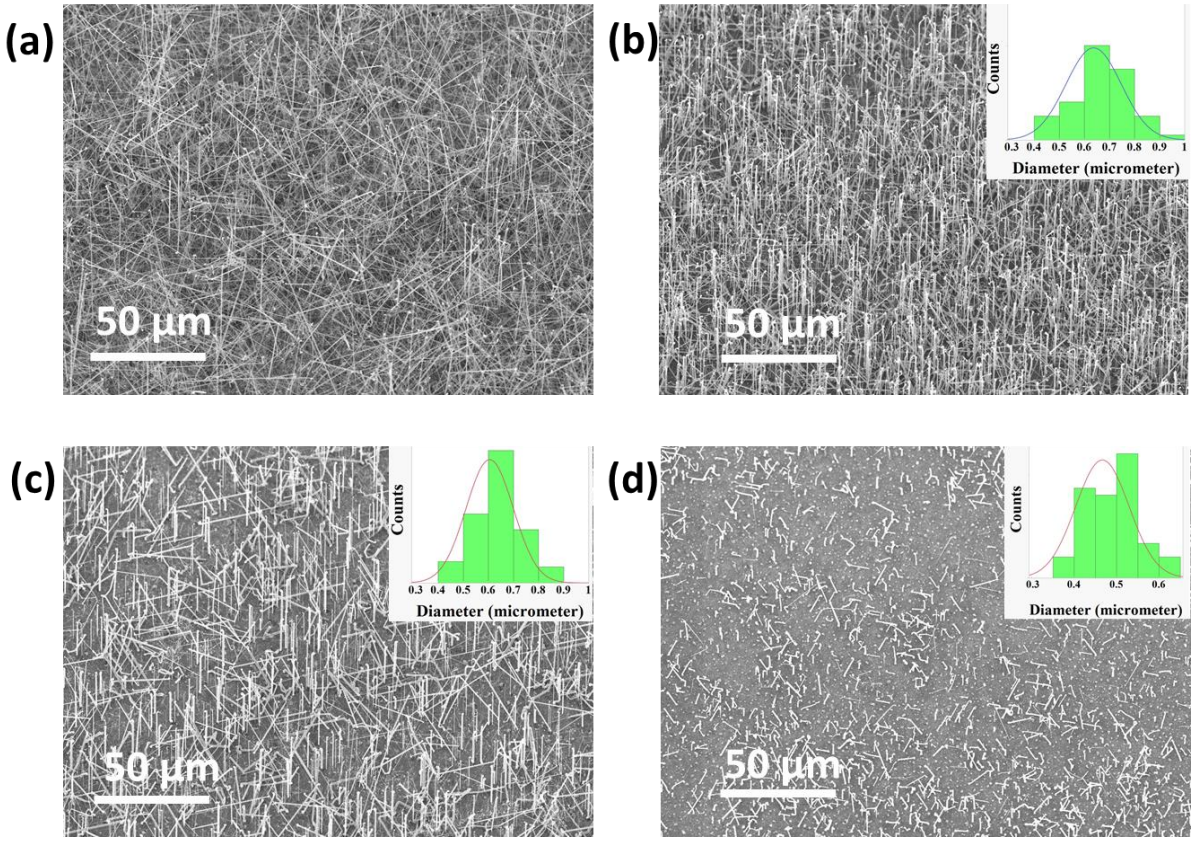


Figure 2.5 Growth of Si MWs at 1000 °C, 3:200 Ar:H_2 flow rate for 1.5 min at (a) D_3, (b) D_4, (c) D_5, (d) and D_6.

Cu (20 nm) thin film was annealed at 700 °C for 40 min, followed by growth at 1000 °C for 1.5 min using 3:200 sccm (Ar: H_2) gas flow rate. The samples were placed at four different positions inside the CVD reactor. The distance of the substrate D_s (s=3, 4, 5, and 6) in the reactor tube was measured from one end of the heater and corresponded to 3, 4, 5, and 6 inches, respectively. The surface morphology of the Si MWs was studied using JEOL JSM 6480 SEM images, and the average diameter of the Si MWs was obtained using the measurement of about

100 wires using ImageJ software. The VLS-grown Si MWs had a smooth surface and uniform diameter along the wire length. The Si MW areal density and diameter were observed to decrease as we move downstream, as seen in Fig. 2.5. The average Si MW diameter decreased from 640±55 nm at D_4, 600±40 nm at D_5, and 460±31 nm at D_6, respectively, as we moved downstream. The decrease in average diameter has been initially observed by Kumar et al.[81] for Ga_2O_3 nanowires grown at low pressure due to the concentration gradient as we move away from the source vapor. We believe that the decrease in diameter as we move downstream could be due to the combination of the concentration and temperature gradient.

2.3.1.5 Tapering: Effect of gas flow rate on morphology

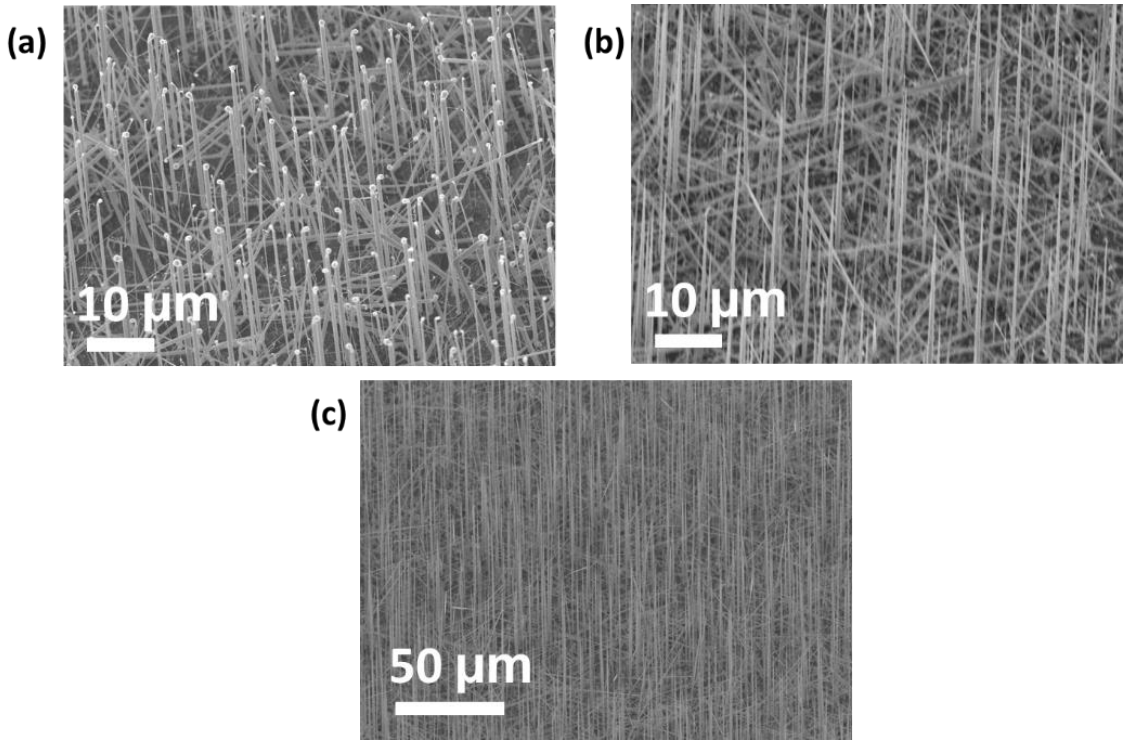


Figure 2.6 Growth of Si MWs using at (a) 10:200 Ar: H_2 flow rate for 1.5 min at (b) 10:100 Ar: H_2 flow rate for 1.5 min, (d) and 10:200 Ar: H_2 flow rate for 5 min.

Tapered Si MW growth was observed when the gas flow rate was reduced from 10:200 sccm to 10:100 sccm ($SiCl_4$:H_2), using 20 nm Cu with a growth time of 1.5 min. The tapering was also observed at 10:200 sccm flow rates on increasing the growth time to 5 min, as seen in Fig. 2.6.

Tapering occurs either due to reduction of the catalyst tip with growth caused by numerous factors like diffusion evaporation; or with catalytic droplet volume remaining the same via uncatalyzed VS deposition of Si.[74, 82] In our growth conditions, we see that Cu catalyst consumption seems to be the most probable cause for tapered MWs. Tapered structures are of significance as they have been reported to have superior field emission characteristics and higher light absorption due to graded refractive index.[74, 83]

2.3.2 Effect of growth parameters on Si MW growth rate and diameter

The effect of $SiCl_4$ and H_2 flow rates, sample position w.r.t. heater, Cu thickness, and growth time on Si MW diameter and length were studied to obtain highly ordered Si MWs and determine the growth rate at various growth conditions.

2.3.2.1 Effect of $SiCl_4$ gas flow rate and position of samples w.r.t heater on Si MW diameter and growth rate (10:200 sccm)

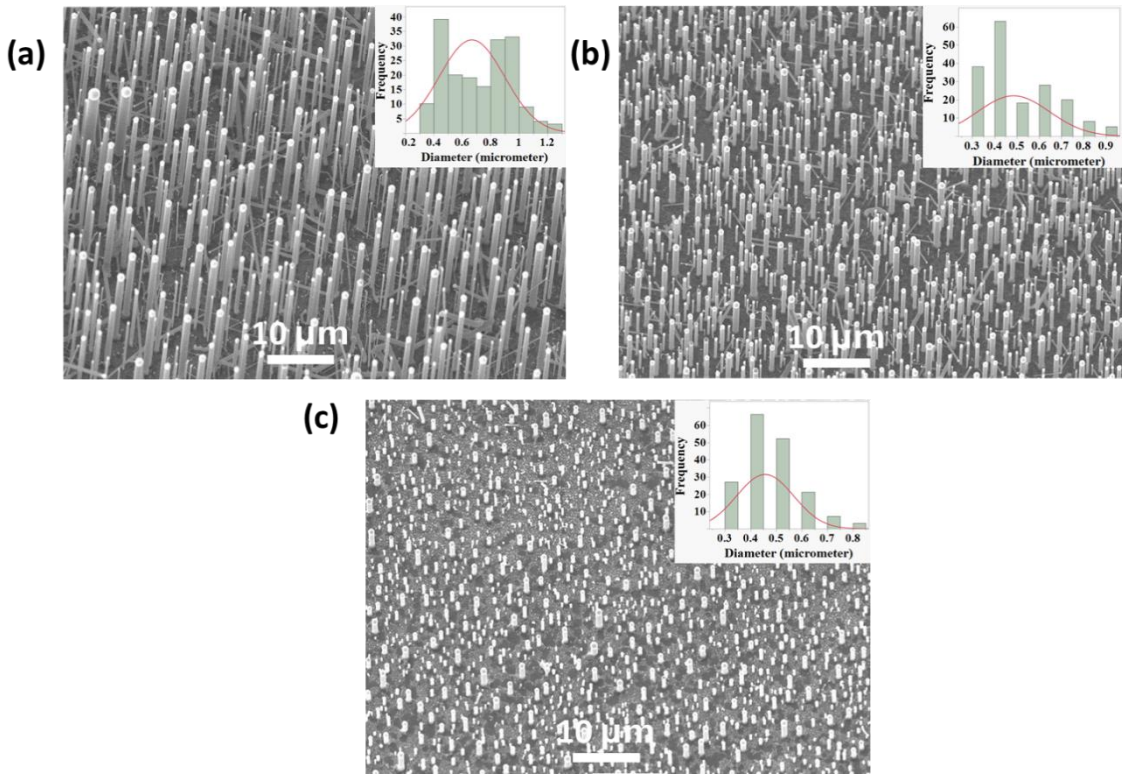


Figure 2.7 SEM micrographs and diameter distributions (insets) of Si MWs grown using 30 nm Cu thin film

30 nm Cu film was deposited on a freshly cleaned Si (111) wafer and annealed in-situ in the presence of Ar and H_2 (10:200 sccm) at 700 °C for 40 min. After annealing, the temperature was ramped up to the growth temperature, i.e., 1000 °C, and Ar bypassed to flow through the stainless-steel container containing $SiCl_4$ for a growth time of 3 min. The samples were placed at three different positions Ds (s=4,5,6 inch, respectively) in the quartz tube. The average diameter of the Si MWs was obtained using the measurement of more than 150 wires. The Si MWs grown at D_4 have an average diameter of 0.67 ± 0.23 µm, and Si MW diameter was observed to decrease downstream to 0.49 ± 0.16 µm at D_5 and 0.46 ± 0.11 µm at D_6, respectively, as shown in the inset

of Fig. 2.7 (a,b,c). In addition to the reduction of the diameter and standard deviation downstream, the Si MW length also decreased downstream from 60 μm at D_4 to 18 μm at D_5=5 inch and 2.8 μm at D_6, respectively, as shown in Appendix A1. The exponential dependence of the axial growth rate with the position is observed due to the decrease in concentration profile downstream, as seen in Fig. 2.8, and is explained in detail below. The velocity of the gas mixture is maximum at the center of the reactor tube and drops to zero when it touches the surface following a parabolic path[84] and is given by equation 1.1:

$$v(r) = v_o\left(1 - \frac{r^2}{r_o^2}\right) \text{.....1.1}$$

$$R_e = \frac{\rho v b}{\mu} \text{.....1.2}$$

where v_o is the maximum velocity, r_o is the reactor tube radius, ρ is density, v is average velocity, b is the diameter (22 mm), and μ is the viscosity of the gaseous mixture (Re is Reynold's number).

This velocity gradient results in the formation of a boundary layer of thickness δ(x). The boundary layer plays a vital role in the growth process and is a function of Reynold's number ($1/\sqrt{R_e}$) and distance (x).[81, 84] Depending upon the gas flow conditions, Reynold's number (R_e) for a CVD system lies between 0.01-100 for temperatures up to 1273K and can be calculated using equation 2.[84, 85] Assuming the equal amount of Ar and $SiCl_4$, the density of the gas mixture (Ar, H_2, and $SiCl_4$) at 1000 °C and 1 atm was calculated to be 1.09×10^{-4} g/cm^3. The average velocity (v) was calculated to be 0.96 cm/s.[85] Using the viscosity of the gas component from the available data,[86-88] viscosity of the mixture was estimated to be 316 μP, and R_e was measured to be about 0.73, which lies in the predicted range for the CVD system, implying that the flow is laminar.[85]

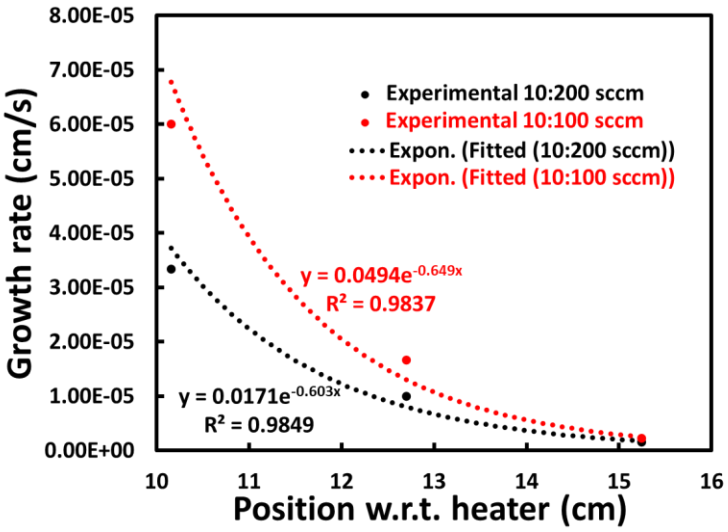
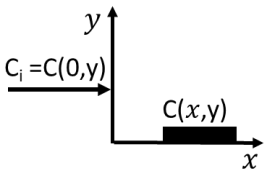


Figure 2.8 Exponential dependence of growth rate w.r.t the position of the substrate in an APCVD system.

After a critical length called entry length, the velocity profile is fully developed, the boundary layer from all sides of the reactor tube merges, and the whole cross-section of the tube consists of boundary layers. The reactant species must diffuse through this boundary layer to reach the surface of the sample for the growth process. The concentration of the reactant species that diffuses through this boundary layer decreases exponentially over the distance, as given by equation 2.3. Using Fick's diffusional law (equation 2.4), the growth rate $\dot{G}$ as an exponential function of x can be obtained as given in equation 2.5.[84]



$$C(x,y) = \frac{4C_i}{\pi} \sin\left(\frac{\pi y}{2b}\right) \exp^{-\left(\frac{\pi^2 Dx}{4vb^2}\right)} \ldots\ldots\ldots 2.3$$

Where C_i is the initial concentration at $x = 0$; D is the diffusivity; b is the diameter of the reactor tube.

From Fick's law, diffusional flux [84] is given by

$$J(x) = -D\frac{\partial C(x,y)}{\partial y} \text{.....2.4}$$

Substituting for $C(x,y)$ in the above equation, growth rate as a function of flux can be derived for CVD system assuming constant temperature, constant velocity component along the reactor axis with reactor length considered to be very long compared to other axes.[84]

$$\dot{G} = \frac{MJ(x)}{\rho M_s} = \frac{2C_i MD}{b\rho M_s} e^{-\frac{\pi^2 Dx}{4vb^2}} \text{.....2.5}$$

where M and M_s are molecular weights of Si and source (here $SiCl_4$), respectively.

Since the growth rate has a weak Arrhenius type temperature dependence,[72, 73] the temperature gradient's effect along the reactor tube would be small compared to the exponential dependence on the position. Hence, the decrease in the axial growth rate of Si MWs downstream with distance, as shown in Fig. 2.8, is mainly due to the exponential decrease in the concentration of the reactant species as it diffuses through the boundary layer to reach the reaction site.

The growth of Si MWs via the VLS process consists of the following four steps (i) mass transport, (ii) adsorption/incorporation of Si atoms in the Cu-Si liquid alloy, (iii) diffusion of Si atoms in the liquid alloy, and (iv) incorporation of the Si atoms in the crystal (crystallization). In the case of Si wires grown in APCVD using high temperature, incorporation or crystallization has been observed to be a rate-limiting step.[72, 73, 76] Jeong et al.[72] observed that crystallization was the rate-limiting step for Pt and Au catalyzed Si wire growth. On the other hand, varying the $SiCl_4$ partial pressure, Eichfeld et al.[73] reported mass-transport of Si flux as a rate-limiting step. Herein, the growth kinetics of Si MWs were studied w.r.t the different positions of the samples in the

APCVD system. An exponential dependence of axial growth rate with position due to the concentration gradient of the reactant species suggests that there is depletion of the reacting species as we move downstream, hence, mass transport of the precursor is the rate-limiting step. We can, thus, conclude that the mass-transport of Si flux mainly limits the axial growth rate of Si MWs as we move downstream, assuming temperature dependence on growth rate to be very small. On the other hand, the catalyst NP size mainly determines the Si MW size and distribution.

2.3.2.2 Effect of hydrogen flow rate and position w.r.t heater on Si MW diameter and growth rate (10:100 sccm)

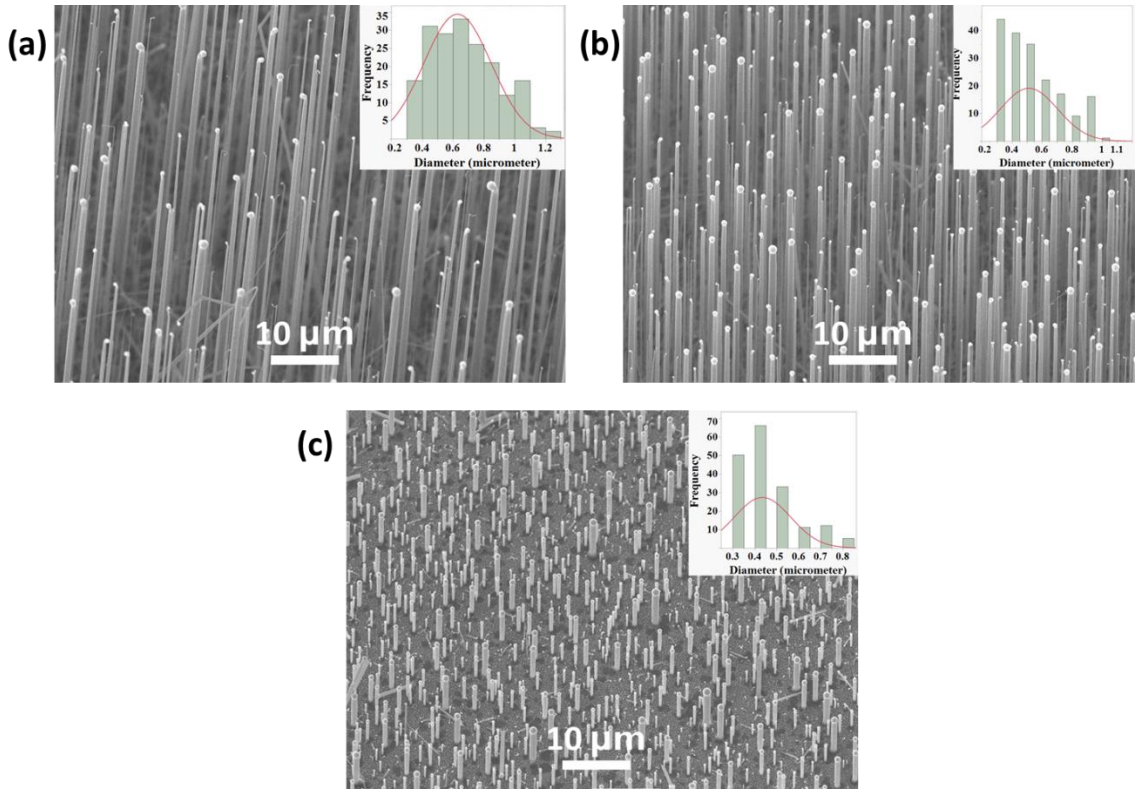


Figure 2.9 SEM micrographs of Si MWs grown using 30 nm Cu, annealed at 700 °C, 40 min with Ar: H_2 (10:100 sccm) for 3 min at position (a) D_4 (b) D_5, and (c) D_6.

Using the same growth condition as mentioned in the previous case and varying H_2 flow rate, the effect of the reducing H_2 flow rate on Si MW diameter and length was studied. The average diameter was observed to decrease downstream from 0.63 ± 0.22 µm at D_4, 0.51± 0.19 µm at D_5 to 0.43± 0.13 µm at D_6, respectively. The Si MW length decreased with distance from 108 µm at D_4 to 30 µm at D_5 and 4 µm at D_6, respectively, as shown in Appendix A2. The average diameter was almost similar in dimension to the previous case with a higher H_2 flow rate (200 sccm). The Si MW length was observed to increase significantly when H_2 flux was reduced, and kinking was prevalent in the longer wires as compared to the ones grown using a higher H_2 flow rate. This increase in length, and hence the growth rate with a decrease in H_2 flux, as shown in Figure 2.8, can be explained in terms of the increase in $SiCl_4$ partial pressure and the higher impingement rate of precursor gas when the gas flow rate is slow.

Table 2.1 Average diameter of Si MWs at different flow rates w.r.t position of Si substrate

Position w.r.t. heater (inches)	Avg. diameter (µm) (10:200)	Avg. diameter (µm) (10:100)
4	0.67±0.23	0.63±0.22
5	0.49±0.16	0.51±0.19
6	0.46±0.11	0.43±0.13

Wagner et al.[89] provided the empirical formula of growth rate for a dynamic system for a high flow rate with a condensation co-efficient of unity and predicted the increase in growth rate due to the higher impingement rate of $SiCl_4$ molecules at a slow gas flow rate. Additionally, Eichfeld et al. reported the dependence of the growth rate of Si wires on the partial pressure of $SiCl_4$ precursor. Depending upon the growth regime (growth vs. etching), the growth rate of Si

MW increases then decreases with an increase in $SiCl_4$ partial pressure.[73] Hence, decreasing the H_2 flow rate from 200 sccm to 100 sccm would reduce the total gas flow rate from 210 sccm to 110 sccm, whereas the molar fraction of $SiCl_4/H_2$ will increase from 0.05 to 0.1; thus, a net increase in growth rate is observed as an increased number of $SiCl_4$ precursor is available at the reaction site at a slower flow rate.

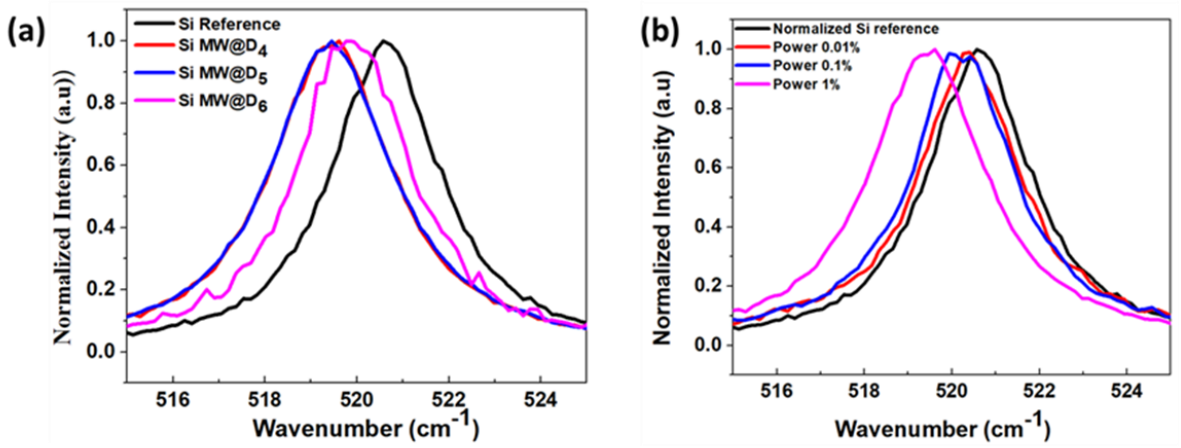


Figure 2.10 Raman spectra for Si MWs grown at Ar: H_2 10:100 sccm at (a) D_4, D_5, and D_6, and (b) Raman spectra of Si MW grown at D_4 using three different laser powers.

Raman spectra for the Si MWs grown at D_4, D_5 exhibited transverse optical (TO) peak at ~519 cm^{-1} with a redshift of ~1cm^{-1} from Si reference when 532 nm laser with incident power of 1% was made incident, as shown in Fig. 3, (a). The full-width half maxima (FWHM) for bulk Si was 2.74 cm^{-1}, and FWHM for Si MWs grown at D_4 and D_5 were ~3.1 cm^{-1}, respectively. A redshift of ~1 cm^{-1} and FWHM broadening observed in TO-mode in the case of Si MWs can be associated with laser-induced heating, phonon confinement, or strain.[90] The average diameter of the Si MWs is in the range of 0.4-0.6 μm; hence phonon confinement can be ruled out as a possible cause for the red shifting of the Si MW peak. The most probable cause of the observed redshift and FWHM broadening in our samples is the localized heating effect caused by the laser beam exposure, as

reported by Torres et al.[91] A laser power-dependent study was performed to confirm the observed redshift in Raman spectra due to the heating effect, as shown in Fig. 2.10 (b). The Raman spectra peak for Si MWs grown at D_4 shifted closer to that of the Si reference from 519.4 cm^{-1} to 520.4 cm^{-1}, and FWHM also decreased from 3.1 cm^{-1} to 2.7 cm^{-1} as the incident power intensity was reduced from 1% to 0.01% hence confirming the heating effect on Raman spectra of Si MWs.

2.3.2.3 Effect of Cu thickness and growth time on Si MW diameter and length

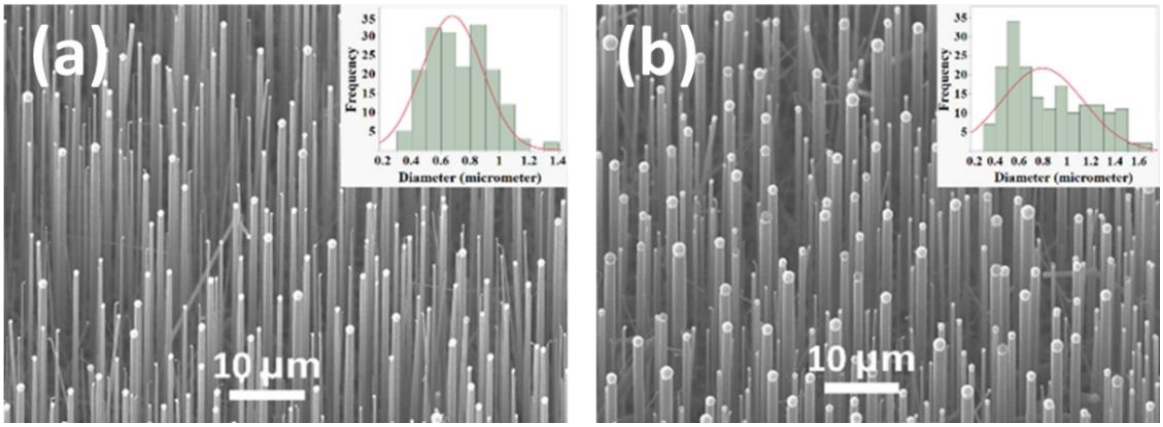


Figure 2.11 SEM micrographs of Si MWs grown using (a) 30 nm Cu (b) 40 nm Cu annealed at 1000 °C, 5 min with Ar: H_2 (10:200 sccm), and growth time of 5 min at D_4.

Table 2.2 Si MW diameter and length at D_4 and D_5 using 30 nm and 40 nm Cu catalyst film, respectively.

Position w.r.t. heater (inches)	Avg. diameter (µm)		Length (µm)	
	30 nm Cu	40 nm Cu	30 nm Cu	40 nm Cu
4	0.68±0.21	0.79±0.34	110	105
5	0.48±0.14	0.62±0.18	47	40

Si MWs were grown for 5 min with Ar and H_2 (10:200 sccm) using Cu thin film of 30 nm and 40 nm, respectively. It was observed that increasing Cu film thickness resulted in larger diameters: 0.68 ± 0.21 μm at D_4 and 0.48±0.14 μm at D_5 using 30 nm Cu thin film; 0.79± 0.34 μm at D_4 and 0.62± 0.18 μm at D_5 for the Si MWs grown using 40 nm Cu thin film as shown in Fig. 2.11. The increase in Si MW diameter is attributed to the increased thickness of the catalyst thin film.[92] However, the Si MW length was observed to decrease from 110 μm at D_4 and 47 μm at D_5 for 30 nm Cu thin film to 105 μm at D_4 and 40 μm at D_5 for 40 nm Cu thin film, respectively, as seen in Appendix A3. In general, an increase in Si MW diameter results in an increase in supersaturation, hence an increase in the growth rate.[85] The opposite dependence of growth rate on diameter has also been observed. The incorporation and crystallization interplay determine the net increase or decrease in Si wire diameter.[76] Dhalluin et al.[71] modified the Schmidt model of diameter dependence and introduced the incubation time to determine the wire length. Additionally, for the same deposition volume, a larger diameter MW will be shorter in length as compared to a smaller diameter MW. Thus, the increase in the incubation time with the increase in diameter and the volume effect results in an observed decrease in MW length for the thicker catalyst layer.

An increase in the growth time from 3 min to 5 min, and 7 min, respectively, for samples grown at position D_4 resulted in the increase in diameter from 0.68±0.26 μm to 0.79 ± 0.34 μm to 0.85 ± 0.30 μm and length increased from 35 μm to 96 μm and about 160 μm, as shown in Figure 2.12, and Appendix A4. In addition to the increase in Si MW length as reported by Eichfeld et al.[73], the diameter was also observed to increase with time. The increase in diameter with time

can be explained by the scattering of the incident gas flux from the sidewalls of the adjacent nanowires resulting in vapor-solid (VS) growth as proposed by Sharma et al. [93]

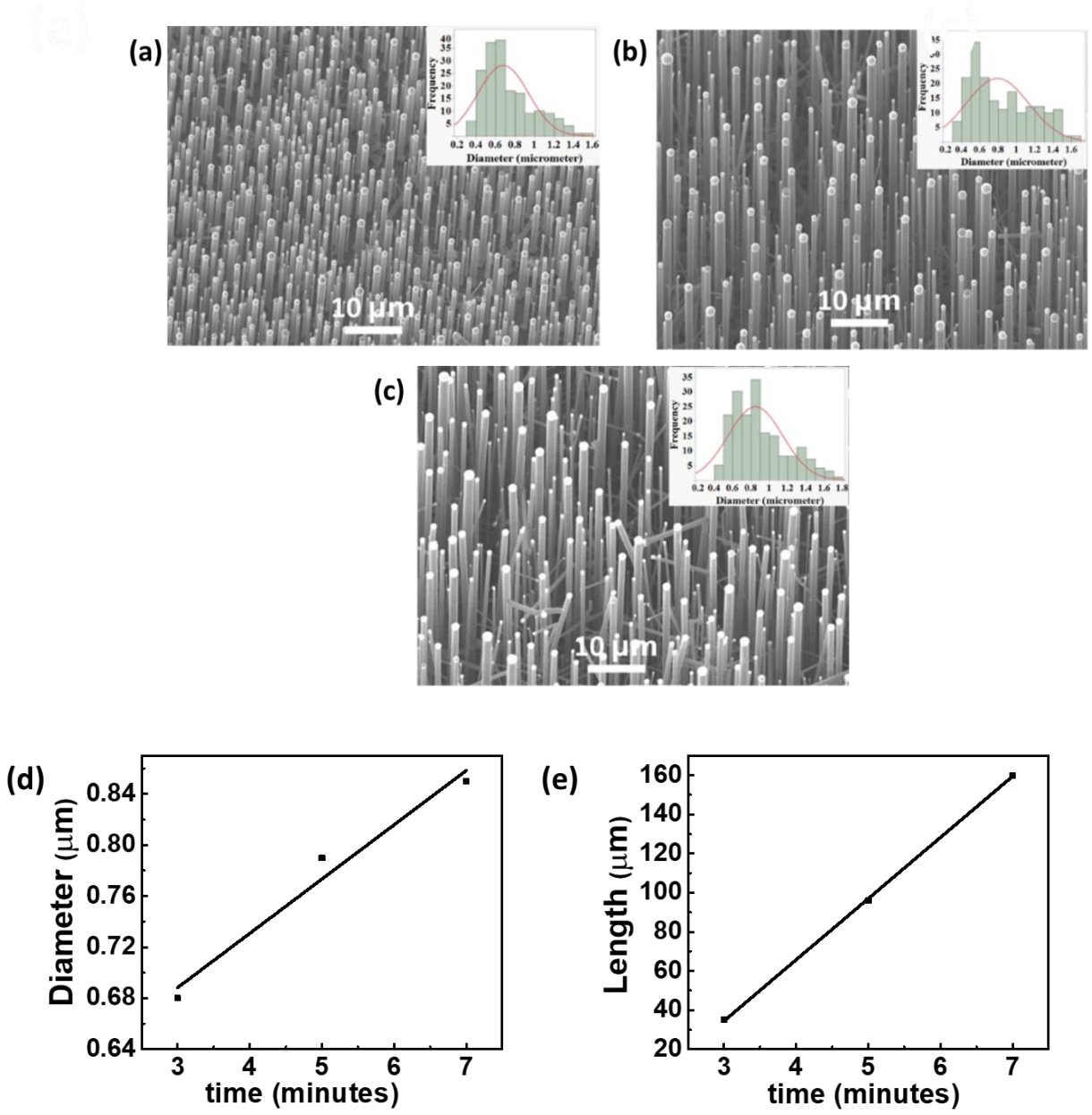


Figure 2.12 SEM micrographs of Si MWs grown using 30 nm Cu annealed at 1000 °C, 5 min with Ar: H_2 (10:200 sccm) at D_4 with growth time (a) 3 min, (b) 5 min, and (c) 7 min, respectively (d) Variation of Si MW diameter and (e) length with time.

2.4 Conclusion

Si MW morphology was observed to be dependent on growth temperature, Cu film thickness, and gas flow rates. The areal density of Si MWs was observed to be influenced by annealing ambiance and position at a low $SiCl_4$ gas flow rate (Ar: H_2::3:200 sccm). It was observed that the Si MW diameter, length, and growth rate can be tuned by varying the gas flow rates, position, Cu thickness, and growth time. The mass transport of the precursor was most likely the rate-limiting step in the Si MW growth resulting in an exponential decrease in the axial growth rate with distance. The average Si MW diameter decreased from 0.67±0.23μm to 0.46±0.11 μm from D_4 to D_6 for Si MWs grown at 200 sccm H_2 flow rate. Si MW growth rate was observed to increase from 20 μm/min to 36 μm/min at D_4 with a decrease in H_2 flux to 100 sccm due to the increase in the partial pressure of $SiCl_4$. An increase in Cu thickness resulted in a larger diameter of up to 0.79±0.34 μm for samples grown at D_4 and exhibited inverse dependence of growth rate on wire diameter due to an increase in incubation time to supersaturate. The increase in Si MW diameter with growth time suggested the contribution of uncatalyzed VS growth on the sidewalls along with the catalyzed VLS growth.

CHAPTER 3: ELECTRICAL CHARACTERIZATION USING TWO-PROBE AND THREE-PROBE MEASUREMENT

3.1 Introduction

3.1.1 Metal-Semiconductor contact

The electrical properties of a semiconductor are strongly dependent on the metal-semiconductor contact.[94] The metal-semiconductor contact can be either rectifying (non-linear) or ohmic (linear) depending upon the difference between the work-function of metal (φ_m) and electron affinity of the semiconductor (χ).[95, 96] A metal-semiconductor contact with the Schottky junction will show asymmetrical I-V characteristics with a large current in forward bias and negligible at reverse bias. On the other hand, an ohmic contact will exhibit symmetric linear I-V characteristics with the negligible voltage drop across the metal-semiconductor junction, allowing easy flow of charge carriers during forward and reverse bias. Schottky and ohmic junction band alignment with a p-type semiconductor will be discussed below.

3.1.1.1 Schottky contact with the p-type semiconductor

We consider an ideal metal-semiconductor (p-type Si) contact for the case when the work function of a metal φ_m is less than that of the semiconductor φ_s. The energy band diagram before and after the metal-semiconductor makes contact and reaches thermal equilibrium is shown in Fig. 3.1 (a-b). Work function φ is the amount of energy required to remove the electron from the Fermi level E_f to the vacuum level. The electron affinity χ is defined as the amount of energy needed to remove an electron from the conduction band E_c of the semiconductor to the vacuum level. When

the metal and p-type semiconductor is in contact with each other, the electrons move from metal to the semiconductor till the Fermi level aligns at thermal equilibrium resulting in net negative charge (hole depletion) at the semiconductor surface. The surface of the semiconductor becomes relatively n-type as compared to bulk resulting in the band bending and formation of the Schottky junction with a barrier height φ_b as shown in Fig. 3.1 (a, b).

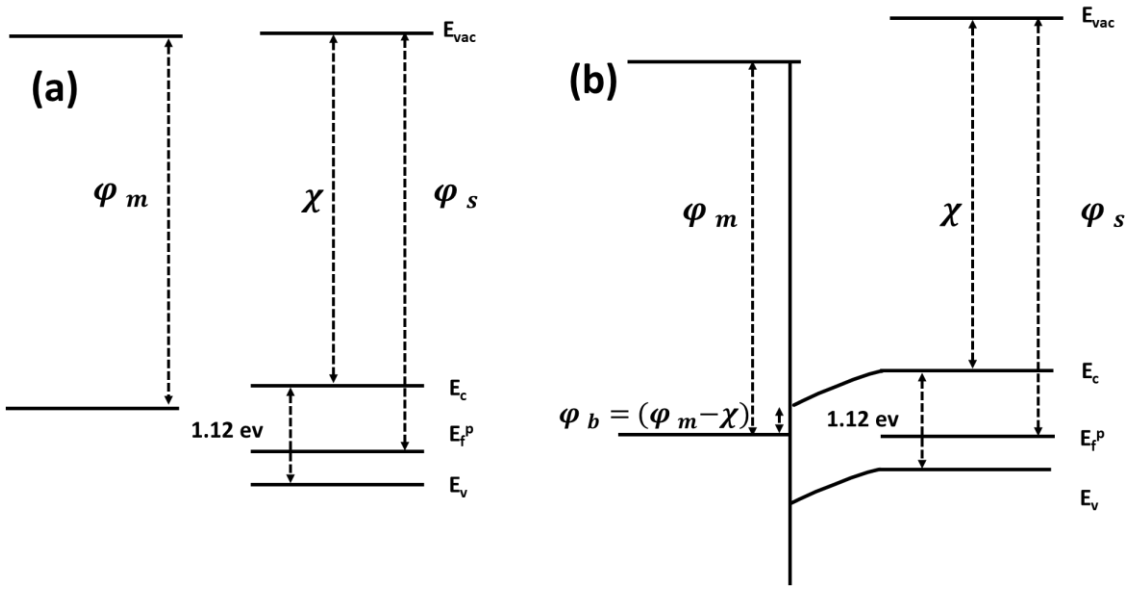


Figure 3.1 Energy band diagram of metal-semiconductor (p-type Si) (a) before coming in contact (b) at thermal equilibrium, showing Schottky behavior.

3.1.1.2 Ohmic contact with the p-type semiconductor

Next, we consider an ideal metal-semiconductor (p-type Si) contact for the case when the work function of a metal (φ_m) is higher than that of the semiconductor (φ_s). The band diagram before and after metal and semiconductor come in contact is shown in Fig. 3.2(a) and (b), respectively. As fermi level of metal (E_f^m) is lower than the Fermi level of semiconductor (E_f^m), the electrons move from semiconductor to metal resulting in the positive charge at the semiconductor surface. Since the surface of the semiconductor becomes more positive as

compared to the bulk, the band bends upwards. Due to this band bending, the hole movement does not see any barrier as seen in the Schottky junction, thus providing an easy flow of carriers across the junction regardless of the applied bias (forward or reverse). Therefore, metal-semiconductor junction with metal work function higher than p-type semiconductor exhibits ohmic behavior.

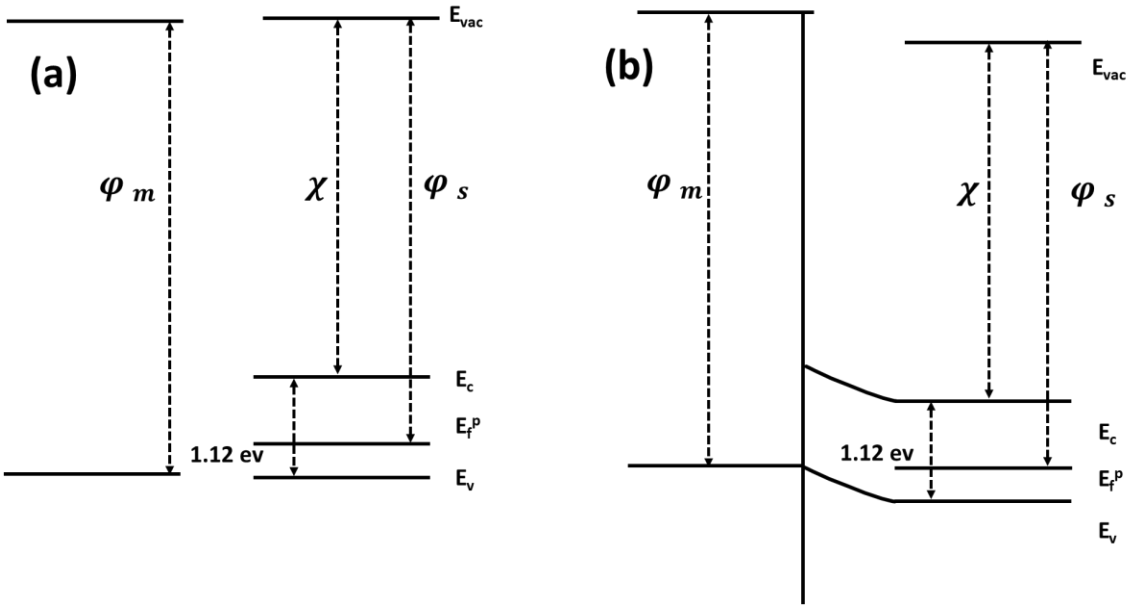


Figure 3.2 Energy band diagram of metal-semiconductor (p-type Si) (a) before coming in contact (b) at thermal equilibrium, showing Ohmic behavior.

3.1.2 Metal-Semiconductor-Metal (M-S-M) contact

The Si MW device with a metal contact on both ends exhibits metal-semiconductor-metal (M-S-M) behavior, with Si MW as a resistor in series with two back-to-back metal-semiconductor (M-S) contacts. During one cycle of the applied bias (positive or negative), in the case of a Schottky contact between a metal and a semiconductor, the M-S-M contact will exhibit forward bias characteristics at one junction, while the other side of the junction will be reverse biased. In this configuration (as reported by Zhang et al.)[97], the reverse-biased junction controls the amount

of current flowing through the system as the maximum voltage will drop across the reverse-biased junction.

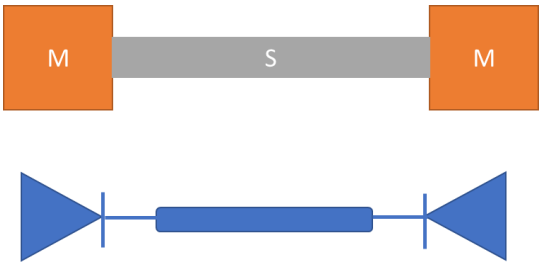


Figure 3.3 Schematic of M-S-M contact

3.1.3 Space charge limited current (SCLC)

Space charge is a term used when the charge is distributed over a region of space, mainly in the dielectric medium (here metal-semiconductor interface). The flow of charge through a semiconductor or dielectric material is often limited by the presence of the space charge formed inside it, resulting in the space charge limited current. The charge carriers tend to accumulate at the trap states present in bulk or at the surface of the material, and as a higher bias is applied, these trap states release the charge carrier and modulate the shape of the I-V curve ($I \alpha V^m$) where m>2, and background dopants lead to m=1 at low bias field.

SCLC measurement helps determine fundamental properties of materials like drift mobility, free carrier density, and trap density.[98] SCLC is mainly observed in materials with low effective carrier concentration like wide bandgap semiconductors, insulators, and poorly conducting polymers.[99] There are two types of SCLC behavior, i.e., trap-assisted and trap-free with power (m>2 and m=2), respectively. The Mott-Gurney (MG) law is applied to determine the I-V characteristics at the SCLC region for the undoped, trap-free semiconducting material sandwiched between ohmic contacts.[95]

At low voltage (V), when the equilibrium electron concentration (n_o) is much larger than the injected carrier concentration, the current density (J) follows ohm's law and is given by the following equation[99, 100]:

$$J = \frac{en_o\mu V}{L} \text{.....(3.1)}$$

where μ is mobility, and L is the separation between the contacts.

At crossover voltage (V_c), when the injected charge carriers exceed the thermal equilibrium carriers, non-linear transport characteristics with $J \propto V^2$ corresponding to the SCL effect is observed, and the electric field and charge distribution becomes non-uniform and depends on the sample geometry.[98, 99, 101] The analytical solution for SCLC characteristics in bulk materials, also known as Mott-Gurney-Law, is given by the following equation[99]:

$$J = \frac{9}{8}\frac{\epsilon_o\epsilon_r\mu V^2}{L^3} \text{.....(3.2)}$$

where ϵ_o is the permittivity of free space, and ϵ_r is the relative permittivity of the bulk material. SCLC regime at a high bias ($I \propto V^a$, with a=2 for trap-free material and a>2 for materials with traps). The sensitivity of nanowires on SCL effects is ascribed to its high aspect ratio, resulting in the poor screening of the injected charge carriers and the depletion of carriers due to enhanced surface states.[99, 102]

Katzenmeyer et al.[103] modified the MG law for the 1D structure (equation 3.3) using scaling factor ς (R/L), given by where R is the radius, L is length, ε permittivity of Si:

$$J = \varsigma\left(\frac{R}{L}\right)\frac{\varepsilon\mu}{L^3}V^2 \text{.....(3.3)}$$

In the case of a high aspect ratio R/L<<1

$$\varsigma\left(\frac{R}{L}\right) = \varsigma_0\left(\frac{R^{-2}}{L^{-2}}\right)\text{.....(3.4)}$$

where ς_0 is the numerical constant of order unity

Thus the mobility of high aspect ratio one-dimensional structure in the SCL regime is given by equation 3.5:

$$\mu_{SCL=\frac{IL}{V^2\pi\varepsilon}}\text{.....(3.5)}$$

In real devices, the non-ideal semiconductor features like traps, doping, and injection barriers due to the type of metal contacts used to deviate from the ideal I-V curve and underestimate mobility.[95] The modified Katzenmeyer equation for SCLC with traps is given by[100, 104] equation 3.6 below:

$$J_{mod} = \theta\varsigma_o\left(\frac{R^{-2}}{L^{-2}}\right)\frac{\varepsilon\mu}{L^3}V^2\text{.....(3.6)}$$

$$\theta = \frac{n}{n+n_t}\text{.....(3.7)}$$

where θ is the trap parameter, n is the density of electrons in the conduction band, and n_t is the occupation density of traps.

In the presence of traps, some injected carriers get trapped; thus, the measured mobility (μ_{eff}) is underestimated by a factor of θ ($\mu_{eff} = \theta\mu$).[104] As we increase the voltage, the number of trap states occupied increases until all trap states are filled. Any increase in voltage beyond this will result in an abrupt increase in current, and the voltage corresponding to this is known as V_{TFL}

(trap-filled limit voltage). The trap state density N_t and trap parameter can determine the trap energy level E_t.[105]

The log-log scale of J-V measurement is used to determine the ohmic region at low voltage with a slope of 1, non-linear SCLC region with traps (if any) at median voltage with slope >2, and trap-free SCLC region at a higher voltage with slope=2.

The trap-density n_t can be extracted from V_{TFL} using $V_{TFL}=\frac{qn_tL^2}{2\varepsilon}$, where q is the elementary charge. The trap-density can be extracted from SCLC when n_t exceeds the free carrier concentration n_{diff}. The minimum trap-density that can be resolved from SCLC is given by[106] :

$$n_{t,min} = n_{diff} = \frac{4\pi^2 KT\varepsilon}{q^2L^2} \text{.....(3.8)}$$

3.2 Experimental method

3.2.1 Sample preparation for two-probe measurement

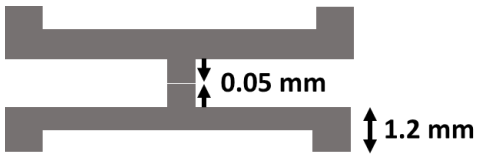


Figure 3.4 Schematic of the shadow mask used for two-probe and three-probe measurements

The process flow for the fabrication of Si MW device for electrical characterization included substrate cleaning, Cu and oxide etching, Si MW dispersion, drop-casting Si MWs on cleaned Si substrate, mask aligning, and thermal evaporation of Ag. The prime grade n-Si substrate (ρ=1-10 Ω-cm) with 300 nm thermal oxide was cut into small pieces of 1x1 cm^2 and rinsed with acetone and isopropyl alcohol, followed by N_2 blow dry. As-grown Si MWs were dipped in

buffered hydrofluoric acid (BHF) to remove the thermal oxide, rinsed with DI water, blow-dried using N_2, and then etched in Cu etchant to remove the residual Cu catalyst. Iron (III) chloride solution was prepared, and the Si MW array was dipped in the Cu etchant for 30 min and rinsed with DI water. After that, the sample was immersed in KOH for 10 s and rinsed with DI water to remove any residual iron (III) chloride. The Si MW array was then treated with BHF solution for 10 s to remove any native oxide layer formed during the reaction. The Si MW array was then ultrasonicated in an isopropyl alcohol solution to disperse it and drop-casted on a glass slide/Si substrate with thermal oxide of 300 nm. The metal contact was deposited on the two ends of Si MWs by aligning a shadow mask (Fig. 3.4) and evaporating 300-400 nm of Ag using a thermal evaporator. The two-probe I-V measurement was performed by using Keithley 4200 semiconductor parameter analyzer system. The Mott-Gurney law was used to determine the effective mobility of the as-grown Si MWs via the SCLC mechanism.

3.2.2 Field-effect transistor (FET) fabrication

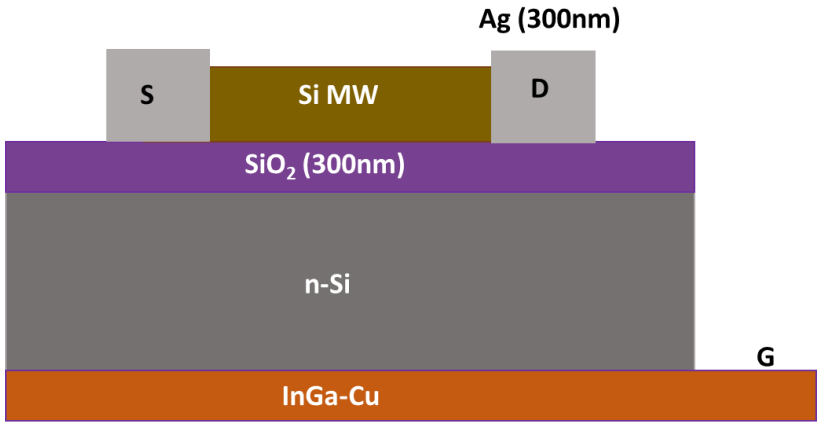


Figure 3.5 Schematic of back-gated FET device

The etched Si MW was drop-casted on a clean Si/SiO_2 substrate, and metal contact was evaporated using the same procedure as mentioned in section 3.2.1. Ag electrode of 400 nm

thickness was thermally evaporated on the drop-casted Si MW using a shadow mask and served as source and drain contact. The gate contact for the FET measurement was fabricated by etching the oxide layer at the back of the Si substrate and using InGa to make contact between the Cu and the backside of the Si substrate. Three-probe I-V measurements were performed at room temperature using a Keithley 4200 characterization system to determine whether the as-grown intrinsic Si MW is p-type or n-type and determine the figure of merit of FET (i.e., g_m, ON/OFF ratio, mobility of charge carrier, and V_T).

3.3 Results and discussion

3.3.1 Two-probe measurement of H-terminated D_4-Si MW via Space charge limited current (SCLC) mechanism

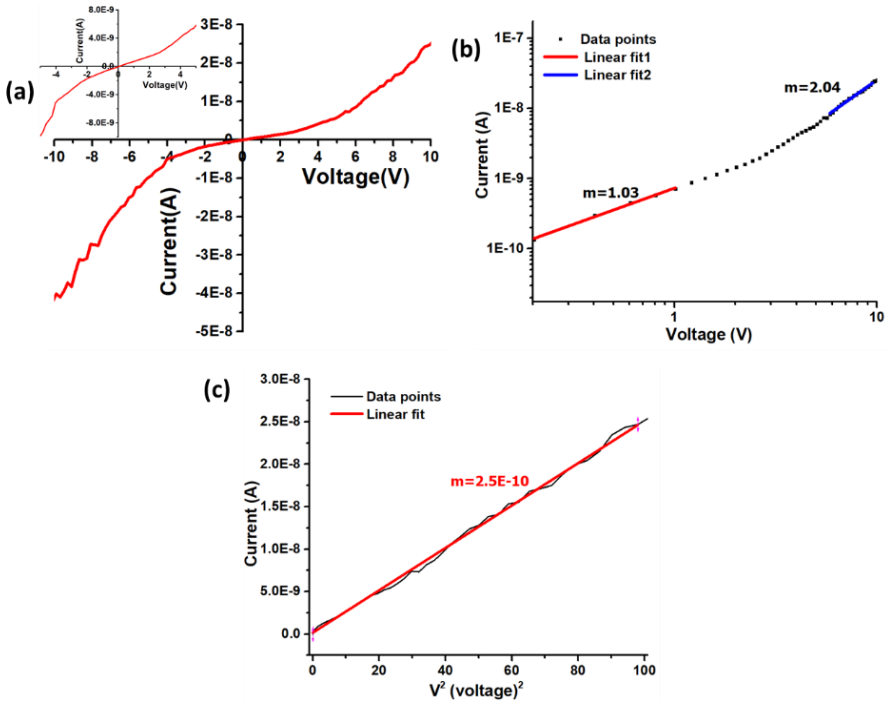


Figure 3.6 (a) I-V characteristics of H-terminated D_4-Si MW on a glass slide, (b) log I-log V plot, and (c) I-V^2 plot

The charge transport property of H-terminated D_4-Si MW (with following growth parameters-Ar: H_2::10:200 sccm, grown at D_4) was studied via two-probe measurement on different substrates. I-V characteristics of Si MW device prepared on glass and SiO_2/Si substrate were investigated at room temperature using Keithley 4200 semiconducting parameter analyzer.

The I-V curve for the Si MW on the glass substrate showed a non-linear and asymmetric behavior due to unintended non-identical M-S contact on both ends of the MW, as shown in Fig. 3.6 (a). The log I vs. log V curve in Fig. 3.6 (b) demonstrated a power dependence relation $I \propto V^m$ in different voltage ranges. The lower voltage region with m=1 exhibits ohmic behavior, and the current in the MW is dominated by thermally generated charge carriers. The current at a higher voltage range shows a power dependence on the applied voltage. The charge transport mechanism can be explained by the injection of charge carriers by space charge known as the SCLC conduction mechanism. The injected charge concentration will dominate the thermally generated charge carriers at high voltages.

Linear dependence obtained in the I-V^2 plot, as shown in Fig. 3.6 (c), confirms that the charge transport is limited by SCLC at a higher voltage. The room temperature mobility of Si MW can be determined using the method reported by Katzenmeyer et al.[103] in equation 3.5. Since the slope m>2, the mobility extracted from MG law would be lower than the actual value by a factor of θ (trap parameter); hence the extracted mobility, in this case, would be the effective mobility due to the trap states. The calculated effective charge mobility for Si MW on glass was found to be 0.192 $cm^2V^{-1}s^{-1}$ for MW of about 25 µm in length.

Wide variation in reported values of hole mobility of Si NWs, from 3.17 $cm^2V^{-1}s^{-1}$ for B-doped Si NW FET by Cui et al.[7], 7.5-102 $cm^2V^{-1}s^{-1}$ for B-doped vertically integrated Si NW FET by Goldberger et al.[107], 0.001-1350 $cm^2V^{-1}s^{-1}$ for B doped Si NW FET by Cui et al.[108], is prevalent in the literature owing to the difference in dopant level, purity of the as-grown wires, the difference in contact material and quality of the contact, dimension of the material (bulk, thin-film or wire configuration), size of the wire, etc. The lower mobility of 0.192 $cm^2V^{-1}s^{-1}$ of as-grown Si MW drop-casted on glass substrate could be because of the surface roughness present between the Si MW and the glass surface resulting in poor contact properties and due to the presence of traps.

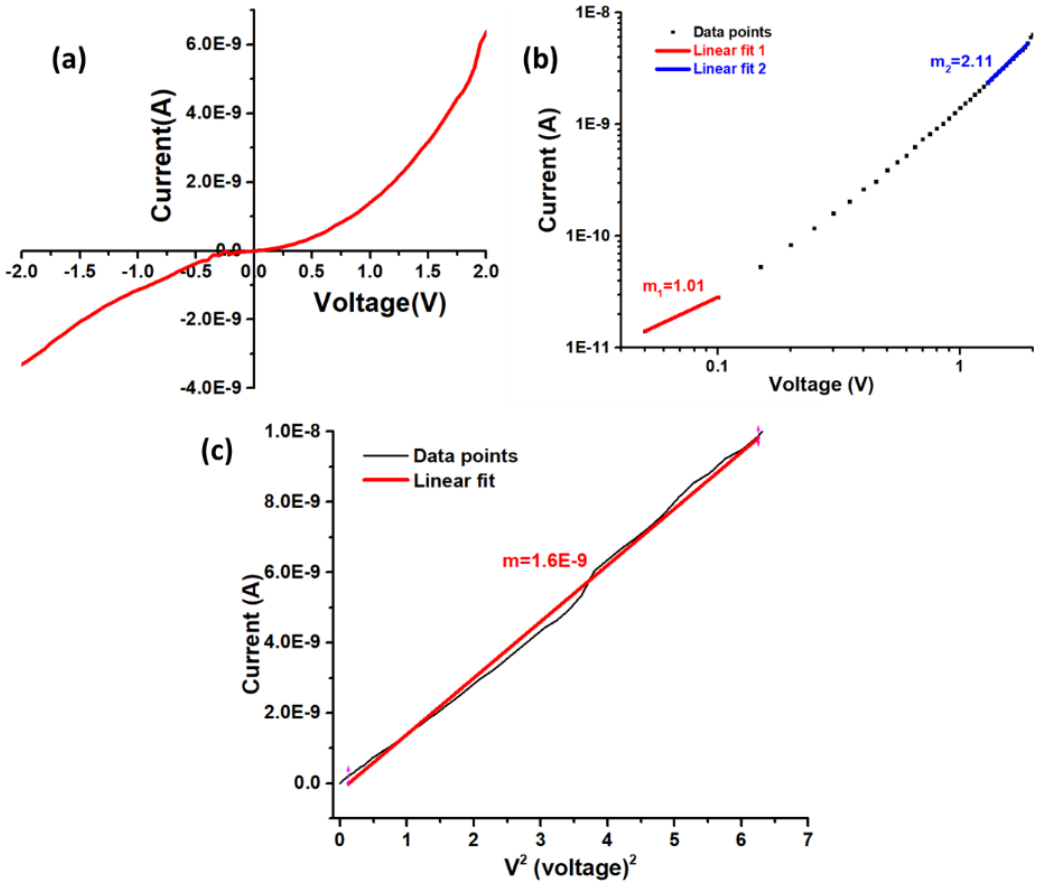


Figure 3.7 (a) I-V characteristics of H-terminated D_4-Si MW on Si/SiO_2 substrate, (b) log I-log V plot, (c) I-V^2 plot

The Si MW with the same growth conditions was drop-casted on SiO_2/Si substrate, and a two-probe room temperature measurement was performed on it. The I-V curve obtained was asymmetric with m=1 at low voltage and m=2.11 at higher voltage and exhibited a linear relationship between I and V^2 as shown in Fig. 3.7 (a-c). An increase in current is observed in the case of MW on SiO_2/Si compared to that on the glass substrate, which clearly shows an improved contact across the MW due to reduced surface roughness of the SiO_2/Si MW surface. The effective mobility of the charge carrier, thus increased to 1.47 $cm^2V^{-1}s^{-1}$ for MW of 30 μm length, improved marginally due to the decrease in surface roughness of the substrate and allowed better charge transfer. Free carrier concentration of $6.8x10^{12}$ cm^{-3} was extracted using equation 3.1.

3.3.2 Three-probe measurement of H-terminated D_4-Si MW via Field-effect transistor (FET) measurement

The electrical transport properties of the FET device fabricated using H-terminated D_4-Si MW grown for different growth time were studied. The output characteristic (I_{ds} vs. V_{ds}) of Si MW (with growth time of 5 min, the radius of 350 nm, 30 μm long) at constant applied gate voltage exhibited an inverse relationship between the V_{gs} and I_{ds}, i.e., with positive/negative V_{gs}, the current across the Si MW decreased/increased, which is the typical behavior of p-type semiconductors, as shown in Fig. 3.8(a). An applied positive/negative V_{gs} creates a depletion /accumulation region at the Si MW surface in contact with the oxide surface, which helps to modulate the majority positive charge (hole) carriers flowing through it under applied $V_{ds,}$ as shown in Fig. 3.8 (a-b). The threshold voltage V_T is defined as V_{gs} needed to induce the conducting channel in the MW. The transfer characteristic (I_{ds} vs. V_{gs} at a constant V_{ds}) showed that as V_{gs}

becomes more negative, the hole current increased, and beyond -0.5 V, I_{ds} saturated and showed a negative slope in the linear region, as shown in Fig. 3.8 (b).

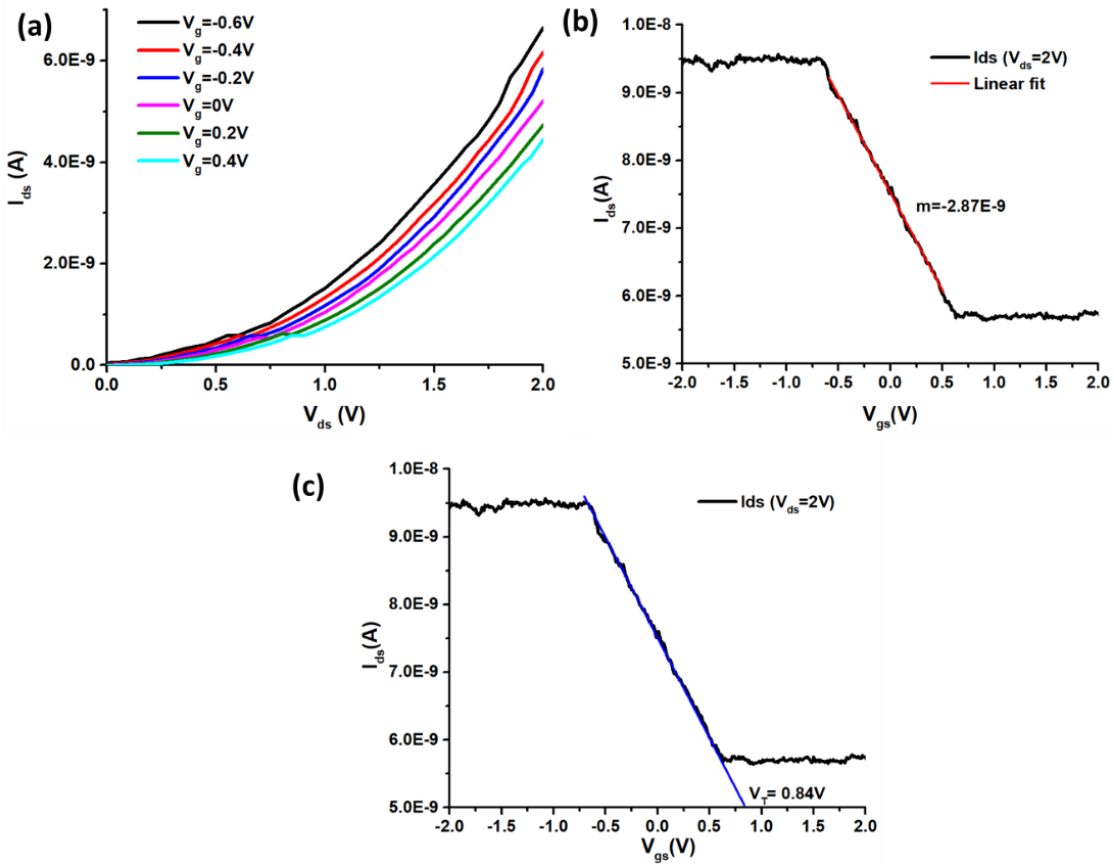


Figure 3.8 (a) Output characteristic (I_{ds} vs. V_{ds}) at various gate-source voltages (V_{gs}), (b and c) transfer characteristics (I_{ds} vs. V_{gs}) at V_{ds} =2V, and threshold voltage (V_T) intercept for H-terminated D_4-Si MW with back-gate FET grown for 5 min.

The figure of merit of H-terminated D_4-Si MW-FET, e.g., transconductance, normalized transconductance, threshold voltage, I_{ON}/I_{OFF} ratio, and mobility, was extracted from the I_{ds}-V_{gs} plot (Fig. 3.8 (b-c)). The effective mobility of the hole in the H-terminated D_4-Si MW-FET was determined using equation 3.8 as reported by Park et al.[109], where g_m is the transconductance, and L is the length of the channel, C is capacitance, and V_{ds} is the source-drain voltage. Capacitance (C) was determined by considering MW as a cylinder using an infinite plate model and was

calculated by using equation 3.9, where t is the oxide thickness, r is the radius of MW, ε_0 is the permittivity of free space, and ε is the dielectric constant of SiO_2. The hole mobility of 1.19 $cm^2V^{-1}s^{-1}$ was obtained for the Si MW at V_{ds}=2V. The mobility of Si MW determined using the SCLC mechanism in section 3.3.1 was 1.47 $cm^2V^{-1}s^{-1}$, which is of the same order as obtained from FET measurement.

$$\mu = \frac{g_m L^2}{C V_{sd}} \text{.....(3.8)}$$

$$C = \frac{2\pi\varepsilon\varepsilon_0 L}{ln(2t/r)} \text{.....(3.9)}$$

$$\mu = \frac{g_m L^2 ln(2t/r)}{2\pi\varepsilon\varepsilon_0 L V_{sd}} \text{.....(3.10)}$$

The transconductance g_m= 2.87x10^{-9} S was extracted from the slope of I_{ds} vs. V_{gs} in the linear region. Considering the effective channel width of FET as same as that of the diameter of Si MW, the normalized transconductance was measured to be ~7.5x10^{-3}S/m. Threshold voltage V_T of 0.84 V was extracted from the I_{ds} vs. V_{gs} curve by extrapolating the slope such that it cuts the x-axis, as shown in Fig. 3.8(c). I_{ON}/I_{OFF} ratio corresponded to the ratio[107] of I_{ds} at current saturation (V_{gs} on) to I_{ds} at depletion (V_{gs} =0) and was about ~2.

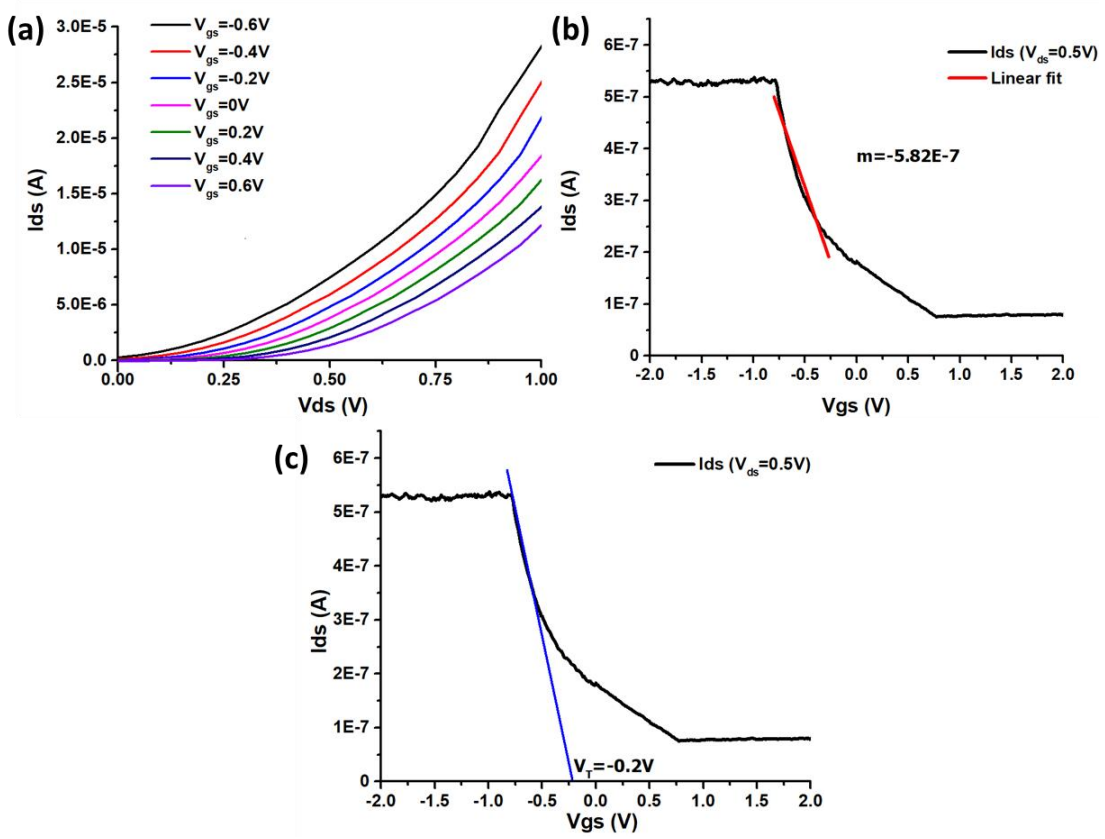


Figure 3.9 (a) Output characteristic (I_{ds} vs. V_{ds}) at various gate-source voltages (V_{gs}), (b and c) transfer characteristics (I_{ds} vs. V_{gs}) at V_{ds} =0.5V, and threshold voltage (V_T) intercept for H-terminated D_4-Si MW with back-gate FET grown for 7 min.

The FET (output/transfer) measurement was performed on a Si MW sample with the same growth conditions but with a growth time of 7 min (radius of 520 nm, 50 µm long). The Si MW FET showed a p-type behavior as shown in Fig. 3.9 with transconductance g_m=582 nS, V_T=-0.2 V, and hole mobility of 428 $cm^2V^{-1}s^{-1}$ at V_{ds}=0.5V. The transconductance and hole mobility obtained for Si MW with a 520 nm radius and 50 µm length was higher than that of Si MW with a radius of 350 nm and length of 30 µm by about 400 times. The effective mobility enhanced by about 400 times which can be attributed to the increased transconductance, Si MW length, and diameter, resulting in an increase in the conductive core and conductivity as deduced from equation

3.10.[110] Additional factors that could affect the mobility are the surface and bulk trap states, as well as contact properties. The surface state acts as trap centers and depletes the MW, reducing the active region and its conductivity.

The threshold voltage V_T is given by equation 3.11, where φ_{gc} is the work function difference between the gate and the channel (Si MW) as shown in eq. 3.12, φ_f is the Fermi level potential, Q_B is depletion charge density, c_{ox} is the oxide capacitance, Q_{ox} is the fixed charge density in the gate oxide. The depletion charge density Q_B is the function of doping density N_A and is given by equation 3.13. Thus, the observed difference in the values of V_T for the Si MW FETs can be attributed to the difference in the size (diameter, channel length), the amount of Cu incorporation and trap states in the Si MW during the VLS growth, and the oxide-interface fixed charge concentration.[111, 112]

$$V_T = \varphi_{gc} - 2\varphi_f - \frac{Q_B}{c_{ox}} - \frac{Q_{ox}}{c_{ox}} \text{.....(3.11)}$$

$$\varphi_{gc} = \varphi_{F\,(MW)} - \varphi_F(Gate) \text{.....(3.12)}$$

$$Q_B = \sqrt{2qN_A\varepsilon_{si} - 2\varphi_f} \text{.....(3.13)}$$

Incorporation of any impurity (metal) into the semiconductor degrades device performance by acting as a recombination center for the charge carriers and reducing the carrier lifetime. The deep-level defects that are closer to the middle of the band gap act as better recombination centers.[113, 114] Cu forms three impurity levels within Si, one close to the middle of the band gap and the other two closer to the valence band, which results in the p-type doping of the Si.[113-115] Cu is reported to form recombination centers in Si like Au, but is comparatively less detrimental for

device performance.[68] Cost and CMOS compatibility of Cu makes it a more favorable choice over Au[68, 113] for the VLS growth of Si MWs. The incorporation of Cu in Si is the most probable cause for the p-type semiconductor behavior observed in the Cu catalyzed Si MW due to the acceptor levels formed within the Si.

3.4 Conclusion

Table 3.1 Si MW mobility extracted from SCLC and back-gated FET measurements

	Mobility ($cm^2V^{-1}s^{-1}$)	Transconductance (nS)	Threshold voltage (V)
SCLC of S1*	1.47		
FET measurement of S1*	1.19	2.87	0.84
FET measurement of S2**	428	582	-0.2

* S1→ Si MW grown at D_4 using 200 sccm H_2 flow rate with a growth time of 5 min

**S2→ Si MW grown at D_4 using 200 sccm H_2 flow rate with a growth time of 7 min

The p-type behavior was observed in the as-grown Si MW, which can be attributed to the acceptor level formed due to the incorporation of the Cu inside the Si MW. The effective mobility obtained for Si MW grown at D_4 via SCLC and FET measurement was of the same order. An increase in the growth time of MW at D_4 under the same condition results in thicker MWs, leading to an increase in the mobility of charge carriers attributed to increased transconductance.

CHAPTER 4: TEMPERATURE-DEPENDENT IV MEASUREMENT OF AS GROWN AND PASSIVATED SI MWs

4.1 Introduction

The size of the 1-D structure plays a vital role in modulating the optoelectronic properties via trap states. The surface states arise due to the unsatisfied or dangling bond at the interface of the Si MW formed during the VLS growth, which undergoes surface reconstruction with oxygen atom from the ambiance. This results in the formation of a native oxide layer of few nm's[116] at the surface, thus leading to the formation of the tail states. The presence of a large density of surface states (Q_{it}) leads to the Fermi level (E_F) pinning, surface band bending, and formation of depletion region across the Si wire surface, which decreases the conductance channel for charge transfer. The width of the depletion layer varies inversely as a function of dopant concentration and diameter of the Si wire structure, which modifies effective radius R_{ND} of as-grown wire compared to R_{PND} as in the case of passivated surface, as shown in Fig. 4.1.

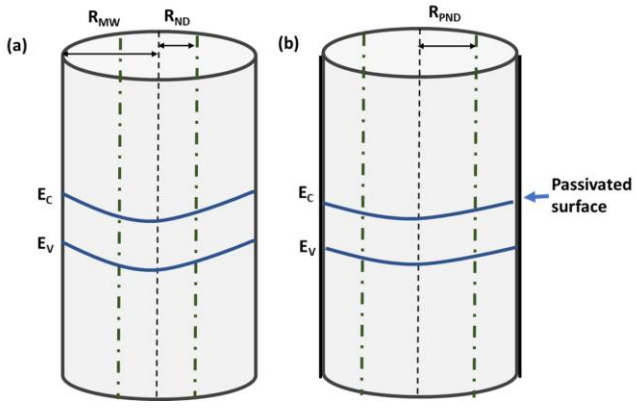


Figure 4.1 Schematic of band bending in (a) as-grown Si wire vs. (b) passivated Si wire.

Several catalysts (Au, Cu, Al, Ni, and Pt) that have been used for the VLS growth of Si wires have been reported in the literature.[114] In this dissertation, we are studying the growth of Si

MW using Cu as the catalyst; more information is provided in Chapter 2. Depending upon the trap levels (i.e., acceptor or donor level) formed by the metal impurity in the Si MW during the VLS growth, the intrinsic Si MW could exhibit p-type or n-type behavior, respectively. The incorporation of Cu in the VLS growth of Si MW can result in three acceptor levels (0.03, 0.16, and 0.32 eV below the Si mid-gap),[114] leading to its p-type behavior. These mid-gap levels, along with the presence of the surface states, quench the optoelectronic performance of the device.

The passivation of the Si MW aids in reducing the surface states by satisfying the dangling bonds at the Si surface, thereby decreasing surface recombination velocity and increasing carrier lifetime. The alkyl chemisorbed films are highly stable to ambient conditions and do not degrade easily with time. There are numerous reports on chemical surface passivation using organic molecules (alkyl groups).[117-119] The bond between organic molecules and Si atoms at the MW surface affects the electrical potential, modulating the work function, surface Fermi level, electron affinity, and band bending.[117, 118]

It is essential to determine the trap levels formed due to the incorporation of the catalyst material and the trap density to quantify the quality of the 1-D structure/device. It is well-reported in the literature[120-125] that temperature-dependent I-V measurement help to determine the trap level and its density. In this chapter, the effect of passivation on the electronic properties of Si MW is determined by extracting trap density and trap energy level via temperature-dependent I-V measurement.

4.2 Experimental method

4.2.1 Surface passivation of Si MWs with methyl (CH_3) group

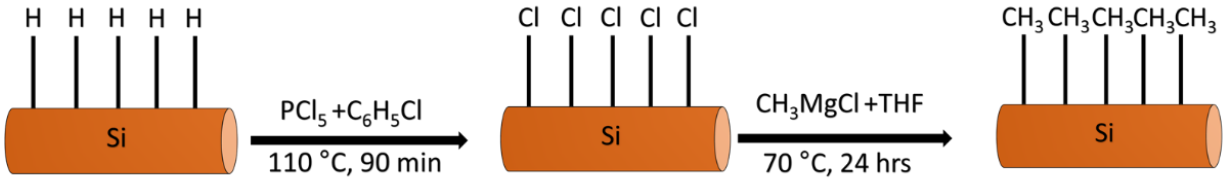


Figure 4.2 Process flow of surface passivation of Si MWs by CH_3-group

The residual Cu and native oxide on the Si MW surface were etched using the procedure as described in section 3.2.1. The chemical treatment of Si MW with BHF etches the native oxide from the Si MW and results in an H-terminated surface. After that, the Si MW array was immersed in a glass vial saturated with phosphorus pentachloride (PCl_5) using dry chlorobenzene (C_6H_5Cl) as a solvent in the glove box. A few grains of benzoyl peroxide were dropped into the solution and used as a radical initiator. The hot plate was dialed up to 110 °C, and the Si MW array dipped in PCl_5 solution was left on the hot plate for about 90 min. This step replaces the H-terminated surface on the Si MW with Cl-atom.

After the chlorination step, the C_6H_5Cl solution was disposed of, and the Si MW array was rinsed with an excess of C_6H_5Cl to get rid of PCl_5 and benzoyl peroxide. This was followed by the alkylation of the Si MW array. This was achieved by immersing the Si MW array in a 3M methyl magnesium chloride (CH_3MgCl) in tetrahydrofuran (THF) at 70 °C for 24 h. After the alkylation reaction, the Si MW array was rinsed with THF, acetone, and methanol. This step replaces the Cl-atom with the CH_3 group.

4.2.2 Substrate preparation and device fabrication

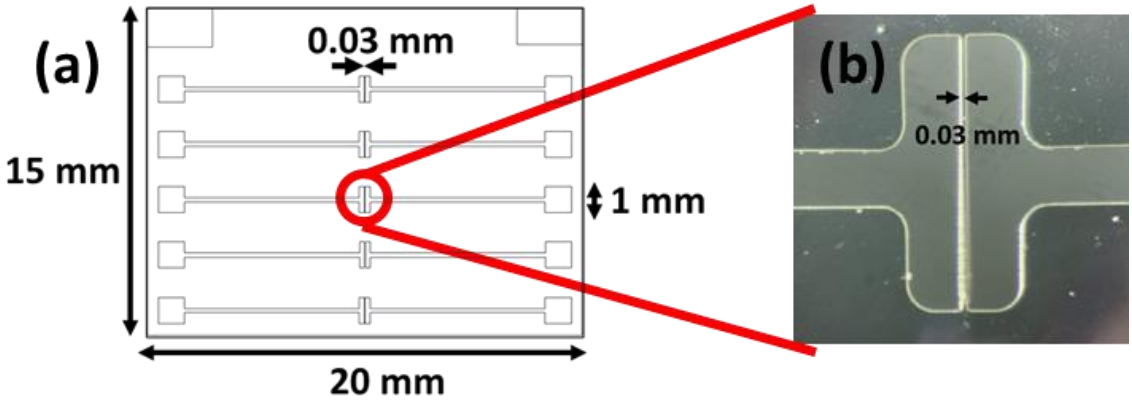


Figure 4.3 (a) Schematic of a single slot of the shadow mask (b) microscopic image of one of the channels of the shadow mask used for temperature-dependent IV measurement.

The prime grade n-Si substrate with 300 nm thermal oxide was cut into 20x15 mm size, cleaned with acetone and isopropyl alcohol, and blow-dried using N_2. The Ossila source-drain shadow mask (Fig. 4.3) was used to deposit 400 nm Ag electrode on the cleaned Si/SiO_2 substrate via thermal evaporation. After the deposition of the Ag electrode, the H-terminated and CH_3-terminated Si MWs were drop-casted on the substrate, as described in section 3.2.1.

4.2.3 Temperature-dependent IV measurement

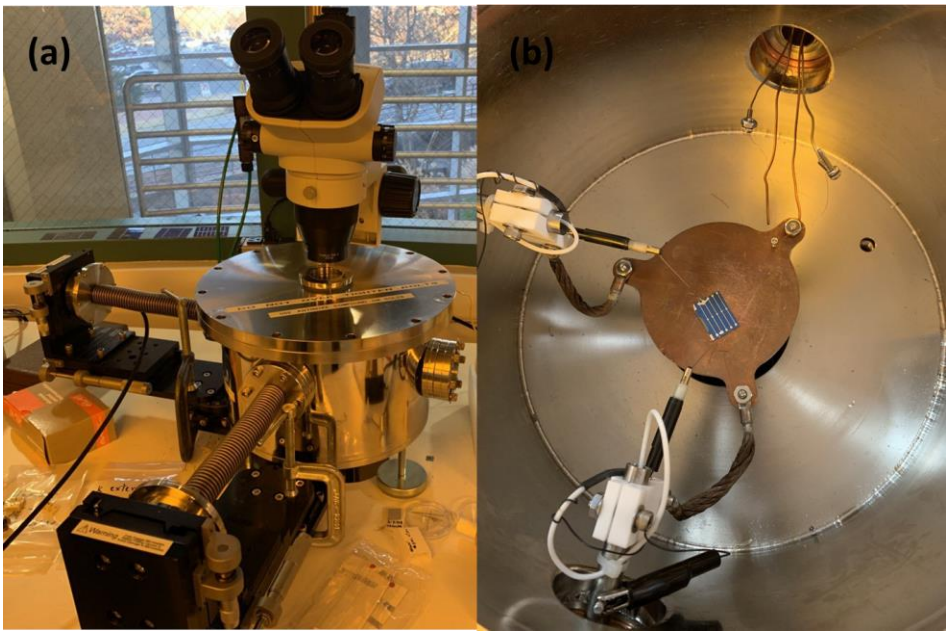


Figure 4.4 Temperature-dependent set-up showing (a) the vacuum chamber and the probe manipulators and (b) probe station.

The temperature-dependent I-V measurement was performed in a vacuum chamber for temperatures ranging from room temperature to 125K. The stage temperature was monitored using a K-type thermocouple and thermocouple meter (Omega DP24T). The two probes were placed at Ag-contact pads across the two ends of the MW, a silver conductive adhesive was applied on the probe and the contact pad to keep the contacts stable during the measurement and was annealed to a temperature of 100 °C for about 15 min to make sure that the silver paste is dry. The system was pumped down to 50 mTorr using a roughing pump before turning on the water supply and He cryostat (Advanced research systems). The temperature of the setup was monitored and controlled using Lakeshore 331 temperature controller.

4.3 Results and discussion

The distribution of trap density P_t (E) around the relative energy level (E) from the top of the valence band is given by equation 4.1[126], where H_t is the density of traps and E_t is the trap energy level. From equation 4.1, we can see that the trap level is distributed exponentially and not localized. The current density expression for the SCLC limited current is given by equation 4.2, where $l=T_c/T$; T is the temperature at which IV measurement is done, and T_c is the characteristic trap temperature. The value of l+1 is the slope of log J vs. log V curve in the SCLC regime, which increases as the temperature decreases, and the slope corresponds to the E_t below the conduction band.

$$P_t(E) = \frac{H_t}{E_t} exp\left(\frac{-E}{E_t}\right) \text{..... 4.1}$$

$$J \propto V^{l+1} \text{.....4.2}$$

$$V_C = \frac{qH_t L^2}{2\varepsilon_s \varepsilon_0} \text{.....4.3}$$

The trap density (H_t) was measured using the equation 4.3 proposed by Kumar et al.[127], where V_c is crossover voltage, ε_0 is the permittivity of free space, ε_s is the dielectric constant of material, q is the electronic charge, L is the Si MW length.

V_c was determined by finding the point of intersection obtained by extrapolating logI-logV plot at various temperatures. The H-terminated and CH_3-terminated Si MWs were investigated by the two-probe temperature-dependent measurement using Keithley 4200 semiconductor parameter analyzer.

4.3.1 Temperature-dependent IV measurement of H-terminated D_4-Si MW

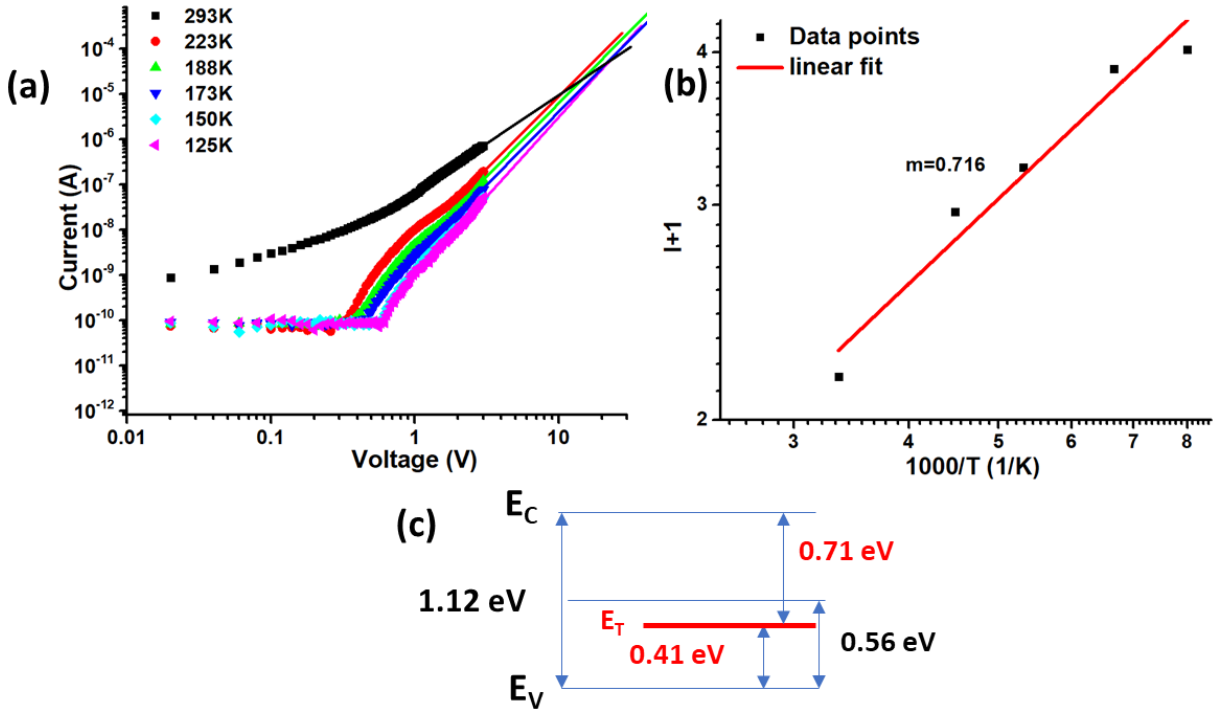


Figure 4.5 (a) log I -log V plot (b) l+1 as a function of the inverse of temperature, and (c) corresponding energy level diagram with the trap energy level of H-terminated D_4 Si MW.

The behavior of free charge (thermal) and injected (SCLC) carriers was studied at various temperatures ranging from 298K to 125K to understand the impact of Cu incorporation on trap levels. The IV measurement of H-terminated Si MW (grown at D_4 with length of 27.1 µm) at room temperature showed linear dependence of current at low voltage. The current in this region corresponds to the thermally generated carriers.[120] SCLC conduction mechanism was observed at high voltage mainly due to the dominance of injected carriers over the free carriers. Current and voltage followed a power dependence ($I \alpha V^{\alpha}$), where $\alpha > 2$ suggesting trap-assisted SCLC at room temperature.

The decrease in the stage temperature below room temperature showed a substantial reduction in the conduction current at a low voltage due to the partial freezing of charge carriers in the trap states and/or a decrease in the thermally generated charges.[128] Whereas, at higher voltage, no substantial decrease in current was observed, as shown in Fig. 4.5(a). The I-V curves were extrapolated to find the crossover voltage V_C from their point of intersection, and it was found that the curve intersects at three different points, viz.10.52 V, 13.7 V, and 21.62 V. A range of crossover voltage region (~1.6-3V) has been reported by Simpkins et al.[129] The highest V_c was used by them to calculate the trap state density since the broader crossover region does not have a significant effect on the trap state density owing to its linear dependence on V_C. Equation 4.3 was used to determine the trap state density and was found to be in the range of $1.85\text{-}3.81\text{x}10^{13}$ cm^{3-} corresponding to the multiple V_C's.[130]

The log-log plot of (l+1) and 1000/T was plotted and linearly fitted to determine the trap energy level where (l+1) is the slope of the SCLC region at a given temperature, as shown in Fig. 4.5 (b). The slope of the curve represents the trap energy level below the conduction band, which is found to be 0.71 eV, as shown in Fig. 4.5 (c). The trap states exist between the Fermi level (E_F) and the valence band, 0.41 eV above the valence band, and have an exponential distribution as given by equation 4.1.

4.3.2 Temperature-dependent IV measurement of CH_3-terminated D_4-Si MW

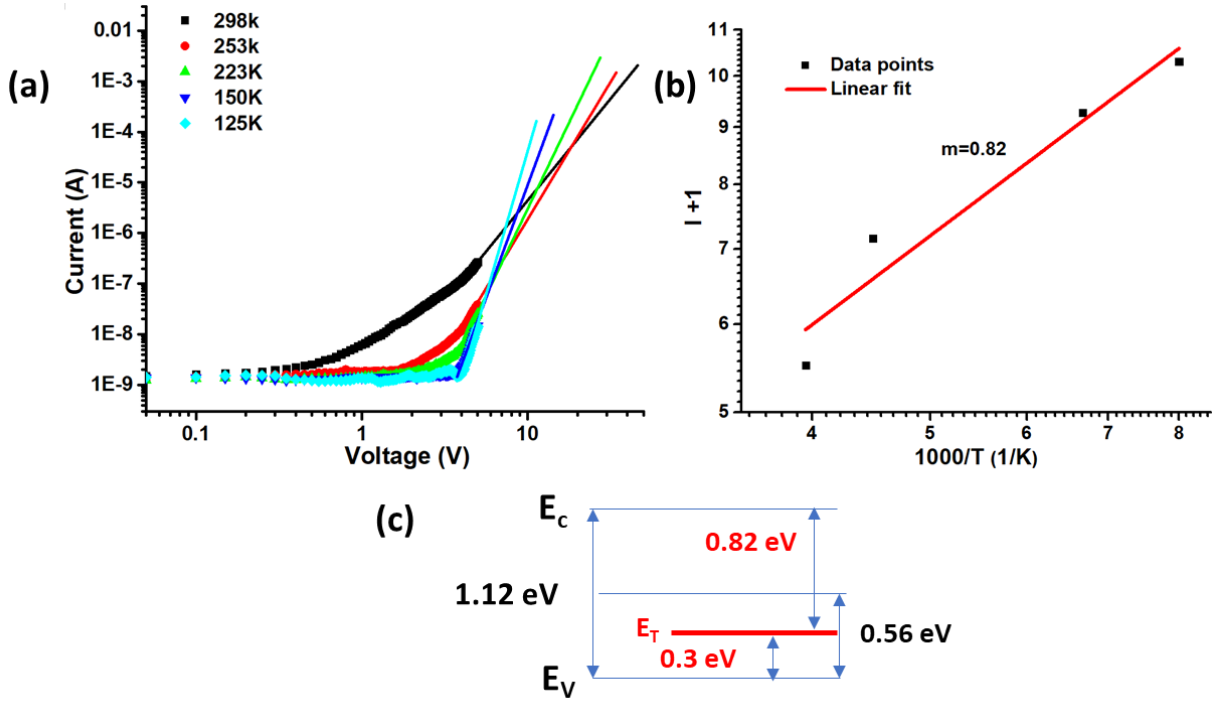


Figure 4.6 (a) log I -log V plot (b) l+1 as a function of the inverse of temperature, and (c) corresponding energy level diagram with the trap energy level of CH_3-terminated D_4 Si MW.

Next, we studied the effect of passivation on trap density and trap energy level for the Si MWs (grown at D_4 with length of 31.7 µm). The Si MW was passivated with the CH_3 group using the procedure mentioned in section 4.2.1. The CH_3 terminated Si MW showed a similar IV response at a lower temperature as observed in H-terminated Si MWs, with a significant change in current at low voltage as compared to higher voltage region on lowering the temperature, as shown in Fig. 4.6 (a). The CH_3-terminated Si MW exhibited three V_C's viz. 5.71V, 11.5V, and 18.6 V, as shown in Fig. 4.6(a), and trap density in the range of 1.01-3.28x10^{13} cm^{-3}. The slope of the l+1 vs. 1000/T at the log-log scale was found to be 0.82 eV, thus, the trap level was 0.30 eV above the valence band, as shown in Fig. 4.6 (c). The observed decrease in the trap state density

can be attributed to the decreased surface states due to the surface passivation of the MW with the CH_3 group.

4.3.3 Temperature-dependent IV measurement of CH_3-terminated D_5-Si MW

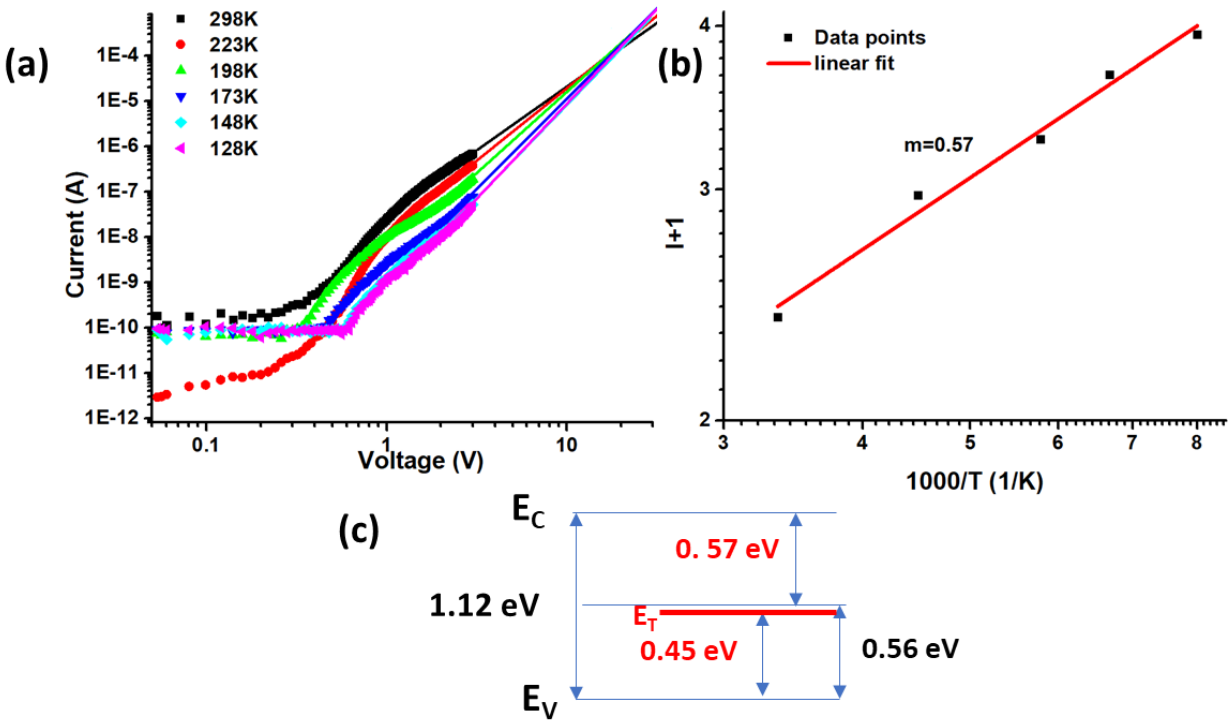


Figure 4.7 (a) log I -log V plot (b) l+1 as a function of an inverse of temperature, and (c) corresponding energy level diagram with the trap energy level of CH_3-terminated D_5-Si MW.

Lastly, the two-probe temperature-dependent measurement was performed on CH_3-terminated D_5-Si MW (30 µm long) under the same conditions. The lowering of temperature had no significant effect on current at lower (ohmic) /higher (SCLC) current, which might be due to better passivation of MW surface as shown in Fig. 4.7 (a). The CH_3-terminated Si MW grown at D_5 exhibited three V_C viz. 5.71 V, 11.5 V, and 18.6 V, as shown in Fig. 4.7(a), and trap density in the range of 0.172-3.3x10^{13} cm^{-3}. The slope of the l+1 vs. 1000/T at the log-log scale was found to be 0.57 eV, thus, the trap level was 0.45 eV above the valence band, as shown in Fig. 4.7 (c).

The trap state density for the CH_3-terminated D_5-Si MW was lower than that of CH_3-terminated D_4-Si MW, and the trap energy level of CH_3-terminated D_5-Si MW was closer to the mid-gap level than in CH_3-terminated D_4-Si MW. This can be explained due to the higher incorporation of Cu in the Si MW attributed to a higher growth rate in the case of D_4 as compared to Si MWs grown at D_5. With higher Cu incorporation, the trap state density will increase, and the corresponding trap energy level will move closer to the valance band due to higher incorporation of Cu will make the Si MW more P-type.

In H-terminated Si MW, the contribution towards trap state density would be from the surface states at the surface and the traps in the bulk of the Si MW formed by the incorporation of Cu during growth. In CH_3-terminated Si MW, if we consider 100% coverage of the surface by methyl group, the contribution towards trap state density would be from the bulk only.

Table 4.1 Cross-over voltages and trap densities extracted from temperature-dependent I-V measurements

	V_{C1} (V)	V_{C2} (V)	V_{C3} (V)	$H_{T1}(cm^{-3})$	$H_{T2}(cm^{-3})$	$H_{T3}(cm^{-3})$
H-terminated D_4 Si MW	10.52	13.7	21.62	$1.85x10^{13}$	$2.41x10^{13}$	$3.81\ x10^{13}$
CH_3-terminated D_4 Si MW	5.71	11.5	18.6	$1.01\ x10^{13}$	$2.03\ x10^{13}$	$3.28\ x10^{13}$
CH_3-terminated D_5 Si MW	0.98	10.75	18.76	$1.72\ x10^{12}$	$1.89\ x10^{13}$	$3.30\ x10^{13}$

4.4 Conclusion

The passivation of Si MW by the CH_3 group resulted in a decrease in surface states, thus resulting in lower trap density. The Cu incorporation during the VLS growth of Si MW results in

the formation of trap states (acceptor level), thereby supporting the p-type behavior observed for the intrinsic Si MW in FET measurement in Chapter 3. Multiple crossover voltages were observed in the low-temperature IV measurement of all the Si MWs, thus showing a range of trap state densities. CH_3-terminated D_5-Si MW showed the lowest V_c and H_t due to the lower incorporation of Cu during the Si MW growth, as seen in Table 4.1. The difference in Cu incorporation during the VLS growth of Si MW at different growth positions due to the difference in growth rate is suggested to affect the trap state density and trap energy level.

CHAPTER 5: SI MW BASED PHOTODETECTOR

5.1 Introduction

The near-infrared (NIR) region is of particular interest as it finds application in spectroscopy, bio-chemical sensing, night surveillance, image sensing, and optical communication.[44-48] Infrared photodetectors are typically made up of expensive materials like InGaAs, GaAs, or Si-Ge, thus adding up to the cost per pixel for NIR imaging.[45, 131-134] GaAs photodetectors became the dominant component in short distance signal communication employing 800-850 nm wavelength due to the wide availability of GaAs laser diodes, thereby making GaAs a choice of material for high performance monolithic optoelectronic receivers (that include transistors and photodetectors) in this wavelength regime.[132, 133]

Si is a promising alternative for optoelectronic application in UV-VIS and short NIR region owing to its cost-effectiveness as compared to GaAs, as well as easy compatibility with very large-scale integration (VLSI) technology. However, the large penetration depth of Si corresponding to its bandgap compared to GaAs limits its application for high-speed detection.[132, 133] The charge carriers in Si are generated farther away from the depletion region as compared to GaAs for a given incident wavelength owing to the differences in the corresponding absorption coefficient and penetration depth. In the case of Si, the for low NIR region (~900 nm), absorption depth is of the order of ~10 μm as compared to GaAs with the absorption of few micrometers,[135] hence, the diffusion of the carriers (as compared to drift) results in longer transit time, resulting in slower response time in the case of Si.

Research is in progress to improve device performance of Si-based photodetectors by improving the bandwidth, responsivity, detectivity, gain, external quantum efficiency (EQE), and increasing the speed of detection such that it can detect weak optical signals with a fast response time with minimum power consumption.[44, 49] Speed of detection can be enhanced by reducing the active layer thickness but at the expense of sensitivity.[133, 53, 132] This problem can be addressed by applying an antireflective layer or by using a vertical array of Si wires.[133, 136] On the other hand, the transit time difference between electrons and holes results in a gain in photoconductors but at the expense of bandwidth.[46]

There are different types of photodetectors like photodiodes, phototransistors, and photoconductors, and out of these, photoconductors are the simplest photodetectors.[49, 50] Photodetectors are also classified according to the spectral response window into a broadband or narrowband photodetectors.[45] Si wire-based photodetectors like p-n junction photodiodes, p-i-n based avalanche photodiodes[20], junctionless MOSFET phototransistors[53, 54], and junctionless MSM photodetectors have been reported with high photoconductivity gain and responsivity. Dhyani et al.[54] reported the peak responsivity of 0.8A/W with the illumination of 750 nm in a single nanowire Si junctionless phototransistor in Si NW MOSFET with gate and drain voltage of |0.35 V|. Change in the current of the order of 10^3 on illumination at a low optical power of about 1 nW suggests high sensitivity of the Si NW phototransistor. Additionally, a rise/fall time of 100/120 μs was reported using a laser source of 660 nm wavelength. On the other hand, Das et al.[53] reported the detection of very low optical signal of the order of picowatts in a Si NW phototransistor configuration with a internal gain of up to 35 at 860 nm, and with responsivity ranging from 0.04-0.18 A/W at 710 nm incident light of power ranging from nW to μW at the gate

and drain voltage of ~|0.35 V|. This suggests Si NW phototransistor to be able to detect weak optical signals corresponding to 700-860 nm with a high internal gain and exhibit a response time in the order of 0.1 ms using a laser source of 660 nm. Flexible photodetector Si NW with the current enhancement of 24.4 on illumination with red light has been reported by Do Hoon et al. without any significant deterioration of device performance over 10,000 cycles.[137]

5.2 Experimental method

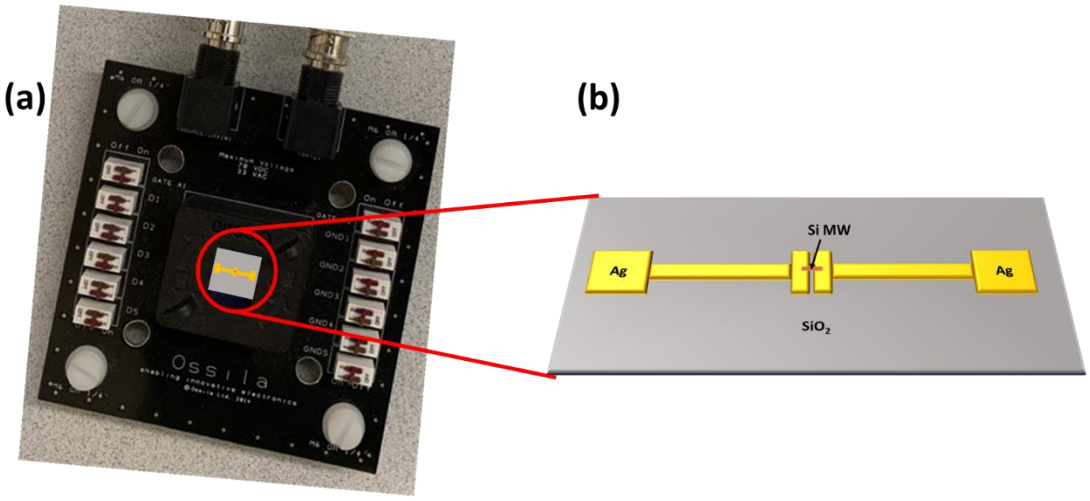


Figure 5.1 (a) Ossila test board used for photodetector characterization (b) Schematic of the Si MW photodetector.

The Si MW grown at the D_4 and D_5 position using Ar: H_2 (10:200) were methylated and used to fabricate M-S-M Si MW photodetector. The Si MW photodetector was fabricated by drop-casting the H-terminated and CH_3-terminated Si MW on the pre-cleaned Si/SiO_2 substrate with thermally evaporated Au/Ag electrodes of 400 nm thickness using the same procedure as mentioned in section 4.2.2.1. The Ossila test board, shown in Fig. 5.1 (a), was used to hold and characterize the Si MW photodetector. The power density of the incident beam was measured

using the standard Si photodetector (Newport) at different wavelengths and slit widths. The incident power density was varied from P_1=1.24x10^{-4}, P_2=1.5x10^{-4}, and P_3= 1.76x10^{-4} W/cm^2 by varying the slit width from 20 nm to 15 nm 10 nm at 900 nm of incident light using the monochromator (RF 5301PC spectrofluorophotometer). The Si MW FET was placed in the optical window slot present in the test board, as shown in Fig. 5.1 (a). The Si MW photodetector was connected to Keithley 2602A sourcemeter via the source/drain connectors in the test board. The light of a specific wavelength was made incident through the optical window in the test board onto the Si MW photodetector. Dark and photo-illuminated two-probe measurement was performed using a monochromator with variable power intensity at a wavelength ranging from (400-900 nm). The temporal response of the Si MW photodetector was measured at a specific wavelength and incident power density.

5.3 Results and discussion

The performance of the photodetector was examined in terms of four figure of merits as mentioned below:

1. Responsivity: Responsivity (R_λ) is defined as the ratio between the photocurrent (I_{ph}) flowing in the photodetector per unit of the incident optical power P_{in} at a particular wavelength (λ).

$$R_\lambda = \frac{I_{Ph}}{P_{in}} = \frac{I_{Light} - I_{Dark}}{P_{in}} \text{ …….(5.1)}$$

2. External quantum efficiency: External quantum efficiency (EQE) is defined as the ratio of the output current to the number of photons for a given incident wavelength where h is Planck's constant, c is the speed of light, and λ is the wavelength of light.

$$EQE = R_\lambda \frac{hc}{q\lambda} \text{ …….(5.2)}$$

3. Gain: Gain (G) represents number of charge carriers generated by a single incident photon, and depends on photocurrent (I_{ph}), incident power (P_{laser}, MW area (A), absorption co-efficient (α), MW diameter (d),

$$G = \frac{{}^{I_{ph}}/_{e}}{\frac{P_{laser}A(1-e^{-\alpha d})}{h\nu}} \text{……..(5.3)}$$

3. Detectivity: Detectivity (D) represents the ability of a detector to detect weak optical signals, which depends on the area of device (A), current (I), gain (G), and responsivity (R_λ). Here, all measurements were done in dark.

$$D = \frac{A^{1/2}R_\lambda}{(4qIG)^{1/2}} \text{ …….(5.4)}$$

4. Ton/Toff: The time required for a photocurrent to increase from 10% to 90% and decrease current from 90% to 10% is known as T_{on} and T_{off}, respectively.

As described in section 4.3, the passivation of Si MW with CH_3 group helps in the reduction in the trap states of the surface, which may help to improve the figure of merit of MW-based photodetector.

5.3.1 H-terminated Si MW photodetector characterization using white light (single wire vs. Si wire mesh)

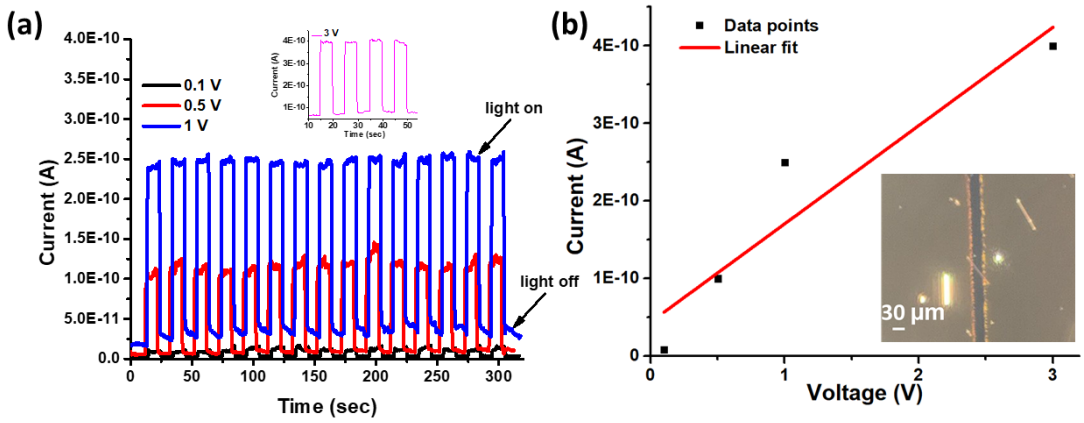


Figure 5.2(a) Time response at 0.1V, 0.5V, 1V, and 3V (inset) (b) Linear dependence of photogenerated current with applied voltage for H-terminated-D_4-Si MW under the illumination of 100 mW/cm^2 incident white light with the microscopic image of Si MW drop-casted on Au electrodes.

The H-terminated Si MWs were drop-casted on the pre-patterned Au electrodes (from Ossila), and its temporal response of H-terminated Si MW was measured by shining the white light from the Newport arc lamp. The current is enhanced by about an order of magnitude when illuminated by the white light of 100 mW/cm^2 power density and an applied bias of 1 V, whereas the current is enhanced by a factor of 2 when an applied bias of 0.1 V was applied. The Si MW photodetector response exhibited fully recyclable behavior when the light was turned on/off over several cycles, as shown in Fig. 5.2 (a). An increase in photocurrent with the increase in voltage has been shown with a linear fitting, as seen in Fig. 5.2 (b).

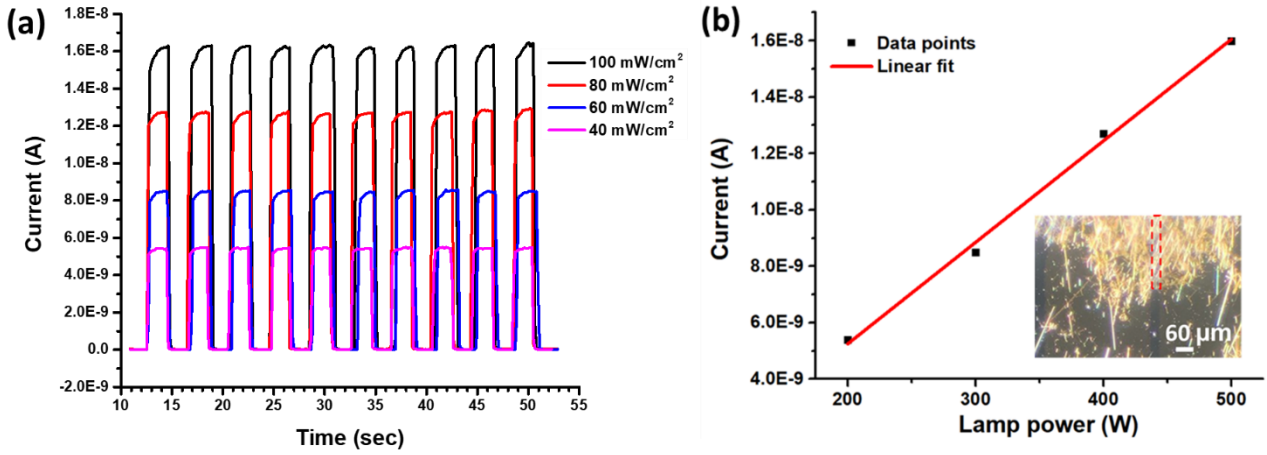


Figure 5.3(a) Time response of Si MW mesh photodetector at 3V (b) Linear dependence of photogenerated current for H-terminated-D_4-Si MW under the illumination of 40, 60, 80, 100 mW cm^{-2} incident white light, respectively, with the microscopic image of Si MW mesh drop-casted on Au electrodes.

The single Si MW device was compared to that with multiple MWs. Considering that only a single layer of Si MW mesh is in contact with the electrodes at the bottom, the effective area in the case of Si MW mesh is about 3 orders higher than for a single Si MW. The photogenerated current increased by about an order of 2, when illuminated by the white light of 100 mW/cm^2 incident power density and 3V applied bias in Si MW mesh photodetector as compared to single Si MW photodetector as seen in Fig. 5.3 (a) and inset of Fig. 5.2 (a). Additionally, a linear increase in photogenerated current with incident lamp power has been observed, as seen in Fig. 5.3 (b), with a maximum photocurrent of about 1.6 x 10^{-8} A when illuminated with white light under 3V applied bias and 100 mW/cm^2 incident power density as seen in Fig. 5.3 (b).

5.3.2 CH_3-terminated-D_4-Si MW photodetector characterization

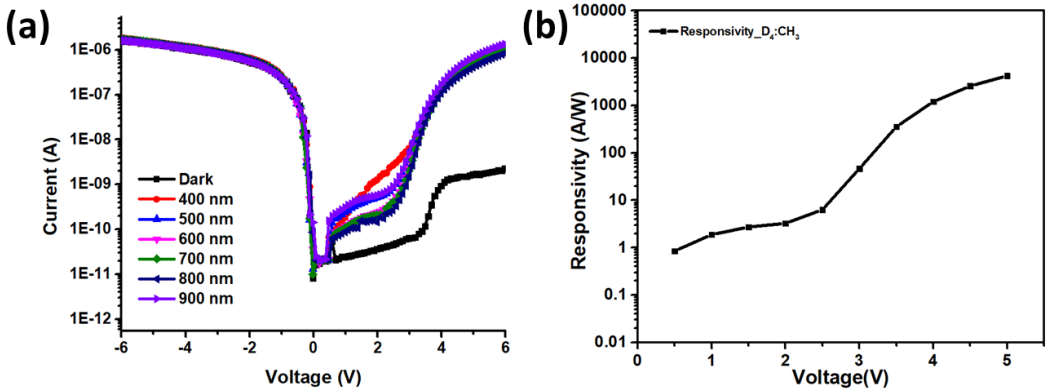


Figure 5.4 (a) I–V characteristics under dark and illumination at different wavelengths (b) responsivity variation with applied bias voltage for CH_3 terminated D_4 -Si MW photodetector.

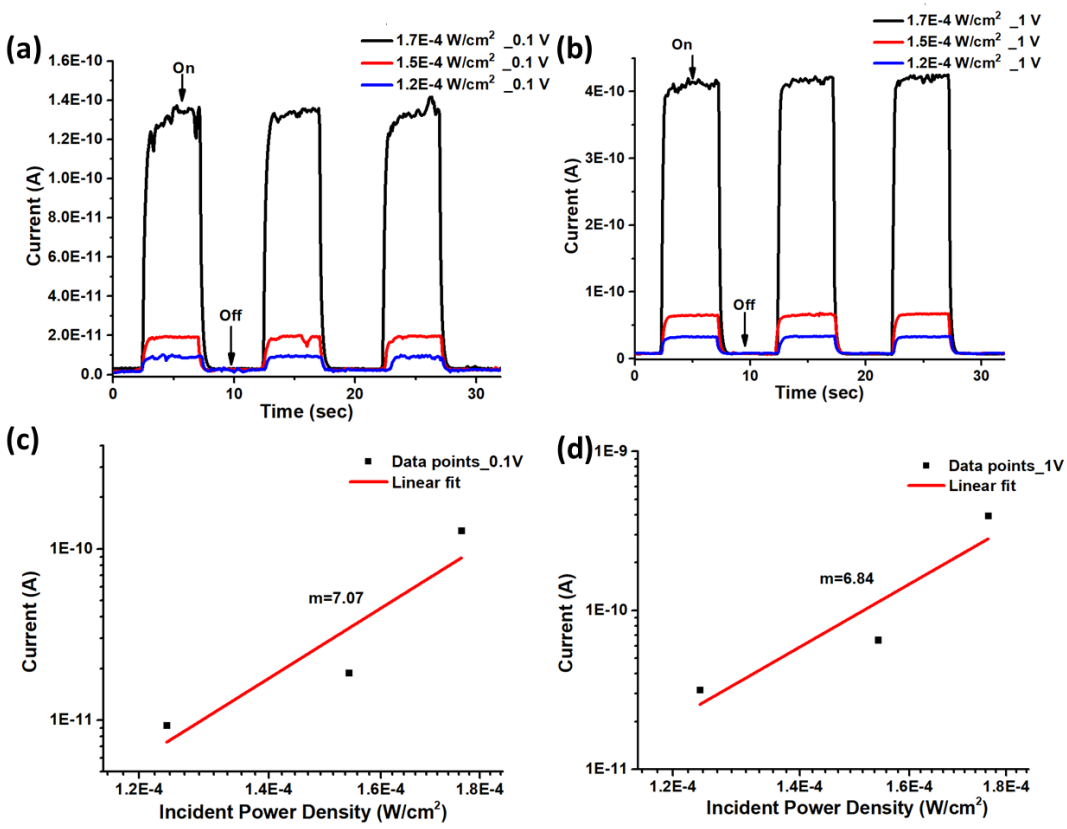


Figure 5.5 (a) Time response at 0.1V and (b)1V for CH_3 terminated-D_4-Si MW under the illumination of different power at 900 nm wavelength, and photocurrent vs. incident power curve for (c) 0.1V (d) 1V applied voltage.*

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The spectral response of CH_3-Si MW photodetector fabricated using Si MWs grown at D_4 exhibited one-sided photoresponse in the range of wavelength from 400-900 nm as shown in Fig. 5.4 (a) and Appendix A5 (a). The time response of CH_3 terminated-D_4-Si MW photodetector under the illumination of 900 nm wavelength at three different incident power densities (P1, P2, and P3) at the applied voltage of 0.1 V and 1V, respectively, is shown in Fig. 5.5 (a-b). The photocurrent was observed to increase linearly with the increase in power density of incident light, as shown in Fig. 5.5 (c-d), signifying an increase in the number of photogenerated charge carriers with an increase in the incident power of light. The responsivity of 0.724 A/W, a gain of 69, detectivity of $6x10^{10}$ J, and EQE of 100% were obtained at a low voltage of 0.1V using a 900 nm* incident wavelength of $1.76x10^{-4}$ W/cm^2 power density. Whereas, at 1V, the responsivity of 2.242 A/W, a gain of 166, detectivity of $3.31x10^{10}$ J, and EQE of 309% were obtained under the illumination of 900 nm* incident wavelength with the power density of $1.76x10^{-4}$ W/cm^2. Additionally, the photodetector exhibited a faster switching time with an increase in the applied voltage from 0.1 to 1V with a reduction in the switching time T_{on} /T_{off} from 0.475 s /0.444 s to 0.216 s /0.231 s, respectively, as shown in Table 5.1, and Appendix A6-A7, respectively.

We could not eliminate some of the unwanted scattered light within the spectrofluorophotometer while using 900 nm incident light, therefore, some of the photodetector response likely resulted in a higher number in higher measured responsivity, gain, detectivity, and EQE.

Table 5.1 Figure of merit of CH_3 terminated-D_4-Si MW under the illumination of 900 nm wavelength at an applied voltage of 0.1 and 1 V*

V	Power (W/cm^2)	Ton (s)	Toff (s)	R (A/W)	D (J)	EQE (%)
0.1V	$1.24x10^{-4}$	0.698	0.416	0.068	$5.84x10^{9}$	9
0.1V	$1.54x10^{-4}$	0.503	0.423	0.113	$2.28x10^{10}$	15
0.1V	$1.76x10^{-4}$	0.475	0.444	0.724	$6x10^{10}$	100
1V	$1.24x10^{-4}$	0.304	0.388	0.197	$9.12x10^{9}$	27
1V	$1.54x10^{-4}$	0.399	0.343	0.379	$1.41x10^{10}$	52
1V	$1.76x10^{-4}$	0.216	0.231	2.242	$3.31x10^{10}$	309

5.3.3 CH_3-terminated-D_5-Si MW photodetector characterization

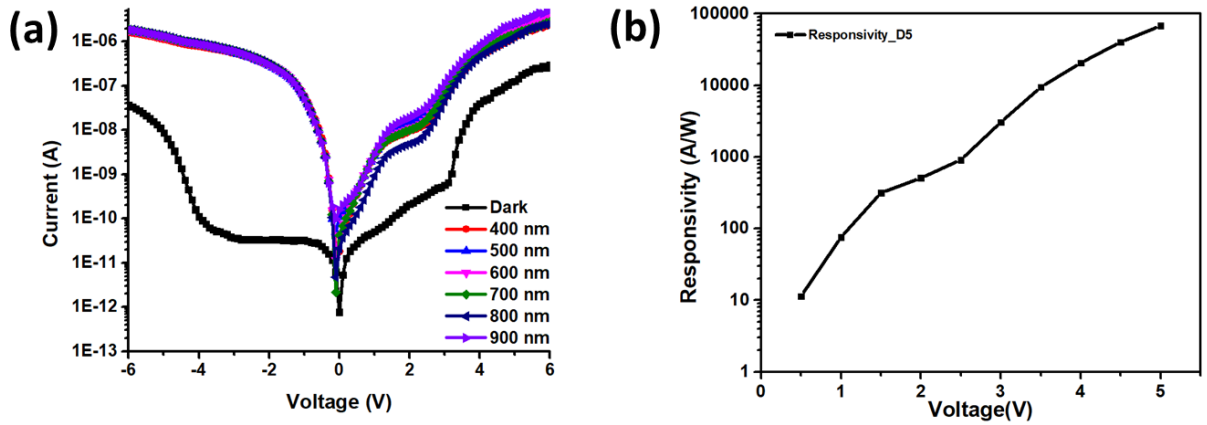

Figure 5.6 (a) I–V characteristics under dark and illumination at different wavelengths (b) responsivity variation with applied bias voltage for CH_3-terminated-D_5-Si MW photodetector.

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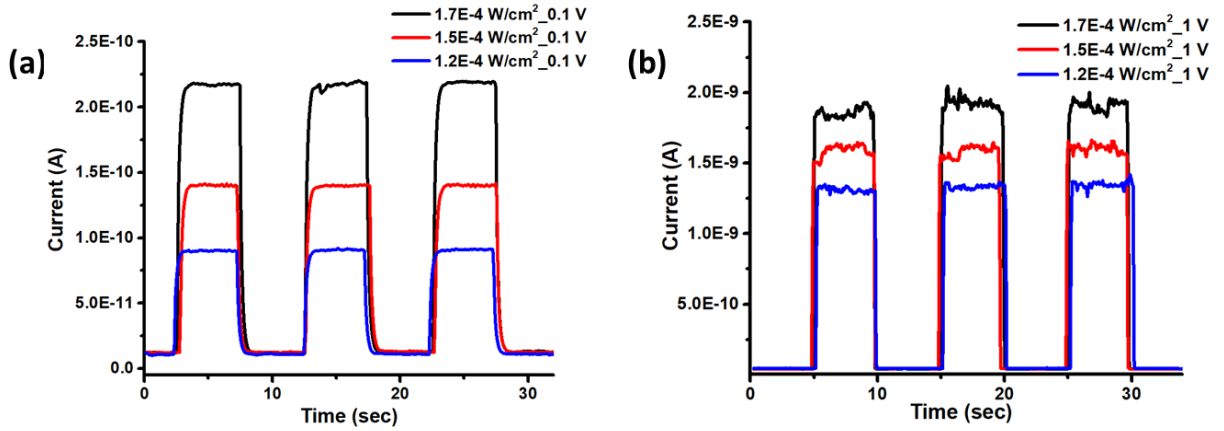

Figure 5.7 (a) Time response at 0.1V and (b)1V for CH_3-terminated-D_5-Si MW photodetector under the illumination of different power at 900 nm wavelength.*

CH_3-terminated-D_5-Si MW photodetector fabricated using Si MWs grown at D_5 was characterized in similar conditions as done for CH_3-terminated-D_4-Si MW photodetector to study the influence of growth conditions on the intrinsic properties and optoelectronic properties of the MW. CH_3-terminated-D_5-Si MW exhibits photoresponse on both sides of the voltage, as shown in Fig. 5.5(a). The responsivity and detectivity demonstrated a similar trend with an increase in the applied voltage as seen in the case of CH_3-terminated-D_4-Si MW photodetector but had significant enhancement in CH_3-terminated-D_5-Si MW photoresponse, as shown in Fig. 5.6 (b) and Appendix A5(b). The time response of CH_3-terminated-D_5-Si MW photodetector exhibits an increase in the photocurrent with increased incident power and applied voltage due to the creation/collection of more charge carriers. The extracted responsivity, gain, detectivity, T_{on}/T_{off}, and EQE value for CH_3-terminated-D_5-Si MW photodetector were 5.47 A/W, 1.96×10^3, 2×10^{10} J, 7.55×10^2% at 0.1 V, and 75.98 A/W, 2.56×10^4, 3.86×10^{10} J, 6.66×10^3 % at 1V, respectively (Appendix A8-A9). The response time also improved from 0.36 s /0.33 s to 0.130 s /0.108 s when applied bias was increased

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from 0.1 V to 1 V, as shown in Table 5.1 and appendix (A4-5). This significant enhancement in photoresponse parameters for CH_3-terminated-D_5-Si MW photodetector as compared to of CH_3-terminated-D_4-Si MW photodetector as shown in Fig. 5.8 can be explained in terms of trap energy level and lower trap state density as deduced in chapter 4.

Table 5.2 Figure of merit of CH_3-terminated-D_5-Si MW photodetector under the illumination of 900 nm wavelength at an applied voltage of 0.1 and 1 V.*

V	Power (W/cm^2)	Ton (s)	Toff (s)	R (A/W)	D (J)	EQE (%)
0.1V	$1.24x10^{-4}$	0.308	0.363	3.05	$1.48x10^{10}$	421
0.1V	$1.54x10^{-4}$	0.36	0.37	3.86	$1.65x10^{10}$	534
0.1V	$1.76x10^{-4}$	0.36	0.33	5.47	$2x10^{10}$	755
1V	$1.24x10^{-4}$	0.098	0.067	49.82	$3.15x10^{10}$	6878
1V	$1.54x10^{-4}$	0.112	0.063	43.95	$2.76x10^{10}$	6067
1V	$1.76x10^{-4}$	0.129	0.108	75.98	$3.86x10^{10}$	6661

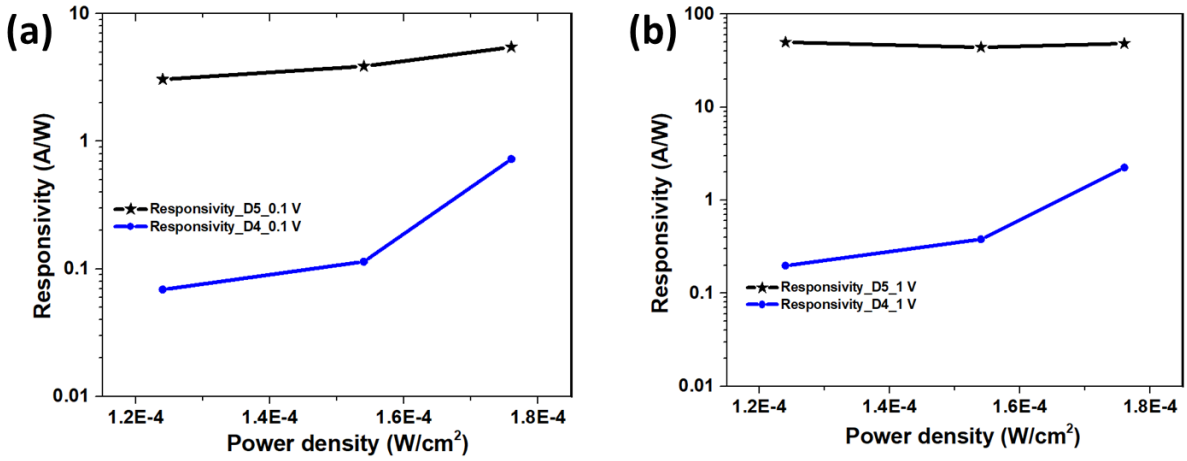

Figure 5.8 Responsivity comparison for CH_3-terminated-D_4-Si MW and CH_3-terminated-D_5-Si MW, respectively, at 900 nm and an applied bias of (a) 0.1V and (b) 1V.*

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5.4 Conclusion

The CH_3-terminated-D_5-Si MW photodetector response time was observed to be two times faster, with enhancement in responsivity and gain by a factor of 30 and 150, respectively, whereas detectivity was almost the same, i.e., in the order of 10^{10} J, as compared to CH_3-terminated-D_4-Si MW photodetector on illumination with 900 nm* light with a power density of 1.76×10^{-4} W/cm^2 at 1 V. The responsivity, gain, detectivity, and EQE of CH_3-terminated-D_5-Si MW photodetector obtained on illumination with the lowest incident power density and applied voltage of 1.24×10^{-4} W/cm^2 and 0.1V was observed to be 3.05 A/W, 1.48×10^{10} J, and 421%, respectively. The rise and fall time were observed to be 0.308 s /0.363 s. The better figure of merits (responsivity, detected, EQE, and T_{on}/T_{off}) in the case of CH_3-terminated-D_5-Si MW is observed since the trap state density is lower in it as compared to CH_3-terminated-D_4-Si MW.

CHAPTER 6: SUMMARY

6.1 Conclusion

Si MW diameter and growth rate can be tuned by optimizing various growth parameters like Cu thickness, gas flow rates, and growth position. An exponential decrease of the axial growth rate of Si MW, similar to that reported for thin film growth, due to the depletion of the precursor as we move downstream suggests mass transport of the precursor is the rate-limiting step and has been reported for the first time in a wire configuration.

Additionally, electronic transport properties of Si MW have been reported with emphasis on the effect of growth parameters and surface chemistry on trap states and device performance. Effect of growth rate/ growth position on trap state density and trap energy level and photoresponse has been studied, along with the effect of surface passivation on trap state density.

FET device characterization suggests Si MW exhibits p-type behavior attributed to unintentional doping by Cu catalyst. The corresponding effective mobility extracted is in the order of ~ 1 $cm^2V^{-1}s^{-1}$, similar to that extracted from the SCLC mechanism using MG law. The temperature-dependent IV measurement was done to extract the trap state density and trap energy level for H-terminated as well as CH_3-terminated Si MW. The temperature-dependent IV measurement corroborates the p-type behavior of Si MW obtained using FET characterization. This suggests that Cu forms acceptor levels, and depending upon the amount of Cu incorporation, the trap state density and trap energy level are altered, which in turn affects the optoelectronic properties of the Si MW device, as seen in Chapter 5.

The photoresponse of CH_3-terminated Si MW was studied for the Si MWs grown at D_4 and D_5 and exhibited a broadband spectral response from 400-900 nm. The CH_3-terminated D_5-Si MW photodetector shows optimum photoresponse at a lower incident power density of $1.24x10^4$ A/W and voltage of 0.1 V with a responsivity of 3.05 A/W with EQE of 421%, and response time in ~0.3 s, in NIR region (900 nm).

The fast response time with high responsivity, detectivity, and high EQE observed under illumination with 900 nm light and low voltage bias, along with its broadband photodetection as observed in the spectral response from 400-900 nm region, makes it a promising candidate for various device applications with low power consumption. The spectral window in VIS- short NIR (400-1050 nm) region finds application in food quality monitoring[47], bio-molecule detection (e.g., DNA molecule)[138], whereas the wavelength in red/short NIR (700-1000 nm) region finds application in biomedical imaging and non-invasive blood glucose monitoring.[45, 48]

6.2 Outlook

Some of the interesting features of Si, like wide availability, tuning of dopant type and concentration during the growth, CMOS compatibility, and excellent passivation by thermal oxide, make it a promising candidate for future electronics with the potential to provide high-speed device performance and low power consumption with the miniaturization. The high aspect ratio of Si wires provides a higher surface area for any sensing application and improves the speed of the device by decreasing the transit time.

Si wires find applications in almost every field from defense, bio-medical applications, photovoltaic applications, food quality control, image and biochemical sensing, and optical

communications. Improving the device performance by optimizing growth conditions to achieve a high-quality Si wire with minimum defects and finding an alternate scalable method to fabricate the Si wire-based device with minimum device degradation with considerations of device limitations and performance would be required before incorporating it in the industrial scale.

The spectral response window of Si has been expanded to up to 2 μm by using microstructured Si and incorporating Au and Pd grating. Huang et al.[46] reported responsivity of 0.09 A/W for microstructured Si, using 1550 nm wavelength. On the other hand, Tanzid et al. reported responsivity >1A/W at 275 mV, using 1375 by incorporating Au and Pd grating on Si, which is higher than the commercially reported values for InGaAs based detector.[134] Thus, with the possibility of expanding the spectral response window of Si wire-based photodetector to a longer NIR region, new paths for emerging optoelectronic applications will open up that would be based entirely on CMOS compatible flexible and compact Si wire that would provide high device performance at a lower cost.

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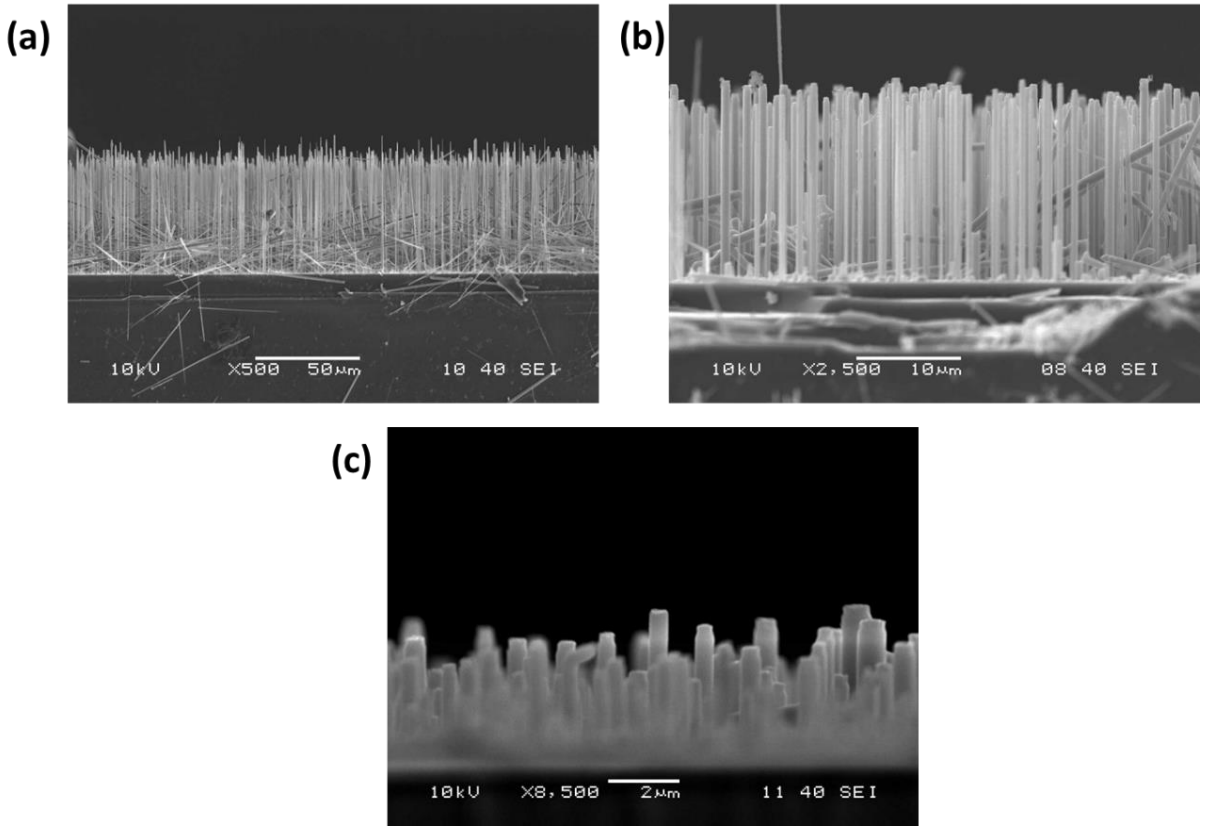
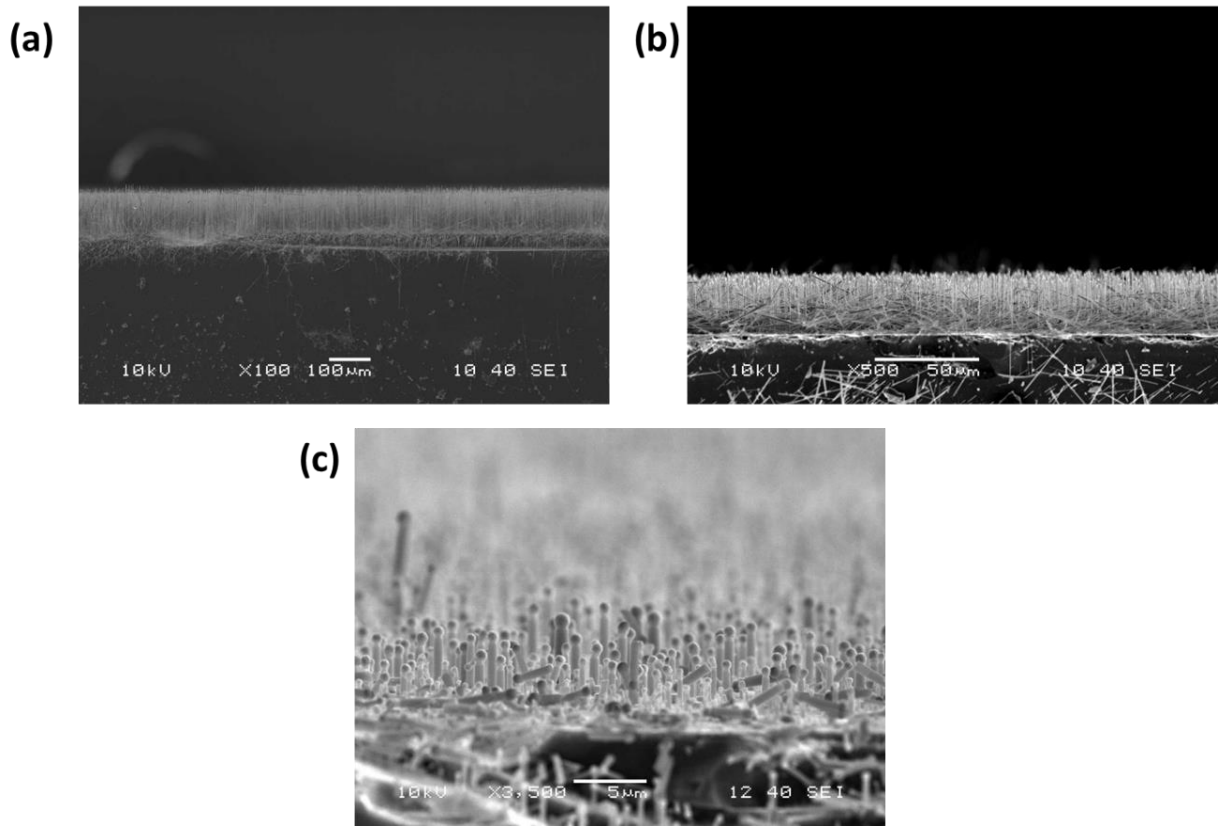
APPENDIX

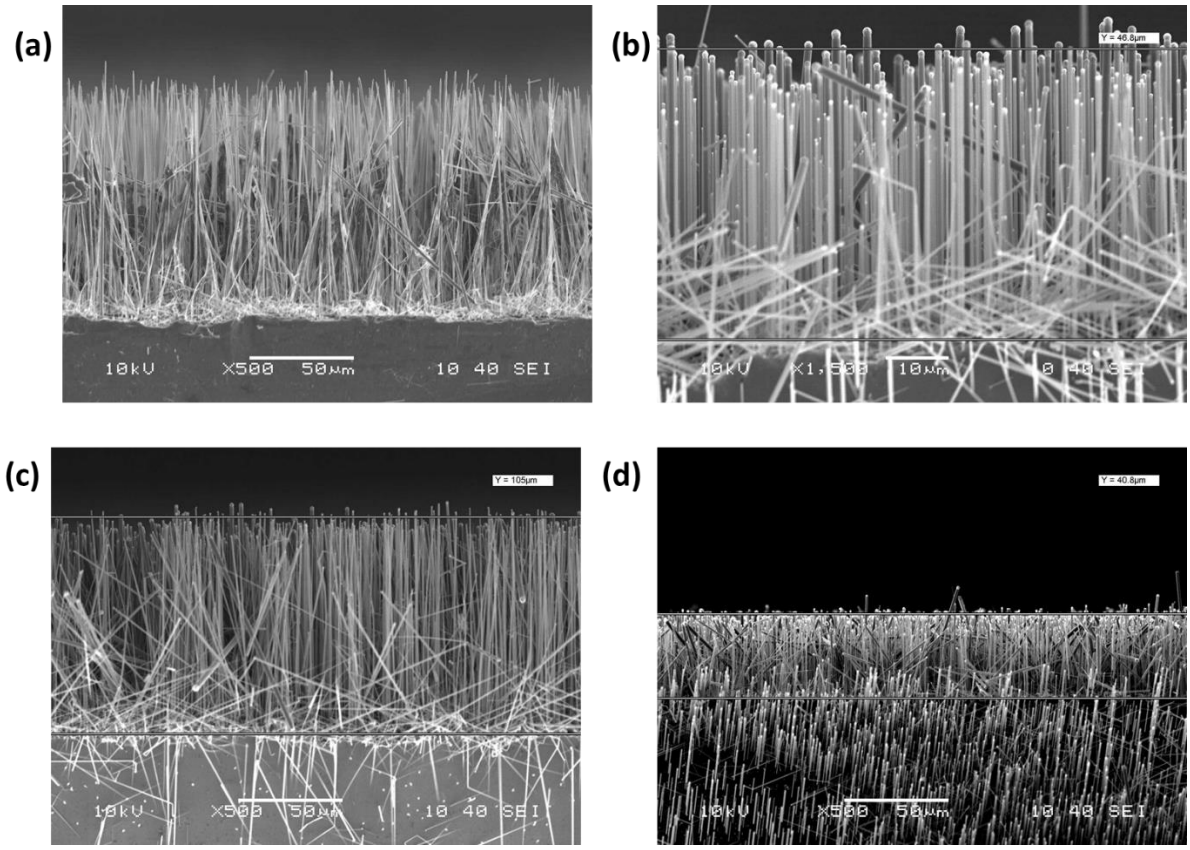
A1: Cross-sectional SEM micrographs of Cu etched Si MWs grown using 10:200 sccm H_2: Ar gas flow rate, growth time 1.5 min, at (a) D_4, (b) D_5, and (c) D_6, respectively.



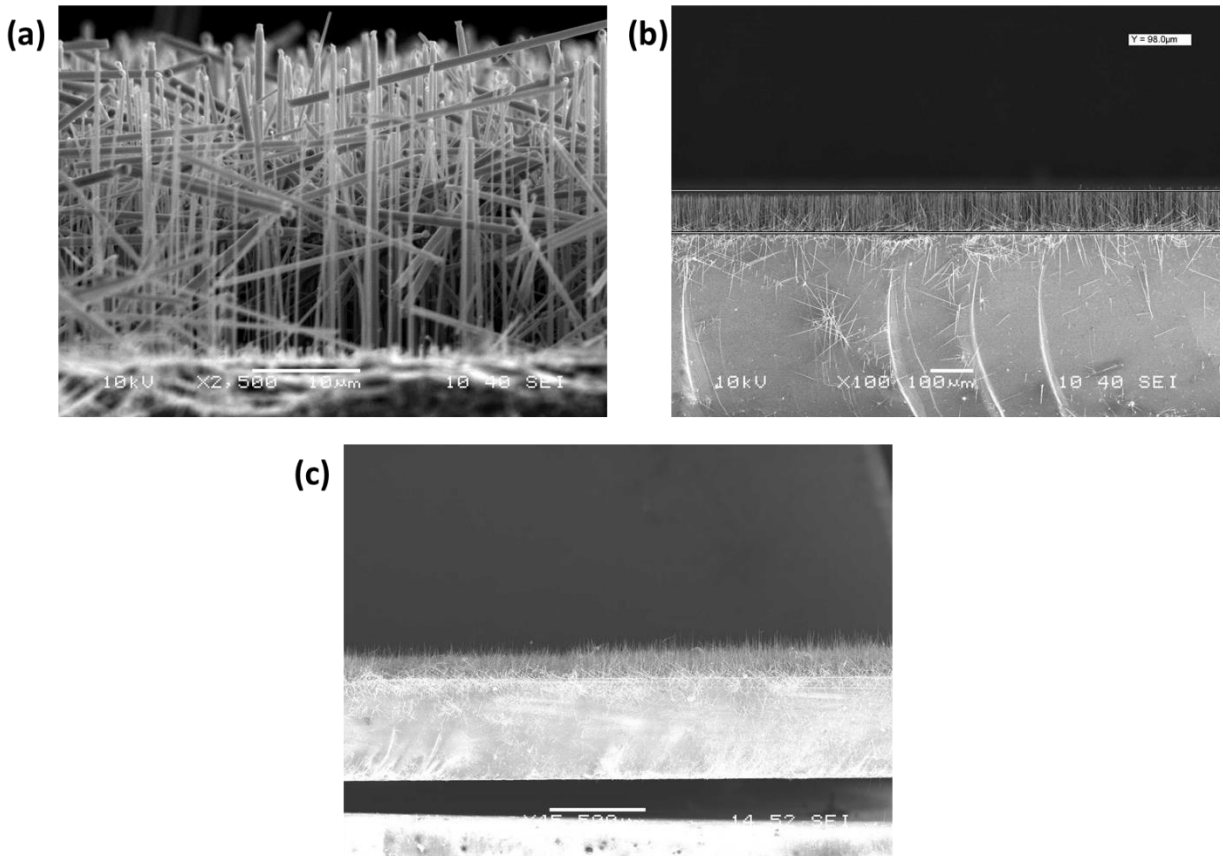
A2: Cross-sectional SEM micrographs of Cu etched Si MWs grown using 10:100 sccm H_2: Ar gas flow rate, growth time 1.5 min, at (a) D_4, (b) D_5, and (c) D_6, respectively.



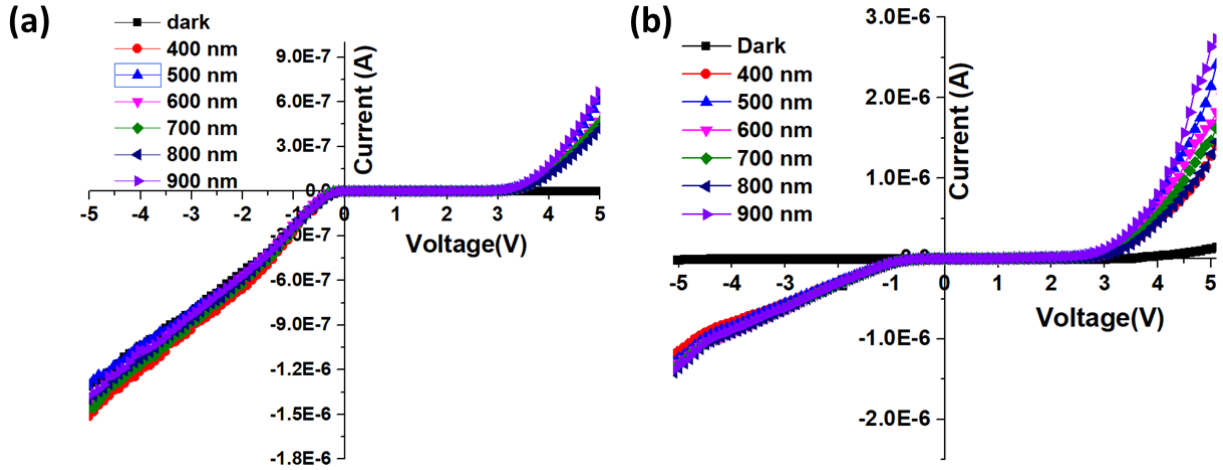
A3: Cross-sectional SEM micrograph of Si MWs grown using (a) 30 nm Cu at D_4 and (b) D_5, (b) and (c) 40 nm Cu thin film at D_4 and (d) D_5, respectively.



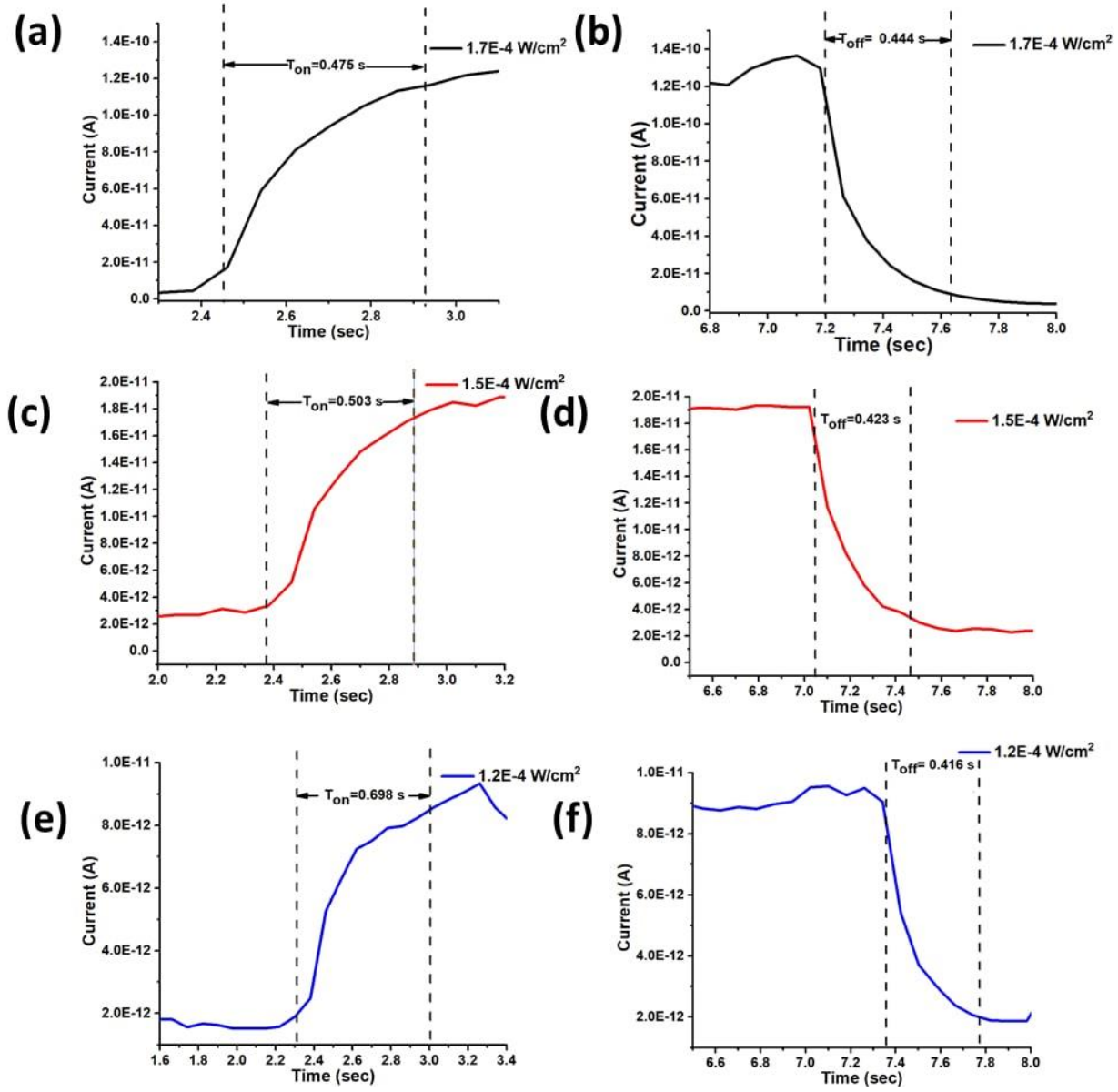
A4: SEM micrograph of Si MWs grown using 30 nm Cu annealed at 1000 °C, 5 min with Ar: H_2 (10:200 sccm) at D_4 with growth time (a) 3 min, (b) 5 min, and (c) 7 min, respectively.



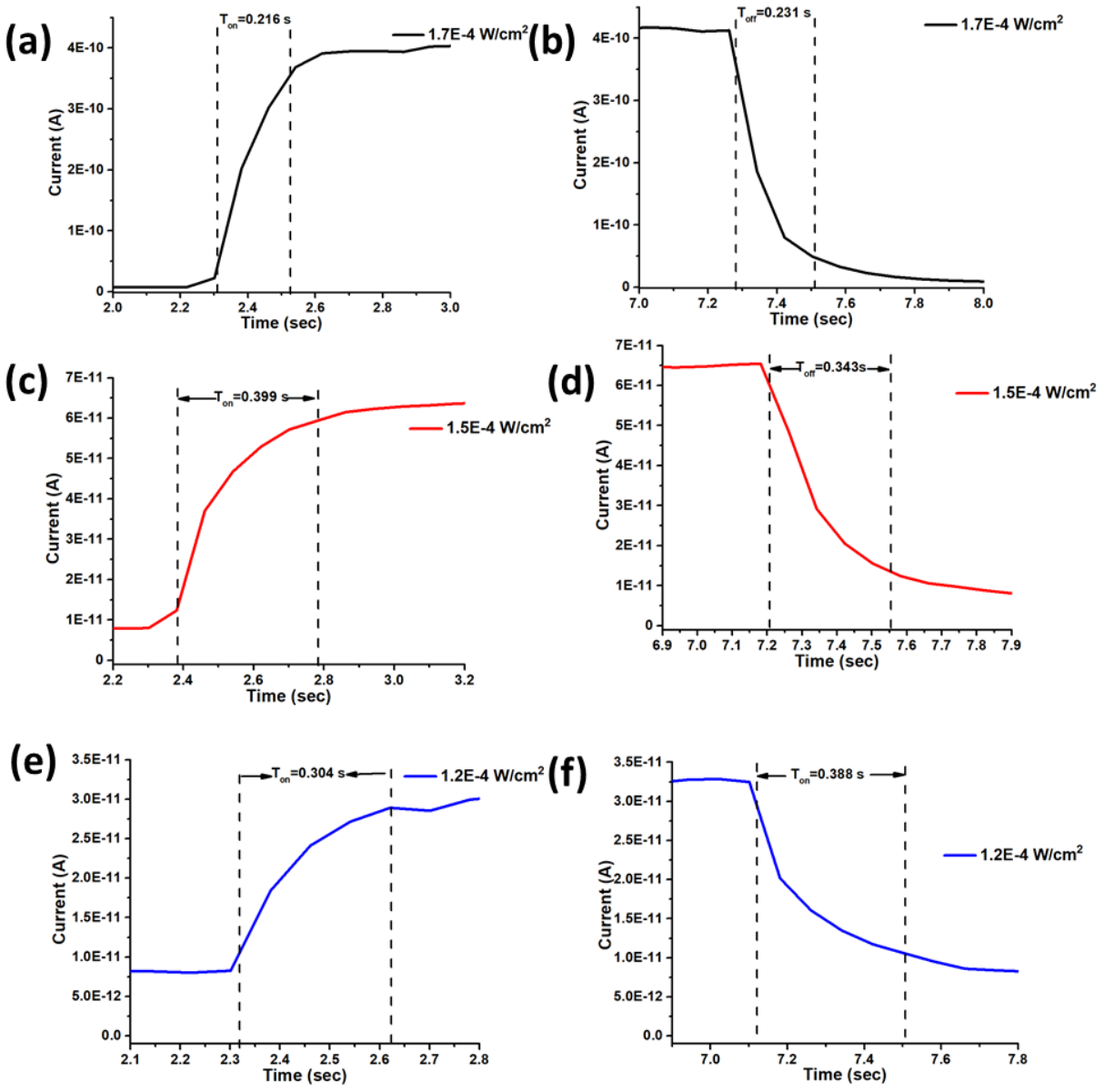
A5: Spectral response of Si MW photodetector using (a) CH_3-terminated D_4 Si MW (b) CH_3-terminated D_5 Si MW, respectively



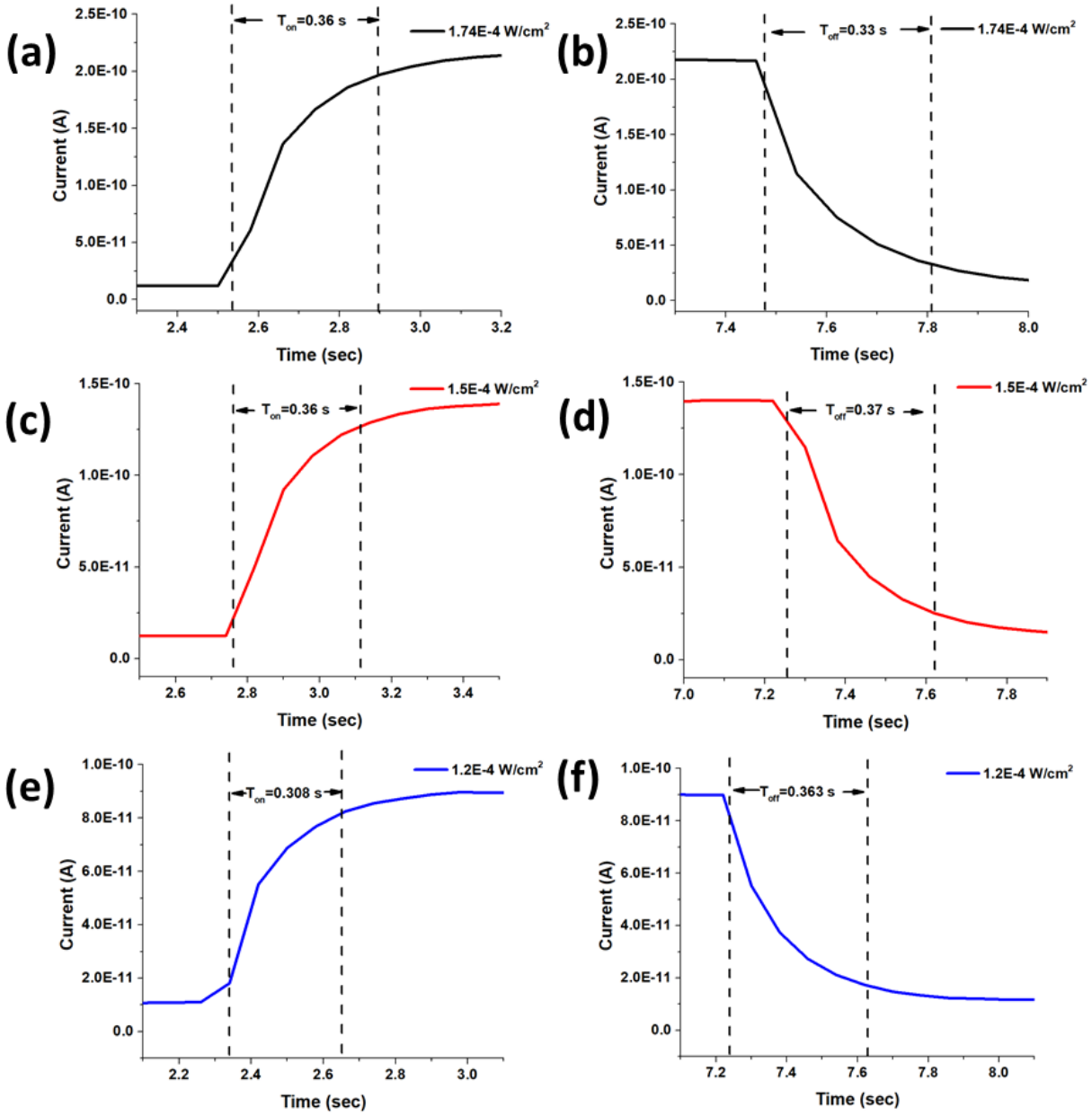
A6: T_{on} and $T_{off\ of}$ CH_3-terminated D_4 Si MW using 900 nm wavelength with different incident power density at 0.1 V applied voltage



A7: T_{on} and $T_{off\ of}$ CH_3-terminated D_4 Si MW using 900 nm wavelength with different incident power density at 1 V applied voltage



A8: T_{on} and $T_{off\ of}$ CH_3-terminated D_5 Si MW using 900 nm wavelength with different incident power density at 0.1 V applied voltage



A9: T_{on} and T_{off} of CH_3-terminated D_5 Si MW using 900 nm wavelength with different incident power density at 1 V applied voltage