# PV-BATTERY SERIES INTEGRATION FOR RESIDENTIAL SOLAR-PLUS-STORAGE SYSTEMS

by

Namwon Kim

A dissertation submitted to the faculty of
The University of North Carolina at Charlotte
in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in
Electrical Engineering

Charlotte

2022

Approved by:

_____
Dr. Babak Parkhideh

_____
Dr. Badrul Chowdhury

_____
Dr. Robert Cox

_____
Dr. Maciej Noras

# ABSTRACT

NAMWON KIM. Pv-battery series integration for residential solar-plus-storage systems. (Under the direction of DR. BABAK PARKHIDEH)

Solar-plus-storage systems provide efficient energy yield and management, resilience, and more revenue to residential houses and buildings. In solar-plus-storage systems, power electronics converters are integral components to generate the maximum output power from a solar photovoltaic (PV) array, store the generated energy into a battery, and finally deliver and manage the power to an electric load or the electric grid. Many existing solar-plus-storage systems still use and combine legacy power electronics converter topologies initially designed for a solar PV generation system or a battery energy storage system (BESS) separately. These power converters are connected in parallel to an AC or DC point of common coupling: AC-parallel and DC-parallel integration methods. Another integration method of a solar-plus-storage system is connecting a high-voltage battery to the high-voltage DC bus in parallel in a solar PV generation system having two-stages power converter architecture: In-line integration method. These methods result in increased costs and size, lower energy yields due to the increased number of power electronics converters, and the requirement of high-voltage PV strings and batteries.

This research studies new PV-battery integration methods and PV-battery series optimizers—power electronics converters optimally designed for different residential solar-plus-storage systems. The two PV-battery integration methods are proposed: AC-series integration and DC-series integration. The proposed integration methods are based on the series connection of PV and battery modules. The AC-series integration method assists the residential panel-level series-connected solar PV inverters in reducing the intermittent PV output fluctuations with a low-voltage-profile battery energy storage inverter. The DC-series integration enables PV voltage support,

reducing the number of power converter stages, reducing the rated power of power converters, improving the system round-trip efficiency, and seamless source integration. Three PV-battery series optimizers are proposed for different solar-plus-storage applications. The proposed power converter topologies and controls are discussed in this dissertation. Off-line simulation, real-time controller hardware-in-the-loop simulation, and lab-scale experiment results are included and analyzed to demonstrate the operating and design principle and the control performance of the proposed system.

# DEDICATION

Dedicated to my wife, my parents, my brother, and my family.

# ACKNOWLEDGEMENTS

I would like to express my deepest appreciation and respect to my advisor, Dr. Babak Parkhideh, for his continuous support and advice on my Ph.D. research and all academic work that I have accomplished at the University of North Carolina at Charlotte (UNC Charlotte). I also would like to acknowledge my dissertation committees, Dr. Badrul Chowdhury, Dr. Robert Cox, and Dr. Maciej Noras, for their invaluable feedback, suggestions, and advice on my dissertation work.

I would like to acknowledge the Department of Electrical and Computer Engineering and the Energy Production and Infrastructure Center (EPIC) at UNC Charlotte for all education, teaching, and research opportunities that helped me build my knowledge and experience in many different aspects including Power Electronics. This background has allowed me to conduct and complete my Ph.D. research. I also would like to acknowledge the Graduate School and the International Student and Scholar Office at UNC Charlotte for all the academic support that helped me continue my Ph.D. research without interruptions, even during this challenging pandemic.

I would like to sincerely thank my lab mates and coworkers at UNC Charlotte—Dr. Mehrdad Biglarbegian, Mr. Chondon Roy, Dr. Hamidreza Jafarian, Dr. Iman Mazhari, Dr. Shahriar Nibir, Mr. Hossein Niakan, Mr. Ali Parsa Sirat, Mr. James Gafford, Dr. Daniel Evans, and Mr. Andrew LeClair—for their collaboration. I also would like to acknowledge our PowerAmerica team at UNC Charlotte and Dr. Madhu Chinthavali and his research team at ORNL for their support in the projects.

TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# LIST OF ABBREVIATIONS

AC Alternating current

AVG Average

BES Battery energy storage

BESS Battery energy storage system

CAVC Current administrator voltage compensator

CHIL Controller hardware-in-the-loop

DAB Dual active bridge

DC Direct current

DDE Detect drop end

DER Distributed energy resource

DRRC Decentralized ramp-rate control

ESS Energy storage system

FB Full bridge

HF High frequency

KVL Kirchhoff's voltage law

MPP Maximum power point

MPPT Maximum power point tracking

P-V Power versus voltage

P&O Perturb and observe

PE Power electronic

PI Proportional-integral

PLL phase locked loop

PPP Partial power processing

PPR Partial-power rate

PR Proportional-resonant

PS Primary side

PV Photovoltaic

RMS Root mean square

RRC Ramp-rate control

SE Series

SS Secondary side

TAB Triple active bridge

TS Tertiary side

V-I Voltage versus current

VMM Voltage mode members

# CHAPTER 1: INTRODUCTION

## 1.1 Motivation

Solar photovoltaic (PV) energy is one of the most promising renewable energy sources. Deployment of solar PV has grown rapidly in the United States over the years. Since 2016, around 10 GW of new PV installation has been made in the U.S. [1, 2]. Although solar PV energy is a clean and sustainable energy resource, the amount of generated electricity is highly dependent on the solar irradiance or panel temperature, which are affected by continuously changing weather conditions [3]. Integration of solar PV generation and battery energy storage (BES), referred to as solar-plus-storage, is an effective energy management solution that improves the utilization of electricity generated by solar PV generation systems [4, 5, 6]. A BES system stores surplus energy when a PV array's output power is higher than a load's power demand and discharges the saved energy when the PV output power becomes lower. This PV-battery integration helps meet power demands from electrical loads or the AC grid, while the generated power from the solar PV generation system varies due to intermittent weather conditions. Solar-plus-storage systems can provide efficient energy yield and management, resilience, and more revenue to residential houses and buildings.

In solar-plus-storage systems, power electronic (PE) converters work as key devices for power transfer from energy sources to loads or the AC grid [7, 8, 9]. The power converters generate the maximum output power from a solar PV array, store or release the energy to or from a BES, deliver the power to electric loads or the grid, and control these internal power distributions. Depending on the used PE converters for each power conversion stage and their coupling locations, different configurations of

solar-plus-storage systems are available [10]—AC-parallel, DC-parallel, and In-line—as shown in Figure 1.1. However, these state-of-the-art system configurations still use and combine legacy PE convert topologies initially designed for a solar PV generation system or a BES system separately. Therefore, they require many power converter stages or high-voltage PV arrays and batteries to interface both PV and battery to the grid. These system integration requirements result in higher system cost, bigger system size, and less round-trip efficiency.

This dissertation focuses on new configurations of solar-plus-storage systems and proposes PV-battery series optimizers—PE converters optimally designed for different residential solar-plus-storage systems.

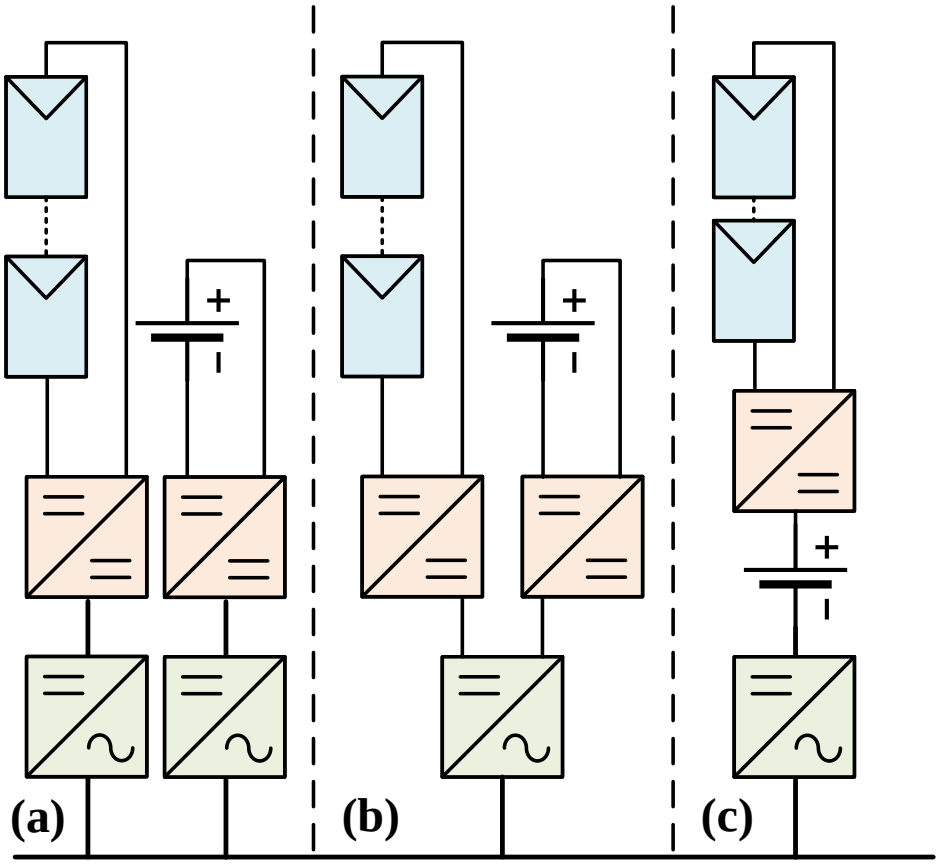


Figure 1.1: State-of-the-art battery integration methods for grid-connected PV inverters in residential and commercial applications (a) AC-parallel integration, (b) DC-parallel integration, and (c) in-line integration.

## 1.2 Literature Review

The most common PV-battery integration strategy is the AC-parallel integration that combines multiple distributed energy resource (DER) inverters at an AC coupling bus in parallel [11, 12, 13], as shown in Figure 1.1a. Each DER inverter regulates power flow between its DC energy source and the AC grid. In both solar PV and BES systems, an individual DER inverter commonly consists of two cascaded power conversion stages: a step-up DC-DC converter and a single- or three-phase DC-AC inverter. The step-up DC-DC converter is utilized to perform the main power control functions with DERs, such as PV maximum power point tracking (MPPT) control or battery charging and discharging control and amplify its input voltage to fit with the DC-AC inverter's DC input voltage range. The DC-AC inverter is responsible for maintaining grid-connection with the AC grid and conducting constant or variable DC input voltage control with the regulation of the AC output power. This two-stage architecture helps solar-plus-battery system overcome a lack of their DC voltage caused by: a) the PV MPPT operation under low solar irradiance and high panel temperature, b) the limited area of solar panel installation in series, or c) a usage of low-voltage battery.

The AC-parallel integration method has been widely accepted by users—who already have DER inverters integrated to their AC grid—because of its system scalability. Additional DER inverters can be simply added to the AC grid since DER inverters are designed for the standard AC grid and are controlled independently. However, this integration method is not an economical solution due to the large number of PE converter stages. Based on the above-mentioned system configuration, the AC-parallel integrated system requires at least four PE converter stages for the PV-battery integration. The more PE converters, the higher the system cost and the lower the system efficiency. Especially, the round-trip efficiency becomes the lowest among all DER integration methods because of the largest number of converters in

the power flow path from a PV array to a battery.

Another common state-of-the-art PV-battery integration strategy is the DC-parallel integration that combines multiple DER converters at a DC power bus in parallel [14, 15, 16], as shown in Figure 1.1b. Like the DER inverters in the AC-parallel integrated system, each DER converter regulates power flow between its input energy source and output loads or the power bus. In the DC-parallel integration, however, the power bus is a DC coupling bus, referred to as DC-link. Therefore, an individual DER converter commonly consists of a single power conversion stage using a step-up DC/DC converter, and DER converters are connected to a separate power conversion stage delivering the DERs' power gathered at the DC-link to the AC load or grid by using a single- or three-phase DC-AC inverter. The operating principles of a step-up DC-DC converter and a DC-AC inverter are the same as or similar to the ones used in the AC-parallel integration.

Accordingly, the DC-parallel integration method has advantages over the AC-parallel integration in the system's cost, size, and energy conversion efficiency. Since only a single DC-AC inverter is used in the entire integrated system, the DC-parallel strategy has a fewer number of PE converter stages; for example, at least three PE converters are necessary for the PV-battery integration in the above-mentioned configuration. This reduction results in lower system cost and higher system efficiency. Especially, the power loss resulting from the round-trip process decreases by half compared to the one from the AC-parallel integration if it is assumed that the efficiencies of individual PE converters are the same. Also, the DC-parallel integration provides system scalability with the parallel coupling of multiple DER converters at the DC-link and their independent control schemes. However, the expansion at the DC-link is limited by the specifications of the DC-AC inverter used, such as DC input voltage range, maximum DC input current or power, etc., and the integrated system still requires additional DER converters for the expansion resulting in an increase in

system cost and size as well as a reduction in efficiency.

The third state-of-the-art PV-battery integration strategy is the In-line integration that directly inserts a BES in parallel to the DC-link of the two-stage grid-connected PV generation system composed of a DC-DC converter and a DC-AC inverter [17, 18], as shown in Figure 1.1c. Once the battery is directly connected to the DC-link, the control scheme of the DC-AC inverter needs to be adjusted from when the DC-AC inverter is used for the PV-only system. This adjustment changes the main operating function of the DC-AC inverter. Consequently, the system configuration can be redefined based on the individual PE converters' operating functions—the combination of a PV DC-DC converter and a battery DC-AC inverter. The PV DC-DC converter conducts the PV array's MPPT control, which is the same operating function of the PV DER converters used in the above mentioned two other integration strategies. On the other hand, the battery DC-AC inverter performs not only the grid-connection but also the battery charging and discharging control by adjusting the AC output power. In this integration method, the DC-link voltage is not controllable by any PE converters due to the voltage-source nature of the battery.

According to the direct integration of the battery, the In-line integration method has the least number of PE converters among all DER integration methods; at least two PE converters are required. Therefore, simplicity of the hardware architecture and further improvement on the system's efficiency are achieved. For instance, the energy conversions between the PV array and the battery or the battery and the AC grid can be made through only a single PE converter: the PV DC-DC converter or the battery DC-AC inverter, respectively. However, the direct integration also restricts the system's scalability and reconfigurability. In this integration method, the battery voltage needs to be higher than the minimum requirement of the DC input voltage of the DC-AC inverter for the grid-connection, or additional voltage amplification devices, such as a line-frequency transformer, are required, which causes an increase

of system cost and size. Also, like the DC-parallel integration method, the power expansion of PV and battery sources is highly dependent on the DC-AC inverter's specifications. Besides, dynamic response of the PE converters' control scheme needs to be adjusted because the battery integration changes the DC-link's system properties that needs to be considered for the controller design process. Furthermore, in case of single-phase grid applications, additional passive or active buffer decoupling double-line-frequency power pulsation from the DC battery power is required, which results an increase of system cost and size as well [19].

## 1.3 Proposed Solutions

This dissertation proposes a new approach to PV-battery integration, referred to as PV-battery series integration, and develops new PE converter solutions called PV-battery series optimizers for solar-plus-storage system applications.

The state-of-the-art PV-battery integration methods reviewed above require either additional PE converter stages or high-voltage energy sources to integrate a BES into a solar PV generation system. This is mainly because these methods adopt the parallel-integration approach. In the parallelly integrated system, the magnitude and form of output voltages of individual modules must be the same. The voltage magnitude of the parallel coupling node is usually higher than the voltage of the sources since the grid voltage or the DC bus voltage is high to be connected to the standard grid systems. This system integration requirement increases system cost and size and reduces the energy delivery efficiency.

On the other hand, the proposed PV-battery series integration approach can lessen this system integration requirement by connecting the PV module and the battery module in series. The series-connected energy modules can share the high-voltage requirement of each other. Therefore, a more optimal system design can be achieved. This dissertation proposes two PV-battery series integration methods depending on the solar-plus-storage system applications; AC-series and DC-series integrations.

The AC-series integration method adds a battery DC-AC inverter module into the AC power bus by adopting the AC-stacked PV inverter architecture approach. The AC-stacked PV inverter architecture is a novel panel-level residential solar PV inverter that achieves system miniaturization with series integration of modular PV inverters and the decentralized control scheme [20, 21]. The advantages of the AC-series integration over other state-of-the-art PV-battery integration methods are the system miniaturization and the highest energy conversion efficiency from the DERs to the AC grid. Costs of inverter components, installation, and maintenance can be significantly reduced by a) the low-voltage and high-frequency hardware design of individual inverter members and b) the removal of communication requirements among themselves or with the supervisory control center for the main power control functions. Also, only a single PE converter is required for the power delivery from DERs to the AC grid resulting in less power loss from the PE converter. Because of the miniaturized system design, the modular battery inverter in this PV-battery AC-stacked inverter architecture is suitable to mitigate sudden PV power fluctuations caused by weather changes: PV ramp-rate control [22, 23, 24, 25]. The proposed AC-series integration system has restrictions in control due to the interactive operation among the different inverter members under various asymmetrical operating conditions. The proposed system's feasibility and effectiveness are investigated through the controller hardware-in-the-loop (CHIL) simulation results and the operating margin analysis. In addition, the decentralized PV ramp-rate control that uses local feedback information only to conduct the PV ramp-rate control function without communication between the PV and battery inverters is developed to maintain the decentralized control environment in the AC-stacked inverter system.

The DC-series integration method directly connects a PV array and a BES in series. These series-connected energy sources are connected to the DC power bus in parallel. Therefore, the above-mentioned high-voltage system integration require-

ment can be reduced. As the DC-series integration has restrictions on independent current control of two series-connected energy sources, a controllable current source is added to inject a compensation current into the PV-battery DC-series coupling node. The PV-battery series optimizer—adopting partial power processing (PPP) converter topology [26, 27, 28, 29, 30]—is applied in the proposed system to configure this controllable current source. The advantages of the DC-series integration over other state-of-the-art PV-battery integration methods are a) PV-battery voltage support to be connected to a high-voltage DC bus without a fully rated power converter, b) reduction of the rated power of the interfacing DC-DC converter by adopting PPP system architecture, c) single power converter stage between the series-connected energy sources and the DC bus, and d) system reconfigurability without changing circuit topology. The proposed system is suitable for energy backup and resilience applications. In this research, two PV-battery series optimizers are developed for two different grid applications: AC grid and DC grid. In the AC grid coupled system, the coordinated closed-loop control between the PV-battery optimizer and the DC-AC inverter is proposed for different operation modes since the DC-bus voltage varies according to the PV's and the battery's operating conditions. In the DC grid coupled system, especially a regulated DC microgrid, a modification of the DC-series integration by adding a variable voltage source to the PV-battery DC series loop and developing the PV-battery-series optimizer working as both a controllable current source and a variable voltage source are proposed. The operating and control principles and the contributions of the proposed systems are demonstrated through DC analysis, off-line simulation, real-time CHIL simulation, and experimental results.

## 1.4 Organization of Dissertation

The dissertation is organized as follows: Chapter 2 describes the AC-series integration method and the operating margin analysis of the PV-battery AC-stacked inverter architecture with the decentralized PV ramp-rate control [31]. Chapter 3 presents the

DC-series integration method and the PV-battery series inverter architecture with the coordinated control algorithm [32]. Chapter 4 discusses the modified DC-series integration method for a regulated DC microgrid application and its interfacing converter, PV-battery-series DC-DC optimizer. Chapter 5 presents the conclusions and discussions of the research.

# CHAPTER 2: CONTROL AND OPERATING RANGE ANALYSIS OF AN AC-STACKED PV INVERTER ARCHITECTURE INTEGRATED WITH A BATTERY

This chapter presents a control scheme to operate a battery-integrated AC-stacked photovoltaic (PV) inverter architecture and its operating range analysis. The main operation strategy is the combination of decentralized controls of individual inverter members; PV and battery. In AC-series integration, battery charging and discharging operations affect operating margins of the PV inverter members. The interactive operation needs to be analyzed to identify the system operating range under different conditions. A ramp-rate control which mitigates PV output variations and improves grid stability is a suitable application for the PV-battery AC-stacked inverter architecture utilizing a panel-level modular inverter design. Decentralized ramp-rate control algorithm is proposed and demonstrated to analyze the system operating range. The detailed system control and analysis are performed through controller hardware-in-the-loop testing.

## 2.1 Introduction

The AC-stacked photovoltaic (PV) inverter architecture is a panel-level cascaded modular inverter topology suitable for single-phase grid-tied PV applications [1], [2]. High-frequency and low-voltage PV inverter members are stacked in series to satisfy the AC voltage for grid-connection and extract maximum output power from individual PV panels. To maximize the architecture's effectiveness, each building block is controlled independently without communications among themselves and with minimum handshaking with the supervisory control center for grid-synchronization [2].

Its tangible advantages and capabilities with smart inverter functions are verified through laboratory experiments, controller hardware-in-the-loop (CHIL) testing, and site demonstration in [2]-[7].

In PV applications, integration of a battery into a PV generation system has received significant attention because of the intermittent nature of solar energy sources [8]-[10]. In most of state-of-the-art battery integration methods, legacy PV power electronics systems [11] are used to configure different integration topologies; a) AC-parallel [12], [13], b) DC-parallel [14]-[16], and c) in-line [17]-[19] integrations. In these integration methods, voltage-amplification power electronics stages or high-voltage battery are required to cope with high DC input voltage requirement of a DC-AC inverter. On the other hand, the AC-stacked PV inverter architecture can integrate a battery without the high voltage requirement by adopting AC-series configuration [20], [21]. Besides, system optimization can be achieved by adding a battery inverter unit into the termination box which has already been applied to the AC-stacked PV inverter architecture for protection, phase locked loop (PLL), and communication with the supervisory control center [2], [3].

This research investigates control scheme and operation characteristics of the PV-battery AC-stacked inverter architecture. In this architecture, modular inverter members are cooperating to maintain grid-connection and control the AC string power. Therefore, this cooperation introduces interactive operations among the inverter members when system operating condition varies. Since the interactive operation creates duty cycle changes in the DC-AC inverters, analysis of the inverter members' interaction is required to clarify the operating range of the architecture with battery charging and discharging operation.

Due to the battery charging and discharging limitations caused by the interaction, a ramp-rate control (RRC) is a suitable application for the PV-battery AC-stacked inverter architecture utilizing a panel-level modular inverter design. A RRC mitigates

fast-changing, high ramp-rate, PV output variations and regulates the desired ramp-rate of the PV output by controlling the battery charging and discharging current [22]-[25]. Grid stability issues such as voltage and frequency fluctuations caused by high penetration of PV generation in especially weak distribution network can be improved by lowering the PV output ramp-rate. In this chapter, the decentralized ramp-rate control (DRRC) using the differentiation of the AC string current as an indicator of PV output variations is proposed to realize the decentralized control environment and minimize the communication requirements between the inverter members [21]. Since the inverter members are connected in series, the differentiation of the AC string current represents both PV and battery output variations when the battery is charged or discharged. Therefore, new criteria to distinguish PV output variations and create the proper amount of the battery current reference for the DRRC are presented. The control performance of the DRRC and the interactive operation among the inverter members with PV and battery output variations are demonstrated through CHIL testing.

## 2.2 PV-Battery AC-Stacked Inverter Architecture

### 2.2.1 Proposed PV-battery AC-stacked inverter architecture

The proposed PV-battery AC-stacked inverter architecture is composed of three different types of modular inverters: a) current administrator voltage compensator (CAVC), b) voltage mode members (VMM), and c) energy storage system (ESS). By stacking or connecting a group of PV inverters in series, the architecture can support the AC grid voltage requirement for grid-connection with low voltage semiconductor devices. Figure 2.1 presents the AC-series configuration and the control diagram of the three different types of modular inverters. A CAVC controls its DC input voltage, $V_{PV1}$, with a closed-loop PI controller. A maximum power point tracking (MPPT) control generates the DC input voltage reference to extract the maximum power from the PV panel. Also, the CAVC is responsible for controlling the AC

string current, $I_{string}$, with a closed-loop PR controller. A VMM only controls its DC input voltage, $V_{PV2}$, for the MPPT control of its PV panel. Multiple VMMs work as voltage buffers to build up the architecture's AC output voltage. An ESS controls the battery charging and discharging current, $I_{Batt}$, with a closed-loop PI controller. The proposed RRC generates the battery current reference to mitigate PV output variations. Individual closed-loop controls generate modulation indices, $m_{inv1}$, $m_{inv2}$, and $m_{inv3}$, to operate individual inverter members, and the feedforward terms, $V_{C1,pu}$, $V_{C2,pu}$, and $V_{C3,pu}$, are applied to improve the system control response and lower the impact of grid disturbances.

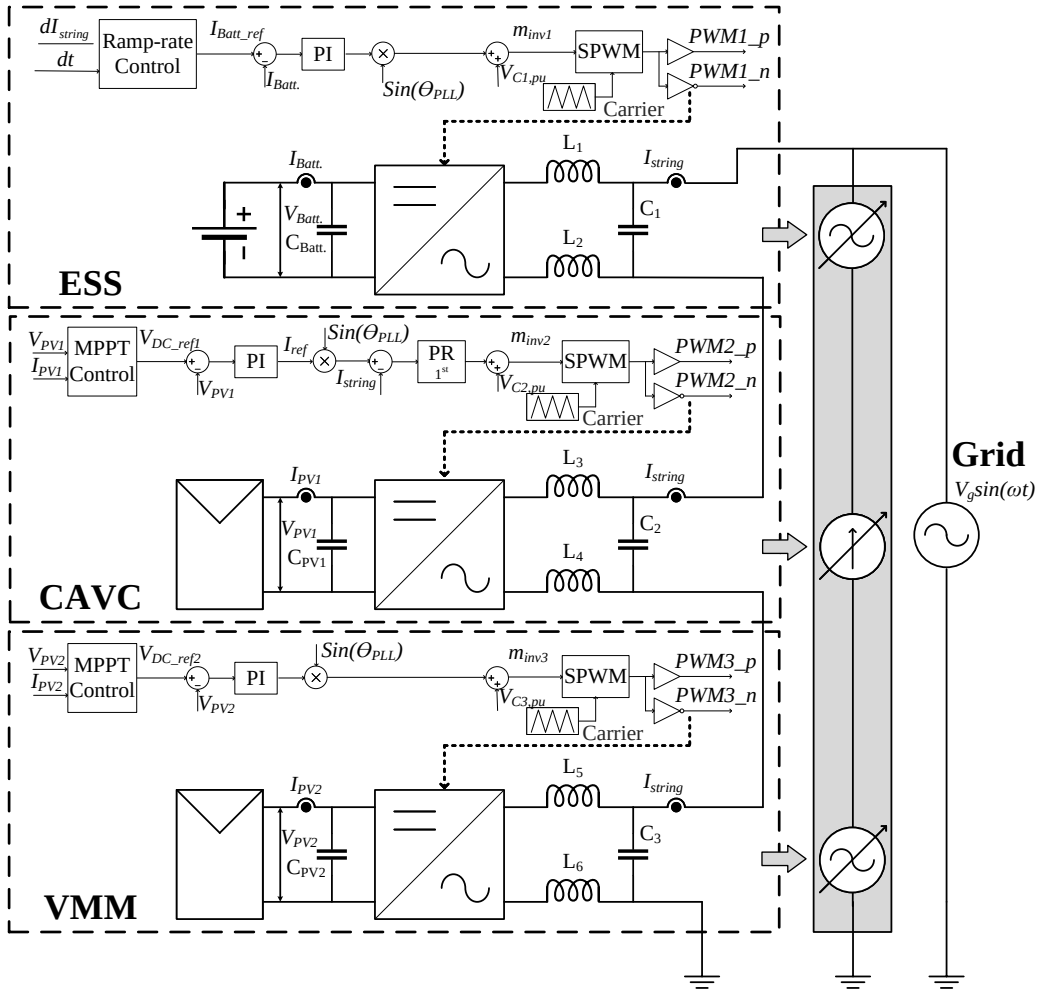


Figure 2.1: PV-battery AC-stacked inverter architecture and control diagram.

Details of the RRC strategy are explained in section III. Since the PV-battery AC-stacked inverter architecture provides the decentralized environment in terms of both physical topology and control, each modular inverter is controlled autonomously by using its local measurements except grid-synchronization information.

### 2.2.2 Interactive operation between inverter members

The main operation principle of the proposed PV-battery AC-stacked inverter architecture is the combination of the decentralized control algorithm of the individual inverter members connected in series. In the AC string where the same AC current, $i_{string}$, is passing through all the inverter members, the inverters' output voltages vary based on the inverter output power. Since the inverters are cooperating to regulate their AC output power in grid-connection, one inverter's output power variations may affect others' AC output voltages corresponding to the inverters' operating margin. Therefore, the interaction between the inverters limits the operating range of the architecture.

When asymmetrical irradiance drop is applied to the PV panels, the PV inverter with the low output power decreases its AC output voltage, and it makes other inverters increase their output voltage to compensate the AC voltage drop and track individual maximum power point (MPP), as presented in previous publications [2], [4]. Likewise, battery charging and discharging operations force PV inverters' AC output voltage changes [21]. When battery charging mode is applied to the ESS inverter, the ESS AC voltage appears to be inverted to have negative power flow through the ESS. The inverted ESS AC voltage makes the CAVC and the VMM increase their AC voltages resulting the PV inverters' higher modulation indices. Higher modulation index requests the use of more operating margin for the inverter. If the amount of the compensated AC voltage is higher than the PV inverters' remaining operating margins, the modulation indices reach the maximum amount (1.0), and abnormal operation such as AC current distortion or losing MPPT occurs because the inverters

have no room to increase their output voltage more. Different control schemes in the CAVC and the VMM introduce the different abnormal operations, AC current distortion and losing MPPT control, since the CAVC utilizes sinusoidal AC string current information as the feedback signal for the closed-loop control and the VMM utilizes DC input voltage information. This interaction is required to be considered to design the reliable PV-battery AC-stacked inverter architecture which has a wide operating range and provides high-quality AC current.

## 2.3 Decentralized Ramp-Rate Control Strategy

In the proposed architecture utilizing a panel-level inverter design, a RRC which smooths out PV output variations is a suitable application of the battery integration due to the battery charging and discharging limitations caused by the interaction addressed in the previous section. In this architecture, the ESS determines its battery current reference without handshaking with PV inverters or supervisory control center to achieve decentralized control environment. In the proposed DRRC strategy, the ESS utilizes its local AC string current measurement, $i_{string}(t)$, for detection of PV output variations and battery current calculation. The overall mechanism of the DRRC is shown in Figure 2.2a. The first step is the detection of PV variations with the differentiation of AC string current, as follows:

$$\frac{di_{string\_avg}(t_k)}{dt} = \frac{di_{string\_avg}(t_k) - di_{string\_avg}(t_{k-1})}{t_k - t_{k-1}} \tag{2.1}$$

where $t_k$ is the time at the $k^{th}$ instant, $t_{k-1}$ is the time at the $(k-1)^{th}$ instant, $i_{string\_avg}(t)$ is the RMS average of $i_{string}(t)$, and $dI_{string\_avg}(t)$ is the AC current difference. To ignore small variations caused by the MPPT control, a dead-band, $dI_{limit}$, is applied, as follows:

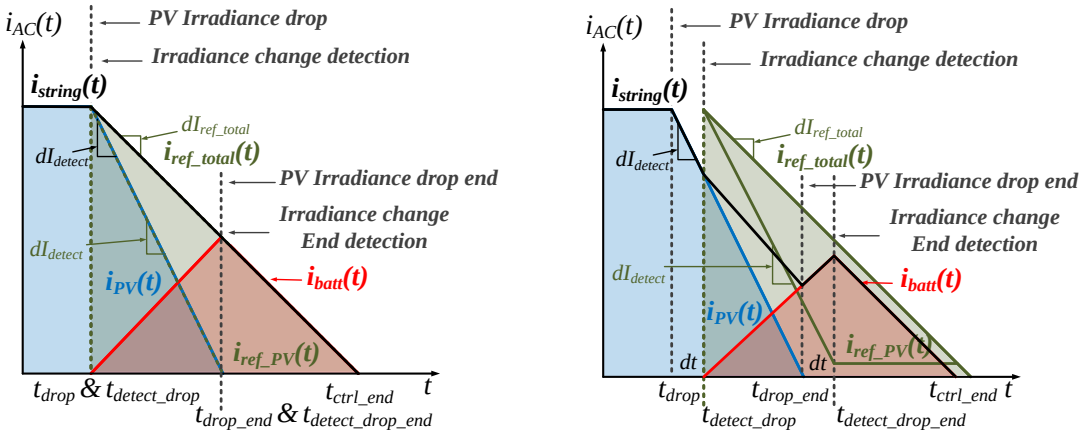


Figure 2.2: Illustration of the DRRC algorithm (a) Ideal case: without detection delay and (b) Practical case: with detection delay.

$$dI_{detect} = \begin{cases} dI_{string\_avg}(t_{detect\_drop}), & dI_{string\_avg}(t_{detect\_drop}) > dI_{limit} \\ 0, & dI_{string\_avg}(t_{detect\_drop}) \leq dI_{limit} \end{cases} \tag{2.2}$$

where $t_{detect\_drop}$ is the moment when PV output variation is detected, $dI_{string\_avg}(t_{detect\_drop})$ is the AC string current difference at $t_{detect\_drop}$, and $dI_{detect}$ is the PV output change detected.

The ESS will start to charge or discharge the battery to achieve the desired ramp-rate of the inverter architecture's output once the PV output variation is detected. In the proposed architecture, a criterion to distinguish the PV output changes from the total AC string output power is required for the decision of the ESS output current since the output of the ESS also affects the differentiation of the AC string current due to the series-connection. As shown in Figure 2.2a, two current references $i_{ref\_PV}(t)$ and $i_{ref\_total}(t)$ are generated with two different ramp-rates; the detected PV output ramp-rate, $dI_{detect}$, and the desired architecture's output ramp-rate, $dI_{ref\_total}$, respectively, as follows:

$$i_{ref\_PV}(t_k) = i_{ref\_PV}(t_{k-1}) + \frac{dI_{detect}}{dt} T_{step} \tag{2.3}$$

$$i_{ref\_total}(t_k) = i_{ref\_total}(t_{k-1}) + \frac{dI_{ref\_total}}{dt} T_{step} \tag{2.4}$$

$$dI_{ref\_total} = dI_{detect} k_{ramp\_rate\_total} \tag{2.5}$$

where $T_{step}$ is the controller time step and $k_{ramp\_rate\_total}$ is the ramp-rate gain (0.1-1.0). By subtracting $i_{ref\_PV}(t)$ from $i_{ref\_total}(t)$, the battery current reference, $i_{batt}(t)$, can be calculated, and its absolute value, $|i_{batt}(t)|$, is increased until the moment of PV output variations stop denoted as $t_{drop\_end}$. After $t_{drop\_end}$, $i_{ref\_PV}(t)$ is set as constant by forcing $dI_{detect}$ zero, and $|i_{batt}(t)|$ decreases constantly until it becomes zero, $t_{ctrl\_end}$, as follows:

$$i_{batt}(t_k) = \begin{cases} (i_{ref\_total}(t_k) - i_{ref\_PV}(t_k))k_{ACtoDC}, & t_k \leq t_{DDE} \\ (i_{ref\_total}(t_k) - i_{ref\_PV}(t_{DDE}))k_{ACtoDC}, & t_{DDE} < t_k \leq t_{ctrl\_end} \end{cases} \tag{2.6}$$

where $k_{ACtoDC}$ is the AC to DC current gain and $t_{DDE}$ is the moment when the ESS detects PV output variation stop. DDE is the abbreviation of "detect drop end". The detection of PV output variation stop is achieved by monitoring the differentiation of the AC current, as below:

$$|i_{batt}(t_k)| \; decreases, \; if \begin{cases} \frac{di_{string\_avg}(t_k)}{dt} \leq 0, & Charging \; mode \\ \frac{di_{string\_avg}(t_k)}{dt} \geq 0, & Discharging \; mode \end{cases}. \tag{2.7}$$

When PV output variations stop, $|i_{batt}(t)|$ continues to increase and the differentiation of the AC current is going to be zero. Moreover, the direction of the differentiation

will be reversed unless $|i_{batt}(t)|$ starts to decrease. The reversed direction of the differentiation can be an indicator of $t_{DDE}$. After $t_{DDE}$, $|i_{batt}(t)|$ decreases to zero ($t_{ctrl\_end}$) and the proposed DRRC is completed. In Figure 2.2a and Figure 2.2b, ideal and practical cases of the DRRC strategy are illustrated. In Figure 2.2b, each transition of detection sequences such as from $t_{drop}$ to $t_{detect\_drop}$ and from $t_{drop\_end}$ to $t_{DDE}$ requires the differentiation calculation delay. This sequence delay will cause the mismatch between the final ramp-rate and the desired ramp-rate, and the small fluctuation of the AC power. The ramp-rate mismatch error can be reduced by optimizing the sequence delay.

## 2.4 Results and Discussions

To verify the effectiveness of the proposed architecture and its DRRC strategy, the CHIL test set-up is built, as shown in Figure 2.3 [26]. In this set-up, two PV inverters, a CAVC and a VMM, and an ESS inverter are constructed. The detail system parameters are represented in Table 2.1.

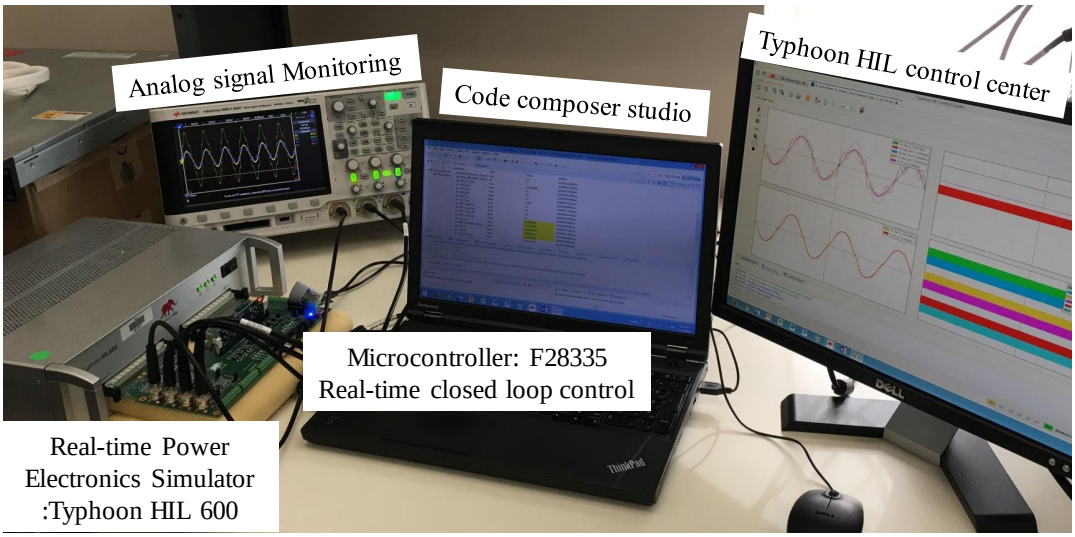


Figure 2.3: CHIL set-up for testing PV-battery AC-stacked inverter system.

Table 2.1: DESIGN PROPERTIES OF THE PV-BATTERY AC-STACKED INVERTER

| System Specifications | | |
|---|---|---|
| Grid | | |
| Voltage | $V_g$ ($V_{RMS}$) | 30 |
| PV panel | | |
| MPPT: Power ($1000W/m^2$) | $P_{MPP}$ (W) | 255.10 |
| MPPT: Voltage ($1000W/m^2$) | $V_{MPP}$ (W) | 33.45 |
| MPPT: Current ($1000W/m^2$) | $I_{MPP}$ (W) | 7.63 |
| Battery | | |
| Nominal voltage | $V_{Battery}$ (V) | 42.20 |
| Capacity | $C_{Battery}$ (Ah) | 20 |

### 2.4.1 Interactive operation between PV and ESS inverters

The CHIL test results of the inverters' interaction under asymmetrical PV output variations and battery charging and discharging are presented in Table 2.2. The minimum irradiance level on the CAVC where the architecture provides stable operation is $320W/m^2$. In this condition, the peak modulation index of the VMM reaches 1.0 by using all operating margin to cover the CAVC AC voltage drop. Below the minimum irradiance level, ($100W/m^2$), the architecture cannot perform MPPT control because the VMM is required to move its operating point to the right side of the MPP to increase its output voltage. In case of asymmetrical irradiance drop on the VMM, the minimum irradiance level is $250W/m^2$. Below the minimum irradiance level, ($100W/m^2$), AC current distortion occurs. The PV inverters' interaction limits the architecture's operating range.

Table 2.2: SUMMARY OF CHIL TEST RESULTS: PEAK MODULATION INDICES AND OPERATING MARGIN OF THE INVERTERS WITH DIFFERENT OPERATING CONDITIONS.

| Detail conditions | | | Peak modulation indices | | | Not in MPP | Current Distortion | Operating margin | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Irradiance level ($W/m^2$) | | Battery current (A) | CAVC | VMM | ESS | | | CAVC | VMM | ESS |
| CAVC | VMM | | | | | | | | | |
| 1000 | 1000 | - | 0.72 | 0.67 | 0.03 | - | - | 28% | 33% | 97% |
| 500 | 1000 | - | 0.51 | 0.89 | 0.03 | - | - | - | 11% (-22%) | - |
| 320 | 1000 | - | 0.39 | 1.0 | 0.03 | - | - | - | 0% (-33%) | - |
| 100 | 1000 | - | 0.28 | 1.0 | 0.03 | ☑ | - | - | 0% (-33%) | - |
| 1000 | 500 | - | 0.91 | 0.46 | 0.03 | - | - | 9% (-19%) | - | - |
| 1000 | 250 | - | 1.00 | 0.29 | 0.03 | - | - | 0% (-28%) | - | - |
| 1000 | 100 | - | 1.00 | 0.16 | 0.03 | - | ☑ | 0% (-28%) | - | - |
| 500 | 500 | - | 0.72 | 0.68 | 0.03 | - | - | 18% (0%) | 32% (-1%) | - |
| 1000 | 1000 | Charging: -4 | 0.99 | 0.97 | 0.46 | - | - | 1% (-27%) | 3% (-30%) | 54% (-43%) |
| 1000 | 1000 | Charging: -4.6 | 1.00 | 1.00 | 0.58 | - | - | 0% (-28%) | 0% (-33%) | 42% (-55%) |
| 1000 | 1000 | Charging: -4.8 | 1.00 | 1.00 | 0.64 | - | ☑ | 0% (-28%) | 0% (-33%) | 36% (-61%) |
| 1000 | 1000 | Discharging: 13.9 | 0.65 | 0.33 | 0.57 | - | - | 35% (+7%) | 67% (+34%) | 33% (-64%) |

Battery charging mode limits the architecture's operating range, as shown in Figure 2.4. When battery current is -4$A_{DC}$, the ESS generates -14.37$V_{RMS}$ AC voltage. The CAVC and the VMM consume their 96.4% (27%/28%×100=96.4%) and 90.9% (30%/33%×100=90.9%) of available operating margin, respectively, to compensate the inverted ESS AC voltage. The maximum battery charging current is -4.6$A_{DC}$ and the peak modulation indices of the PV inverters reach 1.0 by using all operating margin. With higher battery charging current than -4.6A, the AC current distortion occurs, as shown in Figure 2.4c. Therefore, the operating range in battery charging mode is related to the operating margin of the PV inverters (≈28% of CAVC's and ≈33% of VMM's). If the architecture is extended for 120$V_{RMS}$ electrical grid by adding identical PV inverters, the architecture can handle more asymmetrical irradiance drop and battery charging currents. However, the percentage of available operating margin is maintained. The PV inverters must be redesigned with a higher DC input voltage to increase the percentage of available operating margin.

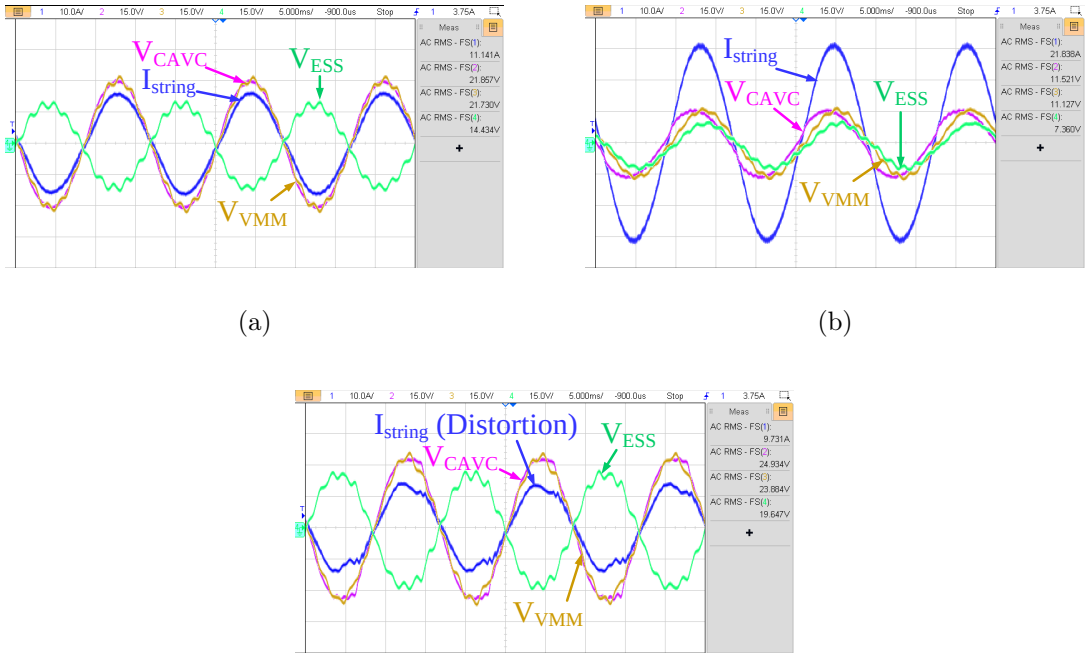


Figure 2.4: Interactive operation of the inverters with battery operating conditions; $I_{string}$: AC string current, $V_{CAVC}$: CAVC AC voltage, $V_{VMM}$: VMM AC voltage, and $V_{ESS}$: ESS AC voltage, (a) charging mode (-4A), (b) discharging mode (4A), (c) charging mode (-4.8A)

### 2.4.2 Decentralized ramp-rate control

Table 2.3 and Figure 2.5 present the CHIL test results of the DRRC under different asymmetrical irradiance changes. In this test, the 0.5 ramp-rate gain, $k_{ref\_total}$, is applied. When a CAVC irradiance drop ($1000W/m^2 \rightarrow 500W/m^2$) is applied, the CAVC output power is decreased by 122.1W for 2.72 seconds introducing the PV output ramp-rate, -1.50$A_{RMS}/s$, as shown in Figure 2.5a. Adopting the DRRC, the architecture achieves 47% of the PV output ramp-rate, -0.70$A_{RMS}/s$, by discharging the battery, as shown in Figure 2.5c. Detecting the AC power changes, the ESS increases the battery discharging current until the irradiance drop ends. Detecting the reversed sign of the differentiation of $i_{string}(t)$, the ESS decreases the battery discharging current from 1.11A to 0A. The interaction between inverters is shown in

Figure 2.5e. The CAVC AC voltage is decreased by the CAVC output power drop. The VMM compensates the CAVC AC voltage drop by increasing its AC voltage. Also, the ESS participates the compensation of the CAVC voltage drop and reduces a burden on the VMM slightly during battery discharging operation. When the CAVC irradiance rise ($500W/m^2 \rightarrow 1000W/m^2$) is applied, the PV output ramp-rate, $1.61A_{RMS}/s$, is achieved as Figure 2.5b. With the DRRC, 49% of the PV output ramp-rate, $0.79A_{RMS}/s$, is achieved by charging the battery, as presented in Figure 2.5d. The maximum battery charging current is 1.51A. In this case, the PV inverters increase their AC voltage to compensate the inverted ESS AC voltage as Figure 2.5f. Therefore, battery charging operation charges more operating margin of PV inverters. As illustrated in Figure 2.2b, the ramp-rate mismatch occurs due to the differentiation calculation delays. The mismatch errors are from 2% (1-49%/50%×100=2%) to 12% (1-44%/50%×100=12%). Also, small fluctuation of the AC current is observed.

Table 2.3: SUMMARY OF CHIL TEST RESULTS: THE DRRC WITH DIFFERENT OPERATING CONDITIONS.

| Detail conditions | | | | | Changes | | | Without DRRC | | With DRRC | | | Ramp-rate ratio (%) | Inverter limitation |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Modular inverter | | Irradiance level (W/m$^2$) | | | $P_{PV}$ (W) | $I_{PV}$ (A) | $I_{string}$ ($A_{RMS}$) | Time (sec) | Ramp-rate ($A_{RMS}$/s) | Time (sec) | Ramp-rate ($A_{RMS}$/s) | MAX. $I_{batt.}$ (A) | | |
| CAVC | VMM | Type | From | To | | | | | | | | | | |
| ☑ | - | Drop | 1000 | 500 | -122. 1 | -4.6 | -4.07 | 2.72 | -1.50 | 5.82 | -0.70 | 1.11 | 47 | - |
| ☑ | - | Rise | 500 | 1000 | 127.2 | 4.6 | 4.24 | 2.64 | 1.61 | 5.34 | 0.79 | 1.51 | 49 | - |
| - | ☑ | Drop | 1000 | 500 | -127.2 | -4.8 | -4.24 | 2.58 | -1.64 | 5.86 | -0.72 | 1.11 | 44 | - |
| - | ☑ | Rise | 500 | 1000 | 127.2 | 4.6 | 4.24 | 2.84 | 1.49 | 6.56 | 0.65 | 1.35 | 44 | - |
| ☑ | ☑ | Drop | 1000 | 500 | -254.4 | -9.2 | -8.48 | 5.48 | -1.55 | 11.34 | -0.75 | 2.23 | 48 | - |
| ☑ | ☑ | Rise | 500 | 1000 | 254.4 | 9.2 | 8.48 | 5.62 | 1.51 | 11.74 | 0.72 | 2.3 | 48 | - |
| ☑ | - | Rise | 350 | 1000 | 164.4 | 5.3 | 5.48 | 2.88 | 1.90 | 8.16 | 0.67 | 1.6 | 35 | ☑ |
| - | ☑ | Rise | 350 | 1000 | 169.8 | 5.3 | 5.66 | 3.4 | 1.66 | 6.16 | 0.92 | 1.35 | 55 | ☑ |

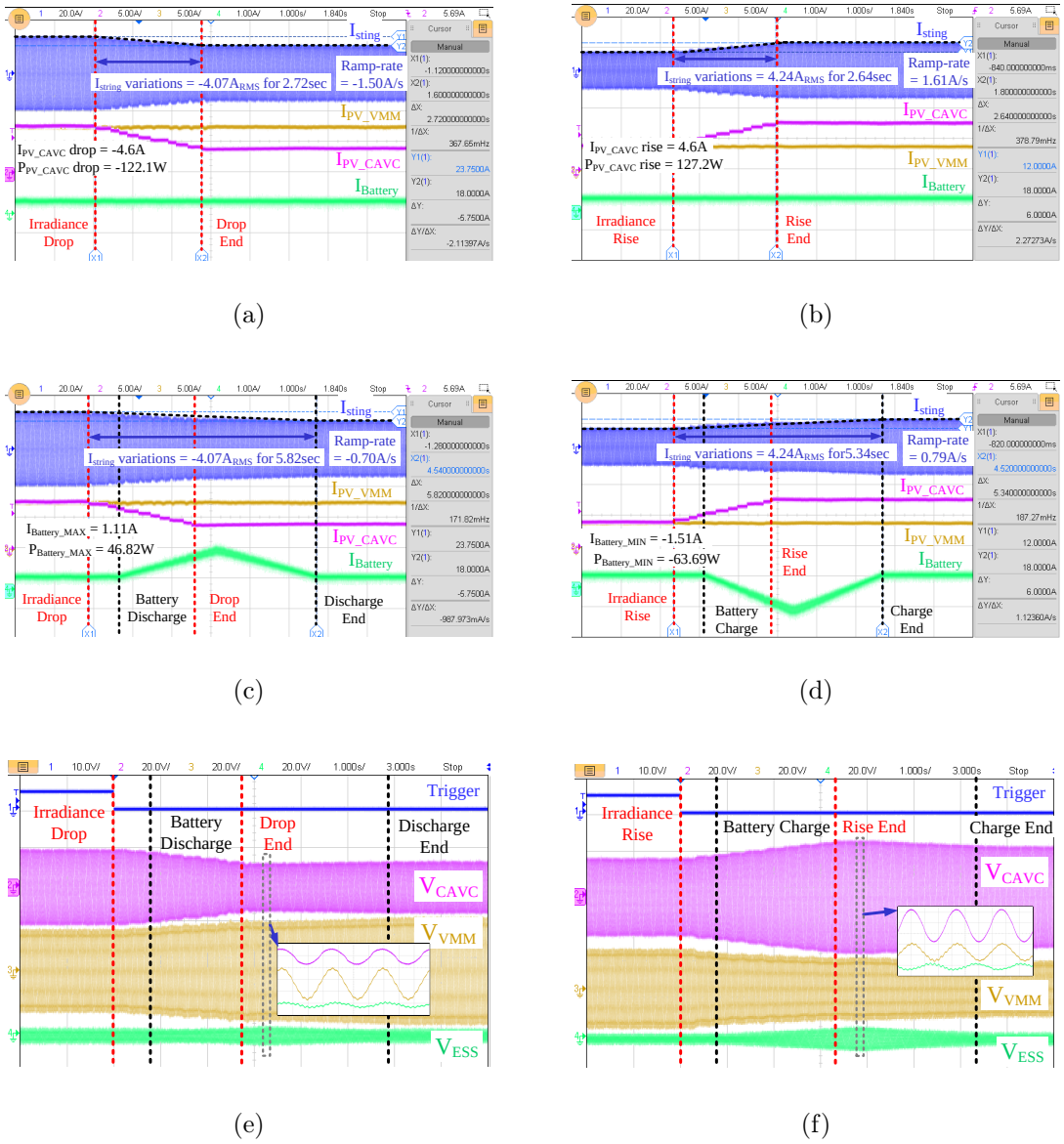


Figure 2.5: DRRC: Asymmetrical irradiance changes on CAVC ($1000W/m^2 \leftrightarrow 500W/m^2$), Ramp-rate factor: 50%, (a) Without DRRC: Irradiance drop, inverter currents, (b) Without DRRC: Irradiance rise, inverter currents, (c) With DRRC: Irradiance drop, inverter currents, (d) With DRRC: Irradiance rise, inverter currents, (e) With DRRC: Irradiance drop, inverter voltages, (f) With DRRC: Irradiance rise, inverter voltages

### 2.4.3 Operating range of the decentralized ramp-rate control

Severe asymmetrical irradiance rise ($350W/m^2 \rightarrow 1000W/m^2$) is applied to the CAVC and the VMM to analyze operating range of the DRRC in the proposed architecture,

as shown in Figure2.6. In case of the CAVC irradiance rise, the AC current distortion occurs in the middle of the slope where two interactions caused by asymmetrical irradiance changes and battery charging mode are overlapped at the same time, as illustrated in Figure2.6c. Since the detection of the PV output change stop is delayed due to the AC current distortion, the DRRC time is extended to 8.16 seconds resulting 35% of the PV output ramp-rate. Therefore, the ramp-rate mismatch error is increased to 30% (1-35%/50%×100=30%). The interaction between inverters is shown in Figure2.6e. The CAVC reaches its maximum AC voltage to cover the VMM AC voltage drop and the inverted ESS AC voltage. In case of the VMM irradiance rise, the limitation of the AC current occurs in the middle of the slope due to the overlapped interactions, as presented in Figure2.6d. Therefore, the VMM moves its operating point from the MPP. This results in the PV current decrease. Since the AC current limitation allows for early detection of the PV output change stop, the DRRC time is shortened to 6.16 seconds resulting 55% of the PV output ramp-rate. Therefore, the negative ramp-rate mismatch error occurs as -10% (1-55%/50%×100=-10%).

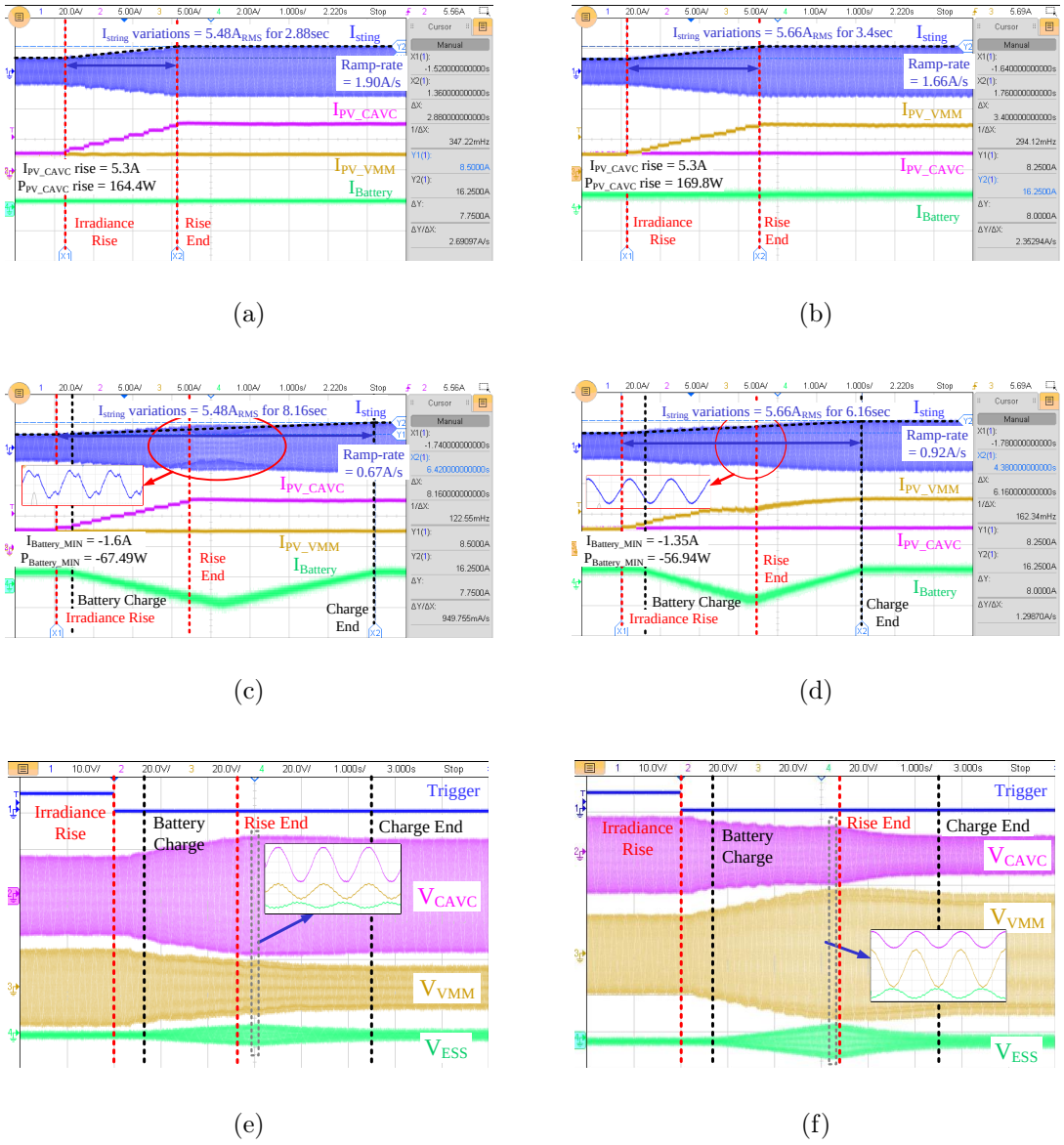


Figure 2.6: DRRC: Severe asymmetrical irradiance changes ($350W/m^2 \rightarrow 1000W/m^2$), Ramp-rate factor: 50%, (a) Without DRRC: On CAVC, inverter currents, (b) Without DRRC: On VMM, inverter currents , (c) With DRRC: On CAVC, inverter currents, (d) With DRRC: On VMM, inverter currents, (e) With DRRC: On CAVC, inverter voltages, (f) With DRRC: On VMM, inverter voltages

## 2.5 Conclusion

This chapter presented a control scheme for the PV-battery AC-stacked inverter architecture and its analysis of system operating range. The PV and ESS inverters' interactive operation and the feasibility of the DRRC were verified through the CHIL

test results. Operation constraints on the constructed architecture were asymmetrical irradiance drop, $320W/m^2$ on CAVC and $250W/m^2$ on VMM, and the -4.6A battery charging current. Operating margins of inverters are critical in designing a reliable inverter architecture. A RRC mitigating PV output variations is a suitable application for the proposed architecture due to the battery charging and discharging limitations caused by the interaction. The DRRC can realize the decentralized control environment and minimize the communication requirements between the inverters. Applying the DRRC, the architecture achieved desired total AC output ramp-rates during the irradiance changes on PV panels. The overlapped interactions (the asymmetrical irradiance level and battery charging mode) affected on the performance of the DRRC. The AC current distortion and early detection of the PV output change stop were observed once the PV inverters use all of their operating margins. Further improvement can be made by implementing PV output curtailment control which can reduce the required amount of the battery charging current.

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# CHAPTER 3: PV-BATTERY SERIES INVERTER ARCHITECTURE: A SOLAR INVERTER FOR SEAMLESS BATTERY INTEGRATION WITH PARTIAL-POWER DC-DC OPTIMIZER

This chapter presents system architecture and control scheme of a photovoltaic (PV) string inverter allowing seamless battery integration with the DC-series integration method. The architecture uses the partial-power processing universal DC-DC optimizer to have flexible power control by regulating the T-node compensation current. The universal optimizer is configured with a dual active bridge DC-DC converter allowing bidirectional power flow and galvanic isolation. Three operation modes are proposed depending on the input sources connected. Based on the operation mode, the universal optimizer and a DC-AC inverter switch their control reference to deliver the maximum PV power and perform battery current control. The steady-state and transient operations of the closed-loop control scheme have been demonstrated through controller hardware-in-the-loop tests to verify feasibility and effectiveness of the PV-battery series inverter architecture.

## 3.1 Introduction

Due to the intermittent nature of solar photovoltaic (PV) energy and concerns regarding the rise of electricity demand, integration of battery energy storage system (ESS) has gained attention as an energy saving solution in residential and commercial grid-tied PV inverter systems [1]-[4]. In PV inverters, legacy PV power electronics topologies [5] are used for integration of a battery ESS, as shown in Figure 1.1: a) AC-parallel integration using a bidirectional grid-tied DC-AC inverter with a battery voltage boosting DC-DC converter [6], b) DC-parallel integration using a bidirectional

DC-DC converter connected to a DC bus with a unidirectional single or cascaded PV DC-DC converters [7], and c) in-line integration inserting a battery to a DC bus directly in parallel [8], and as shown in Figure 2.1: AC-series integration adding a modular bidirectional DC-AC inverter member to an AC string [9], [10]. These integration methods require that a battery ESS has additional voltage-amplification stages such as a DC-DC boost converter or a line-frequency transformer, a high-voltage battery, or restrictions of output power in consideration of interactive operations among inverter members to maintain its grid-connection. These requirements increase system cost and size, lower efficiency, and limit applications of battery ESS. Therefore, it is needed to develop a power electronics topology which relieves these requirements to expedite the integration of battery ESS into grid-tied PV generation system.

This chapter presents a grid-tied PV string inverter allowing seamless battery integration: the PV-battery series inverter architecture. The proposed system adopts the PV-battery DC-series integration method, as shown in Figure 3.1. In this approach, the battery integration does not require additional power electronics stages, a high-voltage battery, or battery power restrictions. Besides, a battery supports the PV string voltage to provide flexibility in delivering the PV string's maximum output power to grid with different system characteristics reducing PV string voltage: for example, a small number of PV panels, solar irradiance drop, ambient temperature rise, and low voltage and low power system design [11], [12]. These benefits are enabled by adopting partial-power processing technique which provides a capability to regulate the T-node compensation current, $I_{comp}$. The proposed architecture uses the partial-power universal DC-DC optimizer working as a current source to offset the battery discharging current and have flexible battery power control. Furthermore, the partial-power universal optimizer requires lower rated power than the state-of-the-art DC-DC converters for PV and battery applications while it handles both PV and battery power [13]-[17]. As the universal optimizer, a dual active bridge (DAB)

DC-DC converter is applied which allows bidirectional power flow, galvanic isolation, a high voltage gain, and soft-switching operation [18], [19].

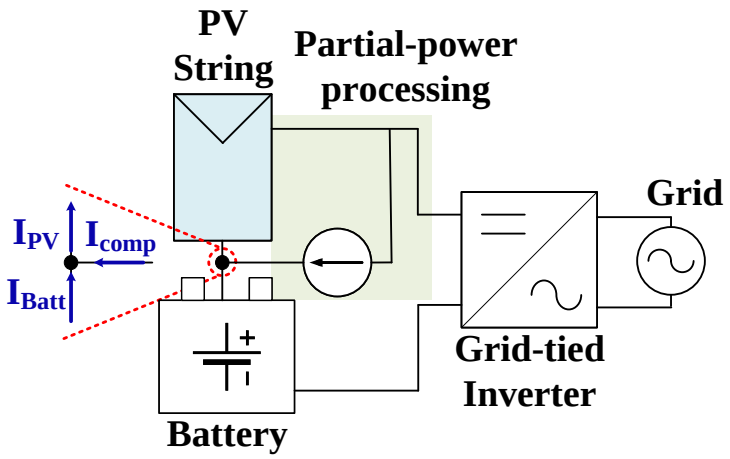



Figure 3.1: The proposed approach: DC-series integration.

The PV-battery series inverter architecture is composed of the universal DC-DC optimizer regulating the T-node compensation current and a grid-tied DC-AC inverter controlling its DC bus voltage. With the seamless battery integration topology, three operation modes are available based on the configurations of the input sources: a) PV-only mode, b) PV-battery mode, and c) battery-only mode. Depending on the operation modes, the universal optimizer coordinates with the DC-AC inverter to meet the system's control objectives: PV maximum power point tracking (MPPT) control and battery current control. The steady-state and transient operations of the closed-loop control have been investigated and demonstrated through the controller hardware-in-the-loop (CHIL) testing to verify the feasibility and the effectiveness of the proposed PV-battery series inverter architecture.

The rest of this chapter is organized and presented as follows. Section II presents the proposed PV-battery integration system architecture. The power electronics topology and its control scheme are proposed in Section III. Section IV provides the results and discussion, and Section V presents the conclusion.

## 3.2 PV-Battery Integration Strategy and System Architecture

The PV-battery series inverter architecture is proposed to achieve seamless battery integration for grid-tied PV inverters. The proposed approach is to connect a battery to a PV string directly in series as shown in Figure 3.1, DC-series integration. This integration does not require a high-voltage battery or additional power electronics stages such as a DC-DC boost converter for a low-voltage battery. Also, a battery supports a PV string in maintaining grid-connection by adding its voltage to the PV voltage. Therefore, voltage amplification stages such as a fully-rated DC-DC boost converter or a line-frequency transformer, the essential devices for the legacy grid-tied PV inverters, are not required to cope with different system characteristics including PV panel installation area, cabling limitations, irregular weather conditions, and different PV voltage and power.

The DC-series integration is enabled by having a current source injecting a DC current into the PV-battery coupling point called T-node. Due to the series connection, the same amount of the DC current passes through the PV string and the battery. Therefore, the battery is discharged as long as the PV string generates output power. Thus, a compensation current needs to be injected into the T-node to offset the battery discharging current. Also, the regulation of the T-node compensation current guarantees flexible battery power control capability as

$$I_{Batt} = I_{PV} - I_{comp} \tag{3.1}$$

where $I_{PV}$ is the PV string current and $I_{Batt}$ is the battery current. Adopting partial-power processing technique [13]-[17], the authors propose the universal optimizer functioning as the T-node current compensator and enabling seamless PV-battery integration. Depending on the configuration of input sources, the proposed universal optimizer has three operation modes.

### 3.2.1 PV-only mode

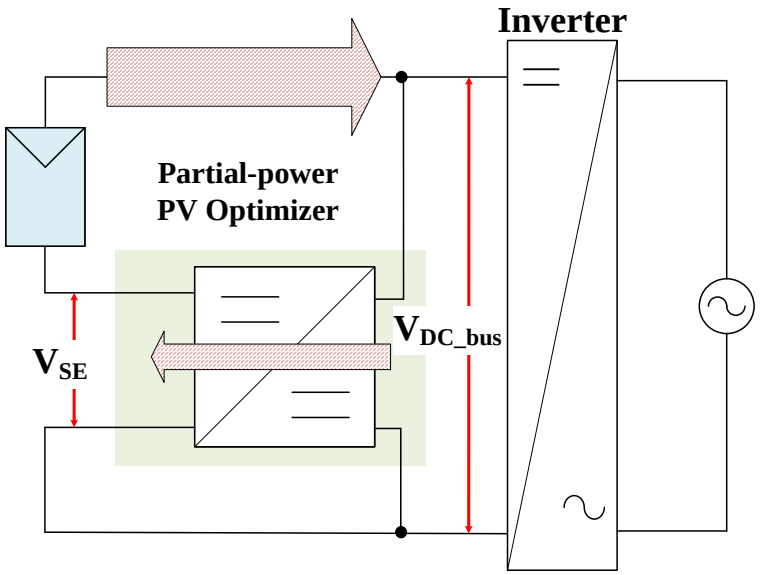
A battery is disconnected from the T-node, as shown in Figure 3.2a. The main operation targets are tracking the PV's maximum power point (MPP) and grid-connection. The partial-power PV optimizer compensates for the DC voltage deficiency caused by the difference between the DC bus voltage, $V_{DC\_bus}$, and the PV voltage, $V_{PV}$, by adding the series voltage, $V_{SE}$, as

$$V_{DC\_bus} = V_{PV} + V_{SE} \tag{3.2}$$

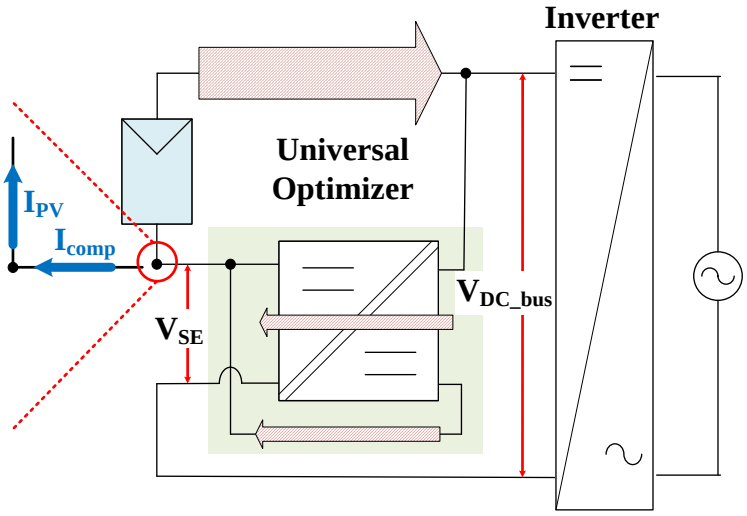
Also, the DC-DC power conversion stage processes only the portion of the PV power through the partial-power processing loop including the DC-DC converter: resulting lower converter rated power and conversion loss to deliver the PV power. The partial-power rate (PPR) for the PV power, $PPR_{PV}$, is proportional to the ratio between the series voltage and the PV voltage as

$$PPR_{PV} = \frac{V_{SE}}{V_{PV}}. \tag{3.3}$$

Besides, further circuit optimization is proposed with improvements in system efficiency and components' voltage stress by achieving partial-power processing for both PV and battery power, as presented in Figure 3.2b: the universal optimizer. The universal optimizer processes the portion of power passing through the partial-power processing loop by having an additional series-connection on the DC bus side with the universal optimizer input voltage and the series voltage. An isolated DC-DC converter topology is adopted to configure the DC bus series-connection. The PPR for the partial-power processing loop power, $PPR_{loop}$, is proportional to the ratio between the PV voltage and the DC bus voltage as




(a)




(b)

Figure 3.2: Development of partial-power universal optimizer in PV-only mode: (a) Partial-power PV optimizer and (b) Universal optimizer.

$$PPR_{loop} = \frac{V_{DC\_bus} - V_{SE}}{V_{DC\_bus}} = \frac{V_{PV}}{V_{DC\_bus}}. \tag{3.4}$$

The total PPR for the PV power, $PPR_{total}$, is achieved with the product of $PPR_{PV}$ and $PPR_{loop}$, and the rated power of the universal optimizer, $P_{optimizer}$, is calculated

with the total PPR and the PV power, $P_{PV}$, as

$$PPR_{total} = PPR_{PV} \cdot PPR_{loop} = \frac{V_{SE}}{V_{PV}} \cdot \frac{V_{PV}}{V_{DC\_bus}} = \frac{V_{SE}}{V_{DC\_bus}} \tag{3.5}$$

$$P_{optimizer} = \frac{P_{PV} \cdot PPR_{total}}{\eta_{converter}} \tag{3.6}$$

where $\eta_{converter}$ is the power efficiency of the DC-DC converter. Due to the decrease of the optimizer rated power, the DC-DC power conversion loss, $P_{loss}$, is reduced, and the DC-DC power conversion efficiency, $\eta_{DC-DC}$, is improved as

$$P_{loss}(\downarrow) = P_{optimizer}(1 - \eta_{converter}) \tag{3.7}$$

$$\eta_{DC-DC}(\uparrow) = \frac{P_{PV} - P_{loss}}{P_{PV}}. \tag{3.8}$$

The remaining power which does not pass through the universal optimizer is delivered to the DC-AC inverter directly.

### 3.2.2 PV-battery mode

Seamless battery integration into the PV system can be achievable by connecting a battery to the open terminals between the PV string and the ground, as shown in Figure 3.3 [20]. The main operation targets of the PV-battery mode are PV MPPT control with extended PV operating range and flexible battery current control. In this configuration, the battery can be used as a power source and a PV voltage supporter simultaneously. Unlike the PV-only mode, the series voltage is enforced to be almost constant by the battery voltage, $V_{Batt}$, as

$$V_{SE} = V_{Batt}. \tag{3.9}$$

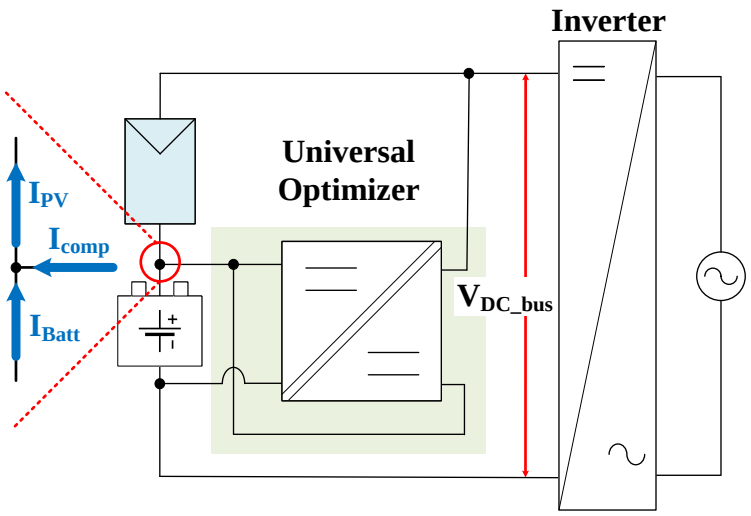



Figure 3.3: The proposed partial-power universal optimizer in PV-battery mode.

Therefore, the battery voltage is added to the PV string voltage to extend the PV operating range. The total PPR of the proposed optimizer is proportional to the battery voltage as follows:

$$PPR_{total} = PPR_{PV} \cdot PPR_{loop} = \frac{V_{Batt}}{V_{PV}} \cdot \frac{V_{PV}}{V_{DC\_bus}} = \frac{V_{Batt}}{V_{DC\_bus}}. \tag{3.10}$$

In the PV-battery mode, there are three sub-operation modes: a) battery zero-current mode, b) battery charging mode, and c) battery discharging mode. The rated power of the universal optimizer varies depending on the sub-operation modes. In the battery zero-current mode, the rated power and the DC-DC power conversion efficiency can be found in the same way with the PV-only mode because the DC-DC conversion stage processes only the PV power. In the battery charging mode, the battery power passes through the partial-power processing loop together with the partial amount of the PV power. The rated power is increased due to the partial amount of the battery power, the product of $-P_{Batt}$ and $PPR_{loop}$, as

$$P_{optimizer(charging)} = \frac{P_{PV} \cdot PPR_{total} - P_{Batt} \cdot PPR_{loop}}{\eta_{converter}}. \tag{3.11}$$

The DC-DC power conversion efficiency is calculated based on the amount of the processed PV and battery power as

$$\eta_{DC-DC} = \begin{cases} \frac{P_{PV}-P_{loss}}{P_{PV}} & P_{PV} \geq P_{Batt} \\ \frac{P_{Batt}}{P_{Batt}+P_{loss}} & P_{PV} < P_{Batt} \end{cases}. \tag{3.12}$$

On the other hand, the battery discharging mode has two ways to deliver the battery power to the grid. Until the battery current becomes the same amount with the PV current, the battery power passes through the PV power loop, the power path across the PV string, and the T-node compensation current is decreased. If the battery current is over than the PV current, only remaining battery power passes through the partial-power processing loop. The rated power and the DC-DC power conversion efficiency are expressed as follows:

$$P_{optimizer(discharging)} = \frac{|P_{PV} \cdot PPR_{PV} - P_{Batt}| \cdot PPR_{loop}}{\eta_{converter}} \tag{3.13}$$

$$\eta_{DC-DC} = \frac{P_{PV} + P_{Batt} - P_{loss}}{P_{PV} + P_{Batt}}. \tag{3.14}$$

### 3.2.3 Battery-only mode

Due to the very low PV voltage or its physical disconnection, the battery-only mode is configured by disconnecting the PV string from the universal optimizer. The main operation target of the battery-only mode is battery current control only. Since the PV current path does not exist, the partial-power processing in the PV-series is not available and $PPR_{PV}$ becomes "1.0". Therefore, only $PPR_{loop}$ is applied to the total PPR, and the rated power and the DC-DC power conversion efficiency can be found as follows:

$$PPR_{total} = PPR_{loop} = \frac{V_{DC\_bus} - V_{Batt}}{V_{DC\_bus}} \tag{3.15}$$

$$P_{optimizer} = \frac{P_{Batt} \cdot PPR_{loop}}{\eta_{converter}} \tag{3.16}$$

$$\eta_{DC-DC} = \frac{P_{Batt}}{P_{Batt} + P_{loss}}. \tag{3.17}$$

## 3.3 Proposed Power Electronics Topology and Control Strategy

The PV-battery series inverter architecture is composed of two power electronics stages: the universal DC-DC optimizer and the grid-tied DC-AC inverter. Figure 3.4 shows the power electronics topology of the universal optimizer. A DAB DC-DC converter is applied because it provides bidirectional power control, galvanic isolation, a high-voltage boosting gain, and soft-switching operation [18], [19]. For the DC-AC inverter stage, a full-bridge single-phase DC-AC inverter is considered.

Also, Figure 3.4 shows the closed-loop control scheme of the proposed architecture in different operation modes. The universal optimizer controls the T-node compensation current by regulating the phase angle difference, $\Psi_{pri-sec}$, between the primary and secondary voltages of the high-frequency transformer [21]. The DC-AC inverter controls the DC bus voltage and maintains grid-connection by regulating the duty cycles of the PWM signals [22]. Based on the operation mode, the universal optimizer coordinates with the DC-AC inverter to achieve the system's control objectives: PV MPPT control and battery current control. The control references of the power electronics units are switched.

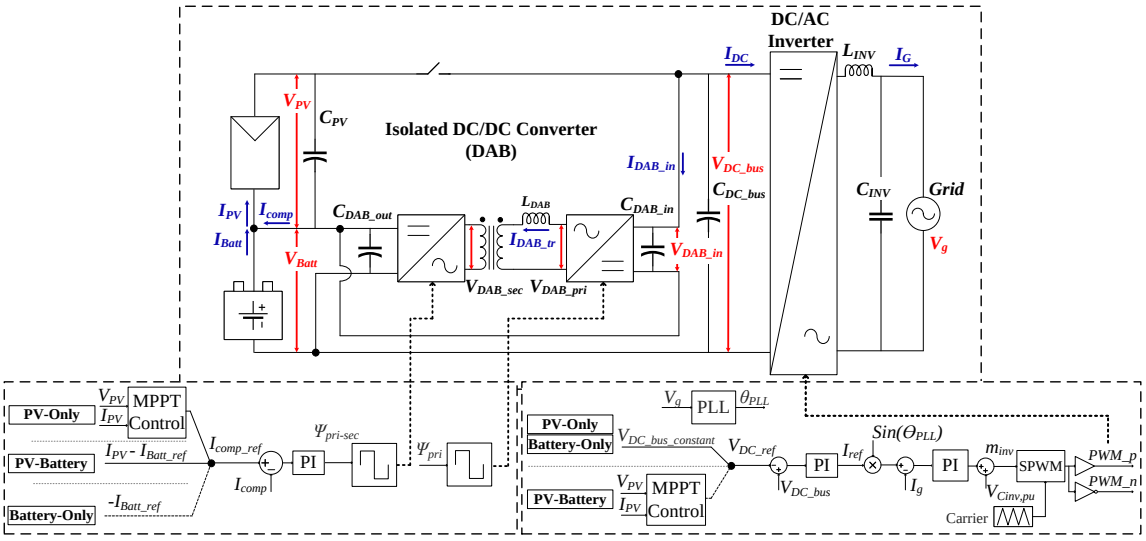



Figure 3.4: Proposed topology for the universal optimizer and control strategy.

### 3.3.1 PV-only mode

The DC-AC inverter maintains a constant DC bus voltage greater or equal to the PV string's open circuit voltage to provide the full range of PV MPPT operation. On the other hand, the universal optimizer performs PV MPPT control by regulating the T-node compensation current which is equal to the PV current. The T-node compensation current reference, $I_{comp\_ref}$, is generated by the perturb and observe (P&O) MPPT control block [23]. As the T-node compensation current increases, the series voltage increases to compensate for the PV voltage drop based on the PV string's V-I curve, as follows:

$$I_{comp\_ref} = I_{MPPT\_CMD} \tag{3.18}$$

$$V_{PV}(\downarrow) + V_{SE}(\uparrow) = V_{DC\_bus}(constant) \tag{3.19}$$

where $I_{MPPT\_CMD}$ is the PV MPPT control command in the PV-only mode.

### 3.3.2 PV-battery mode

Once a battery is connected, the control system can detect the PV-battery mode by monitoring the series voltage which is equal to the output voltage of the optimizer before it starts the switching operation, for example,

$$\begin{cases} PV-Only\ Mode & V_{SE}(orV_{Batt}) < V_{Batt,min} \\ PV-Battery\ Mode & V_{SE}(orV_{Batt}) \geq V_{Batt,min} \end{cases} \tag{3.20}$$

where $V_{Batt,min}$ is the minimum battery voltage which can be detected by the control system. Since the series voltage is equal to the battery voltage, PV MPPT control needs to be performed by the DC-AC inverter. The P&O MPPT control block generates the DC bus voltage reference, $V_{DC\_ref}$, as

$$V_{DC\_ref} = V_{MPPT\_CMD} \tag{3.21}$$

$$V_{DC\_bus}(\downarrow) = V_{PV}(\uparrow) + V_{Batt} \tag{3.22}$$

where $V_{MPPT\_CMD}$ is the PV MPPT control command in the PV-battery mode. The DC bus voltage reference is limited by the peak value of the grid voltage, $\sqrt{2}V_{g\_RMS}$, for grid-connection. In this mode, the universal optimizer regulates the T-node compensation current to perform battery current control as

$$I_{comp\_ref} = I_{PV} - I_{Batt\_ref} \tag{3.23}$$

where $I_{Batt\_ref}$ is the battery current reference.

### 3.3.3 Battery-only mode

The control system can detect the battery-only mode by monitoring the PV string voltage, for example,

$$\begin{cases} Battery-Only\ Mode & V_{PV} < V_{PV,min} \\ PV-Battery\ Mode & V_{PV} \geq V_{PV,min} \end{cases} \tag{3.24}$$

where $V_{PV,min}$ is the threshold PV string voltage for the detection of the battery-only mode.

The DC-AC inverter maintains a constant DC bus voltage to provide the bidirectional rated-power flow under grid-connection. Also, the universal optimizer regulates the T-node compensation current to perform battery current control as

$$I_{comp\_ref} = -I_{Batt\_ref}. \tag{3.25}$$

## 3.4 Results and Discussions

TABLE I presents a case study of the proposed system properties in different operation modes. A 2.5kW $161.5V_{MPP}$ PV string under a nominal weather condition, a 1.0kW 50V battery and single-phase $120V_{RMS}$ AC grid are considered. As the result, the max. 1.4kW optimizer (PPR: 55%) is required to transfer the PV output power: 1.5kW to the grid and 1.0kW to the battery (charging). Since the universal optimizer processes the portion of both the PV and battery power, the battery charging operation requires the maximum rated power. Also, max. 99.6% of the DC-DC

Table 3.1: SYSTEM PROPERTIES - A CASE STUDY OF THE PV-BATTERY SERIES INVERTER ARCHITECTURE (1000 $W/m^2$ AND 25°$C$)

| System Paramters | | | | |
|---|---|---|---|---|
| PV | MPP Power | 2.5kW | | |
| | MPP Voltage. | 161.5V | | |
| Battery | Power | 1.0kW | | |
| | Voltage | 50V | | |
| Grid | Voltage | Single phase, 120$V_{RMS}$ | | |
| A PV/Battery Universal Optimizer | | | | |
| Operation Mode | | PV-only | PV-battery | Battery-only |
| PV Output Voltage | | 161.5V | 161.5V | - |
| Series Voltage | | 38.6V | 50.0V | 50.0V |
| Max. Rated Power ($PPP_{total}$) | | 0.5kW (20%) | 1.4kW (55%) | 0.8kW (22%) |
| Absolute $\eta_{DAB}$ | | 97.5% | 97.5% | 97.5% |
| $\eta_{DC-DC}$ | PV Only | 99.5% | 99.4% | - |
| | Discharging | - | 99.6% | 98.1% |
| | Charging | - | 99.0% | 98.1% |
| A DC-AC Inverter | | | | |
| Rated Power | | 2.5kW | 2.5kW | 2.5kW |
| DC-Link Voltage | | 200V | 211.5V | 200V |
| $\eta_{Inverter}$ | | 98.5% | 98.5% | 98.5% |
| Total Efficiency | | | | |
| $\eta_{TotalC}$ | PV Only | 98.0% | 97.94% | - |
| | Discharging | - | 98.1% | 96.6% |
| | Charging | - | 97.7% | 96.6% |

conversion efficiency during battery discharging operation in the PV-battery mode (+2.1%) and min. 98.1% of the DC-DC conversion efficiency in the battery-only mode (+0.6%) are achieved (when the DAB converter efficiency is assumed as 97.5%).

For the verification of the case study and the control performance of the PV-battery series inverter architecture in different operation modes, a DAB DC-DC converter, a single-phase DC-AC full-bridge inverter, and their closed-loop control scheme are built and run in the CHIL test-bed with a 500ns solution time step real-time power electronics simulator, Typhoon HIL 600, [24] and a 150MHz digital microcontroller, TMS320F28335, as shown in Figure 3.5 The power electronics converters are operated with 10kHz switching frequency to provide clear operation waveform of the DAB phase-shifting control with consideration of the digital-to-analog conversion time response of the real-time power electronics simulator.

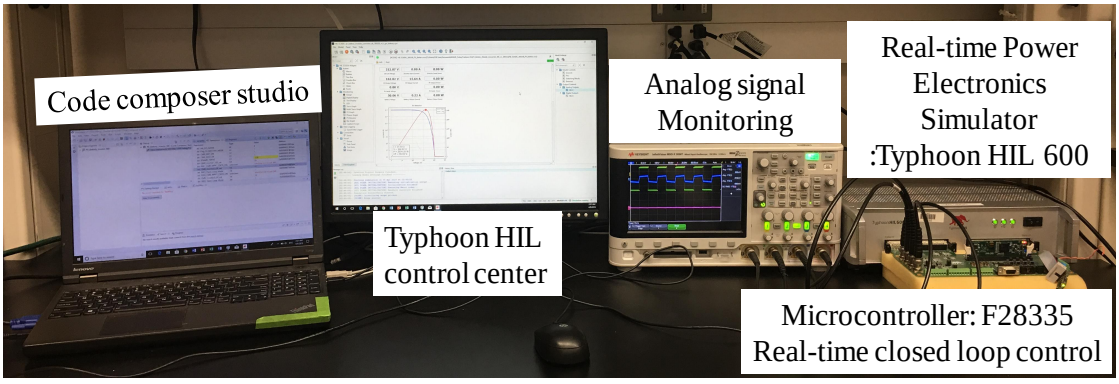


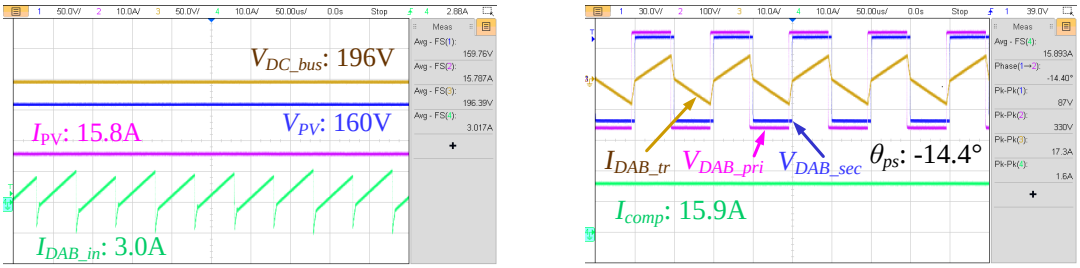

Figure 3.5: CHIL setup for testing the proposed power electronics topology.

### 3.4.1 Steady-state operation

The CHIL experiment results of steady-state operation of the PV-battery series inverter architecture show how the universal optimizer operates in different operation modes.

In the PV-only mode, as shown in Figure 3.6, the DC bus voltage is maintained constant as 196V, the PV string's open circuit voltage, by the DC-AC inverter. To

deliver 2.5kW PV maximum output power to AC grid, the universal optimizer processes 0.5kW (PPR=20%) by regulating the T-node compensation current as 15.9A with $-14.4°$ degrees phase difference.




(a) (b)

Figure 3.6: CHIL experiment results: Steady-state operation of the PV-battery series inverter architecture in the PV-only mode, PV output power: 2.5kW, (a) PV MPPT control and (b) DAB phase-shift control.

In the PV-battery mode, as shown in Figure 3.7, the DC bus voltage is regulated as 207V, the sum of the PV string's MPP voltage and the battery voltage, by the DC-AC inverter to extract 2.5kW PV string's maximum output power. Figure 3.7a and Figure 3.7b show the CHIL results of the battery zero-current mode. The universal optimizer processes 0.6kW rated power (PPR=24%) to maintain 0A battery current which was supposed to be the same with 15.8A PV string current without the T-node compensation current control. $-14.4°$ degrees phase difference is applied to the DAB converter. Due to the differences of the magnitudes of the series voltage and the DC bus voltage between the PV-only mode and the PV-battery mode, the processed power through the universal optimizer is slightly different with the same phase differences.

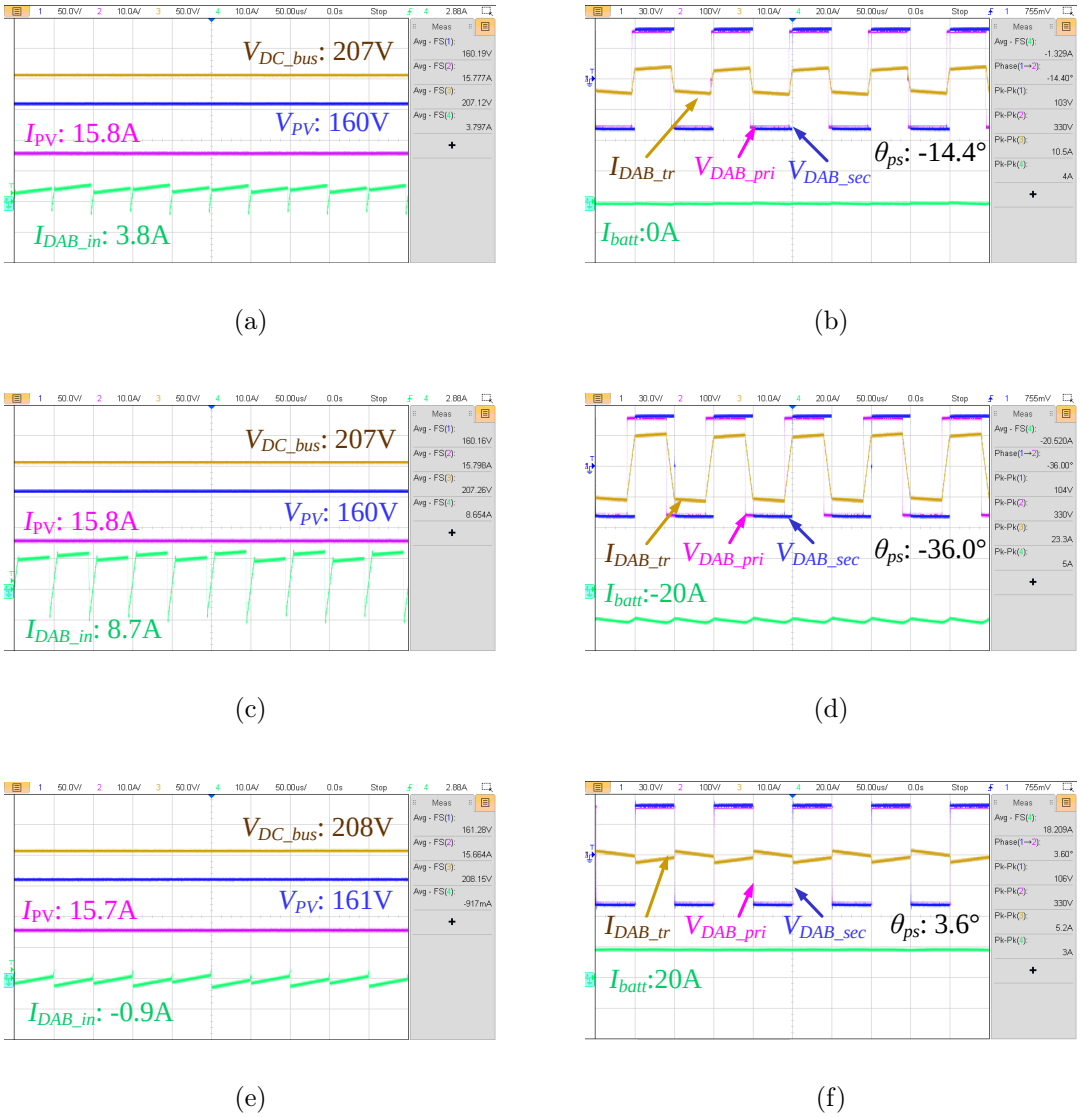



Figure 3.7: CHIL experiment results: Steady-state operation of the PV-battery series inverter architecture in the PV-battery mode, PV output power: 2.5kW (MPPT) and battery output power: ±1kW (battery zero-current mode, battery charging mode, and battery discharging mode); (a) PV MPPT and battery zero-current control, (b) $I_{Batt}$=0A: DAB phase-shift control, (c) PV MPPT and battery charging control, (d) $I_{Batt}$=-20A: DAB phase-shift control, (e) PV MPPT and battery discharging control, (f) $I_{Batt}$=20A: DAB phase-shift control

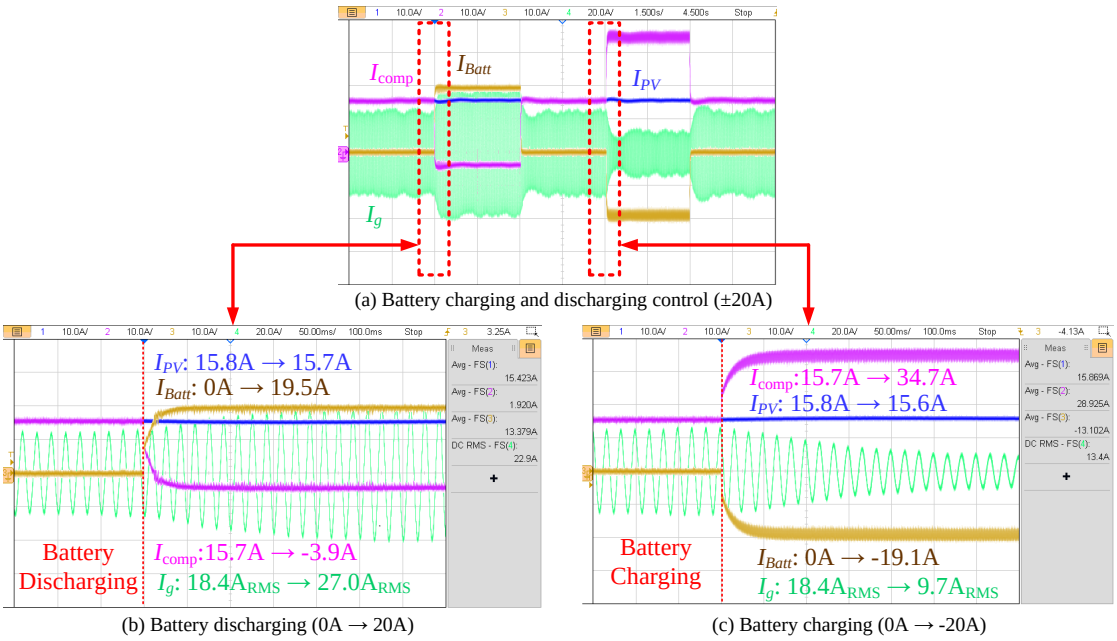
Figure 3.7c and Figure 3.7d show the results of the battery charging mode. By shifting $-36.0°$ degrees phase angle, the battery current is maintained as -20A for 1kW battery charging power. The processed power through the universal optimizer

is 1.4kW (PPR=56%) with 35.8A T-node compensation current. Like the case study, the battery charging mode requires the maximum rated power of the universal optimizer since it processes the portion of both the PV and battery power. Figure 3.7e and Figure 3.7f show the results of the battery discharging mode. In this case, the direction of the phase-shift regulation is reversed. By shifting 3.6° degrees phase angle, the battery current is maintained as 20A, for 1kW battery discharging power. With the amount of the PV current, 15.7A battery current is discharged through the PV power loop and the rest of the battery current, 4.3A, is discharged through the universal optimizer and the battery partial-power processing loop. Therefore, processed power through the universal optimizer is decreased to 0.2kW (PPR=8%).

### 3.4.2 Transient operation

To prove feasibility and performance of the closed-loop control, sudden changes of control reference are investigated.

Figure 3.8 shows the battery current control in the PV-battery mode. Initially, the architecture operates in the battery zero-current mode with 15.8A PV current, 15.7A T-node compensation current, and $18.4A_{RMS}$ AC current. As the transient conditions, changes of the battery current reference from 0A to 20A and from 0A to -20A are applied. As shown in Figure 3.8b, once the battery discharging command is applied, the universal optimizer can reach to the target point, 19.5A battery current, by decreasing the T-node compensation current to -3.9A in 50ms. Also, once the battery charging command is applied, the universal optimizer controls -19.1A battery current, by increasing the T-node compensation current to 34.7A in 50ms, as presented in Figure 3.8c. During transient operations, the PV current is maintained constant as 15.8A by the DC-AC inverter with PV MPPT control. The transient operation verifies the relationship among the PV current, the battery current, and the T-node compensation current, as addressed in (3.18) to (3.23).

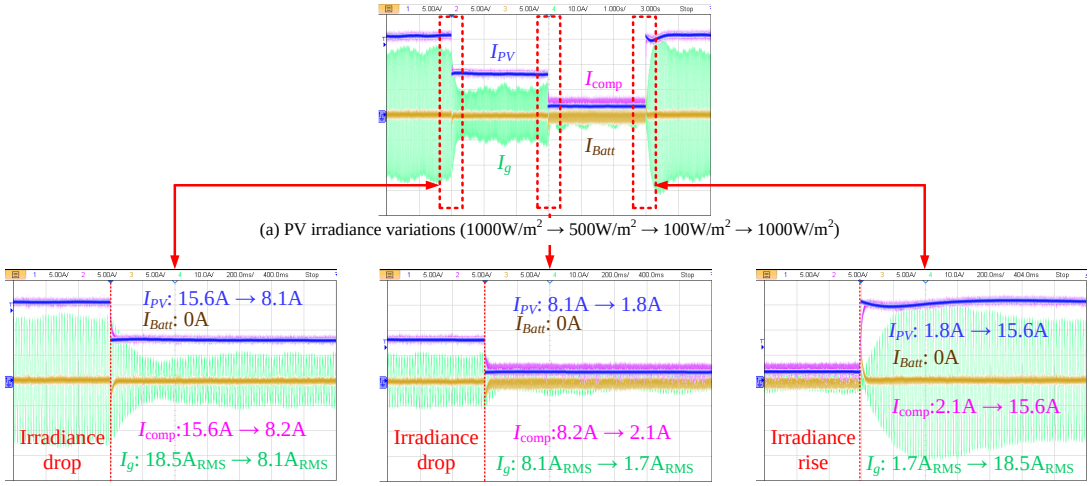



(a) Battery charging and discharging control (±20A)

(b) Battery discharging (0A → 20A)

(c) Battery charging (0A → -20A)

Figure 3.8: CHIL experiment results: Transient operation of the PV-battery series inverter architecture in the PV-battery mode; battery zero-current mode, battery charging mode, and battery discharging mode (PV output power: 2.5kW and battery output power: ±1kW)




(a) PV irradiance variations (1000W/m$^2$ → 500W/m$^2$ → 100W/m$^2$ → 1000W/m$^2$)

(b) Irradiance drop (1000W/m$^2$ → 500W/m$^2$)

(c) Irradiance drop (500W/m$^2$ → 100W/m$^2$)

(d) Irradiance rise (100W/m$^2$ → 1000W/m$^2$)

Figure 3.9: CHIL experiment results: Transient operation of the PV-battery series inverter architecture in the PV-battery mode, PV irradiance variations ($1000W/m^2$ → $500W/m^2$ → $100W/m^2$ → $1000W/m^2$) and battery zero-current mode.

Figure 3.9 shows the PV MPPT control in the PV-battery mode with sudden PV irradiance variations and the battery zero-current control. Once a PV irradiance variation occurs, the PV current changes suddenly based on the PV string's V-I curves. As the result, the battery current is also changed unless the universal optimizer regulates enough T-node compensation current based on the relationship between the three T-node currents (3.1). As shown in Figure 3.9b and Figure 3.9c, once the irradiance drop is applied, the battery charging current appears, and it is compensated by the universal optimizer in 50ms by decreasing the T-node compensation current from 15.6A to 8.2A and from 8.2A to 2.1A, respectively. Also, once the irradiance rise is applied, the battery discharging current appears, and the T-node compensation current is regulated from 2.1A to 15.6A in 50ms, as presented in Figure 3.9d. Also, the transient operation verifies that the proposed architecture provides extended PV operating range with the DC-series integration. Under the different irradiance levels applied, as shown in Figure 3.9, the PV voltage varies from 161.46V to 145.31V. The battery voltage is added to the PV voltage and helps the DC bus satisfies the minimum DC bus voltage, 169.7V, for grid-connection.

## 3.5 Conclusions

This chapter presented system structure and control scheme of the PV-battery series inverter architecture. The DC-series integration with partial-power processing technique allows that a battery can be integrated without additional power electronics stages and support the PV voltage in maintaining grid-connection with different operating conditions. The proposed partial-power DC-DC universal optimizer enables the partial-power processing for both PV and battery power. Therefore, it handled 2.5kW PV power and 1.0kW battery power with 1.4kW rated power. The coordinated closed-loop control between the two power electronics stages was proposed for different operation modes since the controllability of the series voltage is dependent on the battery integration. By switching control objectives of the individual power electron-

ics stages, the PV-battery series inverter architecture achieved flexible battery current control and extended PV MPPT control range. Feasibility and effectiveness of the proposed architecture and the coordinated control scheme were verified through the CHIL tests with the steady-state and the transient operations.

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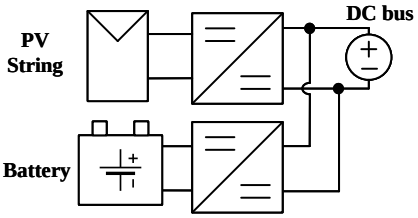
# CHAPTER 4: PV-BATTERY-SERIES DC-DC OPTIMIZER FOR REGULATED DC MICROGRID APPLICATIONS

A DC-series optimizer is developed to integrate a solar photovoltaic (PV) array and a battery energy storage (BES) in series and interface them to a regulated DC microgrid. Due to PV and battery voltage variations, a variable voltage source must be added to the PV-battery DC-series system to be connected to a regulated DC bus. The PV-battery-series DC-DC optimizer is proposed to work as a controllable current source regulating current flow at the PV-battery coupling node and a variable voltage source compensating the voltage difference between the energy sources and the DC bus. The proposed optimizer comprises a triple active bridge DC-DC converter and DC filters. Closed-loop control is developed for PV maximum power point tracking and battery charging and discharging. To handle a 6 kW PV array, a 3 kW BES, and a 3 kW DC load, the proposed optimizer only requires 4.5 kW rated power. This partial power processing also improves round-trip efficiency. DC analysis, simulation, and experimental results demonstrate the operating and design principles and the control performance.

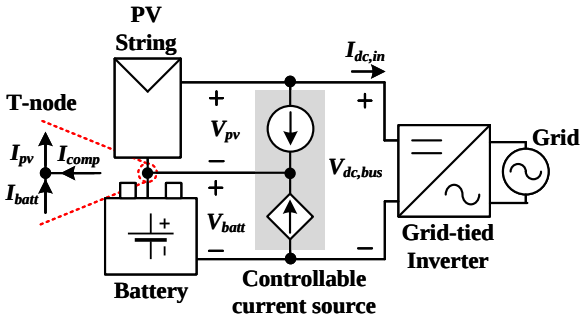
## 4.1 Introduction

Deployment of both solar photovoltaic (PV) and battery energy storage (BES) is growing rapidly in the power system [1], [2]. Integrating solar PV and BES becomes an attractive solution to lower energy costs and increase energy availability with more efficient energy management capabilities. BES also smooths out intermittent PV power and varying electrical loads and supports grid stability and resiliency [3], [4]. Among modern and next-generation electrical grid models, the DC microgrid

incorporating distributed energy sources has been considered as a suitable solution for PV-battery integration because of its high energy conversion efficiency, natural DC interface, and reliable power control [5], [6]. Besides, the DC microgrid allows 200% PV oversizing with the PV-battery integration, which improves the energy usage rate of a PV array with sacrificing less peak energy. For the PV-battery integration in DC microgrids, many works in the literature present DC-parallel-based system configurations [7], [8]. A conventional DC-parallel integration system uses two DC-DC converters connected in parallel to the point of common coupling, a high-voltage DC bus, as shown in Figure 4.1a. This system enables flexible power control between the PV string and the battery. However, it requires two fully rated power electronics converters, leading to bigger system size and higher cost.




(a)




(b)

Figure 4.1: DC-coupling PV-battery integration systems: (a) DC-parallel and (b) DC-series.

DC-series integration has been proposed recently as a new PV-battery integration solution [9]. This novel integration method directly connects a PV array and a BES in series, as shown in Figure 4.1b. This direct integration is enabled by having a controllable current source injecting a compensation current into the PV-battery DC-series coupling node called T-node. The regulation of the compensation current enables the independent control of the PV current and the battery current, which makes PV maximum power point tracking (MPPT) control and battery charging and discharging control available under different operating conditions. The DC-series integration has several benefits compared to the conventional DC-parallel integration:

- PV voltage support: The series connection with a battery supports a PV string to be connected to a high-voltage DC bus with a relatively low PV voltage without using a boost converter.
- Reduction of rated power of power converters: A partial power processing (PPP) converter [10-12] is the only power converter in the DC power processing loop. Therefore, a smaller power converter can be used. Besides, the less processed power, the less power loss. The system efficiency can be improved.
- Single power converter stage: Only a single power converter is used for both a PV array and a BES.
- Seamless integration: Without changing circuit topology, PV-only mode, PV-battery mode, and Battery-only mode are available.

Although the PV-battery DC-series integration has many benefits, it has an application limitation. The voltages of a PV array and a BES vary according to their operating conditions. The PV voltage is dependent on irradiance level, temperature, and MPPT control status. The battery voltage is subject to the state of charge and the loading conditions. As a result, the DC bus voltage—the sum of the PV and battery voltages—needs to be adjusted to satisfy KVL. In contrast, the DC bus voltage

of a regulated DC microgrid is independent of the operating conditions of the PV and the battery and is tightly regulated at a certain voltage level. Thus, the PV-battery DC-series system cannot be directly connected to a regulated DC microgrid.

This chapter presents a modified PV-battery DC-series integration system available for regulated DC microgrid applications and its interfacing power electronics converter called PV-battery-series DC-DC optimizer. The proposed system adds a series voltage source to the PV-battery DC-series system and enables the connection of the DC-series network to a regulated DC bus by compensating for the voltage mismatch between the series-connected sources and the DC bus. The proposed PV-battery-series DC-DC optimizer is a single-stage DC-DC converter interfacing a PV array, a BES, and a DC bus and regulating power among these sources and load. The proposed optimizer works as a controllable current source regulating current flow at the T-node and a variable voltage source compensating for the DC voltage difference. The proposed optimizer comprises a triple active bridge (TAB) DC-DC converter, three DC filter capacitors, and two high-frequency (HF) ripple attenuation inductors. Compared to the conventional DC-parallel integration system, the proposed method reduces the number of power converter stages, reduces the total required rated power of the power converters, and improves round-trip efficiency. The DC-series integration architecture also allows the distribution of the DC voltage rating among the three ports of the TAB converter. Therefore, this approach can also reduce the rated voltage of components such as semiconductor devices and filter capacitors.

The chapter is organized as follows. Section II outlines the configuration and the working principle of the proposed DC-series integration and the PV-battery-series DC-DC optimizer. Besides, DC analysis results are presented to discuss the benefits of the proposed approach. Section III details the converter circuit topology and its design process. Section IV presents closed-loop control and simulation results to verify the control performance and the effectiveness of the system design principle.

Experimental results demonstrating the operating principle of the proposed optimizer and system are shown in Section V. Conclusions are discussed in Section VI.

## 4.2 PV-Battery-Series DC-DC Optimizer

### 4.2.1 DC-Series Integration for a Regulated DC Microgrid

DC-series integration is a new PV-battery integration method that improves a PV-battery integrated power system's power density and round-trip efficiency [9]. Besides, this integration method provides seamless source-configuration capability and a PV voltage support function for a wide PV MPPT range without a boost converter.

Figure 4.1b shows an equivalent circuit diagram of the DC-series integration system connected to a grid-tied inverter. A solar PV string and a battery are directly connected in series, and these series-connected sources are directly connected to the DC bus of the inverter in parallel. In order to control the PV current, $I_{pv}$, and the battery current, $I_{batt}$, independently, a controllable current source is added to the PV-battery coupling node and injects the compensation current, $I_{comp}$, into the T-node. The regulation of the compensation current allows controlling the battery current independently while maintaining the PV maximum power point (MPP) current as

$$I_{batt} = I_{pv} - I_{comp}. \tag{4.1}$$

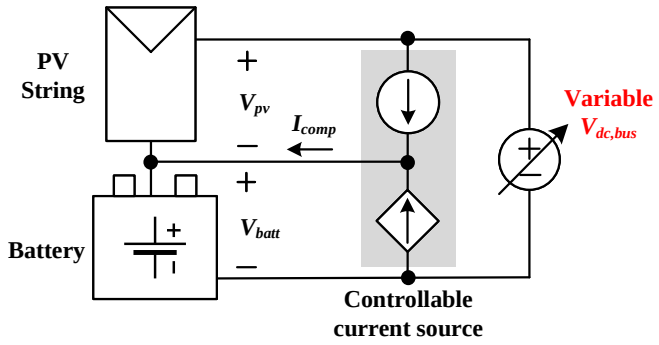
The PV current and voltage are determined according to the PV string's MPP. As the battery voltage, $V_{batt}$, is almost constant, the PV voltage, $V_{pv}$, can be adjusted by the regulation of the DC bus voltage, $V_{dc,bus}$, as

$$V_{pv} + V_{batt} = V_{dc,bus}. \tag{4.2}$$

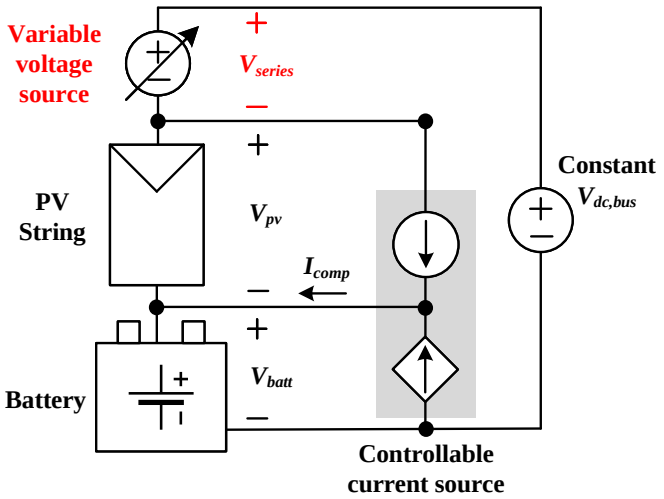
However, this system cannot be directly connected to a regulated DC microgrid—which can be represented as a fixed voltage source—[13]. Voltages of a PV string and a battery vary based on the PV MPPT condition and the battery charging and

discharging condition. Therefore, the DC bus voltage needs to be adjusted according to these operating conditions, as shown in Figure 4.2a and expressed as

$$\widetilde{V}_{dc,bus} = \widetilde{V}_{pv} + \widetilde{V}_{batt}. \tag{4.3}$$




(a)




(b)

Figure 4.2: PV-battery DC-series integrations: (a) connected to a controllable DC bus (a variable DC voltage source) and (b) connected to a fixed DC bus (a constant DC voltage source)

To solve this system restriction, adding a variable voltage source, $V_{series}$, is proposed to compensate for the voltage difference between $V_{pv} + V_{batt}$ and $V_{dc,bus}$, as shown in Figure 4.2b and expressed as

$$\overline{V}_{dc,bus} = \widetilde{V}_{pv} + \widetilde{V}_{batt} + \widetilde{V}_{series}. \tag{4.4}$$

### 4.2.2 PV-Battery-Series DC-DC Optimizer

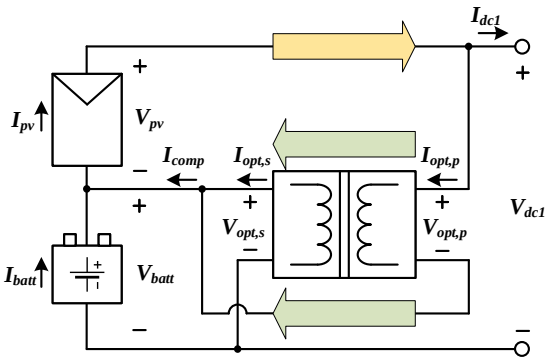
The proposed DC-series integration system needs a power converter working as both the controllable current source and the variable voltage source.

The PV-battery optimizer working as the controllable current source was developed in [9], as shown in Figure 4.3a. An isolated and bidirectional DC-DC converter is used as a PPP converter. The primary side (PS) of the converter is connected across the PV string. The secondary side (SS) is connected across the battery. According to PPP, only a portion of the system power is processed through the PPP converter. The remaining power is transferred directly among the sources and the load. The rated power of the PV-battery optimizer, $P_{opt,pb}$, is expressed as

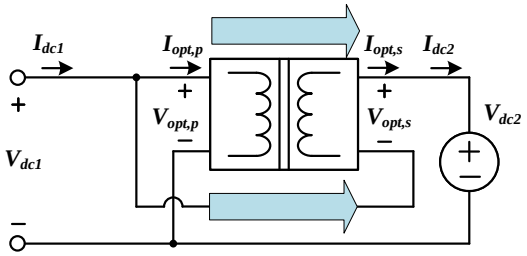
$$P_{opt,pb} = P_{pv}\frac{V_{batt}}{V_{dc1}} - P_{batt}\frac{V_{pv}}{V_{dc1}} \tag{4.5}$$

where $P_{pv}$ is the PV power, $P_{batt}$ is the battery power, and $V_{dc1}$ is the intermediate DC bus voltage.

The variable voltage source can be added to the intermediate DC bus in series using the series-connected boost unit [10]. This power converter is also used for solar PV systems [11] and is widely used as an input-parallel-output-series PPP converter in many applications [12]. Figure 4.3b shows the series optimizer boosting the intermediate DC bus voltage by adding the SS voltage, $V_{opt,s}$, of the isolated and bidirectional DC-DC converter. According to PPP, the rated power of the series optimizer, $P_{opt,series}$, is expressed as




(a)

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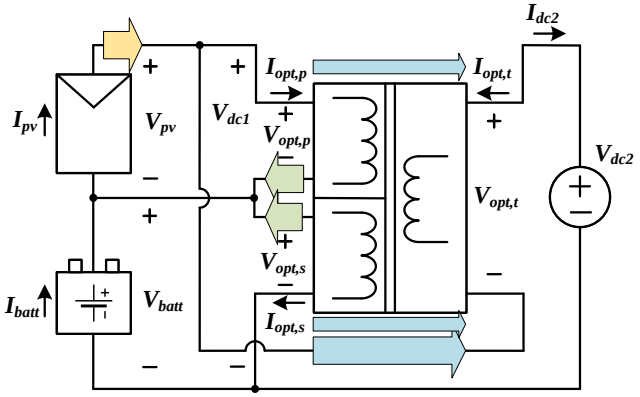



(c)

Figure 4.3: Proposed PV-battery-series DC-DC optimizer topology: (a) PV-battery optimizer, (b) Series optimizer, and (c) PV-battery-series optimizer

$$P_{opt,series} = (P_{pv} + P_{batt})\frac{V_{dc2} - V_{dc1}}{V_{dc2}} \tag{4.6}$$

where $V_{dc2}$ is the output DC bus voltage.

Lastly, these two optimizers are combined as a single power converter unit working as both the controllable current source and the variable voltage source. Figure 4.3c shows the proposed interfacing power converter, the PV-battery-series DC-DC optimizer. A three-port isolated and bidirectional DC-DC converter is used. The proposed optimizer's PS and SS are the same as the PV-battery optimizer. The PV-battery optimizer is stretched out and redrawn. Besides, both the PS and the SS of the proposed optimizer can work as the PS of the series optimizer since the positive terminal of the PS of the proposed optimizer is connected to the positive terminal of the intermediate DC bus, and the negative terminal of the SS of the proposed optimizer is connected to the negative terminal of the intermediate DC bus. Therefore, the PS of the series optimizer can be omitted, and the SS of the series optimizer can be combined with the PV-battery optimizer. As a result, the three-port converter can work as a single unit. The proposed optimizer still has the same PPP loops as the PV-battery optimizer and the series optimizer have. As the rated power of the series optimizer is processed through both the PS and the SS of the proposed optimizer, the power share between them is related to their voltage ratio as

$$P_{opt,pbs,p} = P_{opt,pb} + P_{opt,series}\frac{V_{pv}}{V_{dc1}} \tag{4.7}$$

$$P_{opt,pbs,s} = P_{opt,pb} - P_{opt,series}\frac{V_{batt}}{V_{dc1}} \tag{4.8}$$

where $P_{opt,pbs,p}$ and $P_{opt,pbs,s}$ are the rated power of the PS and the SS of the proposed optimizer, respectively. The rated power of the tertiary side (TS) of the proposed optimizer, $P_{opt,pbs,t}$, is the same as the series optimizer's rated power.

$$P_{opt,pbs,t} = P_{opt,series}. \tag{4.9}$$

### 4.2.3 DC Analysis

DC analysis compares the system design parameters, the required rated power of the power converters, and the system efficiencies between the proposed DC-series and conventional DC-parallel systems to study the impact and effectiveness of the proposed PV-battery-series DC-DC optimizer.

The designed PV-battery integrated system is a 3 kW residential DC microgrid. 6 kW PV array (200% oversizing rate), 3 kW battery, and 380 V DC bus are selected as the design parameters. Table 4.1 lists the designed system parameters. The design is based on the 3 kW PV inverter's datasheet data having two 4.8 kWmax MPP trackers (155-480 $V_{mpp}$, 10 $A_{mpp}$) and showing that the optimal PV voltage is 380 V with the highest efficiency. In the proposed DC-series integration system, five PV panels are connected in series per MPP tracker (1.875 kW). With the voltage support from the battery, the high-voltage requirement of a PV string—to be connected to a high-voltage DC bus—decreases, and instead, the number of MPP trackers increases. This voltage support function helps to optimize the PV array's energy yield by reducing the partial shading effect. The conventional DC-parallel system has eight PV panels in series per MPP tracker (3 kW). This DC analysis assumes that a DC-DC converter has 97.5% efficiency at the rated operating condition. Since a three-port isolated converter topology is used in the proposed optimizer, the efficiency of a full-bridge (FB) module is estimated as 98.5% based on the assumption that an optimally designed dual-active-bridge (DAB) DC-DC converter has 97.5% efficiency. Table 4.2 presents the four system operation cases used for the DC analysis. They are:

Table 4.1: SYSTEM PARAMETERS

| Components | Parameters | Proposed | Conventional |
|---|---|---|---|
| PV panel | Part number | SPV375-R60JWMG | |
| PV String (Single MPP tracker) | Open circuit voltage | 207.5 V | 332 V |
| | Short circuit current | 11.46 A | 11.46 A |
| | MPP voltage | 171.4 V | 274.24 V |
| | MPP current | 10.95 A | 10.95 A |
| | Maximum power | 1.88 kW | 3 kW |
| PV array | # of MPP trackers | 3 | 2 |
| | Maximum power | 5.64 kW | 6 kW |
| Battery module | Part number | BJ DCB105ZKT | |
| Battery | Nominal voltage | 150 V | 150 V |
| | Rated voltage | 161.5 V | 161.5 V |
| | Rated current | 18.6 A | 18.6 A |
| | Rated power | 3 kW | 3 kW |
| DC bus | Rated voltage | 380 V | 380 V |
| | Rated power | 3 kW | 3 kW |
| DC-DC converter | Topology | DAB | DAB or Boost |
| | Estimated efficiency | 97.5% (DAB) | 97.5% |
| | | 98.75% (FB) | |

- Case #1: PV power is the only source providing power to the DC load. 1000 $W/m^2$ irradiance is applied. Due to the PV oversizing, PV curtailment control limits the PV power.

- Case #2: Battery charging command is applied while solar irradiance is 1000 $W/m^2$. PV output power is the maximum (200%). The PV power provides both the battery charging power and the DC load power.

- Case #3: Solar irradiance drops to 100 $W/m^2$ (10%) while continuing battery charging. The available PV output power is less than the battery charging power. The DC bus provides the remaining battery charging power.

- Case #4: Battery discharging command is applied when the PV power is not available. Solar irradiance is 100 $W/m^2$ (10%). The battery provides the DC load. Due to the DC power limit (3 kW), PV curtailment control limits the PV power.

Table 4.2: SYSTEM OPERATION CASES

| # | PV | Battery | DC |
|---|---|---|---|
| 1 | Curtailment - 100% irradiance (3 kW) | Idle (0 kW) | Load (3 kW) |
| 2 | MPPT - 100% irradiance (6 kW) | Charging (-3 kW) | Load (3 kW) |
| 3 | MPPT - 10% irradiance (0.6 kW) | Charging (-3 kW) | Source (-2.4 kW) |
| 4 | Idle (0 kW) | Discharging (3 kW) | Load (3 kW) |

Table 4.3 presents the comparison results between the proposed and conventional PV-battery integration systems. Because of PPP, the rated power of the proposed optimizer is 46.4% less than the rated power of the power converters used in the conventional system. As a result, a 2.8% improvement in round-trip efficiency is achieved. The round-trip is from PV to battery and from battery to DC bus. In addition, the maximum steady-state drain-source voltage of the semiconductor device is reduced to 207.5 V, which is the PV string's open-circuit voltage. The proposed optimizer shares the high DC bus voltage through the three ports with the series configuration. This reduction can contribute to the optimal converter design.

Table 4.3: SYSTEM COMPARISON

| Comparison item | | Proposed | Conventional |
|---|---|---|---|
| Converter's rated power | | 4.45 kW (DAB) + 0.37 kW (FB) | 6 kW (PV DC-DC) + 3 kW (Battery DC-DC) |
| Semiconductor devices' rated drain-source voltage | | 207.5 V | 380 V |
| PV string's maximum open circuit voltage | | 207.5 V (5 series panels) | 332 V (8 series panels) |
| Efficiency | Case 1 | 0.988 | 0.975 |
| | Case 2 | 0.980 | 0.963 |
| | Case 3 | 0.984 | 0.970 |
| | Case 4 | 0.986 | 0.975 |
| | Round-trip (PV-battery-load) | 0.966 | 0.938 |

## 4.3 Converter Circuit and Design

The converter circuit of the proposed PV-battery-series DC-DC optimizer is presented in Figure 4.4. A TAB DC-DC converter—having three FB modules, a three-port HF transformer, and three leakage inductors—is used. The PS FB module is connected to the PV side, the SS FB module is connected to the battery side, and the TS FB module is connected to the series voltage side. The PS and SS FB modules work as a controllable current source regulating the compensation current at the T-node. The TS FB module works as a variable voltage source compensating for the voltage difference between the DC-series node and the DC bus. Passive components—including filter capacitors and HF ripple attenuation inductors—are also designed.

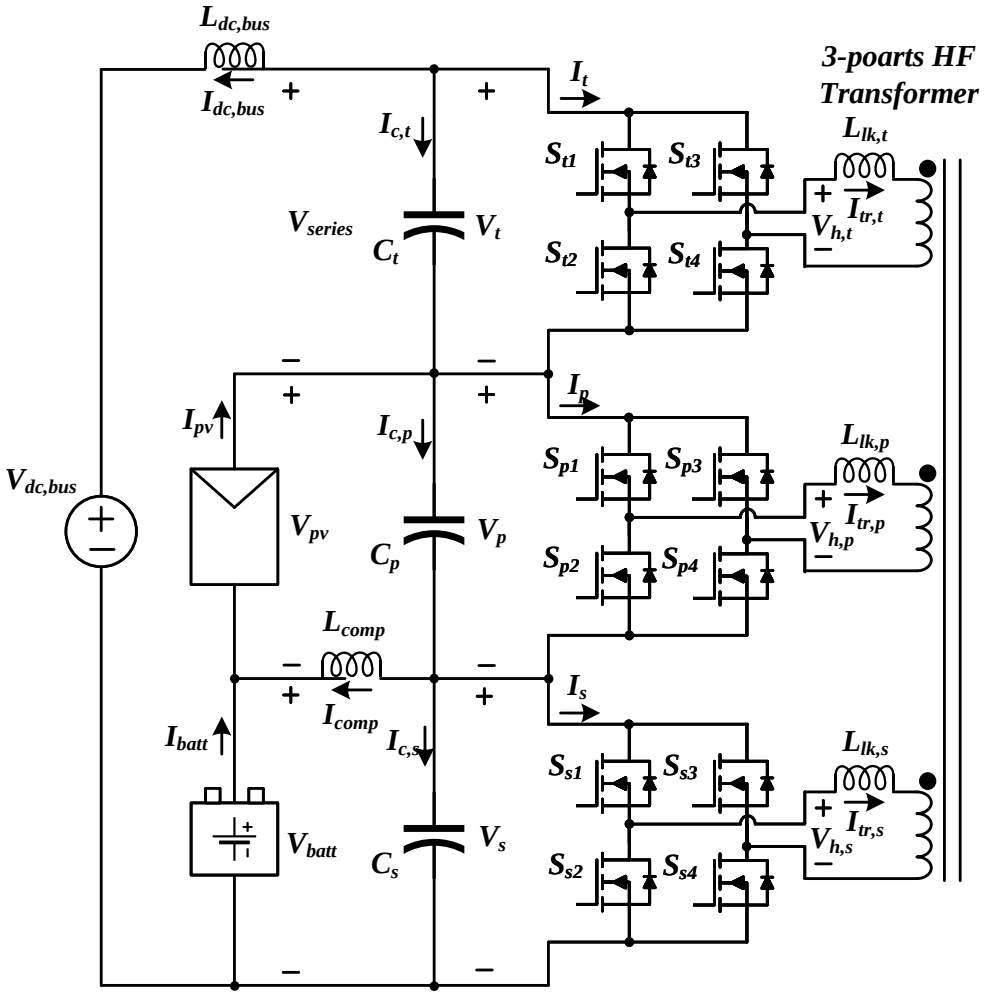



Figure 4.4: Proposed PV-battery-series DC-DC optimizer circuit.

### 4.3.1 HF Three-port Transformer

First, the HF transformer turn ratios are calculated.

$$n_{ps} = \frac{V_{p,mp}}{V_{s,mp}}, n_{pt} = \frac{V_{p,mp}}{V_{t,mp}}, n_{tp} = \frac{V_{t,mp}}{V_{p,mp}} \tag{4.10}$$

where $V_{p,mp}$, $V_{s,mp}$, and $V_{t,mp}$ are the PS, SS, and TS DC voltages under the maximum power condition. $n_{ps}$ and $n_{pt}$ are the transformer turn ratios of the PS to the SS and the PS to the TS, respectively. $n_{tp}$ is the turn ratio of the TS to the PS. The maximum

power condition is where the PV is in MPP, the battery is being charged with full power, and the system provides DC full load.

Next, the three leakage inductances, $L_{lk,p}$, $L_{lk,s}$, and $L_{lk,t}$, are calculated. The leakage inductance is an important parameter determining the amount of maximum power transferred through the transformer. The leakage inductances are calculated from the transformer power equation [14] under the maximum power condition. It is assumed that the magnetizing current is negligible.

$$P_{ps,max} = \frac{n_{ps} V_{p,mp} V_{s,mp} A_{\varphi ps,mp} (1 - A_{\varphi ps,mp})}{2 f_s (L_{lk,p} + {n_{ps}}^2 L_{lk,s})} \tag{4.11}$$

$$L_{lk,p} + {n_{ps}}^2 L_{lk,s} = \frac{n_{ps} V_{p,mp} V_{s,mp} A_{\varphi ps,mp} (1 - A_{\varphi ps,mp})}{2 f_s P_{ps,max}} \tag{4.12}$$

$$P_{pt,max} = \frac{n_{pt} V_{p,mp} V_{t,mp} A_{\varphi pt,mp} (1 - A_{\varphi pt,mp})}{2 f_s (L_{lk,p} + {n_{pt}}^2 L_{lk,t})} \tag{4.13}$$

$$L_{lk,p} + {n_{pt}}^2 L_{lk,t} = \frac{n_{pt} V_{p,mp} V_{t,mp} A_{\varphi pt,mp} (1 - A_{\varphi pt,mp})}{2 f_s P_{pt,max}} \tag{4.14}$$

where $f_s$ is the TAB switching frequency, and $P_{ps,max}$ and $P_{pt,max}$ are the maximum power transferred from the PS to the SS and the PS to the TS, respectively. $A_{\varphi ps,mp}$ and $A_{\varphi pt,mp}$ are the phase-shift modulations between the PS and the SS and between the PS and the TS, respectively. These phase-shift modulations are calculated as

$$A_{\varphi ps,mp} = \frac{\varphi_{ps,mp}}{\pi}, A_{\varphi pt,mp} = \frac{\varphi_{pt,mp}}{\pi} \tag{4.15}$$

where, $\varphi_{ps,mp}$ and $\varphi_{pt,mp}$ are the phase angles between the PS and the SS and between the PS and the TS, respectively. In the maximum power condition, the maximum phase angle, $\pi/2$, is considered.

### 4.3.2 Filter Capacitors

Filter capacitors, $C_p$, $C_s$, and $C_t$, are designed to decouple the double-switching-frequency current ripple from the FB module output currents, $I_p$, $I_s$, and $I_t$. We calculated the capacitor peak current obtained from the transformer peak current and the FB DC average current to calculate the required filter capacitance.

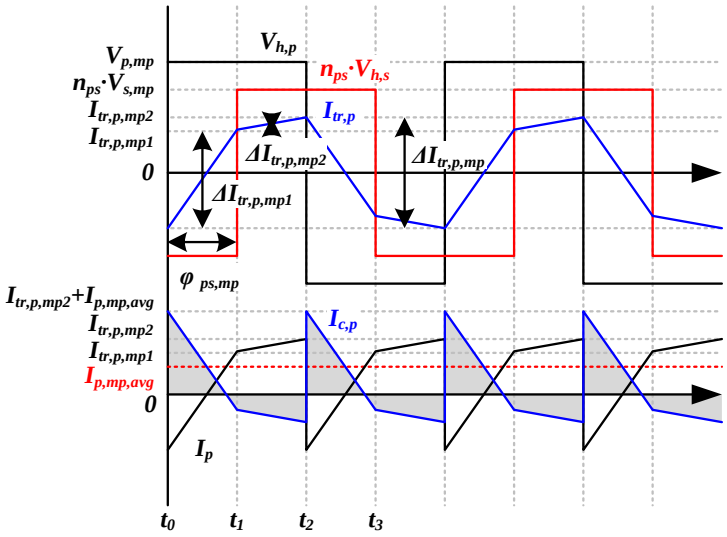
Figure 4.5a shows the PS transformer and filter capacitor current waveforms under the maximum double-switching-frequency current ripple condition where the maximum power is processed through the PS FB module. During the first two intervals, $t_0$-$t_1$ and $t_1$-$t_2$, the transformer current, $I_{tr,p}$, increases and reaches its peak value. The average of these two transformer current variations, $\Delta I_{tr,p,mp1}$ and $\Delta I_{tr,p,mp2}$, is the peak value of the transformer current, $I_{tr,p,mp2}$. It is assumed that the transformer current is balanced. The PS transformer current variations and peak can be calculated as

$$\Delta I_{tr,p,mp1} = \frac{(V_{p,mp} + n_{ps} V_{s,mp}) A_{\varphi ps,mp}}{2 f_s (L_{lk,p} + {n_{ps}}^2 L_{lk,s})} \tag{4.16}$$

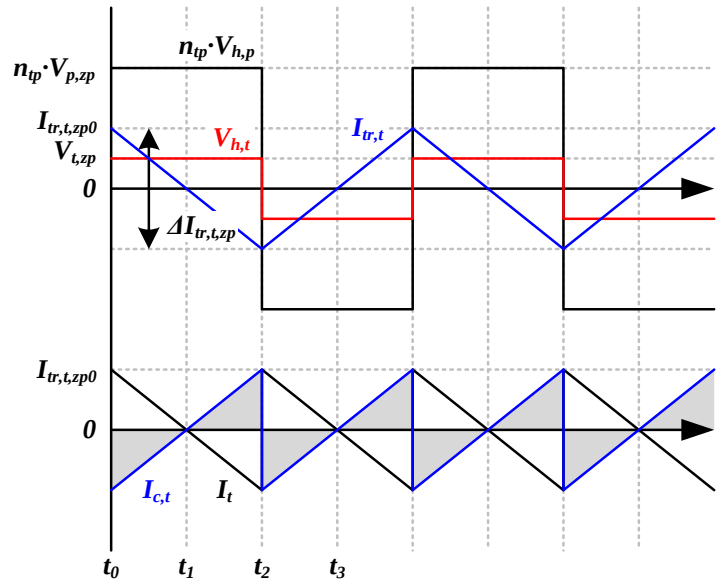
$$\Delta I_{tr,p,mp2} = \frac{(V_{p,mp} - n_{ps} V_{s,mp})(1 - A_{\varphi ps,mp})}{2 f_s (L_{lk,p} + {n_{ps}}^2 L_{lk,s})} \tag{4.17}$$

$$I_{tr,p,mp2} = \frac{\Delta I_{tr,p,mp1} + \Delta I_{tr,p,mp2}}{2} \tag{4.18}$$

The PS FB DC average current is




(a)




(b)

Figure 4.5: TAB transformer voltage and current waveforms (top) and filter capacitor current waveforms (bottom): (a) the PS and (b) the TS.

$$I_{p,mp,avg} = \frac{P_{ps,max}}{V_{p,mp}}. \tag{4.19}$$

The PS capacitor peak current can be calculated by adding the FB DC average current to the transformer peak current. Then, the positive capacitor charge triangle in Figure 4.5a can be used to calculate the filter capacitance with the desired DC voltage ripple ratio, $A_{dv}$, as

$$C_p = C_s = \frac{(I_{tr,p,mp2} + I_{p,mp,avg})A_{\varphi ps,mp}}{4f_s V_{p,mp} A_{dv}}. \tag{4.20}$$

The same capacitance can be selected for the SS filter capacitor since the magnitudes of the capacitor voltage and the capacitor current ripple are similar to those of the PS filter capacitor.

Figure 4.5b shows the TS transformer and filter capacitor current waveforms under the zero-power condition. Under the zero-power condition, the highest TS double-switching-frequency current ripple appears because the highest voltage is applied to the leakage inductance. The TS DC voltage is the minimum, and the PS DC voltage is the maximum—PV open-circuit voltage. During the first two intervals, $t_0$-$t_2$, the transformer current, $I_{tr,t}$, decreases and reaches its negative peak value. The half of this transformer current variation, $\Delta I_{tr,t,zp}$, is the peak value of the transformer current, $I_{tr,t,zp0}$. It is assumed that the transformer current is balanced. The TS transformer current variations and peak can be calculated as

$$\Delta I_{tr,t,zp} = \left| \frac{(V_{t,zp} - n_{tp} V_{p,zp})D}{f_s(L_{lk,t} + {n_{tp}}^2 L_{lk,p})} \right| \tag{4.21}$$

$$I_{tr,t,zp0} = \frac{\Delta I_{tr,t,zp}}{2} \tag{4.22}$$

where $V_{p,zp}$ and $V_{t,zp}$ is the PS and TS DC voltages under the zero-power condition. $D$

is the duty cycle ratio of the PWM signal. The TS FB DC average current is zero in the zero-power condition. The capacitor peak current is the same as the transformer peak current. The positive capacitor charge triangle in Figure 4.5b can be used to calculate the filter capacitance with the desired DC voltage ripple ratio, $A_{dv}$, as

$$C_t = \frac{I_{tr,t,zp0} D}{4 f_s V_{t,mp} A_{dv}}. \tag{4.23}$$

$V_{t,mp}$ is used to select the maximum allowable DC voltage ripple in the TS.

### 4.3.3 HF Ripple Attenuation Inductors

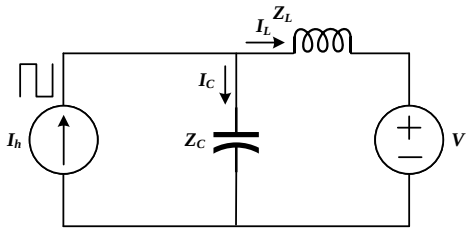
A filter capacitor cannot decouple an HF current ripple properly when connected to an ideal voltage source in parallel. Although the filter capacitor has a low impedance in a certain frequency range, an ideal voltage source has zero impedance in all frequency ranges. Therefore, most of the HF current ripple still flows through the battery and the DC bus that have low impedance.

HF ripple attenuation inductors, $L_{comp}$ and $L_{dc,bus}$, are designed to force the current ripple to flow through the filter capacitors. Figure 4.6a shows an equivalent LC impedance circuit with an HF current source and an ideal voltage source. The inductor adds the impedance, $Z_L$, to the voltage source loop so most of the HF current, $I_h$, can flow through the capacitor impedance, $Z_C$. The current divider circuit equations are derived below:

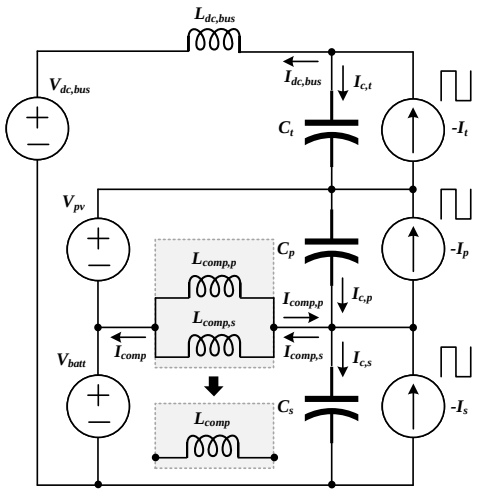
$$I_C = \frac{Z_L}{Z_L + Z_C} I_h, I_L = \frac{Z_C}{Z_L + Z_C} I_h \tag{4.24}$$

where $I_C$ is the capacitor current, and $I_L$ is the inductor current. With the HF ripple attenuation ratio, $A_{atten}$, the required inductance can be calculated as

$$A_{atten} = \frac{I_L}{I_h} = \frac{1}{1 + {\omega_h}^2 LC} \tag{4.25}$$




(a)




(b)

Figure 4.6: HF ripple attenuation inductors: (a) an equivalent LC impedance circuit and (b) implemented HF ripple attenuation inductors in the PV-battery-series optimizer.

$$L_{comp,p} = \left(\frac{1}{A_{atten}} - 1\right) \frac{1}{{\omega_h}^2 C_p} \tag{4.26}$$

$$L_{comp,s} = \left(\frac{1}{A_{atten}} - 1\right) \frac{1}{{\omega_h}^2 C_s} \tag{4.27}$$

$$L_{dc,bus} = \left(\frac{1}{A_{atten}} - 1\right) \frac{1}{{\omega_h}^2 C_t} \tag{4.28}$$

where $\omega_h$ is the angular frequency of the HF current, and $L_{comp,p}$, $L_{comp,s}$, and $L_{dc,bus}$, are the HF ripple attenuation inductors against the PS, SS, and TS filter capacitors, respectively. The locations of these three inductors and HF current flows are illustrated in Figure 4.6b. Since $V_{pv}$ and $V_{batt}$ are connected in series, $L_{comp,p}$ and $L_{comp,s}$ are connected in parallel. Therefore, these two inductors can be combined as

$$L_{comp} = \frac{L_{comp,p} L_{comp,s}}{L_{comp,p} + L_{comp,s}} \tag{4.29}$$

$L_{comp}$ is the total inductance of the combination of $L_{comp,p}$ and $L_{comp,s}$.

### 4.3.4 PV-Battery-Series Optimizer Design Parameters

Table 4.4 lists converter design parameters calculated by using the equations derived above and the system parameters listed in Table 4.1-Table 4.3. As an example of the converter design, a 1.5 kW PV-battery-series optimizer working as a 2 kW PV MPP tracker, a 1 kW BES system, and a 1 kW DC power supply is designed. The 1.5 kW optimizer rated power is selected based on the 4.5 kW converter's rated power calculated for a 6 kW/3 kW PV/battery system having three-MPP trackers, listed in Table 4.3.

The PS and SS FB modules' maximum power selected to calculate the leakage inductance is 2 kW—1.33 times of their 1.5 kW rated power. The TS FB module's maximum power selected is 0.2 kW—1.67 times of its 0.12 kW rated power. This maximum power sizing ensures that the phase-shift modulations do not exceed 0.5 (the absolute maximum level) in the entire system operating range. 20 kHz converter switching frequency is selected. A different switching frequency can be selected for an optimal converter design. 5% of the desired DC voltage ripple ratio and 1% of the HF ripple attenuation ratio are considered for selecting the passive components.

Table 4.4: CONVERTER DESIGN PARAMETERS

| Parameters | Value |
|---|---|
| $V_{p,mp}$ | 171.4 V ($V_{pv,mpp}$) |
| $V_{s,mp}$ | 161.7 V ($V_{batt,rated}$) |
| $V_{t,mp}$ | 46.9 V |
| $V_{p,zp}$ | 207.5 V ($V_{pv,oc}$) |
| $V_{t,zp}$ | 10.8 V |
| $n_{ps}$ | 1 |
| $n_{pt}$ ($n_{tp}$) | 3 (0.33) |
| $P_{ps,max}$ | 2 kW |
| $P_{pt,max}$ | 0.2 kW |
| $f_s$ | 20 kHz |
| D | 0.5 |
| $A_{\varphi ps,mp}$ & $A_{\varphi pt,mp}$ | 0.5 |
| $A_{dv}$ | 0.05 (5%) |
| $A_{atten}$ | 0.01 (1%) |
| $L_{lk,p}$ & $L_{lk,s}$ | 43 uH |
| $L_{lk,t}$ | 79 uH |
| $L_{comp}$ | 30 uH |
| $L_{dc,bus}$ | 60 uH |
| $C_p$ & $C_s$ & $C_t$ | 25 uF |

## 4.4 Closed-Loop Control and Simulation Results

### 4.4.1 Closed-Loop Control

The closed-loop control shown in Figure 4.7 is developed to control the proposed DC-series PV-battery integration system to be in the desired operating states.

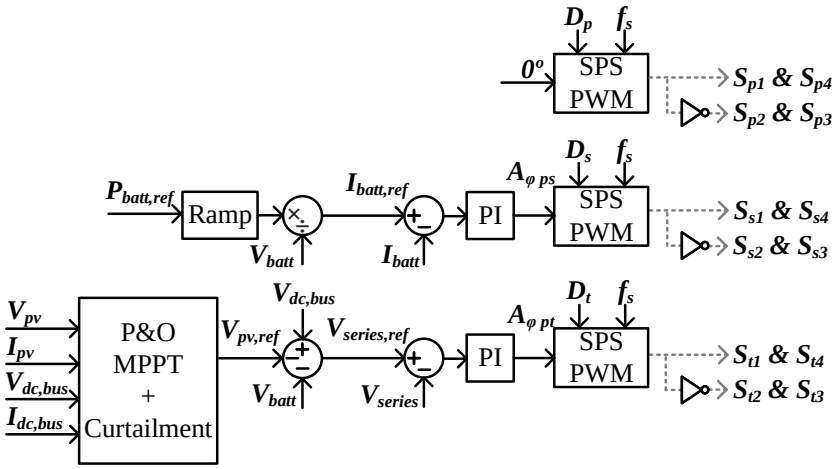



Figure 4.7: SPS PWM based closed-loop control including PV MPPT-plus-Curtailment control, and battery charging and discharging power control.

Single-Phase-Shift (SPS) control—the simplest and most widely used control method for a DAB DC-DC converter [15]—generates PWM signals for the corresponding semiconductor switches in the three FB modules. The SPS control only uses the phase-shift modulation to regulate the power transmission in the HF AC power network. The base PWM duty cycle ratios, $D_p$, $D_s$, and $D_t$, are 0.5. Complimentary PWM signals are applied to two diagonal switch pairs in a FB module to generate an HF square-wave AC voltage. The two phase-shift modulations, $A_{\varphi ps}$ and $A_{\varphi pt}$, referenced to the zero phase-angle of the PS FB square-wave voltage shift the square-wave voltages of the SS and TS FBs.

PV MPPT-plus-Curtailment control is implemented to automatically generate the maximum output power from the PV string and limit the PV output power if the available PV power is more than the sum of the DC load and the battery charging power. A conventional P&O MPPT algorithm is implemented. The curtailment control keeps increasing (perturbation) the PV voltage reference obtained from the P&O MPPT algorithm to move the PV operating point to the right side of the MPP

in the P-V curve if the DC load is higher than the maximum supply power [16], in this case, 1 kW output power. The final PV voltage reference, $V_{pv,ref}$, is used to calculate the series voltage reference, $V_{series,ref}$, as

$$V_{series,ref} = V_{dc,bus} - V_{pv,ref} - V_{batt}. \tag{4.30}$$

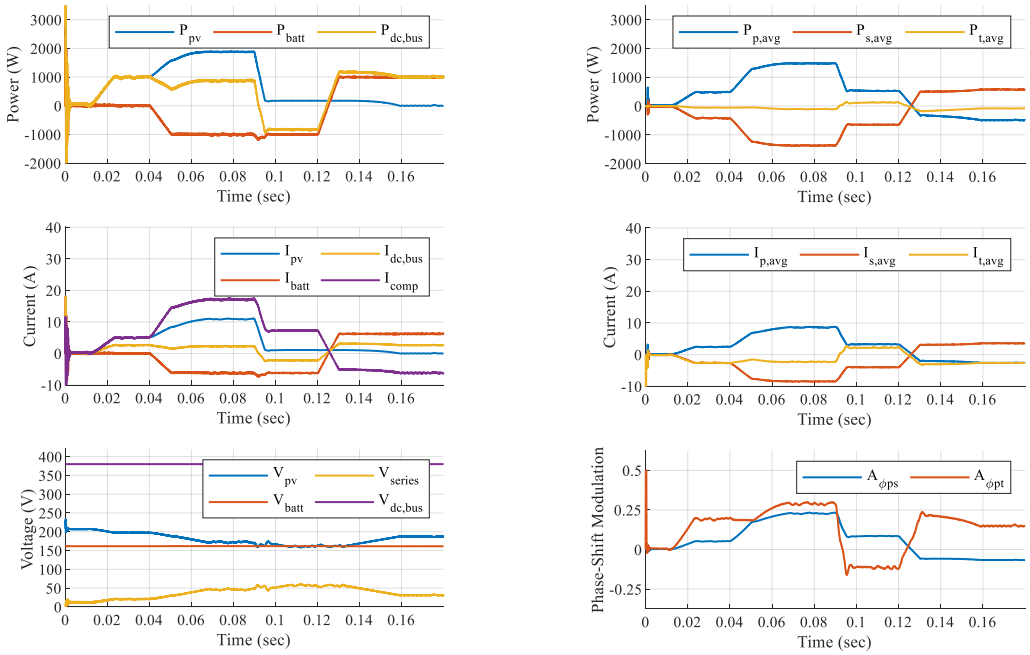
A PI compensator generates the phase-shift modulation between the PS and TS square-wave voltages to control the magnitude of the series voltage.

Battery power control is implemented to regulate the battery charging and discharging current. A PI compensator generates the phase-shift modulation between the PS and SS square-wave voltages to control the magnitude of the battery current according to the battery current reference, $I_{batt,ref}$, calculated by dividing the battery power reference, $P_{batt,ref}$, by the battery voltage. A ramp function is applied to the battery power reference for the smooth transitions.

### 4.4.2 Simulation Results

A MATLAB Simulink simulation model—including the proposed PV-battery-series DC-DC optimizer and its closed-loop control—has been built and run to verify the operating and design principles and the control performance. The converter design parameter values presented in Section III.D are used in this simulation model: a 1.5 kW PV-battery-series optimizer working as a 2 kW PV MPP tracker, a 1 kW BES system, and a 1 kW DC power supply. As the system has been scaled down to a 2 kW/1 kW PV/battery system with a single MPP tracker, the parameter values presented in Table 4.1 are updated.

Figure 4.8 illustrates the simulation results of the four system operation cases presented in Section II.C and Table 4.2. Figure 4.8a shows the DC-series integration system's powers, currents, and voltages. Figure 4.8b shows the PV-battery-series optimizer's powers, currents, and phase-shift modulations.




(a) (b)

Figure 4.8: Simulation results: (a) system power, current, and voltage waveforms and (b) optimizer power, current, and phase-shift modulation waveforms.

- Case #1 (10-40 ms): The PV MPPT control started at 10 ms. The PV voltage decreased from 207 V to 198 V as the series voltage increased from 11.5 V to 20.5 V. To maintain the battery current as 0 A, the compensation current increased from 0 A to 5.1 A, equal to the magnitude of the PV current. Once the DC power reached 1 kW, the curtailment control became active and limit the PV power to 1 kW. Therefore, the PV operating point stayed around 198 V/5.1 A. The powers processed through the optimizer were 0.48 kW (PS), -0.43 kW (SS), and -0.05 kW (TS). The phase-shift modulations increased from 0.00 to 0.05 (PS-SS) and 0.20 (PS-TS) to process these powers.

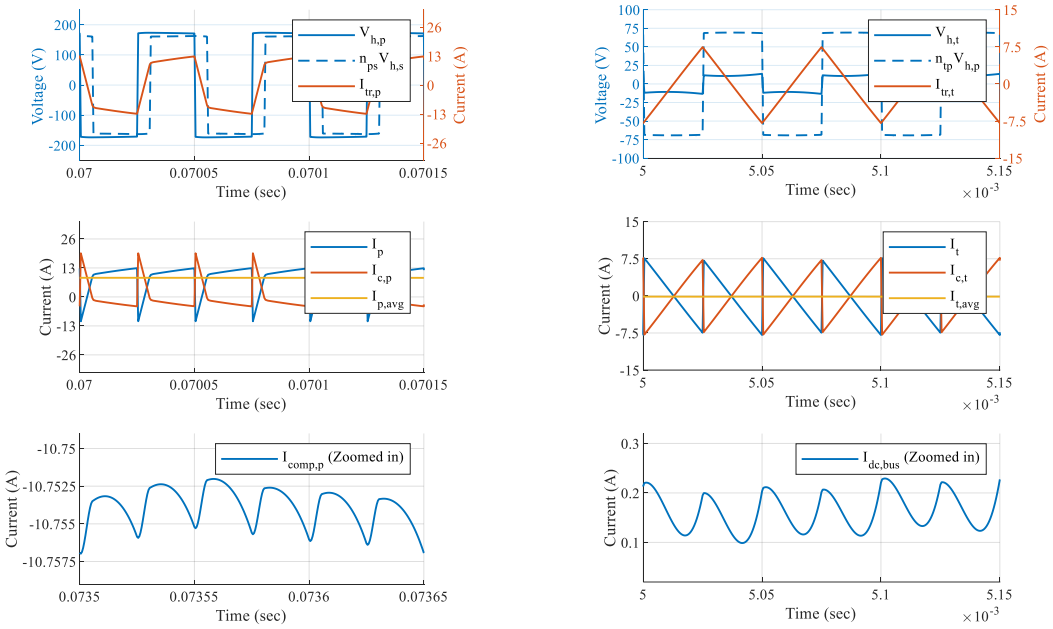
- Case #2 (40-90 ms): The battery full power (1 kW) charging started at 40 ms. The battery current became -6.2 A at 50 ms. As the DC power decreased

because of the battery charging, the PV curtailment control became inactive, and the PV MPPT control increased the series voltage from 20.5V to 47.5 V. As a result, the PV voltage decreased to 171 V that is corresponding to the PV maximum output power, 1.9 kW. The compensation current increased from 5.1 A to 17 A to maintain the 6.2 A battery charging current. The 0.9 kW remaining PV power was converted to the DC power. The powers processed through the optimizer are 1.5 kW (PS), -1.4 kW (SS), and -0.11 kW (TS). The phase-shift modulations increased to 0.23 (PS-SS) and 0.30 (PS-TS) to process these powers.

- Case #3 (90-120 ms): Solar irradiance dropped to 100 $W/m^2$ (10%) at 90 ms. As a result, the PV power decreased to 0.2 kW, and the PV current decreased to 1.1 A. The compensation current decreased to 7.3 A to maintain the 6.2 A battery charging current. As the PV power was less than the battery charging power, the DC bus provided the remaining 0.8 kW to the battery. The powers processed through the optimizer are 0.5 kW (PS), -0.65 kW (SS), and 0.13 kW (TS). The phase-shift modulations increased to 0.09 (PS-SS) and -0.12 (PS-TS) to process these powers.

- Case #4 (120-180 ms): The battery full power (1 kW) discharging started at 120 ms. The battery current became 6.2 A at 130 ms. As the sum of the PV power and the battery power became more than 1 kW, the PV curtailment control became active and limit the PV output power to 0 kW. As a result, the PV voltage went up to 187 V as the series voltage decreased to 31.5 V. The compensation current decreased to -6.2 A. The powers processed through the optimizer are -0.48 kW (PS), 0.56 kW (SS), and -0.08 kW (TS). The phase-shift modulations increased to -0.07 (PS-SS) and 0.15 (PS-TS) to process these powers.

Figure 4.9 illustrates the voltage and the current waveforms of the transformer, FB modules' DC output, filter capacitors, HF ripple attenuation inductors to verify the converter design, especially the selection of the passive components. It is shown that the selected values are effective and suitable. The expected maximum leakage inductor currents, 26 $A_{pk-pk}$ (PS) and 15 $A_{pk-pk}$ (TS), were generated under the maximum and zero power conditions. The filter capacitors and the HF ripple attenuation inductors can decouple the double-switching-frequency current ripple successfully, resulting in almost ripple-free DC currents, 2.9 mA ripple in $I_{comp,p}$ and 0.1 A ripple in $I_{ds,bus}$.




(a) (b)

Figure 4.9: Simulation results: Effect of transformer leakage inductors, filter capacitors, HF ripple attenuation inductors: (a) the PS and (b) the TS.

## 4.5 Experimental Results

### 4.5.1 Hardware Prototype and Experimental Setup

A 400 W hardware prototype has been built to demonstrate the feasibility and the effectiveness of the proposed PV-battery DC-series integration system and the

PV-battery-series DC-DC optimizer. Figure 4.10 shows the built hardware prototype. Three FB daughterboards with four SiC semiconductor devices and their gate driving circuits are installed on the motherboard—from the left, the SS, PS, and TS FB modules. The motherboard has multiple bushing terminals for power circuit configuration, voltage and current sensing circuits for closed-loop control and a TI DSP microcontroller for the digital control interface. A three-port HF transformer, three external leakage inductors, three filter capacitors, two HF ripple attenuation inductors are connected to the power bushing terminals to construct the proposed converter circuit topology illustrated in Figure 4.4. The system parameters are recalculated as listed in Table 4.5. This prototype system is designed for 170 W DC power supply system having a 340 W PV source, a 170 W BES, and a 170 W DC bus. The TI DSP microcontroller board, LAUNCHXL-F28379D, is mounted on the motherboard to provide the phase-shifted PWM signals to the three FB modules and build the closed-loop control system. For this prototype, only the SPS PWM control, the battery current control, and the series voltage control are implemented to show the transient responses to the step changes of the control references. Thus, the PV MPPT-plus-Curtailment control and the battery current ramp function are not implemented here. AMETEK TerraSAS ETS150 Photovoltaic Simulator, a 50 V DC power supply parallel with a DC electric load, and a 130 V DC power supply parallel with a DC electric load are used to emulate the PV array, the BES, and the regulated DC bus, respectively, as shown in Figure 4.11.

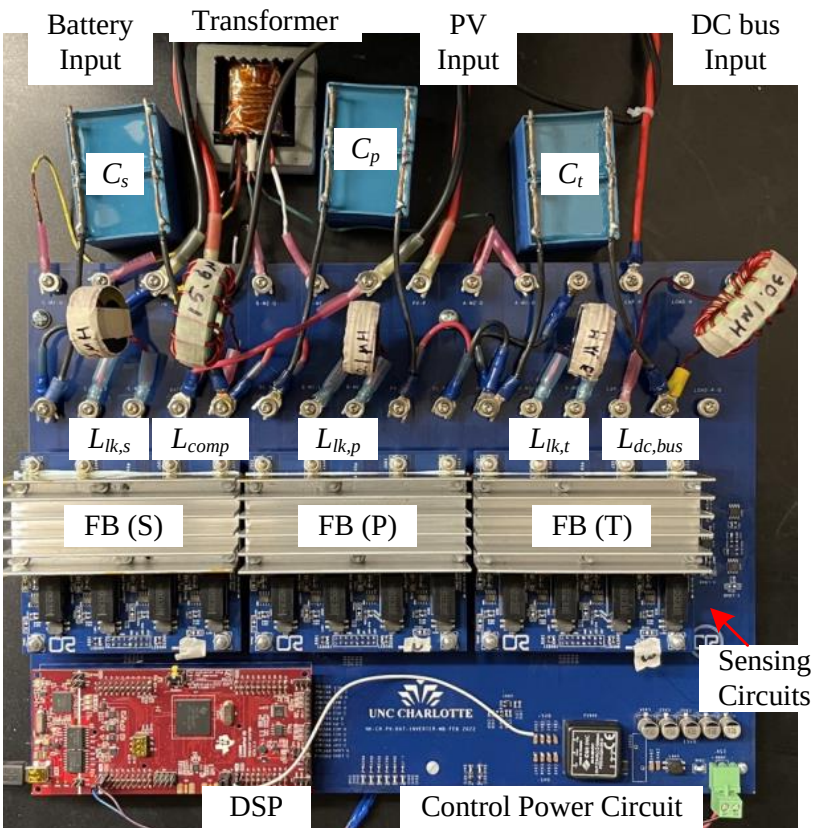



Figure 4.10: Hardware prototype of the proposed system.

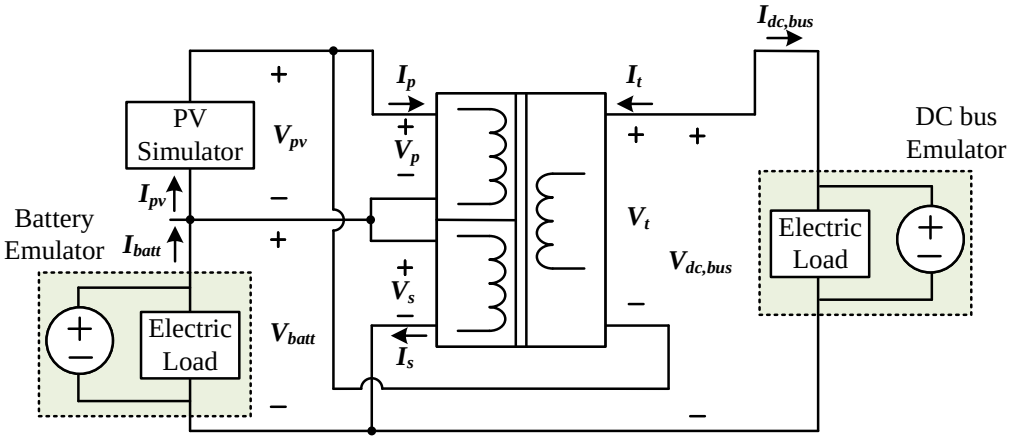



Figure 4.11: Experimental setup.

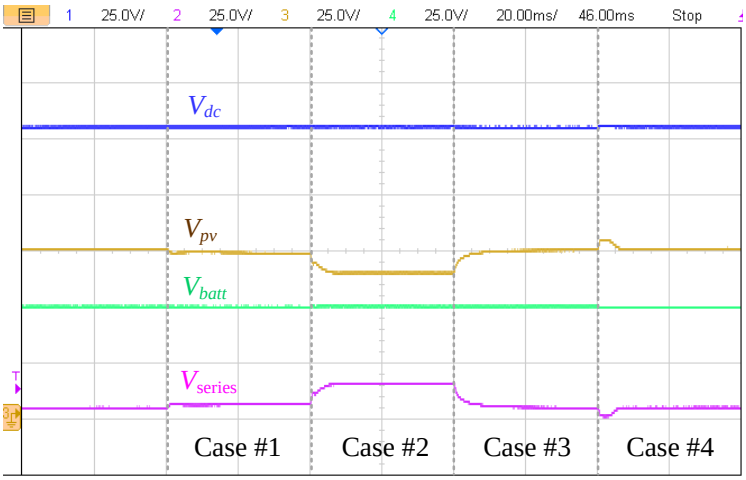
Table 4.5: CONVERTER PROTOTYPE PARAMETERS

| Parameters | | Value |
|---|---|---|
| PV | $V_{pv,oc}$ | 75.6 V |
| | $I_{pv,sc}$ | 5.6 A |
| | $V_{pv,mpp}$ | 62.2 V |
| | $I_{pv,mpp}$ | 5.4 A |
| | $P_{pv,mpp}$ | 339 W |
| Battery | $V_{batt}$ | 50.0 V |
| | $I_{batt,max}$ | 3.4 A |
| | $P_{batt,max}$ | 170 W |
| DC bus | $V_{dc,bus}$ | 13.0 V |
| | $I_{dc,bus,max}$ | 1.3 A |
| | $P_{dc,bus,max}$ | 170 W |
| FB Converter | $f_s$ | 20 kHz |
| Transformer | Turn ratio | 3:3:1 (P:S:T) |
| | $L_{lk,p}$ & $L_{lk,s}$ | 23.6 uH |
| | $L_{lk,t}$ | 21.7 uH |
| Filter Cap. | $C_p$ & $C_s$ & $C_t$ | 58 uF |
| HF A. Inductor | $L_{comp}$ | 15.6 uH |
| | $L_{dc,bus}$ | 30.1 uH |

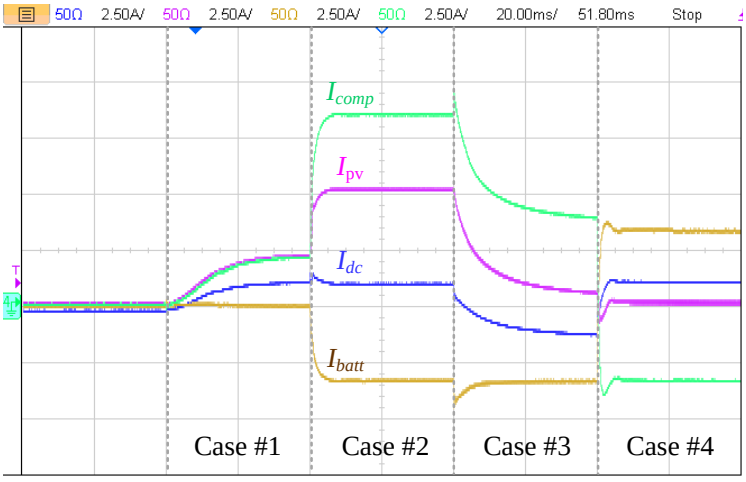
### 4.5.2 Experimental Results

Figure 4.12 presents the oscilloscope captures of the voltage and current waveforms of the proposed DC-series integration system under the four operation cases described in Section II.C and Table 4.2. Instead of decreasing the solar irradiance in Case #3, we increased the PV voltage to reduce the PV output power by reducing the series voltage control reference. The series voltage control reference and the battery current

control reference applied for Case #1-4 are 6.91 V & 0 A, 15.58 V & -3.4 A, 4.90 V & -3.4 A, and 4.90 V & 3.4 A, respectively. The operating status in each case is summarized in Table 4.6. The steady-state results show the system operating behavior aligned with the simulation results described in Section IV.B.




(a)




(b)

Figure 4.12: Experimental results: (a) system voltage waveforms and (b) system current waveforms.

Table 4.6: EXPERIMETNAL RESULTS: VOLTAGE, CURRENT, POWER, EFFICIENCY OF THE PROTOTYPE SYSTEM AND CONVERTER

| | | Cases 1 | Cases 2 | Cases 3 | Cases 4 |
|---|---|---|---|---|---|
| PV | $V_{pv}$ | 73.7 V | 65.0 V | 75.5 V | 76 V |
| | $I_{pv}$ | 2.3 A | 5.3 A | 0.5 A | 0 A |
| | $P_{pv}$ | 170 W | 345 W | 38 W | 0 W |
| Battery | $V_{batt}$ | 50.4 V | 50.6 V | 50.6 V | 50.2 V |
| | $I_{batt}$ | 0.0 A | -3.3 A | -3.4 A | 3.4 A |
| | $P_{batt}$ | 0 W | -167 W | -172 W | 171 W |
| DC bus | $V_{dc,bus}$ | 130.4 V | 130.4 V | 130.2 V | 130.4 V |
| | $I_{dc,bus}$ | 1.1 A | 1.0 A | -1.3 A | 0.9 A |
| | $P_{dc,bus}$ | 143 W | 130 W | -169 W | 117 W |
| FB (P) | $V_{p,avg}$ | 73.3 V | 64.5 V | 75.0 V | 75.5 V |
| | $I_{p,avg}$ | -1.2 A | -4.3 A | -1.8 A | 1.0 A |
| | $P_{p,avg}$ | -88 W | -277 W | -135 W | 76 W |
| FB (S) | $V_{s,avg}$ | 50.0 V | 50.2 V | 50.2 V | 49.8 V |
| | $I_{s,avg}$ | 1.1 A | 4.4 A | 2.1 A | -2.5 A |
| | $P_{s,avg}$ | 55 W | 221 W | 105 W | -125 W |
| FB (T) | $V_{t,avg}$ | 6.3 V | 14.9 V | 4.2 V | 4.3 V |
| | $I_{t,avg}$ | 1.1 A | 1.1 A | -1.3 A | 1.0 A |
| | $P_{t,avg}$ | 7 W | 16 W | -5 W | 4 W |
| System Efficiency | | 0.841 | 0.861 | 0.831 | 0.684 |
| Converter Efficiency | | 0.705 | 0.856 | 0.75 | 0.64 |

The transient-state results show the system control response. Battery current overshoots are observed during the transitions when the direction of the dc bus current changes. This overshoot is caused by the sudden inversion of the phase-shift mod-

ulation between the PS and the TS to switch the power flow direction on the DC bus quickly. Therefore, the phase-shift modulation between the PS and the SS must also be adjusted to change the power processed through the SS FB module. For example, in Case #2, the SS FB module was processing 221 W while the battery charging current was 3.3 A. In Case #3, although the battery charging current was unchanged, the power processed through the SS FB module was decreased to 105 W. This change needs to be made by the battery current controller. Due to this interaction, the system control references need to be changed slowly to avoid unwanted current overshoots. This overshoot issue will not be a concern in the PV-battery integration system because the control references of PV and battery systems are not likely to be changed fast. The solar irradiance and temperature change slowly. The battery current ramp rate is limited.

Figure 4.13 shows the TS current waveforms of the HF transformer, FB DC output, filter capacitor, and HF ripple attenuation inductor under the zero-power condition. This result demonstrates the effectiveness of the filter design presented in Section III. The filter capacitor can decouple the HF current ripple with the help of the HF ripple attenuation inductor. Unlike the simulation, resonant current ripple is observed in the HF current ripple. This resonant current ripple is caused by the interaction of a parasitic loop inductance with the filter capacitor and the decoupling capacitor on the FB module. Although the magnitude of the resonance ripple current is big, it is observed only in the resonance network. This resonant current ripple can be reduced by reducing the loop inductance with optimal layout design between the FB module and the filter network.

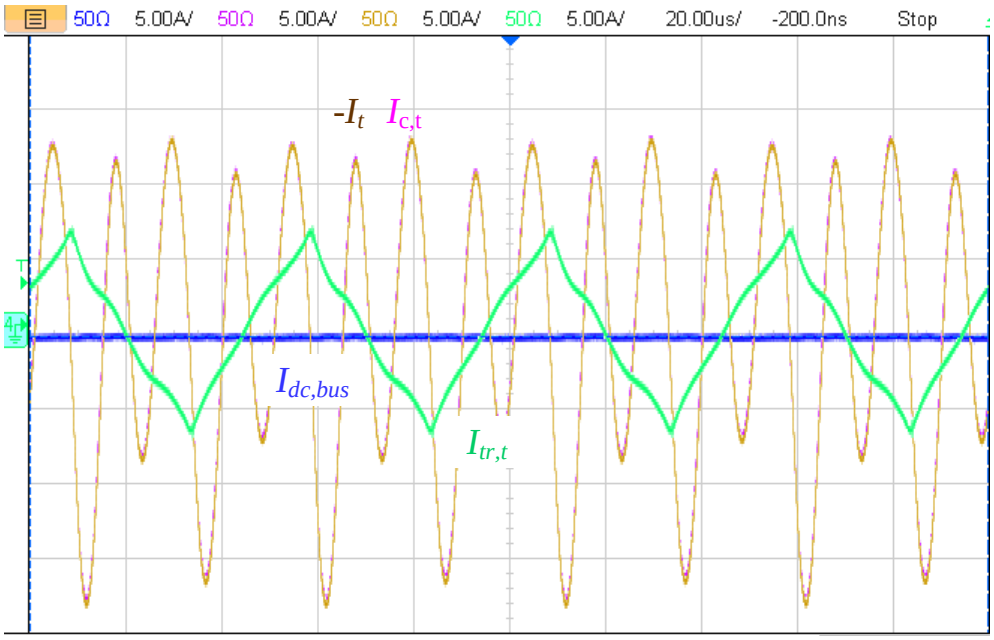



Figure 4.13: Experimental results: Effect of transformer leakage inductors, filter capacitors, HF ripple attenuation inductors in the TS.

Table 4.6 also presents the calculated system and converter efficiencies. Since the prototype is not optimally designed, the measured converter efficiency is low: it varies between 0.640-0.856. However, the final system efficiency is improved because of the PPP, 0.684-0.861.

## 4.6 Conclusion

This chapter presented a modified PV-battery DC-series integration system available for a regulated DC microgrid application and its interfacing power electronics converter called PV-battery-series DC-DC optimizer. The proposed DC-series integration system adds a variable voltage source to the PV-battery DC-series loop to compensate for the voltage difference between the DC bus and the PV and battery energy sources. The PV-battery series DC-DC optimizer composed of a TAB DC-DC converter is developed to work as a controllable current source regulating the com-

pensation current and a variable voltage source regulating the series voltage. The TAB DC-DC converter topology enables interfacing three different DC sources in a single power conversion stage and PPP to improve system efficiency. The proposed system also reduces the voltage requirements for a PV array and a battery to be connected to a high-voltage DC bus. With PPP, the proposed system can use an almost 50%-rated power converter to handle 200% rated PV source, 100% rated BES, and 100% rated DC bus. In addition, the proposed system can improve the round-trip efficiency of the PV-battery integration system. These contributions can finally result in a smaller and cheaper solar-plus-storage system that makes higher revenue. This chapter details the design process of the converter circuit. Besides, it presents the closed-loop control and its simulation results and demonstrates the proposed system's feasibility and effectiveness through the experimental results using the built hardware prototype.

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# CHAPTER 5: CONCLUSION AND FUTURE WORK

## 5.1 Conclusion

This dissertation presented new PV-battery integration methods and series optimizers for residential solar-plus-storage systems. The novel approach of the proposed PV-battery integration methods was based on the series connections of the PV and battery modules in the AC and DC power buses: the PV-battery series integration. The PV-battery series integration reduced the high-voltage system integration requirement that results in higher system cost and size and lower energy efficiency in conventional parallel integration systems. Two PV-battery series integration methods were proposed in this research: AC-series integration and DC-series integration. Besides, three PV-battery series optimizers—the BES decentralized modular DC-AC inverter, the PV-battery DC-DC optimizer, and the PV-battery-series DC-DC optimizer—were proposed to control the power flow in the proposed series integration systems.

This research proposed and investigated the PV-battery AC-stacked inverter architecture based on the AC-series integration method. The AC-stacked inverter architecture allows combining a BES inverter module without the requirements mentioned above since PV inverter modules already support the AC grid voltage requirements for the grid connection. However, this system's BES power rating and applications are restricted because of the interactions among the inverter members during high-power battery charging and asymmetrical PV operating conditions. The operating margin analysis verified the interactive operation between PV and ESS inverters and identified the acceptable operating range. Due to the operation constraints, this system is suitable for mitigating sudden PV power fluctuations, such as PV ramp-rate

control. The decentralized PV ramp-rate control was developed, and the system's capability to reduce the PV ramp rate was verified.

The DC-series integration was proposed for the direct integration of a PV array and a BES. With this direct integration, this system provides PV-battery voltage support and improves system efficiency with a PPP converter—the PV-battery DC-DC optimizer. The proposed optimizer was initially designed to work as a controllable current source regulating the compensation current to control the PV and battery currents separately. It also makes a high-efficient direct-power-processing loop resulting in the reduction of the rated power of the DC-DC converter. As the PV-battery series network is directly connected to the DC bus in parallel, the system cannot be connected to a regulated DC bus such as a DC microgrid.

To solve this issue, the modified DC-series integration method—which inserts a variable voltage source to compensate for the voltage difference with the regulated DC bus—and the PV-battery-series DC-DC optimizer—a single-stage power converter working as both a controllable voltage source and a variable voltage source—were proposed. The hardware prototype composed of a TAB converter was developed, and the operating principle was verified, for the first time. The feasibility and effectiveness of the proposed PV-battery integration methods, the operating and control principles of the proposed PV-battery series optimizers were verified through DC analysis, off-line simulation, real-time CHIL simulation, and experimental results.

## 5.2 Future Work

This work mainly focused on the proof of concept of the newly proposed PV-battery series integration systems. Although the hardware prototype of the PV-battery-series DC-DC optimizer was developed, the prototype was not optimally designed. In this research, the open and reconfigurable hardware structure was preferred over the condensed and optimized hardware design because many design revisions and troubleshooting were expected in the proof-of-concept process. System optimization and

more realistic case studies can be future work. Moreover, the significant impact of the parasitic components in the filter network was observed during the experiments. Also, power loss on the passive components was another concern for hardware prototyping. These practical issues can be handled in the future to show the contributions of the proposed system more effectively. It was also observed that there is control interactions at the series integration coupling nodes. These interactions need to be analyzed to verify the system control stability. In the end, the proposed PV-battery series integration systems are not isolated to the electric grid. In some applications, isolation is mandatory. Further research to develop an isolated PV-battery series integration system needs to be conducted.

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# APPENDIX A: CONTROL AND OPERATING RANGE ANALYSIS OF AN AC-STACKED PV INVERTER ARCHITECTURE INTEGRATED WITH A BATTERY

# Letters

## Control and Operating Range Analysis of an AC-Stacked PV Inverter Architecture Integrated With a Battery

Namwon Kim, *Student Member, IEEE*, and Babak Parkhideh, *Senior Member, IEEE*

***Abstract*—This letter presents a control scheme to operate a battery-integrated ac-stacked photovoltaic (PV) inverter architecture and its operating range analysis. The main operation strategy is the combination of decentralized controls of individual inverter members; PV and battery. In ac-series integration, battery charging and discharging operations affect operating margins of the PV inverter members. The interactive operation needs to be analyzed to identify the system operating range under different conditions. A ramp-rate control, which mitigates PV output variations and improves grid stability, is a suitable application for the PV-battery ac-stacked inverter architecture utilizing a panel-level modular inverter design. In this letter, decentralized ramp-rate control is proposed and demonstrated to analyze the system operating range. The detailed system control and analysis are performed through controller hardware-in-the-loop testing.**

***Index Terms*—AC-stacked PV inverter, battery integration, decentralized ramp-rate control, operating range analysis.**

### I. Introduction

THE ac-stacked photovoltaic (PV) inverter architecture is a panel-level cascaded modular inverter topology suitable for single-phase grid-tied PV applications [1], [2]. High-frequency and low-voltage PV inverter members are stacked in series to satisfy the ac voltage for grid connection and extract maximum output power from individual PV panels. To maximize the architecture's effectiveness, each building block is controlled independently without communications among themselves and with minimum handshaking with the supervisory control center for grid synchronization [2]. Its tangible advantages and capabilities with smart inverter functions are verified through laboratory experiments, controller hardware-in-the-loop (CHIL) testing, and site demonstration in [2]–[7].

In PV applications, integration of a battery into a PV generation system has received significant attention because of the intermittent nature of solar energy sources [8]–[10]. In most of the state-of-the-art battery integration methods, legacy PV power electronics systems [11] are used to configure different integration topologies; 1) ac-parallel [12], [13], 2) dc-parallel [14]–[16], and 3) in-line [17]–[19] integrations. In these integration methods, voltage-amplification power electronics stages or high-voltage battery are required to cope with high dc input voltage requirement of a dc–ac inverter. On the other hand, the ac-stacked PV inverter architecture can integrate a battery without the high voltage requirement by adopting ac-series configuration [20], [21]. Besides, system optimization can be achieved by adding a battery inverter unit into the termination box, which has already been applied to the ac-stacked PV inverter architecture for protection, phase-locked loop, and communication with the supervisory control center [2], [3].

This letter investigates control scheme and operation characteristics of the PV-battery ac-stacked inverter architecture. In this architecture, modular inverter members are cooperating to maintain grid connection and control the ac string power. Therefore, this cooperation introduces interactive operations among the inverter members when the system operating condition varies. Since the interactive operation creates duty cycle changes in the dc–ac inverters, analysis of the inverter members' interaction is required to clarify the operating range of the architecture with battery charging and discharging operation.

Due to the battery charging and discharging limitations caused by the interaction, a ramp-rate control (RRC) is a suitable application for the PV-battery ac-stacked inverter architecture utilizing a panel-level modular inverter design. A RRC mitigates fast-changing, high ramp-rate, PV output variations and regulates the desired ramp-rate of the PV output by controlling the battery charging and discharging current [22]–[25]. Grid stability issues such as voltage and frequency fluctuations caused by high penetration of PV generation in especially weak distribution network can be improved by lowering the PV output ramp-rate. In this letter, the decentralized ramp-rate control (DRRC) using the differentiation of the ac string current as an indicator of PV output variations is proposed to realize the decentralized control environment and minimize the communication requirements between the inverter members [21]. Since the inverter members are connected in series, the differentiation of the ac string current represents both PV and battery output variations when the battery is charged or discharged. Therefore, new criteria to distinguish PV output variations and create the

Manuscript received December 21, 2017; revised February 1, 2018 and April 5, 2018; accepted April 11, 2018. Date of publication April 23, 2018; date of current version September 28, 2018. *(Corresponding author: Namwon Kim.)*

The authors are with the Electrical and Computer Engineering Department, Energy Production and Infrastructure Center, University of North Carolina at Charlotte, Charlotte, NC 28223 USA (e-mail: nkim22@uncc.edu; bparkhideh@uncc.edu).

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Digital Object Identifier 10.1109/TPEL.2018.2829719

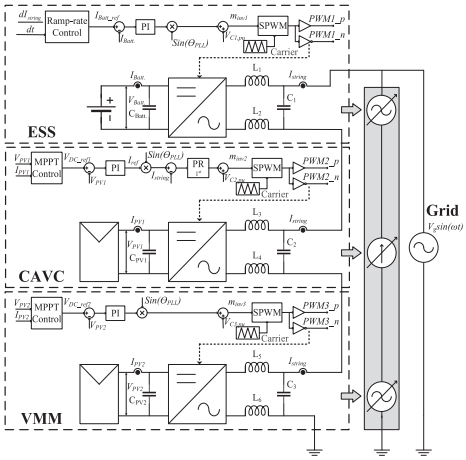



Fig. 1. PV-battery ac-stacked inverter architecture and control diagram.

proper amount of the battery current reference for the DRRC are presented. The control performance of the DRRC and the interactive operation among the inverter members with PV and battery output variations are demonstrated through CHIL testing.

## II. PV-Battery AC-Stacked Inverter Architecture

### A. Proposed PV-Battery AC-Stacked Inverter Architecture

The proposed PV-battery ac-stacked inverter architecture is composed of three different types of modular inverters: 1) current administrator voltage compensator (CAVC), 2) voltage mode members (VMM), and 3) energy storage system (ESS). By stacking or connecting a group of PV inverters in series, the architecture can support the ac grid voltage requirement for grid connection with low-voltage semiconductor devices. Fig. 1 presents the ac-series configuration and the control diagram of the three different types of modular inverters. A CAVC controls its dc input voltage $V_{\mathrm{PV1}}$ with a closed-loop PI controller. A maximum power point tracking (MPPT) control generates the dc input voltage reference to extract the maximum power from the PV panel. Also, the CAVC is responsible for controlling the ac string current $I_{\mathrm{string}}$ with a closed-loop PR controller. A VMM only controls its dc input voltage $V_{\mathrm{PV2}}$ for the MPPT control of its PV panel. Multiple VMMs work as voltage buffers to build up the architecture's ac output voltage. An ESS controls the battery charging and discharging current $I_{\mathrm{Batt.}}$ with a closed-loop PI controller. The proposed RRC generates the battery current reference to mitigating PV output variations. Individual closed-loop controls generate modulation indices $m_{\mathrm{inv1}}$, $m_{\mathrm{inv2}}$, and $m_{\mathrm{inv3}}$ to operate individual inverter members, and the feedforward terms $V_{C1,\mathrm{pu}}$, $V_{C2,\mathrm{pu}}$, and $V_{C3,\mathrm{pu}}$ are applied to improve the system control response and lower the impact of grid disturbances. Details of the RRC strategy are explained in Section III. Since the PV-battery ac-stacked inverter architecture provides the decentralized environment in terms of both physical topology and control, each modular inverter is controlled autonomously by using its local measurements except for grid-synchronization information.

### B. Interactive Operation Between Inverter Members

The main operation principle of the proposed PV-battery ac-stacked inverter architecture is the combination of the decentralized control algorithm of the individual inverter members connected in series. In the ac string where the same ac current $i_{\mathrm{string}}$ is passing through all the inverter members, the inverters' output voltages vary based on the inverter output power. Since the inverters are cooperating to regulate their ac output power in grid connection, one inverter's output power variations may affect others' ac output voltages corresponding to the inverters' operating margin. Therefore, the interaction between the inverters limits the operating range of the architecture.

When asymmetrical irradiance drop is applied to the PV panels, the PV inverter with the low output power decreases its ac output voltage, and it makes other inverters increase their output voltage to compensate the ac voltage drop and track individual maximum power point (MPP), as presented in previous publications [2], [4]. Likewise, battery charging and discharging operations force PV inverters' ac output voltage changes [21]. When battery charging mode is applied to the ESS inverter, the ESS ac voltage appears to be inverted to have negative power flow through the ESS. The inverted ESS ac voltage makes the CAVC and the VMM increase their ac voltages resulting the PV inverters' higher modulation indices. Higher modulation index requests the use of more operating margin for the inverter. If the amount of the compensated ac voltage is higher than the PV inverters' remaining operating margins, the modulation indices reach the maximum amount (1.0), and abnormal operation such as ac current distortion or losing MPPT occurs because the inverters have no room to increase their output voltage more. Different control schemes in the CAVC and the VMM introduce the different abnormal operations, ac current distortion, and losing MPPT control, since the CAVC utilizes sinusoidal ac string current information as the feedback signal for the closed-loop control and the VMM utilizes dc input voltage information. This interaction is required to be considered to design the reliable PV-battery ac-stacked inverter architecture, which has a wide operating range and provides high-quality ac current.

## III. Decentralized Ramp-Rate Control Strategy

In the proposed architecture utilizing a panel-level inverter design, a RRC, which smooths out PV output variations, is a suitable application of the battery integration due to the battery charging and discharging limitations caused by the interaction addressed in the previous section. In this architecture, the ESS determines its battery current reference without handshaking with PV inverters or supervisory control center to achieve decentralized control environment. In the proposed DRRC strategy, the ESS utilizes its local ac string current measurement $i_{\mathrm{string}}(t)$ for detection of PV output variations and battery current calculation. The overall mechanism of the DRRC is shown in Fig. 2(a). The first step is the detection of PV variations with the differentiation of ac string current, as follows:

$$\frac{di_{\mathrm{string\_avg}}\left(t_k\right)}{dt} = \frac{i_{\mathrm{string\_avg}}\left(t_k\right) - i_{\mathrm{string\_avg}}\left(t_{k-1}\right)}{t_k - t_{k-1}} \quad (1)$$

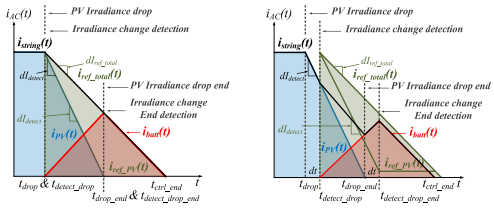



Fig. 2. Illustration of the DRRC algorithm. (a) Ideal case: without detection delay. (b) Practical case: with detection delay.

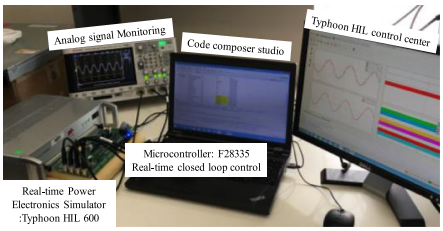



Fig. 3. CHIL set-up for testing a PV-battery ac-stacked inverter system.

where $t_k$ is the time at the $k$th instant, $t_{k-1}$ is the time at the $(k-1)$th instant, $i_{\text{string\_avg}}(t)$ is the rms average of $i_{\text{string}}(t)$, and $dI_{\text{string\_avg}}(t)$ is the ac current difference. To ignore small variations caused by the MPPT control, a dead band $dI_{\text{limit}}$ is applied, as follows:

$$dI_{\text{detect}} = \begin{cases} dI_{\text{string\_avg}}\left(t_{\text{detect\_drop}}\right), & dI_{\text{string\_avg}}\left(t_{\text{detect\_drop}}\right) > dI_{\text{limit}} \\ 0, & dI_{\text{string\_avg}}\left(t_{\text{detect\_drop}}\right) \le dI_{\text{limit}} \end{cases} \tag{2}$$

where $t_{\text{detect\_drop}}$ is the moment when PV output variation is detected, $dI_{\text{string\_avg}}(t_{\text{detect\_drop}})$ is the ac string current difference at $t_{\text{detect\_drop}}$, and $dI_{\text{detect}}$ is the PV output change detected.

The ESS will start to charge or discharge the battery to achieve the desired ramp-rate of the inverter architecture's output once the PV output variation is detected. In the proposed architecture, a criterion to distinguish the PV output changes from the total ac string output power is required for the decision of the ESS output current since the output of the ESS also affects the differentiation of the ac string current due to the series connection. As shown in Fig. 2(a), two current references $i_{\text{ref\_PV}}(t)$ and $i_{\text{ref\_total}}(t)$ are generated with two different ramp-rates; the detected PV output ramp-rate $dI_{\text{detect}}$ and the desired architecture's output ramp-rate $dI_{\text{ref\_total}}$, respectively, as follows:

$$i_{\text{ref\_PV}}\left(t_k\right) = i_{\text{ref\_PV}}\left(t_{k-1}\right) + \frac{dI_{\text{detect}}}{dt} \times T_{\text{step}} \tag{3}$$

$$i_{\text{ref\_total}}\left(t_k\right) = i_{\text{ref\_total}}\left(t_{k-1}\right) + \frac{dI_{\text{ref\_total}}}{dt} \times T_{\text{step}} \tag{4}$$

$$dI_{\text{ref\_total}} = dI_{\text{detect}} \times k_{\text{ramp\_rate\_total}} \tag{5}$$

where $T_{\text{step}}$ is the controller time step and $k_{\text{ramp\_rate\_total}}$ is the ramp-rate gain (0.1–1). By subtracting $i_{\text{ref\_PV}}(t)$ from $i_{\text{ref\_total}}(t)$, the battery current reference $i_{\text{batt}}(t)$ can be calculated, and its absolute value $|i_{\text{batt}}(t)|$ is increased until the moment of PV output variations stop denoted as $t_{\text{drop\_end}}$. After $t_{\text{drop\_end}}$, $i_{\text{ref\_PV}}(t)$ is set as constant by forcing $dI_{\text{detect}}$ zero, and $|i_{\text{batt}}(t)|$ decreases constantly until it becomes zero $t_{\text{ctrl\_end}}$, as follows:

$$i_{\text{batt}}\left(t_k\right) = \begin{cases} \left(i_{\text{ref\_total}}\left(t_k\right) - i_{\text{ref\_PV}}\left(t_k\right)\right) \times k_{\text{ac to dc}}, \\ \qquad t_k \le t_{\text{detect\_drop\_end}} \\ \left(i_{\text{ref\_total}}\left(t_k\right) - i_{\text{ref\_PV}}\left(t_{\text{detect\_drop\_end}}\right)\right) \times k_{\text{ac to dc}}, \\ \qquad t_{\text{detect\_drop\_end}} < t_k \le t_{\text{ctrl\_end}} \end{cases} \tag{6}$$

TABLE I
DESIGN PROPERTIES OF THE PV-BATTERY AC-STACKED INVERTER

| System specifications | | |
|---|---|---|
| Grid | | |
| Voltage | $V_g$ ($V_{RMS}$) | 30 |
| PV panel | | |
| MPPT: Power (1000W/m$^2$) | $P_{MPP}$ (W) | 255.10 |
| MPPT: Voltage (1000W/m$^2$) | $V_{MPP}$ (V) | 33.45 |
| MPPT: Current (1000W/m$^2$) | $I_{MPP}$ (V) | 7.63 |
| Battery | | |
| Nominal voltage | $V_{Battery}$ (V) | 42.2 |
| Capacity | $C_{Battery}$ (Ah) | 20 |

where $k_{\text{ac to dc}}$ is the ac-to-dc current gain and $t_{\text{detect\_drop\_end}}$ is the moment when the ESS detects PV output variation stop. The detection of PV output variation stop is achieved by monitoring the differentiation of the ac current, as follows:

$$|i_{\text{batt}}\left(t_k\right)| \text{ decreases,}$$
$$\text{if} \begin{cases} \frac{di_{\text{string\_avg}}(t_k)}{dt} \le 0, & \text{Charging mode} \\ \frac{di_{\text{string\_avg}}(t_k)}{dt} \ge 0, & \text{Discharging mode.} \end{cases} \tag{7}$$

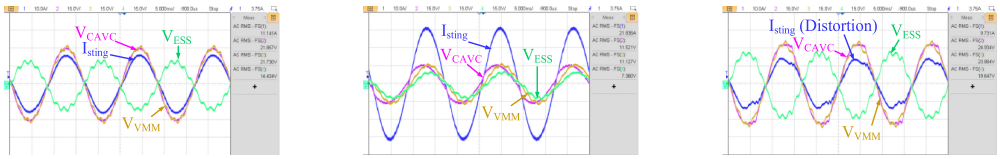
When PV output variations stop, $|i_{\text{batt}}(t)|$ continues to increase and the differentiation of the ac current is going to be zero. Moreover, the direction of the differentiation will be reversed unless $|i_{\text{batt}}(t)|$ starts to decrease. The reversed direction of the differentiation can be an indicator of $t_{\text{detect\_drop\_end}}$. After $t_{\text{detect\_drop\_end}}$, $|i_{\text{batt}}(t)|$ decreases to zero ($t_{\text{ctrl\_end}}$) and the proposed DRRC is completed. In Fig. 2(a) and (b), ideal and practical cases of the DRRC strategy are illustrated. In Fig. 2(b), each transition of detection sequences such as from $t_{\text{drop}}$ to $t_{\text{detect\_drop}}$ and from $t_{\text{drop\_end}}$ to $t_{\text{detect\_drop\_end}}$ requires the differentiation calculation delay. This sequence delay will cause the mismatch between the final ramp-rate and the desired ramp-rate, and the small fluctuation of the ac power. The ramp-rate mismatch error can be reduced by optimizing the sequence delay.

## IV. RESULTS AND DISCUSSIONS

To verify the effectiveness of the proposed architecture and its DRRC strategy, the CHIL test set-up is built, as shown in Fig. 3 [26]. In this set-up, two PV inverters, a CAVC and a VMM, and an ESS inverter are constructed. The detail system parameters are presented in Table I.

TABLE II
SUMMARY OF CHIL TEST RESULTS: PEAK MODULATION INDICES AND OPERATING MARGIN OF THE INVERTERS WITH DIFFERENT OPERATING CONDITIONS

| Detail conditions | | | Peak modulation indices | | | Not in MPP | Current Distortion | Operating margin | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Irradiance level (W/m$^2$) | | Battery current (A) | CAVC | VMM | ESS | | | CAVC | VMM | ESS |
| CAVC | VMM | | | | | | | | | |
| 1000 | 1000 | - | 0.72 | 0.67 | 0.03 | - | - | 28% | 33% | 97% |
| 500 | 1000 | - | 0.51 | 0.89 | 0.03 | - | - | - | 11% (-22%) | - |
| 320 | 1000 | - | 0.39 | 1.0 | 0.03 | - | - | - | 0% (-33%) | - |
| 100 | 1000 | - | 0.28 | 1.0 | 0.03 | ☑ | - | - | 0% (-33%) | - |
| 1000 | 500 | - | 0.91 | 0.46 | 0.03 | - | - | 9% (-19%) | - | - |
| 1000 | 250 | - | 1.00 | 0.29 | 0.03 | - | - | 0% (-28%) | - | - |
| 1000 | 100 | - | 1.00 | 0.16 | 0.03 | - | ☑ | 0% (-28%) | - | - |
| 500 | 500 | - | 0.72 | 0.68 | 0.03 | - | - | 18% (0%) | 32% (-1%) | - |
| 1000 | 1000 | Charging: -4 | 0.99 | 0.97 | 0.46 | - | - | 1% (-27%) | 3% (-30%) | 54% (-43%) |
| 1000 | 1000 | Charging: -4.6 | 1.00 | 1.00 | 0.58 | - | - | 0% (-28%) | 0% (-33%) | 42% (-55%) |
| 1000 | 1000 | Charging: -4.8 | 1.00 | 1.00 | 0.64 | - | ☑ | 0% (-28%) | 0% (-33%) | 36% (-61%) |
| 1000 | 1000 | Discharging: 13.9 | 0.65 | 0.33 | 0.57 | - | - | 35% (+7%) | 67% (+34%) | 33% (-64%) |




(a) (b) (c)

Fig. 4. Interactive operation of the inverters with battery operating conditions; $I_{string}$: ac string current, $V_{CAVC}$: CAVC ac voltage, $V_{VMM}$: VMM ac voltage, and $V_{ESS}$: ESS ac voltage. (a) Charging mode (–4 A). (b) Discharging mode (4 A). (c) Charging mode (–4.8 A).

### A. *Interactive Operation Between PV and ESS Inverters*

The CHIL test results of the inverters' interaction under asymmetrical PV output variations and battery charging and discharging are presented in Table II. The minimum irradiance level on the CAVC where the architecture provides stable operation is 320 W/m$^2$. Under this condition, the peak modulation index of the VMM reaches 1.0 by using all operating margin to cover the CAVC ac voltage drop. Below the minimum irradiance level (100 W/m$^2$), the architecture cannot perform MPPT control because the VMM is required to move its operating point to the right side of the MPP to increase its output voltage. In case of asymmetrical irradiance drop on the VMM, the minimum irradiance level is 250 W/m$^2$. Below the minimum irradiance level (100 W/m$^2$), ac current distortion occurs. The PV inverters' interaction limits the architecture's operating range.

Battery charging mode limits the architecture's operating range, as shown in Fig. 4. When battery current is –4 $A_{dc}$, the ESS generates –14.37 $V_{rms}$ ac voltage. The CAVC and the VMM consume their 96.4% $(27\%/28\% \times 100 = 96.4\%)$ and 90.9% $(30\%/33\% \times 100 = 90.9\%)$ of available operating margin, respectively, to compensate the inverted ESS ac voltage. The maximum battery charging current is –4.6 $A_{dc}$ and the peak modulation indices of the PV inverters reach 1.0 by using all operating margin. With higher battery charging current than –4.6 A, the ac current distortion occurs, as shown in Fig. 4(c). Therefore, the operating range in the battery charging mode is related to the operating margin of the PV inverters (≈28% of CAVC's and ≈33% of VMM's). If the architecture is extended for 120 $V_{rms}$ electrical grid by adding identical PV inverters, the architecture can handle more asymmetrical irradiance drop and battery charging currents. However, the percentage of available operating margin is maintained. The PV inverters must be redesigned with a higher dc input voltage to increase the percentage of available operating margin.

### B. *Decentralized Ramp-Rate Control*

Table III and Fig. 5 present the CHIL test results of the DRRC under different asymmetrical irradiance changes. In this test, the 0.5 ramp-rate gain $k_{ref\_total}$ is applied. When a CAVC irradiance drop (1000 W/m$^2$ → 500 W/m$^2$) is applied, the CAVC output power is decreased by 122.1 W for 2.72 s introducing the PV output ramp-rate –1.50 $A_{rms}$/s, as shown in Fig. 5(a). Adopting the DRRC strategy, the architecture achieves 47% of the PV output ramp-rate –0.70 $A_{rms}$/s by discharging the battery, as shown in Fig. 5(b). Detecting the ac power changes, the ESS increases the battery discharging current until the irradiance drop ends. Detecting the reversed sign of the differentiation of $i_{string}(t)$, the ESS decreases the battery discharging current from 1.11 to 0 A. The interaction between inverters is shown in Fig. 5(c). The CAVC ac voltage is decreased by the CAVC output power drop. The VMM compensates the CAVC ac voltage drop by increasing its ac voltage. Also, the ESS participates the compensation of the CAVC voltage drop and reduces a burden on the VMM slightly during battery discharging operation. When the CAVC irradiance rise (500 W/m$^2$ → 1000 W/m$^2$) is applied, the PV output ramp-rate 1.61 $A_{rms}$/ s is achieved, as shown in Fig. 5(d). With the DRRC, 49% of the PV output ramp-rate 0.79 $A_{rms}$/ s is achieved by charging the battery, as presented in Fig. 5(e). The maximum battery charging current is 1.51 A. In this case, the PV inverters increase their ac voltage to compensate the inverted ESS ac voltage, as shown in Fig. 5(f). Therefore, battery charging operation charges more operating margin of PV inverters. As illustrated in Fig. 2(b), the ramp-rate mis-

TABLE III
SUMMARY OF CHIL TEST RESULTS: THE DRRC WITH DIFFERENT OPERATING CONDITIONS

| Detail conditions | | | | | Changes | | | Without DRRC | | With DRRC | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Modular inverter | | Irradiance level ($W/m^2$) | | | $P_{PV}$ (W) | $I_{PV}$ (A) | $I_{string}$ ($A_{RMS}$) | Time (sec) | Ramp-rate ($A_{RMS}$/s) | Time (sec) | Ramp-rate ($A_{RMS}$/s) | MAX. $I_{batt.}$ (A) | Ramp-rate ratio (%) | Inverter limitation |
| CAVC | VMM | Type | From | To | | | | | | | | | | |
| ☑ | - | Drop | 1000 | 500 | -122. 1 | -4.6 | -4.07 | 2.72 | -1.50 | 5.82 | -0.70 | 1.11 | 47 | - |
| ☑ | - | Rise | 500 | 1000 | 127.2 | 4.6 | 4.24 | 2.64 | 1.61 | 5.34 | 0.79 | 1.51 | 49 | - |
| - | ☑ | Drop | 1000 | 500 | -127.2 | -4.8 | -4.24 | 2.58 | -1.64 | 5.86 | -0.72 | 1.11 | 44 | - |
| - | ☑ | Rise | 500 | 1000 | 127.2 | 4.6 | 4.24 | 2.84 | 1.49 | 6.56 | 0.65 | 1.35 | 44 | - |
| ☑ | ☑ | Drop | 1000 | 500 | -254.4 | -9.2 | -8.48 | 5.48 | -1.55 | 11.34 | -0.75 | 2.23 | 48 | - |
| ☑ | ☑ | Rise | 500 | 1000 | 254.4 | 9.2 | 8.48 | 5.62 | 1.51 | 11.74 | 0.72 | 2.3 | 48 | - |
| ☑ | - | Rise | 350 | 1000 | 164.4 | 5.3 | 5.48 | 2.88 | 1.90 | 8.16 | 0.67 | 1.6 | 35 | ☑ |
| - | ☑ | Rise | 350 | 1000 | 169.8 | 5.3 | 5.66 | 3.4 | 1.66 | 6.16 | 0.92 | 1.35 | 55 | ☑ |

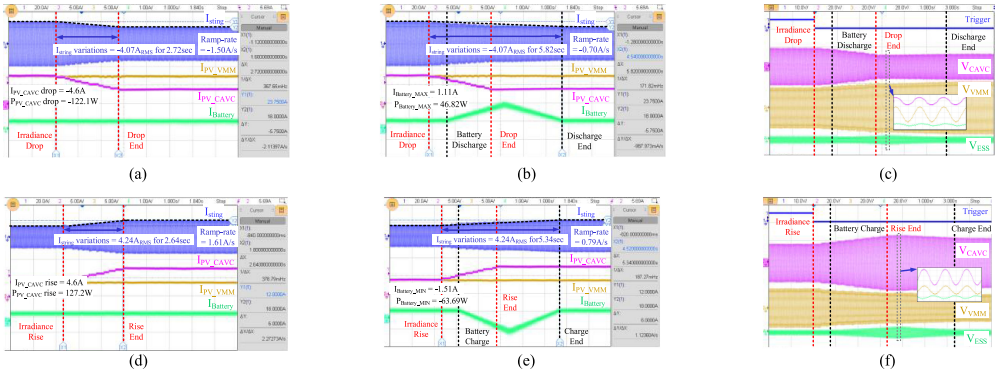



Fig. 5. DRRC: Asymmetrical irradiance changes on the CAVC (1000 W/m$^2$ $\leftrightarrow$ 500 W/m$^2$), ramp-rate factor: 50%. (a) Without DRRC: Irradiance drop, inverter currents. (b) With DRRC: Irradiance drop, inverter currents. (c) With DRRC: Irradiance drop, inverter voltages. (d) Without DRRC: Irradiance rise, inverter currents. (e) With DRRC: Irradiance rise, inverter currents. (f) With DRRC: Irradiance rise, inverter voltages.

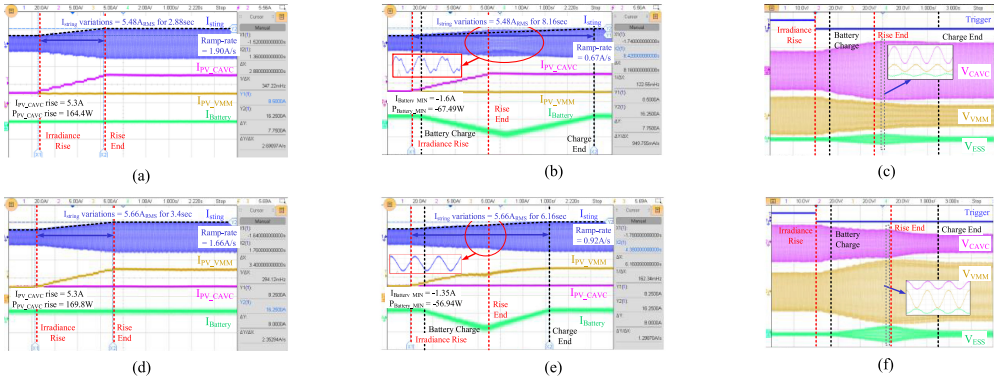



Fig. 6. DRRC: Severe asymmetrical irradiance changes (350 W/m$^2$ $\rightarrow$ 1000 W/m$^2$), ramp-rate factor: 50%. (a) Without DRRC: On the CAVC, inverter currents. (b) With DRRC: On the CAVC, inverter currents. (c) With DRRC: On the CAVC, inverter voltages. (d) Without DRRC: On VMM, inverter currents. (e) With DRRC: On VMM, inverter currents. (f) With DRRC: On VMM, inverter voltages.

match occurs due to the differentiation calculation delays. The mismatch errors are from 2% $(1 - 49\%/50\% \times 100 = 2\%)$ to 12% $(1 - 44\%/50\% \times 100 = 12\%)$. Also, small fluctuation of the ac current is observed.

### C. Operating Range of the Decentralized Ramp-Rate Control

Severe asymmetrical irradiance rise (350 W/m$^2$ $\rightarrow$ 1000 W/m$^2$) is applied to the CAVC and the VMM to analyze the operating range of the DRRC in the proposed architecture, as shown in Fig. 6. In case of the CAVC irradiance rise, the ac current distortion occurs in the middle of the slope where two interactions caused by asymmetrical irradiance changes and battery charging mode are overlapped at the same time, as illustrated in Fig. 6(b). Since the detection of the PV output change stop is delayed due to the ac current distortion, the DRRC time is extended to 8.16 s resulting 35% of the PV output ramp-rate. Therefore, the ramp-rate mismatch error is increased to 30% $(1 - 35\%/50\% \times 100 = 30\%)$.

The interaction between inverters is shown in Fig. 6(c). The CAVC reaches its maximum ac voltage to cover the VMM ac voltage drop and the inverted ESS ac voltage. In case of the VMM irradiance rise, the limitation of the ac current occurs in the middle of the slope due to the overlapped interactions, as presented in Fig. 6(e). Therefore, the VMM moves its operating point from the MPP. This results in the PV current decrease. Since the ac current limitation allows for early detection of the PV output change stop, the DRRC time is shortened to 6.16 s resulting 55% of the PV output ramp-rate. Therefore, the negative ramp-rate mismatch error occurs as –10% $(1 - 55\%/50\% \times 100 = -10\%)$.

## V. Conclusion

This letter presented a control scheme for the PV-battery ac-stacked inverter architecture and its analysis of the system operating range. The PV and ESS inverters' interactive operation and the feasibility of the DRRC were verified through the CHIL test results. Operation constraints on the constructed architecture were asymmetrical irradiance drop, 320 W/m$^2$ on the CAVC and 250 W/m$^2$ on VMM, and the –4.6 A battery charging current. Operating margins of inverters are critical in designing a reliable inverter architecture. A RRC mitigating PV output variations is a suitable application for the proposed architecture due to the battery charging and discharging limitations caused by the interaction. The DRRC can realize the decentralized control environment and minimize the communication requirements between the inverters. Applying the DRRC, the architecture achieved the desired total ac output ramp-rates during the irradiance changes on PV panels. The overlapped interactions (the asymmetrical irradiance level and battery charging mode) affected the performance of the DRRC. The ac current distortion and early detection of the PV output change stop were observed once the PV inverters use all of their operating margins. Further improvement can be made by implementing PV out curtailment control, which can reduce the required amount of the battery charging current.

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# APPENDIX B: PV-BATTERY SERIES INVERTER ARCHITECTURE: A SOLAR INVERTER FOR SEAMLESS BATTERY INTEGRATION WITH PARTIAL-POWER DC-DC OPTIMIZER

# PV-Battery Series Inverter Architecture: A Solar Inverter for Seamless Battery Integration With Partial-Power DC–DC Optimizer

Namwon Kim, *Student Member, IEEE*, and Babak Parkhideh, *Senior Member, IEEE*

***Abstract*—This paper presents system architecture and control scheme of a photovoltaic (PV) string inverter allowing seamless battery integration with the dc-series integration method. The architecture uses the partial-power processing universal dc–dc optimizer to have flexible power control by regulating the T-node compensation current. The universal optimizer is configured with a dual active bridge dc–dc converter allowing bidirectional power flow and galvanic isolation. Three operation modes are proposed depending on the input sources connected. Based on the operation mode, the universal optimizer and a dc–ac inverter switch their control reference to deliver the maximum PV power and perform battery current control. The steady-state and transient operation of the closed-loop control scheme have been demonstrated through controller hardware-in-the-loop tests to verify feasibility and effectiveness of the PV-battery series inverter architecture.**

***Index Terms*—DC-series integration, PV-battery series inverter architecture, partial power processing, seamless battery integration, t-node compensation current, universal optimizer.**

## I. Introduction

DUE to the intermittent nature of solar photovoltaic (PV) energy and concerns regarding the rise of electricity demand, integration of battery energy storage system (ESS) has gained attention as an energy saving solution in residential and commercial grid-tied PV inverter systems [1]–[4]. In PV inverters, legacy PV power electronics topologies [5] are used for integration of a battery ESS, as shown in Fig. 1: a) AC-parallel integration using a bidirectional grid-tied DC-AC inverter with a battery voltage boosting DC-DC converter [6], b) DC-parallel integration using a bidirectional DC-DC converter connected to a DC bus with a unidirectional single or cascaded PV DC-DC converters [7], c) in-line integration inserting a battery to a DC bus directly in parallel [8], and d) AC-series integration adding a modular bidirectional DC-AC inverter member to an AC string [9], [10]. These integration methods require that a battery ESS has additional voltage-amplification stages such as a DC-DC boost converter or a line-frequency transformer, a high-voltage battery, or restrictions of output power in consideration of interactive operations among inverter members to maintain its grid-connection. These requirements increase system cost and size, lower efficiency, and limit applications of battery ESS. Therefore, it is needed to develop a power electronics topology which relieves these requirements to expedite the integration of battery ESS into grid-tied PV generation system.

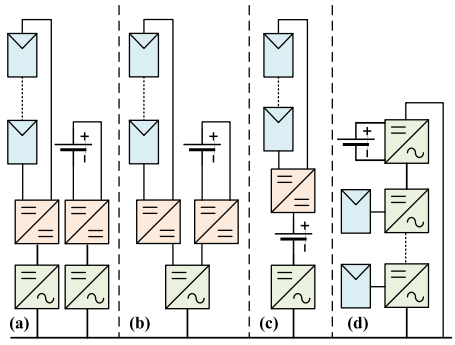


Fig. 1. State-of-the-art of battery integration methods for grid-tied PV inverters in residential and commercial applications. (a) AC-parallel integration. (b) DC-parallel integration. (c) In-line integration. (d) AC-series integration.

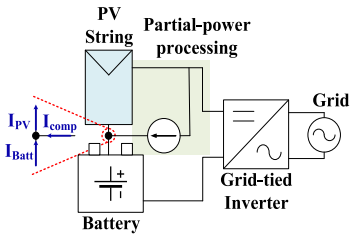


Fig. 2. The proposed approach: DC-series integration.

This paper presents a grid-tied PV string inverter allowing seamless battery integration: the PV-battery series inverter architecture. The proposed system adopts the PV-battery DC-series integration method, as shown in Fig. 2. In this approach, the battery integration does not require additional power electronics stages, a high-voltage battery, or battery power restrictions. Besides, a battery supports the PV string voltage to

Manuscript received April 9, 2018; revised August 22, 2018; accepted September 27, 2018. Date of publication October 3, 2018; date of current version February 26, 2019. Paper no. TEC-00420-2018. *(Corresponding author: Namwon Kim.)*

The authors are with the Department of Electrical and Computer Engineering, Energy Production and Infrastructure Center, University of North Carolina at Charlotte, Charlotte, NC 28223 USA (e-mail: nkim22@uncc.edu; bparkhideh@uncc.edu).

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Digital Object Identifier 10.1109/TEC.2018.2873664

provide flexibility in delivering the PV string's maximum output power to grid with different system characteristics reducing PV string voltage: for example, a small number of PV panels, solar irradiance drops, ambient temperature rise, and low voltage and low power system design [11], [12]. These benefits are enabled by adopting partial-power processing technique which provides a capability to regulate the T-node compensation current, $I_{comp}$. The proposed architecture uses the partial-power universal DC-DC optimizer working as a current source to offset the battery discharging current and have flexible battery power control. Furthermore, the partial-power universal optimizer requires lower rated power than the state-of-the-art DC-DC converters for PV and battery applications while it handles both PV and battery power [13]–[17]. As the universal optimizer, a dual active bridge (DAB) DC-DC converter is applied which allows bidirectional power flow, galvanic isolation, a high voltage gain, and soft-switching operation [18], [19].

In this paper, the proposed architecture and its closed-loop control strategy are presented. The PV-battery series inverter architecture is composed of the universal DC-DC optimizer regulating the T-node compensation current and a grid-tied DC-AC inverter controlling its DC bus voltage. With the seamless battery integration topology, three operation modes are available based on the configurations of the input sources: a) PV-only mode, b) PV-battery mode, and c) battery-only mode. Depending on the operation modes, the universal optimizer coordinates with the DC-AC inverter to meet the system's control objectives: PV maximum power point tracking (MPPT) control and battery current control. The steady-state and transient operations of the closed-loop control have been investigated and demonstrated through the controller hardware-in-the-loop (CHIL) testing to verify the feasibility and the effectiveness of the proposed PV-battery series inverter architecture.

The rest of this paper is organized and presented as follows. Section II presents the proposed PV-battery integration system architecture. The power electronics topology and its control scheme are proposed in Section III. Section IV provides the results and discussion, and Section V concludes this paper.

## II. PV-Battery Integration Strategy and System Architecture

The PV-battery series inverter architecture is proposed to achieve seamless battery integration for grid-tied PV inverters. The proposed approach is to connect a battery to a PV string directly in series as shown in Fig. 2: DC-series integration. This integration does not require a high-voltage battery or additional power electronics stages such as a DC-DC boost converter for a low-voltage battery. Also, a battery supports a PV string in maintaining grid-connection by adding its voltage to the PV voltage. Therefore, voltage amplification stages such as a fully-rated DC-DC boost converter or a line-frequency transformer, the essential devices for the legacy grid-tied PV inverters, are not required to cope with different system characteristics including PV panel installation area, cabling limitations, irregular weather conditions, and different PV voltage and power.

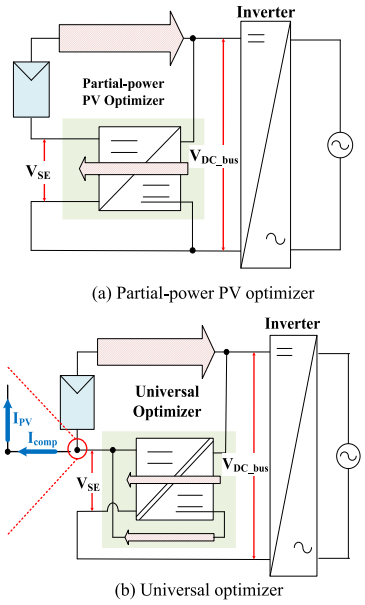



Fig. 3. Development of partial-power universal optimizer in PV-only mode.

The DC-series integration is enabled by having a current source injecting a DC current into the PV-battery coupling point called T-node. Due to the series connection, the same amount of the DC current passes through the PV string and the battery. Therefore, the battery is discharged as long as the PV string generates output power. Thus, a compensation current needs to be injected into the T-node to offset the battery discharging current. Also, the regulation of the T-node compensation current guarantees flexible battery power control capability as

$$I_{Batt} = I_{PV} - I_{comp} \tag{1}$$

where $I_{PV}$ is the PV string current and $I_{Batt}$ is the battery current. Adopting partial-power processing technique [13]–[17], the authors propose the universal optimizer functioning as the T-node current compensator and enabling seamless PV-battery integration. Depending on the configuration of input sources, the proposed universal optimizer has three operation modes.

### A. PV-Only Mode

A battery is disconnected from the T-node, as shown in Fig. 3(a). The main operation targets are tracking the PV's maximum power point (MPP) and grid-connection. The partial-power PV optimizer compensates for the DC voltage deficiency caused by the difference between the DC bus voltage, $V_{DC\_bus}$, and the PV voltage, $V_{PV}$, by adding the series voltage, $V_{SE}$, *as*

$$V_{DC\_bus} = V_{PV} + V_{SE}. \tag{2}$$

Also, the DC-DC power conversion stage processes only the portion of the PV power through the partial-power processing loop including the DC-DC converter: resulting lower converter rated power and conversion loss to deliver the PV output power.

The partial-power rate (PPR) for the PV power, $PPR_{PV}$, is proportional to the ratio between the series voltage and the PV voltage as

$$PPR_{PV} = \frac{V_{SE}}{V_{PV}}. \tag{3}$$

Besides, further circuit optimization is proposed with improvements in system efficiency and components' voltage stress by achieving partial-power processing for both PV and battery power, as presented in Fig. 3(b): the universal optimizer. The universal optimizer processes the portion of power passing through the partial-power processing loop by having an additional series-connection on the DC bus side with the universal optimizer input voltage and the series voltage. An isolated DC-DC converter topology is adopted to configure the DC bus series-connection. The PPR for the partial-power processing loop power, $PPR_{loop}$, is proportional to the ratio between the PV voltage and the DC bus voltage as

$$PPR_{loop} = \frac{V_{DC\_bus} - V_{SE}}{V_{DC\_bus}} = \frac{V_{PV}}{V_{DC\_bus}}. \tag{4}$$

The total PPR for the PV power, $PPR_{total}$, is achieved with the product of $PPR_{PV}$ and $PPR_{loop}$, and the rated power of the universal optimizer, $P_{optimizer}$, is calculated with the total PPR and the PV power, $P_{PV}$, as

$$PPR_{total} = PPR_{PV} \cdot PPR_{loop} = \frac{V_{SE}}{V_{PV}} \cdot \frac{V_{PV}}{V_{DC\_bus}} = \frac{V_{SE}}{V_{DC\_bus}} \tag{5}$$

$$P_{optimizer} = \frac{P_{PV} \cdot PPR_{total}}{\eta_{converter}} \tag{6}$$

where $\eta_{converter}$ is the power efficiency of the DC-DC converter. Due to the decrease of the optimizer rated power, the DC-DC power conversion loss, $P_{loss}$, is reduced, and the DC-DC power conversion efficiency, $\eta_{DC-DC}$, is improved as

$$P_{loss}\,(\downarrow) = P_{optimizer}\,(1 - \eta_{converter}) \tag{7}$$

$$\eta_{DC-DC}\,(\uparrow) = \frac{P_{PV} - P_{loss}}{P_{PV}}. \tag{8}$$

The remaining power which does not pass through the universal optimizer is delivered to the DC-AC inverter directly.

### B. PV-Battery Mode

Seamless battery integration into the PV system can be achievable by connecting a battery to the open terminals between the PV string and the ground, as shown in Fig. 4 [20]. The main operation targets of the PV-battery mode are PV MPPT control with extended PV operating range and flexible battery current control. In this configuration, the battery can be used as a power source and a PV voltage supporter simultaneously. Unlike the PV-only mode, the series voltage is enforced to be almost constant by the battery voltage, $V_{Batt}$, as

$$V_{SE} = V_{Batt}. \tag{9}$$

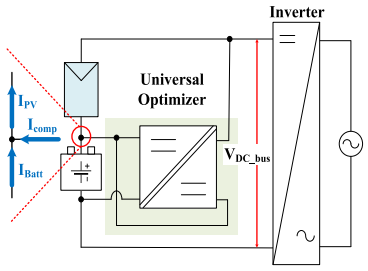



Fig. 4. The proposed partial-power universal optimizer in PV-battery mode.

Therefore, the battery voltage is added to the PV string voltage to extend the PV operating range. The total PPR of the proposed optimizer is proportional to the battery voltage as follows:

$$PPR_{total} = PPR_{PV} \cdot PPR_{loop} = \frac{V_{Batt}}{V_{PV}} \cdot \frac{V_{PV}}{V_{DC\_bus}} = \frac{V_{Batt}}{V_{DC\_bus}}. \tag{10}$$

In the PV-battery mode, there are three sub-operation modes: a) battery zero-current mode, b) battery charging mode, and c) battery discharging mode. The rated power of the universal optimizer varies depending on the sub-operation modes. In the battery zero-current mode, the rated power and the DC-DC power conversion efficiency can be found in the same way with the PV-only mode because the DC-DC conversion stage processes only the PV power. In the battery charging mode, the battery power passes through the partial-power processing loop together with the partial amount of the PV power. The rated power is increased due to the partial amount of the battery power, the product of $-P_{Batt}$ and $PPR_{loop}$, as

$$P_{optimizer(charging)} = \frac{P_{PV} \cdot PPR_{total} - P_{Batt} \cdot PPR_{loop}}{\eta_{converter}}. \tag{11}$$

The DC-DC power conversion efficiency is calculated based on the amount of the processed PV and battery power as

$$\eta_{DC-DC} = \begin{cases} \frac{P_{PV} - P_{loss}}{P_{PV}}, & P_{PV} \geq P_{Batt} \\ \frac{P_{Batt}}{P_{Batt} + P_{loss}}, & P_{PV} < P_{Batt}. \end{cases} \tag{12}$$

On the other hand, the battery discharging mode has two ways to deliver the battery power to the grid. Until the battery current becomes the same amount with the PV current, the battery power passes through the PV power loop, the power path across the PV string, and the T-node compensation current is decreased. If the battery current is over than the PV current, only remaining battery power passes through the partial-power processing loop. The rated power and the DC-DC power conversion efficiency

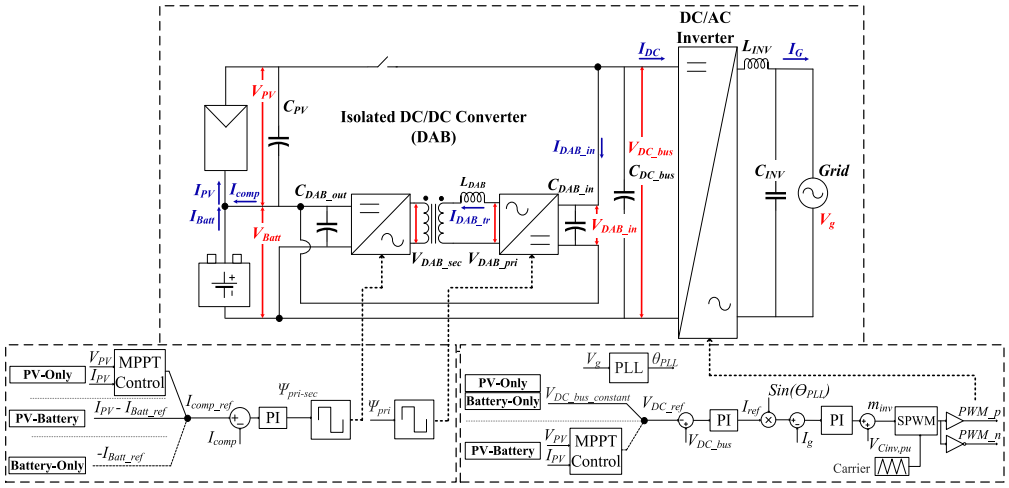



Fig. 5. Proposed topology for the universal optimizer and control strategy.

are expressed as follows:

$$P_{optimizer(discharging)} = \frac{abs(P_{PV} \times PPR_{PV} - P_{Batt}) \cdot PPR_{loop}}{\eta_{converter}} \quad (13)$$

$$\eta_{DC-DC} = \frac{P_{PV} + P_{Batt} - P_{loss}}{P_{PV} + P_{Batt}}. \quad (14)$$

### C. Battery-Only Mode

Due to the very low PV voltage or its physical disconnection, the battery-only mode is configured by disconnecting the PV string from the universal optimizer. The main operation target of the battery-only mode is battery current control only. Since the PV current path does not exist, the partial-power processing in the PV-series is not available and $PPR_{PV}$ becomes "1.0". Therefore, only $PPR_{loop}$ is applied to the total PPR, and the rated power and the DC-DC power conversion efficiency can be found as follows:

$$PPR_{total} = PPR_{loop} = \frac{V_{DC\_bus} - V_{Batt}}{V_{DC\_bus}} \quad (15)$$

$$P_{optimizer} = \frac{P_{Batt} \cdot PPR_{loop}}{\eta_{converter}} \quad (16)$$

$$\eta_{DC-DC} = \frac{P_{Batt}}{P_{Batt} + P_{loss}}. \quad (17)$$

## III. Proposed Power Electronics Topology and Control Strategy

The PV-battery series inverter architecture is composed of two power electronics stages: the universal DC-DC optimizer and the grid-tied DC-AC inverter. Fig. 5 shows the power electronics topology of the universal optimizer. A DAB DC-DC converter is applied because it provides bidirectional power control, galvanic isolation, a high-voltage boosting gain, and soft-switching operation [18], [19]. For the DC-AC inverter stage, a full-bridge single-phase DC-AC inverter is considered.

Also, Fig. 5 shows the closed-loop control scheme of the proposed architecture in different operation modes. The universal optimizer controls the T-node compensation current by regulating the phase angle difference, $\Psi_{pri-sec}$, between the primary and secondary voltages of the high-frequency transformer [21]. The DC-AC inverter controls the DC bus voltage and maintains grid-connection by regulating the duty cycles of the PWM signals [22]. Based on the operation mode, the universal optimizer coordinates with the DC-AC inverter to achieve the system's control objectives: PV MPPT control and battery current control. The control references of the power electronics units are switched.

### A. PV-Only Mode

The DC-AC inverter maintains a constant DC bus voltage greater or equal to the PV string's open circuit voltage to provide the full range of PV MPPT operation. On the other hand, the universal optimizer performs PV MPPT control by regulating the T-node compensation current which is equal to the PV current. The T-node compensation current reference, $I_{comp\_ref}$, is generated by the perturb and observe (P&O) MPPT control block [23]. As the T-node compensation current increases, the series voltage increases to compensate for the PV voltage drop based on the PV string's V-I curve, as follows:

$$I_{comp\_ref} = I_{MPPT\_CMD} \quad (18)$$

$$V_{PV}\,(\downarrow) + V_{SE}\,(\uparrow) = V_{DC\_bus}\,(constant) \quad (19)$$

where $I_{MPPT\_CMD}$ is the PV MPPT control command in the PV-only mode.

### B. PV-Battery Mode

Once a battery is connected, the control system can detect the PV-battery mode by monitoring the series voltage which is

TABLE I
SYSTEM PROPERTIES – A CASE STUDY OF THE PV-BATTERY SERIES INVERTER ARCHITECTURE (1000 W/m$^2$ AND 25 °C)

| System Parameters | | | | |
|---|---|---|---|---|
| PV | MPP PWR | 2.5 kW | | |
| | MPP Volt. | 161.5 V | | |
| Battery | Power | 1.0 kW | | |
| | Voltage | 50 V | | |
| Grid | Voltage | Single phase, 120 $V_{RMS}$ | | |
| A PV/Battery Universal Optimizer | | | | |
| Operation Mode | | PV-only | PV-battery | Battery-only |
| PV Output Voltage | | 161.5 V | 161.5 V | - |
| Series Voltage | | 38.6 V | 50.0 V | 50.0 V |
| Max. Rated Power ($PPR_{total}$) | | 0.5 kW (20%) | 1.4 kW (55%) | 0.8 kW (22%) |
| Absolute $\eta_{DAB}$ | | 97.5% | 97.5% | 97.5% |
| $\eta_{DC\text{-}DC}$ | PV Only | 99.5% | 99.4% | - |
| | Discharging | - | 99.6% | 98.1% |
| | Charging | - | 99.0% | 98.1% |
| A DC-AC Inverter | | | | |
| Rated Power | | 2.5 kW | 2.5 kW | 2.5 kW |
| DC-Link Voltage | | 200 V | 211.5 V | 200 V |
| $\eta_{Inverter}$ | | 98.5% | 98.5% | 98.5% |
| Total Efficiency | | | | |
| $\eta_{Total}$ | PV Only | 98.0% | 97.9% | - |
| | Discharging | - | 98.1% | 96.6% |
| | Charging | - | 97.7% | 96.6% |

equal to the output voltage of the optimizer before it starts the switching operation, for example,

$$\begin{cases} PV-Only\ Mode, & V_{SE}\ (or\ V_{Batt}) < V_{Batt,min} \\ PV-Battery\ Mode, & V_{SE}\ (or\ V_{Batt}) \geq V_{Batt,min} \end{cases} \tag{20}$$

where $V_{Batt,min}$ is the minimum battery voltage which can be detected by the control system. Since the series voltage is equal to the battery voltage, PV MPPT control needs to be performed by the DC-AC inverter. The P&O MPPT control block generates the DC bus voltage reference, $V_{DC\_ref}$, as

$$V_{DC\_ref} = V_{MPPT\_CMD} \tag{21}$$

$$V_{DC\_bus}\ (\downarrow) = V_{PV}\ (\downarrow) + V_{Batt} \tag{22}$$

where $V_{MPPT\_CMD}$ is the PV MPPT control command in the PV-battery mode. The DC bus voltage reference is limited by the peak value of the grid voltage, $\sqrt{2}V_{g\_RMS}$, for grid-connection. In this mode, the universal optimizer regulates the T-node compensation current to perform battery current control as

$$I_{comp\_ref} = I_{PV} - I_{Batt\_ref} \tag{23}$$

where $I_{Batt\_ref}$ is the battery current reference.

### C. Battery-Only Mode

The control system can detect the battery-only mode by monitoring the PV string voltage, for example,

$$\begin{cases} Battery-Only\ Mode, & V_{PV} < V_{PV,min} \\ PV-Battery\ Mode, & V_{PV} \geq V_{PV,min} \end{cases} \tag{24}$$

where $V_{PV,min}$ is the threshold PV string voltage for the detection of the battery-only mode.

The DC-AC inverter maintains a constant DC bus voltage to provide the bidirectional rated-power flow under grid-connection. Also, the universal optimizer regulates the T-node compensation current to perform battery current control as

$$I_{comp\_ref} = -I_{Batt\_ref}. \tag{25}$$

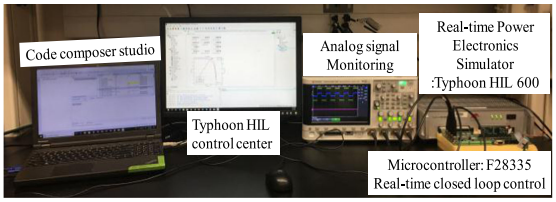
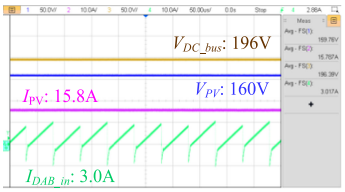
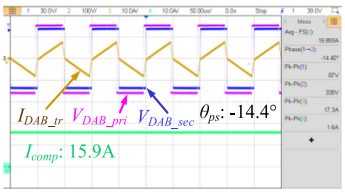



Fig. 6. CHIL setup for testing the proposed power electronics topology.




(a) PV MPPT control



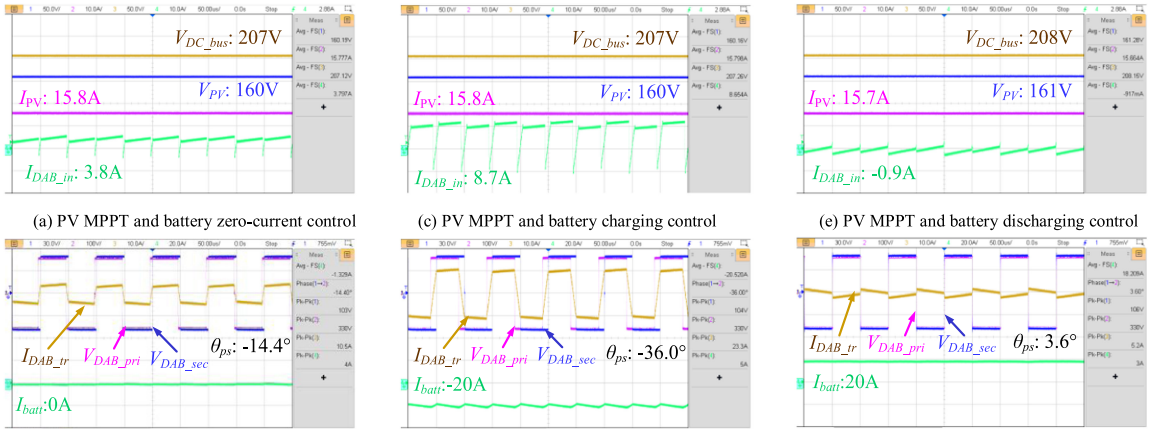

(b) DAB phase-shift control

Fig. 7. CHIL experiment results: Steady-state operation of the PV-battery series inverter architecture in the PV-only mode, PV output power: 2.5 kW.

## IV. RESULTS AND DISCUSSIONS

Table I presents a case study of the proposed system properties in different operation modes. A 2.5 kW 161.5 $V_{MPP}$ PV string under a nominal weather condition, a 1.0 kW 50 V battery and single-phase 120 $V_{RMS}$ AC grid are considered. As the result, the max. 1.4 kW optimizer (PPR: 55%) is required to transfer the PV output power: 1.5 kW to the grid and 1.0 kW to the battery (charging). Since the universal optimizer processes the portion of both the PV and battery power, the battery charging operation requires the maximum rated power. Also, max. 99.6% of the DC-DC conversion efficiency during battery discharging operation in the PV-battery mode (+2.1%) and min. 98.1% of the DC-DC conversion efficiency in the battery-only mode (+0.6%) are achieved (when the DAB converter efficiency is assumed as 97.5%).

For the verification of the case study and the control performance of the PV-battery series inverter architecture in different operation modes, a DAB DC-DC converter, a single-phase DC-AC full-bridge inverter, and their closed-loop control scheme are built and run in the CHIL test-bed with a 500 ns solution time step real-time power electronics simulator, Typhoon HIL 600, [24] and a 150 MHz digital microcontroller, TMS320F28335,




(a) PV MPPT and battery zero-current control (c) PV MPPT and battery charging control (e) PV MPPT and battery discharging control

(b) $I_{Batt}$=0A: DAB phase-shift control (d) $I_{Batt}$=-20A: DAB phase-shift control (f) $I_{Batt}$=20A: DAB phase-shift control

Fig. 8. CHIL experiment results: Steady-state operation of the PV-battery series inverter architecture in the PV-battery mode, PV output power: 2.5 kW (MPPT) and battery output power: ±1 kW (battery zero-current mode, battery charging mode, and battery discharging mode).

as shown in Fig. 6. The power electronics converters are operated with 10 kHz switching frequency to provide clear operation waveform of the DAB phase-shifting control with consideration of the digital-to-analog conversion time response of the real-time power electronics simulator.

### A. *Steady-State Operation*

The CHIL experiment results of steady-state operation of the PV-battery series inverter architecture show how the universal optimizer operates in different operation modes.

In the PV-only mode, as shown in Fig. 7, the DC bus voltage is maintained constant as 196 V, the PV string's open circuit voltage, by the DC-AC inverter. To deliver 2.5 kW PV maximum output power to AC grid, the universal optimizer processes 0.5 kW (PPR = 20%) by regulating the T-node compensation current as 15.9 A with −14.4° degrees phase difference.

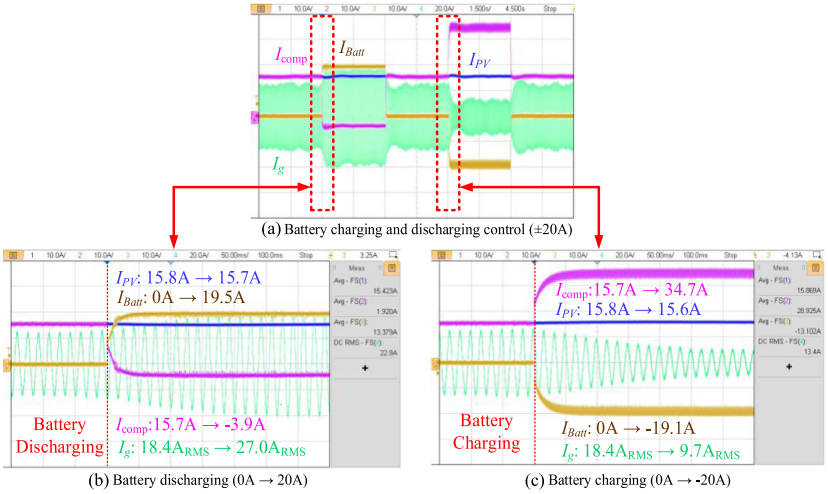
In the PV-battery mode, as shown in Fig. 8, the DC bus voltage is regulated as 207 V, the sum of the PV string's MPP voltage and the battery voltage, by the DC-AC inverter to extract 2.5 kW PV string's maximum output power. Fig. 8(a) and (b) show the CHIL results of the battery zero-current mode. The universal optimizer processes 0.6 kW rated power (PPR = 24%) to maintain 0 A battery current which was supposed to be the same with 15.8 A PV string current without the T-node compensation current control. −14.4° degrees phase difference is applied to the DAB converter. Due to the differences of the magnitudes of the series voltage and the DC bus voltage between the PV-only mode and the PV-battery mode, the processed power through the universal optimizer is slightly different with the same phase differences. Fig. 8(c) and (d) show the results of the battery charging mode. By shifting −36.0° degrees phase angle, the battery current is maintained as −20 A for 1 kW battery charging power. The processed power through the universal optimizer is 1.4 kW (PPR = 56%) with 35.8 A T-node compensation current. Like the case study, the battery charging mode requires the maximum rated power of the universal optimizer since it processes the portion of both the PV and battery power. Fig. 8(e) and (f) show the results of the battery discharging mode. In this case, the direction of the phase-shift regulation is reversed. By shifting 3.6° degrees phase angle, the battery current is maintained as 20 A, for 1 kW battery discharging power. With the amount of the PV current, 15.7 A battery current is discharged through the PV power loop and the rest of the battery current, 4.3 A, is discharged through the universal optimizer and the battery partial-power processing loop. Therefore, the processed power through the universal optimizer is decreased to 0.2 kW (PPR = 8%).

### B. *Transient Operation*

To prove feasibility and performance of the closed-loop control, sudden changes of control reference are investigated.

Fig. 9 shows the battery current control in the PV-battery mode. Initially, the architecture operates in the battery zero-current mode with 15.8 A PV current, 15.7 A T-node compensation current, and 18.4 $A_{RMS}$ AC current. As the transient conditions, changes of the battery current reference from 0 A to 20 A and from 0 A to −20 A are applied. As shown in Fig. 9(b), once the battery discharging command is applied, the universal optimizer can reach to the target point, 19.5 A battery current, by decreasing the T-node compensation current to −3.9 A in 50 ms. Also, once the battery charging command is applied, the universal optimizer controls, −19.1 A battery current, by increasing the T-node compensation current to 34.7 A in 50 ms, as presented in Fig. 9(c). During transient operations, the PV current is maintained constant as 15.8 A by the DC-AC inverter with PV MPPT control. The transient operation verifies the relationship among the PV current, the battery current, and the T-node compensation current, as addressed in (23).

Fig. 10 shows the PV MPPT control in the PV-battery mode with sudden PV irradiance variations, and the battery zero-current control. Once a PV irradiance variation occurs, the PV current changes suddenly based on the PV string's V-I curves. As the result, the battery current is also changed unless the

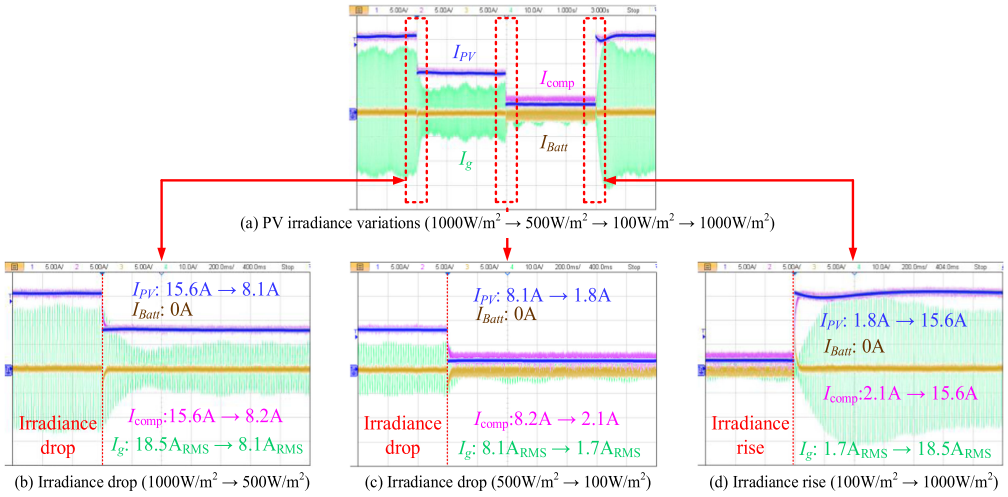



(a) Battery charging and discharging control (±20A)

(b) Battery discharging (0A → 20A)

(c) Battery charging (0A → -20A)

Fig. 9. CHIL experiment results: Transient operation of the PV-battery series inverter architecture in the PV-battery mode; battery zero-current mode, battery charging mode, and battery discharging mode (PV output power: 2.5 kW and battery output power: ±1 kW).




(a) PV irradiance variations (1000W/m$^2$ → 500W/m$^2$ → 100W/m$^2$ → 1000W/m$^2$)

(b) Irradiance drop (1000W/m$^2$ → 500W/m$^2$)

(c) Irradiance drop (500W/m$^2$ → 100W/m$^2$)

(d) Irradiance rise (100W/m$^2$ → 1000W/m$^2$)

Fig. 10. CHIL experiment results: Transient operation of the PV-battery series inverter architecture in the PV-battery mode, PV irradiance variations (1000 W/m$^2$ → 500 W/m$^2$ → 100 W/m$^2$ → 1000 W/m$^2$) and battery zero-current mode.

universal optimizer regulates enough T-node compensation current based on the relationship between the three T-node currents (1). As shown in Fig. 10(b) and (c), once the irradiance drop is applied, the battery charging current appears, and it is compensated by the universal optimizer in 50 ms by decreasing the T-node compensation current from 15.6 A to 8.2 A and from 8.2 A to 2.1 A, respectively. Also, once the irradiance rise is applied, the battery discharging current appears, and the T-node compensation current is regulated from 2.1 A to 15.6 A in 50 ms, as presented in Fig. 10(d). Also, the transient operation verifies that the proposed architecture provides extended PV operating range with the DC-series integration. Under the different irradiance levels applied, as shown in Fig. 10, the PV voltage varies from 161.46 V to 145.31 V. The battery voltage is added to the PV voltage and helps the DC bus satisfies the minimum DC bus voltage, 169.7 V, for grid-connection.

## V. Conclusions

This paper presented system structure and control scheme of the PV-battery series inverter architecture. The DC-series integration with partial-power processing technique allows that a battery can be integrated without additional power electronics stages and support the PV voltage in maintaining grid-connection with different operating conditions. The pro-

posed partial-power DC-DC universal optimizer enables the partial-power processing for both PV and battery power. Therefore, it handled 2.5 kW PV power and 1.0 kW battery power with 1.4 kW rated power. The coordinated closed-loop control between the two power electronics stages was proposed for different operation modes since the controllability of the series voltage is dependent on the battery integration. By switching control objectives of the individual power electronics stages, the PV-battery series inverter architecture achieved flexible battery current control and extended PV MPPT control range. Feasibility and effectiveness of the proposed architecture and the coordinated control scheme were verified through the CHIL tests with the steady-state and the transient operations.

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**Namwon Kim** (S'17) received the B.Sc. and M.Sc. degrees in electrical engineering from Changwon National University, Changwon, South Korea, in 2010 and 2012, respectively. He is currently working toward the Ph.D. degree at Department of Electrical and Computer Engineering, University of North Carolina at Charlotte, Charlotte, NC, USA.

His research interests include design and control of renewable energy systems, PV-battery integrated power electronics, and high-frequency converters.

**Babak Parkhideh** (S'07–M'13–SM'16) received the B.Sc. degree (Hons.) from the University of Tehran, Tehran, Iran, in 2003, the M.Sc. degree from RWTH Aachen University, Aachen, Germany, in 2006, and the Ph.D. degree from North Carolina State University, Raleigh, NC, USA, in 2012, all in electrical engineering.

He is currently an Associate Professor with the Department of Electrical and Computer Engineering, University of North Carolina at Charlotte, Charlotte, NC, where he is also a Faculty Associate with the Energy Production and Infrastructure Center and the Founding Director of the PV Integration Laboratory. His current research interests include photovoltaic/battery power electronic systems, high-frequency power converters, and high-bandwidth current-sensing schemes.