INVESTIGATIONS ON MULTILEVEL AND SURGELESS SOLID-STATE CIRCUIT BREAKERS

by

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ABSTRACT

TIANCAN PANG. Investigations on Multilevel and Surgeless Solid-State Circuit Breakers. (Under the Direction of Dr. MADHAV MANJREKAR)

The Solid-State Circuit Breaker (SSCB), as an emerging semiconductor-based circuit protection technology, is featured with its extremely fast fault interruption/isolation speed and regarded as a promising alternate to the electromechanical circuit breakers in the DC systems.

However, in the conventional SSCBs, large surge voltages are clamped across their semiconductor switches when the breakers open and the dynamic voltage unbalance is incurred when the series-connected switches are used. With these technical defects, the efficiencies and reliabilities of the SSCBs are impaired and their wide adoption to the DC distribution systems is set back.

To overcome these technical limits of conventional SSCBs, four types of Multilevel and Surgeless Solid-State Circuit Breakers have been proposed in this dissertation. By utilizing the fast switching speeds of the semiconductor switches, the proposed SSCBs can commutate the fault current to the different conduction paths of the circuit breakers and attain significant benefits on efficiency and fault isolation speeds in comparison with the conventional SSCBs. Particularly, for the proposed Multilevel Solid-State Circuit Breaker (MLSSCB), the series-connected switches are clamped to their voltage dividing capacitors during their switching transience and then the dynamic voltage unbalancing issues among the switches can be averted. For the proposed surgeless SSCBs, with surge voltage suppressed, the semiconductor switches do not need to be overdesigned for the voltage ratings and the conduction efficiencies of the SSCBs

can be improved on the ground that the semiconductor device with higher voltage block capability has thicker drift regions and larger on-state resistance. Derived from the integration of the Ground-Clamped Surgeless SSCB and the Multilevel SSCB, the proposed Surgeless Multilevel SSCB (SMLSSCB) can solve both the surge voltage and dynamic voltage unbalancing issues in the medium voltage DC SSCBs and attain higher efficiency and an ultra-fast isolation speed prior to the other SSCBs. A fault-tolerant configuration of the SMLSSCB has also been proposed to improve the reliability of SMLSSCB and make it prior to that of the conventional SSCBs.

In this dissertation, the operating principles of the proposed SSCBs have been presented. Besides, to demonstrate the proposed SSCBs' advantages over the conventional SSCBs on fault isolation speeds, power efficiencies and reliability, the comparisons between the proposed SSCBs and their counterparts of the conventional SSCBs have been made in terms of several key parameters of the circuit breakers. Additionally, the simulation/experiment results and design considerations of the proposed circuit breakers have been introduced to validate their technical feasibilities and practical uses.

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DEDICATION

This dissertation is dedicated to my mother, Caixian Li, my father, Dr. Haonong Pang and my partner, Zifen Zeng, for their profound love and great support.

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CHAPTER1: INTRODUCTION

Recently, great interests have been aroused in DC distribution systems because of their high efficiency and flexibility in the integrations of renewable energy resources and electronic loads [1] [2]. However, resulting from the absence of the natural zero-crossing points of current/voltage, the limited over-current-sustaining capability of the power converters and the relatively small inductances of the power cables, the DC systems have a high demand on the response speeds of their circuit protection devices. The conventional electromechanical circuit breakers that have been time-tested in AC systems have their operation speed limited by the critical momentum of their movable parts and are incompetent to protect the DC systems in many cases [3]. As a result, the DC circuit protection has become a well-known challenging problem hindering the deployment of the DC distribution systems.

The Solid-State Circuit Breaker (SSCB), as an emerging semiconductor-based circuit protection technology, is featured with its extremely fast current interrupting speed and regarded as a promising solution to the protection problems in the DC systems [4] [5].

However, due to the system line inductances, surge voltages are induced across the SSCBs when they interrupt the current. Although the MOVs are used in the SSCBs to clamp the surge voltages under the appliable voltage ranges of the semiconductor devices, the clamped surge voltages are still significantly higher than the system voltages to attain the fast isolation speeds and avert the premature aging on the MOV. As a result, the semiconductor switches of the SSCBs have to be overdesigned in terms of their voltage ratings to sustain the surge voltages, which may seriously impair the efficiencies of the circuit breakers.

On the other hand, with the increment of the system voltages, series-connected switches are needed in the SSCBs. Nevertheless, due to the mismatch of the switches' parasitic capacitances and the turn-off delays originating from the gate drivers, the series-connected switches may fail to turn off simultaneously and incur harmful dynamic unbalanced voltage.

To deal with these issues in the different applications of DC distributions, several new topologies of solid-state circuit breakers have been proposed in this dissertation, namely Multilevel Solid-State Circuit Breaker, Surge Voltage Free Solid-State Circuit Breaker, Ground Clamped Solid-State Circuit Breaker and Surgeless Multilevel Solid-State Circuit Breaker. Besides, to compensate the deficiency of reliability caused by the advanced topologies, a fault-tolerant configuration of Surgeless Multilevel Solid-State Circuit Breaker has been proposed. The operating principles, simulation/ experiment results, design considerations of the proposed SSCBs have been presented to validate their technical feasibilities and practical values.

1.1 Unbalanced and Surge Voltage Issues in Solid-State Circuit Breakers

In the medium voltage DC systems, the operating voltages vary from 1kV to 35kV, but the maximum voltage ratings of the commercially available monolithic IGBT modules usually range from 6.5-8.5kV [6]. The wide-bandgap semiconductors, such as SiC MOSFETs and SiC JFETs, which have a great potential in the SSCB applications because of their low on-state resistances and high junction temperature tolerances, have theoretically higher voltage-blocking capability than the Si switches, but, due to the limitation of the current manufacture crafts, the voltage ratings of their existing

commercial products are commonly set only at 1.2 and 1.7kV [7] [8]. Besides, due to the larger chip thickness and lower manufacturing yield, the costs of the high-voltage modules are much higher than that of their series-connected low-voltage counterparts. As a result, series-connected switches as in Figure 1. 1 appear to be an option more applicable to construct the medium-voltage DC SSCBs [9] [10] [11].

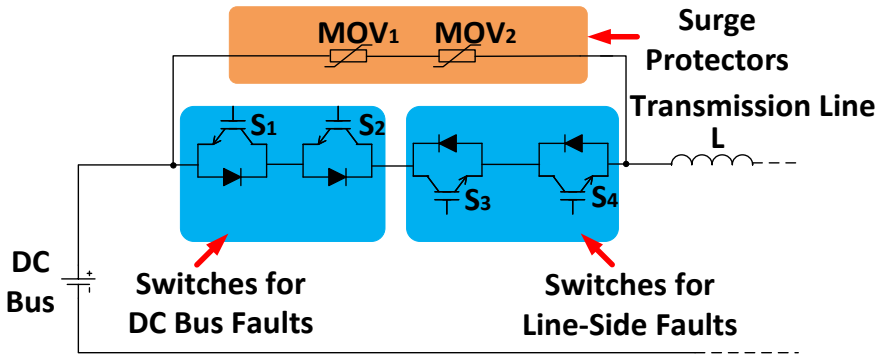


Figure 1. 1 Simplified schematic of the conventional SSCB with series-connected switches.

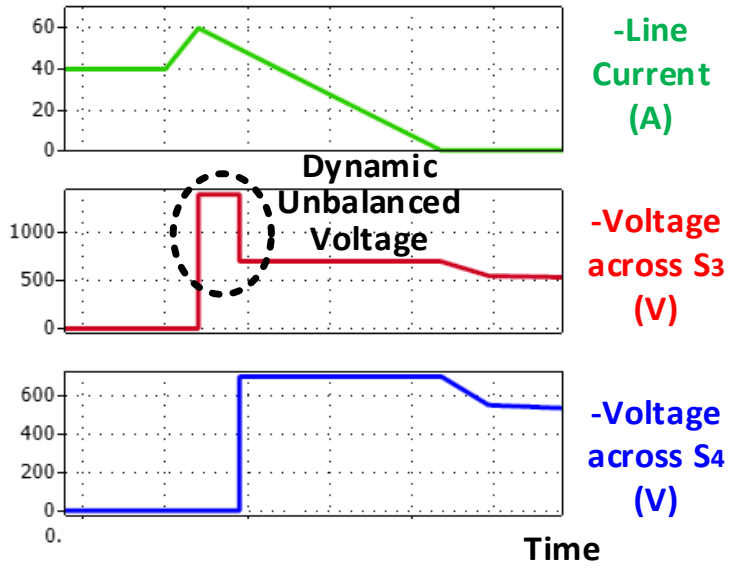


Figure 1. 2 Dynamic voltage unbalancing issue in a conventional SSCB with series-connected switches.

Same as in the other applications of power electronics, the voltage unbalancing among the series-connected switches is also a big concern in SSCBs. Due to the mismatches of the operating speeds of the semiconductor switches and their gate drivers, the series-connected switches may fail to turn off simultaneously during the current interruption of the breaker [12] [13]. As a result, dynamic overvoltage arises across a single switch as shown in Figure 1.2. The overvoltage may exceed the voltage blocking limits of the applied semiconductor switch and cause the failure of the protection.

On the other hand, in SSCBs, back Electromotive Forces (EMF) need to be synthesized across the breakers to absorb the electromagnetic energy stored in the system inductors and ultimately clear the fault current. For the conventional SSCBs, their isolation time changes reversely with the back EMF synthesized from the difference between the clamped surge voltage and the system voltage. In that case, to isolate the faults with a fast speed, the clamping voltages of the surge arrestors in the SSCBs are expected to be much higher than the system voltage [14]. Besides, almost all the commercially available MOVs have clamping voltages much higher than their continuous rated voltage to avert the premature aging on the MOVs during their standby phase [15] [16]. Thus, after MOVs are selected with continuous rated voltages conforming to their system voltages, their clamping voltages will be much higher than the system voltage and enforce the switches in the SSCBs to sustain large surge voltage. Some previous works reduce the surge voltage value of their SSCBs by using the MOVs with continuous rated voltages lower than their applied system voltages. The downsizing of the MOVs causes their repeated intervention after the breakers open and seriously impairs the life spans of the MOVs along with the reliabilities of the SSCBs. For these reasons, large surge

voltage is imposed on the semiconductor switches of the SSCBs as shown in the operating waveforms in Figure 1. 3 [17]. Accordingly, the voltage ratings of the switches cannot be selected as regards their shared system voltages like that in other power electronic applications, but always have to be overdesigned according to their surge voltage values. As the same type of power semiconductor switches with higher breakdown voltages have higher drain-source on-state resistances along with higher cost caused by their thicker drift regions and larger chip thickness, the large surge voltages imposed on the conventional SSCBs seriously impair the efficiencies and cost effectiveness of the breakers.

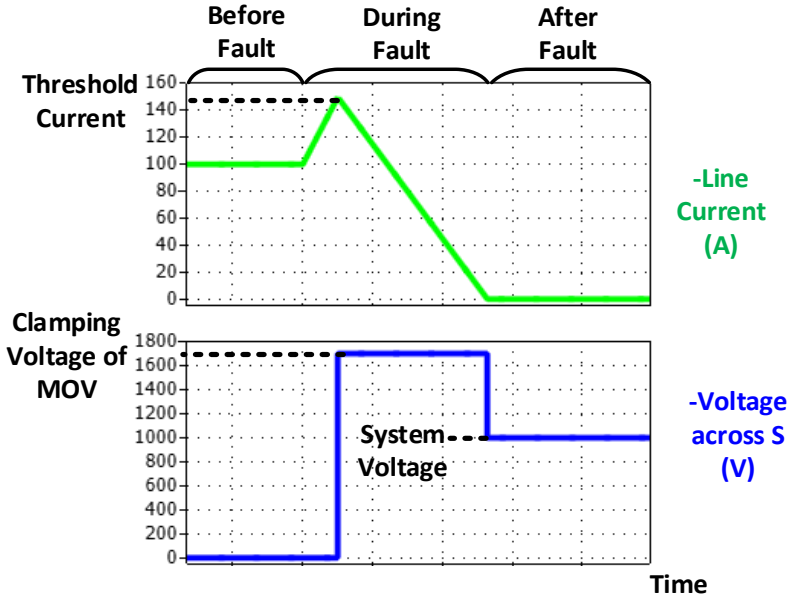


Figure 1. 3 Surge voltage issue in Solid-State Circuit Breaker.

1.2 Proposed Solution to the Dynamic Unbalanced and Surge Voltage Issues

A Multilevel Solid-State Circuit Breaker (MLSSCB) has been proposed in this dissertation to deal with the dynamic voltage unbalancing issue of the series-connected switches. In the proposed MLSSCB, switches are clamped to the voltage dividing

capacitors after they turn off and therefore do not incur dynamic voltage unbalances. Besides, during the operations of the breaker, the switches can be turned off sequentially with significant time differences and basic gate drivers with inherent different working delays can be used in the MLSSCBs. After that, to alleviate the surge voltage across the SSCBs during their operations, two Solid-State Circuit Breaker named Voltage Free Solid-State Circuit Breaker (SVFSSCB) and Ground Clamped Solid-State Circuit Breaker (GCSSCB) have been proposed in this dissertation. In the SVFSSCB, the DC source is actively grounded to minimize the surge voltage on the semiconductor devices during the energy absorbing phase. In the GCSSCB, as its ultrafast fault isolation speed is decoupled from the clamping voltage of its MOV, the MOV and its auxiliary switch can be rated at low voltages and the surge voltage across the breaker can be effectively suppressed. Afterward, by integrating the GCSSCB with the MLSSCB, a Surgeless Multilevel Solid-State Circuit Breaker (SMLSSCB) has been derived to effectively solve both the surge voltage and dynamic voltage unbalancing issues of the conventional SSCB technologies in medium voltage DC distribution systems. Compared to the MLSSCB in the same operating scenarios, the SMLSSCB has faster isolation speed as well as lower demands on the voltage dividing capacitors. Furthermore, compared to the conventional SSCBs, SMLSSCB exhibits both higher efficiency and faster isolation speed. At last, a Fault-Tolerant Multilevel Solid-State Circuit Breaker has been proposed that inherits all the technical advantages of SMLSSCB and also has significantly higher reliability through the fault-tolerant operations.

1.3 Outline of the Dissertation

The rest of the dissertation is organized as follows. In Chapter 2, a review of the latest technologies of SSCBs is made including SCR based SSCB, Si IGCT based SSCB, Si IGBT/SiC MOSFET based SSCBs and SiC JFET based SSCB. The comparisons among the circuit breakers are also included in the chapter. In Chapter 3, the Multilevel Solid-Solid State Circuit Breaker (MLSSCB) is proposed. The operating principle, design considerations and bi-directional configuration of the MLSSCB are discussed in the chapter. In Chapter 4, the operating principles of two surgeless Solid-State Circuit Breakers are presented along with their design considerations and their comparisons with the conventional SSCBs. Chapter 5 presents the concept of the Surgeless Multilevel Solid-State Circuit Breaker (SMLSSCB). The breaker's operating principles, design considerations, comparisons with the conventional SSCB and bi-directional configurations have been dealt with. Chapter 6 introduces the fault-tolerant configuration of the SMLSSCB, or Fault-tolerant Multilevel Solid-State Circuit Breaker (FT-MLSSCB). The operating principle of the breaker has been presented with the simulation results. The comparisons among FT_MLSSCB, SMLSSCB and conventional SSCB have been made on their reliabilities, efficiencies and isolation speeds. Eventually, a chapter of conclusion and future work has been presented.

CHAPTER 2: A REVIEW OF SOLID-STATE CIRCUIT BREAKER

Solid-State Circuit Breaker (SSCB) is an emerging circuit protection technology implementing power semiconductor switches. Unlike the electromagnetic circuit breakers, the SSCBs have no movable units and do not induce electric arc during their current interruption. Besides, thanks to the shorter switching transience of the semiconductor switches, the SSCBs can interrupt fault current in a speed several order of magnitude faster than the mechanical circuit breakers. Moreover, with a high controllability of their semiconductor switches, the SSCBs can perform advanced functions including remote operation, dynamic time-current curve adjustment and system soft start [18].

The general structure of the conventional SSCB is as shown in Figure 2.1. In the figure, the SSCB is mainly composed of semiconductor switches, surge arrestors, current sensors, controller and gate drivers. During normal operation, the semiconductor switch turns on and have load current conduct through it. When a fault happens, the line current starts to increase and gets monitored by the current sensor. Once the current value increases to be higher than the preset threshold, the controller will generate a trip signal to turn the semiconductor switch off and interrupt the increment of the fault current immediately. After that, the fault current is transferred to the surge arrestor where the surge voltage caused by the stray line inductor is clamped. After the surge arrestor absorbs all the energy stored in the line inductor, the line current is cleared and the fault is isolated from the normally operating areas of the system.

Theses years, studies of SSCBs have been mainly focused on introducing emergent semiconductor technologies and developing new circuit topologies aiming to improve the breakers' conducting efficiencies, operating speed and cost effectiveness. As

the topologies of the SSCBs usually varies with the characteristics of their applied switches, in this dissertation, the review of the SSCBs is categorized by the implemented semiconductor switches in the circuit breakers.

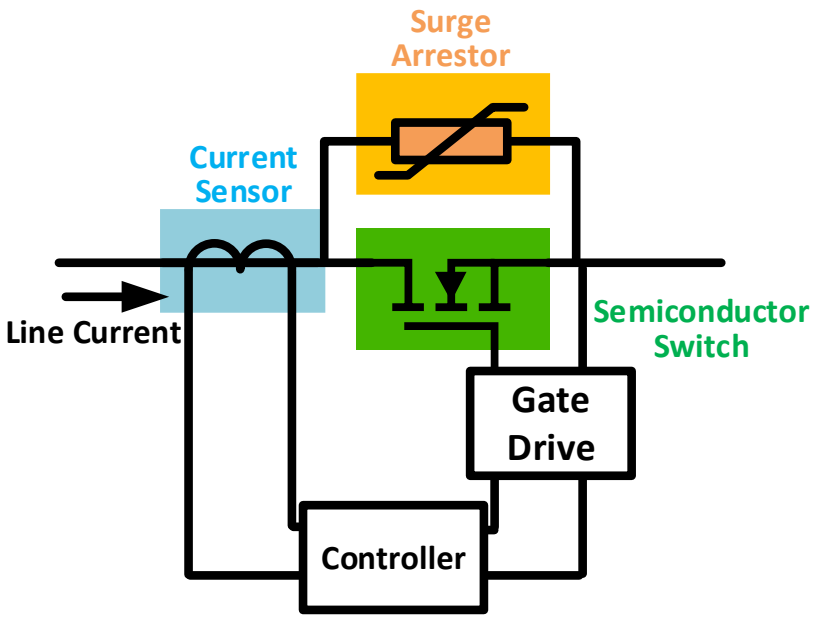
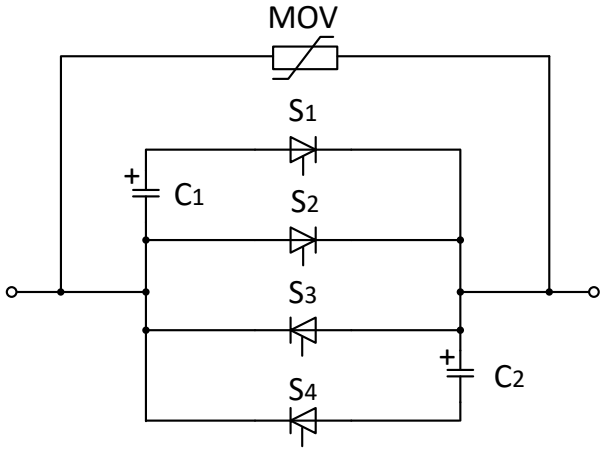


Figure 2. 1 General structure of SSCB

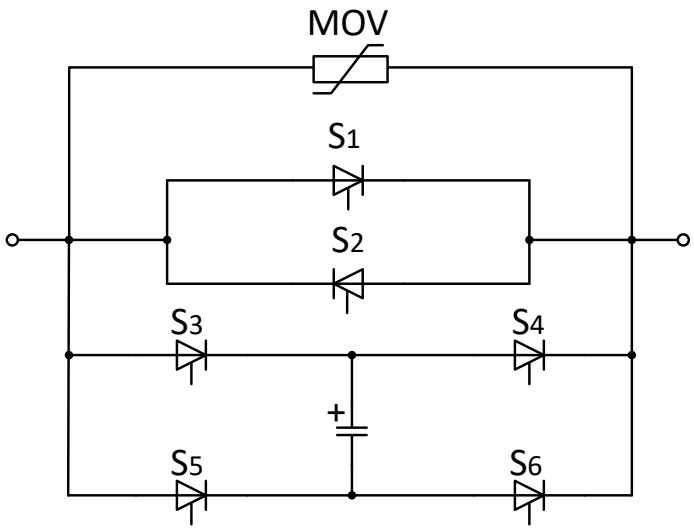
2.1 SCR Based Solid-State Circuit Breaker

Silicon Controlled Rectifier (SCR) is a type of thyristor that have been widely used in power electronics application for rectification of AC to DC. Due to its relatively low conduction loss, high operating power range and low material cost, SCR has been seen as an applicable option to construct SSCBs. As the SCR cannot be actively turned off by its gate signal, an extra auxiliary circuit known as force commutation circuit needs to be designed to forcedly commutate the current thorough the SCR to zero and then turn the circuit breaker off. Owing to the rarity of the switching activity in the SSCB applications, the commutation circuit for the SCR in SSCBs can be well simplified compared to those in power rectifiers.

The simplified schematic of the SCR based SSCBs with basic commutation circuit are shown in Figure. 2.2(a) and (b). In Figure. 2.2(a), the SSCB consists of two antiparallel SCR as its main current conduction paths, two fully controlled switches in series with commutation capacitors as auxiliary paths and a MOV as surge arrestor. During normal operations, SCRs turn on, the auxiliary switches turn off and the load current follows through the SCRs bidirectionally. When the fault happens, the auxiliary switches turn on and provide discharging loop for the commutation capacitors and forcedly transfer the line current from SCRs to the auxiliary paths. After the current through the SCR decreases to zero, the auxiliary switches turn off and transfer the line current to the MOV. Eventually, the line inductor is demagnetized and the breaker clears the line current. To decrease the number of the commutation capacitors and shorten the capacitors' pre-charging periods, a SCR based SSCB with a H-bridge commutation circuit has been introduced as shown in Figure 2.2(b). In the breaker, only a single capacitor is used but, in exchange, two more auxiliary switches are needed to convert the current through the capacitor.



(a)



(b)

Figure 2. 2 Basic SCR based SSCB with forced commutation capacitors.

As the following basic SCR based SSCBs cannot have their commutation capacitors charged by a unidirectional source current, the SSCBs are more suitable for AC systems. In DC application, additional power supplies are needed to pre-charge the commutation capacitors. Although in Figure. 2.2(b), the capacitor can be charged by DC current after adjusting the operating quadrant of the auxiliary switches, additional control loop along with sensors are needed to regulate the pre-charged voltage value.

Several ways have been presented to design SCR based SSCBs without external pre-charging circuits [19]. Nevertheless, these breakers can only charge their commutation capacitors after the breaker closes which enhances the risks of their failure during the reclosing process [20] [21]. A large capacitance can alleviate the drawback, but will compromise the compactness of the breaker.

Lately, a novel SCR based SSCB has been proposed that can charge its commutation capacitor during the period when the breaker is off and do not need extra sensor and source to interrupt current under DC sources. The simplified schematic of the

breaker is drawn in Figure 2.3. All the switches in the breaker are SCRs. During normal operation, the switch, S_1, turns on and conducts load current. When the fault happens, the switches, S_2 and S_3, turn on simultaneously and allow the capacitor provides a reverse current to offset the current through S_1. After the current of S_1 decreases to zero, a resonant loop of the commutation capacitor and line inductor is produced. Once the resonance damps, the switches S_2 and S_3 turn off. At the same time, the diode, D, conducts and recharges the commutation capacitor by the DC source. During the operation of the breaker, the charging/discharging periods of the capacitor need to be compatible to the reverse recovery of the SCR switches and the resonance of the line current. Therefore, the design of the commutation capacitor in the breaker is very challenging to the breakers operating in a wide range of current rating. In addition, as the line current can be eventually cleared only after the resonances between the capacitor and line current are damped, the responding and isolating time of the breaker are significantly longer than the basic SCR SSCBs.

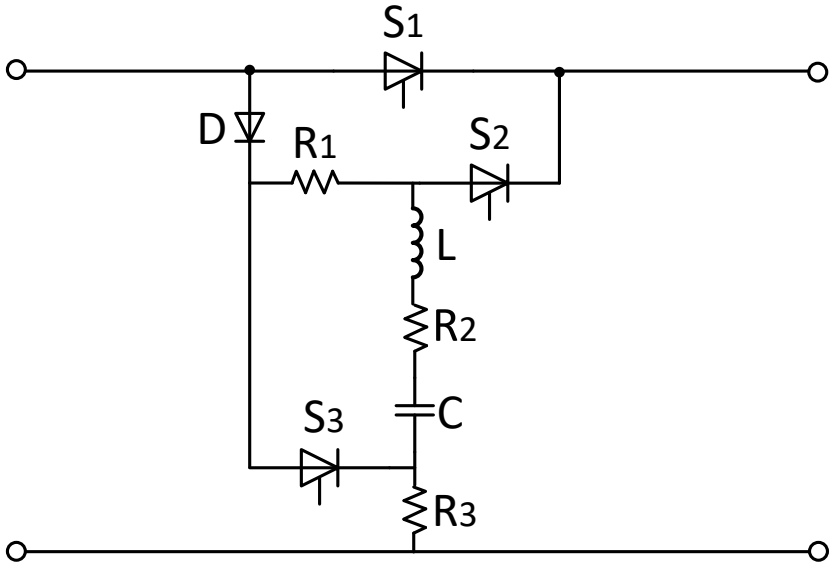


Figure 2. 3 SCR based SSCB in DC system.

To attain a fast fault responding and isolating speed, a series of SCR based SSCB named Z-source SSCB has been proposed arousing the great interests in academia. Compared to the other SCR based SSCB, the Z source SSCB operates autonomously when the fault happens and therefore can have a much faster operating speed. It is worthwhile mention that although the Z source SSCBs do not need control signals to trip their current breaking operation, but they still need sensors and controllers to assist grounding the gate signal of the SCR after the device's current decreases to zero. The schematic of the original Z source SSCB is as shown in Figure. 2.4. In normal situation, load current follows through the SCR and the two inductors in the breaker. At the moment when a fault occurs, the line current starts to conduct through the capacitors in the breaker in that the current increasing rate in the capacitors can be much larger than that in the inductors. Since the total capacitor voltage is twice of the source voltage, the SCR is reverse biased and its current drops to zero at a very fast speed. After that, the fault area is isolated from the DC source and the inductor is resonant with the capacitor until the diode-resistor branch damps the inductor current to zero. From its working principle, the Z source SSCB operates only when the increasing rate of the fault current is sufficiently high. For the fault current having slower transience, the Z source breaker may fail to respond and result in the extension of the faults. Besides, the following researches show that the Z source SSCB also fails to operate when the amplitude of the fault current is not prominent compared to the load current [22].

Several methods have been presented to improve the controllability of the Z source SSCB and make them to operate successfully in different fault scenarios. In [22], the circuit topology modified from the original Z source SSCB has been proposed as in

Figure 2.5. The operating principle of the breaker is similar to the original one except a common ground for the source and the power ground is attained by making a tradeoff of a little isolation speed. Besides, an additional grounding switch is added in the circuit as S_2 in Figure 2.5 to actively ground the Z source SSCB when a fault is detected by the relay and enforce the breaker to operate in less severe fault scenario. In addition, the boundary of the minimum fault current amplitude and ramp rate for the breaker to spontaneously operate has been derived in the paper to determine the working range for the active grounding switch and optimize the responding speed of the breaker. In [23], a Z source breaker with a coupled inductor has been proposed as shown in Figure 2.6. The threshold current value for the breaker's spontaneous operation can be set by adjusting the turn ratio of the coupled inductor. In that case, the controllability of the Z source SSCB can be further improved.

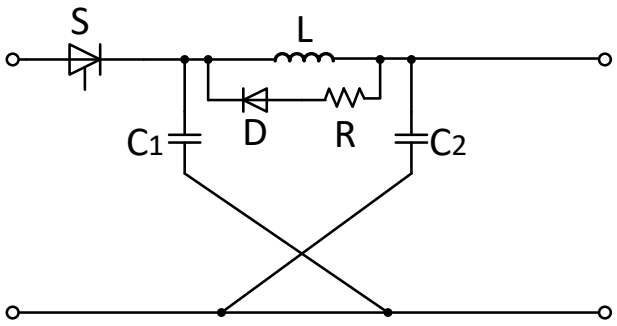


Figure 2. 4 Z source SSCB.

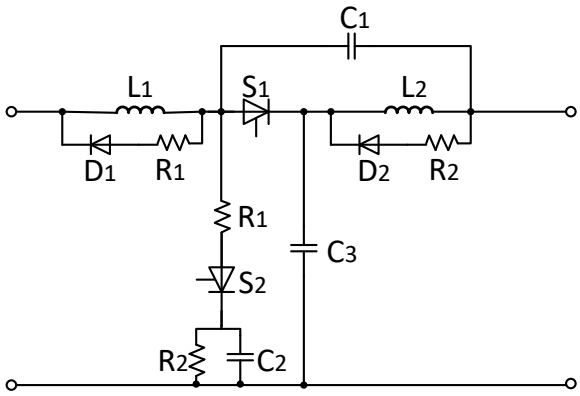


Figure 2. 5 Modified Z source SSCB.

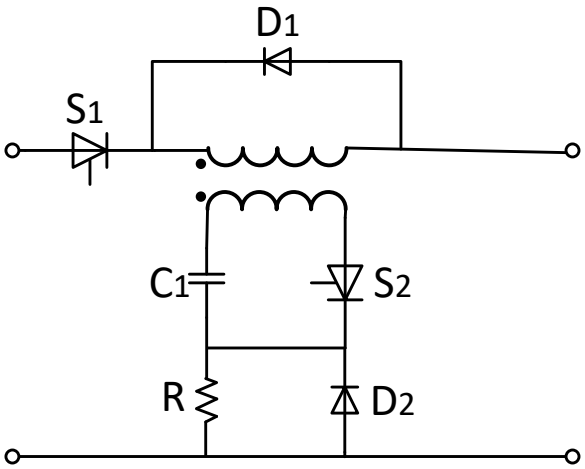


Figure 2. 6 Z source SSCB with a coupled inductor.

Except for the controllability issues, the passive component selection is also a big concern in Z source SSCBs. Since the inductor in the breaker conducts continuous current in normal situations, the size of the inductors and capacitors may be unacceptably large in the applications with high voltage and current ratings.

2.2 Si IGCT Based Solid-State Circuit Breaker

The Integrated Gated-Commutated Thyristor (IGCT) is a type of semiconductor switch related to Gate Turn-Off (GTO) Thyristor. After it is turned on, the IGCT device

operates in deep latch-up mode and has generally higher conduction efficiencies in comparison with their counterparts of fully controlled switches, such as IGBT and MOSFET switches. In exchange, the switching losses of the IGCT switches are relatively higher. With the above attributes, the IGCT devices are well suitable for the applications of SSCB where the switching frequency is extremely low and conduction loss dominate the power losses. In [24], a 2.5kV IGCT switch was applied to a SSCB. Under a testing scenario of 1kV/1.5kA DC system, the on-state voltage across the IGCT device is only 0.9 V, which translates into a principal power efficiency of 99.9%. In [25], a new IGCT semiconductor device named Low On-state voltage Integrated Gate-Commutated Thyristor (LO-IGCT) has been proposed specified in SSCB applications. In the device, the on-state voltage is optimized by reducing the total base length, lowering the doping rate in the base region and prolonging the bipolar length. Although the switching power needed for the device turns out to be higher than the standard IGCT switches, it is not a big concern in the SSCBs. As shown in the experimental results in [25], the proposed LO-IGCT device maintains a significantly lower on-state voltage in a wide range of operating currents compared to the commercialized IGCT switches.

Except for the material characteristics of the IGCT devices, their potential of bidirectional voltage blocking also makes them suitable for the SSCB applications. By integrating its die with a diode, the IGCT device can attain the reverse voltage blocking capability and have a substantial reduced power loss. This type of IGCT switch with expanded operating quadrant is named Reverse Blocking IGCT (RB-IGCT) switch. The RB-IGCT switches can construct bidirectional SSCBs with antiparallel configuration as shown in Figure. 2.7. Compared to IGBT based bidirectional SSCB with two back-to-

back switches, the RB-IGCT based SSCB has one less semiconductor device on its conduction path and therefore can attain improved power efficiency.

In SSCBs, parallel connected switches are applied to enhance their current interrupting limits. However, when it comes to the IGCT devices, due to their negative temperature coefficients, their parallel connection cannot attain a balanced current sharing and may cause over current and temperature imposed on a single switch. In [26], mathematic model has been determined to quantify the effect of the bus bars' stray inductors on the transient current deviation among the devices. Besides, the effectiveness of the devices' threshold voltage, on-state resistance and negative temperature coefficient on the steady-state current sharing of the devices are also discussed. In the paper, the current balancing among three parallel connected 5kA rated IGCT devises is roughly achieved under a 15kA load current by matching the devices' characteristics and carefully deploying bus stray inductors in the breaker as shown in Figure 2.8. Nevertheless, under a long term of operation, the negative temperature coefficient may still compromise the static current balance of the switches. Besides, the current deviation to the changing rate of the current still needs to be further studied.

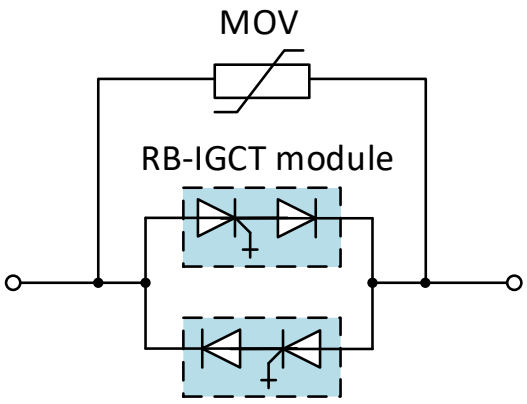


Figure 2. 7 RB-IGCT based bidirectional SSCB.

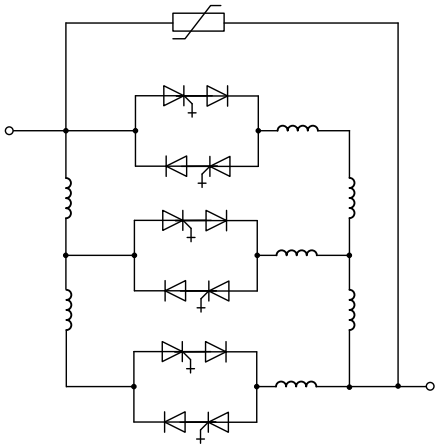


Figure 2. 8 Bus stray inductor deployment in the parallel IGCT based SSCB

2.3 Si IGBT/ SiC MOSFET Based Solid-State Circuit Breaker

Insulated-Gate Bipolar Transistor (IGBT) and Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) are two types of the most-commonly applied semiconductor devices in power converters due to their high technical maturity and low manufacturing cost. IGBTs utilize conduction modulation to attain lower conduction losses [27]. On the other hand, although MOSFETs which are unipolar devices cannot use conductivity modulation to improve their conduction efficiencies, they may take lower conduction losses than their IGBT counterparts by applying Silicon Carbide (SiC)

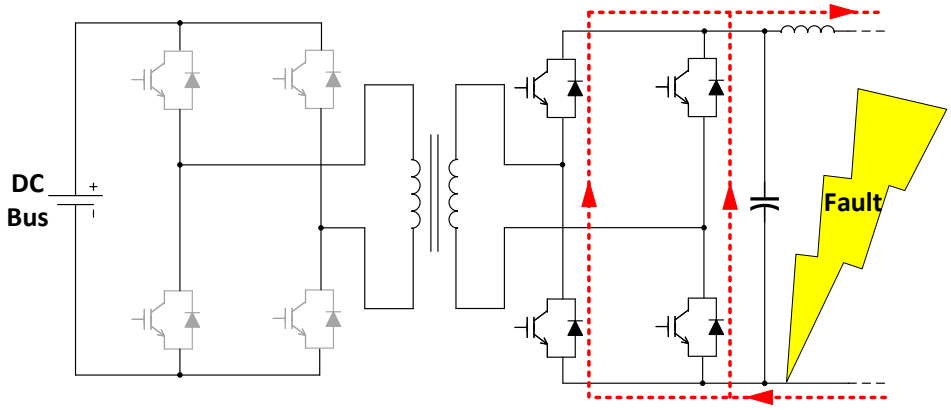


Figure 2. 9 DAB converter based circuit protection.

material [28] [29]. The applications of Si IGBT and SiC MOSFET in solid-state circuit protection have been widely discussed in both industries and academia. The recent studies of the area represent two main trends.

The first is to integrate the circuit protecting function into the power converters and use IGBT/MOSFET in the converters to interrupt the fault current. In [30] [31], a Dual-Active-Bridge (DAB) DC/DC converter has been used to clear a fault happening on the DC microgrid as in Figure 2.9. When there is a fault happening, all the switches of the DAB converter are tripped off and the power source from the AC grid is isolated from the fault through the switches in the inverter phase of the converter. In other words, only the DC bus capacitor, C_2, supplies the fault current. After all the energy stored in the capacitor is discharged, the line current stops increasing and conducts through the free-wheel diodes of the DAB converter as highlighted in Figure 2.9. Eventually, the line current is cleared after the line inductive energy is dissipated by the internal resistor of the power cable.

In the DAB converter based circuit protection, the fault current following through the converter can be interrupted but the line current is only interrupted after the DC bus voltage reduces to zero. Thus, the protection scheme may fail to interrupt the fault current before it increases too much when the fault spot is close to the DC bus. To avert the problem, in [32] [33], the Modular Multilevel Converter (MMC) with H-bridge submodules is used to interrupt the line current when a fault occurs on its DC bus. During the fault, all the switches in the MMC turn off and the current through the MMC is transferred to the conduction loop charging the submodule capacitors as in Figure 2.10. Since then, the increment of the fault current ceases and the DC voltage twice as high as

the original DC bus voltage can be synthesized across the AC source and the line inductor. Consequently, a large negative EMF is introduced over the faulted line and the fault current decreases to zero after the line inductor is demagnetized. Although the H-bridge based MMC can effectively interrupt its line current, it has to use much more power switches than the other half-bridge MMC and correspondingly brings about much higher material costs and conduction losses. Besides, as the back EMF across the faulted line is synthesized by the capacitors in the converter, the capacitance and size of the capacitors needs to be larger for avoiding the overcharge of the capacitors during the fault interruption. For the reasons mentioned above, nowadays, the converters alone can hardly execute effective circuit protection and so the independent SSCBs are seemed to be a more practical way to perform solid-state circuit protection.

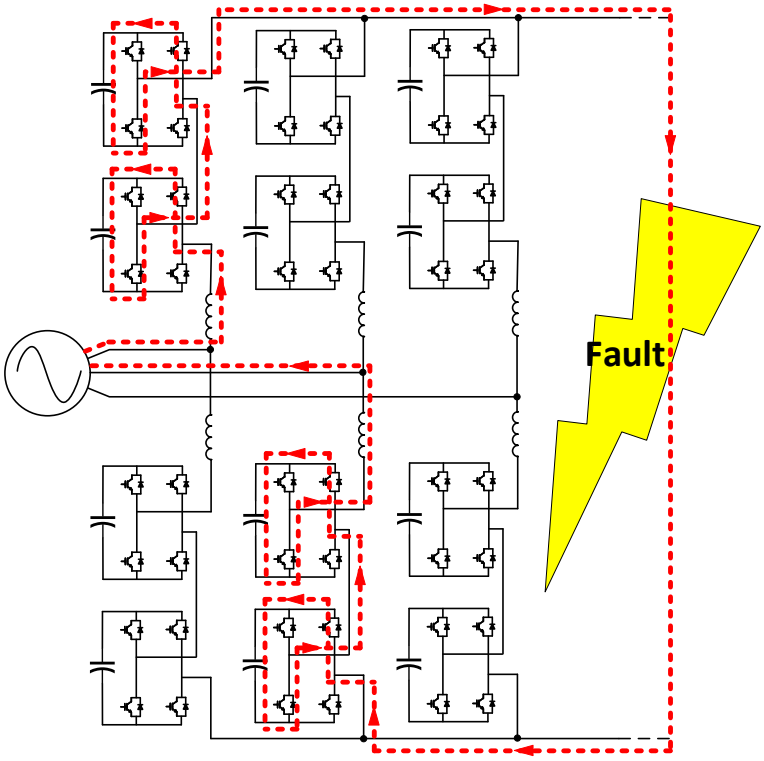


Figure 2. 10 MMC based circuit protection.

Another trend of the IGBT/MOSFET based SSCB is to use the high controllability of the devices to enhance the performances of the breakers. In [34], a SSCB with self-adapting fault current limiting capability has been proposed as depicted in Figure 2.11. In the breaker, an auxiliary source, as V_b in Figure 2.11, is used to sustain a consistent current following though the current limiting inductor, L_r. As the current through D_2 and S_2 tracks the changes in the line current, the current limiter's current stays constant during the normal situations and can be preset according to the current limiting threshold of the breaker. When a fault happens, the line current increases abruptly until it reaches the current limiting threshold. At the moment, the current through D_2 reduces to zero and all the increased amount of current is forced to conduct through the current limiting inductor. Therefore, the increasing rate of the fault current is limited. Unlike the conventional current limiting tactics of directly increasing line inductance, the introduced SSCB inserts the current limiter into the circuit only after a fault happens. In this way, the breaker does not impair the fast transient response of the applied system. In addition, during the energy absorbing process of the breaker, once the

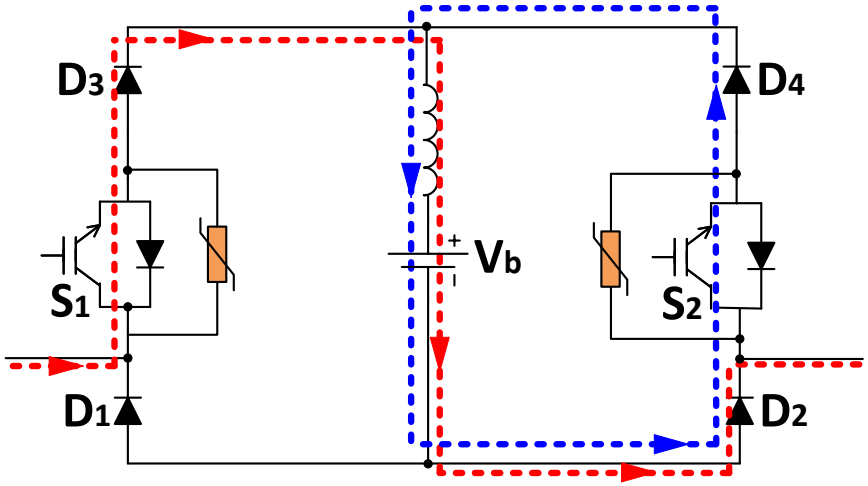


Figure 2. 11 SSCB with self-adapting fault current limiting capability.

line current decreases to be lower than the current limiting threshold, the current limiter is bypassed again and therefore the energy volume of the MOV does not need to be scaled up with the current limiting inductor. At the same time, the isolation time of the breaker is not prolonged significantly by the current limiter.

On the other hand, in [35], a surgeless SSCB with the grounded MOV has been proposed as in Figure 2.12. During its current breaking process, fault current is transferred from the DC bus to the branch of the ground connected MOV after the switch S_1 opens. As the DC bus is bypassed by the diode, D_2, the clamping voltage of the MOV does not need to be higher than the DC bus voltage for synthesizing a negative EMF across the line inductor. For this reason, the surge voltage imposed on the switch during the breaker's operation can be reduced effectively. As a result, the material cost of the breaker may be lower than its counterpart of conventional SSCBs.

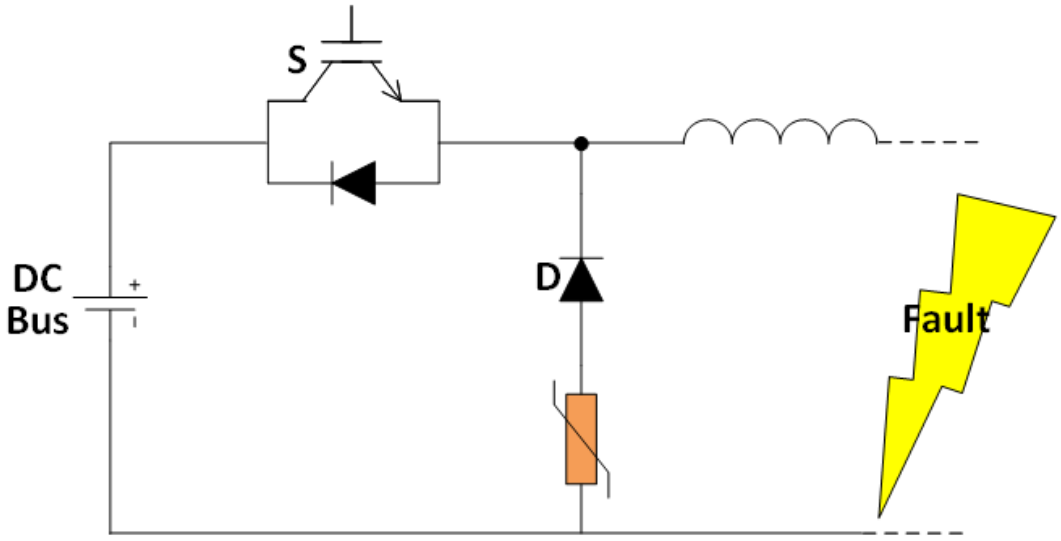


Figure 2. 12 Surgeless SSCB with grounded MOV.

2.4 SiC JEFT based Solid-State Circuit Breaker

SiC Junction-gate Field-effect Transistor (JFET) is an emergent commercialized WBG semiconductor switch. Unlike most of the fully-controlled semiconductor switches, such as IGBT and MOSFET, SiC JFET is normally-on, meaning when there is no drive signal on its gate terminal it maintains on-state and it is turned off only if a negative signal is imposed on its gate. Relying on the normally-on trait, the SiC JFET switches can be applied to the construction of advanced SSCBs, such as self-powered SSCB and supercascode SSCB that have some practical advantages over the conventional SSCBs. Besides, same as the other SiC based semiconductor devices, such as SiC MOSFET, SiC JFET exhibits a very low on-state resistance and a robust performance at high temperature. As regards the energy handling capability, SiC JEFT is potentially better from the testing results in [36]. In addition, without a change of the device structure, the SiC JEFT can further decrease its on-state resistance by shortening the channel length and advance a new semiconductor device named SiC Static Induction Transistor (SiC SIT) [37]. So, it seems that SiC JEFTs have a great potential in solid-state protection industry. Several state-of-art SiC JFET based SSCB with great practical values have been proposed.

Self-powered SSCB utilizes the normally-on characteristics of the SiC JFET devices to realize spontaneous fault interruption and can have a response speed much faster than the SSCBs relying on current sensor and relay [38]. Besides, as its drive energy all drawn from the fault, the breaker does not need any auxiliary sources for its gate driving and the faults happen in the gate driving circuit of the semiconductor switch does not affect the operation of the breaker. The simplified schematic of the self-powered SSCB is shown in Figure 2.13. In the breaker, the output of the DC/DC converter,

namely the gate voltage of the switch, is directly associated with the drain to source voltage of the switch. In normal situation, the voltage across the JFET is low and correspondingly the output voltage of the DC/DC converter sustains lower than the gate threshold voltage of the device. The SiC JFET is turned on and the load current conducts through it. When a fault occurs, the output voltage of the DC/DC converter increases along with the switch's current. While the voltage value is higher than the threshold voltage, the switch turns off and interrupt the fault current. As the polarities of the input and output of the DC/DC converter is reversed, the flyback converter is generally applied to the self-powered SSCB.

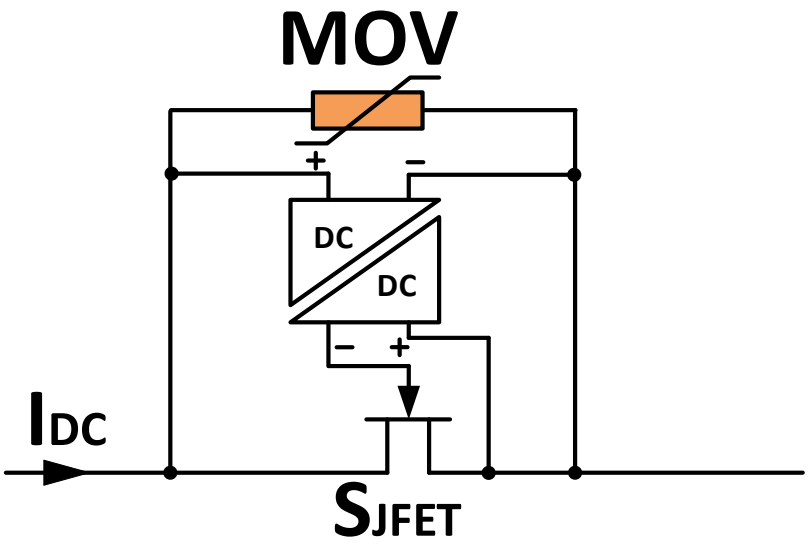


Figure 2. 13 Self-powered SSCB.

Supercascode SSCB is another type of SSCB utilizing SiC JFET switches. With the increment of the voltage ratings, the number of the gate drivers and the isolated DC/DC converters increases along with the number of the series-connected switches in the SSCB. For this reason, the conventional SSCBs in medium/high voltage applications contain a large amount of auxiliary components for gate driving, which enhances their

costs and impairs their reliabilities. The schematic of a typical supercascode SSCB is as drawn in Figure 2.14. From the figure, the supercascode switch of the breaker contains multiple high voltage SiC JEFT switches and a low voltage MOSFET. Only the MOSFET operates relying on the gate driver and the JFETs do not need drivers to switch their states. In that case, by applying the supercascode structure, the number of the auxiliary driving components in the breaker can be effectively reduced and the high voltage isolated DC/DC converters for the gate signals of the upstream switches can be saved. When there is a fault detected, the MOSFET turns off and its drain-to-source voltage enhances and induces a negative voltage across the gate of the J_1. After the amplitude of the voltage exceeds the threshold of the JFET, J_1 turns off and has its drain-to-source voltage starts to increase along with the voltages of the snubber capacitors, C_2 to C_5. When the voltage value is higher than the clamping voltage of the TVS diode, D_2, the voltage of C_2 is clamped and the voltages of C_3 to C_5 keep increasing. When the voltage difference between C_2 and C_3 is higher than the threshold of the SiC JEFTs, J_2 turns off. Similarly, J_3, J_4, J_5 turns off sequentially. After J_5 turns off, the whole line current is transferred from the supercascode circuit to the MOV and decreases to zero gradually. After the fault is cleared, the breaker operates to reclose. The low voltage MOSFET turns on firstly and then the gate voltage of J_1 drops to zero. After J_1 turns on, the snubber capacitor C_2 discharges and the gate voltage of J_2 reduces to zero. Similarly, the Switches, J_3, J_4, J_5, turn on sequentially and the power supply of the loads restores.

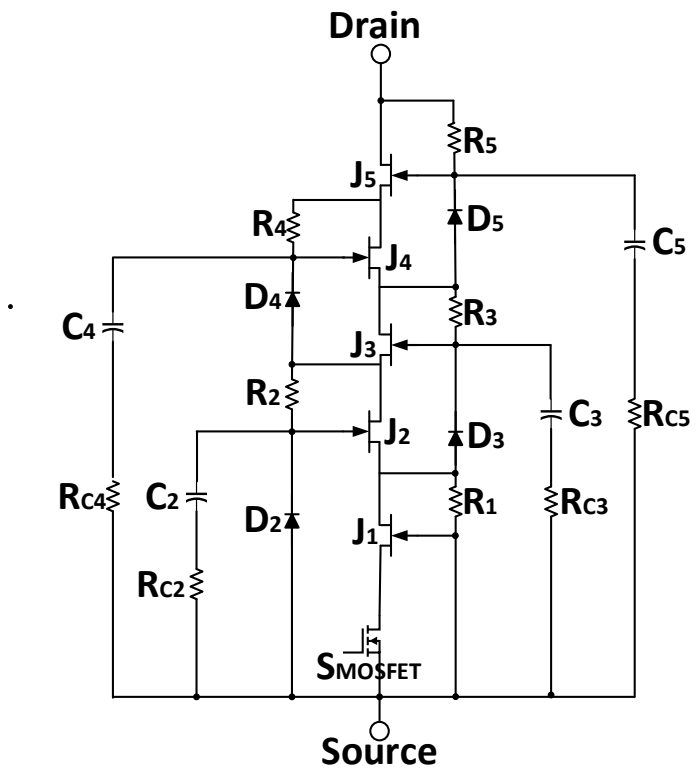


Figure 2. 14 Supercascode SSCB.

2.5 Comparisons of the Reviewed Solid-State Circuit Breakers

In this chapter, the existing SSCB technologies have been reviewed in the categories of the semiconductor devices applied to these breakers. From the reviews, the SCR based SSCBs present benefits of large power ratings, high conduction efficiencies and low material costs. However, as the SCR switches cannot be actively turned off, additional commutation circuits are required, which makes the design of the SCR based SSCB sophisticated and impairs the reliability of the breaker. The IGCT based SSCBs are also compatible to high voltage/current applications. Besides, the reverse current blocking capability of the RB-IGCT allows it to perform bi-directional current interruptions in an anti-parallel structure. Thus, unlike other SSCBs, the RB-IGCT based

SSCB does not trade off its power efficiency for its bidirectional protection capability. Due to the negative temperature coefficients of the IGCTs, the parallel connected IGCT may fail to share equal amount of current and the effective solution for the current deviation problem still needs further studies. The Si IGBT and SiC MOSFETs based SSCB have a wide range of power ratings that cover most applications of power electronics due to the wide uses of the semiconductor devices. Furthermore, the high controllability and fast transience of the devices enables the breakers to perform advanced functions such as surge voltage suppression and self-adapting current limiting. The SiC JEFT based SSCBs seem to have lower power ratings due to the contemporary low maturity of the device. Nevertheless, counting on the normally-on attribute, SiC JEFT based SSCB can operate without sensor and relays in the self-powered topology and perform with only a single gate driver in a supercascode configuration containing multiple series-connected SiC JFETs. The main attributes and comparisons of the reviewed SSCBs have been summarized in TABLE 2-1. In the table, the voltage ratings and the current ratings of the breakers are determined by the parameters of their semiconductor devices. The voltage ratings of the breakers are set to be 1/1.5 time of the ratings of semiconductor switches to ensure the breakers to sustain the surge voltages during their operations and the current ratings of the breakers are 1/1.5 time of the switches' ratings considering the increment of current during the breaker's response time.

TABLE 2 - 1: Comparisons among the Reviewed Solid-State Circuit Breakers

SSCBs Categories	Voltage Ratings (kV)		Current Ratings (A)	Typical Topologies	Fault Current Limiting	Fast Fault Isolation	Fast Fault response	Surge Voltage Suppression	Design Complexity	Size
SCR Based SSCB	(2.8~6.5)/1.5		(1405~2630)/1.5	SSCB with Commutation Capacitors					Medium	Medium
				Z Source SSCB	√	√	√		High	Large
Si IGBT/ SiC MOSFET based SSCB	IGBT	(0.05~6.5)/1.5	(50~3600)/1.5	Self-Adapting Current Limiting SSCB	√			√	High	Medium
	SiC MOSFET	(0.65~1.7)/1.5	(5~765)/1.5	Surgeless SSCB with Ground MOV		√		√	Medium	Medium
IGCT Based SSCB	(2.8~4)/1.5		(1290~2660)/1.5	RB-IGCT Based SSCB					Low	Medium
SiC JFET Based SSCB	(0.65~1.7)/1.5		(3.4~85)/1.5	Self-Powered SSCB			√		Medium	Small
				Supercascode SSCB					High	Large

CHAPTER 3: CONCEPT OF THE PROPOSED MULTILEVEL SOLID-STATE CIRCUIT BREAKER

These years, low-voltage SSCBs have gradually become technically mature and started to come into market. However, with the increment of the operating voltage, series-connected switches are needed in the conventional SSCBs and result in dynamic voltage unbalance among the switches. The series-connected devices may fail to turn off simultaneously because of the different dynamic performances of both switching devices and gate drivers, which causes overvoltage across a single switch when the SSCBs open. Serval auxiliary circuits dealing with the voltage transient unbalancing problem were proposed in [39]. However, these auxiliary circuits increase the complexity of SSCBs and may fail to maintain the switches' voltage balance in some cases. To solve the problem, a new Multilevel Solid-State Circuit Breaker (MLSSCB) has been proposed in this dissertation. In the proposed SSCB, switches are turned off sequentially rather than simultaneously during the faults. The voltages across the switches depends on the voltages of the capacitors associated with the switches and the camping voltage of the MOVs. Hence, the voltage dynamic unbalancing issues can be averted in the MLSSCB and the voltage imposed on the switches can be assured lower than their voltage blocking limits. Besides, the requirement for the total clamping voltage of the MOVs in the MLSSCB is much lower than that of the conventional SSCB so that the surge voltage induced during the breaker's operation is effectively reduced. The working principles of the snubber circuits for dynamic voltage unbalancing issues and the proposed MLSSCB are presented here along with the design considerations of the MLSSCB.

3.1 Conventional Snubber Circuits for Dynamic Voltage Unbalancing Issues

Capacitor snubber circuits have been widely applied to the disposal of the dynamic voltage unbalance among the series-connected semiconductor switches. In the snubber circuit as depicted in Figure 3.1, the capacitors are equally placed in parallel with each of the switches on the series-connected string to provide transient current paths that bypass the early recovered semiconductor devices and allow the latterly recovered switches to recover and to support the source voltage. The minimum required capacitance of the snubber capacitor has been determined as in Expression (3.1) under the worst scenario where a single switch recover for zero charge and the others only recover when they attain their maximum required recovery charge.

$$C_{sb} \geq \frac{(n_s-1)Q_{max}}{n_s(1-k_s)V_{sn}} \tag{3.1}$$

In the expression, $n_s$is the number of the series-connected switches, Q_{max} is the maximum recovery charge of the semiconductor switch provided by the manufacturers, V_{sn} is the rated voltage of the switches and k_s is the voltage sharing factor equaling $\frac{V_{DC}}{n_s}/V_{sn}$ and indicating the voltage margin of the selected switches in the applied system.

Although the snubber circuit can effectively obviate the dynamic overvoltage among the semiconductor switches caused by their different recovering speed, the dynamic voltage balance among the devices still cannot be guaranteed because of the potential asynchronous delay in the switches' gate drivers and controllers [40]. For this reason, exclusive gate drivers are usually used along with the snubber circuits, which increases the complexity and impairs the reliability of the design. In addition, the

capacitive snubbers bring about large surge current when the switches turn on, which may damage the switches and cause their misoperation during the reclosing [25]. For these drawbacks, the existing technologies of the snubber designs may not be sufficient to solve the dynamic voltage unbalancing issue in the Solid-State Circuit Breakers that have a high demand on the reliability of their switches' operations. To deal with the dynamic voltage unbalance in the conventional SSCBs, the Multilevel Solid-State Circuit Breaker has been proposed in this dissertation as a competitive alternate to the conventional snubber based strategies.

3.2 Operating Principle of the Multilevel Solid-State Circuit Breaker

The general structure of the MLSSCBs in 3 level and n level are drawn in Figure 3.2(a) and (b). The levels of the breakers here are determined by the numbers of the voltage levels across the faulted areas during the breakers' operation. The MLSSCB is mainly composed of the semiconductor switches for current interrupting and voltage blocking, the capacitors for voltage dividing and the diodes for clamping the switches' voltage to the different voltage levels of the breaker.

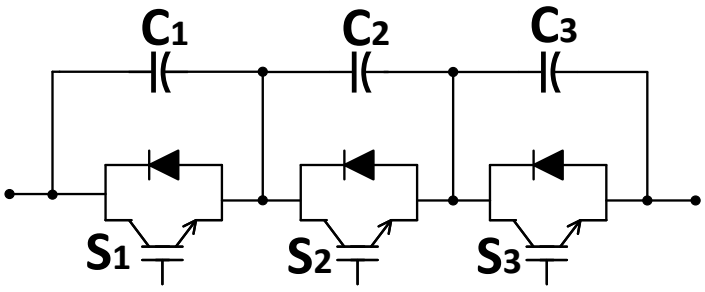


Figure 3. 1 The conventional capacitive snubber circuit for series-connected switches.

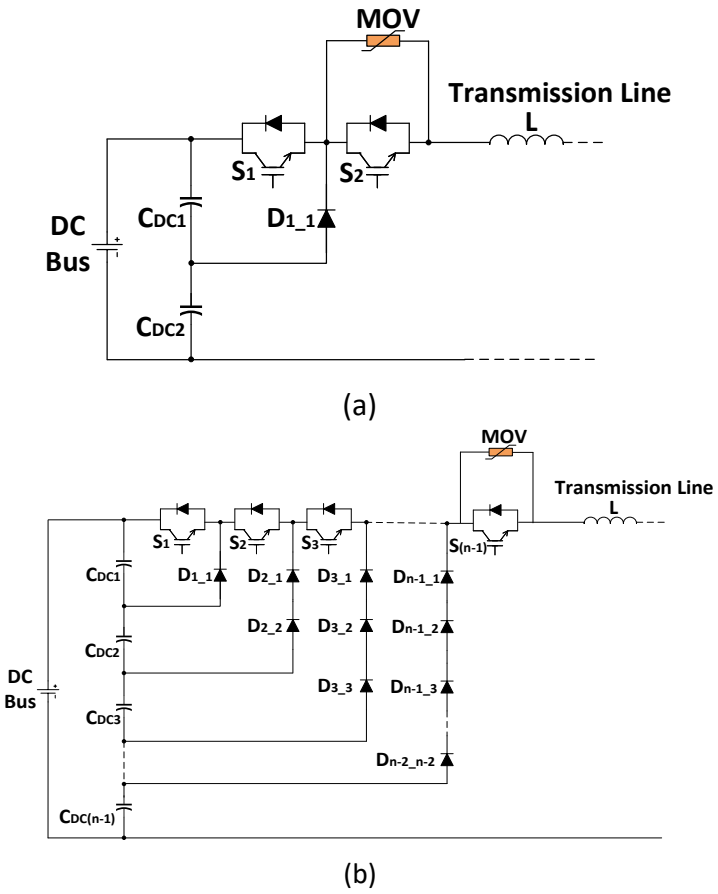


Figure 3. 2 Multilevel SSCB. (a) 3 level SSCB. (b) n levels.

In the MLSSCB, the capacitors, C_{DC1} to C_{DCn}, work as voltage dividers and have the same capacitance to share the DC-bus voltage equally. After the switches turn off, the voltages across the switches will be clamped to the voltage of the capacitors, equaling the DC bus voltage divided by the number of the capacitors. In other words, the operating voltage of the breaker can be as high as the product of the employed switches' rated voltage and the switches' number.

The subintervals of a 3-level MLSSCB dealing with a line-side fault are shown in Figure 3.3 and the simulation waveforms are shown in Figure 3.4 depicting the line

current as well as the voltage of switches in the breaker when the breaker operates. During normal operations, all the switches are turned on and the conduction path through the MLSSCB is as shown in Figure 3.3(a). Whenever the relay detects the line-side fault current exceeding the threshold current, Switch S_1 will be tripped to open and transfer the fault current to the conduction loop shown in Figure 3.3(b). During this subinterval, the voltage across the fault is decreased to half of the DC-bus voltage, so the increment of the fault current slows down as shown in Figure 3.4 from t_1 to t_2. After a short period of delay time, S_2 is turned off and the fault current is commuted into the MOV where the energy stored in the transmission line is absorbed. After that, the fault current decreases gradually to zero as shown in Figure 3.4 from t_2 to t_3. It can be seen from the waveforms of the voltages on S_1 and S_2, that the two switches are not turned off at the same time and there is no overvoltage imposed on either of the switches during the whole breaking process. This demonstrates that the proposed MLSSCB does not incur dynamic voltage unbalancing issues. After the fault is cleared, the static voltage balance among the switches can be easily attained by connecting snubber resistors in parallel with each of the switches. Therefore, if the capacitor values are properly selected, there will be neither dynamic nor static overvoltage imposed on the devices. Consequently, auxiliary circuits for voltage dynamic balancing of the switches are not needed in this topology. The experimental waveforms are also achieved for a 3-level MLSSCB in a laboratory-scale short-circuit scenario as shown in Figure 3.5. The experimental results conform to the simulation results of the proposed breaker and its operating principles get further validated.

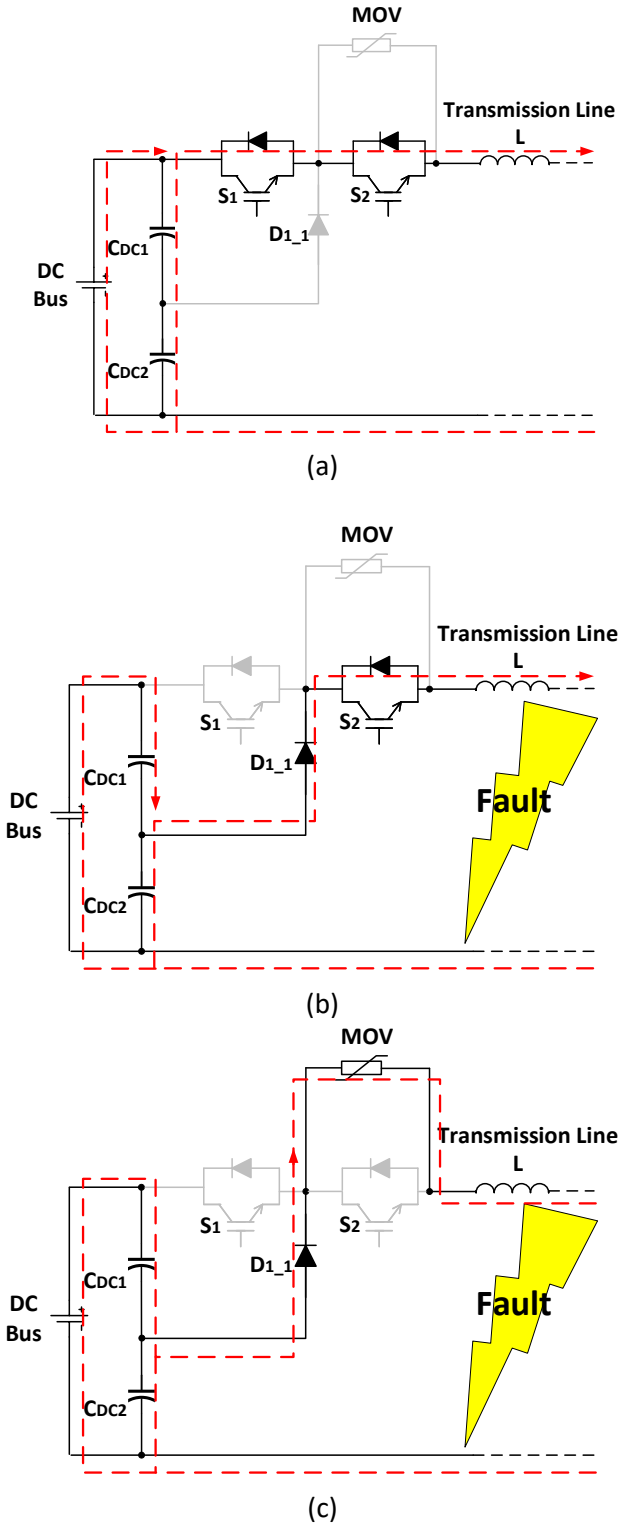


Figure 3. 3 Subintervals during the MLSSCB's operation.

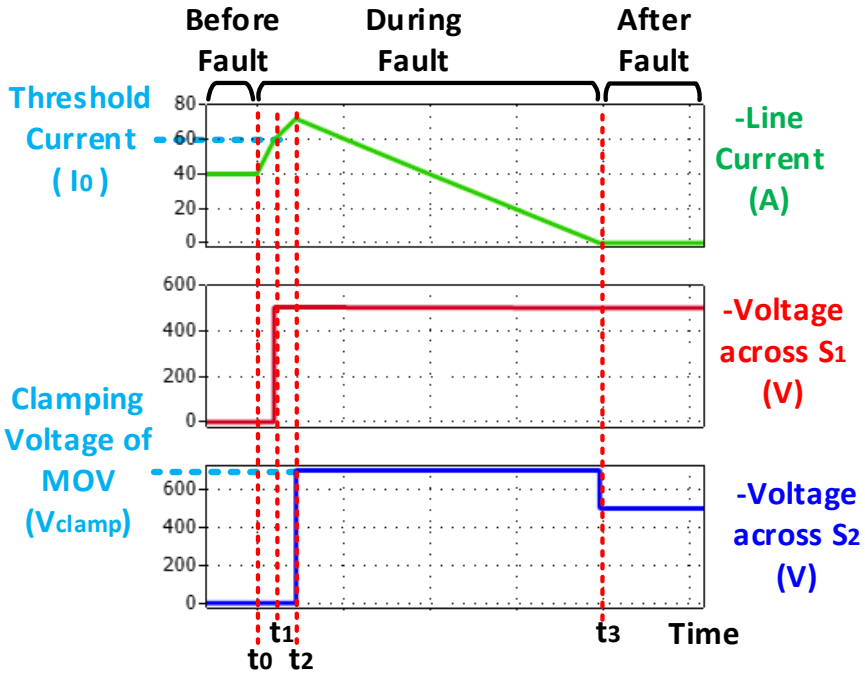
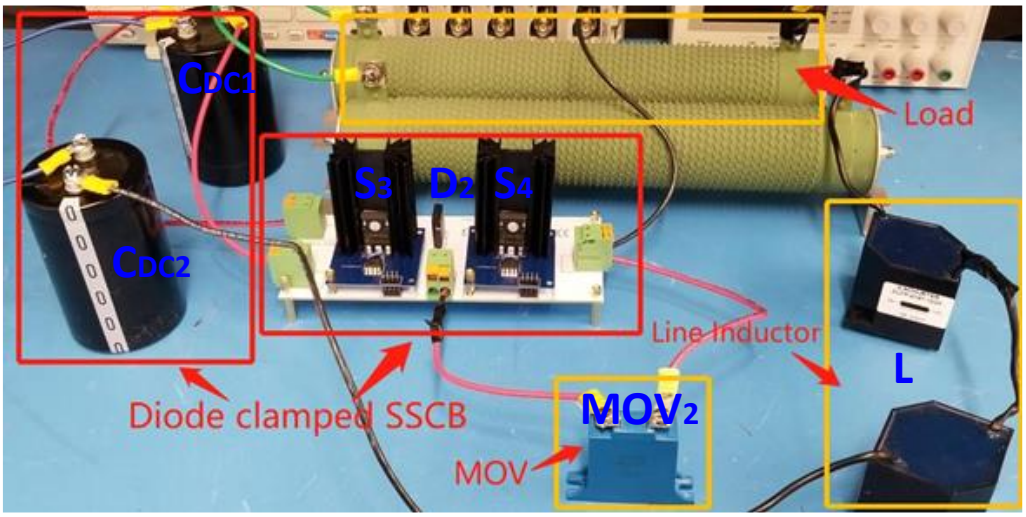
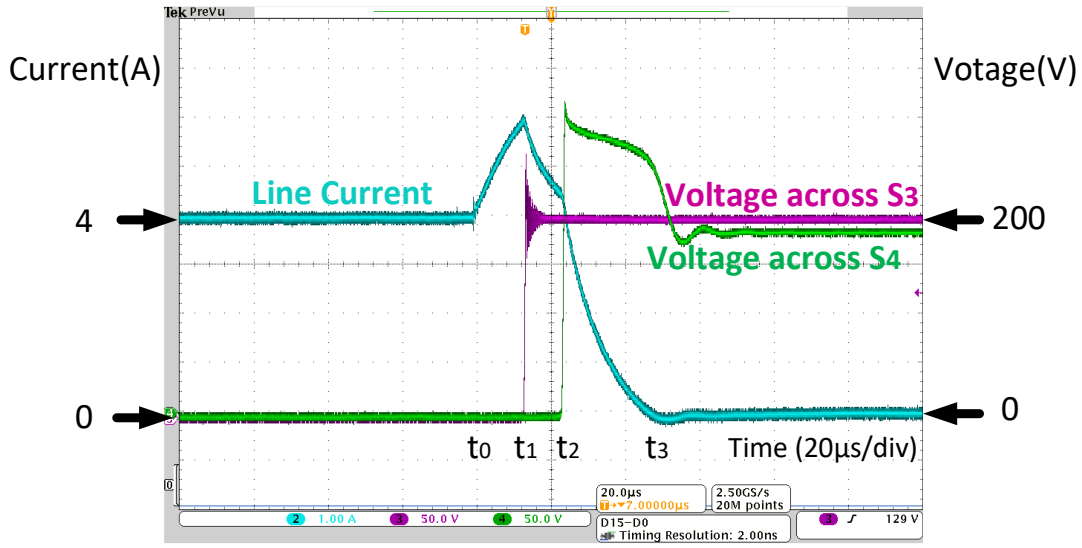


Figure 3. 4 Simulation waveforms of a 3-level MLSSCB during its circuit breaking process ($C_{DC1} = C_{DC2} = 0.5mF$, $V_{DC} = 1000V$, $I_{load} = 40A$).



(a)



(b)

Figure 3. 5 Experiments of a 3-level MLSSCB during its circuit breaking process ($C_{DC1} = C_{DC2} = 1mF$, $V_{DC} = 400V$, $I_{load} = 4A$). (a)Experimental setup. (b)Experimental results.

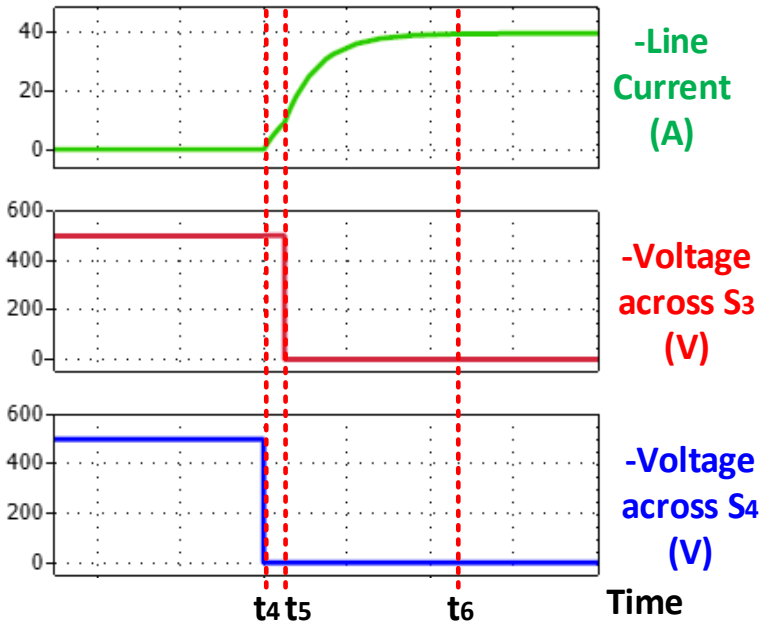


Figure 3. 6 Simulation waveforms of a 3-level MLSSCB during its reclosing process.

After the fault is cleared, the circuit breaker needs to be reclosed to restore the power supply for the load. By means of proper gate signals, the MLSSCB can be reclosed without the voltage unbalancing issues. There is no auxiliary devices or external sources required to reclose the proposed breaker. The simulation waveforms of the Diode Clamped SSCB during it reclosing process are plotted in Figure 3.6. In the waveforms, S_2 is turned on first at t_4 and followed by S_1 at t_5. Since the switches in the breaker have their voltage clamped by the capacitors when they are off, they do not incur any overvoltage while they are reclosed sequentially with a time difference between t_4 and t_5. After a short period of time for the line inductor to be charged, the line current increases to the rated current at t_6 and then the power supply to the load is restored.

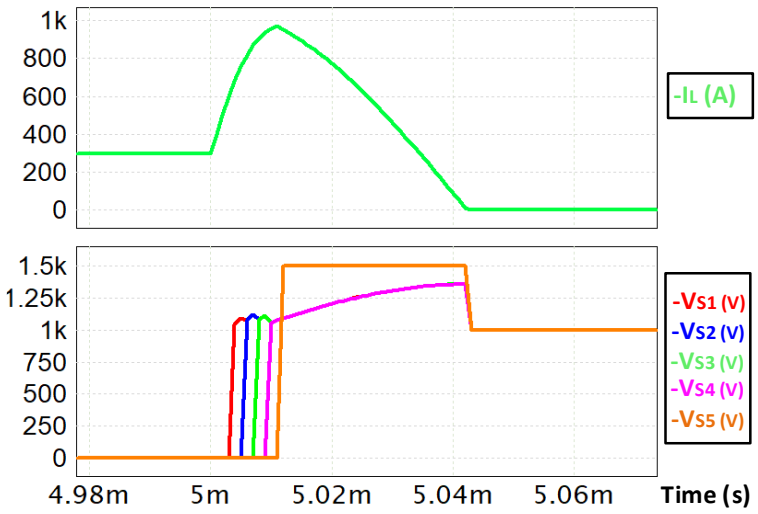


Figure 3. 7 Simulation waveforms of a 6-level MLSSCB during its circuit breaking process ($C_{DC1} = C_{DC2} = 12\mu F,\ V_{DC} = 5000V,\ I_{load} = 300A$).

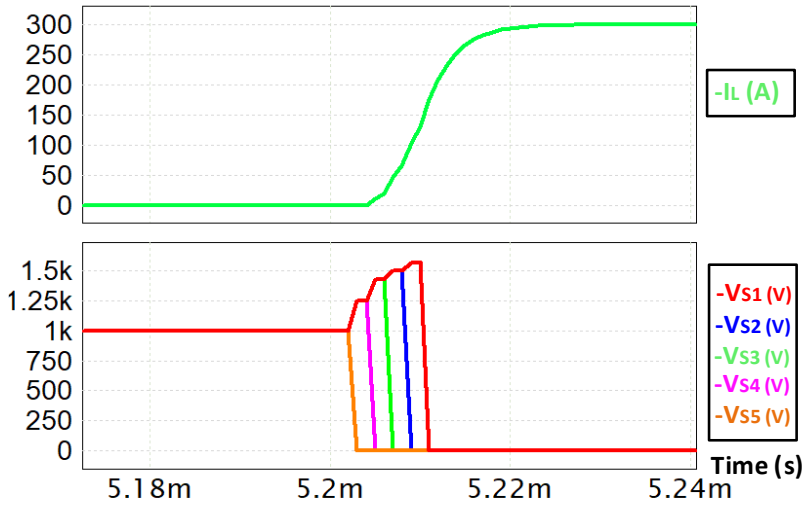


Figure 3. 8 Simulation waveforms of a 6-level MLSSCB during its circuit reclosing process ($C_{DC1} = C_{DC2} = 12\mu F,\ V_{DC} = 5000V,\ I_{load} = 300A$).

The opearting process of the 3-level MLSSCB may be easily extended to the n-level MLSSCB. The simulation results of a 6-level SSCB during its circuit breaking and reclosing are drawn in Figure 3.7 and Figure 3.8 respectively.

3.3 Design Considerations of the Multilevel Solid-State Circuit Breaker

To warrant the normal operation of the MLSSCB, several technical considerations need to be made during the design of the breaker. First, the capacitances of the capacitors, C_{DC1} to C_{DCn}, need to be selected carefully to avert the overvoltage imposed on the switching devices after the interruption of current. Second, the energy required to be absorbed during the breaking process should be quantified to make sure that the energy volume of the selected MOV is large enough for the situation. Finally, special considerations have been taken into of the selection of the semiconductor devices in the

breaker design to make the selected devices meet the requirements of operating voltage, operating current and conduction efficiency of the applied system.

3.3.1 Capacitor Selection

In Figure 3.2 (a) and (b), after Switch S_1 opens, the line current in the breaker is transferred to the conduction loops charging capacitor C_{DC1}. At the same time, the voltage across C_{DC1}, V_{CDC1}, increases gradually until the line current is extinguished by the breaker. As the voltage across S_1 is clamped by C_{DC1} when the breaker recloses, the voltage increment on C_{DC1} is imposed directly on the Switch S_1. With the enhance of the levels of the breaker, the voltage increment also occurs on other switches but is always the most serious in the switch S_1 as shown in Figure 3.8. To avert the damages on the switches during the breaker's operation, the value of V_{CDC1} should be limited below the rated voltage of S_1 and this can be achieved by the proper selection of the capacitors. Since all the capacitors in the breaker have equal capacitances, after the voltage of S_1 is suppressed successfully, the voltages across the other switches are also limited under their voltage ratings.

If the breaker detects the fault and starts to operate at the time instant when $t = 0$, the increment of V_{CDC1} can be expressed as

$$\Delta V_{CDC1} = \frac{1}{C_{DC1}} \int_0^{T_{iso}} i_{CDC1}(t)\, dt$$

$$= \frac{1}{C_{DC1}} \left[\int_{0}^{T_d} \frac{n-2}{n-1} i_L(t)\, dt + \int_{T_d}^{2T_d} \frac{n-3}{n-1} i_L(t)\, dt + \cdots + \int_{(n-3)T_d}^{(n-2)T_d} \frac{1}{n-1} i_L(t)\, dt \right.$$

$$\left. + \int_{(n-2)T_d}^{T_{iso}} \frac{1}{n-1} i_L(t)\, dt \right] \qquad 3.2$$

where T_d is the delay time between the adjacent switches, T_{iso} is time for the breaker to isolate the fault from the DC bus and n is the level of the breaker and ΔV_{CDC1} is the voltage margin of the semiconductor switch equaling the difference between the switch's rated voltage and the theoretical voltage shared by the switch in steady state.

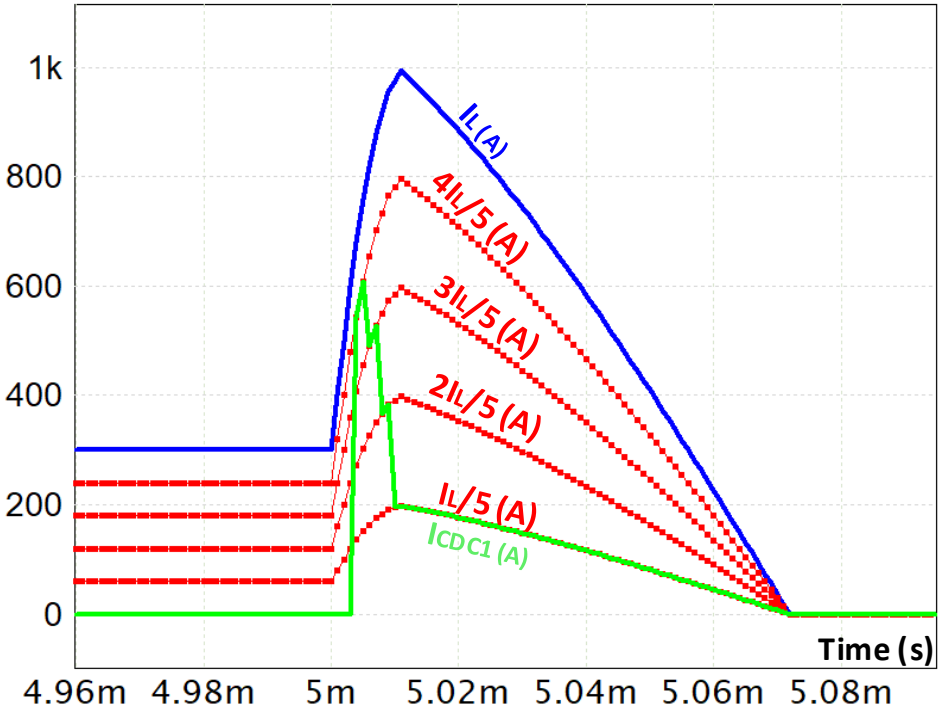


Figure 3. 9 The relationship between i_L and i_{CDC1}.

With the change of the conduction loop charging or discharging the capacitors, the capacitor current steps down during the operation of the MLSSCB and the relationship between the capacitor current and line current can be illustrated in the simulation result of Figure 3.9. Thus, i_{CDC1} can be substituted by i_L as in the Equation (3.2).

The expression of line current has also been determined as in the Equation (3.3). As the inductor voltage steps down during the current breaking of the MLSSCB, the Equation (3.3) changes in different subintervals of the breaker. In (3.3), V_{CLAMP} stands the clamping voltage of the MOV applied to the breaker.

$$i_L(t) = I_0 + \frac{1}{L}\int_0^{T_{iso}} V_L(t)\,dt$$

$$= \begin{cases} I_0 + \frac{1}{L}\frac{n-2}{n-1}V_{DC}t, & 0 \le t \le T_d \\ I_0 + \frac{1}{L}\frac{n-2}{n-1}V_{DC}T_d + \frac{1}{L}\frac{n-3}{n-1}V_{DC}(t-T_d), & T_d \le t \le 2T_d \\ \vdots & \\ I_0 + \frac{1}{L}\frac{n-2}{n-1}V_{DC}T_d + \frac{1}{L}\frac{n-3}{n-1}V_{DC}T_d + \cdots + \frac{1}{L}\frac{1}{n-1}V_{DC}[t-(n-3)T_d], & (n-3)T_d \le t \le (n-2)T_d \\ I_0 + \frac{1}{L}\frac{n-2}{n-1}V_{DC}T_d + \frac{1}{L}\frac{n-3}{n-1}V_{DC}T_d + \cdots + \frac{1}{L}\frac{1}{n-1}V_{DC}T_d & \\ \quad + \frac{1}{L}(\frac{1}{n-1}V_{DC} - V_{CLAMP})[t-(n-2)T_d], & (n-2)T_d \le t \le T_{iso} \end{cases} \quad 3.3$$

By inserting (3.3) to (3.2), the capacitance value of C_{DC1} that can maintain the voltage change of the capacitor lower than the margin of switches' voltage rating may be

determined as

$$C_{DC1} = \frac{1}{\Delta V_{CDCmax}}\left\{\sum_{a=1}^{n-2}\frac{a}{n-1}I_0T_d + \frac{1}{n-1}I_0T_{MOV} + \left[\frac{1+2+\cdots(n-2)}{n-1}\ \ \frac{1+2+\cdots(n-3)}{n-1}\ \ \cdots\ \ \frac{1}{n-1}\right]\begin{bmatrix}\frac{n-2}{n-1}\\ \frac{n-3}{n-1}\\ \vdots \\ \frac{2}{n-1}\end{bmatrix}\frac{1}{L}V_{DC}{T_d}^2 + \sum_{a=1}^{n-2}\left(\frac{a}{n-1}\right)^2\frac{1}{L}V_{DC}\frac{{T_d}^2}{2} - \frac{1}{5}\frac{1}{L}EMF\frac{{T_{MOV}}^2}{2} + \sum_{a=1}^{n-2}\frac{1}{5}\frac{a}{5}\frac{1}{L}V_{DC}T_dT_{MOV}\right\} \quad 3.4$$

where *EMF* represents the back Electromotive Force synthesized across the line inductor for demagnetizing the inductor, ΔV_{CDCmax} represents the largest voltage deviation that the switch can sustain and T_{MOV} represents the operating time of the MOV. The value of T_{MOV} can be expressed as

$$T_{MOV} = (I_0 + \frac{1}{L}\frac{n-2}{n-1}V_{DC}T_d + \frac{1}{L}\frac{n-3}{n-1}V_{DC}T_d + \cdots + \frac{1}{L}\frac{1}{n-1}V_{DC}T_d)\frac{L}{EMF} \quad 3.5$$

TABLE 3 - 1: Key Parameters in the Simulation Case

Parameters	Values
DC bus voltage V_{DC}	5000V
Line current I_L	400A
Line inductor L	50μH
Voltage divider C_{DC}	66μF
Clamping voltage V_{clamp}	1500V
Threshold current I_0	$1.5 \cdot I_L$

The proposed capacitor selection scheme for the MLSSCB has been validated in a simulation case with the parameters in TABLE 3-1. According to the Equation (3.4), the capacitor value in the case equals 66μF. The simulation results are shown in Figure 3.10. In the figure, although the voltage across S_1 increases while the capacitor, C_{DC1}, gets charged and reaches the capacitor voltage when the breaker recloses, the switch's voltage are suppressed to be lower than its voltage rating of 1200V during the whole operating process of the breaker. Therefore, the simulation results conform to the results of the mathematic analysis.

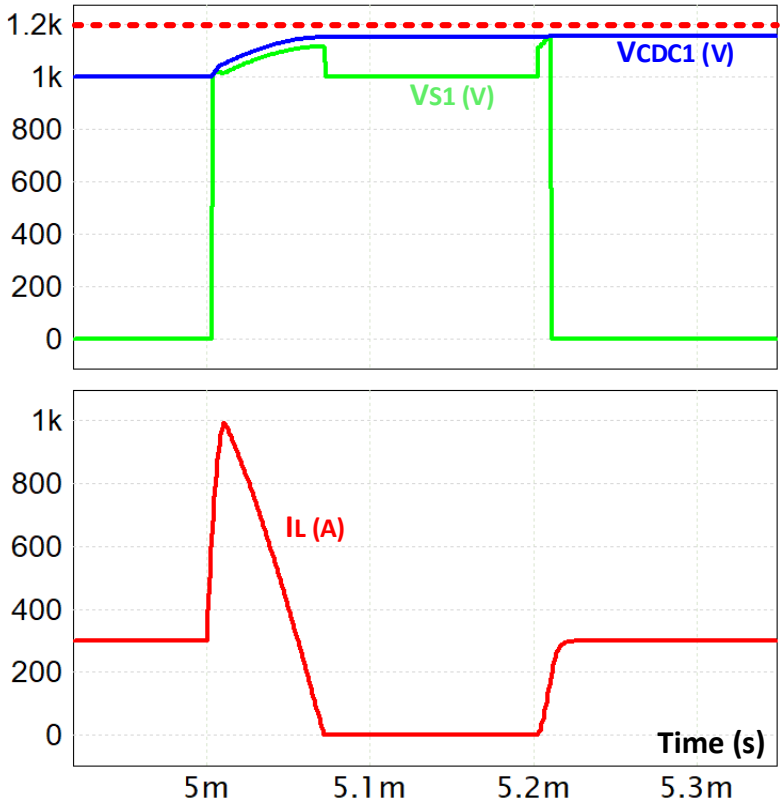


Figure 3. 10 Simulation case for capacitor design in the MLSSCB.

3.3.2 MOV Selection

Same as the conventional SSCB, the MLSSCB uses a MOV for energy absorption during its breaking process. The crucial parameters of the MOV, including clamping voltage and energy volume, need to be determined during the design of the breaker.

Since the voltage across the faulted transmission line during the operation of the MOV in the MLSSCB is reduced to the unit level of the source voltage, the required clamping voltage of the MOV can be lower than that required in its counterpart of conventional SSCB. For instance, in the operating scenario with parameters in TABLE 3-1, if the limit of the fault isolation time of the system is 200μs, the MOV clamping voltage in the applied conventional SSCB needs to be higher than 5150V from the Equation (3.6). On the other hand, for the MLSSCB, the minimum clamping voltage of the MOV can be determined from the Equations (3.5) and (3.7) and is equal to 1261V. By comparison, the needed clamping voltage of the MOV is reduced effective by using the proposed MLSSCB.

$$T_{iso\_conv} = I_0 \frac{L}{V_{clamp} - V_{DC}} \tag{3.6}$$

$$T_{iso\_MLSSCB} = (n-1)T_d + T_{MOV} \tag{3.7}$$

On the other hand, the energy volume also needs to be considered during the selection of the MOV. The inductive energy absorbed in the MLSSCB during the whole breaking time can be calculated by

$$W_R = \int_0^{t_{mov}} V_{clamp} \left(I_0 + \frac{1}{L}\frac{n-2}{n-1} V_{DC} T_d + \frac{1}{L}\frac{n-3}{n-1} V_{DC} T_d + \cdots + \frac{1}{L}\frac{1}{n-1} V_{DC} T_d - \frac{V_{clamp} - V_{CDC1}(0)}{L} t \right) dt = I_0 T_{MOV} + \frac{1}{L} V_{DC} \frac{n-2}{2} T_d T_{MOV} - \frac{EMF}{2L} {T_{MOV}}^2 \tag{3.8}$$

where $t = 0$ when the last switch of the breaker opens and the MOV starts to operate.

After t_{mov} in the Equation (3.5) is substituted into Equation (3.8) W_R can be expressed as

$$W_R = \frac{1}{2} L \frac{V_{clamp}}{V_{clamp} - \frac{V_{DC}}{n-1}} \left(I_0 + \frac{1}{L} V_{DC} T_d \frac{n-2}{2}\right)^2 \quad 3.9$$

From Equation (3.9), the value of W_R can be obtained by using several parameters of the breaker and the transmission line. In comparison with the required MOV energy volume in conventional breakers as depicted in Equation (3.10) [35], the requirement in the MLSSCB is lower in most cases because the value of $\frac{V_{DC}}{n-1}$ is significantly smaller than V_{DC} and the value of $\frac{1}{L} V_{DC} T_d \frac{n-2}{2}$ is usually negligible compared to I_0.

$$W_R = \frac{1}{2} L \frac{V_{clamp}}{V_{clamp} - V_{DC}} {I_0}^2 \quad 3.10$$

3.3.3 Power Semiconductor Devices Selection

Several power semiconductor devices including active switching devices and diodes are needed in the Diode Clamped SSCB as shown in Figure 3.2(b). Their selection is mainly based on some of their crucial parameters including voltage rating, current rating and conducting efficiency. From the voltage rating point of view, the switching devices S_1 to S_{n-2} should equally share the source voltage and their voltage ratings need to be higher than the DC bus voltage divided by the number of the switches in the breaker. On the other hand, the rated voltage of S_{n-1} should be set to be higher than the clamping voltage of the MOV; the voltage ratings of D_{1_1} to D_{n-1_n-1} are set according

to S_1 to S_{n-2}. In terms of current rating, the requirements for all the semiconductor devices are the same and their rated currents need to be higher than $I_0 + V_{DC}T_d(n - 2)/2L$. In regard to conducting efficiency, IGBTs, GaN HEMTs, SiC MOSFETs and SiC JFETs with low $R_{ds(on)}$ or $V_{ds(on)}$ are superior candidates as applied to solid-state circuit breakers at different voltage and power levels [41] [7] [42].

3.4 Bi-directional Configurations of the Multilevel Solid-State Circuit Breaker

For non-regenerative loads and PV plants interfaces, the uni-directional topologies of the MLSSCB as shown in Figure. 3.2(a) and Figure. 3.2(b) may be directly applied to their breakers. Nonetheless, for the applications with bidirectional currents, bidirectional breaker must be implemented. To make the proposed MLSSCB compatible for these applications, two types of bidirectional configurations are presented below.

3.4.1 Symmetric Bi-directional Multilevel Solid-State Circuit Breaker

By mirroring the topologies of the unidirectional MLSSCB in Figure. 3.2 horizontally, the symmetrical bidirectional configuration of the MLSSCB can be obtained as in Figure 3.11. The right half of the breaker is for interrupting the line-side faults and the left part is for the DC bus faults. The current limiter L_S is needed to limit the increment of the DC bus fault current. During the current breaking process of the bidirectional SSCB, the switches for the line-side fault and their symmetrical counterparts for DC-bus fault turn off sequentially from the middle to the two ends. The working principle of the breaker is the same as the unidirectional MLSSCB except that the

resonance between the line inductance and the voltage dividing capacitors need to be considered additionally in the analysis.

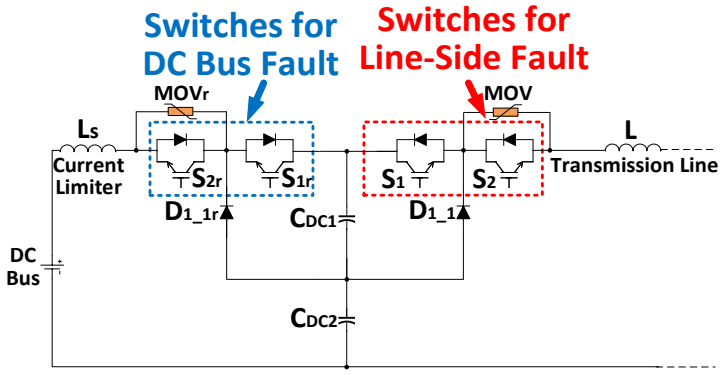


Figure 3. 11 Symmetrical bidirectional configuration of a 3-level MLSSCB.

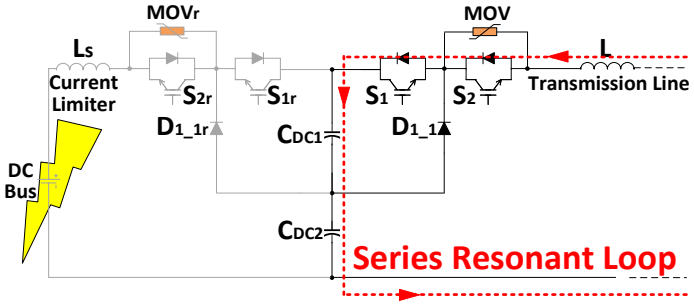


Figure 3. 12 Series resonant loop of the symmetrical bidirectional MLSSCB during a DC bus fault.

During the operation of the symmetrical bidirectional MLSSCB in a DC bus fault, after its main switches are turned off, the transmission line is isolated from the faulted DC bus and a series-resonant loop of the line inductor and voltage dividing capacitors is formed as highlighted in Figure 3.12. In this way, the resonant voltage ripple is applied to each of the capacitors and can be given by

$$\Delta V_{C_{DC_{Resonant}}}(t) = \sqrt{\frac{L}{C_{DC}(n-1)}} I_0 sin \sqrt{\frac{n-1}{LC_{DC}}}(t). \qquad 3.11$$

The amplitude of the ringing may be quantified as

$$Max\left(\Delta V_{C_{DC_{Resonant}}}(t)\right) = \sqrt{\frac{L}{C_{DC}(n-1)}}I_0. \quad 3.12$$

After taking into account the increment of the capacitor voltage during the switches delay time, the maximum value of the capacitor voltage's increment in a symmetrical bi-directional MLSSCB may be attained from

$$\Delta V_{CDCmax} = \frac{1}{C_{DC1}}\int_0^{T_{iso\_MLSSCB}} I_L\, dt + \sqrt{\frac{L}{C_{DC}(n-1)}}I_0. \quad 3.13$$

To ensure that switches do not incur overvoltage during the breaker's reclosing, the capacitors need to be large enough to suppress their peak voltage values under the rated voltage of the switches as

$$C_{DC1} > \left[\frac{2\int_0^{T_{iso\_MLSSCB}} I_L\, dt}{-I_0\sqrt{\frac{L}{n-1}}+\sqrt{I^2\frac{L}{n-1}+4\Delta V_{CDCmax}\int_0^{T_{iso\_MLSSCB}} I_L\, dt}}\right]^2. \quad 3.14$$

In Equation (3.3), the integral of I_L can be derived as

$$\int_0^{T_{iso_{MLSSCB}}} I_L\, dt =$$

$$\sum_{a=1}^{n-2}\frac{a}{n-1}I_0T_d + \frac{1}{n-1}I_0T_{MOV} + \left[\frac{1+2+\cdots(n-2)}{n-1}\ \ \frac{1+2+\cdots(n-3)}{n-1}\ \ \cdots\ \ \frac{1}{n-1}\right]\begin{bmatrix}\frac{n-2}{n-1}\\ \frac{n-3}{n-1}\\ \vdots \\ \frac{2}{n-1}\end{bmatrix}$$

$$\frac{1}{L}V_{DC}{T_d}^2 + \sum_{a=1}^{n-2}\left(\frac{a}{n-1}\right)^2\frac{1}{L}V_{DC}\frac{{T_d}^2}{2} - \frac{1}{5}\frac{1}{L}EMF\frac{{T_{MOV}}^2}{2} + \sum_{a=1}^{n-2}\frac{1}{5}\frac{a}{5}\frac{1}{L}V_{DC}T_dT_{MOV}. \quad 3.15$$

From the Equation (3.14), the capacitance increases with the system line inductance result from the enhancement of the capacitors' resonant voltage, which makes the symmetric bi-directional configuration more suitable for the medium voltage DC systems with smaller line inductances, such as electric shipboards.

3.4.2 Hybrid Bi-directional Multilevel Solid-State Circuit Breaker

To perform bidirectional protection in the applications with larger line inductances, a hybrid bidirectional configuration of the MLSSCB has been proposed as presented in Figure 3.13. In this figure, the configuration is composed of a MLSSCB to interrupt line side fault and a conventional SSCB to address DC bus fault. In the DC bus fault scenario, the operation of the breaker is the same as that in the conventional SSCB and the resonant effect on the capacitor voltage is averted. In this way, the hybrid bidirectional configuration may be applied to the medium voltage distribution systems with larger line inductances, such as offshore wind farms. Also, because half of the hybrid configuration uses the conventional topology, its efficiency may be lower than that of the symmetrical configuration but still higher than that of the conventional bidirectional SSCBs.

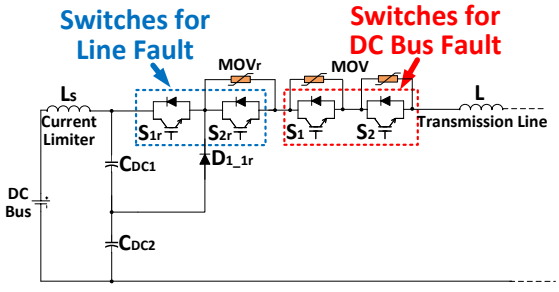


Figure 3. 13 Hybrid bidirectional configuration of a 3-level MLSSCB.

CHAPTER 4: CONCEPTS OF THE PROPOSED SURGELESS SOLID-STATE CIRCUIT BREAKERS

During the operations of the conventional Solid-State Circuit Breakers (SSCBs) in DC systems, surge voltages are induced across their semiconductor device due to the stray line inductors existing in the power cables and clamped by their surge arrestors, such as Metal Oxide Varistor (MOVs) [43] [44]. The clamping voltages of the surge arrestors are usually much higher than the source voltage to ensure the fast isolation speed of the SSCBs in that the current clearing time of the breakers varies inversely with the clamped surge voltage [38]. Besides, the present commercially available MOVs usually have clamping voltages much higher than their continuous rated voltage for averting the premature aging on the MOVs when they are ineffective [15] [16]. For these reasons, the semiconductor switches in the SSCBs have to sustain substantial amount of surge voltages, usually around 1.5 to 2.5 times of their system voltages and their voltage ratings always need to be overdesigned according to the surge voltage values, which increases the material costs and conduction losses of the breakers.

To address these problems, two types of new Surgeless Solid-State Circuit Breaker named Voltage Free Solid-State Circuit Breaker (SVFSSCB) and Ground Clamped Solid-State Circuit Breaker (GCSSCB) have been proposed in this dissertation. In the SVFSSCB, the DC source is actively grounded to minimize the surge voltage on the semiconductor devices during the energy absorbing phase. Besides, unlike the conventional SSCB, the SVFSSCB has separate energy absorbers of system and current-limiting inductors. Therefore, the breaker does not trade its isolation speed for the fault

current limiting capability. In the GCSSCB, the DC source voltage and surge amount of voltage are separated and distributed to two separate switching devices, namely main switch and auxiliary switch. In that case, the main switch in the breaker can be rated at the system voltage level and the auxiliary switch can be rated at a low voltage value to synthesize enough back EMF to demagnetize the line inductors. Besides, as the source is isolated from the fault right after the main switch turns off, the GCSSCB can isolate the fault from the protected sources in an ultrafast speed regardless of the clamped surge voltage value across the breaker.

4.1 Operating Principle of Surge Voltage Free Solid-State Circuit Breaker

The simplified schematic and the simulation waveforms of the proposed SVFSSCB are drawn in Figure 4.1 and Figure 4.2 respectively, the key parameters in the simulation are listed in TABLE 4-1, the subintervals of the breaker through its operating process are shown in Figure 4.3 and the experimental results of the breaker has been presented in Figure 4.4.

In Figure 4.1, the proposed SSCB is mainly composed of a main switch, S_2, conducting the line current and blocking the source voltage before and after the breaker's operation, a MOV demagnetizing the energy store in the system inductor, a ground clamping switch, S_1, bypassing the DC bus, and a current limiting inductor, L_S, along with its resistive energy absorber.

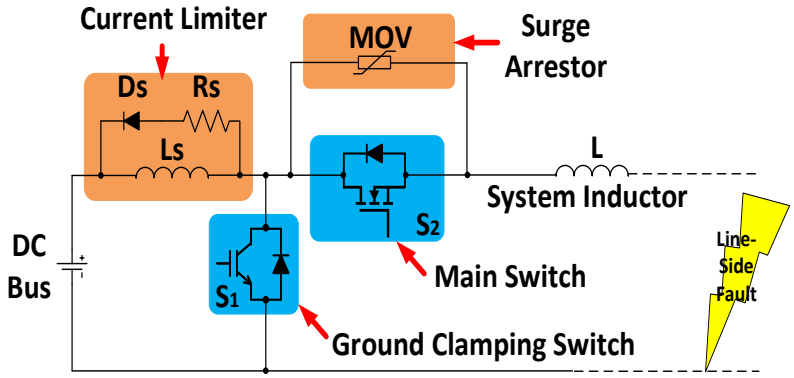


Figure 4. 1 The topology schematic of the proposed SVFSSCB.

During normal situations, the ground clamping switch, S_1, is turned off and the breaker switch, S_2, is on. The load current flows thorough S_2 and current limiter, L_s, as shown in Figure.4.3(a). When a fault occurs, the line current increases with its rising rate limited by L_s as shown in Figure 4.2 at t_0. Once the fault is diagnosed by the relay, S_1 turns on and S_2 off and the line current is transferred to a ground clamping loop as shown in Figure 4.3(b). Instantaneously, the increment of the fault current is interrupted as the line current waveform in Figure 4.2 at t_1. At the same time, the voltage across S_2 increases dramatically resulting from the stray line inductor and gets clamped by the MOV of the breaker. Thus, a reverse EMF that equals to the clamped voltage can be synthesized across the line inductor, L, and enforce the current to decrease as manifested in the line current waveform in Figure 4.2 from t_1 to t_2. After the line-side fault current is extinguished at t_3, S_1 opens and clears the source current immediately as the source current waveform displayed in Figure 4.2 at t_2. Eventually, the diode, D_s, conducts and the energy absorbing resistor, R_s, dissipates the energy stored in the current limiter, L_s, as shown in Figure 4.3(c).

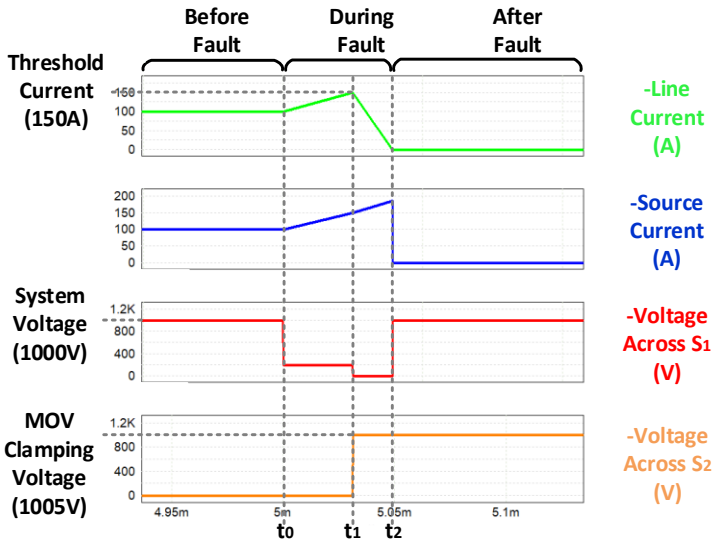
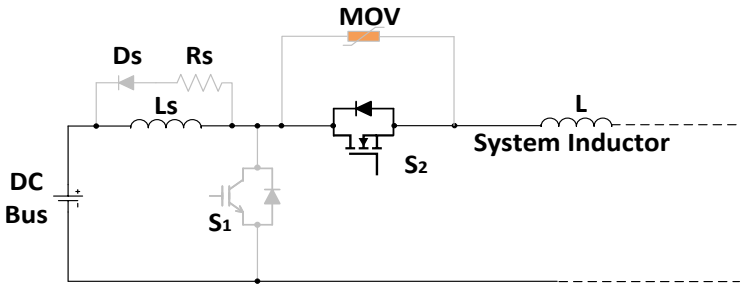


Figure 4. 2 The simulation waveforms of the proposed SVFSSCB.

TABLE 4 - 1: Key Parameters in the Simulation Case

Parameters	Values
DC bus voltage V_{DC}	1000V
Line current I_L	100A
Line inductor L	120μH
Current limiting inductor L_s	0.5mH
Clamping voltage V_{clamp}	1005V
Threshold current I_0	$1.5 \cdot I_L$



(a)

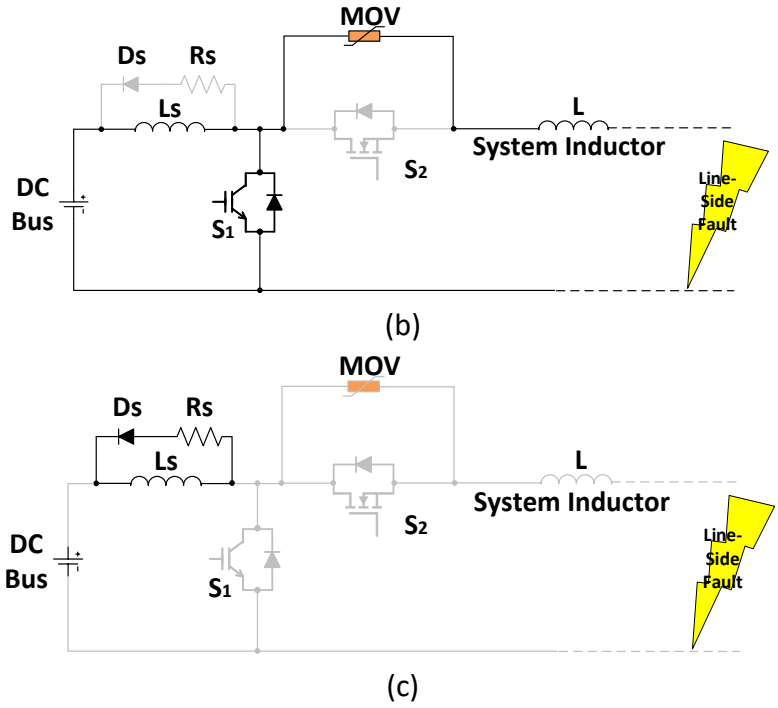
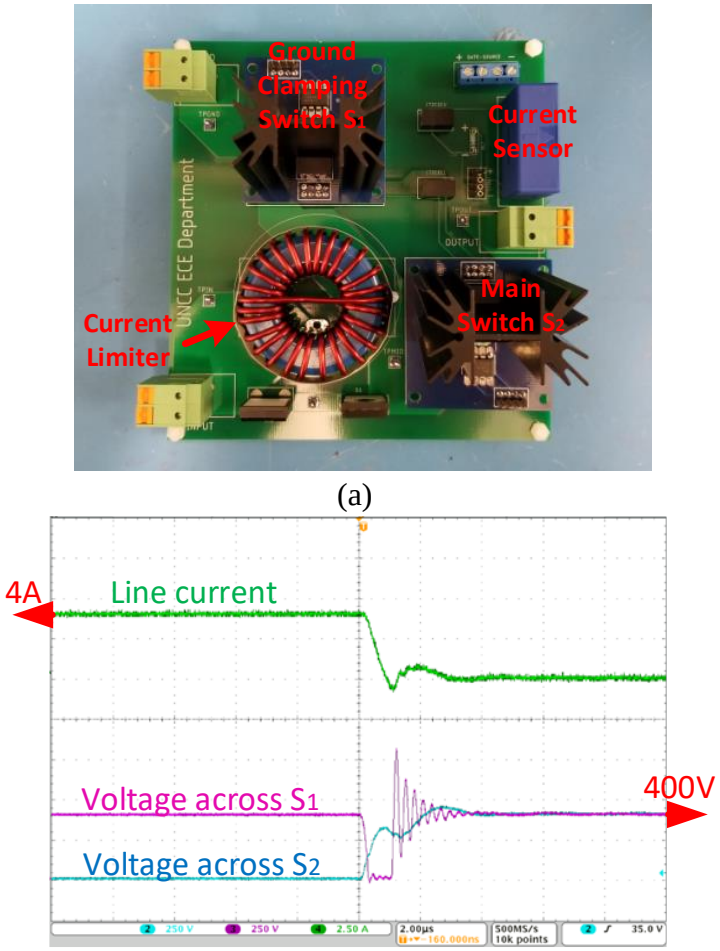


Figure 4. 3 The subintervals of the SVFSSCB during a line-side fault.

In the experiment, the proposed SVFSSCB is applied to a laboratory-scale short-circuit testing system with 400V DC source, 22μH line inductor and 1600W pure resistive load. The experimental waveforms of line current and switches voltages during breaking process are shown in Figure 4.4. From the waveforms, the prototyped breaker can interrupt and clear the line current successfully without inducing surge voltage on its switch on its normal current conducting loop, namely S_2 here. Thus, the working principles and surgeless capability of the breaker are validated in the experiment.

From the above analysis, during the whole operating process of the proposed breaker, there is no surge voltage imposed on the semiconductor switches. As in the switches' voltage waveforms in Figure 4.2, the highest voltage across the switches is 1005V. Thus, the switches can be selected based on their system voltage level. In the simulation case

here, for example, having a system voltage of 1000V, switches rated at 1200V can be selected to construct the SVFSSCB. On the other hand, since the energy absorbing process of the current limiter in the breaker is separate from that of the system inductor, the current limiter has negligible effect on the isolation speed of the breaker.



(a)

(b)

Figure 4. 4 Experiments of the SVFSSCB during current breaking process. (a) Experimental setup. (b) Experimental results.

4.2 Design Considerations of the Surge Voltage Free Solid-State Circuit Breaker

4.2.1 Current Limiter Selection

During the operation of the SVFSSCB, after the Switch, S_1 turns off and S_2 turns on, the DC bus voltage is directly imposed on the current limiting inductor as indicated in Figure 4.3(b). After that, the current through the inductor keeps increasing until the line current is extinguished by the MOV. For this reason, the minimum inductance of the current limiter needs to be specified to ensure the inductor current changes in a safe range.

The increment of the current through the current limiting inductor during the breaker's operation can be expressed as in the Expression (4.1) and its value need to be smaller than the difference between the saturation current of the inductor and the threshold current of the breaker.

$$i_{Ls} = \frac{1}{L_s} V_{DC}(T_{Break\_SVFSSCB} + T_{det}) < I_{Lsat} - I_0 \tag{4.1}$$

where T_{det} is the time period of the breaker to detect the zero current and send the trip signal to S_1, I_{Lsat} is the saturation current of the applied current limiting inductor.

From Expression (4.1), the minimum current limiting inductance of the SVFSSCB can be determined as

$$L_s > \frac{V_{DC}(T_{Break\_SVFSSCB} + T_{det})}{I_{Lsat} - I_0} \tag{4.2}$$

4.2.2. Semiconductor Switches Selection

As shown in Figure 4.1, there are two semiconductor switches in the SVFSSCB, namely the main switch and the ground clamping switch. Because of the different functions and installed positions of the switches, different semiconductor technologies can be applied to the switches to improve the efficiencies and cost effectiveness of the SVFSSCB.

For the main switch, as it is on the conduction loop of the breaker, semiconductor devices exhibiting low R_{dson} or V_{dson}, such as SiC MOSFETs, SiC JFETs and GaN HEMTs, should be used in priority to optimizing the efficiency of the breaker [39] [42] [45]. Besides, the voltage rating of the main switch may be set according to the system voltage as there is no surge voltage appears on the switch. In addition, the current rating of the switch need to be higher than the threshold current of the breaker. On the other hand, for the ground clamping switch, since it does not conduct current in the normal situations, the efficiency profile of the semiconductor device is not the main concern during its selection. In this way, the semiconductor devices with lower costs, such as Si IGBTs and Si MOSFETs, can be chosen for the switch. Other than that, the voltage rating of the ground clamping switch need to be 1.5 times of the system voltage to sustain the transient voltage caused by the mismatch of the switching dynamics of the switch and the MOV and the current rating of the switch need to be higher than the saturation current of the current limiting inductor. It is worthy to mention that notwithstanding the voltage rating of the ground clamping switch is overdesigned, the efficiency of the breaker is not affected in that the switch is not on the conduction path of the breaker.

4.3 Comparison between the Surge Voltage Free Solid-State Circuit Breaker and the Conventional Solid-State Circuit Breaker.

4.3.1 Isolation Time

The isolation time of SSCBs is usually defined as the time interval between the instant when the switches in the breakers receive the trip signals and the time when the line current is decreased to the leakage current level [46]. During the design of the breakers, the isolation time needs to be as short as possible to minimize the effect of the faults. In the conventional SSCBs, if the clamping transience of their MOVs is neglected, their isolation time may be expressed as in (4.3) [38].

$$T_{iso\_SSCB} = T_{switch} + \frac{I_0(L + L_S)}{V_{clamp} - V_{DC}} \tag{4.3}$$

where T_{switch} is the turn-off time of the semiconductor device, I_0 is the threshold current, L is the system inductance, L_S is the current limiter inductance, V_{clamp} is the clamping voltage of the surge arrestor and V_{DC} is the DC bus voltage. V_{clamp} is assumed to be constant and equals its rated maximum rated value when the MOV is active. After the V-I characteristic of the MOV is considered, the V_{clamp} attenuates with the line current and the isolation time of the conventional SSCB may become even longer.

From (4.3), the isolation time increases with the inductance of the inserted current limiter and decreases with the clamped surge voltage of the MOV. Thus, to maintain a fast circuit breaking speed and employ the current limiter, the conventional SSCBs are required to sustain a large surge voltage during their breaking process.

On the other hand, in the proposed SVFSSCB, since the power source to the faulted line has been grounded and isolated from the faults before the operation of the MOV, the back EMF synthesized in the breaker is not offset by the source voltage and is equal to the MOV's clamping voltage. Therefore, the isolation time of the SVFSSCB can be expressed as

$$T_{iso\_SVFSSCB} = T_{switch} + \frac{I_0 L}{V_{clamp}} \tag{4.4}$$

From the comparison between Expression (4.3) and Expression (4.4), if the proposed SVFSSCB has a clamping voltage equaling the source voltage, its isolation time can be as short as that of the conventional SSCBs with a clamping voltage twice as high as the source voltage. Besides, the clamping voltage in the conventional SSCBs is usually set at 1.5 times of the system voltage. Thus, the SVFSSCB can attain a shorter isolation time than the conventional SSCBs and have no surge voltage induced on its semiconductor switches.

The short isolation time and surge-voltage-free feature of the SVFSSCB has been proven in the simulation results shown in Figure 4.5. In the simulations, both breakers are applied to the same 1000V 100kW DC distribution system and with the same inductive current limiter. From the current waveforms, the isolation time of the SVFSSCB is notably faster than that of the conventional SSCB. Besides, from the voltage waveforms, there is no surge voltage introduced across the switch on the conduction path of the SVFSSCB, namely S_2 in Figure 4.1.

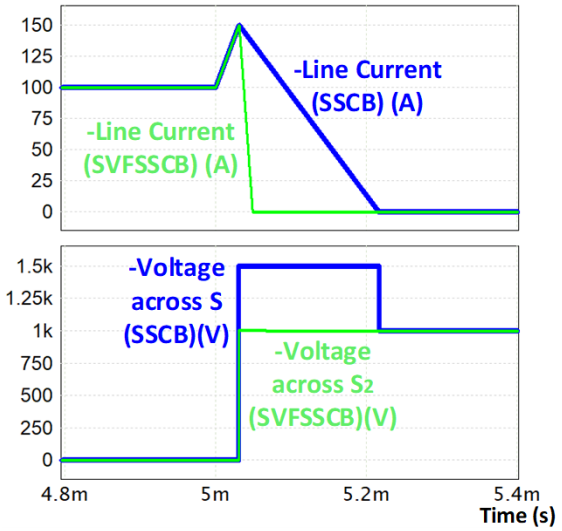


Figure 4. 5 Comparison between a SVFSSCB and a conventional SSCB.

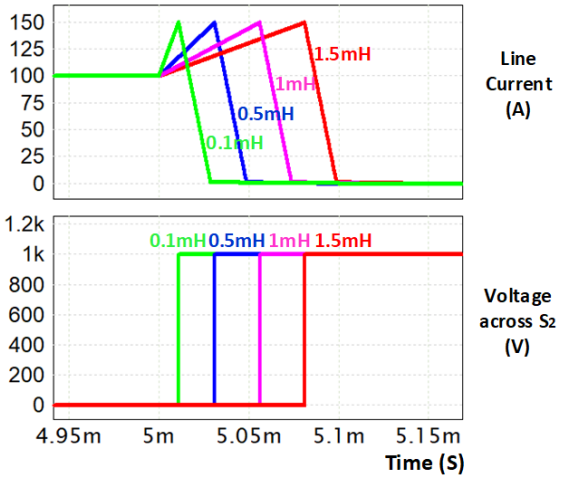


Figure 4. 6 Switch voltage and line current of the SVFSSCBs having different current limiting inductors (0.1mH, 0.5mH, 1mH and 1.5mH).

Furthermore, since the current limiter in the proposed breaker has an individual energy absorber, the isolation time as shown in Expression (4.4) is not affected by the inductance of the current limiter. As illustrated in the simulation results of Figure 4.6, the increasing inductance values of the current limiters in the SVFSSCBs neither retards their fast fault clearing speed nor introduces surge voltages on their switches.

4.3.2 Efficiency

Caused by the higher conduction losses of the semiconductor switches compared to the metal contactors, the efficiency of the SSCBs is lower than that of the electromechanical circuit breakers and is the main factor that hinders the adoption of the SSCBs in the main power protection markets. Moreover, with the surge voltage induced across the SSCBs during their current breaking process, the voltage ratings of their semiconductor switches have to be overdesigned. In the power semiconductor switches, to receive higher voltage block capability, thicker and lower doped drift regions are needed and larger on-state resistance is incurred [8] [47]. As a result, the overdesign of the switches' voltage ratings can exacerbate the efficiency problem in the SSCBs.

On the contrary, without surge voltage on the semiconductor device on its conduction path, the proposed SVFSSCB can get an improved efficiency by using lower voltage rated devices. The comparison between the SVFSSCB and the conventional SSCB are made in a 1000V system here to manifest the advantage of the SVFSSCB on efficiency.

Two commercial SiC MOSFET switches from the product series of the same manufacturer are applied to the two breakers respectively for the comparison. In the SVFSSCB, the switch, CM0025120D, rated at 1200V can be used because the breaker does not induce surge voltage during the operation. In the conventional SSCB, however, the switch, C2M0045170D, rated at 1700V, is needed to sustain the surge voltage of 1500V during the breaker's operation. The on-state resistances of both switches versus

drain current are drawn in Figure 4.7 as regards the datasheet provided by the manufacturer.

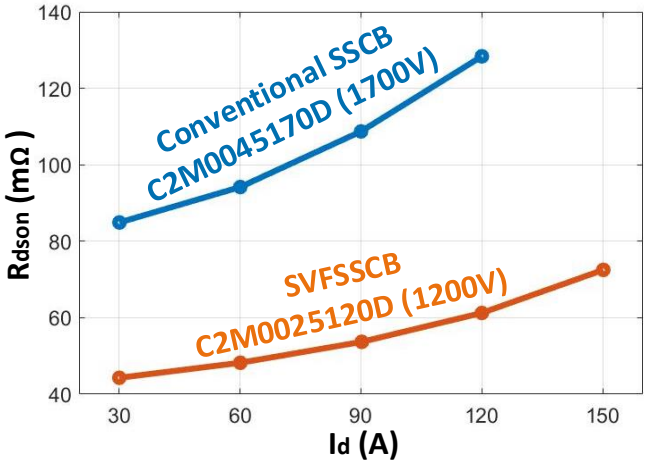


Figure 4. 7 Comparison between the R_{dson} of the SiC MOSFETs applied to the circuit breakers. (Vgs=20V,T_j=150℃)

From the figure, the semiconductor switch in the SVFSSCB has lower on-state resistances than that of the conventional SSCB along with a larger current upper limit.

The ground clamping switch in the SVFSSCB is installed across the DC source and its leakage current during the off-state causes extra conduction losses in the breaker under the normal conditions. However, as the switch only conducts current in the transience of the breaker's operation, its junction temperature can be easily maintained around the room temperature, which makes its loss negligible in regard to the conduction loss of the main switch. Herein, the leakage current is set at 100μA that can be easily attained by using off-the-shelf Si switches at a junction temperature of 25℃.

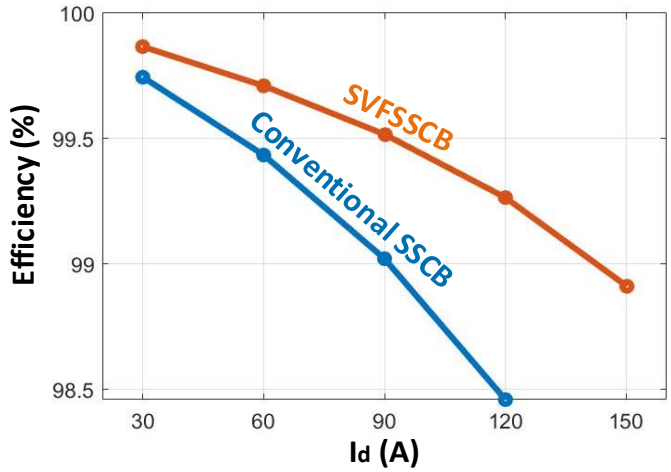


Figure 4. 8 Comparison between the efficiencies of the SVFSSCB and conventional SSCB. ($V_{gs} = 20V, T_j = 150℃, V_{DC} = 1000V$).

From the above analyses, the results of the comparison between the power efficiencies in the SVFSSCB and that in the conventional SSCB can be achieved as summarized in Figure 4.8. The conduction losses of the current limiting inductors are not included in that they are the same for the two breakers compared here. From Figure 4.8, the efficiencies of the SVFSSCB are notably higher than those of the conventional SSCB in the whole current range and the advantage is expected to be more prominent with the increment of the operating current.

4.4 Operating Principle of Ground Clamped Solid-State Circuit Breaker (GCSSCB)

The simplified schematic of the proposed GCSSCB is shown in Figure 4.9. In the figure, the GCSSCB mainly consists of a main switch to sustain the source voltage after the braker opens, an auxiliary switch to sustain surge amount of voltage during the breaker's operation, a ground clamping diode to bypass the DC bus and a MOV to limit the surge voltage. It's worth to mention that, as the auxiliary switch does not withstand

significant voltage after the breaker opens, both the auxiliary switch and the MOV can be rated at low voltages. During a normal scenarios, both switches in the GCSSCB, S_1 and S_2, are turned on to conduct the line current as shown in Figure 4.10(a). In the line-side fault scenario, once the fault current comes to be higher than the threshold current of the protection system, the Switch S_1 will be tripped to transfer the current to the loop following through the Ground clamping diode as indicated in Figure 4.10(b). Instantaneously, the DC bus is isolated from the fault and thereby the source output current drops to zero as shown in Figure 4.11 at t_1. After that, the system inductor is grounded, which makes the line current stops increasing and gets limited to a range around the threshold current as shown in the line current waveform from t_1 to t_2 in Figure 4.11. After a short period of delay time, the Switch S_2 is opened and then the fault current is commuted to the MOV as in Figure 4.10(c) and ultimately cleared as the line current waveform from t_2 to t_3 in Figure 4.11. On the other hand, from the voltage waveforms of the switches, the DC source voltage and back EMF are sustained by two separate switches without any voltage unbalancing issues as the voltage waveforms in Figure 4.11.

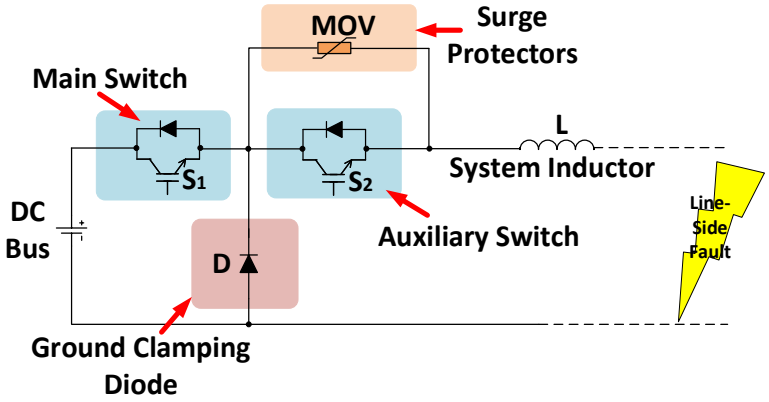


Figure 4. 9 The simplified schematic of the proposed GCSSCB.

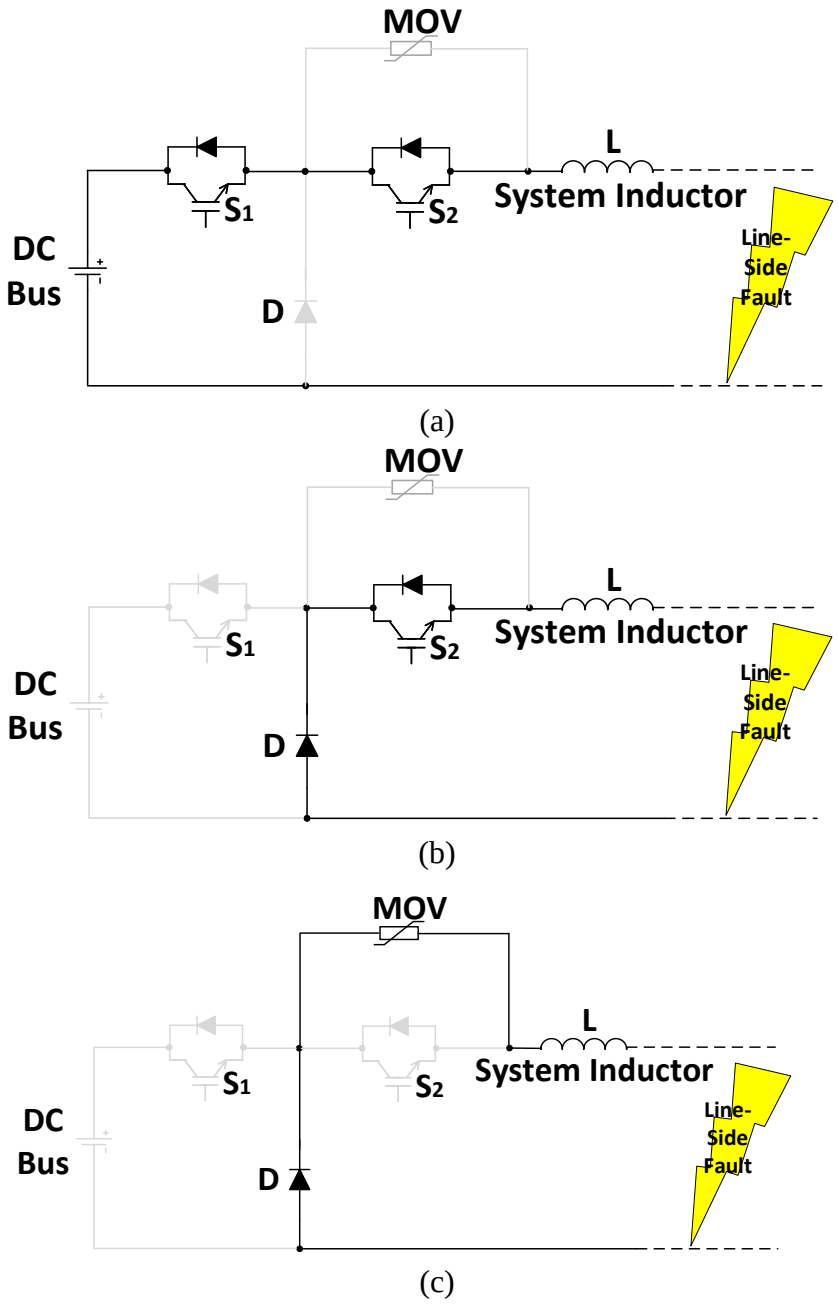


Figure 4. 10 Subintervals of the GCSSCB during the line side fault.

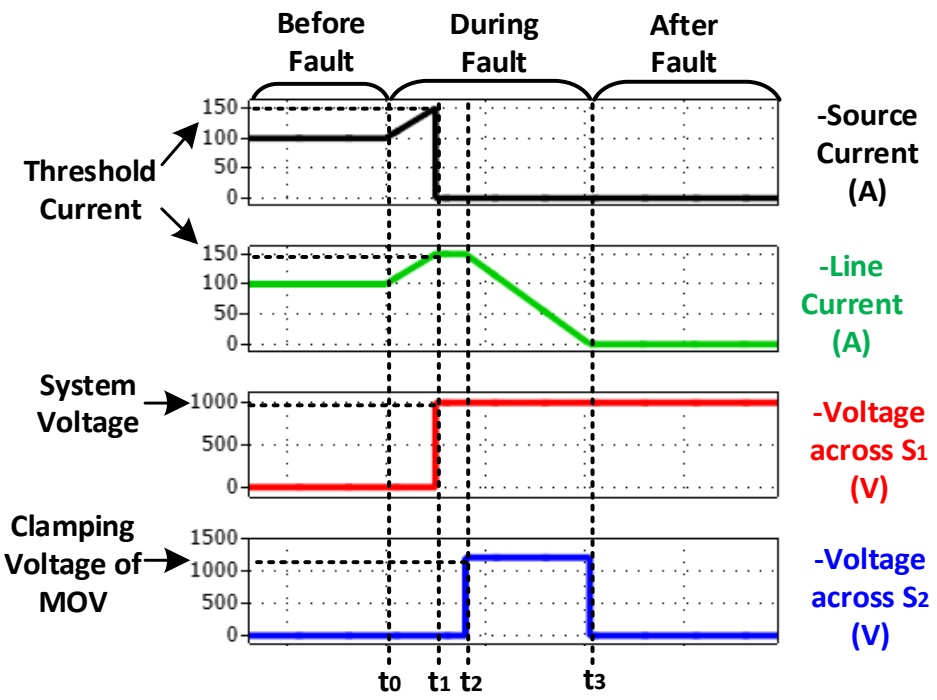
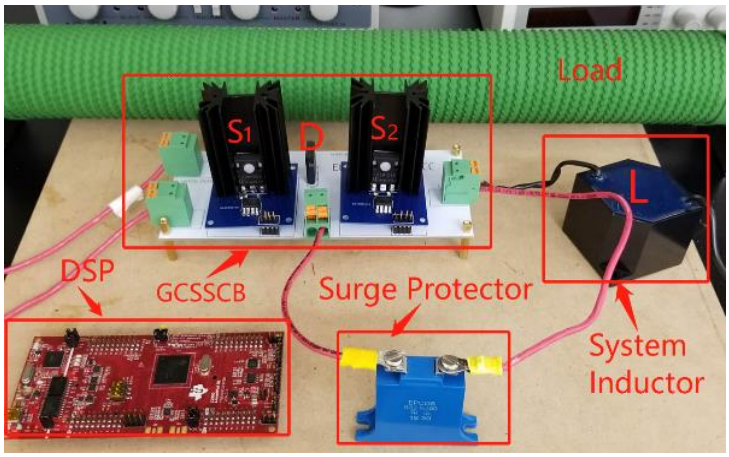
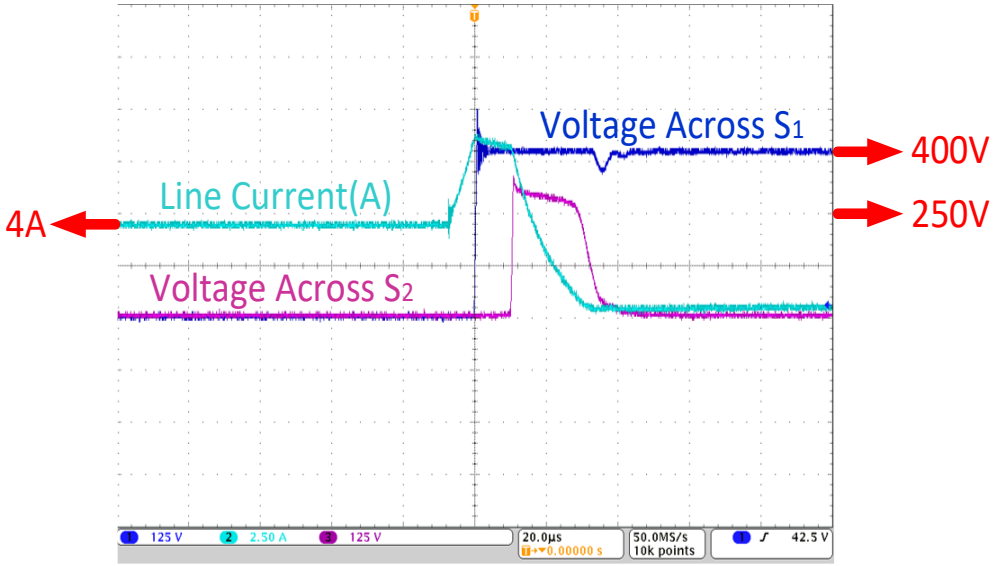


Figure 4. 11 Simulation results of the GCSSCB during the line side fault.

Experimental results of the GCSSCB have also been achieved as shown in Figure 4.12. In the experiment, the breaker is applied to a testing system with a 400V DC source and a 1.6kW pure resistive load. The transmission line between the source and the load is modeled by a 0.5mH inductor. The fault in the experiment is executed by shorting the load with a ground connected mechanic circuit breaker. The experiment waveforms of the line current and switches voltages are shown in Figure 4.12. From the waveforms, the prototyped GCSSCB can interrupt the fault current successfully and distribute DC source voltage and back EMF voltage to two different switching devices. The experimental results match with the simulation results in Figure 4.11. Therefore, the technical feasibility of the breaker get further validated.



(a)



(b)

Figure 4. 12 Experiments of the GCSSCB during a current interruption process. (a) Experimental setup, (b) Experimental results.

4.5 Design Considerations of the Ground Clamped Solid-State Circuit Breaker

4.5.1 Source resonant capacitor design

Depending on the structure of the applied DC system, there might be a significant inductor existing between a DC bus and a GCSSCB as the source inductor, L_s, in Figure

4.13. Since there is no surge protector for the front switch S_1 in the GCSSCB, the source inductor can cause overvoltage damages on the switch while it is turned off. To avert this problem, GCSSCBs need to be installed either close enough to their sources or with source resonant capacitors on its source side as shown in Figure 4.13. The source resonant capacitor provides conduction path for the source inductor current after S_1 opens and relieve the risk of surge voltage on the switch. However, as the resonance between the source inductor and the capacitor, an oscillation is added to the switch voltage as shown in Figure 4.14. To ensure the oscillation does not exceed the voltage rating of the switch, the source capacitor of the breaker needs to be designed properly.

After S_1 opens, the source isolates from its load and constructs a series-resonant circuit with the source inductor and resonant capacitor. In this way, the expression of the capacitor voltage can be achieved as

$$V_{C1}(t) = V_{DC} + \sqrt{\frac{L_s}{C_s}} I_0 sin \frac{1}{\sqrt{L_s C_s}}(t) \qquad 4.5$$

where V_{DC} is the DC bus voltage, L_s is the inductance of the source inductor, C_s is the capacitance of the resonant capacitor and I_0 is the threshold current.

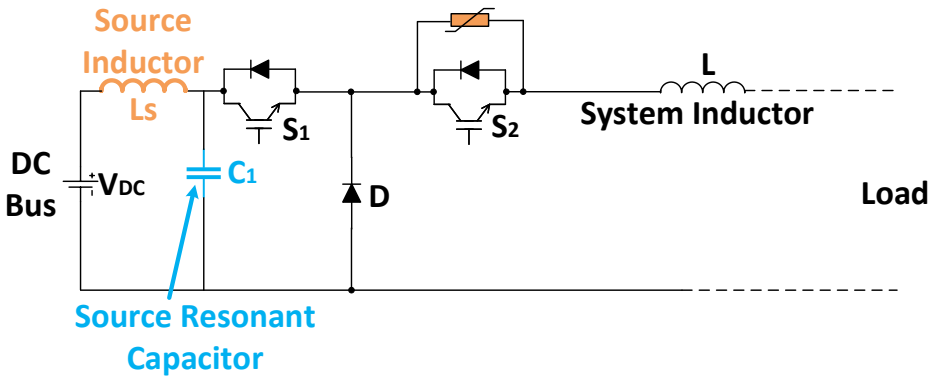


Figure 4. 13 Source inductor and source resonant capacitor in GCSSCB.

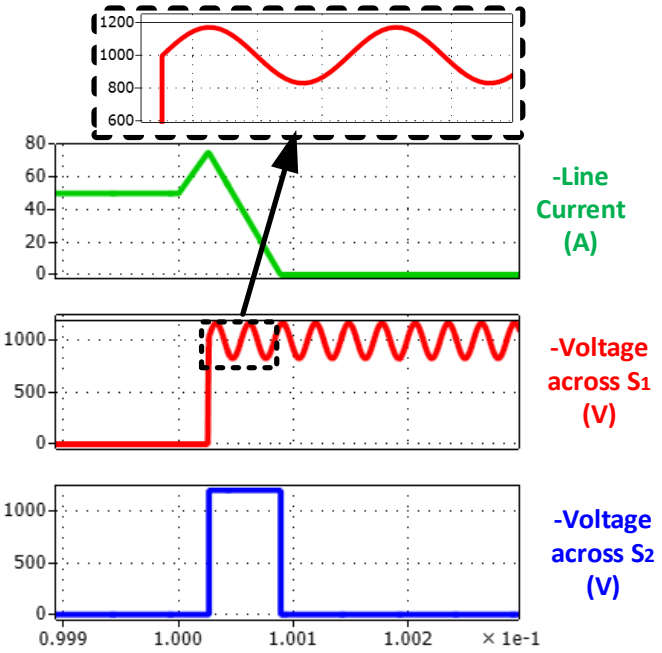


Figure 4. 14 Oscillation on the switch voltage in a GCSSCB.

As the voltage of S_1 equals to $V_{C1}(t)$ after the switch opens, the maximum value of $V_{C1}(t)$ is required to be lower than the voltage rating of the switch as

$$\max\left(V_{C1}(t)\right) = V_{DC} + \sqrt{\frac{L_s}{C_s}} I_0 < V_{s*} \qquad 4.6$$

where V_{s*} is the rated voltage of the Switch, S_1.

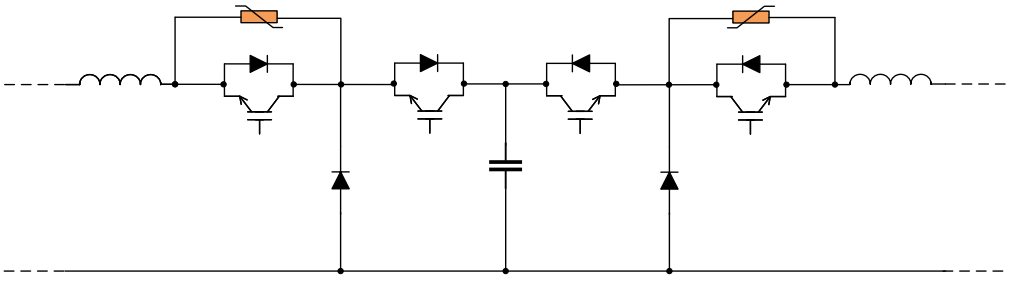


Figure 4. 15 Bidirectional configuration of the GCSSCB.

From Expression (4.6), the range of the source resonant capacitance with a 50% margin has been determined as Expression (4.7). The plausibility of the design has been validated by a simulation result in PLECS as shown in Figure 4.14, where the ripple of the switch voltage is suppressed to be lower than its rated voltage by the resonant capacitor.

$$C_s > 1.5\left(\frac{I_0}{V_{s*} - V_{DC}}\right)^2 L_s \tag{4.7}$$

Additionally, with a proper design of the resonant capacitor regards to the two ends of the breaker, the GCSSCB can be extended to a bi-directional configuration as shown in Figure 4.15 and introduced into the applications having regenerative loads.

4.5.2 The integration of the Ground Clamped Solid-State Circuit Breaker with buck converter.

The GCSSCB can be integrated with the load DC/DC converter to reduce its conduction loss and financial cost. In the DC distribution systems, the DC bus is usually with higher voltage rating than its loads and connected to the loads through buck converters [48]. In the structure of the GCSSCB as Figure 4.5, the front switch S_1 and clamping diode D can construct a buck converter and their switching operation does not interrupt the flow of the line current even during the dead time between the switches. Hence, the GCSSCB can be integrated with the DC load DC/DC converters as show in Figure 4.16. As in the figure, the integrated GCSSCB can keep its circuit breaking switch on to perform as a buck converter in the normal situation and can work as a circuit break by open the switches sequentially as a GCSSCB when a fault happens. In comparison with

the independent GCSSCB, the converter integrated GCSSCB uses one less switching device and can achieve both higher efficiency and lower costs.

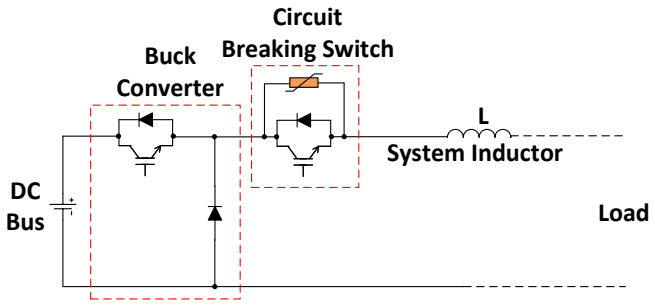


Figure 4. 16 Buck converter integrated GCSSCB.

4.6 Comparison between the Ground Clamped Solid-State Circuit Breaker and the Conventional Solid-State Circuit Breaker.

4.6.1 Isolation Time

In the conventional SSCB, after its switches open, its source still has connection to the fault until the fault current is extinguished by the MOVs, which aggravates the DC bus voltage dropping during the fault and increases the risk of system failure [22].

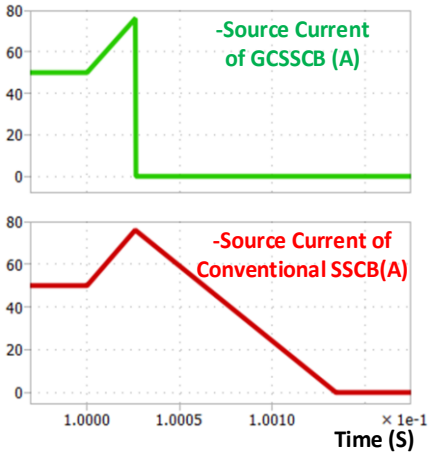


Figure 4. 17 Simulation waveforms of source current in a conventional SSCB and a GCSSCB.

In the GCSSCB, when the first operating switch opens, the source isolates from the fault immediately and does not experience the main fault path. This attribute of the GCSSCB is validated in a simulation case as Figure 4.17. From the waveforms, the average current drawn from the source during the fault is apparently lower in the GCSSCB than the conventional SSCB. In this way, the voltage dropping of DC bus under the protection of the GCSSCB can be limited, which represents an advantage of the GCSSCB over the conventional SSCB in isolation speed.

4.6.2 Surge Protector.

In the conventional breakers, the energy required to be absorbed during its breaking process can be expressed as Expression (4.8) [35].

$$W_{SSCB} = \frac{1}{2} \cdot L_{DC} \cdot \frac{V_{clamp}}{V_{clamp} - V_{DC}} \cdot {I_0}^2 \quad 4.8$$

In the GCSSCB, since its system inductor is grounded during its energy absorbing process, the absorbed energy is equivalent to the energy stored in the system inductor as Expression (4.9).

$$W_{GCSSCB} = \frac{1}{2} \cdot L_{DC} \cdot {I_0}^2 \quad 4.9$$

In comparison with Expressions (4.8) and (4.9), since the value of $\frac{\mathrm{V_{clamp}}}{\mathrm{V_{clamp} - V_{DC}}}$ is usually much larger than 1, the requirement of MOV energy volume in a GCSSCB is lower than that in its counterpart conventional SSCB. This difference is especially apparent in the applied systems with high line inductance and power rating as shown in

Figure 4.18. In this way, the size, cost and life span of the surge protectors can be reduced by the application of GCSSCBs.

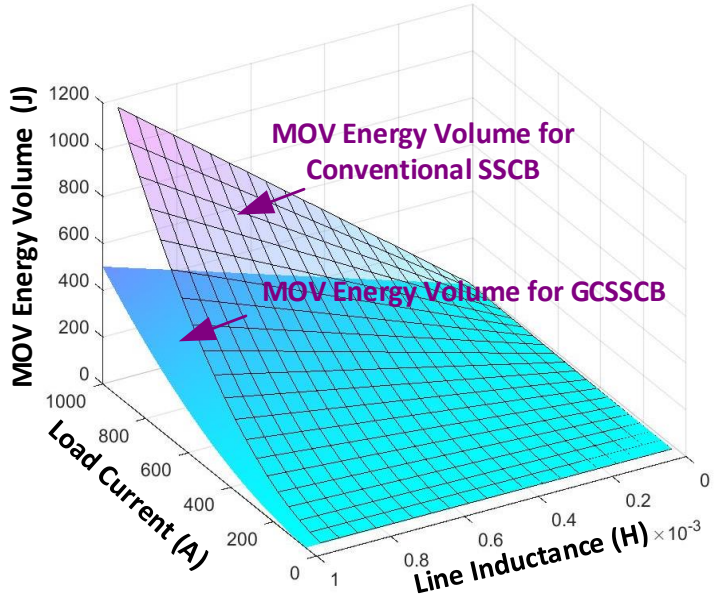


Figure 4. 18 The comparison between the minimum MOV energy volume of a conventional SSCB and a GCSSCB.

CHAPTER 5: CONCEPT OF THE PROPOSED SURGELESS MULTILEVEL SOLID-STATE CIRCUIT BREAKER

In the conventional medium voltage Solid-State Circuit Breakers (SSCBs) as shown in Figure 5.1, series-connected semiconductor switches are used with Metal Oxide Varistors (MOVs) in parallel with each of them to extend the voltage ratings of the breakers without incurring the dynamic voltage unbalance. The clamping voltages of the MOVs are expected to be much higher than the system voltage shared by the switches to ensure the fast fault isolation speed of the breakers [49]. In that case, large surge voltage is imposed on every switch of the conventional medium voltage SSCBs as shown in the operating waveforms in Figure 5.2 [17]. Accordingly, the voltage ratings of the switches cannot be selected based on their shared system voltages like that in other power electronic applications, but always have to be overdesigned according to their surge voltage values. As the same type of power semiconductor switches with higher breakdown voltages has higher drain-source on-state resistances caused by their thicker and lower doped drift regions, the large surge voltages imposed on the conventional SSCBs seriously impair the efficiencies of the breakers. To overcome this dilemma, a Surgeless Diode-Clamped Multilevel Solid-State Circuit Breaker (SMLSSCB) has been proposed integrating the GCSSCB with MLSSCB [50]. During the operations of the SMLSSCB, the series-connected switches are tripped sequentially to open and get their voltage clamped by the voltage dividing capacitors during their switching transience. In that case, the dynamic voltage unbalancing issues of the switches can be averted. Besides, since the main switches in the breaker does not interrupt the line current, the switches do

not incur surge voltage when they turn off. At the same time, as the isolation speed of the SMLSSCB is not related to the clamped surge voltage value of the MOV in the breaker, the MOV as well as its parallel-connected auxiliary switch can be rated at a low voltage rating. With these traits, the proposed SMLSSCB can use the semiconductor switches rated at meaningfully lower voltage ratings compared to the conventional SSCBs in the same scenarios and also get a shorter isolation period. Consequently, the MLSSCB can effectively improve the conduction efficiencies and isolation speed of the solid-state protection in the medium voltage DC distributions and promote their adoptions in more industrial applications.

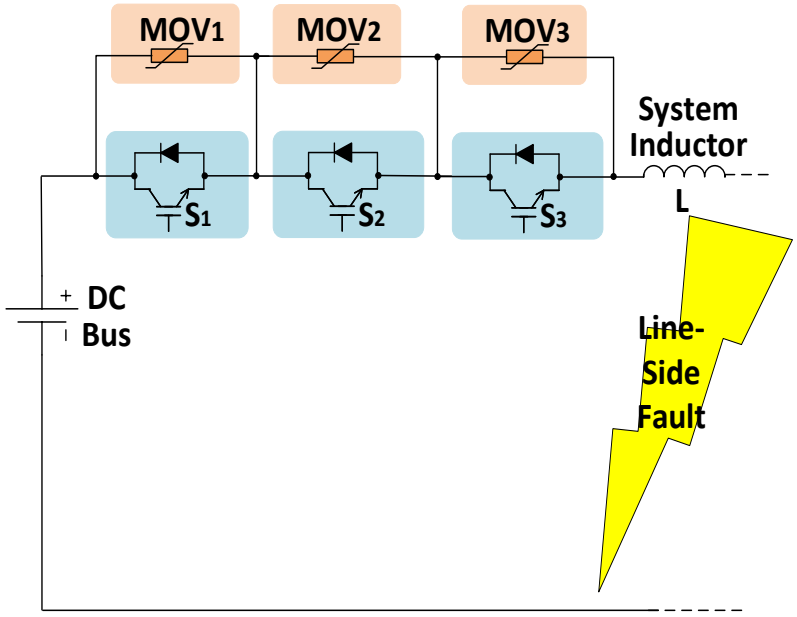


Figure 5. 1 Topology of the conventional medium voltage SSCB using series-connected switches.

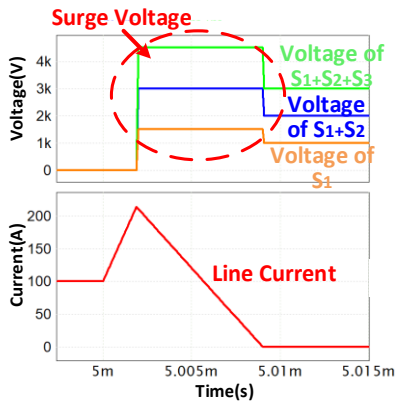


Figure 5. 2 Simulation results of the conventional medium voltage SSCB.

5.1 Operating Principles of the Surgeless Multilevel Solid-State Circuit Breaker

The simplified schematic of the proposed Surgeless Diode-Clamped Multilevel Solid-State Circuit Breaker (SMLSSCB) with three levels and its general structure with n levels are drawn in Figure 5.3 and Figure 5.4 respectively. The levels of the breaker here are determined by the number of the voltage levels across the faulted transmission line during its breaking process. In the figures, the SMLSSCB mainly consists of series-connected switches, voltage clamping diodes, resistive snubbers, voltage dividing capacitors and a MOV. The switches are divided into two categories, namely multiple main switches and one auxiliary switch as marked in Figure 5.3 and Figure 5.4.

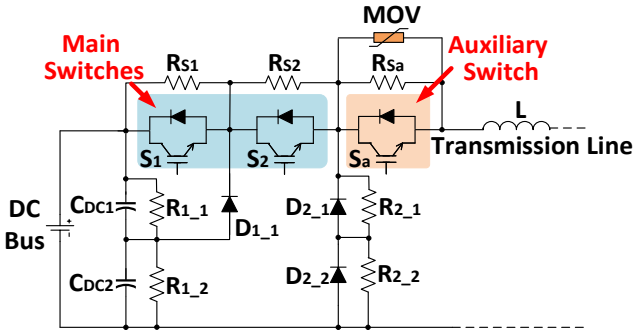


Figure 5. 3 Simplified schematic of the proposed SMLSSCB (3 levels).

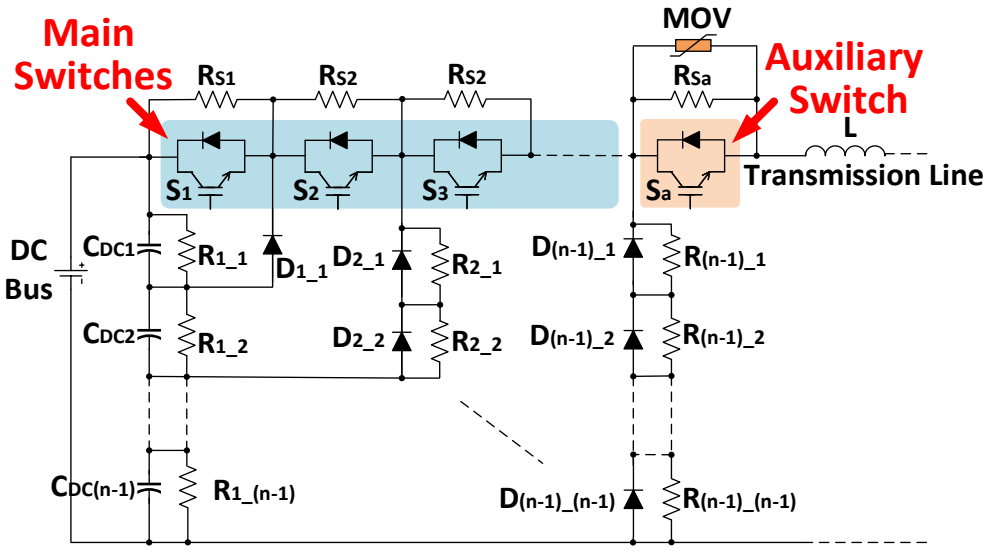


Figure 5. 4 General structure of the proposed SMLSSCB (n levels).

The main switches here are designed to isolate fault currents and block DC bus voltage; the auxiliary switch is to commutate current to the MOV and does not sustain significant voltages in a steady state. The capacitors, C_{DC1} to $C_{DC(n-1)}$, have the same capacitance and work as voltage dividers. The snubber resistors, R_{S1} to $R_{S(n-1)}$ and R_{2_1} to $R_{(n-1)\_(n-1)}$ are installed to keep the static voltage balance of the main switches after the breaker opens and the voltage balance of the clamping diodes after the breaker closes respectively. R_{1_1} to $R_{1\_(n-1)}$ are for resetting the capacitors voltages after the operations of the breaker. Beyond that, the snubber resistor for the auxiliary switch, R_{Sa}, is much smaller than the snubber resistors for the main switches to ensure a low voltage across the auxiliary switch and the MOV in a steady state. The operating principle of the SMLSSCB is presented below.

As the operating principles of the SMLSSCB in different levels are similar, here the 3-level SMLSSCB is mainly focused on and the analytical processes may be

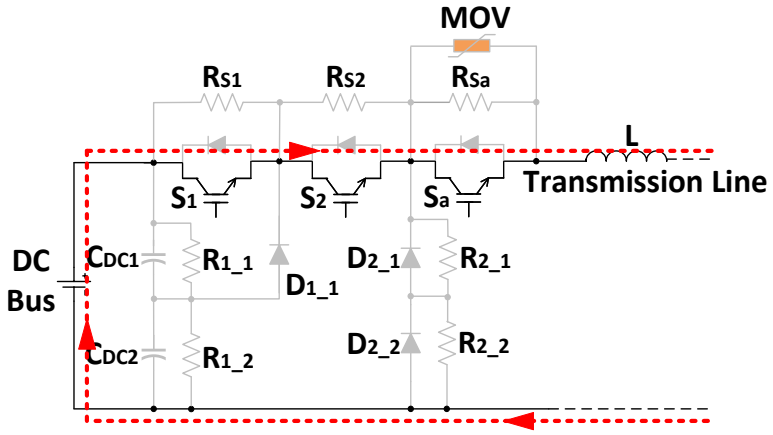
generalized to the SMLSSCBs with higher number of levels. The main subintervals of a 3-level SMLSSCB during its current breaking process are shown in Figure 5.5. The simulation results in PSIM are displayed in Figure 5.6 to assist interpreting the operating principle of the breaker. The key parameters in the simulation are summarized in TABLE 5-1.

During normal operation, all the switches in the breaker are turned on and the load current is conducted through the switches as shown in Figure 5.5(a). When there is a fault current detected, switch S_1 opens and transfers the fault current to the voltage clamping diode, D_{1_1}, as in Figure 5.5(b). Simultaneously, the voltage of S_1 is clamped to that of C_{DC1} and the source current drawn from the DC bus is decreased by half as in Figure 5.6 at t_0. After a short period of delay time preset by a controller, at t_1, switch S_2 opens and commutates the current from the DC bus to the ground clamping diodes as in Figure 5.5(c). Immediately, the voltage of S_2 is clamped to C_{DC2} and the source current drops to zero as Figure 5.6 at t_1. In other words, right after the switching of the main switches, the target of the protection for the breaker, that is, the DC bus, is isolated from the fault. Besides, at t_1, the increment of the fault current is interrupted as the line current waveform in Figure 5.6 from t_1 to t_2. After another short period of delay time, at t_2, the auxiliary switch S_a opens and transfers the line current to the MOV as Figure 5.5(d). Eventually the line current decreases gradually to zero as in the line current waveform in Figure 5.6 from t_2 to t_3.

TABLE 5 - 1: Key Parameters in the Simulation Case

Parameters	Values
DC bus voltage V_{DC}	2000V
Line current I_L	200A
Line inductor L	50μH
Voltage divider C_{DC}	10μF
Clamping voltage V_{clamp}	400V
Threshold current I_0	$1.5 \cdot I_L$

From the switches' voltage waveforms in Figure 5.6, during the whole current breaking process, there is no dynamic unbalanced voltage appearing on any of the semiconductor switches even though the switches are sequentially opened. Since the MOVs for dynamic voltage balancing are not needed in the SMLSSCB, the main switches in the breaker does not incur surge voltages and can be rated according to the system voltage. On the other hand, because the DC bus has already been isolated from the fault before the operation of the MOV, the clamping voltage of the MOV along with the rated voltage on the auxiliary switch can be rated at a low voltage level and does not induce significant surge voltages on the breaker as shown in the voltage waveform across the auxiliary switch, S_a, in Figure 5.6. In addition, since the steady-state voltages across S_a is very small, the low voltage rating of the MOV does not cause its premature aging after the breaker turns off. Thus, the SMLSSCB isolates fault current with an ultrafast speed and does not induce significant surge voltages or dynamic voltage unbalancing on its semiconductor switches.


MOV
RS1
RS2
RSa
L
Transmission Line
S1
S2
Sa
DC
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CDC1
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D1_1
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CDC2
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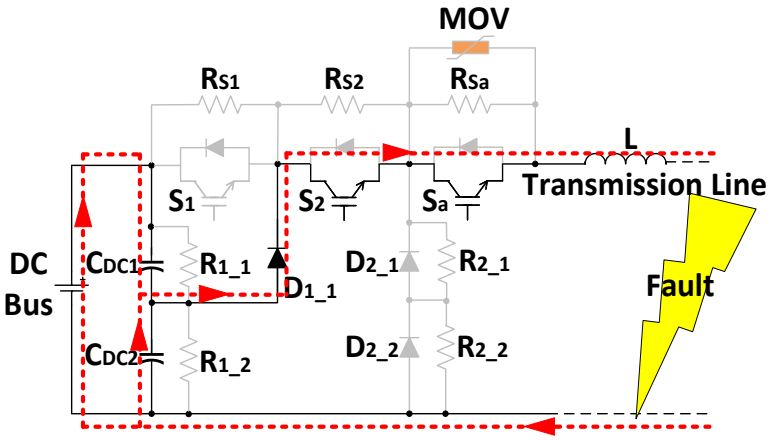
D2_2
R2_2

(a)


MOV
RS1
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Sa
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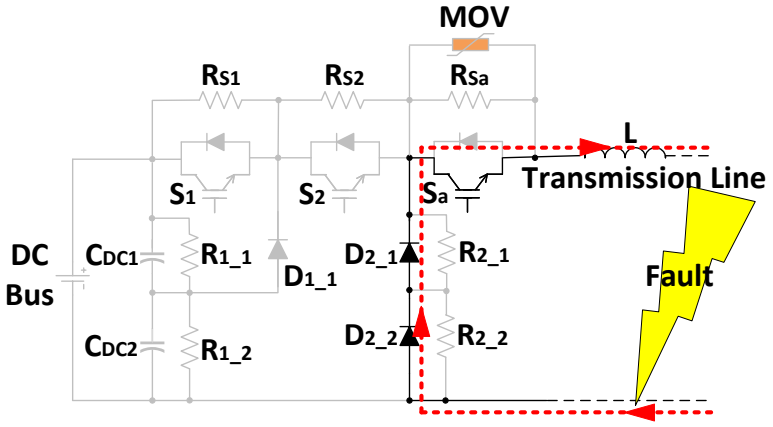
(b)


MOV
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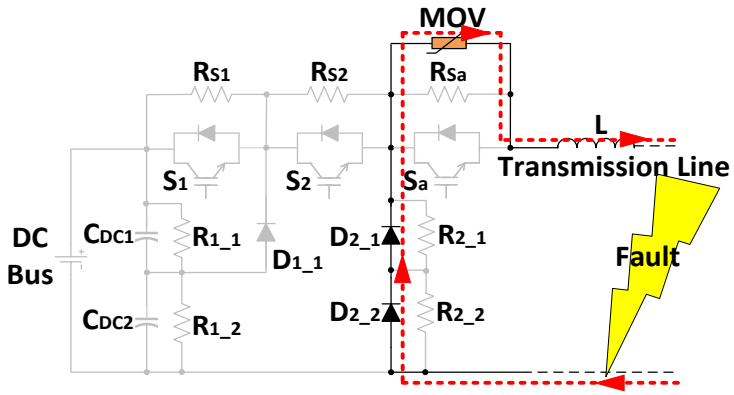
(c)



(d)

Figure 5. 5 Subintervals of a 3-level SMLSSCB during current breaking process.

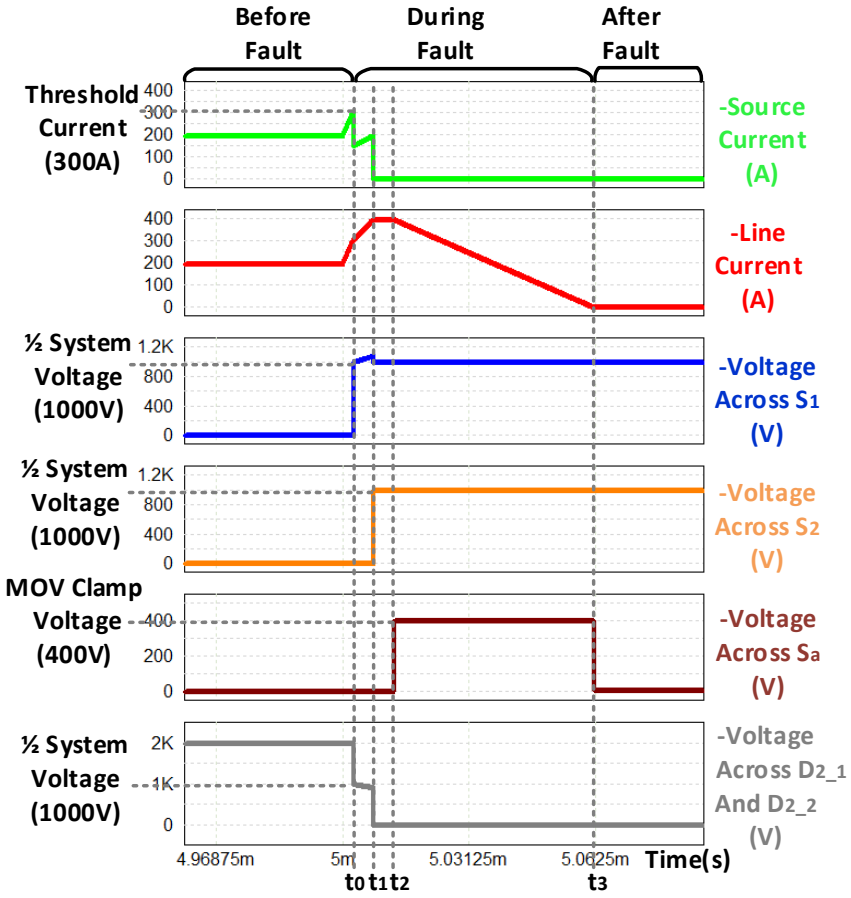
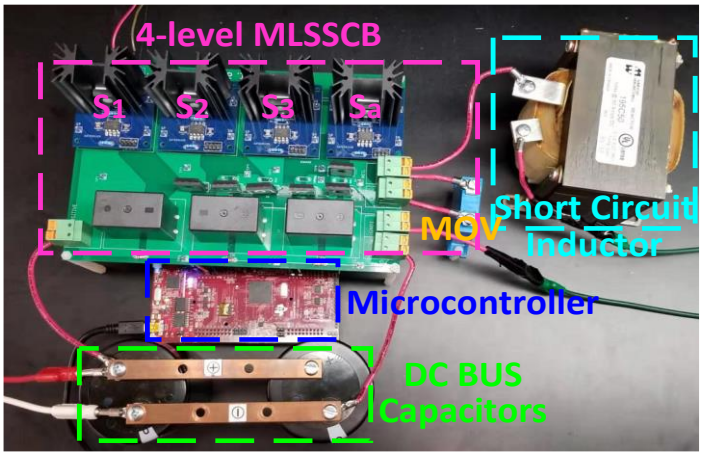
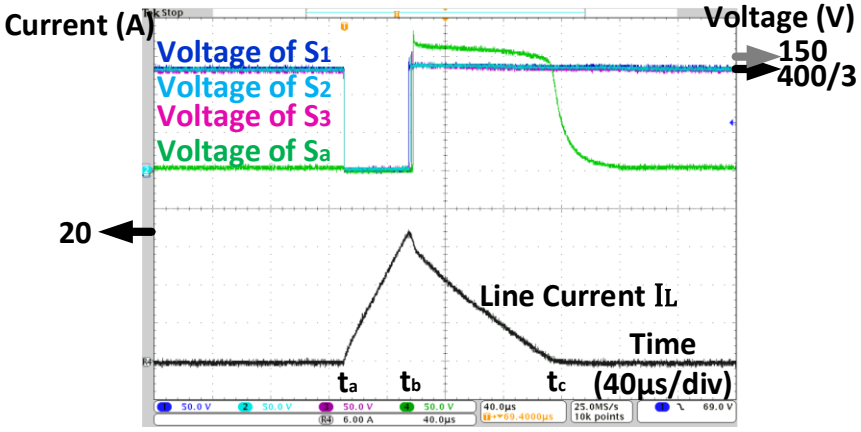


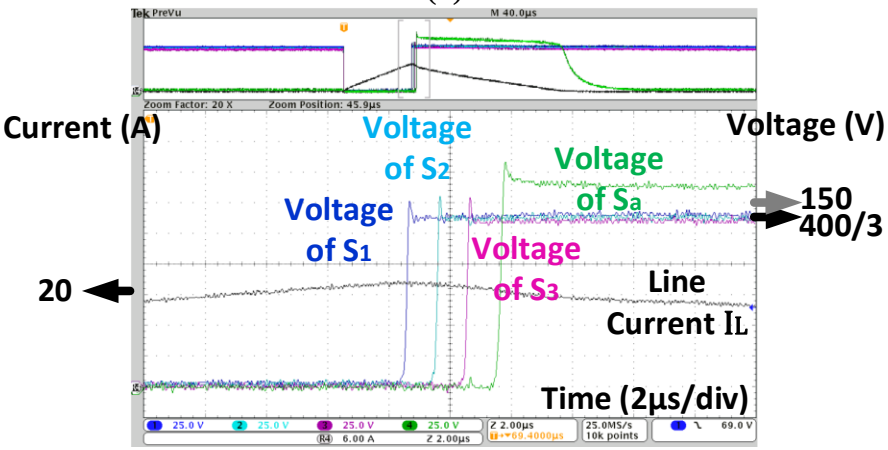
Figure 5. 6 Simulation waveforms of a 3-level SMLSSCB during current breaking process.



(a)



(b)



(c)

Figure 5. 7 Experiments of the proposed 4-level SMLSSCB, (a) Experimental Setup. (b) Experimental results during fault current interruption, 40µs/div. (c) 2µs/div.

The experimental results of a 4-level SMLSSCB during its current breaking process in a short-circuit tester are presented in Figure 5.7 to validate the simulation results. As shown in the voltage waveforms in the Figure 5.7(b), all the switches of the breaker turn on simultaneously at t_a to emulate a ground fault across the DC bus capacitors. After that, the line current starts to increase rapidly until t_b when the current exceeds 20A and breaker starts to operate. At t_b, the switches in the breaker are tripped to open from S_1 to S_a sequentially with 1μs time difference and their voltages are clamped to their corresponding voltage dividing capacitors. After the auxiliary switch, S_a, turns off, the line current is transferred to the MOV and finally extinguished at t_c in the current waveform of Figure 5.7(b). As shown in the enlarged voltage waveforms of the switches in Figure 5.7(c), during the whole operation of the breaker, there is no dynamic unbalanced voltage across any of the switches even though the switches are not turned off at the same time. Besides, the main switches, S_1, S_2 and S_3, do not have any of surge voltage across them during the operation so their voltage ratings do not need to be overdesigned like those in the conventional SSCBs. The auxiliary switch selected here is the same as the main switches and only a single MOV is used to demagnetize the short-circuit inductor. The clamping voltage of the MOV is only 150V that is much lower than the DC bus voltage but the MOV can still clear the line current effectively because the DC bus has been isolated from the fault during the operation of the MOV. Furthermore, since the steady-state voltage across S_a is very small as in the voltage waveform of Figure 5.7(b) after t_c, the MOV with a low continuous rated voltage of 100V in the prototype does not incur its premature aging after the operation of the breaker.

After the fault is cleared, the circuit breaker needs to be reclosed to restore the power supply for the load. During the reclosing process of the SMLSSCB, the switches are turned on sequentially and no dynamic overvoltage is induced on the series-connected semiconductor devices in the breaker. Furthermore, there is no additional auxiliary devices or sources needed to reclose the proposed breaker. The simulation waveforms of the SMLSSCB during it reclosing are plotted in Figure 5.8. In the waveforms, S_a is turned on first at t_4 followed by S_2 at t_5 and S_1 at t_6. Since the switches in the breaker have their voltage clamped by the capacitors during the switching transience, they do not incur any overvoltage while they are reclosing as shown in the switches' voltage waveforms in Figure 5.8. Moreover, from the voltage waveform across the series-connected diodes, D_{2_1} and D_{2_2}, at t_5, the total voltage across the diodes is only half of the DC bus voltage while they are switched off. In this way, even if the diodes have very different recovery speeds, the dynamic voltage across the diodes will not exceed their voltage ratings during the reclosing process. After the breaker is reclosed, the line current increases gradually to the rated current at t_7 and then the power supply to the load is restored.

The waveforms of the switches' voltages and line current during the reclosing test of the 4-level SMLSSCB prototype are displayed in Figure 5.9(a). From the voltage waveforms, the switches turn on sequentially from S_a to S_1 at t_d with a time difference of 1μs and do not have dynamic unbalanced voltage imposed on any of the switches. After that the line current starts to increase gradually without any current spike and reach its rated value of 4A at t_e as the current waveform in Figure 5.9(a). During the reclosing

process, the series-connected diodes are reversed biased and the voltages across them increase step by step as in Figure 5.9(b). From the experimental results in the figure, the total voltage across the diodes, D_{3_1}, D_{3_2} and D_{3_3}, is only one third of the DC bus voltage during the switching transience of the diodes and the overvoltage on the diodes due to their dynamic voltage unbalance can be averted. Besides, in steady state, the voltage is well shared by the didoes with the help of the snubber resistors.

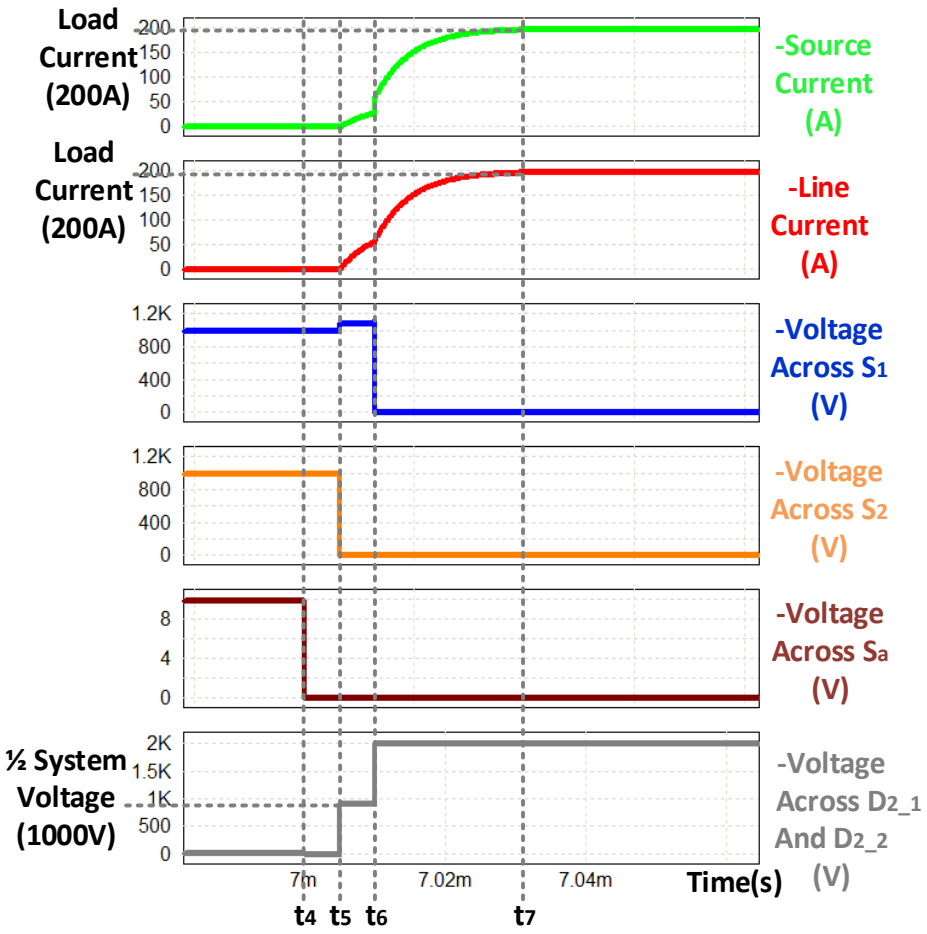
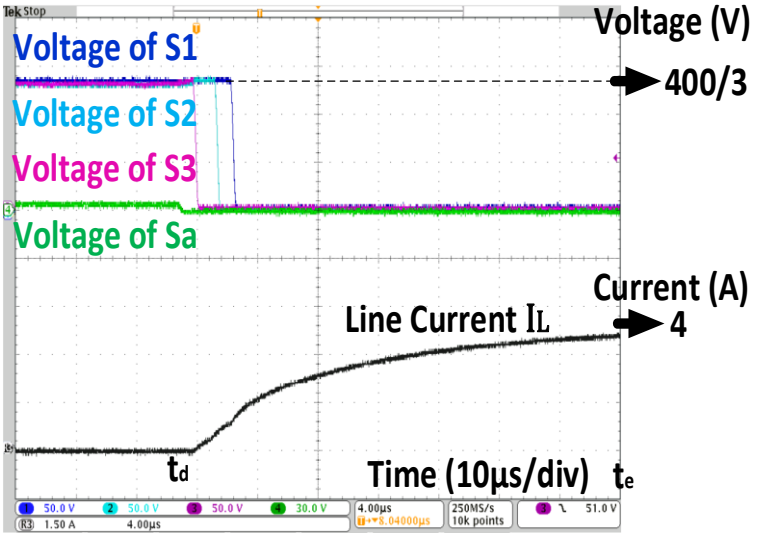
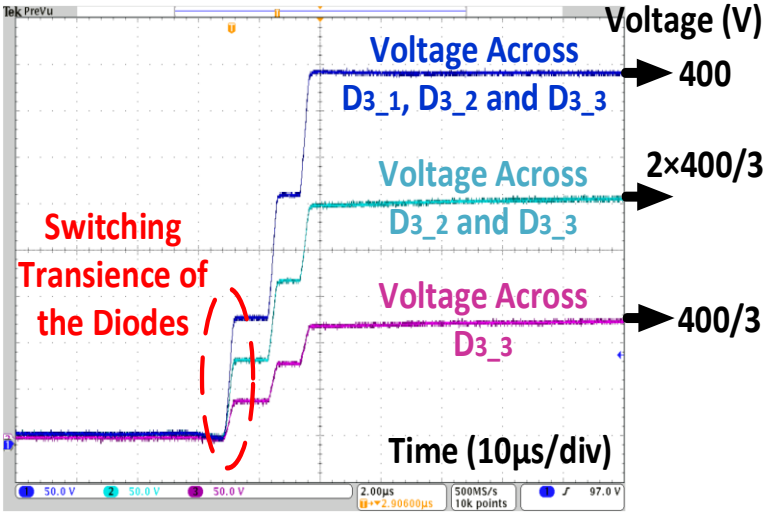


Figure 5. 8 Simulation waveforms of a 3-level SMLSSCB during circuit reclosing process.



(a)



(b)

Figure 5. 9 Experimental results of the 4-level SMLSSCB during circuit reclosing. (a) Switches' voltages and line current. (b) Diodes' voltages.

5.2 Design Considerations of the Surgeless Multilevel Solid-State Circuit Breaker

To warrant the normal operation of the SMLSSCBs, several technical considerations have to be made during the design of the breaker. First of all, the resistive

snubber circuits for static voltage balancing of the semiconductor devices need to be designed. Besides, the MOV in the breaker need to be selected according to the demands on its clamping voltage and energy volume. Finally, special consideration should be taken into the capacitances of the voltage dividers to avert the overvoltage imposed on the switching devices during the operations of the breaker.

5.2.1. Snubber Circuit Design

In the SMLSSCBs, snubber resistors are installed in parallel with the semiconductor devices to suppress the static voltage unbalance among the devices in the series-connected strings. After the breakers close, the voltage clamping diodes turn off and their snubber resistors enforce them to share the same amount of voltage. The resistances of the snubbers can be determined as

$$R_{sb} \leq \frac{(n-1)(1-k_s)V_{SN}}{(n-2)\widehat{I_b}} \tag{5.1}$$

where V_{SN} is the voltage rating of the devices, k_s is the voltage sharing factor equaling $\frac{V_{DC}}{(n-1)V_{SN}}$ and $\widehat{I_b}$ is the maximum leakage current of the device.

In the expression the maximum number of the series diodes in the breaker is used. To optimize the efficiency of the breaker, the snubber resistances for each of the diodes' strings can be calculated separately. After the breaker opens, the snubber resistors of the main switches conduct the leakage current and neutralize the switches' static voltage unbalance. Besides, as the auxiliary switch sustains a small amount of source voltage, reverse voltages are imposed on the voltage dividing diodes. In that case, the snubber

resistors of the didoes can conduct part of the leakage current of the switches and have influences on the switches' voltage in a steady state. From Figure 5.10, the static voltage of the switches can be expressed as

$$V_{S_1} = V_{S_2} = V_{S_3} + i_{D_2}R_s = V_{S_{n-1}} + \left(i_{D_2} + i_{D_3} + \cdots + i_{D_{n-2}}\right)R_s$$
$$= \frac{V_{DC}}{n-1} - \frac{1}{2}i_{D_2}\left(R_{2_1} + R_{2_2}\right) \qquad 5.2$$

where i_{D_2} to $i_{D_{n-2}}$ are the current through the conduction loop of the voltage clamping diodes as marked in Figure 5.10, R_s is the resistance of the snubber for the main switches. As the values of i_{D_2} to $i_{D_{n-2}}$ are all positive, from the Expression (r4), the voltage stresses on the switches decreases sequentially from S_1, S_2 to S_{n-1} and their maximum value of V_{S_1} maintains lower than $\frac{V_{DC}}{n-1}$ as well as the rated voltage of the switches. Therefore, the influence of the diodes' snubber resistors on the switches' voltage can be neglected during their design and the resistance of the switches' snubbers can also be determined from Expression (5.2).

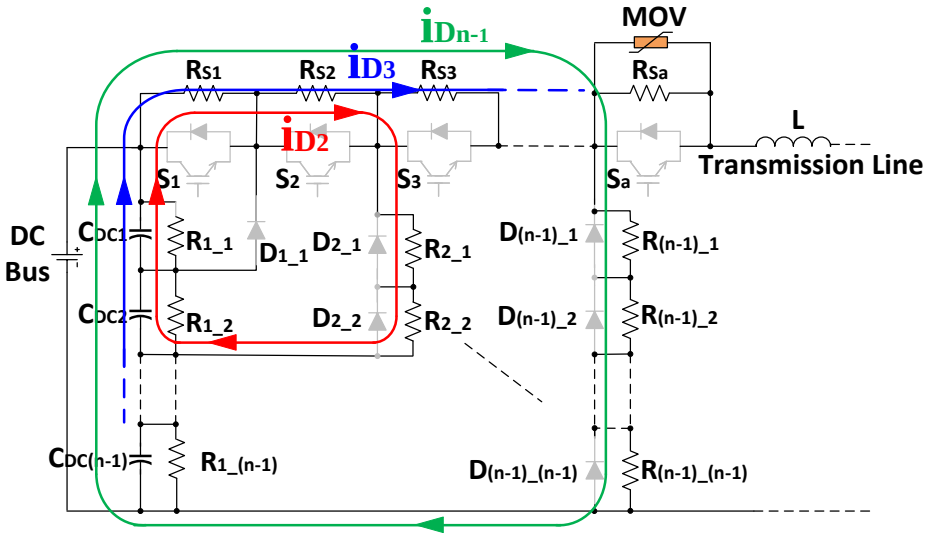


Figure 5. 10 The conduction loops of the diode's snubbers when the breaker opens.

5.2.2. MOV Selection

Unlike the conventional SSCB, which needs MOVs with large clamping voltages to shorten its fault isolation time, the SMLSSCB has an ultrafast isolation speed decoupled from its clamping voltage. For this reason, the MOV in the breaker can be rated at a low clamping voltage as long as it can clear the line current within the rated impulse duration set regards to the life span of the MOV. For a certain surge current value, the number of the current pulses that the MOV can sustain decreases reversely with the width of the pulses. In this way, to ensure a long-life span of the SMLSSCB, its MOV needs to clear the line current within a rated impulse duration according to their datasheet and the minimum clamping voltage of the MOV can be calculated by (5.3).

$$V_{clamp} \geq 1.5L\frac{I_0+\frac{n-2}{L}V_{DC}T_{delay}}{T_{id}} \tag{5.3}$$

where 1.5 is the safe margin for the different voltage-current characteristics of MOVs and T_{id} is the impulse duration.

Besides, since the impulse durations of the MOVs are typically much shorter than the reclosing time of the breaker that is usually 0.2-0.5s, the breaker with the MOV selected by (5.3) can meet its demand on circuit reclosing [15].

From (5.3), the clamping voltage of the MOV in the proposed breaker can be rated at low voltage levels for many common medium voltage DC systems. Such as the simulation case in Tab. I, if a MOV from the little fuse's TMOV (20mm) series is used, according to the MOV's datasheet, the impulse duration of the MOV that allow the breaker to operate for 1000 times is 30μs. After the impulse duration is substituted into

(5.3), the minimum clamping voltage of the MOV is calculated to be 1125V that is much lower than the clamping voltage of 3000V for the conventional SSCB counterpart.

Except for the clamping voltage, the energy volume of the selected MOV needs to be larger than the residual energy in the system line inductance as expressed in (5.4).

$$W_{MLSSCB} = \frac{1}{2} L (I_0 + \frac{n-2}{L} V_{DC} T_{delay})^2 \quad 5.4$$

5.2.3. Capacitor Selection

To warrant the normal operation of the SMLSSCBs, the capacitances of the voltage dividers in the breaker need to be carefully determined.

As shown in Figure 5.5(b), between the operations of the Switches, S_1 and S_2, the line current is transferred to the conduction path charging the capacitor C_{DC1}. At the same time, the voltage across C_{DC1} along with the voltage across the switch S_1 increases as shown in the voltage waveform of S_1 between t_0 and t_1 in Figure 5.6. After S_2 opens at t_1, the voltage of S_1 drops a bit in that the diode, D_{1_1}, blocks part of the capacitor voltage, but the voltage clamps back to the voltage of C_{DC1} when the breaker recloses. In that case, the voltage increment on S_1 during the operation of the breaker is directly affected by the voltage change of C_{DC1}. For the SMLSSCBs of higher levels, this voltage increment also appears on some of the other main switches, but it is always worst in S_1. Thus, to avert the switching devices in the SMLSSCBs impaired by overvoltage during their operations, the voltage across C_{DC1} needs to be kept lower than the rated voltage of the switching

device, which can be achieved by the proper selection of the voltage dividing capacitors in the breaker.

If the breaker detects the fault and starts to operate at the time instant when $t = 0$, the increment of the voltage across $\mathrm{C_{DC1}}$ during the breaking process can be expressed as

$$\Delta V_{\mathrm{C_{DC1}}} = \frac{1}{C_{DC1}} \int_0^{T_{iso\_MLSSCB}} i_{C_{DC1}}(t)dt. \tag{5.5}$$

Since the number of the capacitors on the conduction path of $\mathrm{C_{DC1}}$ increases gradually while the SMLSSCB opens, the current through $\mathrm{C_{DC1}}$ steps down after each of the main switches in the breaker turns off and its value can be expressed by the line current, $i_L(t)$, as

$$i_{C_{DC1}}(t) = \begin{cases} \dfrac{n-2}{n-1} i_L(t) & 0 \le t \le T_d \\ \dfrac{n-3}{n-1} i_L(t) & T_d \le t \le 2T_d \\ \vdots & \\ \dfrac{1}{n-1} i_L(t) & (n-3)T_d \le t \le (n-2)T_d \end{cases} \tag{5.6}$$

With the voltage across the transmission line stepping down sequentially to different voltage levels during the current interruption of the breaker, the line current during each time period in (5.6) can be determined by

$$i_L(t) = \begin{cases} I_0 + \frac{1}{L}\frac{n-2}{n-1} V_{DC}\, t & 0 \le t \le T_d \\ I_0 + \frac{1}{L}\frac{n-2}{n-1} V_{DC}\, T_d + \frac{1}{L}\frac{n-3}{n-1} V_{DC}\,(t - T_d) & \\ & T_d \le t \le 2T_d \\ \vdots & \\ I_0 + \frac{1}{L}\frac{n-2}{n-1} V_{DC}\, T_d + \cdots + \frac{1}{L}\frac{1}{n-1} V_{DC}[t - (n-3)T_d] & \\ & (n-3)T_d \le t \le (n-2)T_d \end{cases} \tag{5.7}$$

After 5.6 and 5.7 are introduced into 5.5, the range of the capacitance of C_{DC1} can be attained from some easily available parameters of the breaker and its applied system as

$$C_{DC1} > \frac{1}{\left(V_{SN} - V_{C_{DC1}(0)}\right)(1-10\%)}\left[\frac{n-2}{2} I_0 T_{delay} + \sum_{a=1}^{n-3} \frac{(a+1)a}{2(n-1)^2}(n - a - 2)\frac{1}{L} V_{DC}\left(T_{delay}\right)^2 + \sum_{b=1}^{n-2}\left(\frac{n-b-1}{n-1}\right)^2 \frac{1}{L} V_{DC} \frac{(2b-1)\left(T_{delay}\right)^2}{2}\right] \quad 5.8$$

where $V_{C_{DC1}(0)}$ is the initial voltage of C_{DC1} that equals $\frac{V_{DC}}{n-1}$ and 10% of capacitance tolerance is included.

To evenly share the system voltage, the other voltage dividing capacitors have the capacitance same as C_{DC1}. As the capacitors' charging periods are shorter than that of C_{DC1}, their voltage increments are also suppressed in the safe ranges of the main switches' rated voltage.

Thus, the minimum capacitances of the voltage dividers in the proposed SMLSSCBs may be determined according to 5.8 and are presented in Figure 5.11. From Figure 5.11, it may be seen that the capacitance in the breaker increases with the system power rating and decreases reversely with the system inductance. Besides, in the voltage range from 2000 V to 5000 V, current range from 100 A to 300 A and system inductor from 50 μH to 90 μH, the demands on the capacitances in the breakers are lower than 15 μF which may be easily met by the commercially available film capacitors.

The design of the capacitors for the SMLSSCB is also discussed with a simulation case shown in Figure 5.12. In the simulation, a 6-level SMLSSCB is applied to a 5000 V, 300 A and 50 μH DC distribution system. The voltage dividing capacitors are set to be

14.5 µF according to the results in Figure 5.11. From Figure 5.12, the voltage of S_1 clamps to C_{DC1} and reaches its maximum value when the breaker recloses. The maximum voltage is right below the switch's rated voltage of 1.2 kV and the capacitor selection method is validated in this case.

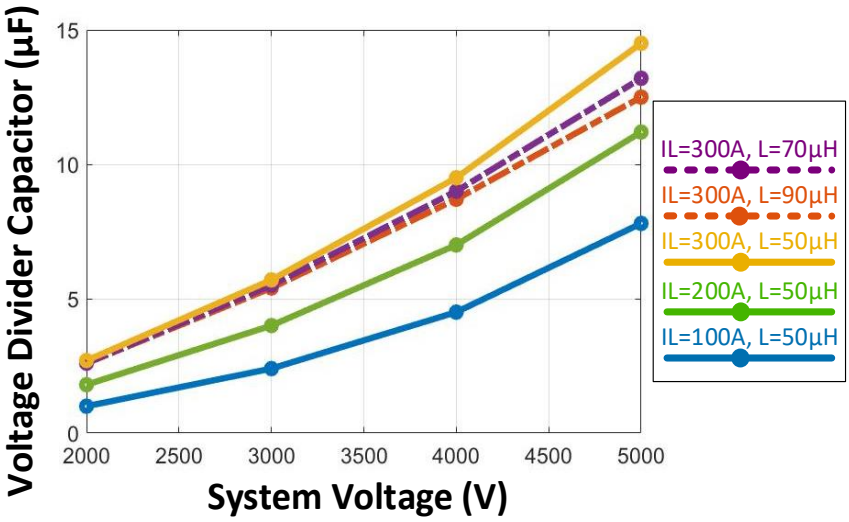


Figure 5. 11 Minimum capacitances in voltage divider for proposed SMLSSCBs in typical medium voltage DC distribution systems.

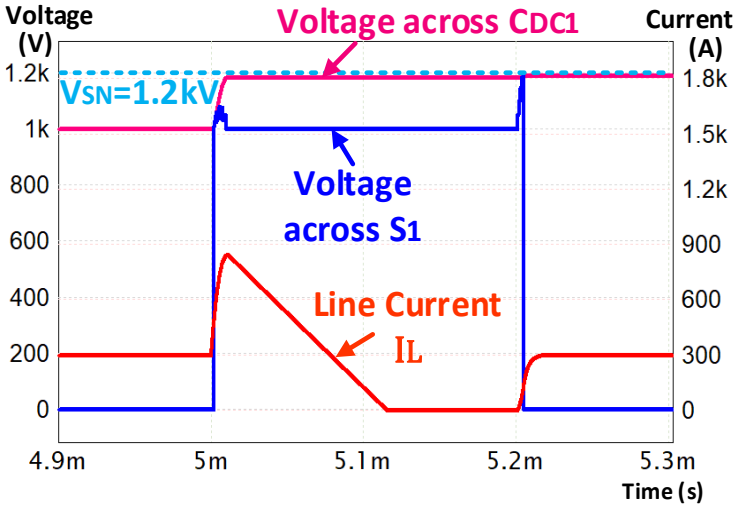


Figure 5. 12 Voltages across C_{DC1} and S_1 during the operation of the 6-level SMLSSCB in a 5000 V, 300 A and 50 µH applied system.

5.3 Comparisons between the Surgeless Multilevel Solid-State Circuit Breakers and the conventional Solid-State Circuit Breaker

To illustrate the advantages of the proposed SMLSSCB in terms of fault isolation speed and efficiency, the comparison of the proposed breaker with the conventional SSCB is presented as below.

5.3.1. Isolation Time

One of the principal objectives of the circuit breaker is to isolate the source from the faulted area at a higher speed. If the speed of the isolation is not fast enough, severe voltage drop may happen on the source capacitors and results in the failure of the entire system [38].

For the proposed SMLSSCB, the breaker isolates the fault from the sources immediately after the operations of its main switches and its isolation speed is directly decided by the characteristics of its semiconductor switches and fault detectors.

That is, even in the working scenarios with large line inductance and load current, the breaker can still isolate faults at an ultrafast speed by using a small MOV. The isolation time of a n level SMLSSCB can be estimated by

$$T_{Iso\_MLSSCB} = T_{off} + (n-2)T_d \tag{5.9}$$

where T_d is the delay time set between the gate signals for the adjacent switches in the breaker.

To validate the faster isolation of the SMLSSCB, a comparison between the isolation time of the breaker and that of the conventional SSCB are made in a 2000 V 200

A DC system shown in Figure 5.13 where the system parameters in TABLE 5-1 are used. For the conventional SSCB, V_{clamp} is set at 1.5 times of the system voltage and I_0 is 1.5 times of the line current. T_{off} for the fault current is selected to be 1 μs that can be easily achieved by using commercial SiC MOSFETs [51]. For the SMLSSCB, T_d needs to be larger than the maximum T_{off} of the switch to ensure the sequentially switching of the semiconductor devices and is set twice of the T_{off}, namely 2 μs. From Figure 5.13, it may be observed that the isolation speed of the proposed breaker is significantly faster than that of the conventional one in wide ranges of line inductances. Besides, with the increment of the line inductances, this advantage becomes more prominent.

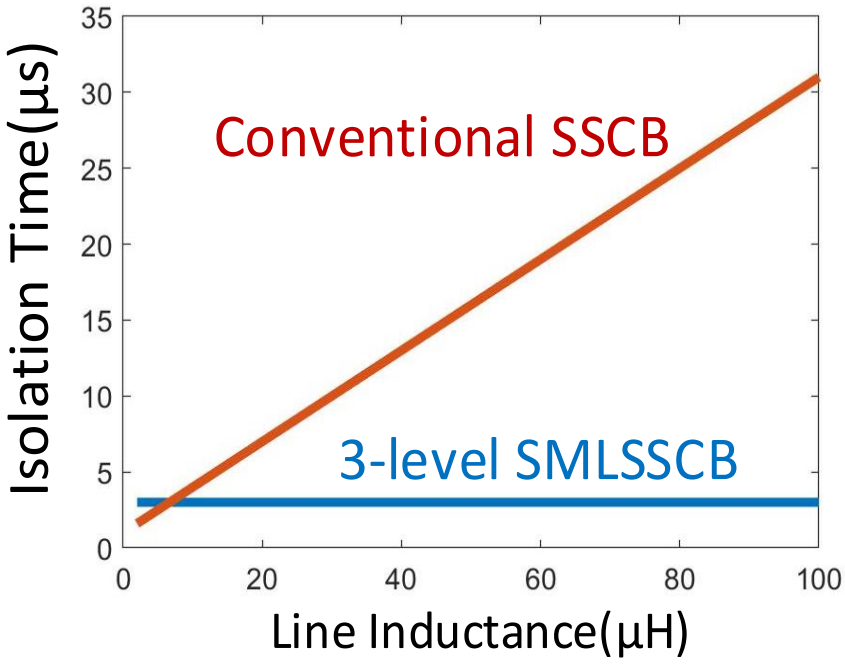


Figure 5. 13 Comparisons between the isolation time of a conventional SSCB and that of a 3-level SMLSSCB in a 2000 V 200 A DC system.

5.3.2. Power Efficiency

The relatively low efficiency of SSCBs is the main barrier that restricts the adoption of the SSCBs in the main power protection markets and has been attributed to the conduction losses of the semiconductor switches. With the large surge voltages during their operations, the conventional medium voltage DC SSCBs have to use semiconductor devices with overdesigned voltage ratings. This exacerbates the low efficiency problem because the same type of power semiconductor device with higher breakdown voltage has a thicker drift region and larger on-state resistance [47]. This tradeoff has been manifested by the ideal specific drift region resistance of MOSFETs as shown in (5.10) [52],

$$R_{on\_sp,ideal} = \frac{4BV^2}{\varepsilon_s \mu_n {E_C}^3} \tag{5.10}$$

where BV is the breakdown voltage of the device, ε_s is the dielectric constant of the applied material, $\mu_n$is carrier mobility and E_C is the critical electric field for breakdown. The denominator in (5.10) is decided by the semiconductor material properties, so the specific on-resistance of the same type of switches is increased exponentially with its breakdown voltage [53] [54].

Conversely, by employing the SMLSSCB with no surge voltage on its main switches, the efficiency of the solid-state protection is significantly improved. To demonstrate this advantage, the proposed breakers of different levels are compared with the conventional SSCBs in regard to their efficiencies. In the comparison, for the conventional SSCB, the topology in Figure 5.1 is used and the total clamping voltage of

the MOVs in the breaker is set to be 1.5 times of the system voltage; for the SMLSSCBs, the auxiliary switch uses the same power device as the main switches. Two types of SiC MOSFETs from the product series made by the same manufacturer as in TABLE 5-2 are applied to the SMLSSCB and the conventional SSCB respectively.

TABLE 5 - 2: Switches Used in Breakers' Efficiency Comparison.

	SMLSSCB	**Conventional SSCB**
Selected Devices	**C2M0025120D**	**C2M0045170D**
Drain to source voltage (V_{dss})	1200 V	1700 V
Continuous Drain (Id) @ 25°C	90 A	72 A
$R_{ds\ on}$ max @ 50A (Id), 20V (V_{gs})	34 mΩ	70 mΩ

The switch for the SMLSSCB is rated at 1.2 kV to withstand its shared system voltage of 1 kV and the switch for the conventional SSCB is rated at 1.7 kV to sustain the clamping voltage of the MOV of 1.5 kV. The number of the switches in both breakers increases by one more whenever the system voltage value increases 1 kV. The load current for the comparison is 50 A in which the on-state resistances in TABLE 5-2 is measured. In the aforementioned conditions, the conduction losses of the SMLSSCB and conventional SSCB may be calculated by

$$P_{con} = {I_L}^2 n_s R_{ds\ on} \tag{5.11}$$

where I_L is the line current, n_s is the number of the semiconductor switches and $R_{ds\ on}$ is the drain-source on resistance of the switches.

Except for the conduction loss, the power losses caused by the snubber resistors in the SMLSSCB is also considered in the comparison. As the switches and the diodes in

the breaker have the same maximum number of series-connected components and their static voltage balances are not affected by the snubber resistors of each other, the resistance ranges of the snubbers for both the switches and the diodes in a n-level breaker can be determined by (5.1).

Since the snubbers for the switches do not impair the efficiency of the breaker, they are not included in the analysis. The didoes do not conduct the current in normal situations and their junction temperature can be maintained at room temperature. Therefore, the maximum leakage current of the diodes here is set at 100 μA that can be easily achieved by the commercial 1200 V Si/SiC diodes at 25ºC. As the snubbers for the capacitors have a long working period, their time constants along with resistances are allowed with large values. To be decoupled from the diodes' snubbers, the resistance of the capacitor's snubbers can be expressed as

$$R_{cb} = \frac{(n-1)V_{SN} - V_{DC}}{(n-3)V_{DC}} R_{sb} \tag{5.12}$$

With the above assumptions, the losses of the snubbers can be given by

$$P_{sb} = \frac{n_{sb}{V_{DC}}^2}{(n-1)^2 R_{sb}} + \frac{{V_{DC}}^2}{(n-1)R_{cb}} \tag{5.13}$$

where n_{sb} is the number of the snubber resistors for the diodes and capacitors in the breaker, which equals $\frac{n^2+n-4}{2}$.

Resulting from the rarity of the switching operations of the SSCBs, the switching losses of the semiconductor devices are usually not considered during the efficiency evaluation of the SSCBs. Thus, the power efficiency of the SMLSSCB can be estimated by

$$\eta = \frac{P_{out}}{P_{out} + P_{con} + P_{sb}} \tag{5.14}$$

where P_{out} stands the output power through the circuit breaker.

From (5.14), the comparison results are achieved as shown in Figure 5.14. From the figure, in a wide range of system voltages, the efficiencies of the SMLSSCBs are significantly larger than those of the conventional SSCB. Besides, from the comparison between the efficiency of the SMLSSCB with snubber losses and that without snubber losses, the snubber circuit in the SMLSSCB has negligible effect on the breaker's efficiency.

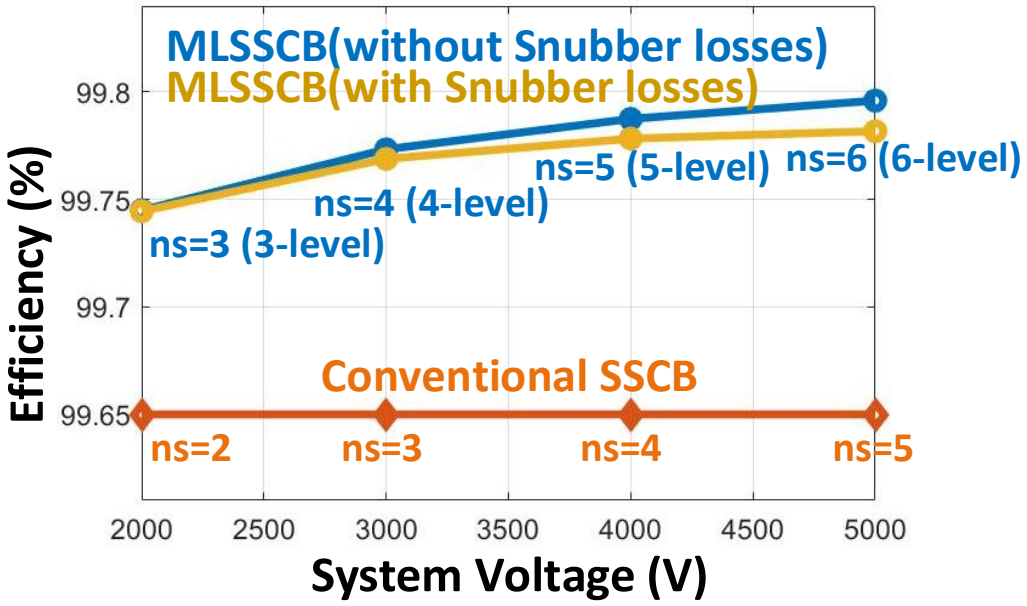


Figure 5. 14 Comparison between the efficiencies of the proposed SMLSSCB and those of the conventional SSCB ($I_L = 50$ A).

5.4 Bi-directional Configurations of the Surgeless Multilevel Solid-State Circuit Breaker

Similar to the MLSSCB, the symmetric bi-directional configuration of the MLSSCB can be attained by mirroring the topology of the unidirectional SMLSSCB in Figure 5.3 horizontally and is drawn in Figure 5.15. The right half of the breaker is for interrupting the fault current flowing from the DC Bus to the transmission line and the left part is for the fault current from the line to the DC Bus. The current limiter, L_S, is installed to limit the increment of the fault current. During the current breaking process of the bidirectional SSCB, the switches for the line-side fault and their symmetrical counterparts for DC-bus fault turn off sequentially from the middle to the two ends.

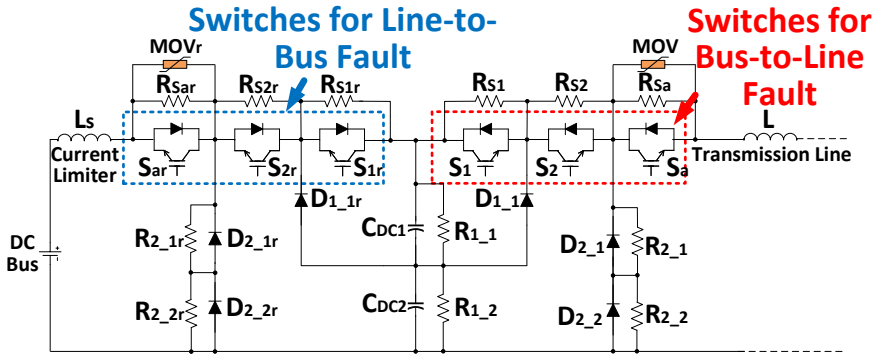


Figure 5. 15 Symmetrical bidirectional configuration of a 3-level SMLSSCB.

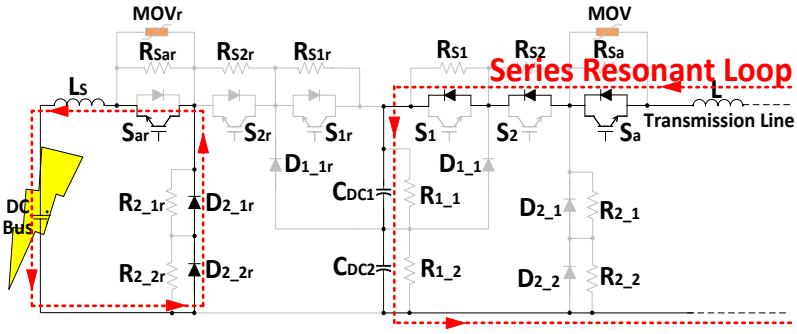


Figure 5. 16 Series resonant loop of the symmetrical bidirectional SMLSSCB during a line-to-bus fault.

To interrupt a fault current following through line to the DC bus, the main switches in the symmetric bi-directional SMLSSCB trip to open and a series-resonant loop of the line inductor and voltage dividing capacitors is formed as highlighted in Figure 5.16. The resonant voltage ripple on the capacitors can be expressed as

$$\Delta V_{C_{DC_{Resonant}}}(t) = \sqrt{\frac{L}{C_{DC}(n-1)}}\, I_0 sin \sqrt{\frac{n-1}{LC_{DC}}}(t) \qquad 5.15$$

After taking into account the increment in the capacitor voltage during the switches delay time, the maximum value of the capacitor's voltage increment in a symmetrical bi-directional SMLSSCB may be attained from

$$\Delta V_{C_{DC1}}(t)_{max} = \frac{1}{C_{DC}} \int_0^{T_{iso\_MLSSCB}} i_{C_{DC1}}(t)\, dt + \sqrt{\frac{L}{C_{DC}(n-1)}}\, I_0 \qquad 5.16$$

To avert the overvoltage imposed on the switches during the breaker's reclosing, the capacitors need to be large enough to suppress their peak voltage under the rated voltage of the switches as

$$C_{DC1} > \left[\frac{2 \int_0^{T_{iso_{MLSSCB}}} i_{C_{DC1}}(t)\, dt}{\sqrt{\frac{L}{n-1} {I_0}^2 + 4 \int_0^{T_{iso_{MLSSCB}}} i_{C_{DC1}}(t)\, dt \left(V_{SN} - V_{C_{DC1}}(0) \right)} - \sqrt{\frac{L}{n-1}} I_0} \right]^2 \qquad 5.17$$

In a 5000 V, 300 A and 50 μH simulation case, the feasibility of the capacitor design is validated as shown in Figure 5.17. In the figure, with the capacitance of 90 μF attained from (5.17), the voltage across the switch is suppressed under its rated voltage of 1.2 kV. By setting the system voltage, the line current and inductance in Expression (5.17) as variables, the minimum capacitances for the bidirectional SSCBs in serval medium

voltage DC systems may be summarized as illustrated in Figure 5.18. From the figure, the capacitance values decrease with the enhancement of the system voltage because of the larger voltage margin made by more switches. Besides, because of the resonant voltage on the capacitors, the capacitances increase with the system line inductance, which makes the bi-directional configuration more suitable for the medium voltage DC systems with smaller line inductances, such as electric shipboards. In addition, if the current limiting inductance, L_s, is larger than the system inductance, the L in Expression (5.17) needs to be substituted by L_s to make the design method valid for bi-directional circuit protection.

To perform bidirectional protection in the applications with larger line inductances, a hybrid bidirectional configuration of the SMLSSCB has been proposed as presented in Figure 5.19. In the figure, the configuration is composed of a SMLSSCB to interrupt the bus-to-line fault and a conventional SSCB to address line-to-bus fault. In the line-to-bus fault scenario, the operation of the breaker is the same as that in conventional SSCB and the resonance on the capacitor voltage is averted. In this way, the hybrid bidirectional configuration may be applied to the medium voltage distribution systems with larger line inductances, such as offshore wind farms. Also, the installment of the breaker's current limiter, as L_S in Figure 5.19, does not affect the selection of the voltage dividing capacitors. In addition, because half of the hybrid configuration uses the conventional topology, its conducting efficiency is lower than that of the symmetrical configuration but still higher than that of the conventional bidirectional SSCBs.

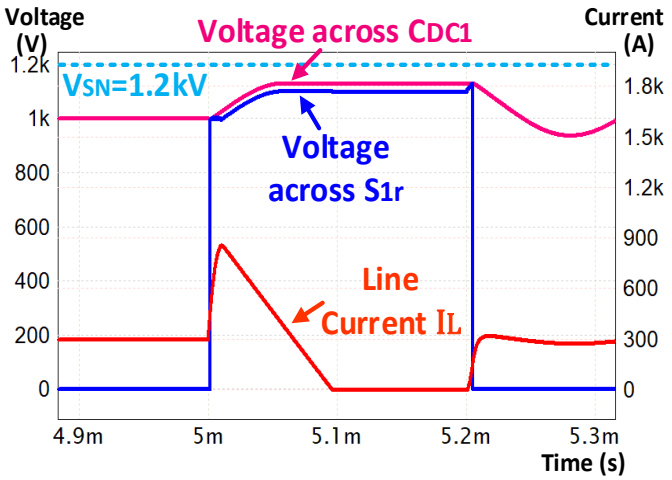


Figure 5. 17 Voltages across C_{DC1} and S_{1r} during the operation of the symmetrical bidirectional 6-level SMLSSCB in a 5000 V, 300 A and 50 µH applied system.

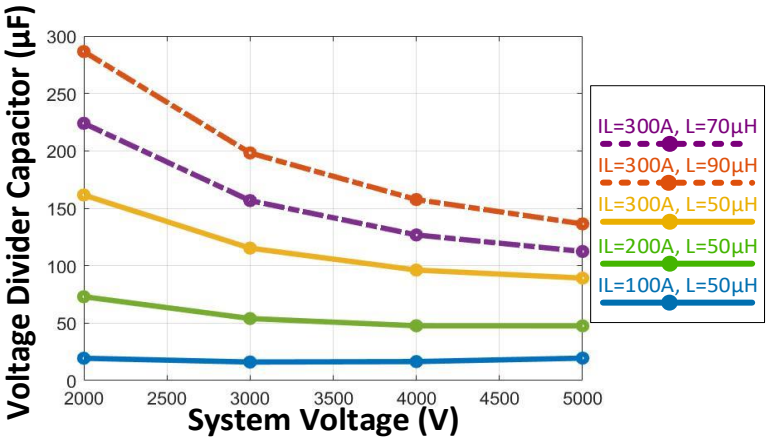


Figure 5. 18 Minimum voltage divider capacitances of the symmetrical bidirectional SMLSSCBs in typical medium voltage DC systems.

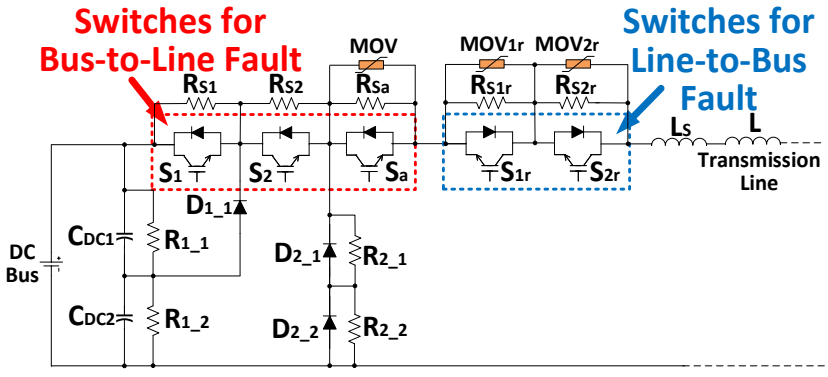


Figure 5. 19 Hybrid bidirectional configuration of a 3-level SMLSSCB.

CHAPTER 6: CONCEPT OF THE PROPOSED FAULT-TOLERANT MULTILEVEL SOLID-STATE CIRCUIT BREAKER

The Surgeless Multilevel Solid Solid-State Circuit Breaker (SMLSSCB) with its surgeless capability exhibits higher conducting efficiency and faster fault isolation speed compared to the conventional Solid-State Circuit Breakers (SSCBs). However, in exchange for these benefits, more auxiliary components are used in the breaker and make its reliability lower than that of the conventional SSCBs. To deal with this issue, a Fault-Tolerant SMLSSCB (FT-MLSSCB) has been proposed that can perform fault interruption even if one of its main switches fails. Besides, the proposed circuit breaker retains the surgeless capability of the SMLSSCB and, consequently, it can provide an efficient and reliable protection solution to the medium voltage DC systems. The operating principle of the FT-MLSSCB has been verified by simulations and its advantages on reliability, efficiency and isolation speed have been indicated in the comparisons among conventional SSCB, SMLSSCB and FT-MLSSCB.

In the MLSSCB, the switches turn off sequentially and with their voltage clamped to the corresponding voltage dividing capacitors, so that the dynamic voltage unbalancing among the switches can be averted. Also, with the ultra-fast isolation speed unrelated to MOV’s clamping voltage, the surge voltage on MLSSCB can be minimized and the efficiency of the MLSSCB can be higher than that of the conventional SSCB. However, to attain the advantages, extra auxiliary components are need in MLSSCB including voltage clamping diodes and film capacitors, which makes the reliability of the MLSSCB lower than the conventional SSCB. To improve the reliability of MLSSCB and maintain

its advantages on power efficiencies and isolation speeds, a fault-tolerant MLSSCB (FT-MLSSCB) have been proposed. In the FT-MLSSCB, several voltage clamping switches are installed to actively clamp the main switches' voltages to the lower voltage levels and maintain the switches' voltages lower than the voltage rating even if one of the switches fails. It is worth mentioning that the voltage clamping switches are not on the conduction path of the breaker and have no effect on the breaker's efficiency. Furthermore, the voltage clamping switches in short or open failure do not affect breaker's normal operations, so the addition of the switches does not impair the breaker's reliability. Moreover, the voltage clamping switches are tripped by the signals of the main switches and the extra sensors are not needed for the breaker's fault tolerant operations. In this chapter, the operating process of the FT-MLSSCB will be presented with the simulation results. The comprehensive reliability assessment will be made for the breaker according to a demonstrated evaluation method used for multilevel converters [55]. Eventually, the comparisons among the FT-MLSSCB, MLSSCB and conventional SSCB in terms of reliability, efficiencies and isolation time will be made and validated.

6.1 Operating Principles of the Fault-Tolerant Multilevel Solid-State Circuit Breaker

The circuit diagrams of the 4 level FT-MLSSCB and its general structure with n level are depicted in Figure 6.1 and Figure 6.2. From the figures, the FT-MLSSCB is mainly composed of the main switches, S_1 to S_{n-1}, low-voltage auxiliary switch, S_a, MOV, voltage clamping diodes, D_{2_1} to $D_{(n-1)\_(n-1)}$, voltage clamping switches, S_{VC1}

to $S_{VC(n-2)}$ and redundant switch, S_r. Herein, the operating principle of the 4-level FT-MLSSCB is mainly focused on and the analytical method can be generalized to the FT_MLSSCB with higher levels. The subintervals and simulation results of the 4-level

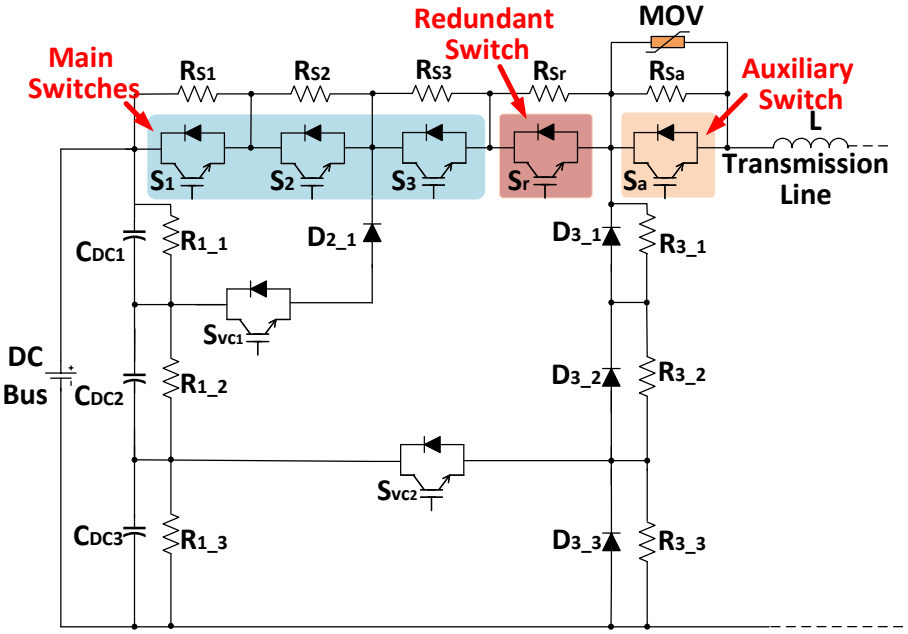


Figure 6. 1 Simplified schematic of 4-level FT-MLSSCB.

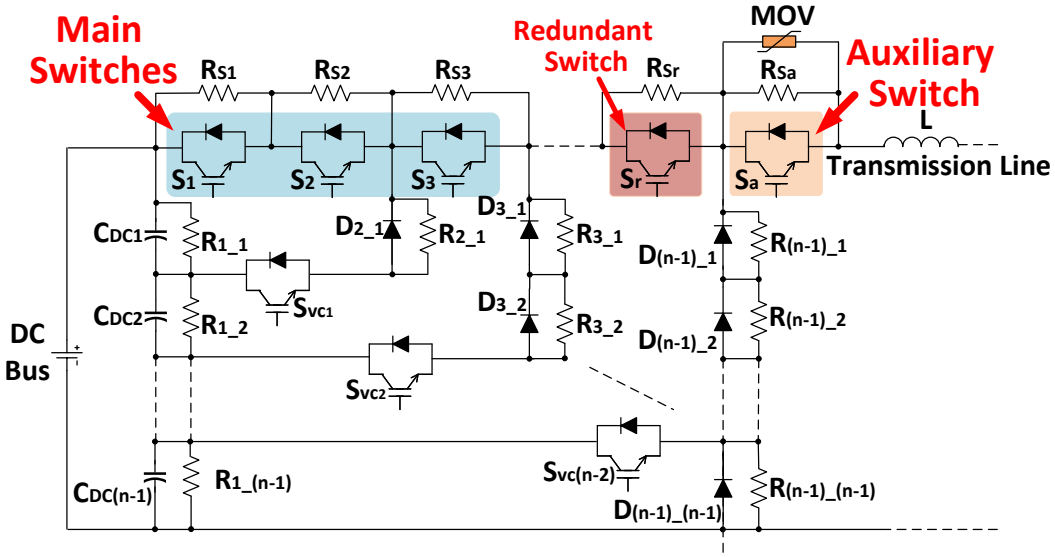
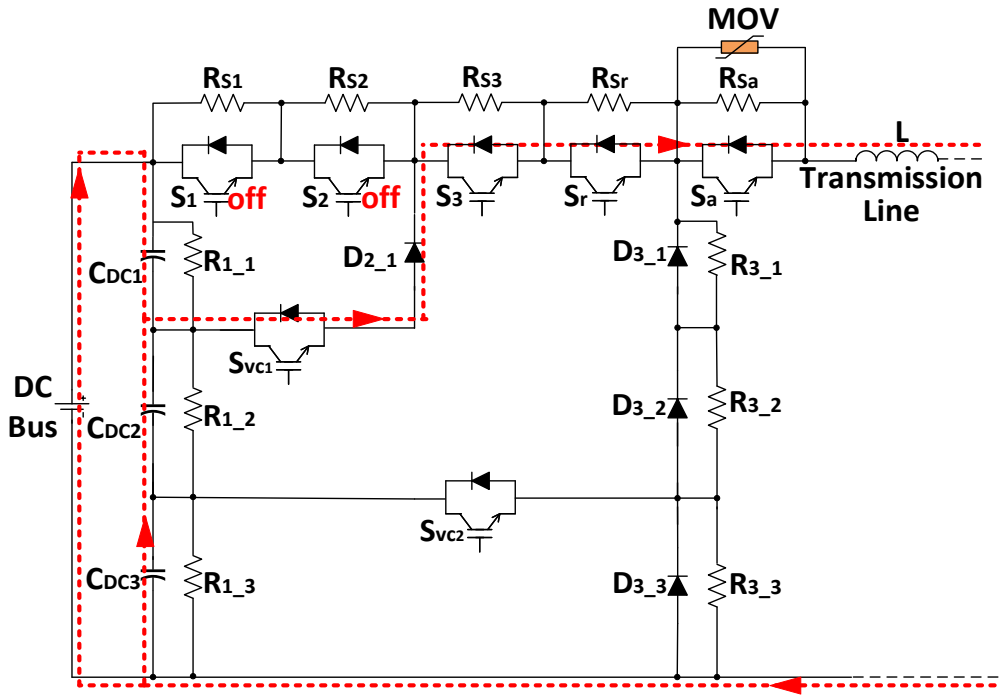
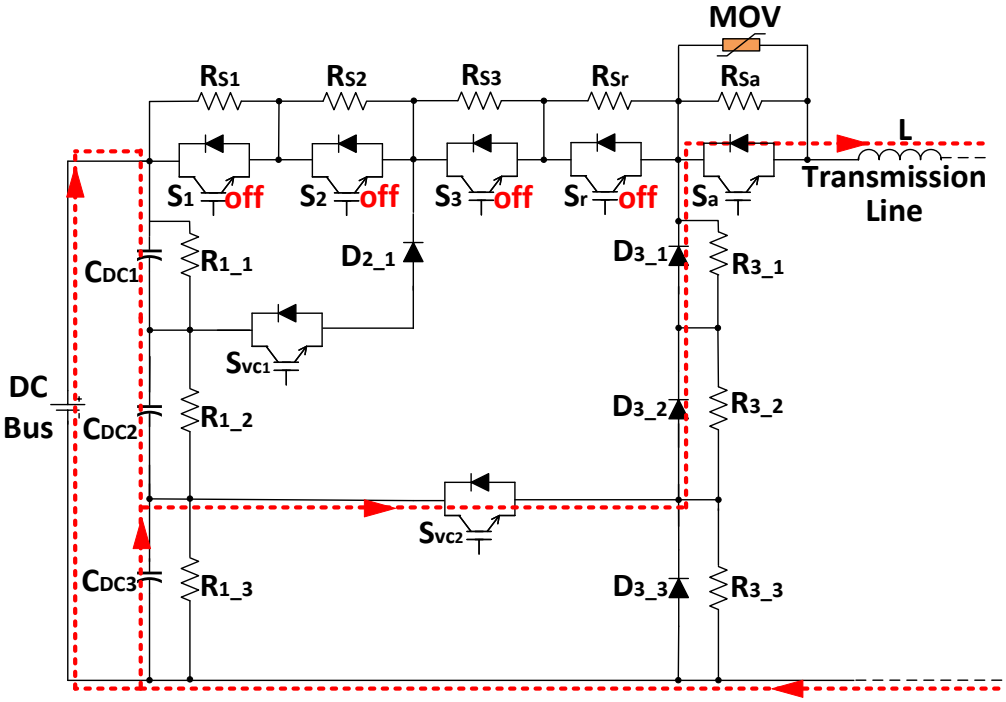


Figure 6. 2 Simplified schematic of n-level FT-MLSSCB.

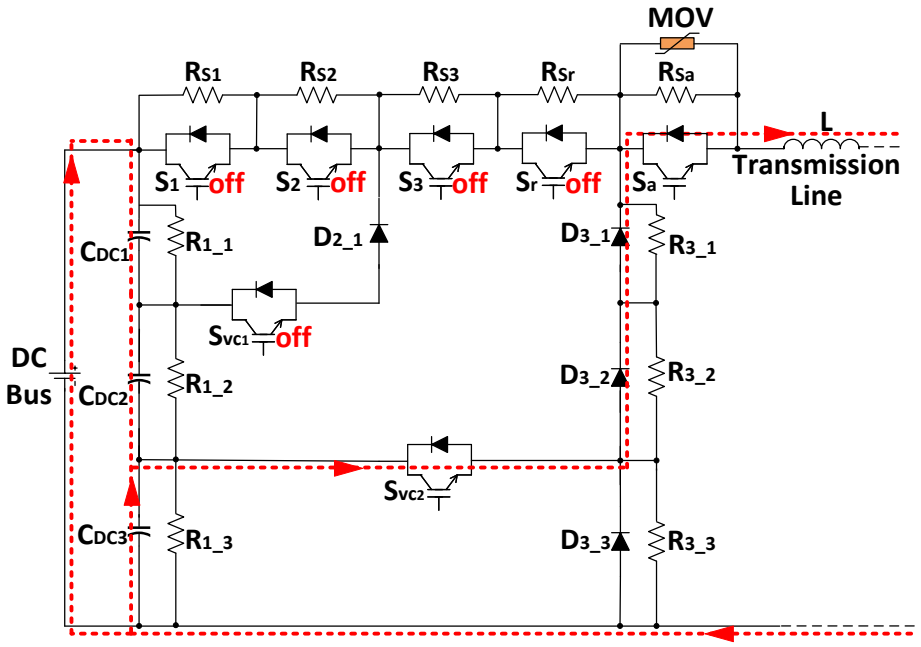
FT-MLSSCB in the current breaking process are depicted in Figure 6.3 and Figure 6.4 respectively. Under normal conditions, all the switches of FT-MLSSCB turn on and the load current conduct through the main switches and the auxiliary switch. When there is a fault detected, S_1 and S_2 turn off and transfer the fault current to the conduction path through S_{VC1} as shown in Figure 6.3(a). During the subinterval, as the total voltage across the two switches is just one third of the system voltage, the potential dynamic voltage unbalance among S_1 and S_2 does not cause overvoltage on the switches. Besides, with C_{DC1} inserted into the conduction path of the DC bus, the source current drawn from the DC bus is decreased by one third as the waveforms of I_S in Figure 6.4 at t_0. After a short period of delay time, S_3 and S_r turn off and commutate the fault current to S_{VC2} as shown in Figure 6.3(b). In the switching state, the total voltage stress on S_3 and S_r is only one third of the system voltage, so the voltage on each switch can be guaranteed lower than their voltage ratings. Meanwhile, C_{DC2} added on the conduction path of the course current decreases the current value by another one third as in Figure 6.4 at t_1. After another short delay, S_{VC1} turns off and release the voltage clamp of S_1 and S_2 and allow the switches to share more voltage stress than the voltage of C_{DC1}. Eventually, S_{VC2} and S_a turn off transferring the fault current to the ground clamping diodes and MOV. Meanwhile, the source current drops to zero and the rest one third of system voltage is imposed on the main switches as shown in Figure 6.4 at t_3.


MOV
RS1
RS2
RS3
RSr
RSa
L
Transmission Line
S1 off
S2 off
S3
Sr
Sa
CDC1
R1_1
D2_1
D3_1
R3_1
SVC1
DC Bus
CDC2
R1_2
D3_2
R3_2
SVC2
CDC3
R1_3
D3_3
R3_3

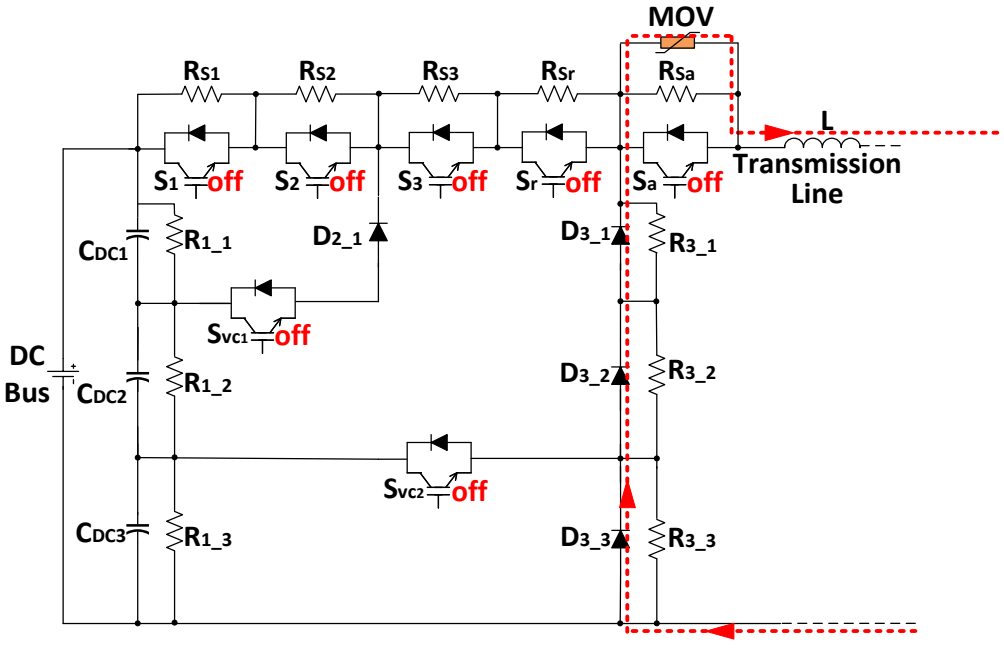
(a)


MOV
RS1
RS2
RS3
RSr
RSa
L
Transmission Line
S1 off
S2 off
S3 off
Sr off
Sa
CDC1
R1_1
D2_1
D3_1
R3_1
SVC1
DC Bus
CDC2
R1_2
D3_2
R3_2
SVC2
CDC3
R1_3
D3_3
R3_3

(b)



(c)



(d)

Figure 6. 3 Subintervals of a 4-level FT-MLSSCB during current breaking process.

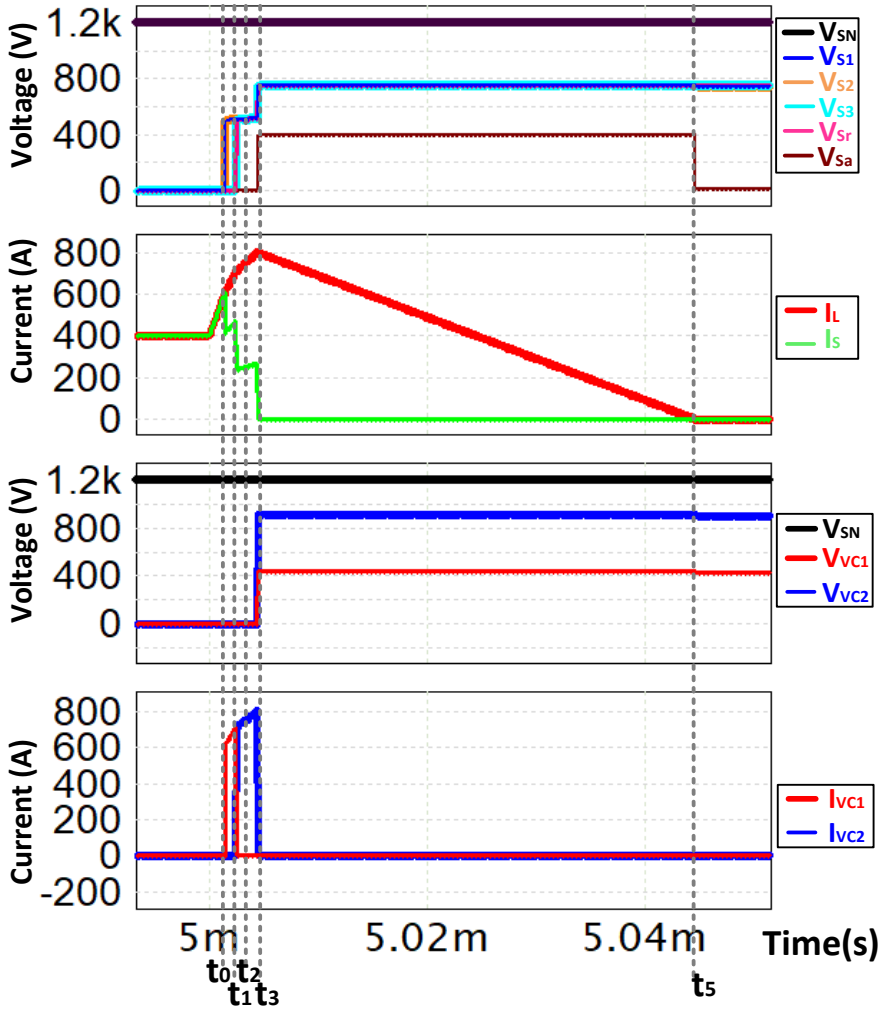
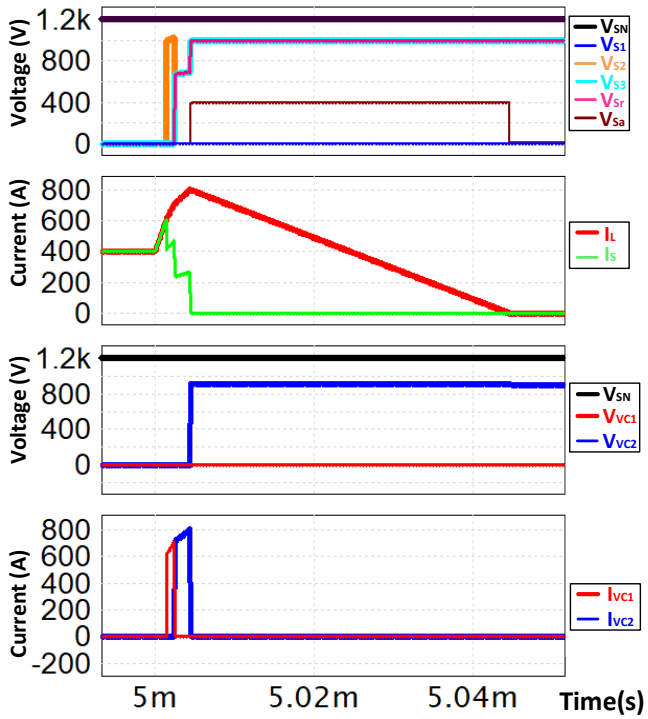


Figure 6. 4 Simulation waveforms of a 4-level FT-MLSSCB during current breaking process.

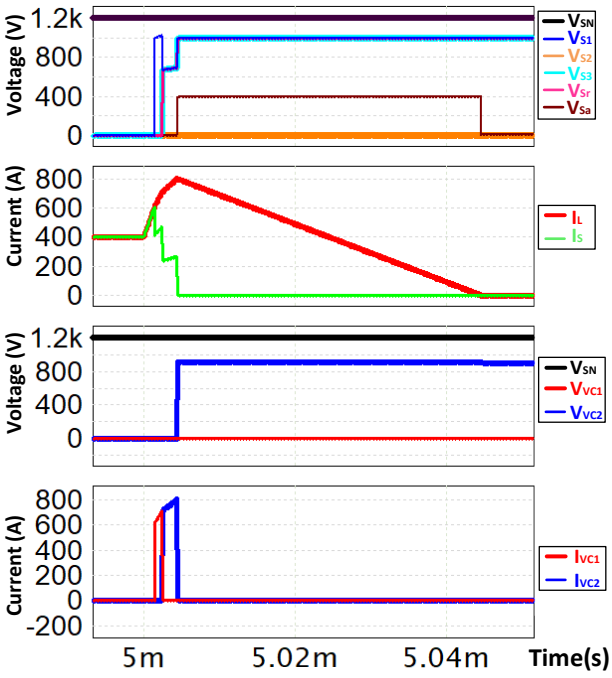
From the operating principle of the proposed FT-MLSSCB, the main switches' voltages are clamped to the corresponding capacitors and step up gradually during the fault interruption. Furthermore, at each step of the breaker's operation, there is always one extra switch opened to share the capacitors' voltage. Therefore, even if one of the

switches fails during the breaker's operation, the voltage on the other switches do not exceed their voltage limits.

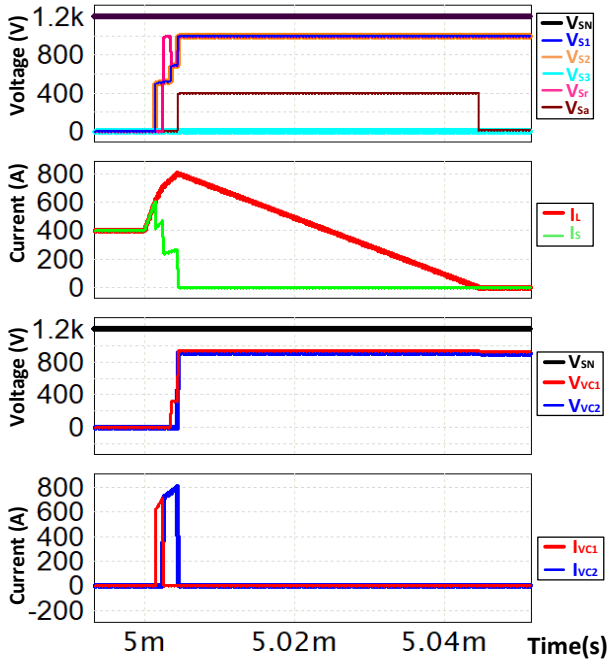
The fault-tolerant capability of FT-MLSSCB has been validated by simulation results of a 4-level FT-MLSSCB in all the cases of one main switch fail as shown in Figure 6.5. From the simulation waveforms, no matter which main switch of the breaker fails to open, the breaker can interrupt the fault current and does not incur overvoltage on the normal devices. Moreover, form the waveform of the source current, I_S, the ultra-fast fault isolation can still be obtained during the fault-tolerant operations.



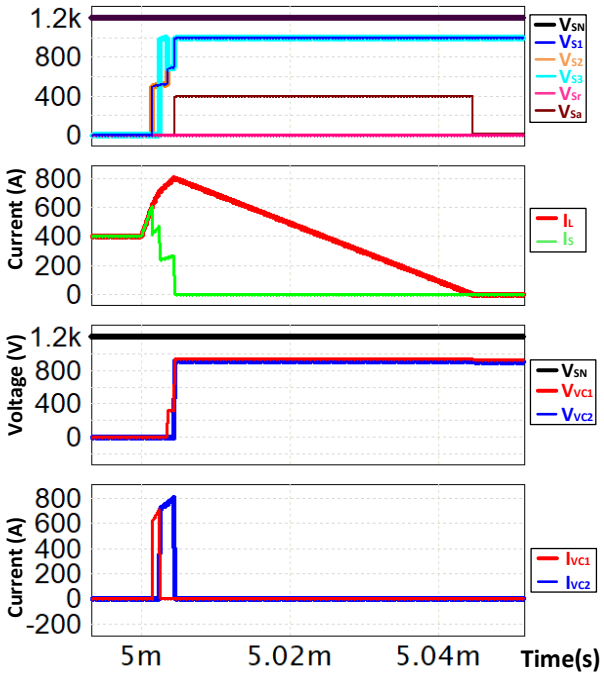
(a)


Voltage (V)
1.2k
800
400
0
VSN
VS1
VS2
VS3
VSr
VSa
Current (A)
800
600
400
200
0
IL
IS
Voltage (V)
1.2k
800
400
0
VSN
VVC1
VVC2
Current (A)
800
600
400
200
0
-200
IVC1
IVC2
5m
5.02m
5.04m
Time(s)

(b)


Voltage (V)
1.2k
800
400
0
VSN
VS1
VS2
VS3
VSr
VSa
Current (A)
800
600
400
200
0
IL
IS
Voltage (V)
1.2k
800
400
0
VSN
VVC1
VVC2
Current (A)
800
600
400
200
0
-200
IVC1
IVC2
5m
5.02m
5.04m
Time(s)

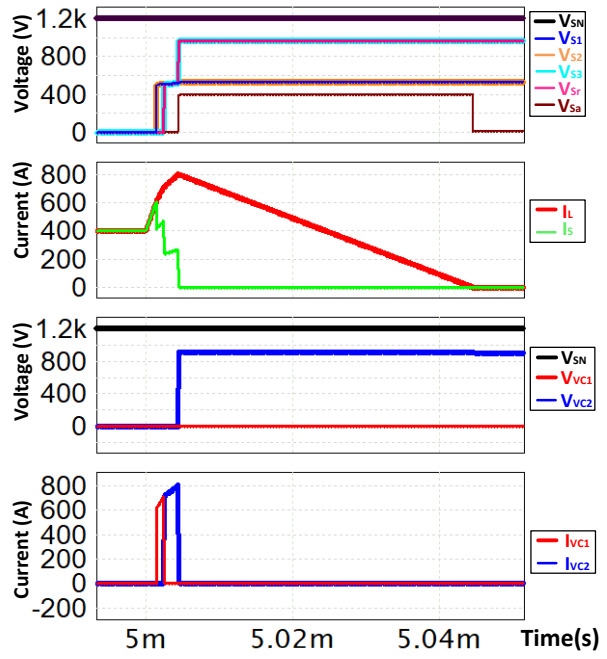
(c)



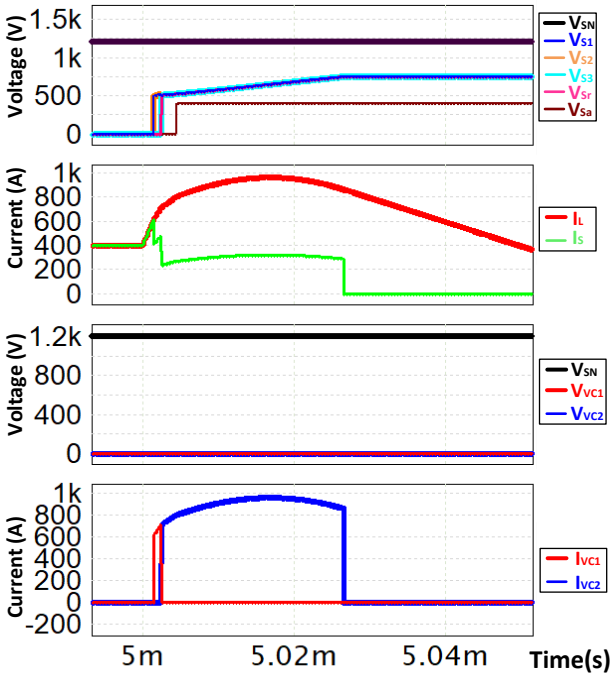
(d)

Figure 6. 5 Simulation results of FT-MLSSCB under fault tolerant operations. (a) S_1 fails. (b) S_2 fails. (c) S_3 fails. (d) S_{r} fails.

From waveforms of the clamping switches, S_{VC1} and S_{VC1}, in Figure 6.4, before the breaker's operation, both the voltage and current of the switches are zero and therefore the switches do not cause any losses under the normal conditions. Besides, since the switches are in dormant mode, their junction temperature can be maintained at room temperature and their installment have very limited impact on the whole breaker's reliability. Additionally, even if any number of the voltage clamping switches fail to open, the low-stream main switch can still interrupt fault current as shown in Figure 6.6. In exchange, the breaker loses its fault-tolerant capability. When the last voltage clamping switch experiences short failure, the breaker losses the fast fault isolation as well. With the diode clamping circuits the same as the MLSSCB, the FT-MLSSCB in Figure 6.7 can



(a)



(b)

Figure 6. 6 Operations of FT-MLSSCB when voltage clamping switches in short failure. (a) S_{VC1} fails. (b) S_{VC1} and S_{VC2} fails.

perform its normal operation regardless the voltage clamping switches are in short failure or open failure as the simulation results shown in Figure 6.8. Consequently, the installments of the voltage clamping switches can bring fault tolerant capability to the MLSSCB without any negative effect on the breaker's reliability.

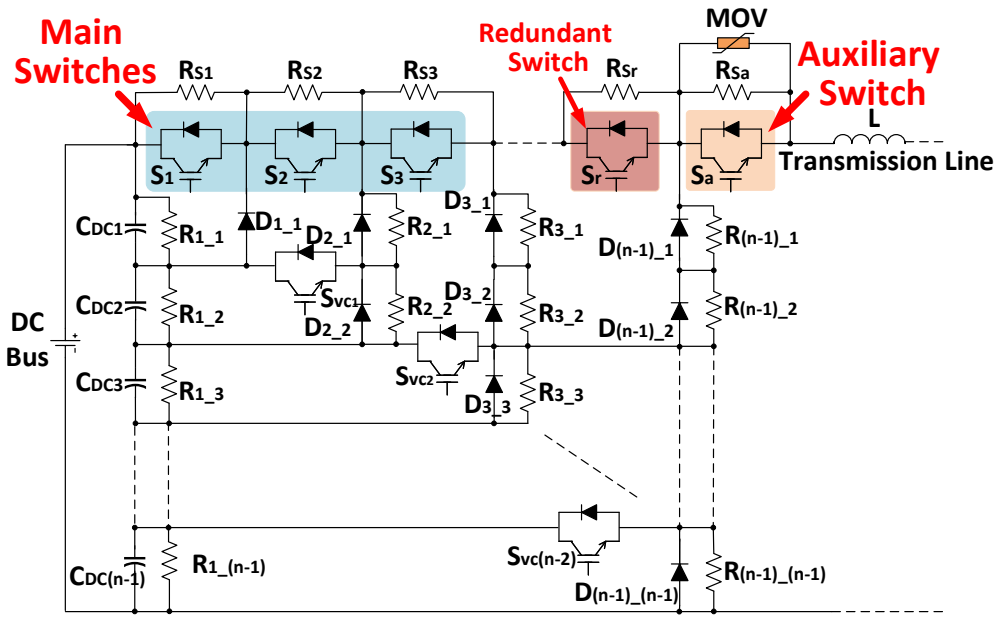
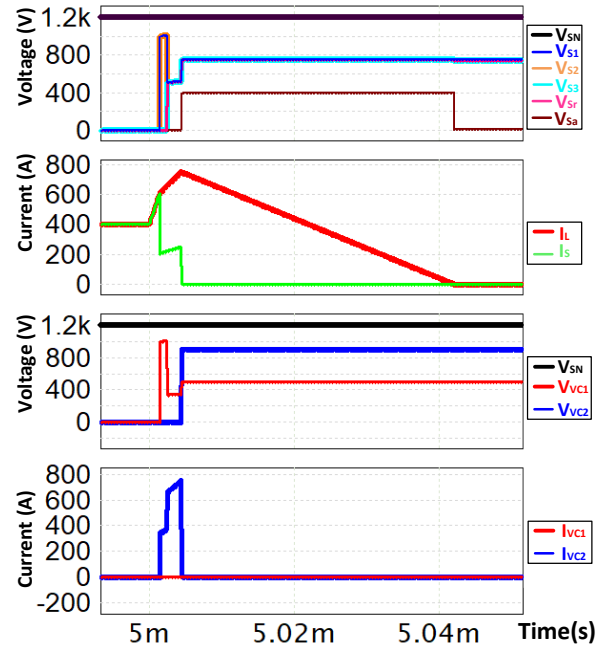
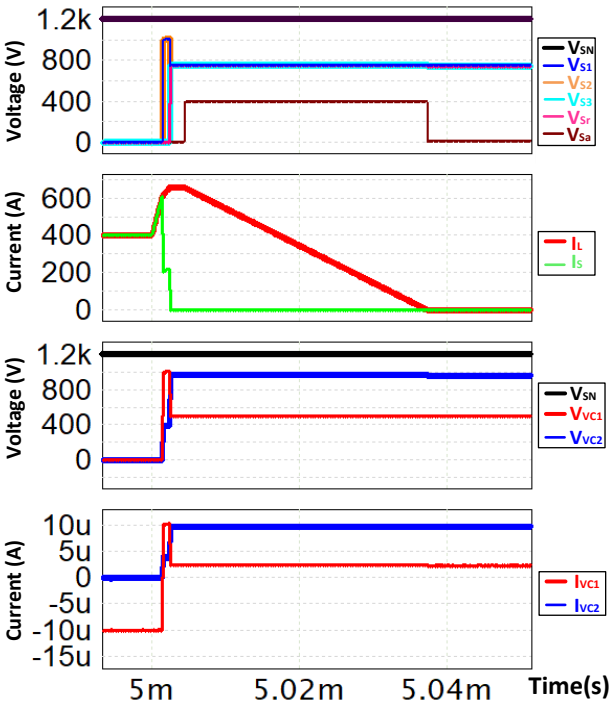


Figure 6. 7 Simplified schematic of n-level FT-MLSSCB with voltage clamping diode.



(a)



(b)

Figure 6. 8 Operations of FT-MLSSCB when voltage clamping switches in open failure. (a) S_{VC1} fails. (b) S_{VC1} and S_{VC2} fails.

6.2 Reliability Analysis of Fault-Tolerant Multilevel Solid-State Circuit Breaker

The reliable fault protection is an important prerequisite for electric power systems [56]. If the fault protection device in a system fails to operate during a fault, the fault may propagate to a wider area and wreak massive power outages. Circuit breakers as the crucial part of the circuit protection system whose reliability has a great impact on the reliable operations of the whole system.

To validate the improvement of FT-MLSSCB on reliability, a comprehensive reliability analysis has been made for the breaker referring to a validated reliability assessment method proposed for multilevel converters [55] [57].

In the reliability analysis, the probability density functions of the breakers' components are assumed in an exponential distribution as

$$f(x) = \lambda e^{-\lambda x} \tag{6.1}$$

where λ is a constant and x is time.

And then, the failure rate of the components in the breakers can be constant as

$$h(x) = \frac{f(x)}{1 - \int_0^x f(x)dx} = \frac{\lambda e^{-\lambda x}}{1 - (-e^{-\lambda x} + 1)} = \lambda \tag{6.2}$$

Thus, the reliability of the components can be simplified as

$$R(x) = 1 - \int_0^x f(x)dx = e^{-\lambda x} \tag{6.3}$$

According to the previous references [58] [59] [60], the standard failure rates of the components in the compared breakers can be set as in TABLE 6 – 1.

TABLE 6 - 1: Switches Used in Breakers' Efficiency Comparison

Components	Failure rates of the components	
	FIT(10^{-9}occ./h)	occ./yr.
IGBT+Gate Driver	$\lambda_1 = 120 + 150$	0.0024
Freewheeling Diodes	$\lambda_2 = 60$	0.00053
Clamping Diodes	$\lambda_3 = 20$	0.000175
Snubber Resistors	$\lambda_4 = 10$	0.000088
Film Capacitors	$\lambda_5 = 2$	0.000018

The standard failure rates in the table are just used for the purpose of reliability comparisons and cannot reflect the hazard rates of the components in the real cases. Besides, as the life of MOVs varies significantly with some random factors, such as the number of the surges and the peak of the fault current, the failure rates of MOVs are not included in the reliability analysis [61] [62]. As the quantity and energy volume of the MOVs in FT-MLSSCB are both lower than those in the conventional SSCB, the assumption does not affect the results of the reliability comparisons among the circuit breakers.

The conventional SSCB can operate only when all the semiconductor switches, gate drivers, snubbers and freewheeling didoes are healthy, so the reliabilities of the SSCB can be expressed as

$$R_{con} = \left(e^{-\lambda_1 t}\right)^{n_s}\left(e^{-\lambda_2 t}\right)^{n_s}\left(e^{-\lambda_4 t}\right)^{n_{sb}} \quad 6.4$$

where n_s stands for the number of the series-connected switches in the breaker and n_{sb} the number of snubber resistors.

For SMLSSCB, all the components need to be healthy including semiconductor switches, gate drivers, snubbers, freewheeling didoes, voltage clamping diodes and voltage dividing capacitors and then the reliability of the breaker can be expressed as

$$R_{MLSSCB} = \left(e^{-\lambda_1 t}\right)^{n_s}\left(e^{-\lambda_2 t}\right)^{n_s}\left(e^{-\lambda_3 t}\right)^{n_d}\left(e^{-\lambda_4 t}\right)^{n_{sb}}\left(e^{-\lambda_5 t}\right)^{n_c} \quad 6.5$$

where n_d is the number of the voltage clamping diodes and n_c is the number of the voltage dividing capacitors.

The reliability of FT-MLSSCB can be mainly divided into two parts. One part is the probability of the breaker to perform the normal operation. Its expression is the same as the reliability of the SMLSSCB. The other part is the probability for the breaker to perform its fault-tolerant operation with one switch fails. The probability can be expressed as

$$R_{FT} = (n_s - 1)\left(1 - e^{-\lambda_1 t}\right)\left(e^{-\lambda_1 t}\right)^{(2n_s-4)}\left(e^{-\lambda_2 t}\right)^{(2n_s-3)}\left(e^{-\lambda_3 t}\right)^{n_d}\left(e^{-\lambda_4 t}\right)^{n_{sb}}\left(e^{-\lambda_5 t}\right)^{n_c}$$
$$+\left(e^{-\lambda_1 t}\right)^{(2n_s-3)}(n_s - 1)\left(1 - e^{-\lambda_2 t}\right)\left(e^{-\lambda_2 t}\right)^{(2n_s-4)}\left(e^{-\lambda_3 t}\right)^{n_d}\left(e^{-\lambda_4 t}\right)^{n_{sb}}\left(e^{-\lambda_5 t}\right)^{n_c} \quad 6.6$$

Eventually, with the tolerance of one switch failure, the reliability of FT-MLSSCB can be expressed as

$$R_{FT-MLSSCB} = R_{FT} + R_{MLSSCB} \quad 6.7$$

The number of the components in the expression are summarized in TABLE 6 - 2. From the table, the number of the switches in all the breakers is increased by one whenever the system voltage is increased by 1kV. MLSSCB has one more auxiliary switch compared to the conventional SSCB. FT-MLSSCB has one more switch than SMLSSCB due to the installment of the redundant switch. The voltage clamping switches

of FT-MLSSCB are not counted because they have no effect on the reliability of the breaker as illustrated in the breaker's operating principles.

TABLE 6 - 2: Quantities of the Components in Conventional SSCB, SMLSSCB and FT-MLSSCB

System Voltage		n	$\mathbf{n_s}$	$\mathbf{n_d}$	$\mathbf{n_{sb}}$	$\mathbf{n_c}$	$\mathbf{n_{MOV}}$
3kV	SSCB	\	3	\	3	\	3
	SMLSSCB	4	4	6	12	3	1
	FT-MLSSCB	4	5	6	12	3	1
mkV	SSCB	\	m	\	m	\	m
	SMLSSCB	m+1	m+1	(m+1)m/2	$(m^2+5m)/2$	m	1
	FT-MLSSCB	m+1	m+2	(m+1)m/2+1	$(m^2+5m)/2$	m	1

From (6.4), (6.5) and (6.7), the reliabilities of the breakers can be attained as shown in Figure 6.9 in an example of 3kV system. From the figure, with the extra components, reliability of MLSSCB is lower than that of the conventional SSCB for the whole time frame. On the other hand, for the FT-MLSSCB, with the fault-tolerant capability, its reliability is improved significantly compared to MLSSCB and can also be higher than the conventional SSCB. As regards the general expressions of the components' quantity in TABLE 6-2, the advantage of the FT-MLSSCB over conventional SSCB on reliability can also been seen in the applications with higher system voltages as shown in Figure 6.10.

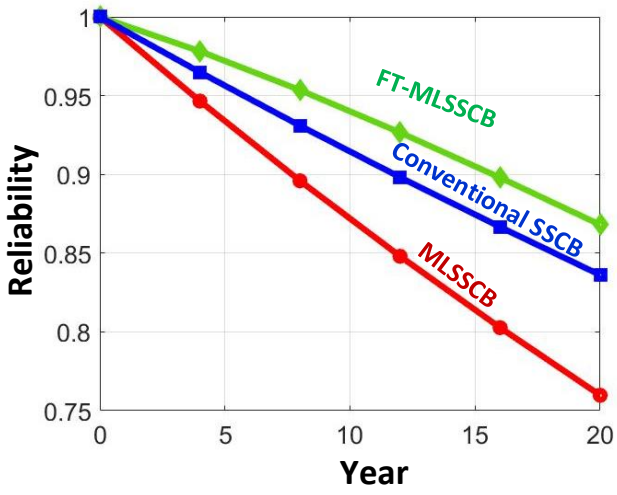


Figure 6. 9 Reliability comparison among conventional SSCB, MLSSCB and FT-MLSSCB in 3kV

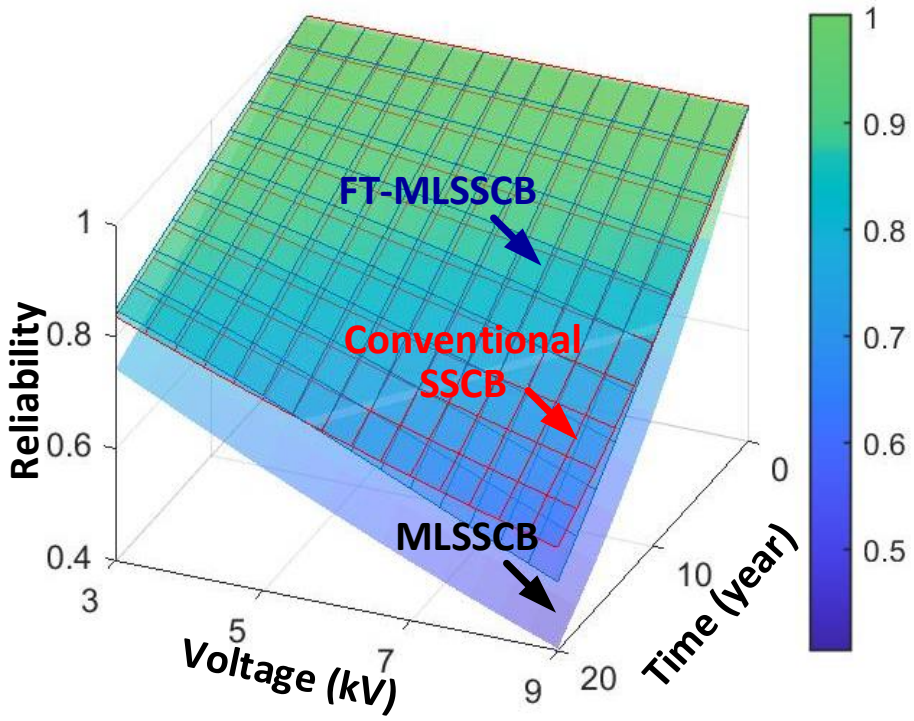


Figure 6. 10 Reliability comparison among conventional SSCB, MLSSCB and FT-MLSSCB in higher voltages.

6.3 Comparisons between the Fault-tolerant Multilevel Solid-State Circuit Breaker and Conventional Solid-Sate Circuit Breaker

6.3.1 Isolation Time

Same as the MLSSCB, the FT-MLSSCB can isolate the fault from the protected sources right after its semiconductor switches turn off as its operating principle shown in Figure 6.5. Therefore, the breaker can achieve an ultra-fast fault isolation speed unrelated to system line inductance and MOV clamping voltage as

$$T_{Iso\_MLSSCB} = T_{off} + (n-1)T_d \tag{6.8}$$

where T_{off} is the turn-off time of the semiconductor switch and T_d is the delay time set between the switches' adjacent trip signals.

The comparison of the isolation time has been made as shown in Figure 6.11 for the conventional SSCB, MLSSCB and FT-MLSSCB in a 3000 V DC system with variable system inductance and 300 A threshold current. The fault detection times of the relays in the breakers assumed to be the same are not included in the comparison. In the conventional SSCB, V_{clamp} is set to be 1.5 times of the system voltage. T_{off} is set at 1 μs that can be met by the commercial SiC MOSFETs [51]. In the SMLSSCB and FT-MLSSCB, T_d is set twice of the T_{off}, namely 2 μs, to maintain the sequentially switching of the switches. From Figure 6.11, it may be observed that the isolation time of the FT-MLSSCB is longer than that of MLSSCB by a unit of delay time due to the use of the redundant switch but is still significantly shorter than that of the conventional SSCB in wide ranges of line inductances. Also, from the figure, the isolation speed of FT-MLSSCB is not affected by the system line inductance.

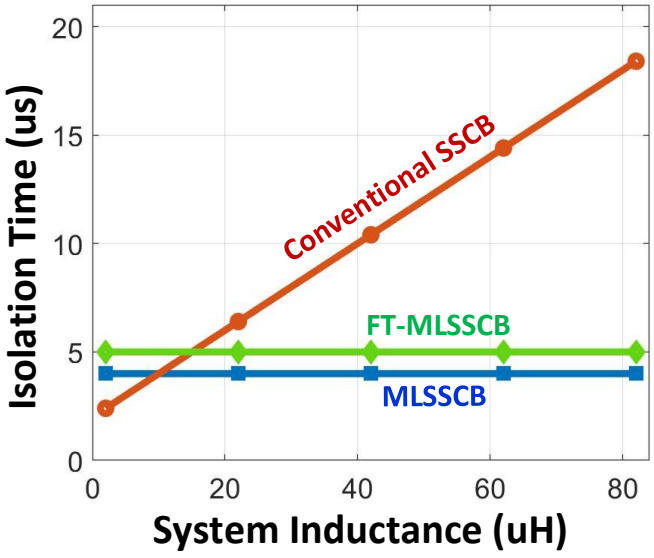


Figure 6. 11 Isolation time comparisons among conventional SSCB, MLSSCB and FT-MLSSCB (3000V, 200A).

6.3.2 Power Efficiency

With much less surge voltage on the semiconductor switches, the voltage rating of the switches in FT-MLSSCB can be lower than that in conventional SSCB. Therefore, even if one extra main switch is used in FT-MLSSCB, its conduction efficiency can still be higher than conventional SSCB. To demonstrate that, the comparisons among the efficiencies of conventional SSCB, FT-MLSSCB and MLSSCB have been made in some typical medium voltage DC systems.

In the comparison, 1.7kV devices are used in the conventional SSCB to sustain the MOVs' clamping voltage of 1.5kV and 1.2kV devices are used in the FT-MLSSCB/SMLSSCB to block the system voltage of 1kV. For all the breakers, the number of semiconductor devices is increased by one whenever the system voltage is

enhanced by 1kV. Besides, for FT-MLSSCB/SMLSSCB, the auxiliary switch is selected the same as the power device to simplify the analysis. In real cases, the voltage rating of the auxiliary switch can be easily set at a lower volage [50]. Two types of SiC MOSFETs from the product series of the same manufacturer are applied to the breakers as in TABLE 6-3.

TABLE 6 - 3: Switches Used in Breakers' Efficiency Comparison

	FT-MLSSCBS/MLSSCB	**Conventional SSCB**
Selected Devices	**C2M0025120D**	**C2M0045170D**
Drain to source voltage (V_{dss})	1200 V	1700 V
Continuous Drain (Id) @ 25°C	90 A	72 A
$R_{ds\ on}$ max @ 50A (Id), 20V (V_{gs})	34 mΩ	70 mΩ

With the $R_{ds\ on}$ of devices shown in TABLE 6 -3, the conduction losses of the SSCBs may be calculated from expression (5.11).

Except for the conduction loss, the power losses caused by the snubber resistors in the breaker is also considered in the comparison. Since the snubbers for the switches do not impair the conduction efficiency of the breaker, they are not included in the analysis. For didoes, the resistance of their snubbers under the worst cases of static voltage unbalance can be determined as (5.1).

As the didoes conduct no current in normal conditions, their junction temperature can be easily maintained at room temperature and the maximum leakage current of the diodes in the 6.9 is set at 100 μA that can be widely met by the commercial 1200 V Si/SiC diodes. For the voltage dividing capacitors, to decouple the effects of the diodes,

their snubbers' resistance can be calculated from (5.12). And then, the losses of the snubbers can be achieved from (5.13). Eventually, the efficiency of the FT-MLSSCB can be attained from (5.14) as summarized in Figure 6.12. The number of the switches used in the circuit breakers are specified in the figure by n_s. From the figure, the efficiency of FT-MLSSCB is lower than that of MLSSCB due to the extra conduction losses caused by the redundant switch. Nevertheless, the efficiency of the FT-MSSCB is still significantly higher than that of the conventional SSCB in the whole range of system voltage in the figure. Thus, the improvement of the efficiency in FT-MLSSCB can be validated. Together with the fault-tolerant capability, the proposed FT-MLSSCB can provide a protection solution that prevails over the conventional SSCB on both efficiency and reliability in the medium voltage DC systems.

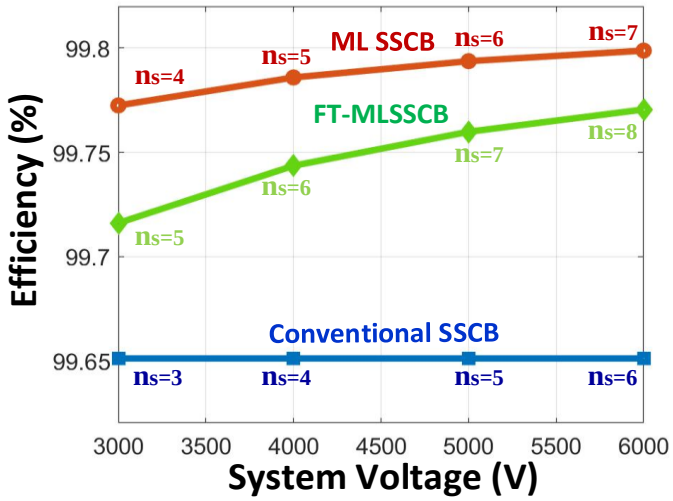


Figure 6. 12 Comparison among the efficiencies of conventional SSCB, SMLSSCB and FT-MLSSCB ($I_L = 50$ A).

6.3.3 Comprehensive Comparison

To summarize, a comprehensive comparison has been made among the Conventional SSCB with series-connected switches, SMLSSCB and FT-MLSSCB as shown in TABLE 6 – 4. From the results, the proposed SMLSSCB and FT-MLSSCB have the capabilities of surgless current limiting, surge voltage suppression and fast fault isolation and can attain higher efficiencies in comparison with the conventional SSCB. Specifically for the FT-MLSSCB, with the fault-tolerant capability, the reliability of the circuit breaker can be competitive with that of the conventional SSCB.

TABLE 6 - 4 Comprehensive Comparison of Conventional SSCB, SMLSSCB and FT-MLSSCB

SSCB Categories	Surgeless Current Limiting	Surge Voltage Suppression	Fast Fault Isolation	Fault Tolerance	Efficiencies	Reliability	Size
Conventional SSCB (Switches in Series)				√	Low	High	Medium
SMLSSCB	√	√	√		High	Medium	Medium
FT-MLSSCB	√	√	√	√	Medium	High	Large

CHAPTER 7: CONCLUSION AND FUTURE WORK

In this dissertation, the dynamic voltage unbalancing issue and surge voltage issue of the conventional Solid-State Circuit Breakers (SSCBs) have been introduced that impairs the breakers' efficiency and can cause their failure. With these issues, the adoption of SSCBs is hindered, especially in the medium voltage DC applications.

To deal with the dynamic voltage unbalance issue, a Multilevel Solid-State Circuit Breaker (MLSSCB) has been proposed that can maintain the dynamic voltage balancing among its series-connected switches utilizing the diode clamped circuit. Compared to the conventional modular SSCB having MOV in parallel with each of the series-connected switches, the MLSSCB incurs much less surge voltage on its switches. After that, two types of surgeless SSCBs, namely Surge Voltage Free Solid-State Circuit Breaker (SVFSSCB) and Ground Clamped Solid-State Circuit Breaker (GCSSCB), have been proposed. The SVFSSCB actively grounds the sources during the fault and can acquire a faster isolation speed with nearly zero surge voltage on its semiconductor switch. Nonetheless, due to the large peak current drawn from the DC source during the breaker's operation, the application of the breaker is limited to the systems having a certain needs on current limiting inductance. The GCSSCB, on the other hand, averts the defects of the SVFSSCB and can deliver an even faster isolation speed. Although an extra auxiliary switch is used in the breaker, the voltage rating of the switch can be easily set at a low voltage as the isolation speed of the breaker is unrelated to the MOV's clamping voltage. Besides, in GCSSCB, the main switch is free from surge voltage and its voltage rating can be set according to the system voltage. Next, a Surgeless Multilevel

Solid-State Circuit Breaker (SMLSSCB) has been proposed by integrating the topologies of GCSSCB and MLSSCB. Same as the GCSSCB, the SMLSSCB can effectively suppress the surge voltage on its semiconductor switches and achieve faster isolation speed along with higher conducting efficiency compared to conventional SSCBs. Meanwhile, like MLSSCB, the dynamic voltage unbalance among the series-connected switches in the breaker can be averted. At last, to compensate the lower reliability of SMLSSCB caused by the larger number of its components, a Fault-tolerant Multilevel Solid-State Circuit Breaker (FT-MLSSCB) has been proposed with a reliability prior to the conventional SSCB utilizing its fault-tolerant capability and retains all the advantages of MLSSCB on efficiency, isolation speed and dynamic voltage balancing.

The simulation/experiment results and design considerations of the proposed circuit breakers have been presented to validate the technical feasibility and practical use of the proposed circuit breakers. Also, the comparisons among the proposed circuit breakers and the conventional SSCB have been made to delineate the advantages of the proposed SSCB over the conventional one in the different applications.

Further investigations can be made for the proposed Surgeless Multilevel Solid-State Circuit Breaker to improve its performance and expand its applications. At first, in the proposed topology, basic resistive snubbers are used to maintain the static voltage balance among the series-connected diodes and causes extra losses. In the high voltage applications, the losses may affect the breaker's advantages on efficiency. To expand the applications of the SMLSSCB to higher voltage ratings, more advanced snubber circuits with active switches could be used to address this issue. Second, when the SMLSSCB

closes, the voltage across the transmission line steps up gradually, which naturally slows down the rising rate of the line current. This property can be potentially applied to the system soft start and replace the current soft starting technology of SSCB that requires high frequency switching. Third, the fault-tolerant configuration of SMLSSCB can be further developed to allow the breaker tolerating the failures on multiple switches and reach higher reliability. At last, the performances of the proposed circuit breakers need to be further studied in the specific applications to figure out the applications matching best the characteristics of the circuit breakers.

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