DESIGN AND ANALYSIS OF ACTIVE ISOLATION IN POWER CONVERTER SYSTEMS

by

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ABSTRACT

CLINT WADE HALSTED. Design and analysis of active isolation in power converter systems. (Under the direction of DR. MADHAV MANJREKAR)

This dissertation presents a new class of power converter topologies that realize galvanic isolation by utilizing active transistor devices instead of conventional transformers. The power converters employ standard switch-mode topologies but isolate the ground connections with the addition of active switches on the ground side of the power path. Compared to transformer isolation, the Active Isolated (AI) converters have reduced size and cost with increased efficiency. A generalized approach is given that is used to create thirty-six new active isolated topologies based on the following basic converters: buck, boost, buck-boost, Cuk, SEPIC, and Zeta. Of these, the buck-boost and boost-buck are determined optimum topologies since they achieve pulsating and non-pulsating galvanic isolated conversion with the fewest component count, respectively. The two optimum converters are modeled mathematically and various prototypes are developed that confirms proper galvanic isolation. The concept of unipolar and bipolar isolation is explored and it is found that in many applications, including the application chosen for this work, that unipolar isolation is adequate to provide proper operation and safety for the user. Common-mode transient and steady-state models of the converters are developed and correlated to experimental results. The two optimum converters are used in two applications: PV microinverter and offline AC-DC power supply with fault protection.

DEDICATION

This dissertation is dedicated to my wife, Kristen Elizabeth (Martell) Halsted. Without her love, dedication, and support this work would not have been possible.

ACKNOWLEDGEMENTS

I would like to acknowledge my Ph.D. adviser, Dr. Madhav D. Manjrekar, who encouraged me to explore my own ideas which lead to the development of the concepts in this dissertation. Also, I would like to thank my co-adviser, Dr. Babak Parkhideh, and the other members of my Ph.D. committee including: Dr. Robert Cox, Dr. Brigid Mullany, and former Ph.D. committee member Dr. Umit Cali for their commitment.

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CHAPTER 1: INTRODUCTION

This chapter presents a brief introduction and organization of the dissertation. Benefits of galvanic isolation is presented in Section 1.1. Motivation for the research is presented in Section 1.2. Section 1.3 presents the organization of the dissertation.

1.1 Benefits of Galvanic Isolation

Since 1892, transformers have been used for both voltage ratio transformation and galvanic isolation in the United States. The initial use of transformers in electric power distribution was to step up/down the ac voltage. The added benefit in the use of transformers is achieving galvanic (or electrical) isolation. Galvanic isolation provides for improved safety, ability to shift output voltages, and elimination of common-mode leakage currents in electrical systems and living creatures [1]. As seen in Figure 1.1, the output of an isolation transformer can be allowed to float so that a human touching the high- or low-side rail will not receive an electrical shock since the output secondary side will float due to high-resistance insulation between primary and secondary side of the windings.

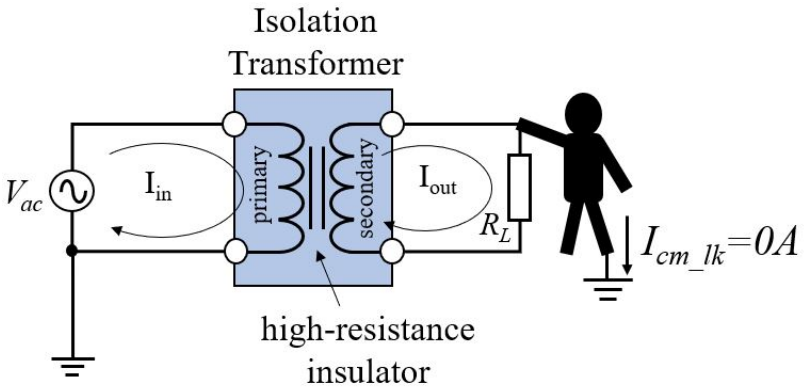


Figure 1.1: Float for safety to prevent electrical shock

Another benefit of galvanic isolation is safety grounding of electrical conductors and electrical equipment chassis. As shown in Figure 1.2, the secondary-side isolation transformer is grounded at the midpoint of the 240V ac output which provides split-phase 120V to the residential customer. The neutral midpoint is grounded at the pole. The neutral conductor is connected to a grounding bar inside the main breaker box and connected to ground at the residence. The neutral grounded connection is distributed to the loads which require chassis grounding of the electrical equipment. This is only possible because of galvanic isolation due to the high electrical resistance between primary- and secondary-side of the isolation transformer. The grounding of the electrical neutral conductors and chassis prevents electrical shock to humans and causes a safety breaker to trip in the event of short from hot conductor to neutral or chassis.

Galvanic isolation is also used to shift the output voltage on the secondary side of the isolation transformer. As shown in Figure 1.3. the output voltage on the secondary side is 24V differential, but the load is split in two and grounded in-between. The creates a dual supply of $\pm$12V.

In all the examples above the benefits obtained are due to decoupling of the common-mode voltages and currents in the systems. As shown in Figure 1.4, the high electrical resistance betwen the primary- and secondary-side of the transformer breaks the common-mode current path in the system. In some systems, high-frequency transformers are used to break this common-mode leakage current path which allows the system to meet electrical standards and specifications on output dc and leakage currents [2, 3].

1.2 Motivation

There is motivation in power conversion to transition from transformer isolation (magnetic coupling) to electronic active isolation (semiconductor switch isolation). The main motivation for removing the transformer is to simply remove the extra com-

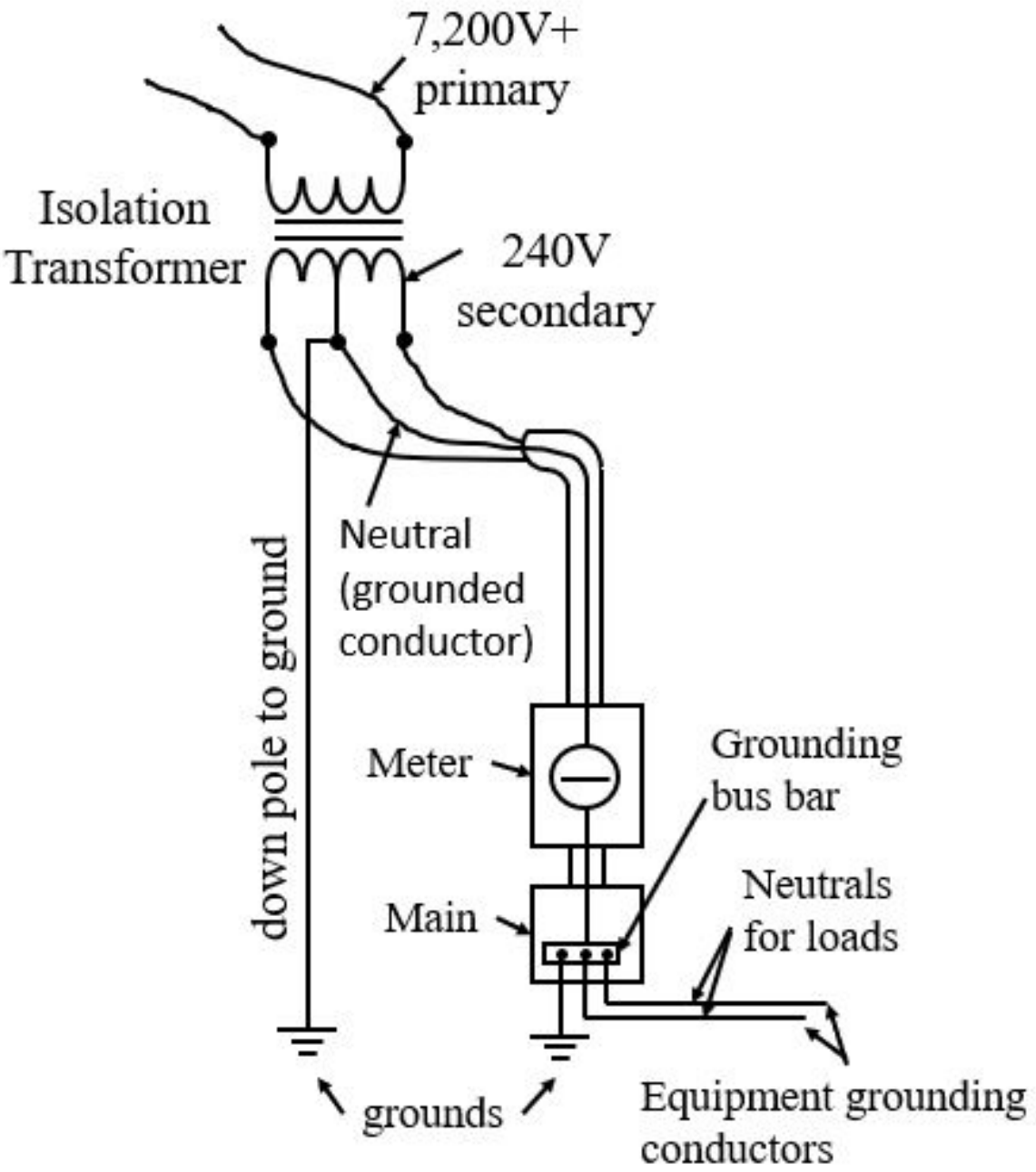


Figure 1.2: Float for safety to ground neutral wire and equipment chassis

ponent, that is, the transformer. For example, a non-isolated buck-boost converter contains two switch devices, an inductor, and an output filter capacitor. To isolate this converter, the inductor is replaced by a transformer, as shown in Figure 2.2. The transformer is more complicated than an inductor, and thus is more expensive to manufacture and larger since it must contain two separate windings. Due to the

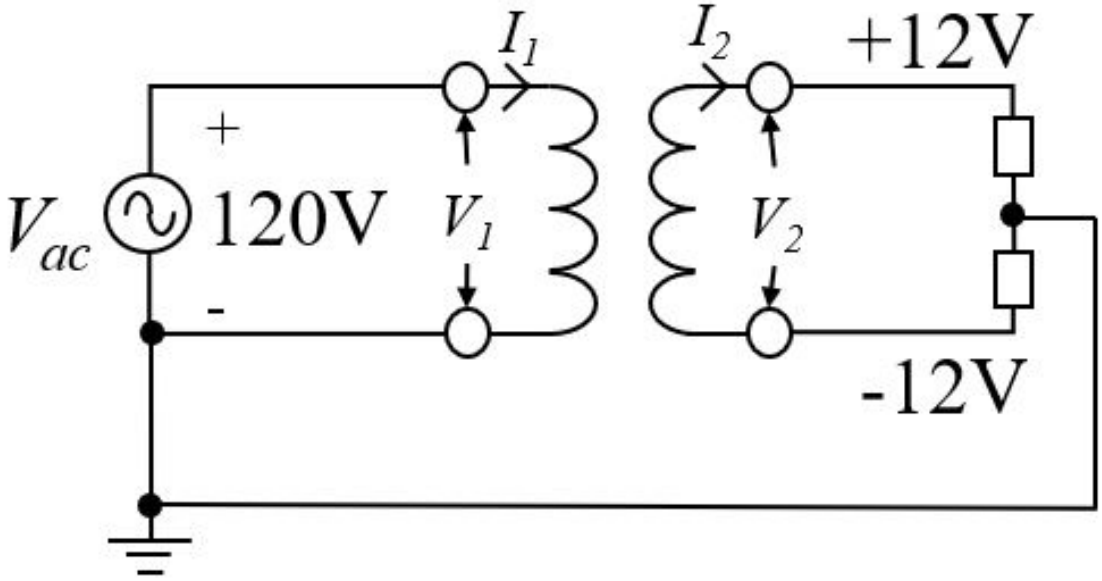


Figure 1.3: Float to shift output voltage

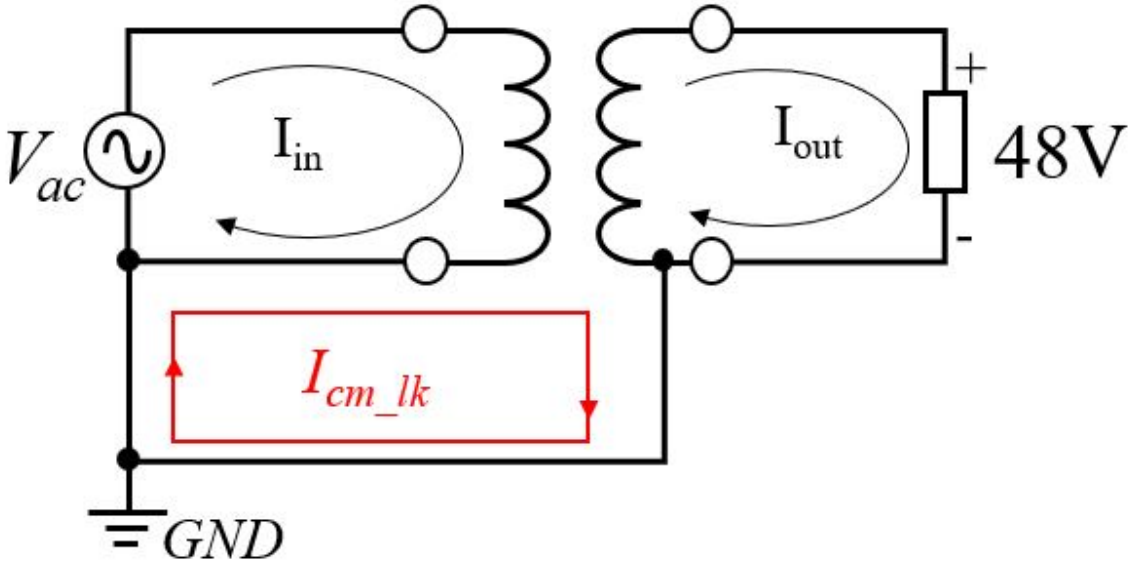


Figure 1.4: Elimination of common-mode leakage current

two separate windings, the wires in the transformer must be made with smaller gauge to fit in the same size as an equivalent inductor. Thus, removing the requirement for containing a transformer is a sufficient condition for reducing the converter size, volume, and weight, and increasing the efficiency. This research seaks to answer the

question, "can we transform a traditional non-isolated power converter to an isolated one without adding any new type of component." (The "new" component refered to here is the transformer since it does not exist in the non-isolated buck-boost converter circuit.) It is allowed that we add additional existing componets, i.e., more switch devices and control. It is not the goal of this research to measure the magnitude of the difference of the replacement since it has already been shown that transformer isolated 250W power converters vs. non-isolated ones are 1) 6% less efficient (98% vs. 92%), 2) 75% more heat dissipative, 3) 50% more expensive, and 4) 65% larger [4].

Transformers serve a two-fold purpose in power converters: 1) DC voltage (galvanic) isolation, 2) and step-up/down functionality. It is not the goal of the paper to investigate the loss of step-up/down capability. However, DC/DC converters already have the ability of step-up/down voltage ratios. Possible cascading of converters can likely achieve a similar step-up/down ratio, but will not be investigated in this research. It is, however, the goal to explore the differences of the provided galvanic isolation between transformer isolation and active isolation. One consequence of active isolation is high common-mode (leakage) current due to Coss parasitic switch capacitance. Another consequence is lack of fault protection from primary to secondary side of the converter. Both these consequences will be explored in this research. Also, it is desired to investigate the circuit topologies that can be actively isolated and those that are optimal and the requirements and limitations to active isolation in this regard.

1.3 Organization of Dissertation

This section presents an overview of the organization of the remainder of the dissertation. Chapter 2, entitled "Literature Review", presents an introduction (section 2.1), a review of safety (section 2.2), a review of the relevant literature for conventional isolation (section 2.3), a review of existing transformerless isolated converter technolo-

gies (section 2.4), and a review of existing research in transformerless PV inverters and common mode current comparisons (section 2.5). Chapter 3, entitled "Active Isolation Topologies", provides an introduction (section 3.1), operating principles and comparisons (section 3.2), a generalized approach to active isolation (section 3.3), and an analysis of thirty-six dual cascade combinations of basic converter topologies (section 3.4). Chapter 4, entitled "Modeling and Analysis", presents an introduction (section 4.1), modeling of the active isolated boost-buck converter (section 4.2), modeling of the active isolated buck-boost converter (section 4.3), and experimental results (section 4.4). In chapter 5 applications of active isolation are presented. An introduction is given (section 5.1), an active isolated photovoltaic microinverter presented (section 5.2), and an AC/DC power adapter with fault protection given (section 5.3) with experimental results included for each application in the corresponding sections. Conclusions and Future Work are discussed in chapter 6.

CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

This section contains a scholarly literature review on safe levels of currents for humans (section 2.2), of conventional isolation methods (section 2.3), of tranformerless isolation approaches (section 2.4), and of transformerless PV inverter common-mode current solutions and issues (section 2.5). This section begins with a review of affects of small currents on living creatures which is the basis of the need for fault isolation in converters. Next, conventional isolation methods are discussed with a focus on the most popular approaches and include only transformer-based isolated converters using high-frequency transformer integrated inside the converters, since this is the most widely adopted approach in modern design practices. Transformerless isolation approaches discussed focus on capacitor-based isolation approaches and switch-based isolation attempts (Semiconductor Galvanic Isolation) for switched-capacitor topologies, since they are designed for medium to high power applications from few Watts to kilo Watt range. Relatively speaking, there has been little research performed on this topic in this power range. No research publications were found by the author concerning switch-based isolation using conventional volt-second balanced converters such as isolated buck, boost, buck-boost, Cuk, Zeta, SEPIC, etc. All prior research has focused either on capacitor-based isolation or switch-based isolation using switched-capacitor converters. These transformerless converter topologies will be reviewed in detail in this section. It is important to note that many transformerless converter topologies exist in photovoltaic (PV) inverter research, however, the input PV voltage is allowed to float, which means isolation is not needed. It is not only tranformerless converter technology that we are interested in here, but tranformer-

less and isolated converter technologies. The main application chosen to showcase this new technology (active isolation) is PV microinverter applications. A review of transformerless inverter issues and topologies are discussed. Issues of common-mode leakage current and modulations methods used to reduce this current are discussed. Finally, grid standards and PV inverter topologies for reducing this common-mode leakage current are discussed.

2.2 Safety

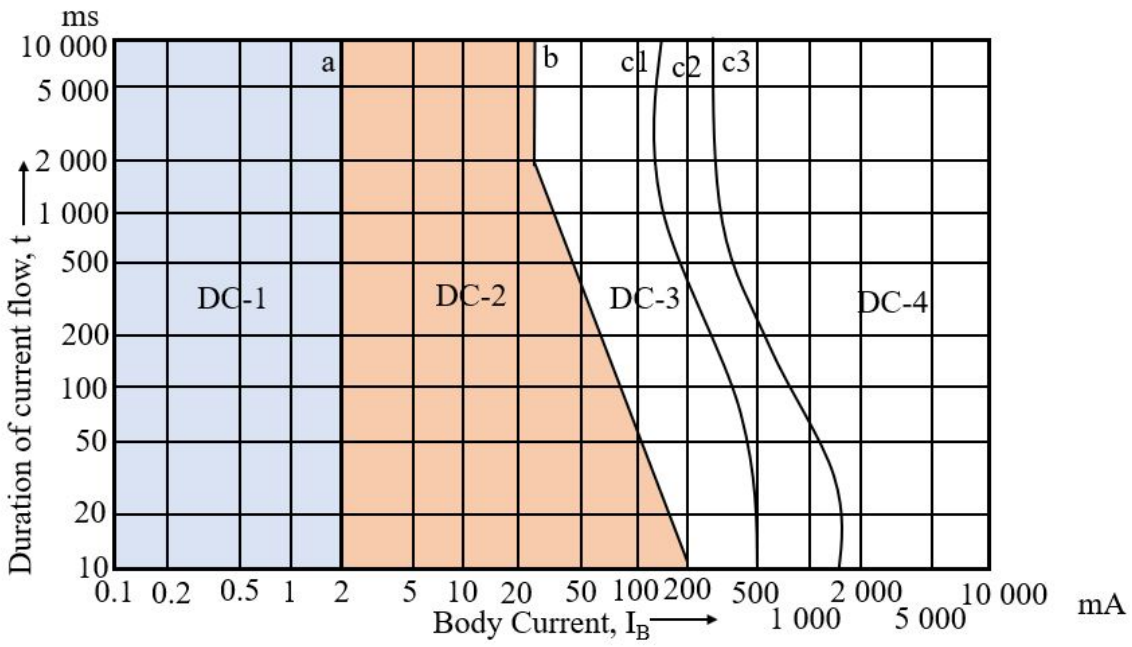


Figure 2.1: Conventional time/current zones of effects of DC current on persons for a longitudinal upward current path (see Table 2.1) [1]

Studies have been conduction to determine the safe level of current in humans and livestock. According to [1], a current of 30mA through the human body for 400ms causes muscle contractions with reversable effects, see Figure 2.1 and Table 2.1 [1]. Even higher levels of current eventualy lead to irreversable effects for humans. So, it is importaint to limit or mitigate this common-mode current. Various standards limit this common-mode current in a variety of applicatios (including photovoltaic inverters, information technology, and electronic vehicle charging equipment) [2, 3, 5,

Table 2.1: Time/current zones for DC for hand to feet pathway

Zones	Boundaries	Physiological effects
DC-1	Up to 2mA curve a	slight pricking sensation
DC-2	2mA up to curve b	involuntary muscular contractions
DC-3	curve b and above	strong invol. muscular contractions
DC-4	above curve c1	cardio arrest, burns, cellular damage

6, 7, 8, 9]. The use of transformerless converter topologies results in higher overall efficiency, decreased size, and lower cost compared with transformer-isolated types[10]. However, it has been shown that the use of non-isolated converters causes unwanted common-mode leakage currents to flow through the converter and onto the ground system[11, 12, 13]. If not limited, these common-mode currents can reduce system efficiency and trip protection devices such as Ground Fault Circuit Interrupter (GFCI) and Residential Current Devices (RCD) that are designed to detect ground fault conditions that protect humans and equipment.

2.3 Conventional Isolation

Traditional methods to achieve voltage (galvanic) isolation include seven distinct approaches: 1) magnetic isolation (transformers), 2) capacitor isolation, 3) relay, 4) optical isolation (opto-isolators), 5) hall effect, 6) magnetoresistance, and 7) semiconductor galvanic isolation (SGI). The approach proposed in this research is a type of SGI called "active isolation (AI)." Both SGI and AI -based isolation are a type of switch-based isolation.

Before continuing too far into the literature review, it is important to review some grammar. It is common practice in some engineering disciplines (specifically "power electronics and power systems") to refer to transformer isolation as galvanic isolation. However, galvanic isolation does not refer to transformer isolation or magnetic isolation or any particular way of achieving isolation. The word "galvanic" simply means voltage. The term originates from the discoverer of electricity Dr. Luigi Galvani who discovered that voltaic electricity and animal electricity are the same. The word

"voltaic", at the time, referred to the type of voltage produced by the invention of Alessandro Volta. In particular, the voltaic pile. Although transformers can be used to achieve voltage (galvanic) isolation, the other six previously mentioned devices can also achieve the same effect. The first three mentioned (transformers, capacitors, and relays) are able to achieve high power isolation, while the latter devices/methods normally are used in low power isolation.

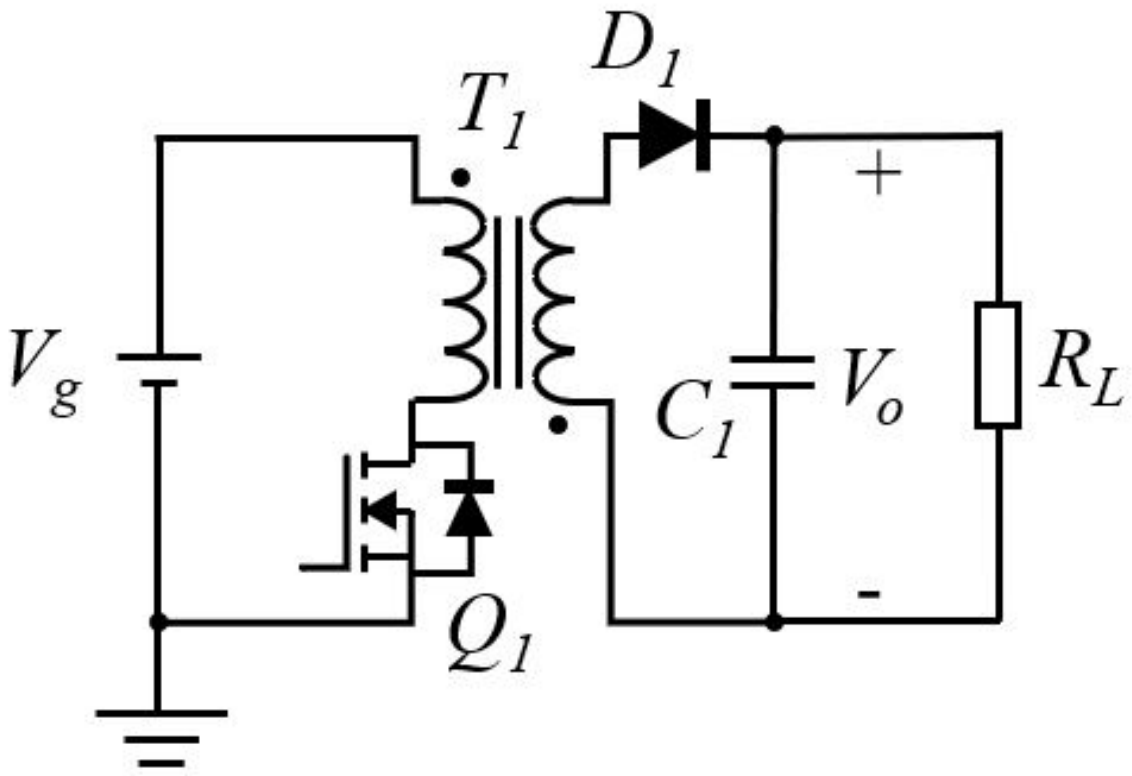


Figure 2.2: Flyback converter

The traditional approach to achieve voltage (galvanic) isolation in power conversion uses isolation transformers which exploit the properties of magnetic coupling between windings. To reduce the required size of the transformer, high frequency (HF) switch-mode power supplies are used. The flyback converter shown in Figure 2.2 is an isolated buck-boost topology. This converter topology is created by replacing the inductor in a buck-boost converter with a transformer and rearanging the components. The

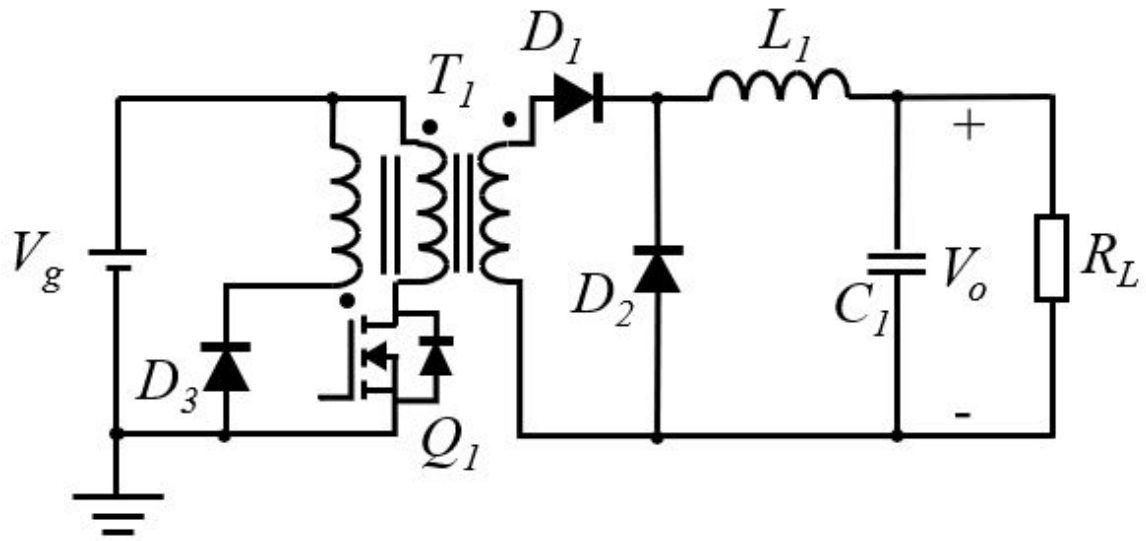


Figure 2.3: Forward converter

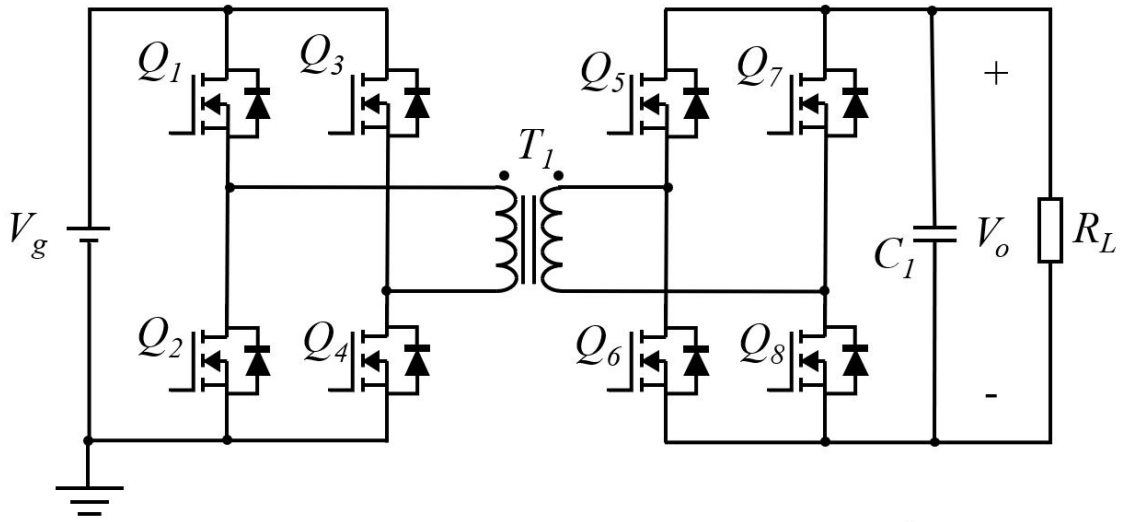


Figure 2.4: Dual-Active Bridge (DAB) converter

forward converter shown in Figure 2.3 is an isolated buck topology. The Dual-Active Bridge (DAB) shown in Figure 2.4 is an isolated back-to-back DC-to-AC and AC-to-DC (buck cascaded with boost) topology [14]. The LLC (inductor-inductor-capacitor) series resonant converter shown in Figure 2.5 is an isolated resonant buck converter cascaded with a boost converter [15].

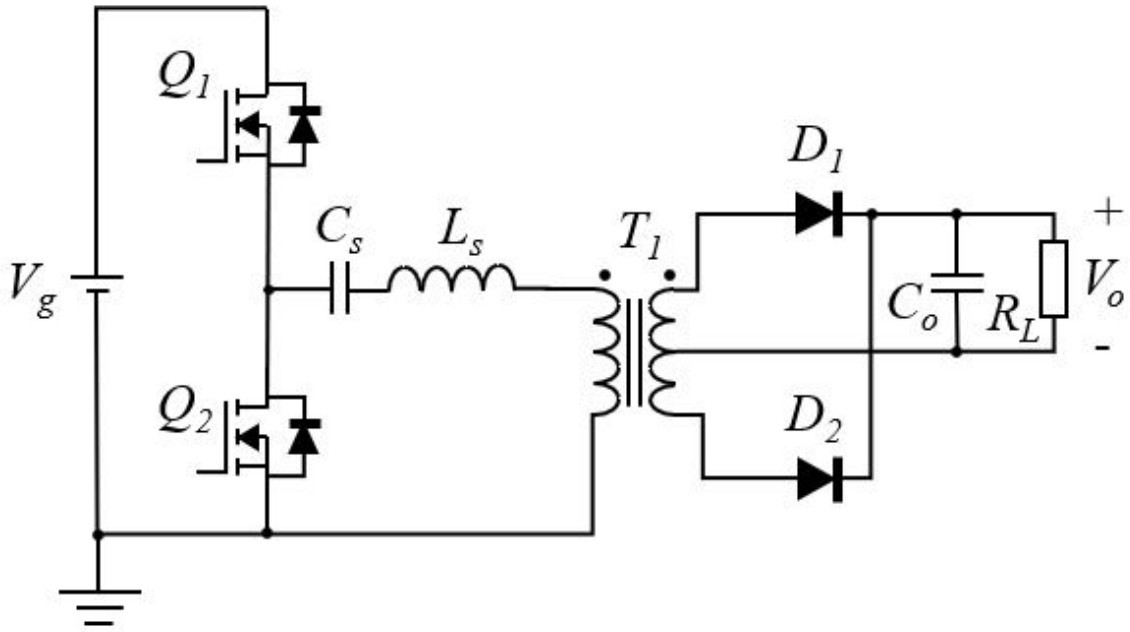


Figure 2.5: LLC series resonant converter

2.4 Transformerless Isolation

One method to achive transformerless isolation is through the use of dual series coupling capacitors in the power path. This solution was used in a 85W AC/AC Cold Cathode Florescent Lamp (CCFL) liquid Crystal Display (LCD) TV backlight system. The principle is to control the power path impedance by blocking the low-frequency part of the touch current (TC) and allowing the high-frequency power to flow to the output. The disadvantages given in the paper include the following: 1) structure is more complicated than transformer isolation and 2) modification is always needed for different applications. The author suggested the research could be extended to DC/DC converter applications, but no experimental data given [16].

A similar approach to capacitor isolation is used in primary-side controller and H-bridge driver for isolated power-supply circuits by Maxim Integrated. The integrated circuit with integral FETs provide up to 3W of power to the primary winding of a transformer. In the application note, the device drives a pair of capacitors that

substitute for the transformer in providing isolation and also providing power transfer to the load [17].

A 60W capacitor isolated converter was later developed for Light Emitting Diode (LED) lighting applications, as shown in Figure 2.6 [18]. The solution is based on a series resonant converter (SRC). The capacitor is used for both isolation and current balancing the two-output rectifier structure. As shown, the resonant capacitor and inductor are duplicated, then the transformer is removed since it is no longer needed for isolation. The capacitors Cr1 and Cr2 act as resonant capacitors, isolation capacitors, and current-balancing capaictors for both outputs. The circuit operates just higher than the resonant frequency as traditional SRC to accomplish zero-voltage switching (ZVS) at primary-side of the converter. Optionally, a common-mode (CM) choke can be added to help reduce the leakage current if the output side is connected to earth ground for class I equipment [18].

Disadvantages of capacitor isolated supplies include 1) the inability of the converter to supply DC current at the output, 2) large current spikes when the DC potential difference across the isolation barrier changes, 3) equivalent series resistance (ESR) losses in the coupling capacitors since they are in the power flow path, 4) high required coupling capacitor voltage ratings required, and 5) non-polarized capacitors required. Capacitive isolation approaches require adding an additional type of component that is not in the original non-isolated converter since the added capacitor is not similar to the already existing capacitors in the non-isolated version. For example, in a capacitor isolated converter with 25V output, the required output capacitance voltage rating is 50V (assuming a two times safety margin). However, to achieve 600V of DC voltage (galvanic) isolation, an additional 1,200V capacitor would need to be selected. It is obvious here that the 1,200V capacitor is an additional component that needs to be added that is not of similar type to the capacitor in the original bill-of-materials (BOM). The goal of the proposed active isolation is to eliminate any additional type

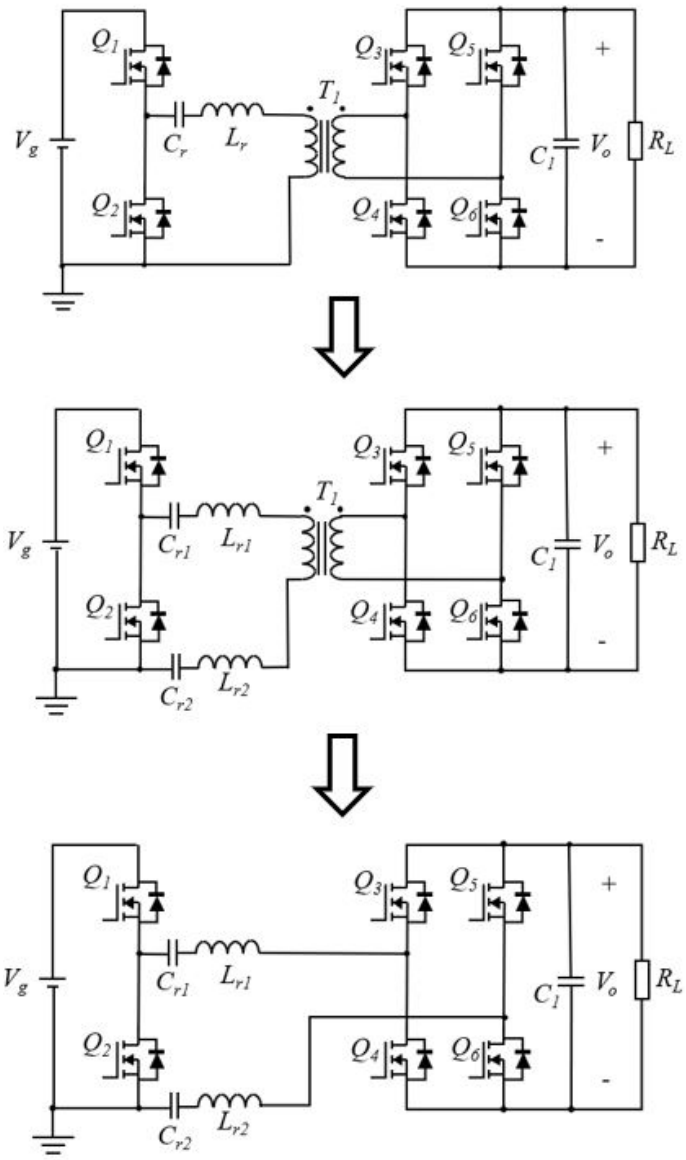


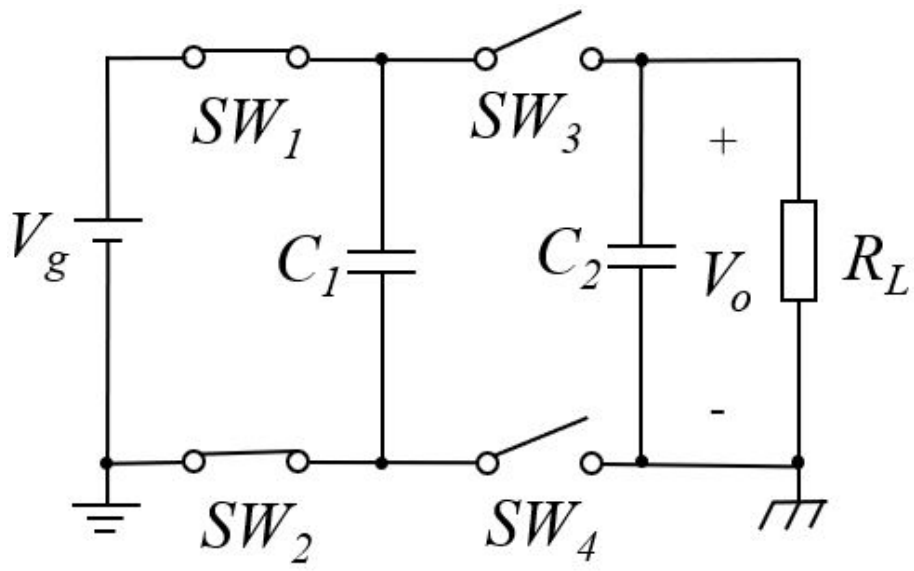
Figure 2.6: Derivation of approach for capacitor isolation

of component from the BOM. For example, adding another MOSFET to the BOM is allowed if it is of similar voltage and current rating as the existing MOSFET devices used in the original non-isolated BOM.

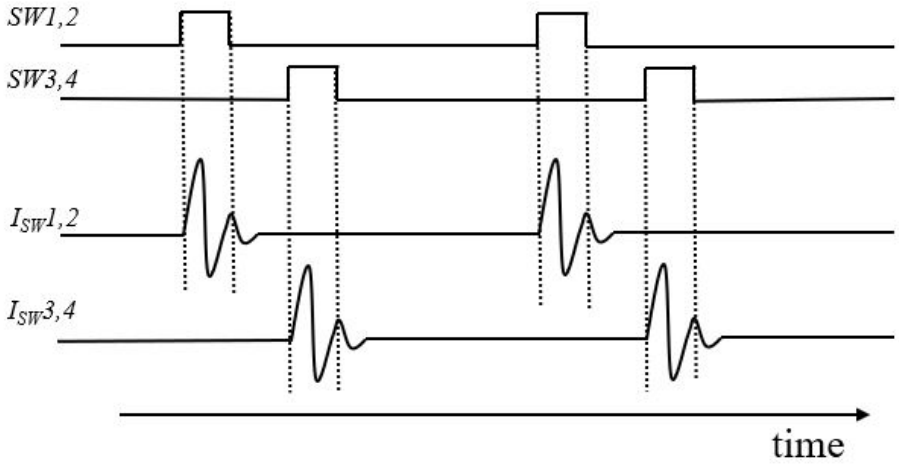
The use of power switch (active) devices to isolate a power converter was first introduced in the form of a cascaded Switched-Capacitor (SC) buck converter, as shown in Figure 2.7 [19]. The converter was designed for application in aerospace indus-

try application where use of a transformer-isolated converter would pose a reliability concern due to possibility of single-point failure of the converter. This failure would result in the loss of multiple sensor outputs. For the isolated SC converter to function properly, the circuit shown in Figure 2.7 must be cascaded with another standard SC topology, i.e., Vg is generated from another SC converter. The waveforms for the circuit, Figure 2.7b, show capacitor in-rush current coincident with switch transitions. This current is only limited by MOSFET on-resistance and capacitor ESR. The dead-time between the switch transitions ensure voltage (galvanic) isolation between input and output. The resonant character of the signals shown is due the capacitors C1, C2 and circuit parasitic inductance. The peak value of this current is a major liming factor in the isolated SC design since switch devices must be rated a peak current handling capabilities. In addition, this in-rush current would contribute heavily to magnetic field induced electromagnetic interference (EMI). The inrush current must be managed by making C1 and C2 small and the switch resistance high so in-rush current is limited. However, high switch resistance reduces efficiency and output power. Small capacitor size also reduces output power capabilities. Experimental measurements of the circuit shown with 0.5V 50Hz test signal connected between input and output ground show that ground noise across an added 10k Ohm ground resistance is reduced 36dB compared to a non-isolated version of the SC converter.

Using the same basic SC cell as in [19], but modified to use Zero-Current Switching (ZCS) resonance, a converter was developed for a 400V 400W AC/DC application, as shown in Figure 2.8a [20]. To achieve high efficiency (>95%) ZCS is used as shown Figure 2.8b. The circuit does not use magnetic components but instead capacitors to transfer energy from output to input and thus has the potential for high power density. However, due to the switching action of the lateral MOSFET devices that charge output parasitic MOSFET capacitance each switching cycle, the circuit topology internally generates common-mode (leakage) current two times per switching



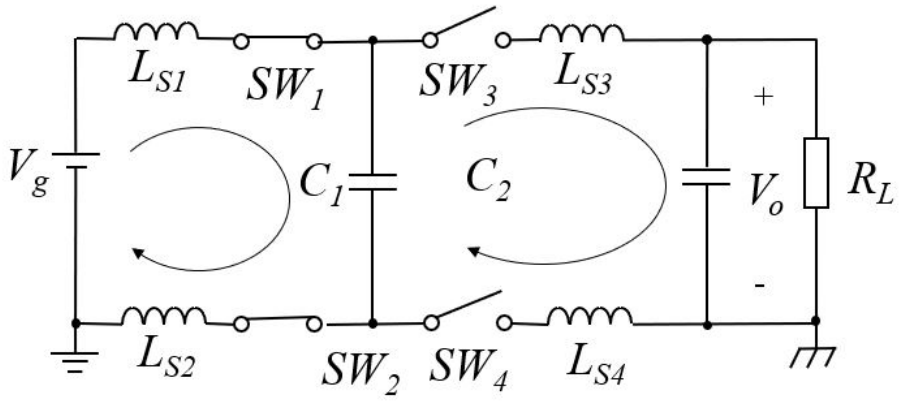
(a) Schematic



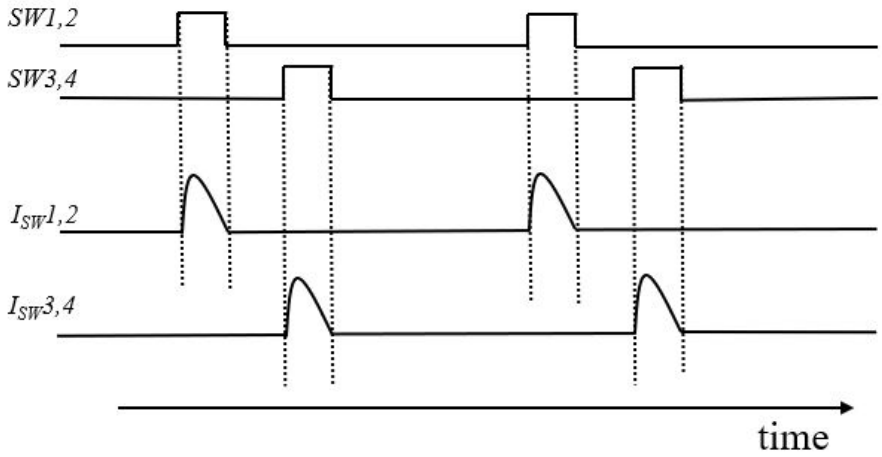
(b) Waveform

Figure 2.7: Switched-capacitor isolation for 5W aerospace application

cycle. The converter is designed for use in off-line power supplies and thus must meet IEC60950 touch current (TC) requirements [5, 6]. Due to the large in-rush current spikes at each lateral switch device turn off/on, the converter is not able to mean peak TC standards even though it does meet RMS current TC requirements. The TC is shown to be proportional to common-mode voltage (Vcm), MOSFET parasitic output capacitance (Coss), and switching frequency. The converter is designed with silicon carbide (SiC) devices that have low (30pF) output parasitic capacitance (Coss).



(a) Schematic



(b) Waveform

Figure 2.8: Resonant switched-capacitor isolation

Further research by the Ohio State group resulted in TC measurements that nearly met the requirement [21]. The converter was a 400V, 400W isolated converter used at the back end of an AC/DC power converter. The prototype used 1.7kV SiC MOSFETs that had 30pF of parasitic output capacitance (C_{oss}). A transient model was developed that resulted in a hyperbolic sine function output response, as shown in Equation 2.1, where V_{cm} is the common mode voltage source; L_{stray} is the loop stray inductance; C_{oss} is the switch output capacitance; and R is the total series loop resistance including the loop stray resistance (R_{stray}), the switch on-resistance (R_{ds_on}), and the 500Ω resistance in the human-body impedance.

$$I_{cm}(t) = \frac{2V_{cm}e^{-t\frac{R}{2L_{stray}}}sinh(\frac{t\sqrt{C_{oss}(C_{oss}R-4L_{stray})}}{2L_{stray}C_{oss}})\sqrt{C_{oss}(C_{oss}R-4L_{stray})}}{C_{oss}R^2-4L_{stray}} \quad (2.1)$$

Based on Equation 2.1, it is found that 1) larger C_{oss} results in larger values of I_{cm}, 2) larger L_{stray} damps the I_{cm}, and 3) since I_{cm} flows each switch cycle, I_{cm} increases with switch frequency.

Further research conducted by the Ohio State group resulted in using TC suppression to meet the TC standard [22, 23]. To suppress the TC, current sources are built into the gate drive that forces a current to flow opposite of the internally generated leakage current. The circuit used is a small buck-boost converter that operates as a current compensating supply. It is shown experimentally that the TC voltage for the converter with no compensation is 231mV RMS compared to 117mV RMS for the compensated design, which is lower than the 125mV RMS IEC60950 limit.

Using this same suppression approach, the TC is reduced below the IEC60950-1 limit in [24]. A 2kW SGI-based resonant SC converter is developed with integral active TC suppression circuit. The converter is designed for use in transformerless electric vehicle charger applications. The topology uses a two-stage totem-pole design cascaded with an SGI dc/dc solution which is selected due to high efficiency. The efficiency of the converter is maintained above 98%.

2.5 Transformerless PV Inverters

The transformerless isolated converters previously mentioned are used in applications such as off-line power supply, low-power DC/DC auxiliary supply for aerospace, AC/AC LED TV backlight, and EV battery charger applications. In these applications, the common-mode leakage currents that flow are referred to as "touch currents (TC)" in the IEC60950-1 specification and are limited- as previously discussed. The PV inverter and PV microinverter industry has taken a much different approach

Table 2.2: Standards of the grid connected PV system

Standards	**IEEE1547.2**	**IEC61727**	**US NEC (NFPA 70)**	**VDE 0126-1-1 VDEARN4105**
galv iso/sys gnd	-	-	rqd >50V	-
leakage gnd cur	-	-	-	30mA >0.3s 100mA >0.4s 300mApk >0.3s disconnect <5s
DC curr. inj.	<0.5 rated%	<1% rated	-	<1A

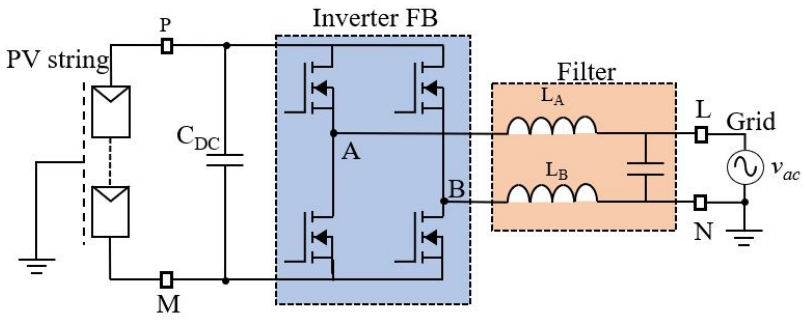
to reducing common-mode leakage current (known as earth ground current or simply ground current). Instead of attempting to design transformerless isolated inverter circuits, the PV inverter industry has attempted to solve common-mode leakage current issues by the following: 1) control modulation schemes to produce zero common-mode voltage thereby producing zero ground current and/or 2) develop a wide variety of topologies that result in either zero ground current or reduced ground current. Both these methods are aimed at reducing ground current levels to meet IEEE1547.2, IEC61727, U.S. NEC (NFPA 70), VDE 0126-1-1, and VDE-AR-N 4105 [2, 3, 10]. The common-mode currents that result can produce 1) DC current injection onto the grid, and 2) ground leakage currents. The IEEE, IEC, and VDE standards limit DC current injection, but only the VDE standards limit the ground leakage current specifically. The NEC specification requires either isolation or system grounding. Important limits are shown in Table 2.2.

Beginning in 2005, national electric code (NEC) section 690.35 allowed PV systems meeting certain requirements to have ungrounded conductors [25]. This change permitted the use of inverters without isolation between the DC input to AC output called *non-isolated inverters* or also known as *transformerless inverters*- for increased efficiency and cost savings. A consequence of this change was transformerless inverter designs that suffered from excessive earth ground current. Research as early as 1999 demonstrated that this ground current was due to the following factors: 1) parasitic

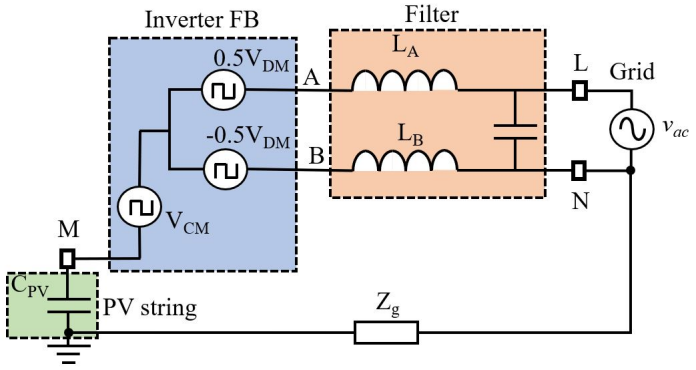
capacitance from PV module to earth ground, 2) inductance of inverter filter, and 3) common-mode voltage of inverter. However, efforts to mitigate this current did not begin until 2006 when Oscar Lopez compared three different inverter topologies (full-bridge, neutral-point clamped, and cascaded full-bridge) with both unipolar and bipolar modulation schemes [11]. Lopez demonstrated through simulation that 1) the full-bridge topology could reduce the earth ground current to zero by using bi-polar modulation of the switch devices, 2) the neutral-point clamped topology maintains zero earth ground current since the midpoint of the DC sources are grounded resulting in zero common-mode voltage to excite the ground current loop path. The remaining topologies (uni-polar modulated full-bridge and cascaded full-bridge) exhibited high levels of earth ground current. Neither modulation strategy reduced earth ground currents in the cascaded full-bridge topology.

In subsequent research [12, 13], Lopez demonstrated empirical results and showed that the earth ground current was due to a resonant tank circuit (Figure 2.9) around the system consisting of the following components in series: 1) parasitic capacitance from PV module frame to earth ground, 2) common-mode voltage of the inverter, 3) equivalent common-mode inductance of the inverter filter, and 4) earth ground impedance. This resonant tank circuit is difficult to measure and varies with environmental conditions. Due to the resonant nature of the circuit, large amounts of earth ground current can flow with only a small common-mode excitation voltage.

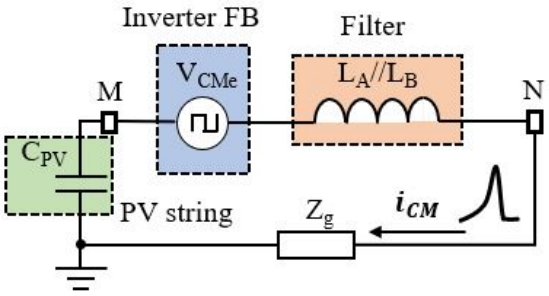
A review of 45 transformerless PV inverter topologies in [26] gives a classification system and compares the leakage current of each. For the comparison, each topology is simulated with PLECs software. Figure 2.10 shows that the transformerless inverters are first classified according to magnitude of DC link voltage. Additionally, there are four sub-types under the single PV (Vpv) DC link category. There are three additional sub-types under the H-bridge topologies as shown. The comparison of the converters is given in Table 2.3. As seen, only the common-ground converters (CMN-



(a) Non-isolated string inverter system



(b) Equivalent common-mode model of non-isolated string inverter



(c) Equivalent common-mode model of non-isolated PV inverter systems showing series resonant tank circuit in earth ground loop

Figure 2.9: Development of common-mode model for non-isolated string inverter system

GND) have zero common-mode leakage current. Twenty-six (26) of the converters do not meet the VDE specification requiring less than 30mA of leakage current.

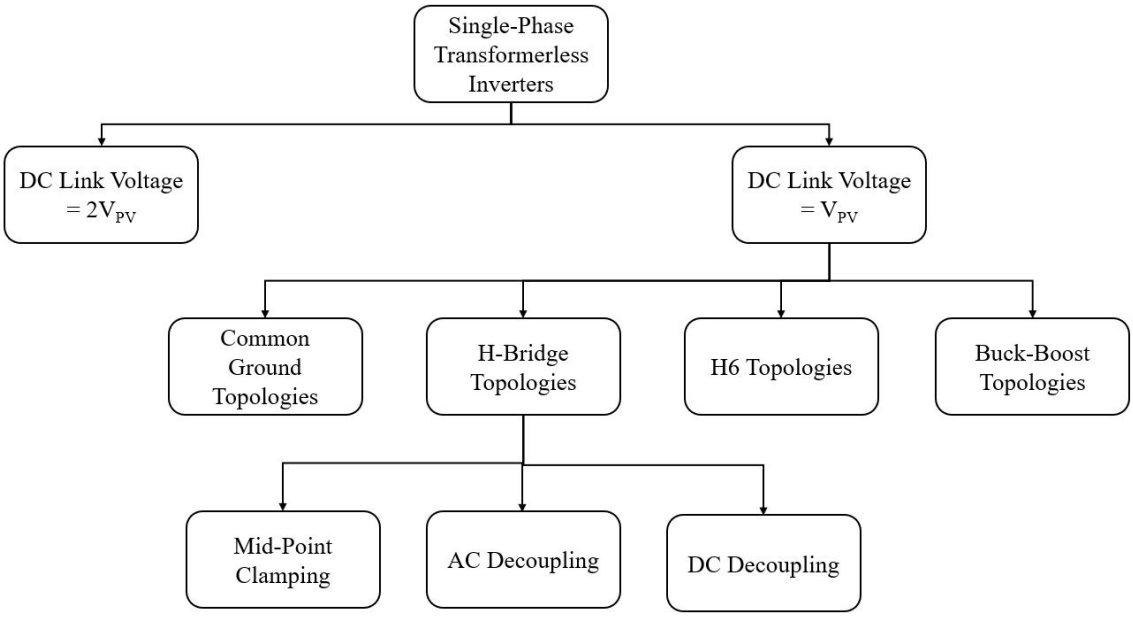


Figure 2.10: Single-Phase Tranformerless Inverter Classification

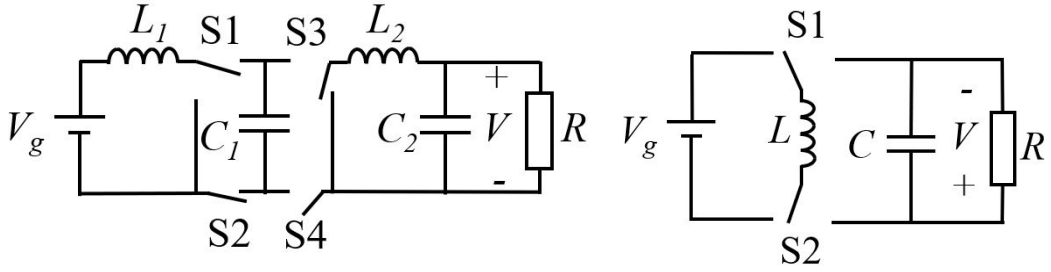
Table 2.3: Summary of Single Phase Transformerless Inverters

Topology Name	**Category**	**CM Curr.(mA)**	**Meets VDE**
Two-Switch	2Vpv	≤ 2	$\surd$
NPC	2Vpv	≤ 3.5	$\surd$
ANPC	2Vpv	≤ 2.5	$\surd$
T-type	2Vpv	≤ 4	$\surd$
Variant NPC	2Vpv	≤ 4.2	$\surd$
DC curr. inj.	2Vpv	≤ 2	$\surd$
Unipolar FB	Vpv	≤ 55	
Bipolar FB	Vpv	≤ 1800	
Virt. DC Bus	CMN-GND	~ 0	$\surd$
S4	CMN-GND	~ 0	$\surd$
Siwakoti-H	CMN-GND	~ 0	$\surd$
Siwakoti	CMN-GND	~ 0	$\surd$
Flyig cap	CMN-GND	~ 0	$\surd$
Flying Inductor	CMN-GND	~ 0	$\surd$
Karschny	CMN-GND	~ 0	$\surd$
iH5/oH5	Mid-Clamp	≤ 20	$\surd$
oH5-1	Mid-Clamp	≤ 200	
oH5-2	Mid-Clamp	≤ 200	
H5-D	Mid-Clamp	≤ 50	
HERIC Active 1	Mid-Clamp	≤ 25	$\surd$
HERIC Active 2	Mid-Clamp	≤ 25	$\surd$
HERIC Active 3	Mid-Clamp	≤ 25	$\surd$
PN NPC	Mid-Clamp	≤ 35	
HB-ZVR	Mid-Clamp	≤ 200	
HB-ZVR-D	Mid-Clamp	≤ 40	
Heric	AC Decoupling	≤ 200	
Heric AC	AC Decoupling	≤ 200	
H5 type	DC Decoupling	50-200	
H6-type	DC Decoupling	200-400	
H6 (4-types)	H6-type	≤ 200	
impr. H6 with diodes-1	H6-type	≤ 20	$\surd$
Hybrid Bridge	H6-type	≤ 250	
ZCT-H6-1	H6-type	≤ 250	
SLF-H6-1	H6-type	≤ 150	
bkbst1 (5-types)	Buck-Boost	≤ 250	
bkbst2 (3-types)	Buck-Boost	≤ 20	$\surd$
Tang	other	≤ 20	$\surd$
Xia	other	≤ 200	
Liu	other	≤ 40	

CHAPTER 3: ACTIVE ISOLATION TOPOLOGIES

3.1 Introduction

This section introduces a new transformerless isolation technique called active isolation in which active semiconductor power devices are used to isolate conventional converters such as boost-buck and buck-boost, as seen in Figure 3.1. The approach is different from previous attempts since it does not rely on capacitors to form the isolation barrier nor does it use capacitors to perform the conversion ratio, rather it uses the traditional volt-second balance of the converter inductor to perform conversion.



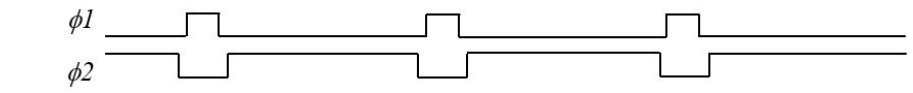
(a) Boost-Buck Converter (b) Buck-Boost Converter

Figure 3.1: Proposed galvanic active isolated topologies

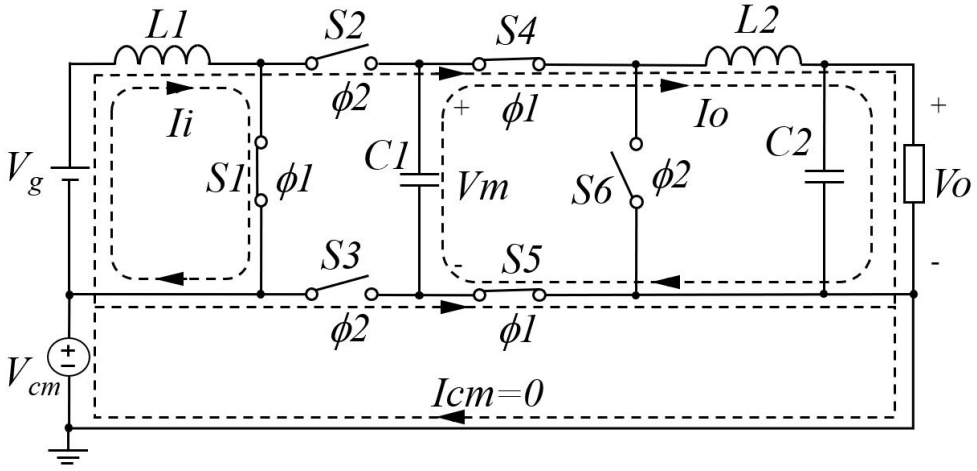
3.2 Operating Principles and Comparisons

The basic operation of the active isolated boost-buck converters is shown in Figure 3.2. During Mode 1, inductor L1 is charged while the input and output are galvanically isolated by S2 and S3. Concurrently, energy from C1 is filtered and transferred to the load through S4 and S5. During mode 2, capacitor C1 is charged while switches S4 and S5 galvanically isolated the input from output. Concurrently, energy from L2 charges C2 and supports the load.

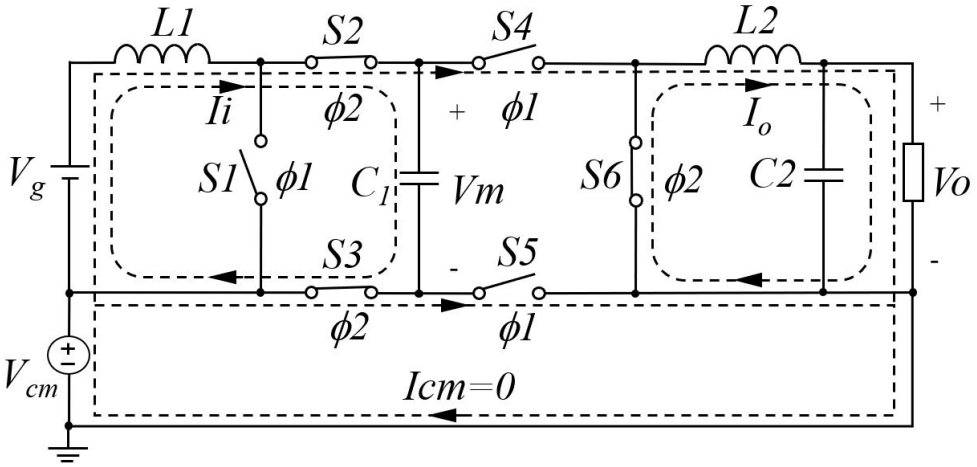
The basic operation of the active isolated buck-boost converter is shown in Figure



(a) Timing waveform



(b) Mode 1: Energy transferred from C1 to load

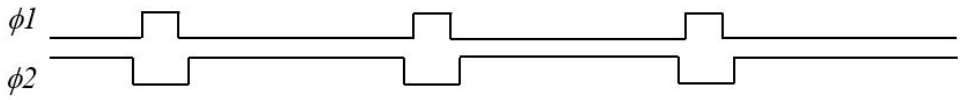


(c) Mode 2: Energy transferred from source to C1

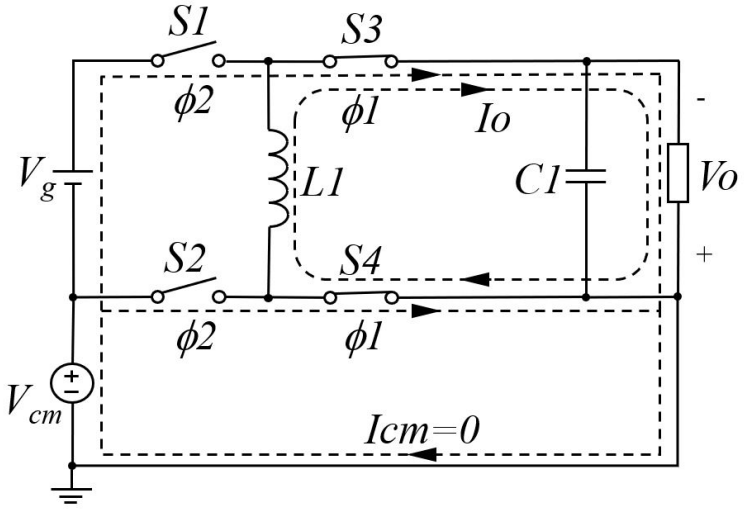
Figure 3.2: Operating principle of active isolated boost-buck converter

3.3. During mode 1, S1 and S2 open to provide galvanic isolation while S3 and S4 close to transfer energy from the inductor L1 to the load and charge C1. During mode 2, S1 and S2 are closed and energy is stored in the inductor L1, while S3 and S4 provide galvanic isolation from input to output; capacitor C1 supports the load.

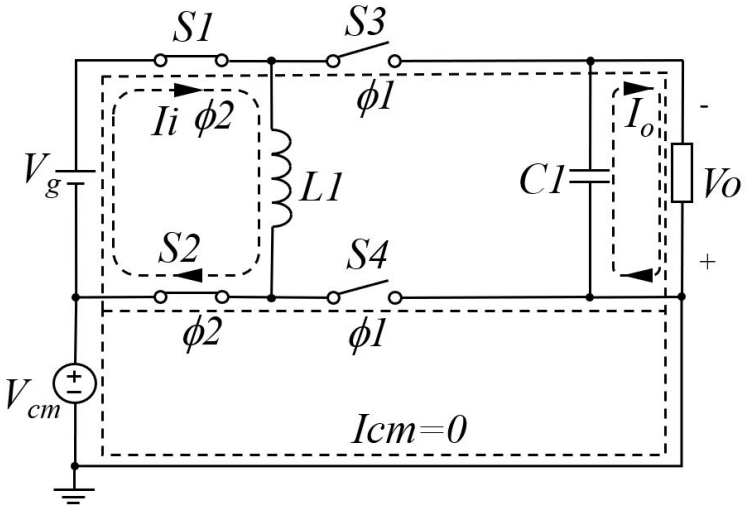
A comparison of the proposed boost-buck (Act. Bst-Bk) and buck-boost (Act. Bk-Bst) converters with *Dual Active Bridge* (DAB) and transformer isolated Cuk



(a) Timing waveform



(b) Mode 1: Energy transfer from L1 to load



(c) Mode 2: Energy transfer from source to L1

Figure 3.3: Operating principle of active isolated buck-boost converter

converter operating with Vin=400V and Vout=48V are shown in Table 3.1. As shown, the proposed converters' main advantage is elimination of the bulky transformer. The DAB and active isolated buck-boost converters need an additional input EMI filter which would require additional magnetics and capacitance. The proposed active isolated boost-buck and transformer isolated Cuk converters have properties that

Table 3.1: Comparison of proposed converters to conventional topologies

Topology	**DAB**	**Act. Bk-Bst**	**Act. Bst-Bk**	**Isolated Cuk**
num. switches	8	6	12	2
num. transf.	1	0	0	1
transf. ratio	4:1	n/a	n/a	1:1
num. induct.	0	1	2	2
num. cap.	2	1	2	3
Incl EMI filt?	no	no	yes	yes

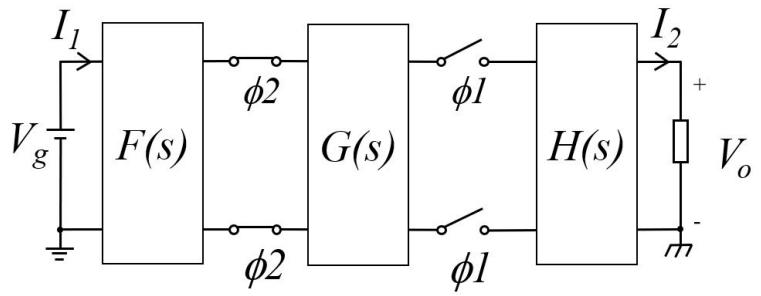
approach an ideal DC transformer since they have smooth input and output current.

3.3 Generalized Approach to Active Isolation

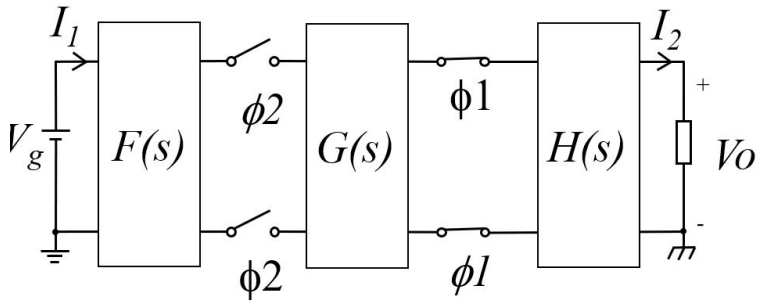
The active isolation method can be applied generically to inductor volt-second conversion circuits by breaking the low-side return path, as shown in Figure 3.4. For the method to be applied, the following conditions must be met: 1) energy transfer network must be completely in the input circuit during one interval and completely in the output circuit during the next interval [27], 2) switched capacitor operation is not used in active isolation since excessive in-rush currents impose additional restrictions on devices and design layout not consistent with conventional switched-mode topology design restraints, 3) switched operation of modes must be non-overlapping. If the previous conditions are met, the converter may be active isolated by breaking the converter return paths with appropriate switches similar to the conventional high-side-only switches in the basic converter topologies. The simplest case of this is shown in Figure 3.4c with the active isolated buck-boost converter.

Application of this method to the three basic converters, shown in Figure 3.5, reveals that only the cascaded buck-boost converter of Figure 3.5c is applicable to the method, since energy transfer is separated between the two different converter modes as required.

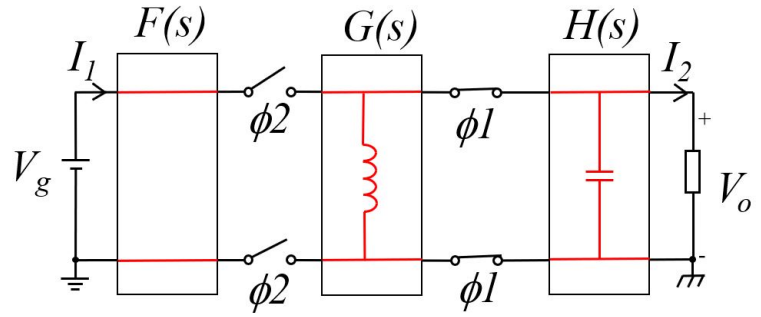
The converter of Figure 3.5c is redrawn with an extra switch added in the low-side as shown in Figure 3.6a and Figure 3.6b. As seen, the energy transfer is the



(a) Mode 1



(b) Mode 2

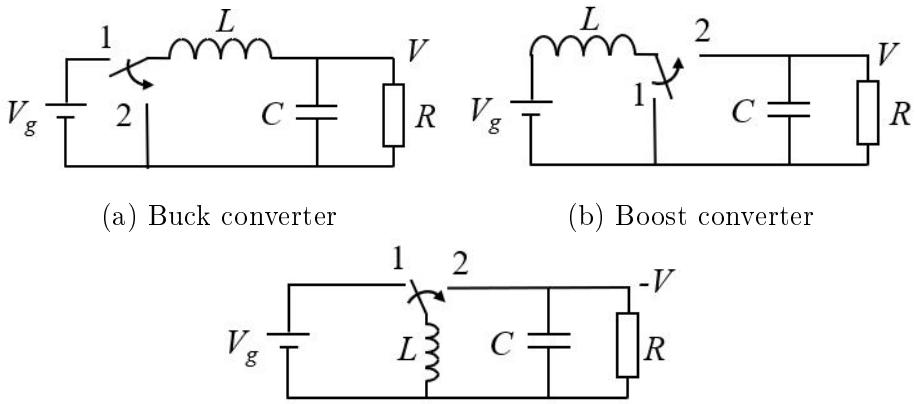


(c) The simplest case showing buck-boost topology

Figure 3.4: Generalized structure and simplest case for active isolation

same as before but now the input and output are galvanically isolated by the switch. This results in the active isolated buck-boost converter shown in Figure 3.6c. This result indicates that cascaded converters may be good candidates for conversion to active isolated topologies. The buck-boost converter just analyzed is one of four basic cascaded converter topologies as shown in Figure 3.7.

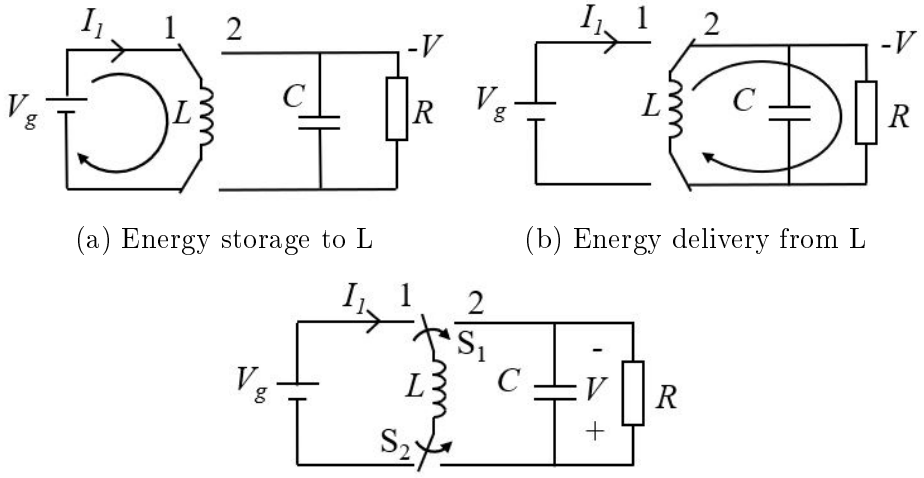
The general approach to active isolation is now applied to the non-inverting buck-boost converter shown in Figure 3.7b. Single-pole single-throw (SPST) switches are added to the non-isolated topology as shown in Figure 3.8a and Figure 3.8b. After the



(a) Buck converter (b) Boost converter

(c) Buck-boost converter

Figure 3.5: General approach to active isolation applied to the three basic converters shows that only the buck-boost has the potential for active isolation



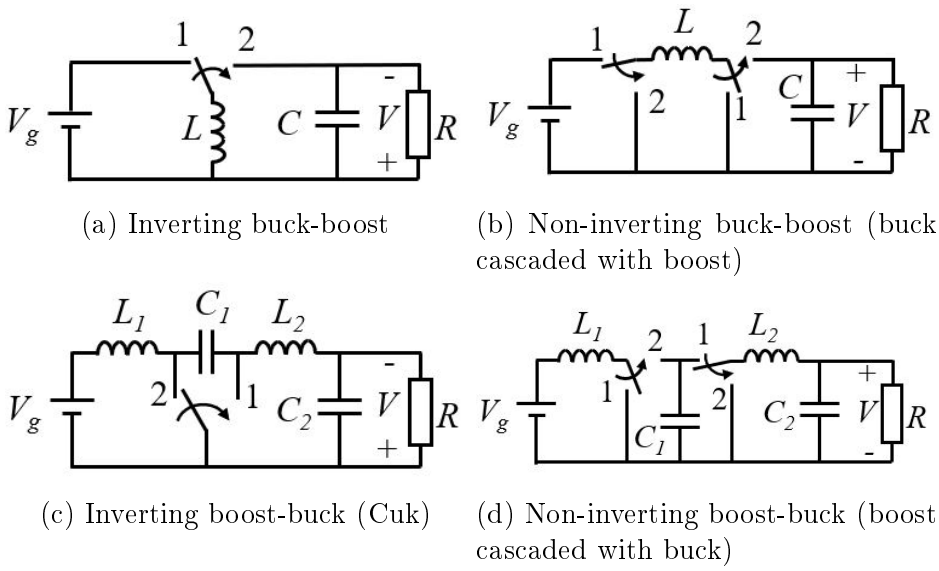
(a) Energy storage to L (b) Energy delivery from L

(c) Isolated buck-boost

Figure 3.6: General approach to active isolation applied to the buck-boost converter shows that it reduces to the active isolated buck-boost converter proposed

circuit is redrawn and flipped as shown in Figure 3.8c, it becomes obvious that this converter is really identical to the previously-derived isolated buck-boost converter as seen in Figure 3.6c.

The general approach to active isolation is applied in a similar manner to the inverting and non inverting boost-buck converters shown in Figure 3.7c and Figure 3.7d. These converter derivations are shown in Figure 3.9 and Figure 3.10. Both convert-



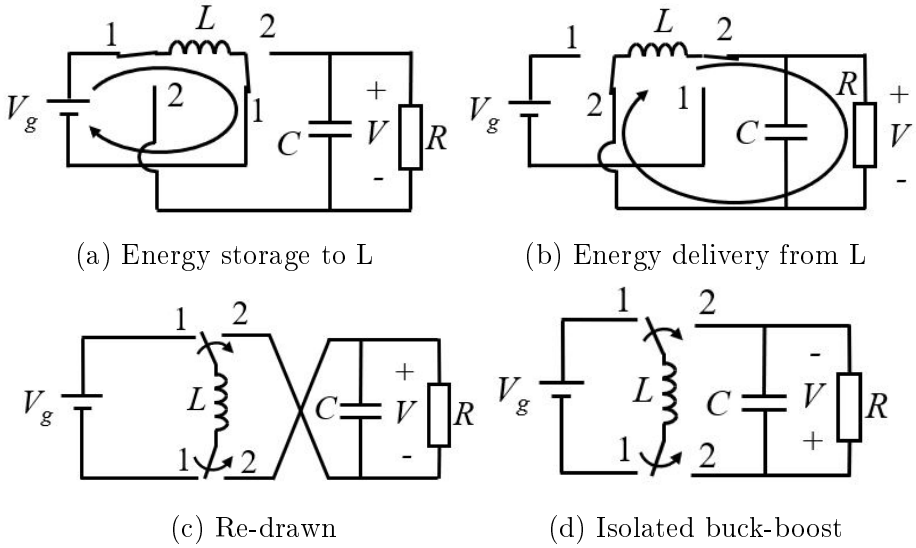
(a) Inverting buck-boost

(b) Non-inverting buck-boost (buck cascaded with boost)

(c) Inverting boost-buck (Cuk)

(d) Non-inverting boost-buck (boost cascaded with buck)

Figure 3.7: The four basic cascaded converters before conversion to active isolation types



(a) Energy storage to L

(b) Energy delivery from L

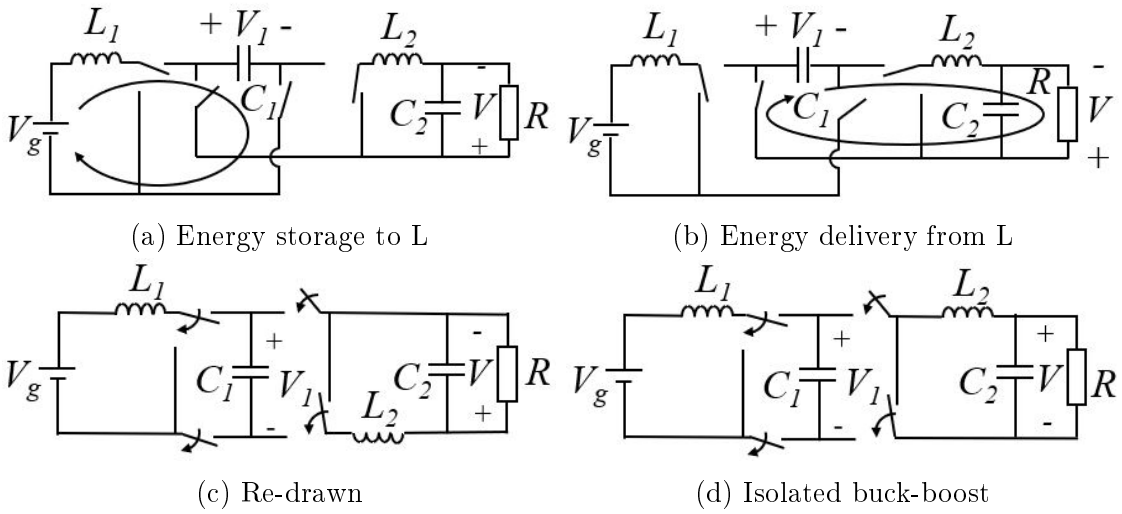
(c) Re-drawn

(d) Isolated buck-boost

Figure 3.8: General approach to active isolation applied to the non-inverting buck-boost converter shows that it also reduces to the active isolated buck-boost converter proposed

ers reduce to the active isolated boost-buck converter as seen in Figure 3.9d and Figure 3.10c.

So, the four cascaded converters shown in Figure 3.7 become two converters, the active isolated boost-buck, and active isolated buck-boost converters.



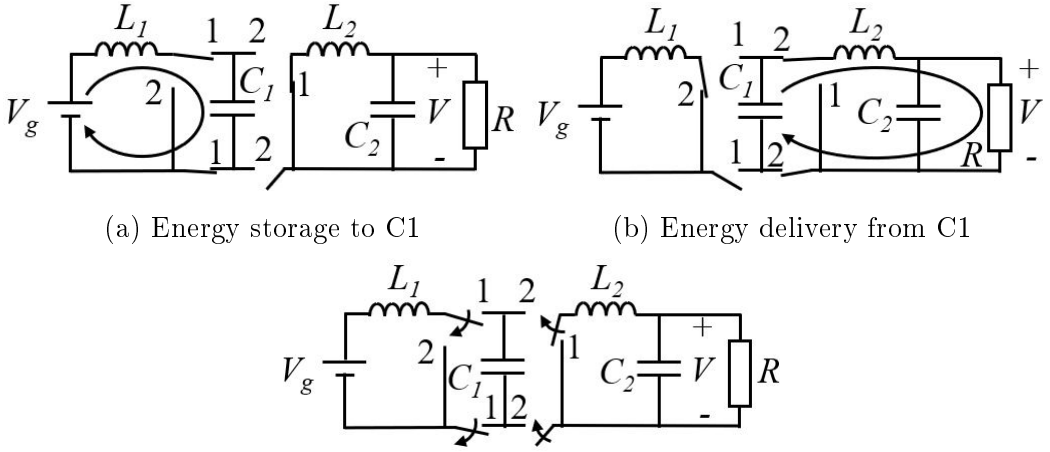
(a) Energy storage to L

(b) Energy delivery from L

(c) Re-drawn

(d) Isolated buck-boost

Figure 3.9: General approach to active isolation applied to the inverting boost-buck (Cuk) converter shows that it reduces to the active isolated boost-buck converter proposed



(a) Energy storage to C1

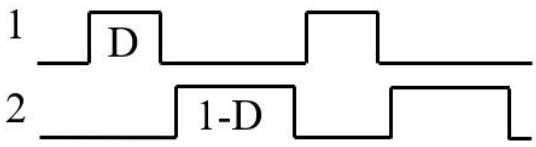
(b) Energy delivery from C1

(c) Isolated boost-buck

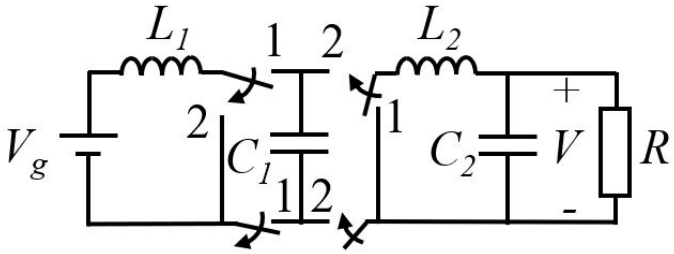
Figure 3.10: General approach to active isolation applied to the non-inverting boost-buck converter shows that it also reduces to the active isolated boost-buck converter proposed

3.4 Dual Cascaded Combinations

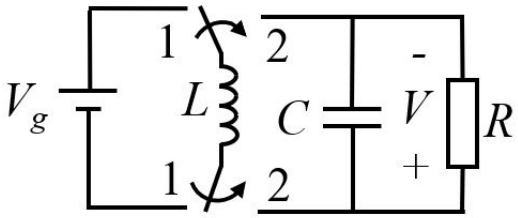
It is possible to create additional active isolated topologies by examining other dual-cascade combinations. In this section, topologies derived from the following basic topologies are investigated: Buck, Boost, Buck-Boost, Cuk, Single-Ended Primary-Inductor Converter (SEPIC), and Zeta (Inverse SEPIC).



(a) Non-overlapping switch waveform



(b) AI boost-buck Converter

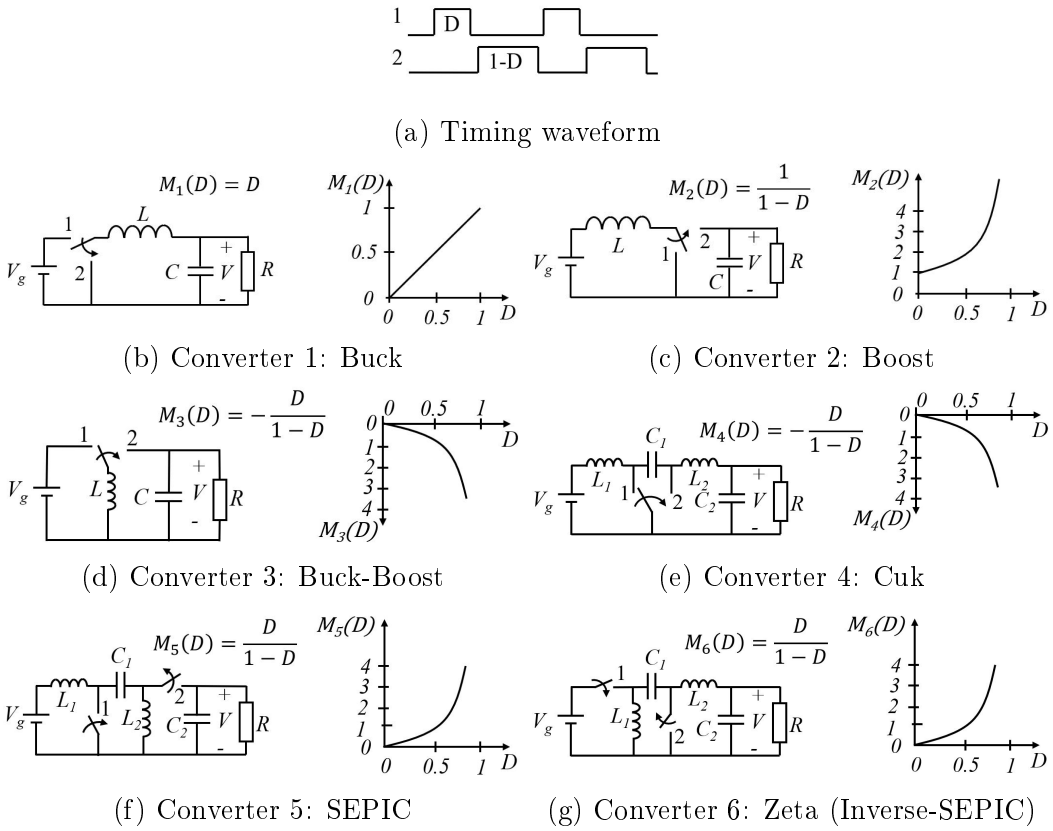


(c) AI inverting buck-boost Converter

Figure 3.11: Existing buck- and boost-derived AI topologies [32, 38]

3.4.1 Development of New Active Isolated Topologies

This section is devoted to the development of new active isolated topologies. The objective is to determine the set of AI converters that result from dual cascade combinations of the following basic six converter topologies: buck(1), boost(2), buck-boost(3), Cuk(4), SEPIC(5), and Zeta(6), as shown in Fig 3.12, and with conversion ratios $M_1(D)$, $M_2(D)$, $M_3(D)$, $M_4(D)$, $M_5(D)$, $M_6(D)$, respectively. The method used to develop the new set of AI converters is to first form a dual cascade combination of converters. Thirty-six possible converter combinations results, as shown in Table 3.2. Numeric codes one (1) to six (6) are used to index each converter for referencing new converter topologies, e.g., 1-1 refers to a buck-buck cascaded converter, and 1-2 refers to a buck-boost cascaded converter, etc. The second step is to add isolation switches to the converters. These additional switches are inserted in a lateral



(a) Timing waveform

(b) Converter 1: Buck

(c) Converter 2: Boost

(d) Converter 3: Buck-Boost

(e) Converter 4: Cuk

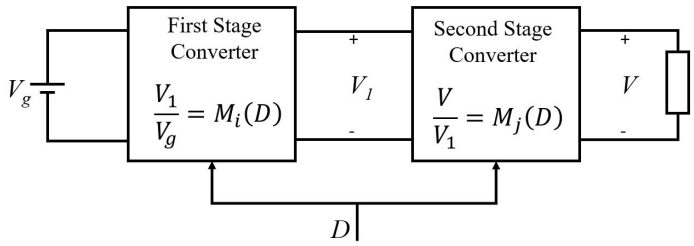
(f) Converter 5: SEPIC

(g) Converter 6: Zeta (Inverse-SEPIC)

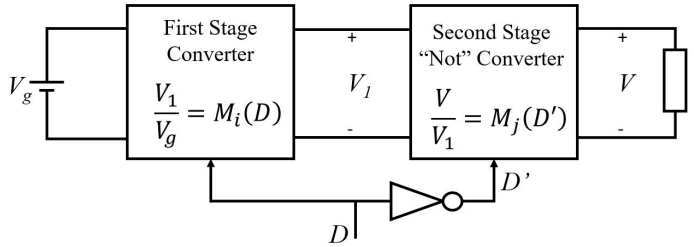
Figure 3.12: Six basic converter topologies and conversion ratios

Table 3.2: All thirty-six possible dual-cascade combinations of the six basic converters of Figure 3.12

Stage: 2nd → 1st ↓	**Buck (1) VI**	**Boost (2) IV**	**Buck-Boost (3) VV**	**Cuk (4) II**	**SEPIC (5) IV**	**Zeta (6) VI**
Buck(1) VI	(1-1) VI-VI	(1-2) VI-IV	(1-3) VI-VV	(1-4) VI-II	(1-5) VI-IV	(1-6) VI-VI
Boost(2) IV	(2-1) IV-VI	(2-2) IV-IV	(2-3) IV-VV	(2-4) IV-II	(2-5) IV-IV	(2-6) IV-VI
Buck-Bst(3) VV	(3-1) VV-VI	(3-2) VV-IV	(3-3) VV-VV	(3-4) VV-II	(3-5) VV-IV	(3-6) VV-VI
Cuk(4) II	(4-1) II-VI	(4-2) II-IV	(4-3) II-VV	(4-4) II-II	(4-5) II-IV	(4-6) II-VI
SEPIC(5) IV	(5-1) IV-VI	(5-2) IV-IV	(5-3) IV-VV	(5-4) IV-II	(5-5) IV-IV	(5-6) IV-VI
Zeta(6) VI	(6-1) VI-VI	(6-2) VI-IV	(6-3) VI-VV	(6-4) VI-II	(6-5) VI-IV	(6-6) VI-VI



(a) First and second stage converter having the same clock phase



(b) Second stage with inverting clock phase creating a "not" converter

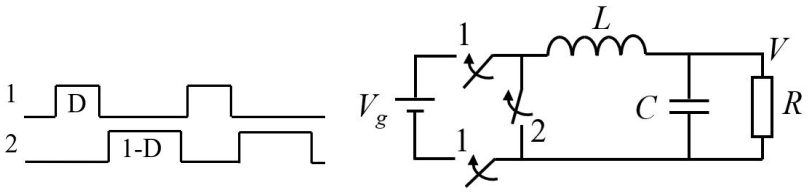
Figure 3.13: Dual-cascaded converters used for creation of new active isolation topologies

configuration on the low-side rail and operate in synchronization with lateral switches on the high-side rail. They are placed so that energy transfers from input to output without galvanic connection of supply and load. Exactly four lateral switches are required to actively isolate the converters. More than four lateral switch devices on high- and low-side rail is considered redundant and is not desirable. Third, excessive passive components are removed (if applicable). In some cases, a high-order filter is created due to the cascade combination. These can be reduced to first-order filters to simplify the topology without affecting the conversion ratio. In other cases, redundant switches are removed. Finally, the new converter characteristics are analyzed and compared to other combinations as follows: (1) galvanic isolation capabilities, (2) number and type of components, and (3) conversion ratio. The conversion ratio of the resulting dual-cascade combination is given by:

$$M_{ij} = M_i(D)M_j(D), \tag{3.1}$$

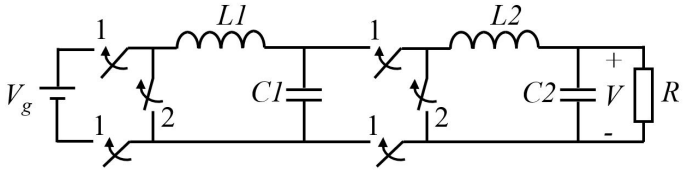
where i is the index of the first stage, j is the index for the second stage, and D is the mean on-time duty ratio, as shown in Figure 3.13a. It may be necessary to invert the clock phasing of the second stage to achieve isolation, as shown in Figure 3.13b. In this case, a "not" converter is produced with conversion ratio of $M_j(D')$ as shown in Figure 3.13b.

3.4.2 Primary-Side Buck Architectures

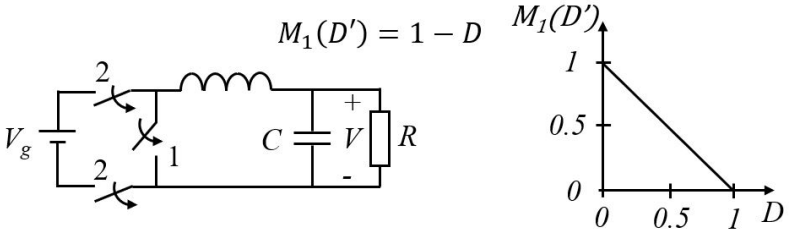


(a) Timing waveform

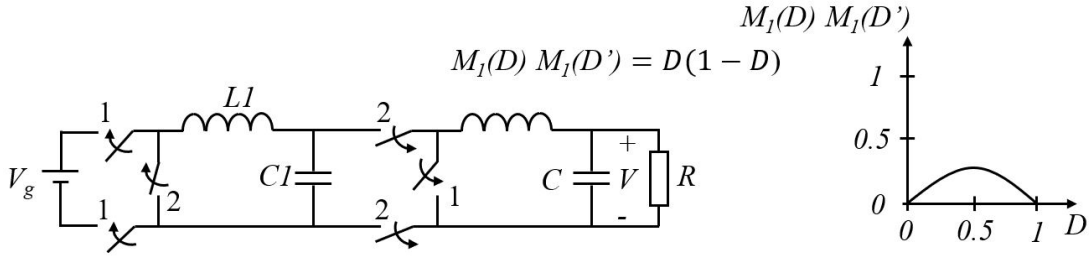
(b) Three-switch buck converter



(c) Buck-buck Converter (does not isolated)



(d) Three-switch not buck converter

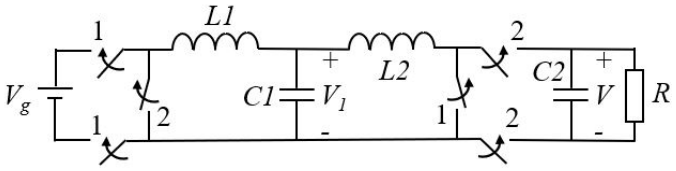


(e) Buck-not buck converter

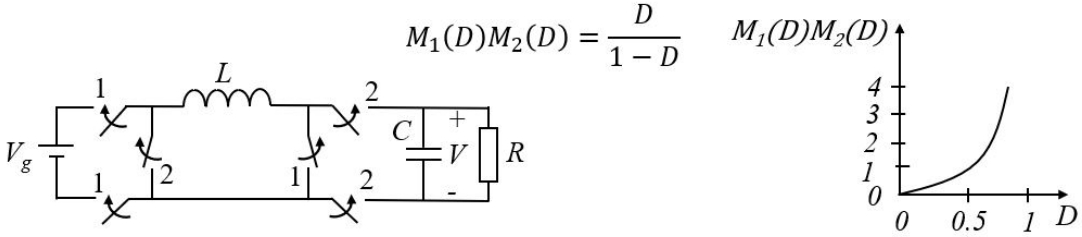
Figure 3.14: Development of AI Buck-not buck converter

The first dual-cascade combination to be considered is the buck-buck converter,

indicated in Table 3.2 as (1-1) and as "VI-VI". (Since a buck converter has an internal voltage-to-current (V-to-I) architecture, the acronym "VI" is used to describe the converter structure.) As shown in Figure 3.14c, the resulting cascade combination does not result in galvanic isolation since both pairs of high and low side switches open and close during the same clock phase cycle. However, if the second stage clock phase cycle is inverted, the second stage converter becomes a not buck (Figure 3.14d) and the resulting cascade combination with an initial buck stage results in the buck-not buck converter shown in Figure 3.14e with corresponding conversion ratio equation and plot. The conversion ratio is not desirable since it falls back to zero for $D > 0.5$. The converter requires six switches (two more than the minimum), two inductors, and two capacitors.



(a) Cascade combination of buck followed by boost showing proper switch phasing for isolation but containing a third-order T-filter

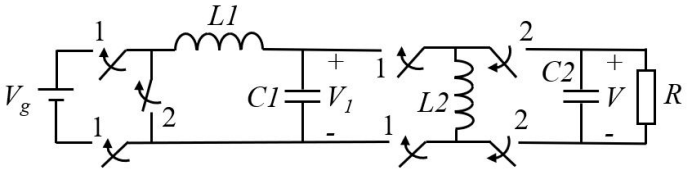


(b) AI non-inverting buck-boost converter after filter order reduction showing circuit and conversion ratio equation with corresponding plot

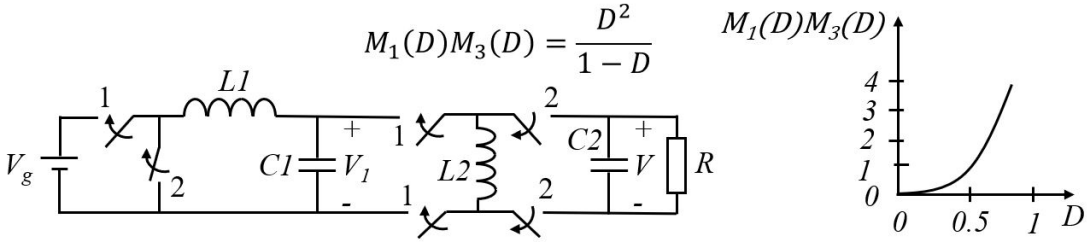
Figure 3.15: Development of AI non-inverting buck-boost converter

The second dual-cascade combination to be considered is the buck-boost converter indicated in Table 3.2 as (1-2) with internal VI-IV architecture. As seen in Figure 3.15a, the converter phasing is correct to achieve isolation since both the high- and low-side lateral switches have alternate phasing. However, the internal third-

order T-filter requires reduction to minimize passive component count, as shown in Figure 3.15b. The resulting converter requires six switches (two more than the minimum), one inductor, and one capacitor.



(a) Cascade of buck with buck-boost converter showing redundant set of mode-1 isolation switches



(b) AI buck-buckboost converter circuit with redundant mode-1 switch removed from low-side buck converter

Figure 3.16: Development of AI non-inverting buck-buckboost converter

The third dual-cascade combination to be considered is the buck-buckboost converter indicated in Table 3.2 as (1-3) with internal VI-VV architecture. As seen in Figure 3.16a, the converter is isolated but has a redundant set of mode-1 lateral switches. The converter with redundant switch removed from the low-side buck converter requires six switches (three more than the minimum), two inductors, and two capacitors, as shown in Figure 3.16b.

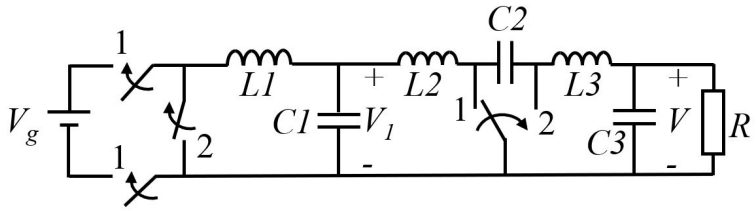
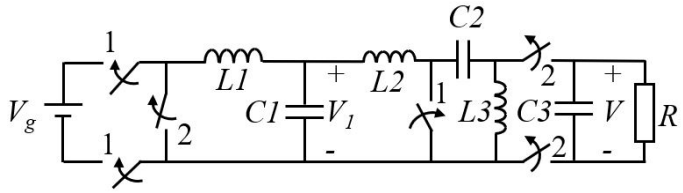


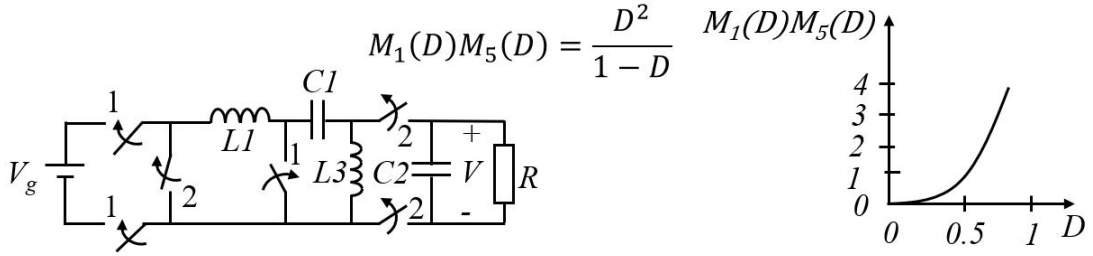
Figure 3.17: Cascade connection of buck and Cuk showing that the converter does not isolate

The forth dual-cascade combination to be considered is the buck-Cuk converter

indicated in Table 3.2 as (1-4) with internal VI-II architecture. As seen in Figure 3.17, the converter does not isolate since the switch in the Cuk is shut connected and does not have the required lateral switches to properly isolate the converter.



(a) Cascade combination of buck followed by SEPIC showing proper switch phasing for isolation but containing a third-order T-filter

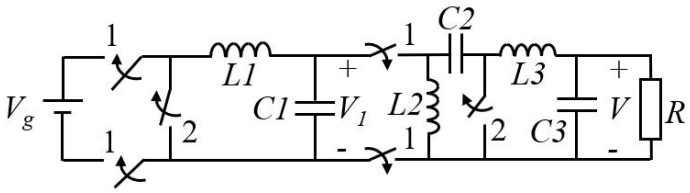


(b) AI buck-SEPIC converter after filter order reduction showing circuit and conversion ratio equation with corresponding plot

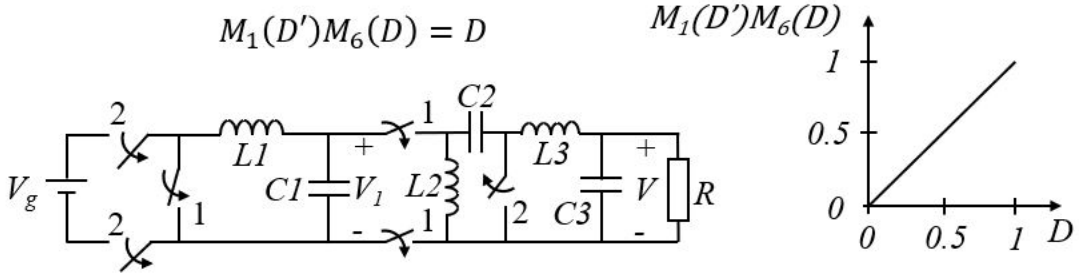
Figure 3.18: Development of AI buck-SEPIC converter

The fifth dual-cascade combination to be considered is the buck-SEPIC converter indicated in Table 3.2 as (1-5) with internal VI-IV architecture. As seen in Figure 3.18a, the converter phasing is correct to achieve isolation since both the high- and low-side lateral switches have alternate phasing. However, the internal third-order T-filter requires reduction to minimize passive component count, as shown in Figure 3.18b. The resulting converter requires six switches (two more than the minimum), two inductors, and two capacitors.

The sixth dual-cascade combination to be considered is the buck-Zeta converter indicated in Table 3.2 as (1-6) with internal VI-VI architecture. As seen in Figure 3.19a, the converter phasing is incorrect to achieve isolation since both the high- and low-side lateral switches have the same phasing. However, phase inversion of the first stage isolates input-to-output and results in the AI not buck-Zeta converter, as



(a) Cascade combination of buck followed by Zeta showing improper switch phasing for isolation



(b) AI not buck-Zeta converter after phase inversion of the first stage showing circuit and conversion ratio equation with corresponding plot

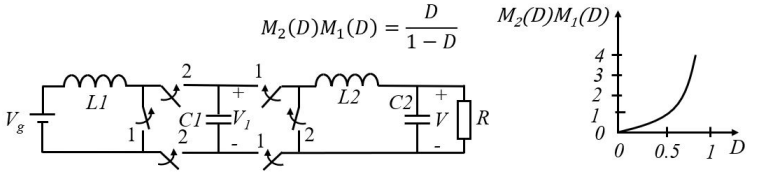
Figure 3.19: Development of AI buck-not Zeta converter

shown in Figure 3.19b. The resulting converter requires six switches (two more than the minimum), three inductors, and three capacitors.

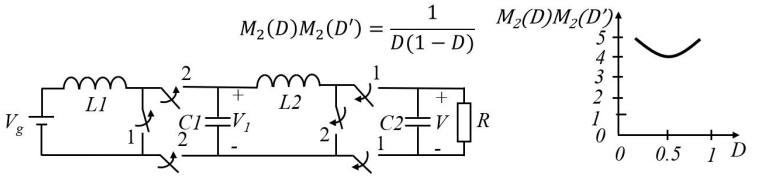
The total component count for the first-stage buck-type converters range from eight to twelve devices.

3.4.3 Primary-Side Boost Architectures

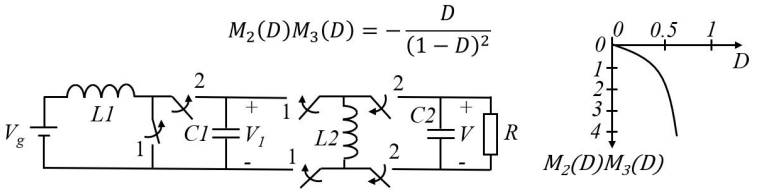
This subsection considers AI primary-side boost converters, that is, dual combinations of converters with a boost first stage. Using the procedure of the previous subsection whereby the converter is (1) cascaded, (2) checked for isolation, (3) phase inversion is applied if needed, and (4) filter reduction implemented, the converters in Figure 3.20 result. The AI boost-buck converter in Figure 3.20a is the same introduced in Figure 3.11b and has already been evaluated and prototyped in [32]. The AI boost-not boost converter in Figure 3.20b has a minimum conversion ratio of four at fifty percent duty cycle and increases at both higher and lower values of duty cycle. It requires six switches, two inductors, and two capacitors. The boost-buckboost converter in Figure 3.20c has a redundant low-side mode-2 isolation switch removed



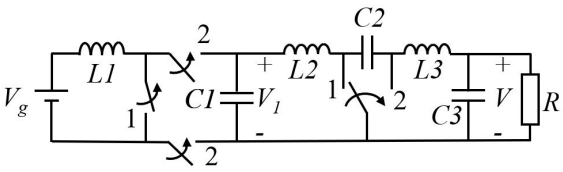
(a) AI boost-buck converter



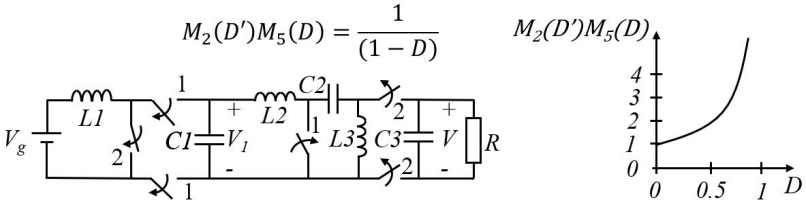
(b) AI boost-not boost converter



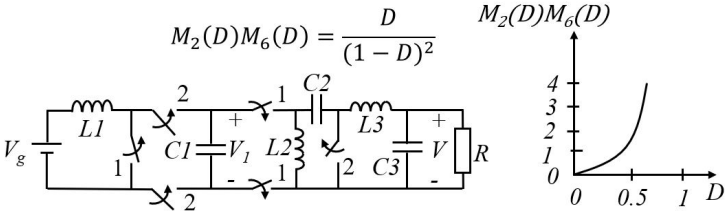
(c) AI boost-buckboost converter



(d) Boost-Cuk converter (does not isolate)



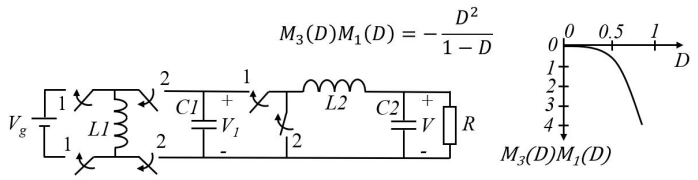
(e) AI not boost-SEPIC converter



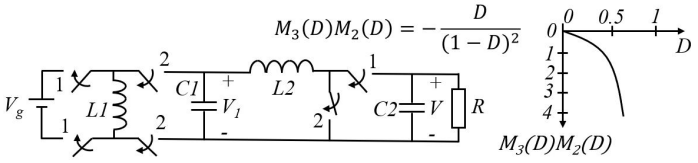
(f) AI boost-Zeta converter

Figure 3.20: Resultant AI primary-side boost converters and corresponding conversion ratio equations with plots

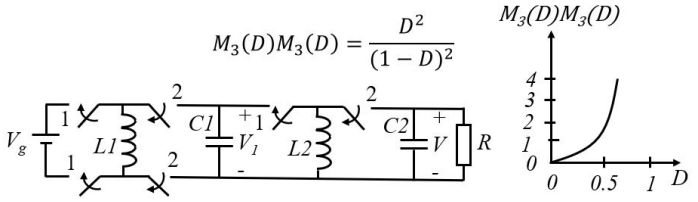
from the boost stage which results in a converter consisting of six total switches, two inductors, and two capacitors. The cascade combination of boost and Cuk converters



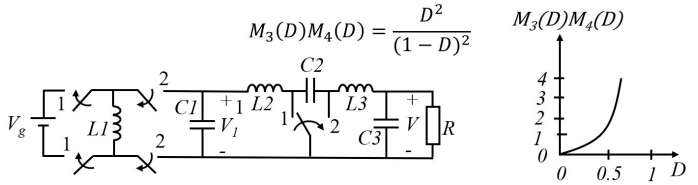
(a) AI buckboost-buck



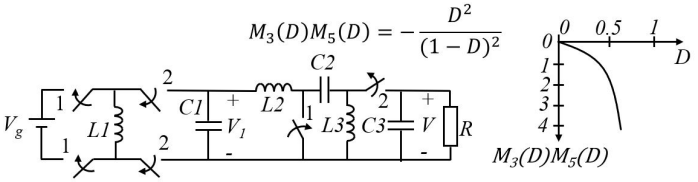
(b) AI buckboost-boost



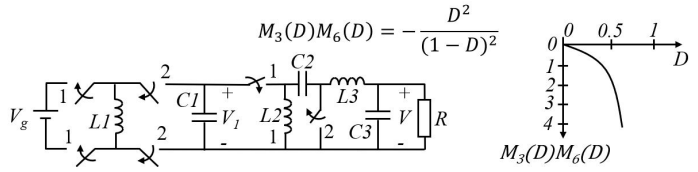
(c) AI buckboost-buckboost



(d) AI buckboost-Cuk



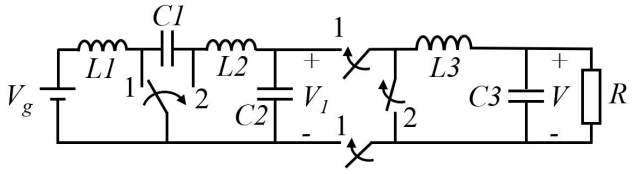
(e) AI buckboost-SEPIC



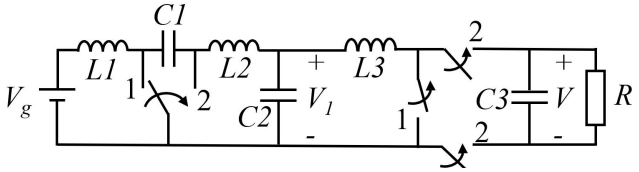
(f) AI buckboost-Zeta

Figure 3.21: Resultant AI primary-side buck-boost converters and corresponding conversion ratio equations with plots

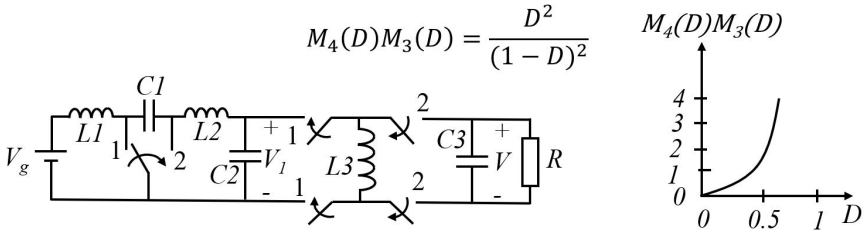
does not isolate, as seen in Figure 3.20d. The AI not boost-SEPIC and boost-Zeta converters require six isolation switches, three inductors, and three capacitors, as shown in Figure 3.20e and Figure 3.20f, respectively. The boost-Zeta converter has a



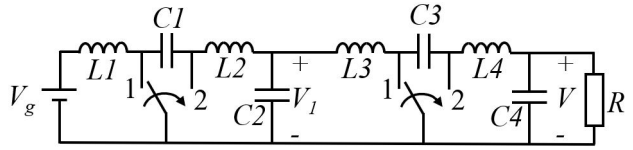
(a) Cuk-buck (does not isolate)



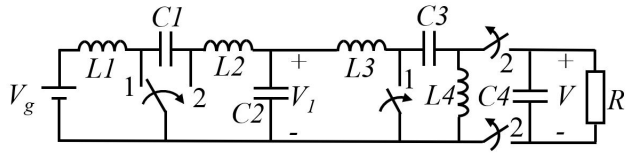
(b) Cuk-boost (does not isolate)



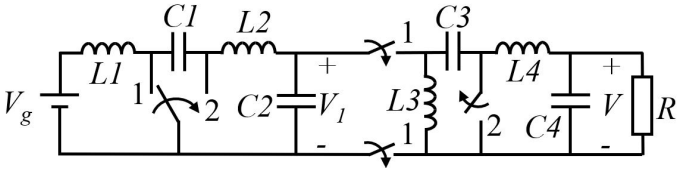
(c) AI Cuk-buckboost converter



(d) Cuk-Cuk (does not isolate)



(e) Cuk-SEPIC (does not isolate)



(f) Cuk-Zeta (does not isolate)

Figure 3.22: Resultant AI primary-side Cuk converters and corresponding conversion ratio equations with plots

desirable smooth input and output current. It also has non-inverting buck and boost capabilities. The total component count for these converters range from ten to twelve devices.

3.4.4 Primary-Side Buck-Boost Architectures

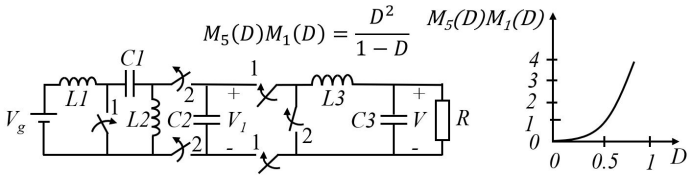
This subsection considers AI primary-side buck-boost converters. Using methods described in previous sections, AI converters with first-stage buck-boost converters are developed. Circuit diagrams and conversion equations with corresponding plots are shown in Figure 3.21. Since the buck-boost stage is isolated, all the resulting converters are also isolated, however, all but the buckboost-Cuk contain a redundant isolation switch that is removed. The resulting converters all contain six switches and from two to three capacitors and inductors each. All these converters contain a squared term in the numerator, denominator, or both of the conversion ratio. As such, these converters are good for large step-up or -down conversion ratios.

3.4.5 Primary-Side Cuk Architectures

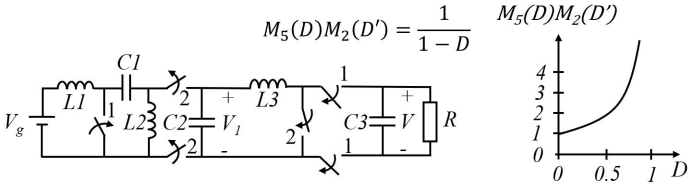
In this subsection, primary-side Cuk dual-cascaded converter architectures are considered. Of the six possible combinations, only one converter, the AI Cuk-buckboost converter, is able to provide the proper isolation, as shown in Figure 3.22. The converter contains six switch devices, three inductors, and three capacitors. Since the Cuk converter switch orientation is shunt, it is difficult for this class of converter to actively isolate. Converter types with laterally oriented switches provide the required disconnection from input source to output load for proper active isolation capabilities.

3.4.6 Primary-Side SEPIC Architectures

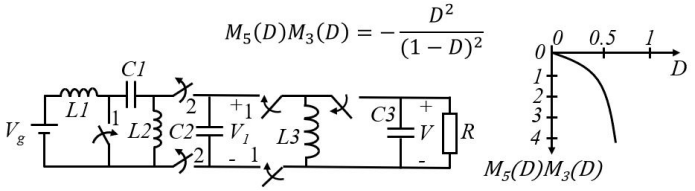
This subsection covers dual-cascade combination with initial Zeta stage. Only one combination does not properly isolate, the SEPIC-Cuk, as shown in Figure 3.23. The SEPIC-buck and SEPIC-not boost contain six switches, three inductors, and three capacitors. The SEPIC-buckboost contains six switches after removing one redundant mode-2 switch. It also contains three inductors and three capacitors. The SEPIC-not SEPIC converter always has a unit conversion ratio regardless of the duty cycle and contains six switches, four inductors, and for capacitors. The SEPIC-Zeta converter



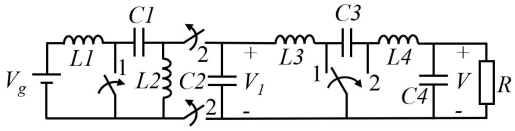
(a) AI SEPIC-buck converter



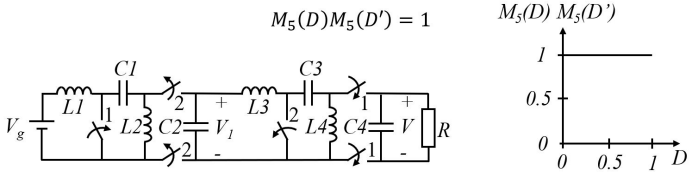
(b) AI SEPIC-not boost converter



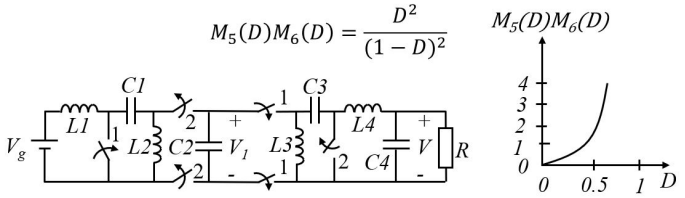
(c) AI SEPIC-buckboost converter



(d) SEPIC-Cuk (does not isolate)



(e) AI SEPIC-notSEPIC converter



(f) AI SEPIC-Zeta converter

Figure 3.23: Resultant AI primary-side SEPIC converters and corresponding conversion ratio equations with plots

contains the same number and type of components as the previous converter (SEPIC-not SEPIC), but has the ability to buck and boost the output voltage without polarity

change, as does the SEPIC-buck converter. The SEPIC-buckboost has an inverting buck/boost conversion ratio while the SEPIC-not SEPIC converter has a boost-type conversion ratio. Of these, only the SEPIC-buck and SEPIC-Zeta have smooth input and output current. The total component count for these converters range from twelve to fourteen devices.

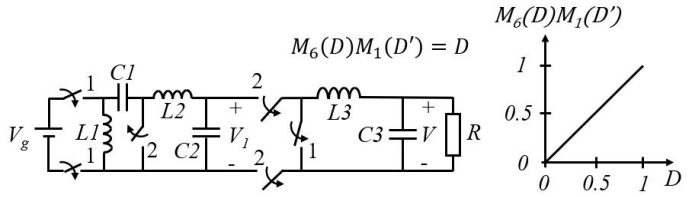
3.4.7 Primary-Side Zeta Architectures

In this subsection we investigate the development of primary-side Zeta dual-cascade AI topologies, as shown in Figure 3.24. The first converter to be considered is the Zeta-not buck converter. The converter has a buck-type conversion ratio and contains six switch devices, three capacitors, and three inductors. The second Zeta-derived converter, the AI Zeta-boost, has a buck/boost conversion ratio and fewer component count due to an internal T-filter reduction. The converter has six switches, two inductors, and two capacitors. The third converter, the Zeta-buckboost, has in inverting buck/boost conversion ratio and after eliminating an extra mode-1 switch contains six switches, three inductors, and three capacitors. The fourth converter in this class, the Zeta-Cuk, does not isolate due to the lack of lateral switches in the second Cuk stage. The fifth converter in this subsection, the Zeta-SEPIC, has a non-inverting buck/boost conversion ratio and a reduced internal T-type filter. This converter contains six switch devices, three inductors, and three capacitors. The sixth and final converter in this class, the Zeta-not Zeta, has a unity conversion ratio regardless of the duty ratio and contains six switch devices, four inductors, and four capacitors.

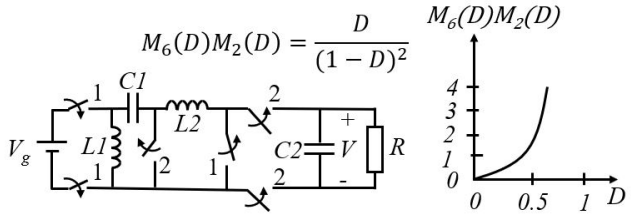
None of the Zeta-architectures have smooth input and output current.

3.4.8 Summary and Comparisons

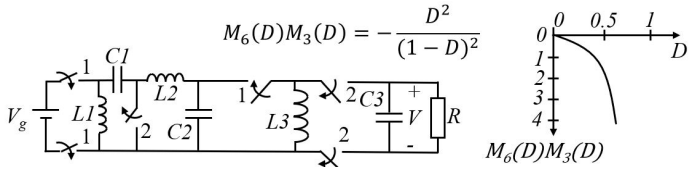
The thirty-six possible dual-cascade AI converters developed in the previous section are listed in Table 3.3. The table includes the architecture, component type and count, smooth input/output current, and conversion ratio. It is found that all con-



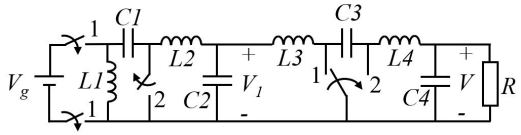
(a) AI Zeta-not buck converter



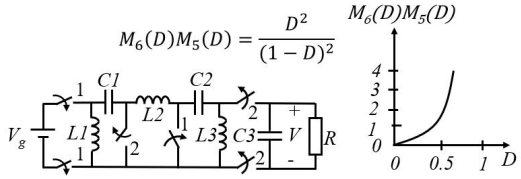
(b) AI Zeta-boost converter



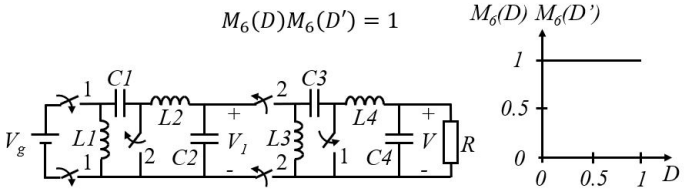
(c) AI Zeta-buckboost converter



(d) Zeta-Cuk (does not isolate)



(e) AI Zeta-SEPIC converter



(f) AI Zeta-not Zeta converter

Figure 3.24: Resultant AI primary-side Zeta converters and corresponding conversion ratio equations with plots

verter topologies have six switches except the inverting buck-boost converter (index 3). This converter has pulsating input/output current. Among the four converters

that have smooth input/output current, the boost-buck (index 2-1) has the fewest component count. These two converters (inverting buck-boost and boost-buck) are deemed "optimal" converters since they require the fewest components with pulsating and non-pulsating current. These converters are described in detail with theoretical calcuations and experimental data given in [32].

The non-inverting buck-boost converter (index 1-2) has the next fewest component count with only eight components required with pulsating input/output current. However, the inverting buck-boost (index 3) has two fewer components for the same functionality. Nine converters do not isolate without the addition of extras switches. Ten converter topologies require ten total components with six switches, two inductors, and two capacitors. Of these ten, three are good for applications that require very low conversion ratios (since $M(D) = \pm D^2/D'$), three are good for applications that require very high conversion ratios (since $M(D) = \pm D/D'^2$), and one is good for applications requiring both high and low conversion ratios (since $M(D) = D^2/D'^2$). The remaining converters contain a total of twelve or fourteen components with no known added benefits.

3.4.9 Discussion

In this section, dual-cascade combinations of the six basic converter topologies (buck, boost, buck-boost, Cuk, SEPIC, and Zeta) were developed. After filter reduction of the resultant typologies and evaluation for isolation capabilities, the converters were analyzed and compared based on component count and conversion ratio. A detailed table (Table 3.3) was generated to aid in the comparison. It was discovered that none of the newly developed topologies were better than the two previously analyzed AI boost-buck (index 2-1) and AI inverting buck-boost (index 3) topologies given in [32] which are deemed "optimum" active isolated topologies. This being that case, no simulation or prototyping of the new topologies has been performed as these new topologies are not better than the two previously studied.

Table 3.3: Summary of dual-cascade AI converters as listed in Table 3.2

Conv Index	**Con Name**	**Conv Arch**	**# SWs**	**# Ls**	**# Cs**	**# Cmp**	**Con Cur**	**Conv Ratio**
1-1	bk-not bk	VI-VI	6	2	2	10		DD'
1-2	bk-bst	VI-IV	6	1	1	8		D/D'
1-3	bk-bkbst	VI-VV	6	2	2	10		D^2/D'
1-4	bk-Cuk	VI-II	N/A	N/A	N/A	N/A	N/A	N/A
1-5	bk-SEPIC	VI-IV	6	2	2	10		D^2/D'
1-6	not bk-Zeta	VI-VI	6	3	3	12		D
2-1	bst-bk*	IV-VI	6	2	2	10	$\surd$	D/D'
2-2	bst-not bst	IV-IV	6	2	2	10		$1/DD'$
2-3	bst-bstbk	IV-VV	6	2	2	10		$-D/D'^2$
2-4	bst-Cuk	IV-II	N/A	N/A	N/A	N/A	N/A	N/A
2-5	not bst-SEP	IV-IV	6	3	3	12		$1/D'$
2-6	bst-Zeta	IV-VI	6	3	3	12	$\surd$	D/D'^2
3	inv. bkbst**	VV	4	1	1	6		$-D/D'$
3-1	buckbst-bk	VV-VI	6	2	2	10		$-D^2/D'$
3-2	bkboost-boost	VV-IV	6	2	2	10		$-D/D'^2$
3-3	bkbst-bkbst	VV-VV	6	2	2	10		D^2/D'^2
3-4	bkbst-Cuk	VV-II	6	3	3	12		D^2/D'^2
3-5	bkbst-SEPIC	VV-IV	6	3	3	12		$-D^2/D'^2$
3-6	bkbst-Zeta	VV-VI	6	3	3	12		$-D^2/D'^2$
4-1	Cuk-bk	II-VI	N/A	N/A	N/A	N/A	N/A	N/A
4-2	Cuk-bst	II-IV	N/A	N/A	N/A	N/A	N/A	N/A
4-3	Cuk-bkbst	II-VV	6	3	3	12		D^2/D'^2
4-4	Cuk-Cuk	II-II	N/A	N/A	N/A	N/A	N/A	N/A
4-5	Cuk-SEPIC	II-IV	N/A	N/A	N/A	N/A	N/A	N/A
4-6	Cuk-Zeta	II-VI	N/A	N/A	N/A	N/A	N/A	N/A
5-1	SEPIC-buck	IV-VI	6	3	3	12	$\surd$	D^2/D'
5-2	SEPIC-not bst	IV-IV	6	3	3	12		$1/D'$
5-3	SEPIC-bkbst	IV-VV	6	3	3	12		$-D^2/D'^2$
5-4	SEPIC-Cuk	IV-II	N/A	N/A	N/A	N/A	N/A	N/A
5-5	SEP-notSEP	IV-IV	6	4	4	14		1
5-6	SEPIC-Zeta	IV-VI	6	4	4	14	$\surd$	D^2/D'^2
6-1	Zeta-not buck	VI-VI	6	3	3	12		D
6-2	Zeta-bst	VI-IV	6	2	2	10		D/D'^2
6-3	Zeta-bkbst	VI-VV	6	3	3	12		$-D^2/D'^2$
6-4	Zeta-Cuk	VI-II	N/A	N/A	N/A	N/A	N/A	N/A
6-5	Zeta-SEPIC	VI-IV	6	3	3	12		D^2/D'^2
6-6	Zeta-notZeta	VI-VI	6	4	4	14		1

Notes: * Optimal converter w/ smooth current[32]
** Optimal converter w/ min. comp. count[32]

CHAPTER 4: MODELING AND ANALYSIS

4.1 Introduction

It was shown in the previous section that the four basic cascaded converters reduce to two actively isolated converters: the boost-buck and buck-boost. The boost-buck converter is the focus of this section since it has properties that approach an ideal DC transformer– smooth input and output current.

4.2 Boost-Buck

As shown in the previous section, the non-inverting boost-buck and inverting boost-buck (Cuk) converters reduce to the active isolated boost-buck converter. The ideal (lossless) model of the active isolated boost-buck converter is similar to that given in [27] for the Cuk converter except with additional losses due to added low-side isolation switches.

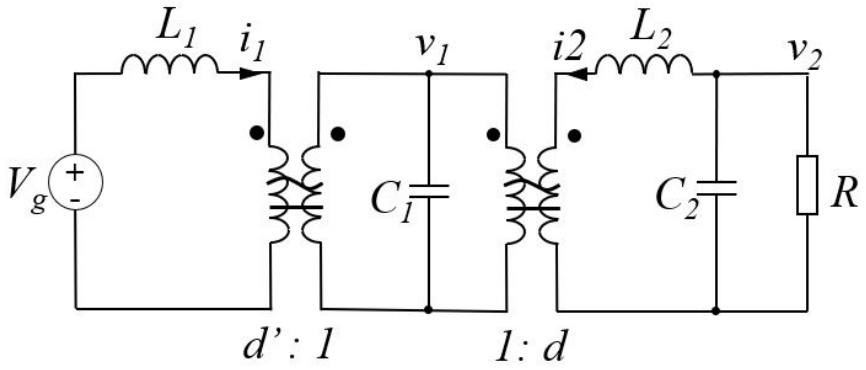


Figure 4.1: Ideal (lossless) average model of active isolated boost-buck converter

The ideal averaged circuit model for the converter is shown in Figure4.1, with corresponding model parameters given as:

$$V_2/V_g = d/d',\ d' = 1 - d \tag{4.1}$$

$$V_2/V_1 = d \tag{4.2}$$

$$I_2/I_1 = d'/d \tag{4.3}$$

$$V_2/I_2 = R \tag{4.4}$$

4.2.1 Lossless Average linearized Circuit Model of Active Isolated Boost-Buck Converter

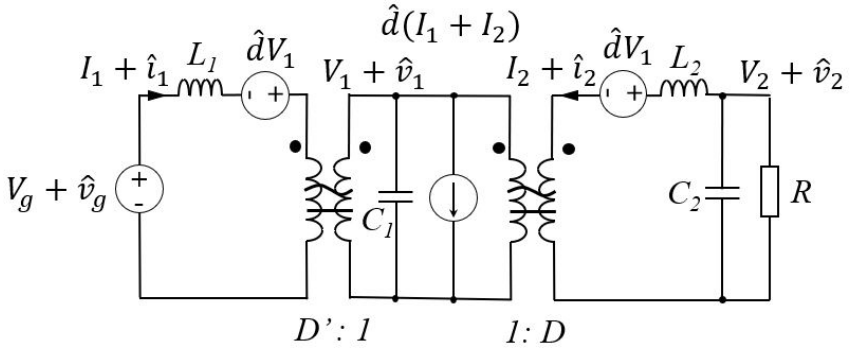


Figure 4.2: Ideal average linear circuit model of active isolated boost-buck converter

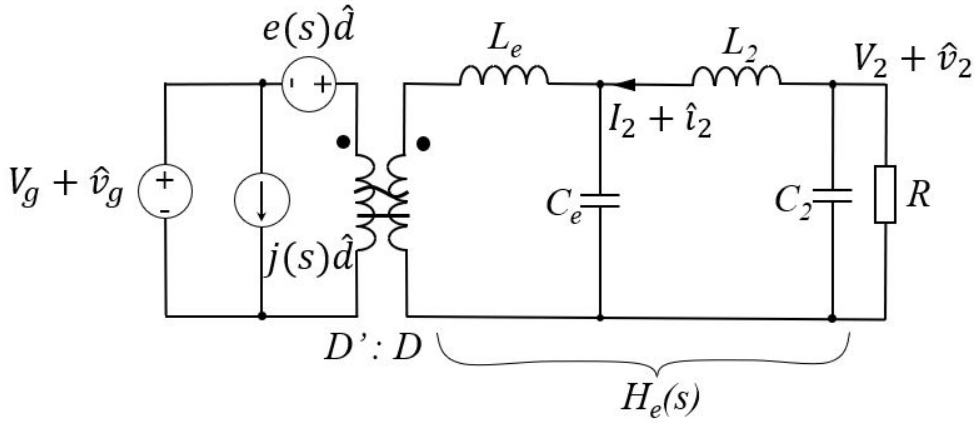


Figure 4.3: Ideal average linearized canonical model of active isolated boost-buck converter

After perturbation and linearization, the circuit in Figure 4.2 is obtained. Through equivalent circuit transformations and DC relations, the *ideal average linear circuit model* can be transformed into the canonical circuit form as shown in Figure 4.3 with model parameter values defined as follows:

$$L_e = (D/D')^2 L_1 \tag{4.5}$$

$$C_e = C_1/D^2 \tag{4.6}$$

$$j(s) = \frac{V_2}{D'^2 R}(1 - sC_e R D') \tag{4.7}$$

$$e(s) = \frac{V_2}{D^2}(1 - s\frac{L_e}{R} + s^2 L_e C_e D') \tag{4.8}$$

$$H_e(s) = \frac{1}{P_1(s) + P_2(s)} \tag{4.9}$$

$$P_1(s) = 1 + \frac{L_e + L_2}{R}s + (L_e C_e + L_2 C_2 + L_e C_2)s^2 \tag{4.10}$$

$$P_2(s) = \frac{C_e L_e L_2}{R}s^3 + L_e C_e L_2 C_2 s^4 \tag{4.11}$$

If $C_e >> C_2$ and $C_e >> L_2/R^2$, then $P_1(s) + P_2(s)$ can be approximated as:

$$P_1(s) + P_2(s) = (1 + \frac{L_e}{R}s + L_e C_e s^2)(1 + \frac{L_2}{R}s + L_2 C_2 s^2) \tag{4.12}$$

Which has the following corner frequencies and Q factors:

$$f_{C1} = \frac{1}{2\pi\sqrt{L_e C_e}}, \quad Q_1 = \frac{R}{\omega_{C1} L_e} \tag{4.13}$$

$$f_{C2} = \frac{1}{2\pi\sqrt{L_2 C_2}}, \quad Q_1 = \frac{R}{\omega_{C2} L_2} \tag{4.14}$$

Using the converter parameters listed in Table 4.1, the circuit in Figure 4.3 is used to plot the output to input relationship using MATLAB as seen in Figure 4.4.

4.2.2 Canonical Circuit Model with Parasitic Resistances

The previous loss-less models were useful for ideal conversion ratios and frequency analysis of the converter. To obtain practical conversion ratio and efficiency, inductor winding resistance, switch R_{DSon}, and wire resistance are included in the final canon-

Table 4.1: Active Isolated Boost-Buck Converter Parameters

Ref. Des.	Value
V_g	5V
L_1, L_2	0.5mH
R_{L1}, R_{L1}	0.1Ω
R_{w1}, R_{w2}	0.1Ω
C_1	$47\mu F$
C_2	$1\mu F$
R	10Ω
f_{sw}	$50kHz$

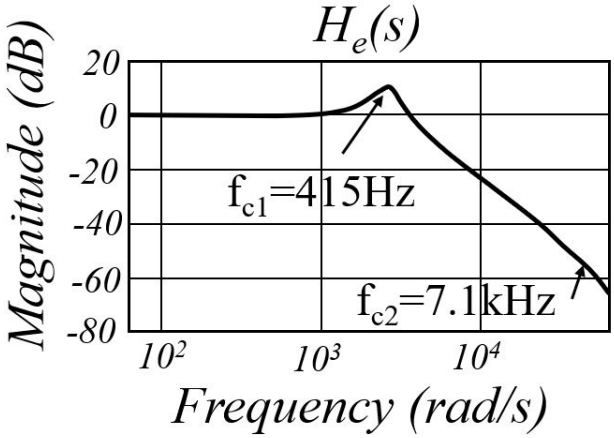


Figure 4.4: Bode plot of isolated buck-boost converter using parameters from Table 4.1 showing dominant pole at f_{C1}

ical circuit model of the active isolated boost-buck converter, as shown in Figure 4.5.

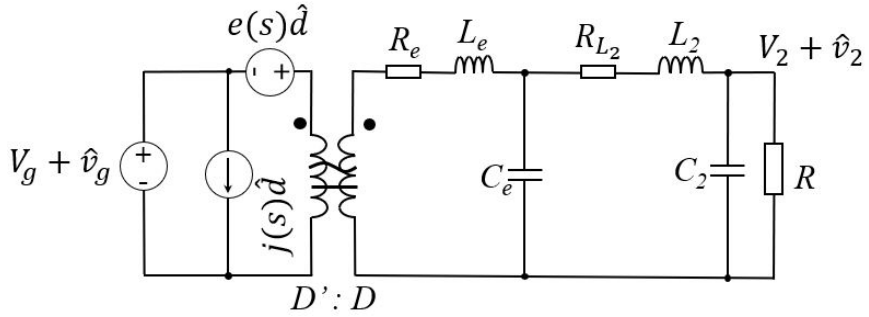


Figure 4.5: Average linearized canonical model with parasitic switch Rds_{on} resistance and inductor winding resistance included

The passive component value definitions remain the same except for the new re-

flected equivalent resistance from the primary side given as:

$$R_e = (D/D')^2 R_{L1}. \tag{4.15}$$

The dependent sources of the model are modified by the addition of the parasitic resistances as follows:

$$j(s) = \frac{V_2}{D'^2 R}[1 - sC_e R D'(1 + \frac{R_{L2}}{R})] \tag{4.16}$$

$$e(s) = \frac{V_2}{D^2}(1 + \frac{R_{L2} - R_e}{R} - s(\frac{L_e}{R} - A) + s^2 L_e C_e D' B) \tag{4.17}$$

Where, $A = R_e C_e D'(1 + R_{L2}/R)$ and $B = 1 + R_{L2}/R$

From the circuit model in Figure 4.5, loss-based conversion equations are given by:

$$\frac{I_2}{I_g} = D'/D \tag{4.18}$$

$$M(D) = \frac{V_2}{V_g} = \frac{D}{D'} \frac{1}{1 + \frac{R_{L1}}{R}(\frac{D}{D'})^2 + \frac{R_{L2}}{R}} \tag{4.19}$$

If we denote η as the converter efficiency, then Equation 4.19 can be rewritten as:

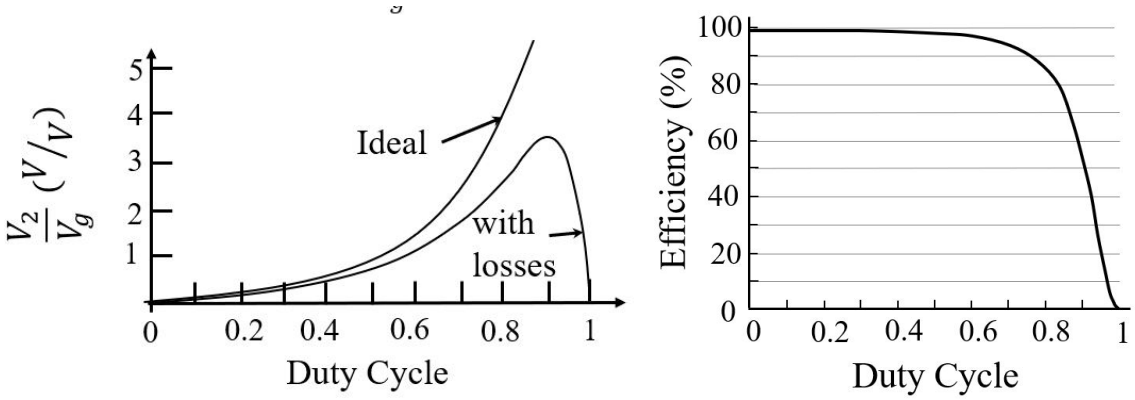
$$M(D) = \frac{V_2}{V_g} = \frac{D}{D'}\eta \tag{4.20}$$

The converter efficiency is then given by:

$$\eta = \frac{1}{1 + \frac{R_{L1}}{R}(\frac{D}{D'})^2 + \frac{R_{L2}}{R}} \tag{4.21}$$

If the converter parameters from Table 4.1 are used, the output to input gain and efficiency can be plotted as shown in Figure 4.6a and Figure 4.6b, respectively.

It is worth mentioning that the addition of parasitic loss components has negligible



(a) Plot comparing ideal versus loss-based conversion ratio

(b) Plot of efficiency vs. duty cycle

Figure 4.6: Plots of conversion ratio and efficiency using derived equations for parameters listed in Table 4.1

effect on the converter frequency transfer function since $R_{L1} << R$ and $R_{L2} << R$. In this case, the controlled voltage source definition simplifies to the following:

$$e(s) = \frac{V_2}{D^2}[1 - s(\frac{L_e}{R} - R_e C_e D') + s^2 L_e C_e D')] \tag{4.22}$$

The two complex zeros become left half-plane zeros if $L_e/R - R_e C_e D' < 0$. The location of the zero is then:

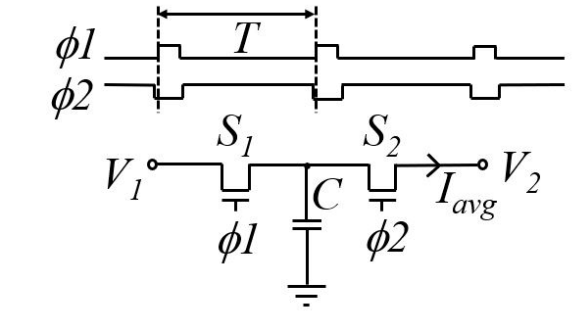
$$f_{z1} = \frac{1}{2\pi\sqrt{L_e C_e D'}} \tag{4.23}$$

The zero at f_{z1} almost completely cancels f_{c1} since they are close together, thus giving a second-order response with effective complex poles at $f_c 2$[27].

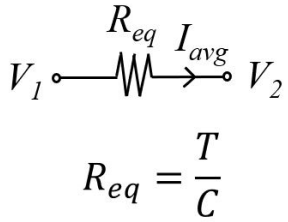
4.3 Buck-Boost

Of the two unipolar active isolated converters shown in Figure 5.9, the unipolar buck-boost converter shown in Figure 5.9a has the lowest device count and is simplest in operation. The averaged *differential-mode* canonical model of this converter is given in [27]. The goal of this section is to develop an averaged *differential-* and *common-mode* model of the unipolar buck-boost converter. This averaged model can be used to ensure compliance with applicable equipment standards such as UL2202,

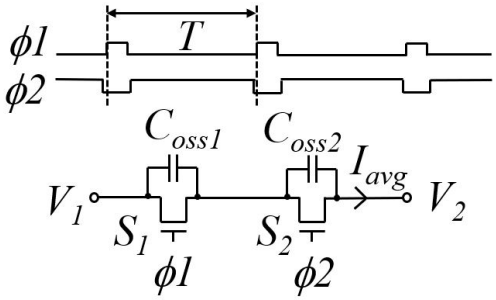
IEC60950, IEC60950-1, VDE 0126-1-1, and VDE-AR-N 4105 [7, 5, 6, 2, 3].



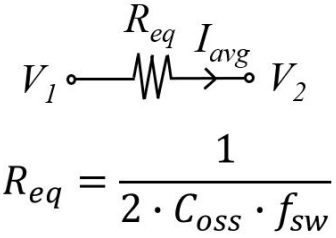
(a) Switched-capacitor circuit



(b) Resistor equivalent circuit



(c) Active isolated switch circuit



(d) Active isolation barrier resistor equivalent

Figure 4.7: Averaged resistor equivalence of switched circuits

To begin, we determine the equivalent resistance of the parasitic switch output capacitors C_{ossN}. A basic switched-capacitor circuit, commonly used in analog integrated circuit design, is shown in Figure 4.7. The forward charge transfer per clock cycle is given by:

$$\Delta Q = C(V_1 - V_2). \tag{4.24}$$

The averaged resistor equivalence of Figure 4.7a is shown in Figure 4.7b [40]. The

value of the equivalent resistance is

$$R_{eq} = \frac{T}{C}. \tag{4.25}$$

Where the average current through the equivalent resistance is

$$I_{avg} = \frac{V_1 - V_2}{R_{eq}}. \tag{4.26}$$

Substituting for R_{eq} results in

$$I_{avg} = \frac{C(V_1 - V_2)}{T}. \tag{4.27}$$

And substituting $T = \frac{1}{f_{sw}}$ into this equation for R_{eq} gives

$$R_{eq} = \frac{T}{C} = \frac{1}{Cf_{sw}}. \tag{4.28}$$

The switched circuit of the active isolation barrier of a buck-boost converter is shown in Figure 4.7c. The forward charge transfer per cycle is given by

$$\Delta Q = C_{oss1}(V_1 - V_2) + C_{oss2}(V_1 - V_2). \tag{4.29}$$

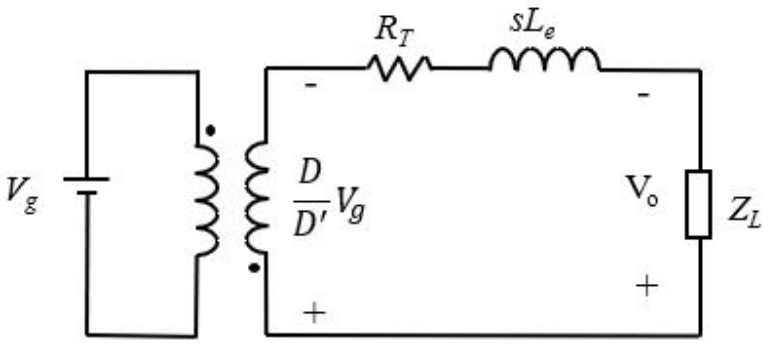
Assuming $C_{oss} = C_{oss1} = C_{oss2}$, this equation reduces to

$$\Delta Q = 2C_{oss}(V_1 - V_2). \tag{4.30}$$

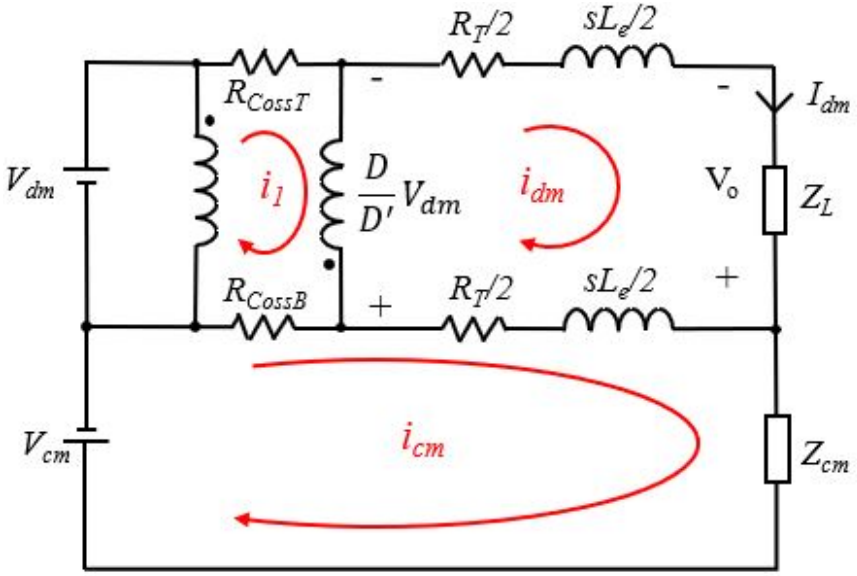
The averaged active isolation resistor equivalence of Figure 4.7c is shown in Figure 4.7d. The value of the equivalent resistance in terms of the switching frequency is

$$R_{eq} = \frac{1}{2C_{oss}f_{sw}}. \tag{4.31}$$

The result in Equation 4.31 is used to develop the averaged switch model of the active isolation buck-boost converter. The *differential-mode* model of a buck-boost converter is shown in Figure 4.8a [27]. Figure 4.8b shows the proposed averaged *differential- and common-mode* model of the active isolated buck-boost converter.



(a) Buck-boost averaged differential-mode model[27]



(b) Proposed buck-boost averaged differential- and common-mode model

Figure 4.8: Buck-boost averaged models

The parameters for the model in Figure 4.8b are:

$$R_{CossT} = \frac{1}{2C_{ossT}f_{sw}} \tag{4.32}$$

$$R_{CossB} = \frac{1}{2C_{ossB}f_{sw}} \tag{4.33}$$

$$Z_L = \frac{1}{sC}//R_L \tag{4.34}$$

$$L_e = \frac{L}{D'^2} \tag{4.35}$$

$$R_T = (\frac{D}{D'})^2 Re_1 + \frac{1}{D'} Re_2 \tag{4.36}$$

$$Re_1 = R_{ds1} + R_{ds2} + R_l \tag{4.37}$$

$$Re_2 = R_l + R_{ds3} + R_{ds4} \tag{4.38}$$

Circuit mesh analysis on Figure 4.8b and solving for i_{cm} results in the following averaged linear equation:

$$i_{cm} = \frac{A + B}{C - D}. \tag{4.39}$$

Where,

$$A = R_{CossB}(V_{dm} + \frac{D}{D'}V_{dm}) \tag{4.40}$$

$$B = (R_{CossT} + R_{CossB})[\frac{R_T + sL_e}{2} i_{dm} - V_{cm}] \tag{4.41}$$

$$C = (R_{CossT} + R_{CossB})(R_{CossB} + \frac{R_T + sL_e}{2} + Z_{cm}) \tag{4.42}$$

$$D = {R_{CossB}}^2 \tag{4.43}$$

If $R_{CossB} = R_{CossT} = R_{Coss}$, then Equation 4.39 simplifies to the following:

$$i_{cm} = \frac{V_{dm} + \frac{D}{D'}V_{dm} + (R_T + sL_e)i_{dm} - 2V_{cm}}{(R_{Coss} + R_T + sL_e + 2Z_{cm})}. \tag{4.44}$$

To obtain a practical approximation for the differential-mode current (i_{dm}), i_{cm} is set to zero (since in practice $i_{cm} \ll i_{dm}$) which gives us:

$$i_{dm} = \frac{\frac{D}{D'}V_{dm}}{sL_e + Z_L + R_T}. \tag{4.45}$$

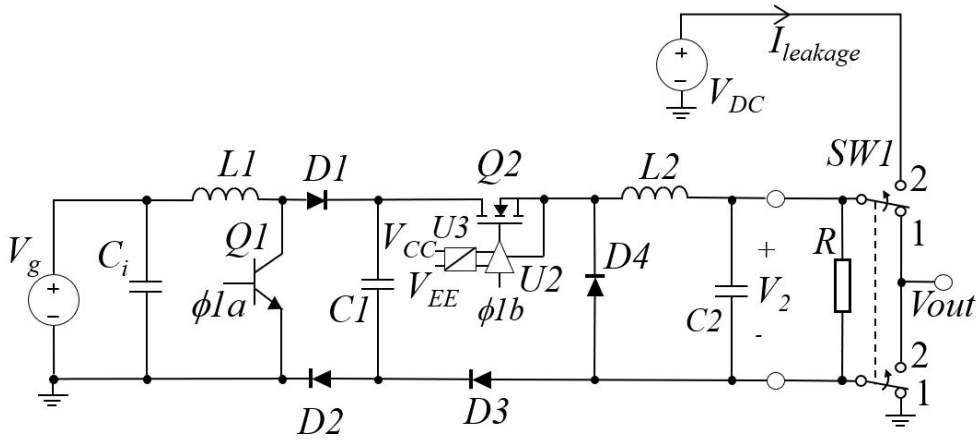
Together, Equation 4.44 and Equation 4.45 can be used to determine voltages and currents of interest in the active isolated buck-boost converter when used in various applications. In this section, they are used to determine the ground leakage current (common-mode current) and ground voltage potential in a PV microinverter system. Based on these equations, devices should be selected to minimize the parasitic output capacitance (C_{oss}) of the isolation switches. As such, GaN devices are used for the converters in this dissertation (since they have relatively low C_{oss} values) to develop prototypes for experimental testing, as seen in the following section.

4.4 Experimental Validation

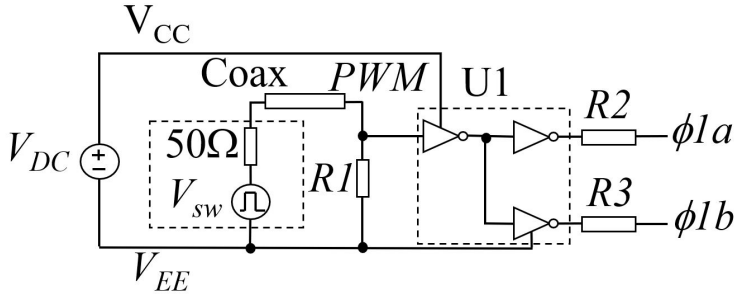
This section contains simulation and experimental results of the boost-buck active isolated converter in both uni-polar (partially-isolated) and bi-polar (fully-isolated) operation. The uni-polar converter is demonstrated in a half-bridge inverter application.

4.4.1 Uni-polar Active Isolated Boost-Buck Converter

A uni-polar active isolated boost-buck converter is able to operate in such a way that its output voltage can float relative to the input ground in only one direction. This is useful in several different practical applications– including active rectifiers and inverters. The circuit for the converter is given in Figure 4.9 with circuit parameters listed in Table 4.2.



(a) Power stage and test switches



(b) Clock generation

Figure 4.9: Schematic and test setup for realization of uni-polar active isolated boost-buck converter with circuit parameter values given in Table 4.2

Table 4.2: Unipolar Active Isolated Boost-Buck Converter Parameters for Figure 4.9

Ref. Des.	**Value**
Q_1	2N3904
Q_2	PSMN5R0-80PS
$D_1 - D_4$	1N5818
$U1$	74LS04
$U2$	HCPL 3180
$U3$	PDS1-S24-S15-S
R	200 Ω
C_i	47 μF
C_1	10 μF
C_2	1 μF
V_g	5V
L_1, L_2	$0.5mH$
f_{sw}	50 kHz
duty cycle	0.6

The switch, SW1, is able to operate in position 1 or 2 with leakage current, $I_{leakage}$ measured less than a few milliamps. The converter was tested with offset voltage, V_{DC}, set at 0 to 4V for both switch positions. Figure 4.10 shows the converter operating with SW1 in position 2 with $V_{DC} = 2V$. The ideal expected result is -5.5V with the actual output operating at just under -5V due to converter losses.

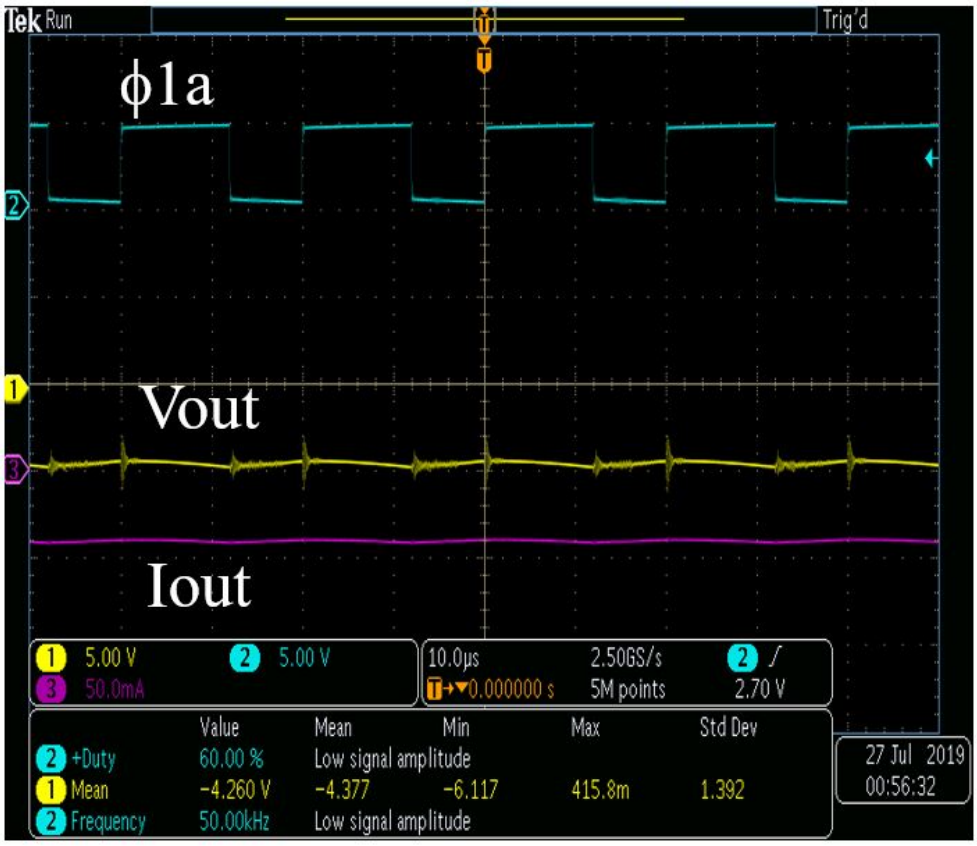


Figure 4.10: Oscilloscope capture of unipolar boost buck with switch SW1 in position 2 with $V_{DC} = 2V$ showing the converter output operating at the expected value of just under -5V.

4.4.2 Uni-polar Active Isolated Boost-Buck Converter in Inverter Application

The uni-polar boost-buck converter shown in Figure 4.9 is used in a mid-point biased inverter half-bridge circuit to demonstrate the converter's ability to float in one direction, as can be seen in Figure 4.11. The parameters for this inverter are listed in Table 4.3. As seen in Figure 4.11a, the uni-polar boost-buck is used to

create a mid-point grounded dual supply (V+ and V-) for the inverter half-bridge. The duty cycle is set to output a 24V signal that is level shifted down by 12V by the capacitor divider C1 and C2. This allows diodes D2 and D3 of Figure 4.9a to always remain reversed biased. The 555 timer is used to generate the 715Hz square wave to drive the half-bridge inverter. The circuit is simulated with SiMetrix SPICE software and expected results are shown in Figure 4.11b. The experimental results, shown in Figure 4.11c, confirm proper operation of the inverter.

Table 4.3: Inverter Circuit Parameters of Figure 4.11a

Ref. Des.	**Value**
Q_1	2N3904
Q_2	PSMN5R0-80PS
$D_1 - D_4$	1N5818
$U1$	74LS04
$U2$	HCPL 3180
$U3$	PDS1-S24-S15-S
R	200 Ω

4.4.3 Bi-polar Active Isolated Boost-Buck Converter

To demonstrate the full capabilities of active isolation, a bi-polar (fully isolated) boost-buck active isolated converter is prototyped and tested, as shown in Figure 4.12. The circuit diagram consists of five bidirectional series-connected switches S2-S6 and one unidirectional switch S1, as shown in Figure 4.12a. Inductor current in L1 is increased by turning on S1. The non-overlapping clock generation circuit shown in Figure 4.12b ensures that S1 and S2 are not closed at the same time. During the S1 and S2 commutation dead-time, the voltage across the output capacitance of S1 will increase and will cause the device to avalanche protect if this time is too long. The deadtime control circuit is designed to provide a minimum deadtime so the device will not go into avalanche protection. The deadtime is set at 280ns with the 100Ω resistors (R1-R2) and 330pF capacitors (C3-C4). The deadtime may be adjusted by changing C3-C4. The same commutation strategy is used for S4 and S6 for output

inductor L2.

Table 4.4: Bi-polar Active Isolated Boost-Buck Converter Parameters

Ref. Des.	**Value**
V_g	5V
C_i	$200\mu F$
C_1	$47\mu F$
C_2	$1\mu F$
$C_3 - C_4$	$330pF$
L_1, L_2	0.5mH
R	10Ω
$R1 - R2$	100Ω
$S1 - S6$	PSMN5R0-80PS
f_{sw}	$50kHz$
duty cycle	0.6
U1	74LS02
U2	74LS244
U3-U8	HCPL 3180
V_{sw}	10V
V_1	-20V to 20V

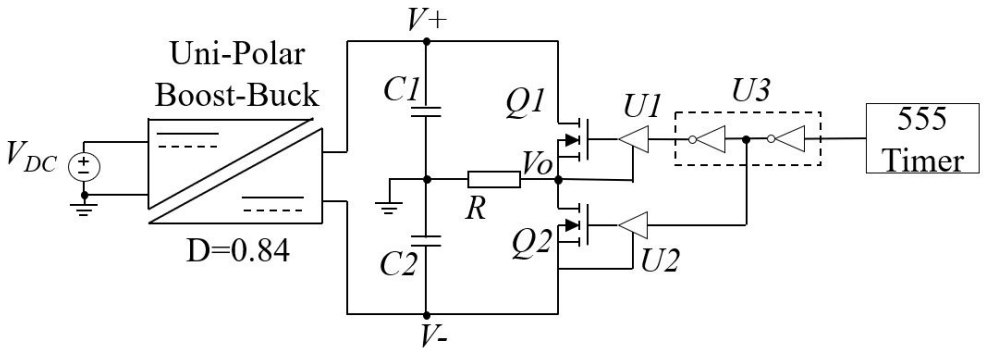
The *Printed Circuit Board* (PCB) is shown in Figure 4.12c. As seen, the design does not contain any consideration for heat sinks. As such, the steady-state power of this prototype is limited to 15W.

To test for isolation capabilities, the voltage source V1 was adjusted from +20V to -20V demonstrating the ability of the output voltage to float relative to the input. The results shown in Figure 4.13a verify proper operation of the positive voltage isolation from input to output, whereas results in Figure 4.13b verify proper operation of the negative voltage isolation.

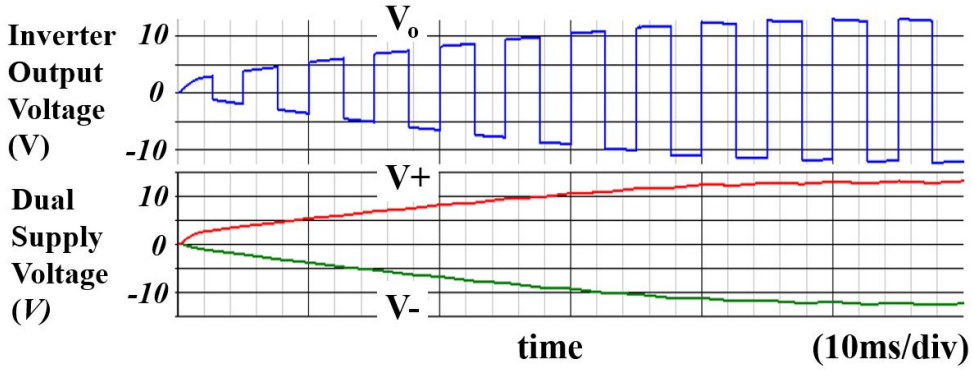
Empirical data collected for the converter was shown to match the conducted efficiency model given in Equation 4.19 as shown in Figure 4.14a and 4.14b.

The leakage current for the converter was measured for increasing isolation voltage and is found to be proportional to isolation votlage, as shown in Figure 4.14c. The leakage current was also measured with increasing switching frequency, as shown in Figure 4.14d, and is seen to be proportional to switching frequency. This is consistent

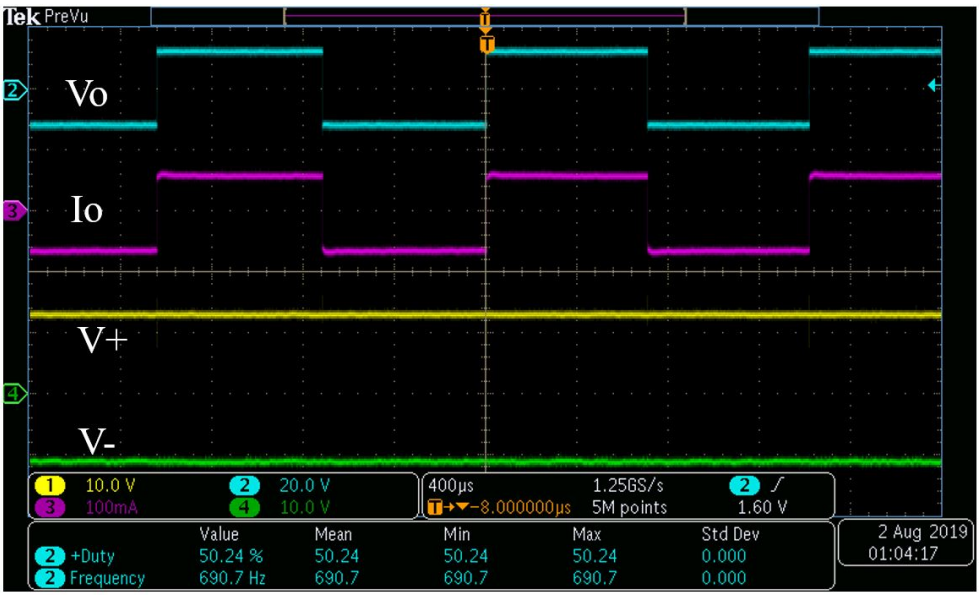
with expected results as in [22].



(a) Schematic of active isolated converter used to create +/-12V dual supplies for use in inverter application with circuit parameter listed in 4.3.

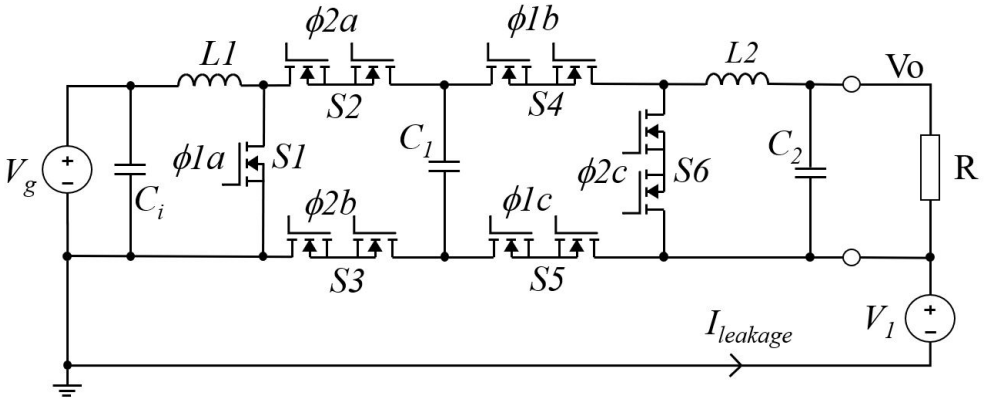


(b) Simulation (using SiMetrix) of active isolated converter used to create +/-12V dual supplies for use in inverter application.

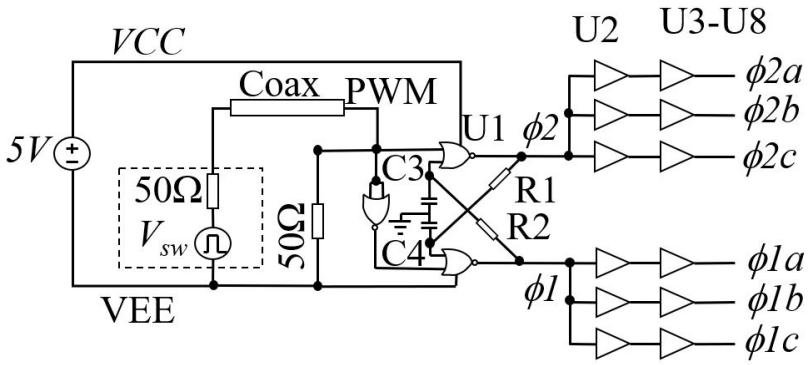


(c) Experimental waveform with Ch1: +12V DC, Ch2: Output voltage, Ch3: Output current, Ch4: -12V DC

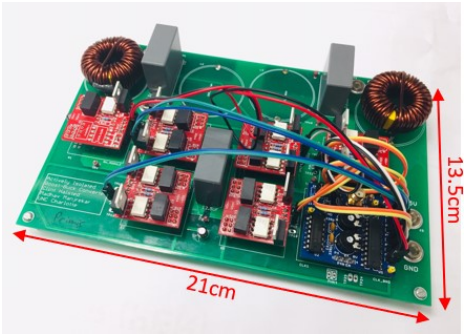
Figure 4.11: Schematic diagram and experimental waveform of active isolated boost-buck converter used in inverter application



(a) Power stage schematic diagram and test setup of bi-polar active isolated boost-buck converter.

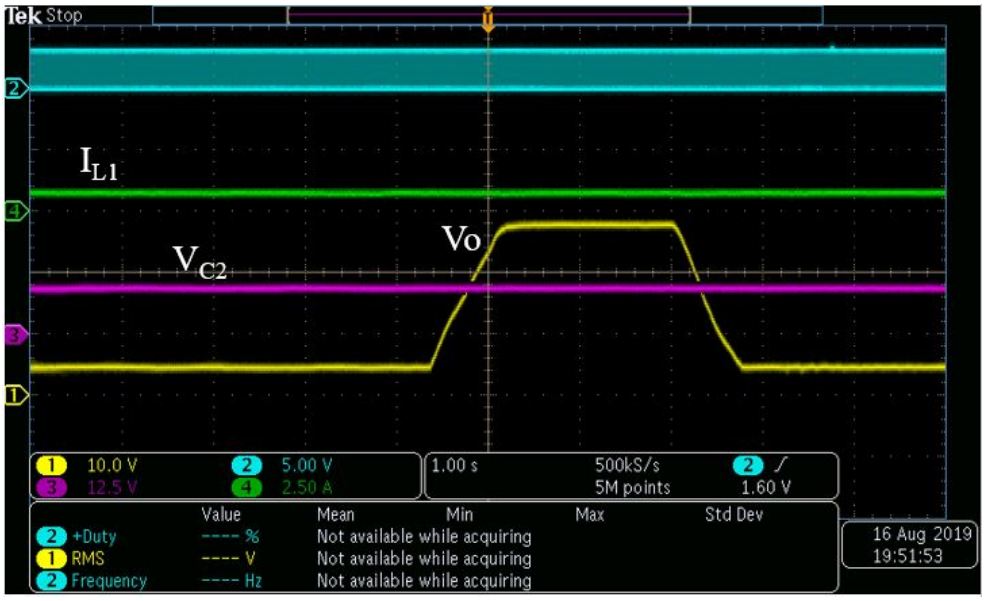


(b) Non-overlapping clock generation schematic diagram

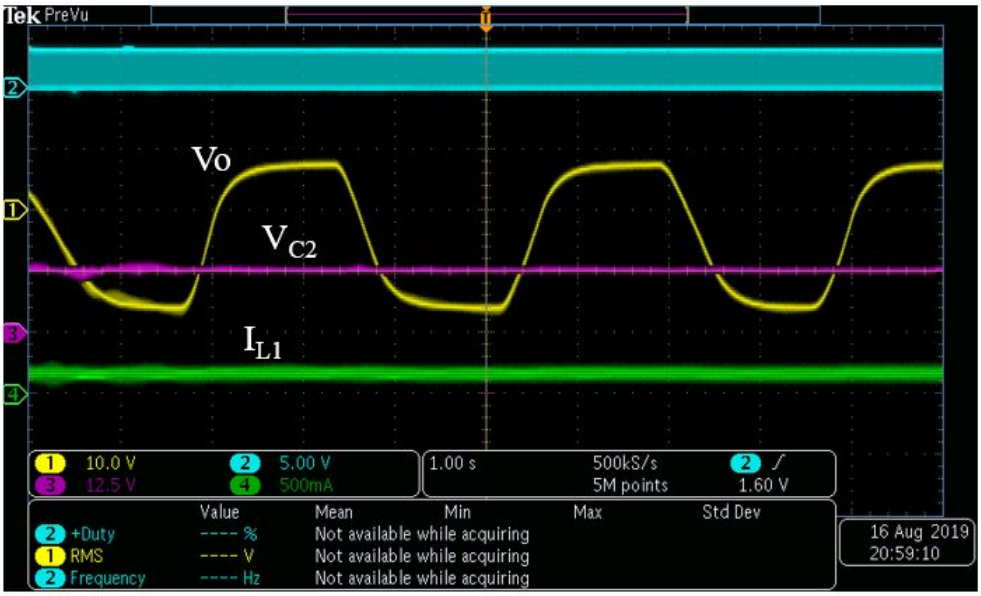


(c) 15W PCB prototype

Figure 4.12: Schematic and test setup for realization of fully active isolated boost-buck converter with circuit parameter values listed in Table 4.4.

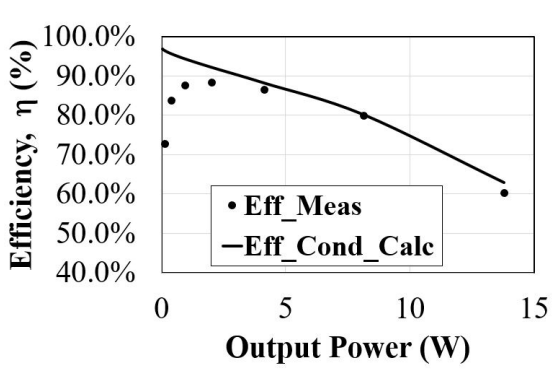


(a) Isolated voltage V1 varied from 0 to +20V: Ch1: Output voltage V_o, Ch2: PWM, Ch3: internal boost voltage V_{C2}, and Ch4: inductor current I_{L1}

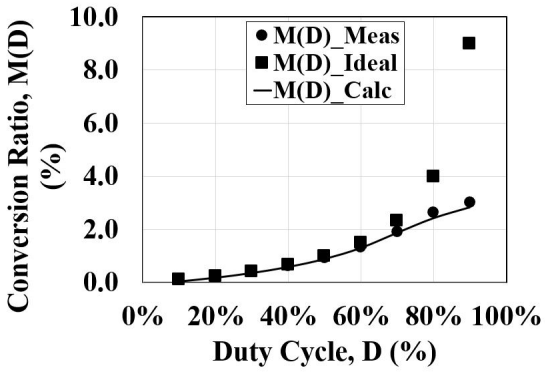


(b) Isolated voltage V1 varied from 0 to -20V: Ch1: Output voltage V_o, Ch2: PWM, Ch3: internal boost voltage V_{C2}, and Ch4: inductor current I_{L1}

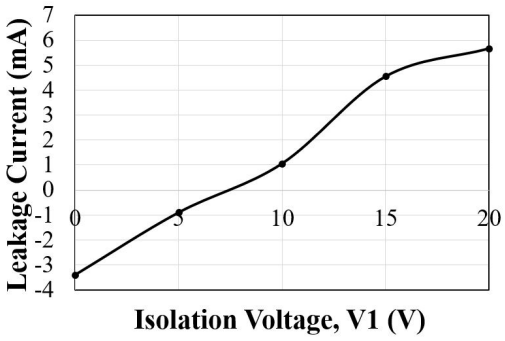
Figure 4.13: Experimental waveforms of prototype active isolated boost-buck



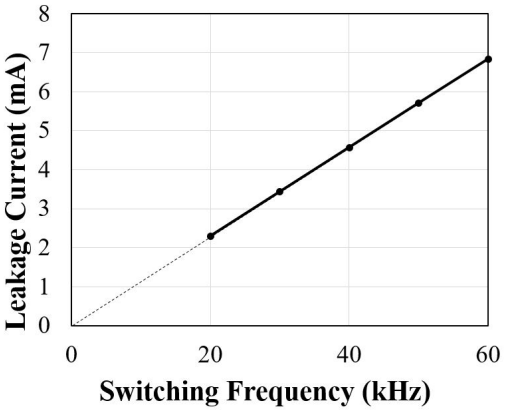
(a) Efficiency vs. output power with R=4Ω to 113Ω.



(b) Conversion ratio vs. duty cycle



(c) Isolation leakage current vs. isolation voltage shows a linear relationship



(d) Isolation leakage current vs. switching frequency shows a linear relationship

Figure 4.14: Experimental waveforms of prototype active isolated boost-buck for circuit values listed in Table 4.4

CHAPTER 5: APPLICATIONS

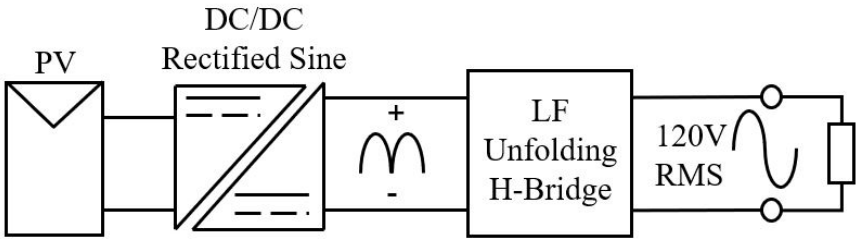
5.1 Introduction

This chapter presents two applications of active isolated converters using the two optimal topologies: buck-boost and boost-buck AI converters. Section 5.2 covers the use of unipolar AI buck-boost converter in our patented common-ground PV microinverter application and section 5.3 uses the unipolar AI buck-boost converter in AC/DC power adapter for laptop computer applications with integrated fault protection [28].

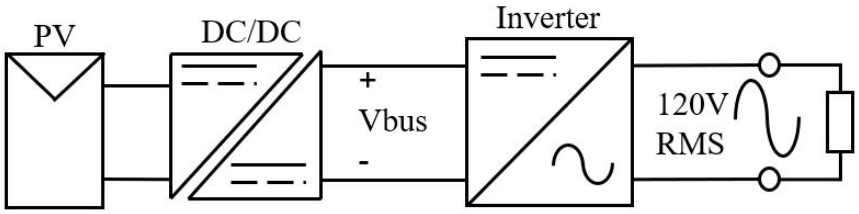
5.2 Photovoltaic Microinverter

In microinverter applications, two conventional approaches to the converter topology are single-stage with unfolding bridge and two-stage, as shown in Figure 5.1. Single-stage refers to the fact that the boosting and wave shaping are performed in a single-stage, whereas, the two-stage approach requires two converters to perform the same operation [29]. The single-stage design consists of an isolated DC/DC rectified sine wave converter utilizing an unfolding bridge that operates at line frequency (LF). The two-stage microinverter consists of an isolated DC/DC converter followed by an inverter.

In both topologies, a high-frequency (HF) transformer is often used to provide galvanic isolation which improves safety without the need for a bulky line-frequency transformer[10]. A more detailed diagram of a two-stage design utilizing a full-bridge (FB) inverter is shown in Figure 5.2a. As shown, the photovoltaic (PV) module is allowed to float but the frame is grounded as required by various standards [30]. The equivalent model in Figure 5.2b includes a parasitic PV capacitance (C_{PV}) (approxi-



(a) Single-stage with unfolding bridge

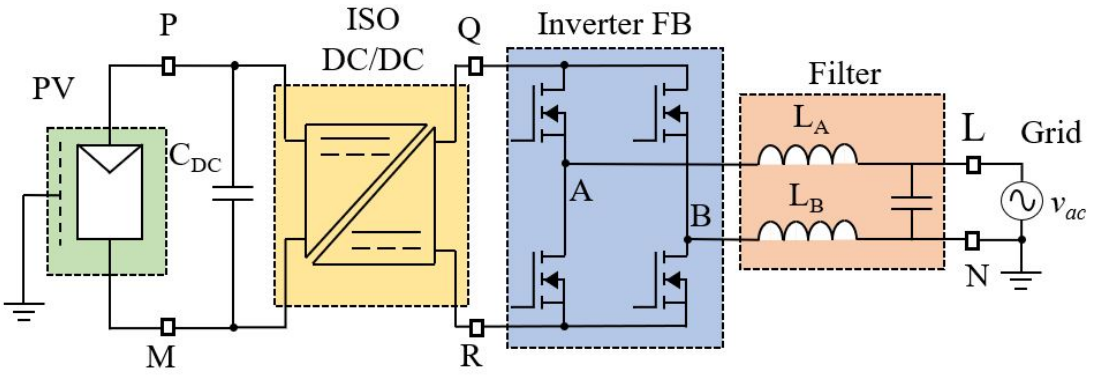


(b) Two-stage

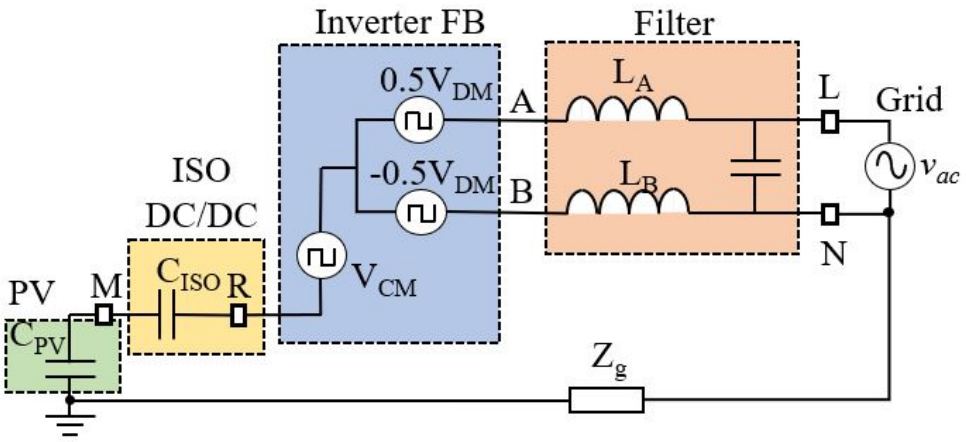
Figure 5.1: Traditional Microinverter Topologies

mately 7nF per installed PV kW [30]) and parasitic transformer winding capacitance (C_{ISO}) (about 16pF or less for flyback transformers [41]) along with the effective common-mode voltage (V_{CM}) and differential-mode voltage (V_{DM}) model of the inverter. As seen in Figure 5.2c, the common-mode current (i_{CM}) is effectively eliminated by the isolation stage due to the high reactance of C_{ISO} around the ground loop.

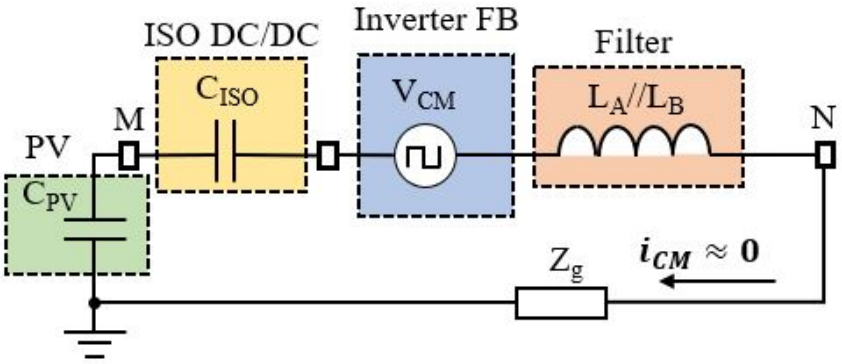
In the case of non-isolated converter topologies, the parasitic PV capacitance (C_{PV}) combined with the inverter effective common-mode voltage (V_{CM}) and filter inductance ($L_A//L_B$) results in a resonant ground loop path that produces a common-mode current (i_{CM}), as seen in Figure 5.3, also refered to as leakage current [30, 8]. Several standards limit this current, e.g. the German standards limit the value to below 30mA [10, 8]. However, the benefit in removing the HF transformer is improved efficiency, higher power density, and reduced cost [31].



(a) Isolated two-stage microinverter system



(b) Equivalent common-mode model of isolated microinverter

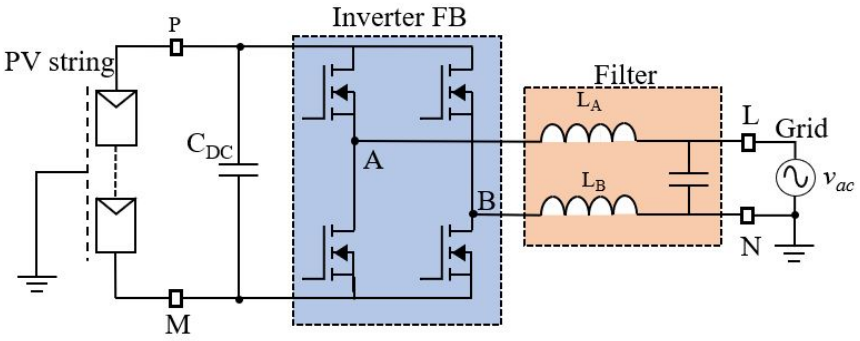


(c) Simplified common-mode model showing negligible common-mode current due to a low value of C_{ISO} in spite of high value of C_{PV}

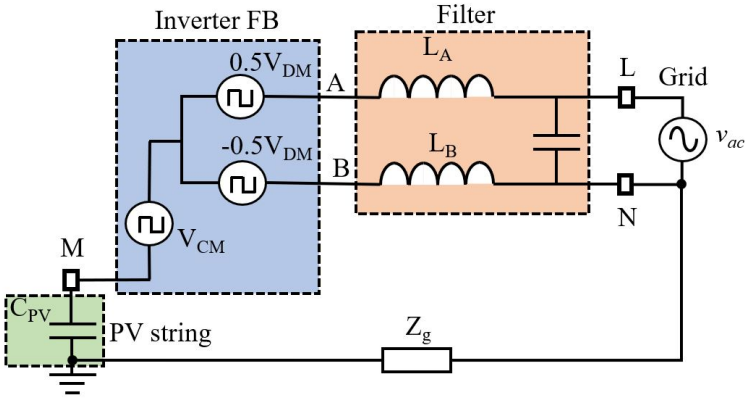
Figure 5.2: Development of common-mode model for isolated two-stage microinverter system

5.2.1 Proposed Solution

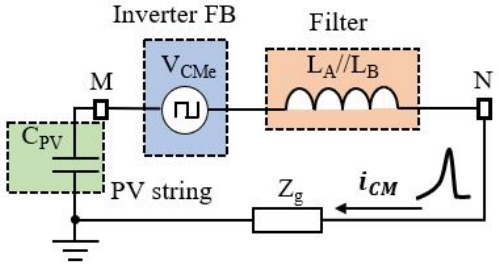
This dissertation proposes to remove the HF isolation transformer by using transformerless active isolation in the first stage of the PV microinverter. As seen in



(a) Non-isolated string inverter system



(b) Equivalent common-mode model of non-isolated string inverter

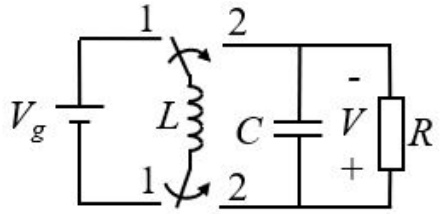


(c) Simplified common-mode model showing significant common-mode current due to the absence of series C_{ISO} and presence of high C_{PV}

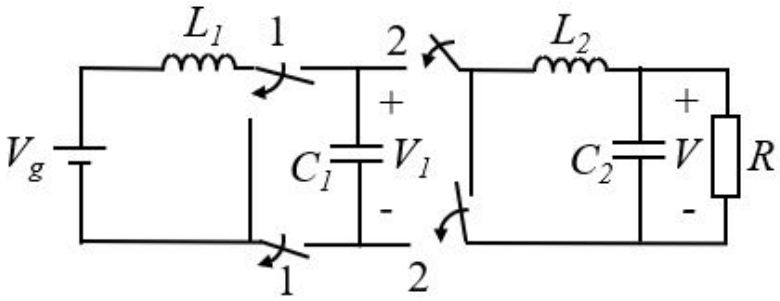
Figure 5.3: Development of common-mode model for non-isolated string inverter system

Figure 5.4, active isolated converters use semiconductor power devices to isolate conventional converters such as buck-boost and boost-buck [32]. In the first stage of a two-stage microinverter topology, unipolar active isolation is used to enable the

use of a common-ground connection from AC neutral (N) to PV module minus terminal (M). Although full system isolation is not obtained, the intermediate isolation provided between the two stages eliminates system leakage current since the common-ground connection effectively shorts out the common-mode voltage generated by the inverter.



(a) Buck-Boost

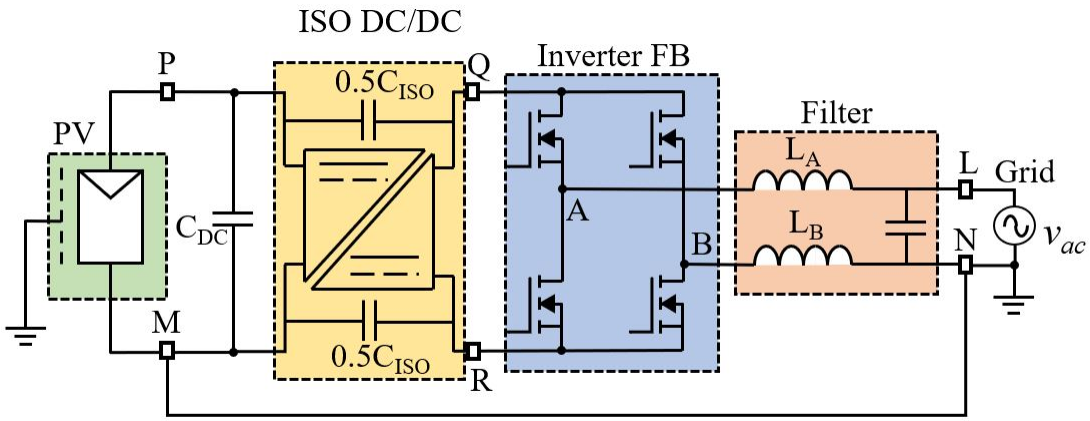


(b) Boost-Buck

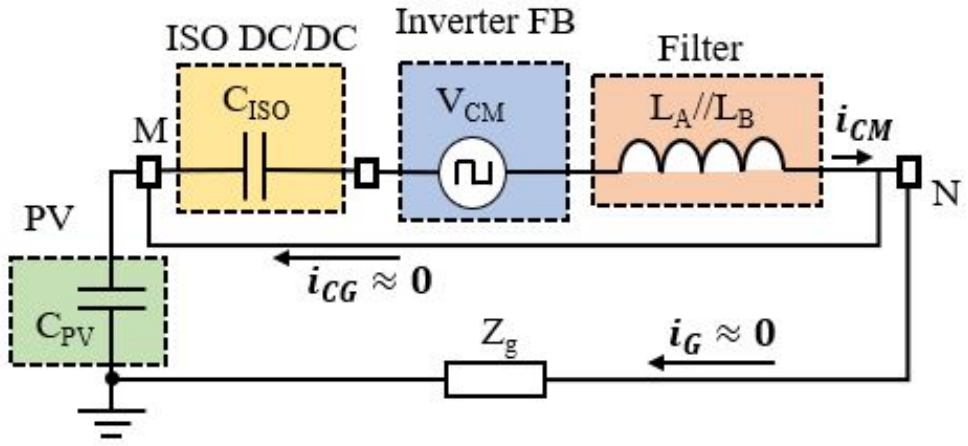
Figure 5.4: Active Isolated Power Converters

5.2.2 Derivation of Common-Ground Active Isolated PV Microinverter System

In transformerless converters, it has been shown in [26] that the use of a common-ground connection is the only method that results in complete elimination of the common-mode ground current. Traditionally, the common-ground connection requires the use of an isolation transformer as shown in Figure 5.5a. The PV minus terminal (M) is grounded by connection to AC output neutral (N), this is known as *common-grounding*. This common-ground connection effectively shorts out the common-mode voltage, V_{CM}, produced by the inverter thus eliminating the driving force around the resonant ground loop, as shown in Figure 5.5b, and reduces the common-mode current to zero.



(a) Common-ground connection of isolated PV inverter system



(b) Simplified equivalent common-mode model of isolated grid-connected FB inverter with common-ground connection showing zero common-ground current (i_{CG}) and zero ground current (i_G)

Figure 5.5: Circuit and model of isolated PV system with common-ground connection for mitigation of common-mode ground current

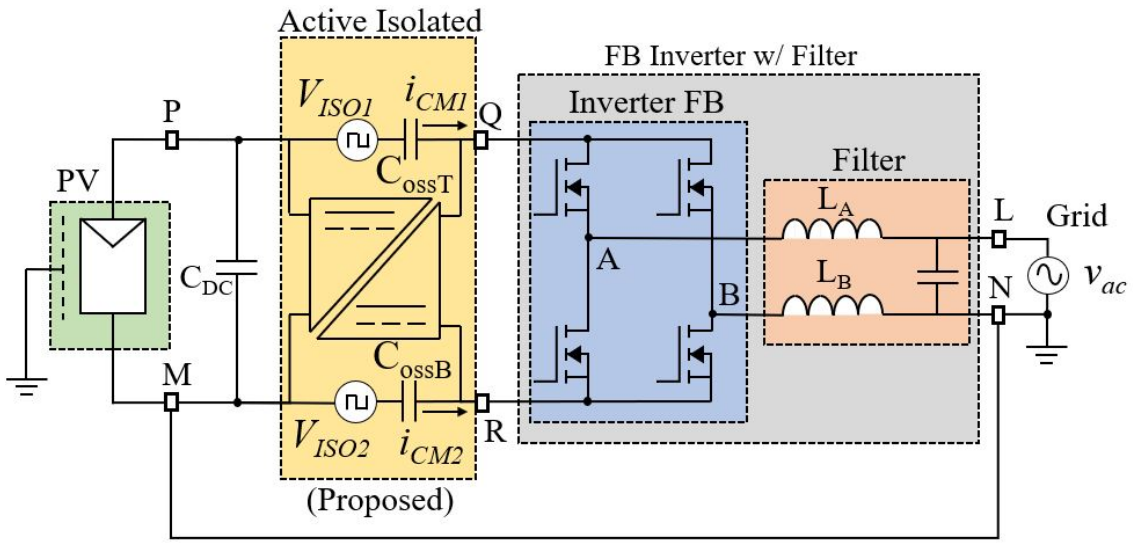
The transformer-based isolated converter of Figure 5.5a can be replaced with a transformerless active isolated converter as shown in Figure 5.6a. Actively isolated converters generate common-mode leakage currents (i_{CM1} and i_{CM2}) due to the switching action of semiconductor devices used to isolate the input from output [20, 21]. The switching current through the semiconductor output capacitance (C_{ossT} and C_{ossB}) is responsible for this common-mode isolation current [20, 21]. Methods have been developed to suppress this common-mode isolation current, however, in this application this current can be easily mitigated by using a common-ground

connection[22, 23], as shown in Figure 5.6a. This effectively suppresses the effect of the isolation currents and simultaneously shorts out the common-mode voltage of both the DC/DC converter (V_{ISO}) and inverter (V_{CM}) which eliminates the ground current (i_G) flowing through the ground impedance (Z_g) as shown in Figure 5.6b. (The magnitude of V_{ISO} depends on the active isolation topology.) The internally generated common-mode current (i_{CM}) flowing through the common-ground connection (i_{CG}) is due largely to a combination of several semiconductor output capacitances (nC_{oss}) that allows transient currents to flow internally around the resonant loop formed by V_{ISO}, nC_{oss}, V_{CM}, and $L_A//L_B$ but does not flow through the ground impedance Z_g due to Kirchhoff's Current Law (KCL). In effect, the common-ground connection causes the internally generated common-mode current (i_{CM}) to split into two currents: a common-ground component (i_{CG}), and a ground component (i_G). Since the impedance of the common-ground path is much lower than the ground impedance path, zero current flows through the ground impedance (Z_g).

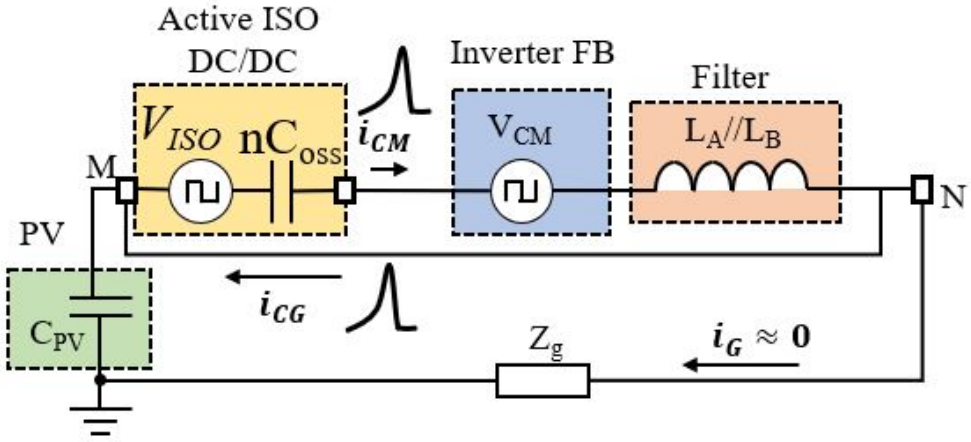
The common-ground current (i_{CG}) reduces the efficiency of the converter. This current can be minimized by choosing switch devices that have low values of parasitic output capacitance, C_{OSS}. Wide bandgap devices, such as Gallium Nitride (GaN) and Silicon Carbide (SiC), are good candidates for active isolation converters since they have comparatively lower values of parasitic output capacitances. A survey of commercially available SiC and GaN devices show output capacitances (Coss) in the range from 46pF to 289pF [33, 35]. Thus, the use of wide bandgap devices enables high efficiencies for the converter proposed in this microinveter system.

5.2.3 Unipolar Active Isolation in Common-Ground Microinverters

The magnitude of the isolation voltage available in active isolation is relatively limited compared to transformer isolation. It is limited to the blocking voltage of the isolation switch devices, e.g. 650V, 1200V, etc. The use of wide bandgap devices with high blocking voltage enables the practical application of active isolation in the



(a) Common-ground connection of active isolated PV inverter system



(b) Simplified equivalent common-mode model of active isolated grid-connected FB inverter with "common ground" connection showing switching current (i_{CG}) present through the common-ground connection but zero ground current (i_G) through the ground impedance

Figure 5.6: Circuit and model of active isolated PV system with common-ground connection for mitigation of common-mode ground current

microinveter system. In PV inverter applications with common ground connections, the amount of required isolation is known since the converter input (M) to output negative (R) is effectively clamped by the common ground connection, as seen in Figure 5.7.

A detailed analysis of various commonly used inverter topologies and modulation schemes, as seen in Figure 5.8, shows that the amount of isolation and polarity is

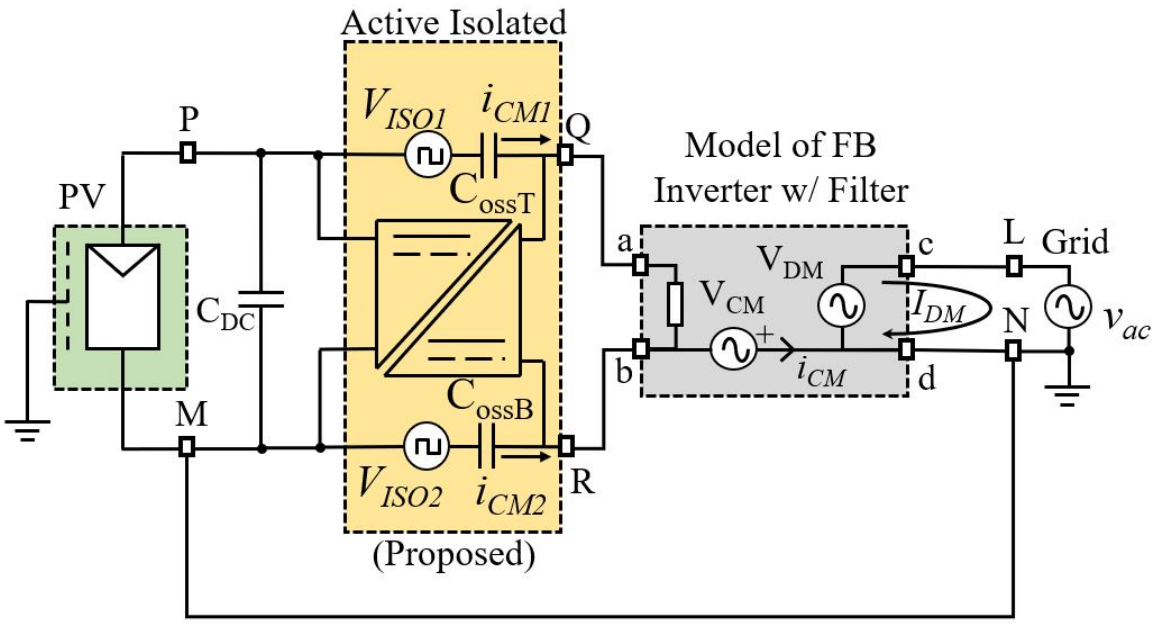
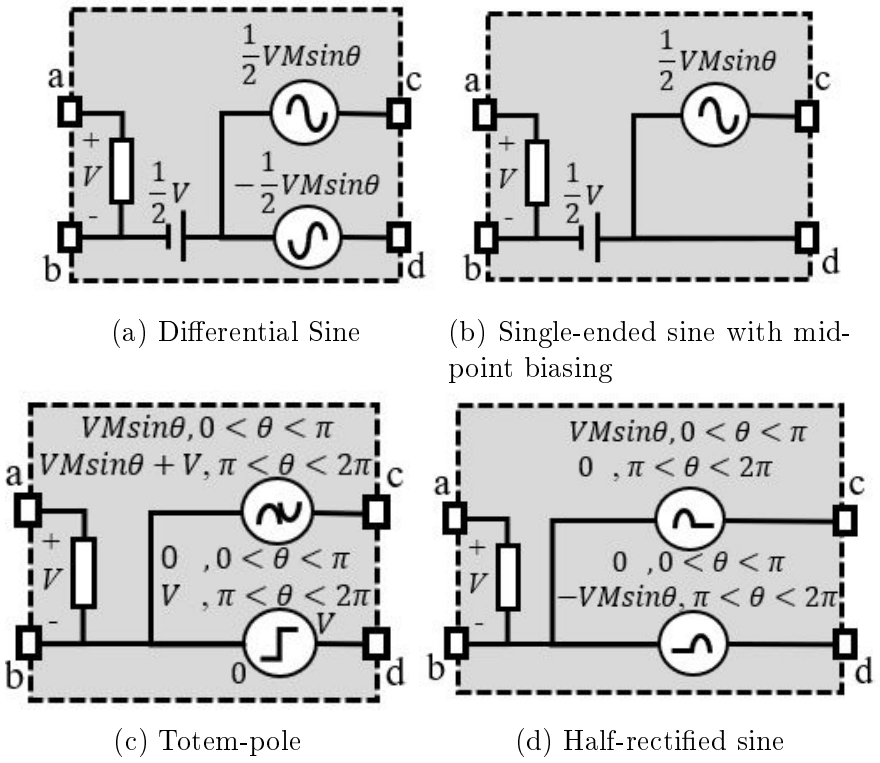


Figure 5.7: Model of active isolated PV microinverter with common-ground connection showing that $V_{MR} = V_{db} = V_{CM}$

limited to the PV module voltage and is unipolar. As such, unidirectional switches are utilized to realize the converters of Figure 5.4 as shown in Figure 5.9. The GaN HEMT devices for both converters are arranged to allow the body diode to freewheel the inductor currents during commutation deadtime.

5.2.4 Experimental Validation

This section contains simulation and experimental measurement results of unipolar active isolated buck-boost and boost-buck converters for two-stage PV microinverter applications as shown in Figure 5.1b. For the first DC/DC isolation stage, a unipolar active isolated converter is used as shown in Figure 5.9. The converters are first characterized with resistive load and then cascaded with a 1kW GaN-based inverter (TDINV1000P100) manufactured by Transphorm [34]. This inverter uses a half-rectified sine modulation scheme as shown in Figure 5.8d. The modulation scheme allows common-mode currents to flow in the converter since the common-mode voltage is a unipolar half-rectified sine wave. This enables the use of a unipolar DC/DC



(a) Differential Sine

(b) Single-ended sine with mid-point biasing

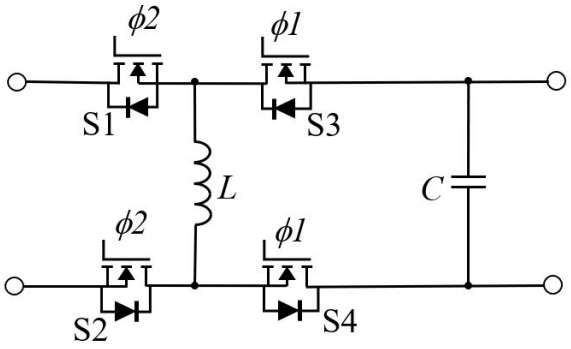
(c) Totem-pole

(d) Half-rectified sine

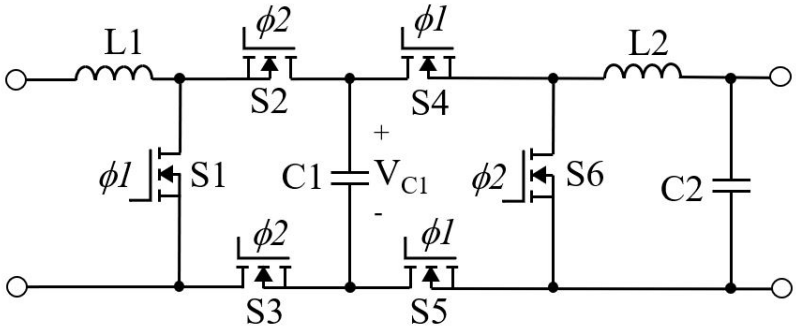
Figure 5.8: Non-isolated FB inverter in PV application showing generation of equivalent model with filter

isolation stage. The DC/DC converters operate from a 47V input and provide up to 190V output voltage for the inverter stage input. A Newtons4th N4L PPA1530 power analyzer is used for all efficiency measurements.

Figure 5.10 shows correlation between the averaged *differential- and common-mode* model shown in Figure 4.8b and SiMetrix SPICE switching model, with parameter values given in Table 5.1. Figure 5.10a shows correlation of common-mode current (i_{cm}) with the common-mode voltage set to zero, which is the worst-case scenario since the common-mode voltage tends to cause a current to flow in the opposite direction of the high-side common-mode currents. Figure 5.10b shows close correlation between the output voltage (V_o) of the averaged *differential- and common-mode model* compared to the SPICE switching model. These values have also been correlated to experimental measurements over a wide operating range.



(a) Buck-boost



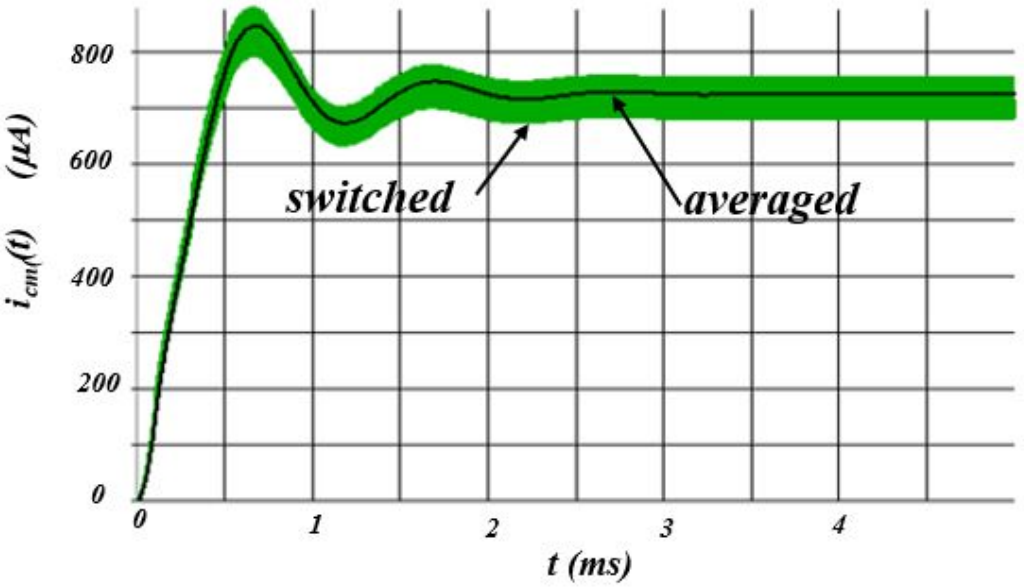
(b) Boost-buck

Figure 5.9: Proposed circuit to implement unipolar active isolated converters

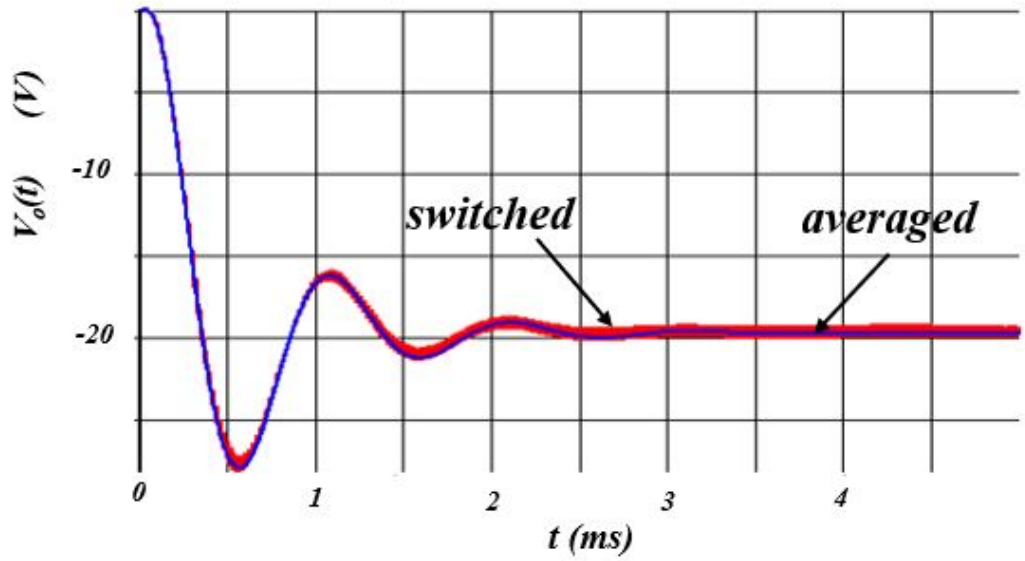
Table 5.1: Component values used in simulation of the active isolated buck-boost converter shown in schematic of Figure 5.9a.

Parameter	**Value**
D	0.5
C_{ossN}	180pF
V_g	20V
Z_L	25 Ω
R_l	22mΩ
R_{dsN}	35mΩ
R_{CossN}	55kΩ
V_{cm}	0V
R_{cm}	10.8Ω
R_T	0.276Ω
L	500μH

A 47V/190V, 350W GaN-based unipolar active isolated boost-buck converter was prototyped on Printed Circuit Board (PCB) as shown in Figure 5.11. The converter schematic is shown in Figure 5.9b with circuit parameters given in Table. 5.2. Fig-



(a) Simulation of output common-mode current (i_{cm}) showing close correlation



(b) Simulation of output differential-mode voltage (V_o) showing close correlation

Figure 5.10: SPICE simulation of switching model compared to *averaged differential- and common-mode* model (Figure 4.8b) showing close correlation

ure 5.12 shows an efficiency plot of the converter with measured results and calculated values plotted using equations given in [32]. As shown, the experimental and calculated values correlate well. The wire trace per switch (R_{wire}) was measured to be about $5m\Omega$ per switch. The peak efficiency is approximately 96.2% at 200W. The

efficiency could be improved by increasing board trace width, improving heat sink design, and choosing GaN switch devices with lower R_{ds-on} values.

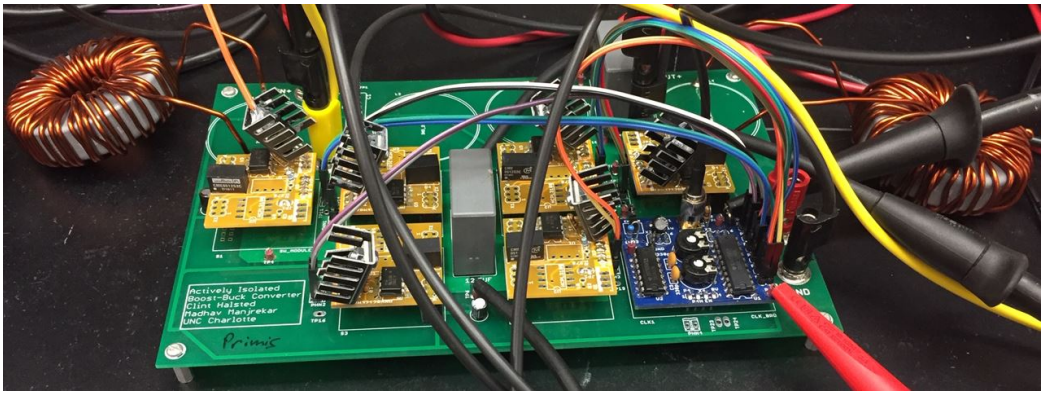


Figure 5.11: Prototype of 47V/190V, 350W unipolar GaN-based active isolated boost-buck converter PCB

Table 5.2: Parameter values used in testing of the 350W unipolar active isolated boost-buck converter shown in schematic of Figure 5.9b. and PCB shown in Figure 5.11

Parameter	**Value**
$L1 - L2$	500μH
$C1 - C2$	12.5μF
$S1 - S6$	TPH3212PS
$duty\ cycle, D$	0.83
f_{sw}	50 kHz
R_{ds-on}	85mΩ
R_{wire} per switch	5mΩ
Normalized R_{ds-on}	1.65
Q_{rr}	73nC

A 47V/190V, 1kW GaN-based unipolar active isolated buck-boost converter was prototyped on PCB as shown in Figure 5.13. The design consists a main motherboard with a dual pair of removable GaN modules with included heatsinks (middle) and non-overlapping clock buffer board (far left). A schematic of the converter power stage is shown in Figure 5.9a and parameter values given in Table 5.3. The waveform in Figure 5.14a shows the first phase of the non-overlapping clock signal ($\Phi 1$), along with output voltage (V_o), inductor voltage (V_L), and inductor current (I_L). Figure 5.14b

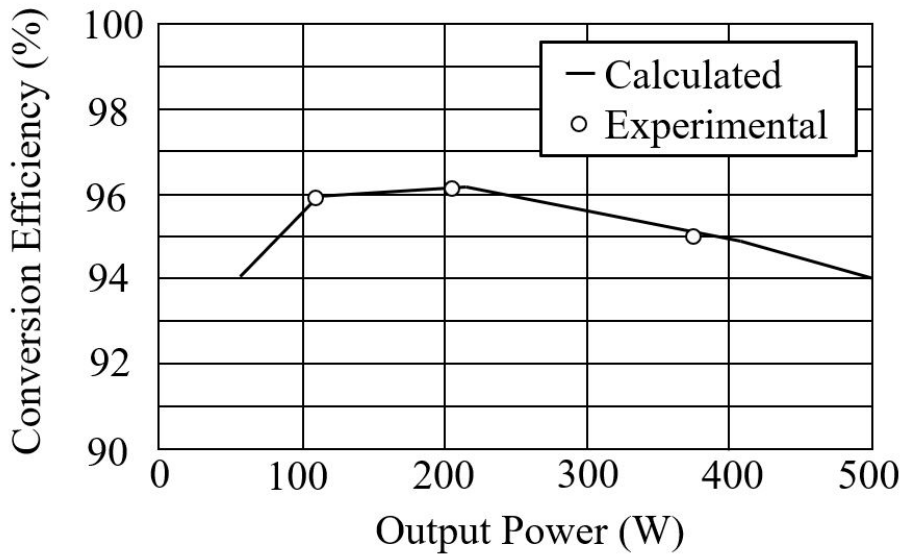


Figure 5.12: Measured and calculated efficiency of 350W unipolar active isolated boost-buck converter

Table 5.3: Parameter values used in testing of the 1kW unipolar active isolated buck-boost converter shown in schematic of Figure 5.9a and PCB shown in Figure 5.13

Parameter	**Value**
L	500μH
C	12.5μF
$S1 - S6$	TP65H035WS
Heatsink	530002B02500G
Thermal Pads	4169G
$duty\ cycle, D$	0.81
f_{sw}	50 kHz
R_{ds-on}	35mΩ
R_{wire} per switch	15mΩ
Normalized R_{ds-on}	1 to 1.9
Q_{rr}	144nC

shows an efficiency plot of the converter with measured results and calculated values plotted. As seen, the peak efficiency is 97.5% at 111W-150W.

To demonstrate the common-mode current isolation capabilities of the proposed solution, a 1kW GaN-based unipolar active isolated buck-boost converter was used in a two-stage microinverter configuration, as shown in Figure 5.15a. The waveform shown in Figure 5.15b verifies proper operation for a 580W load. The efficiency of the

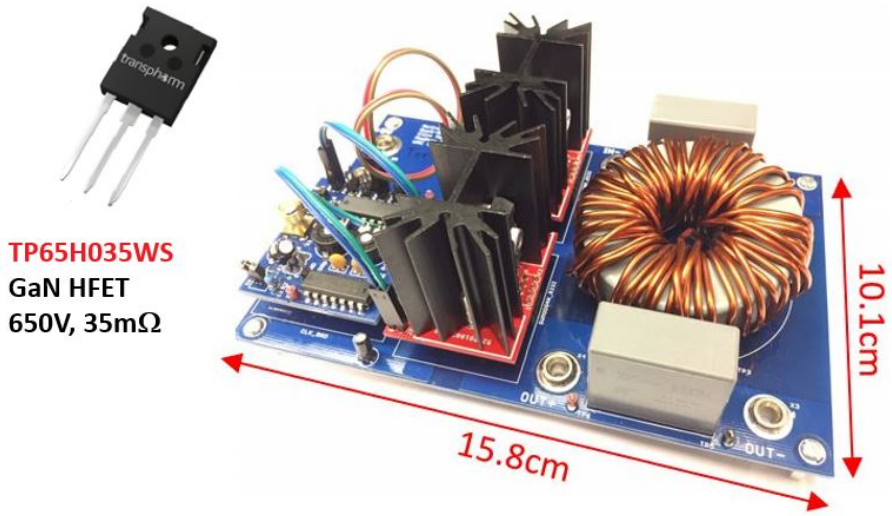
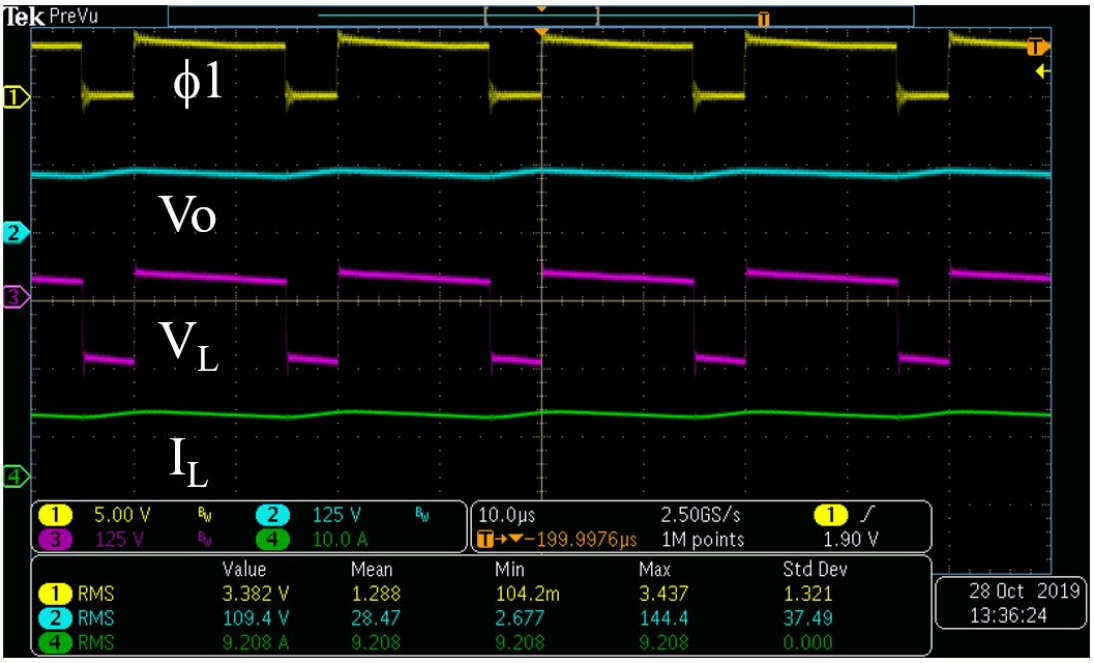


Figure 5.13: Prototype of 47V/190V, 1kW unipolar GaN-based active isolated buck-boost converter PCB

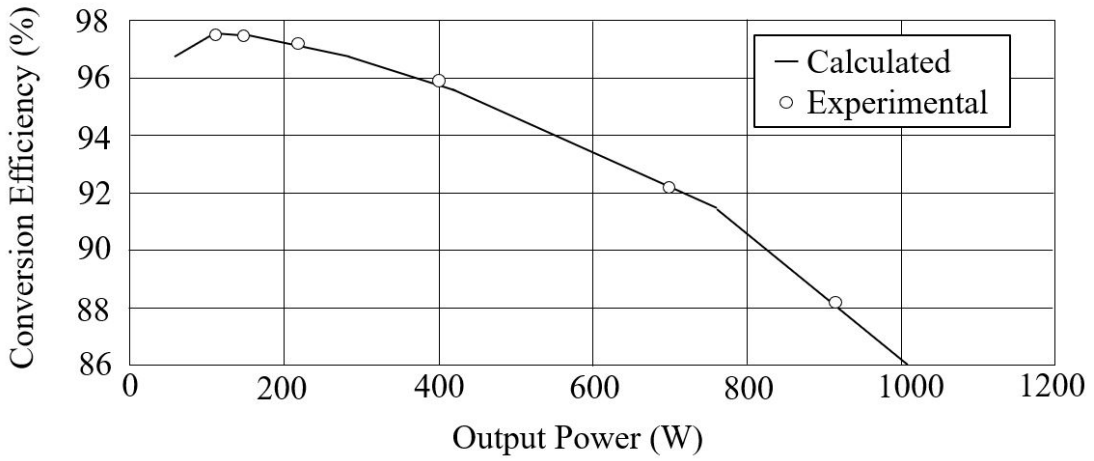
entire microinverter system is 88.56% while operating at 580W. As seen in Fig 5.16, the inner loop current flowing through the common-ground connection (i_{CG}) in the converter was measured to have an average value of 48.95mA with peak currents up to 3A, however, as discussed previously, this current flows around the interior of the converter and does not flow through the PV system ground (Z_g) since the common-mode voltage of the inverter has effectively been shorted by the common-ground connection. The total system efficiency is reduced by the current flowing through the common-ground connection (i_{CG}); so, the efficiency could be increased by selecting switch devices with lower output capacitance (C_{oss}). With a ground impedance (Z_g) value of 10.8Ω, the ground current (i_G) is measured to be zero as expected.

5.2.5 Discussion

In this section, two transformerless active isolated converter topologies were proposed to replace the conventional first transformer isolation stage of a two-stage microinverter system. Common-mode ground current concerns were mitigated by proper analysis and selection of a common-ground connection and unipolar active isolation



(a) Waveform of unipolar active isolated buck-boost converter showing clock signal (Φ1), output voltage (V_o), inductor voltage (I_L) and inductor current (I_L)



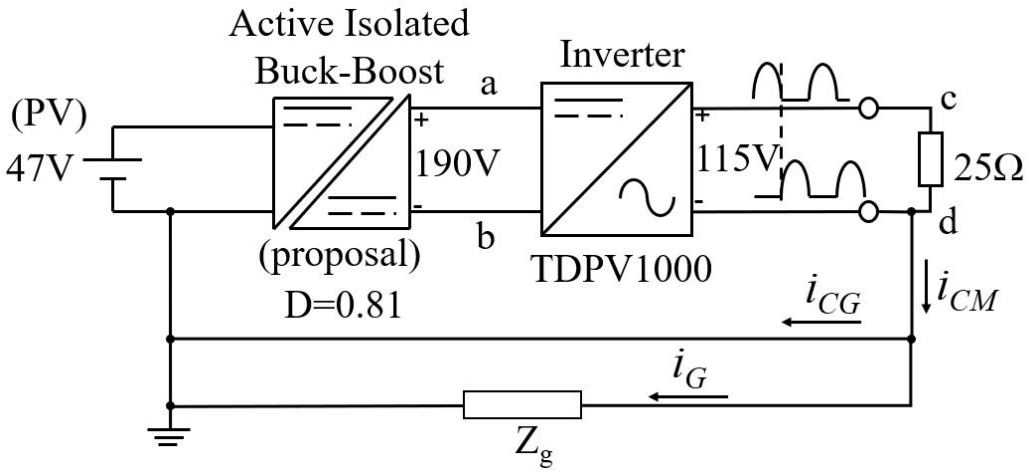
(b) Efficiency Curve of unipolar active isolated buck-boost converter showing peak efficiency of 97.5% at 111W-150W

Figure 5.14: Unipolar GaN-based 1kW active isolated buck-boost converter

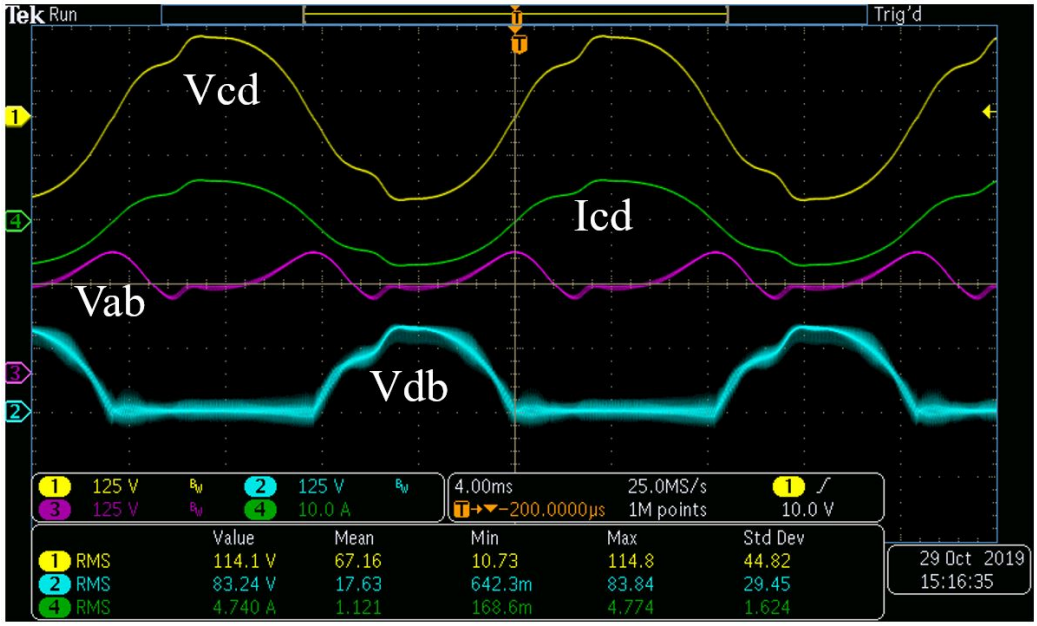
to improved converter efficiency, increase power density, and reduce cost.

5.3 AC/DC Power Adapter with Fault Protection

This section presents a transformerless common-ground AC/DC switching converter that consists of a diode bridge cascaded with unipolar Active Isolated (AI)



(a) Microinverter test schematic consisting of active isolated buck-boost converter cascaded with inverter



(b) Microinverter experimental waveform showing output voltage (V_{cd}), output current (I_{cd}), inverter input voltage (V_{ab}), and isolation voltage (V_{db}).

Figure 5.15: GaN 1kW Unipolar active isolated buck-boost converter followed by Transphorm GaN FB inverter EVB

DC/DC converter [32, 38], as shown in Figure 5.17. The application shown is a power adapter for laptop computers. (Safety standards are less stringent for voltages below twenty volts.) The converter provides galvanic isolation across switches that deliver energy to inductor L_1 during mode 1 (ϕ1 high) and transfers this energy to an output load during mode 2 (ϕ2 high) while preventing a direct connection between

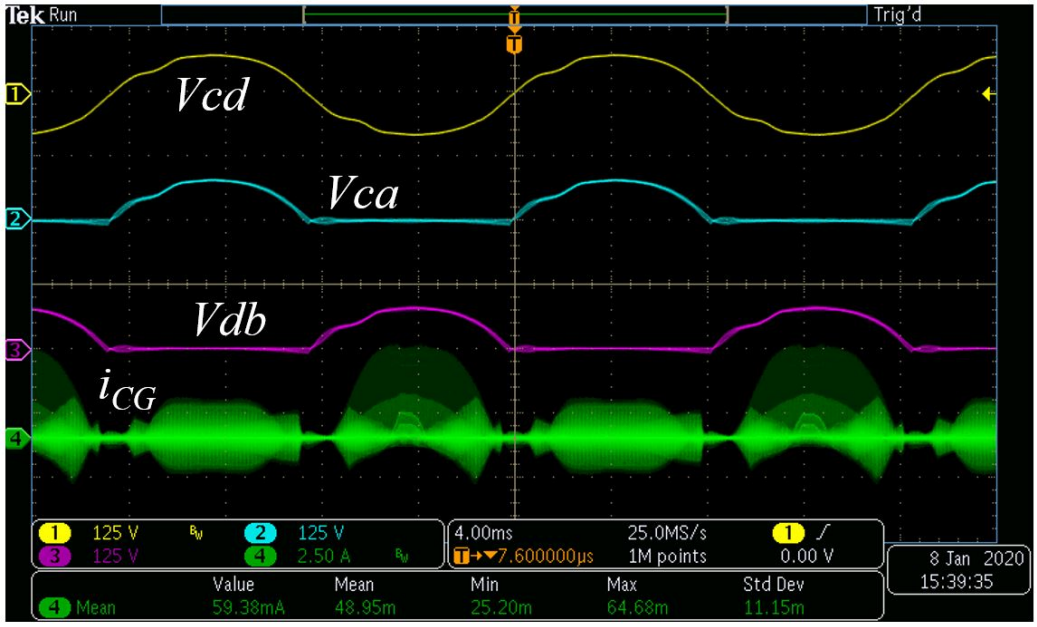
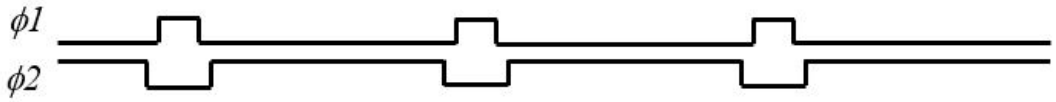
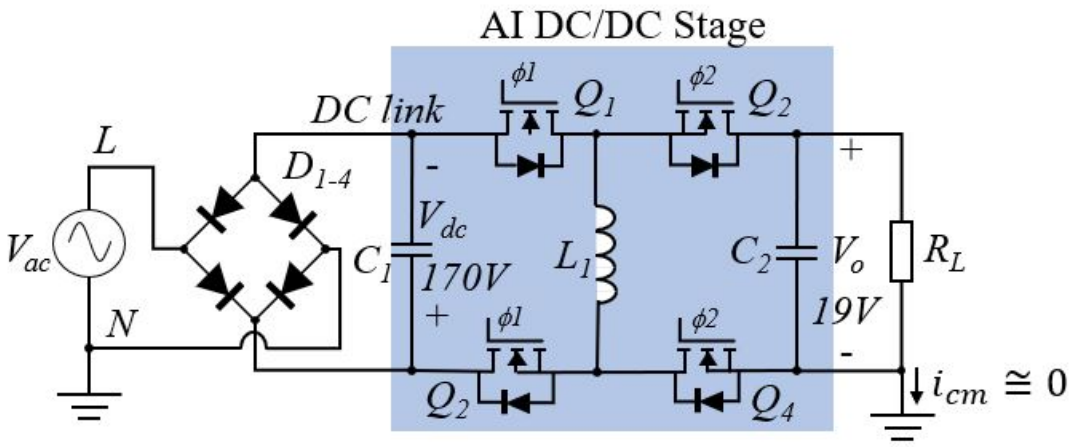


Figure 5.16: Measured common-ground current (i_{CG}) showing an average value of 48.95mA with peak currents up to 3A



(a) Timing waveform



(b) Circuit diagram

Figure 5.17: Proposed transformerless common-ground ac/dc converter (without fault protection) consisting of diode bridge cascaded with unipolar Active Isolated (AI) buck-boost converter

input and output via proper phasing of the switch devices $Q_1 - Q_4$.

The active isolation DC/DC stage has four major challenges that must be considered: 1) the generation of internal common-mode currents, 2) the presence of four switch parasitic output capacitors (C_{oss1-4}) that allow common-mode currents to flow, 3) the unipolar nature of the isolation prevents the output low-side connection from being higher than ground, and 4) the possibility of a switch failure would cause excessive common-mode currents to flow and could present a high voltage at the output terminals that could be a shock hazard, as shown in Figure 5.18.

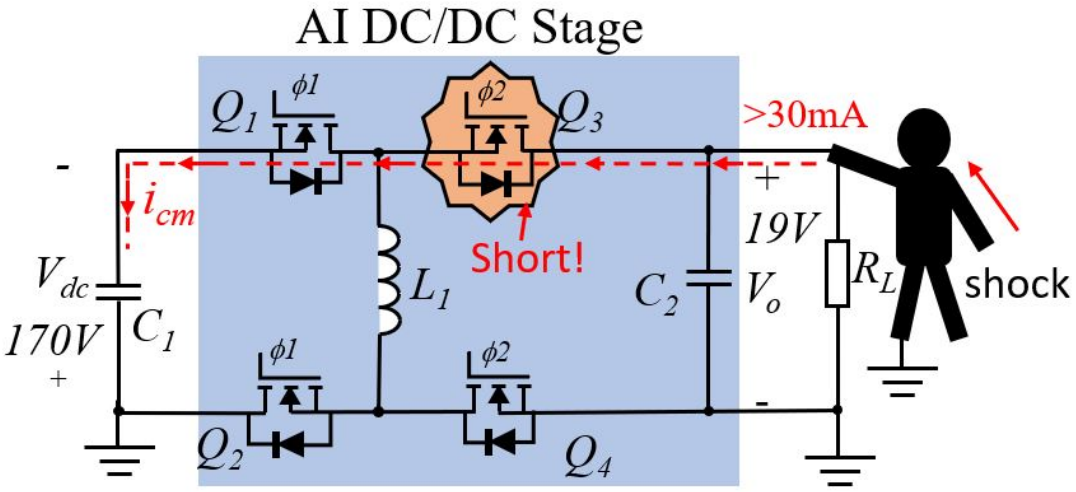


Figure 5.18: Circuit diagram of unipolar AI DC/DC stage of proposed converter showing the possibility of shock hazard in the event of switch short failure when transistor Q_1 is closed

The first issue has been solved for bipolar isolated converters with touch current suppression techniques as described in[22, 24, 23] and is solved in this converter design by shoring out the internally generated currents with the common-ground clamp connection at the output. The second issue is mitigated by ensuring the magnitude of the parasitic capacitance is close to the primary-to-secondary parasitic capacitance of a flyback transformer winding, e.g. $\leq$ 16pF [41]. A survey of wide bandgap devices show output capacitances (Coss) in the range from 46pF to 289pF[33, 35]. The selection of gallium nitride (GaN) transistors devices in this realization allow the output

capacitance to approach that of the primary-to-secondary parasitic capacitance of a conventional flyback transformer winding. The third issue is also solved by clamping the output low-side connection to ground through the use of a common-ground connection. The forth issue solution is proposed in this dissertation. The proposed approach is to actively measure the converter common-mode leakage current and disconnect the AI DC/DC stage using relay or bidirectional switch devices, as shown in Figure 5.19.

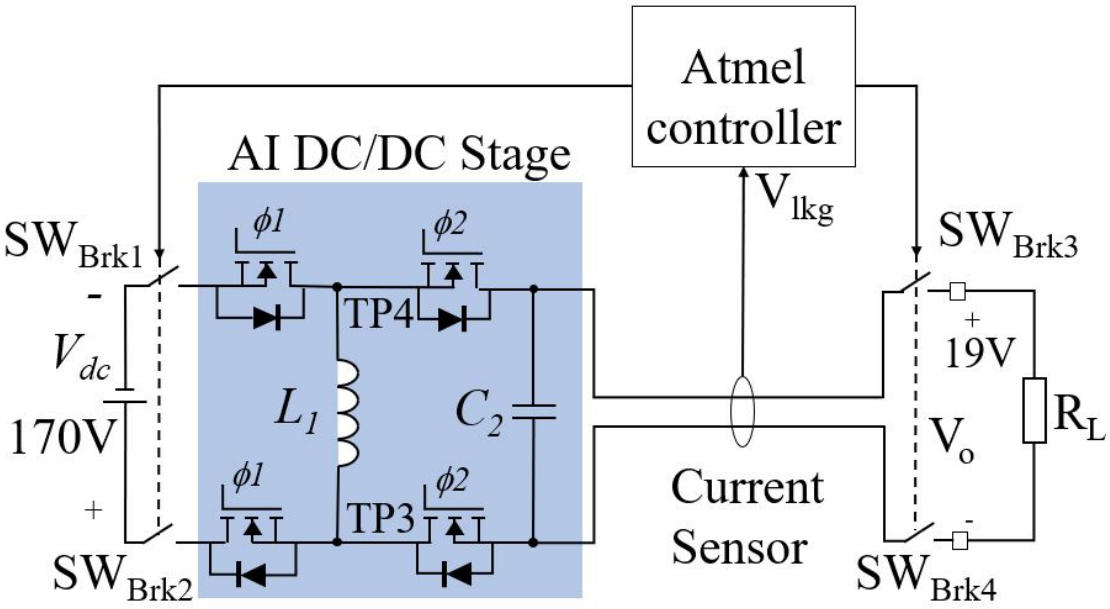


Figure 5.19: Circuit diagram of proposed AI DC/DC stage with additional fault protection circuitry consisting of: common-mode relay disconnect switches SW_{Brk1-4}, leakage current sensor, and controller

5.3.1 Development, Operating Principles, and Modeling of Common-Ground Transformerless Converter

This section covers the development and operating principles of the proposed common-ground transformerless AC/DC converter.

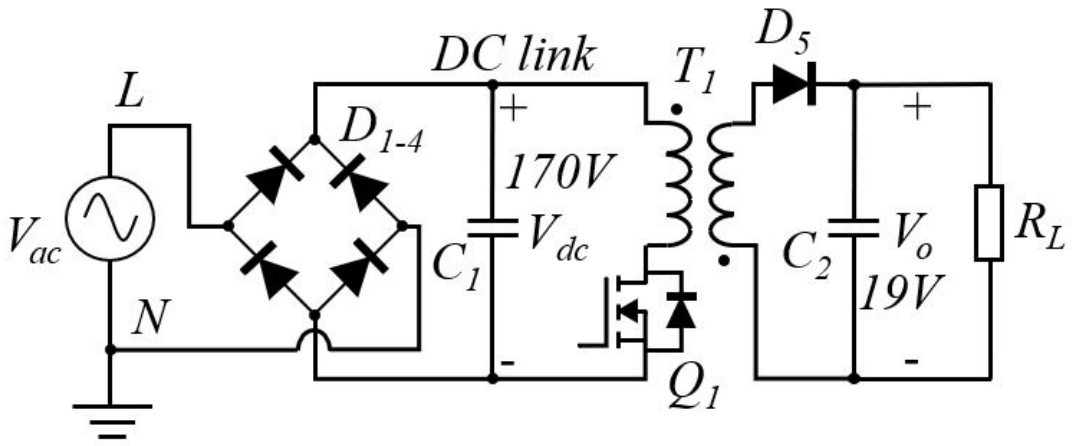


Figure 5.20: Conventional isolated ac/dc converter consisting of diode bridge cascaded with isolated buck-boost (flyback) converter [39]

5.3.2 Development and Operating Principles

A conventional isolated AC/DC converter utilizing a first stage diode bridge and second stage non-isolated buck-boost (flyback) converter is shown in Figure 5.20. The first stage diode bridge rectifier can optionally be replaced by a wide variety of different passive and active rectifier circuits– including a Power Factor Correction (PFC) stage. Due to the diode rectifier stage, the DC link voltage capacitor C_1 alternates between negative and positive ground. It is possible to replace the isolated DC/DC second stage flyback converter with a non-isolated buck-boost converter shown in Figure 5.21. If the output is grounded, a large undesirable common-mode leakage current (i_{cm}) flows and rapidly discharges the DC link capacitor C_1. However, if the output negative terminal of the converter is grounded through a human body, a shock is felt due to the high common-mode leakage current flowing to ground. Adding a lateral commutating switch pair on the low-side DC link prevents the previously mentioned undesirable common-mode leakage ground current from flowing, as shown in Figure 5.17.

Bidirectional switches are not needed in the DC/DC stage since the body diodes are reverse blocking during both positive and negative AC cycles; this allows for a unipolar

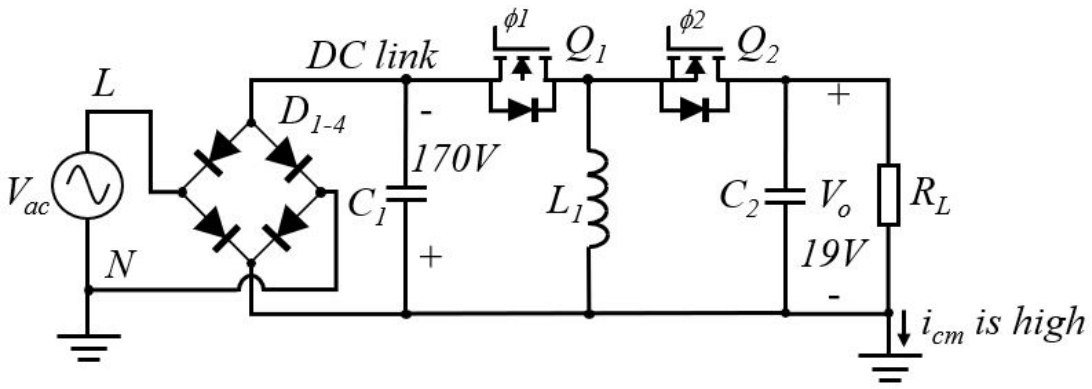
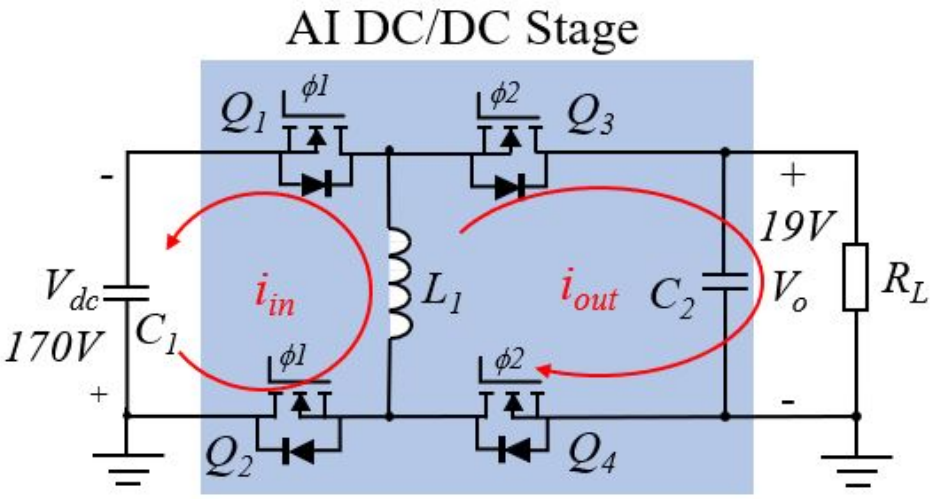
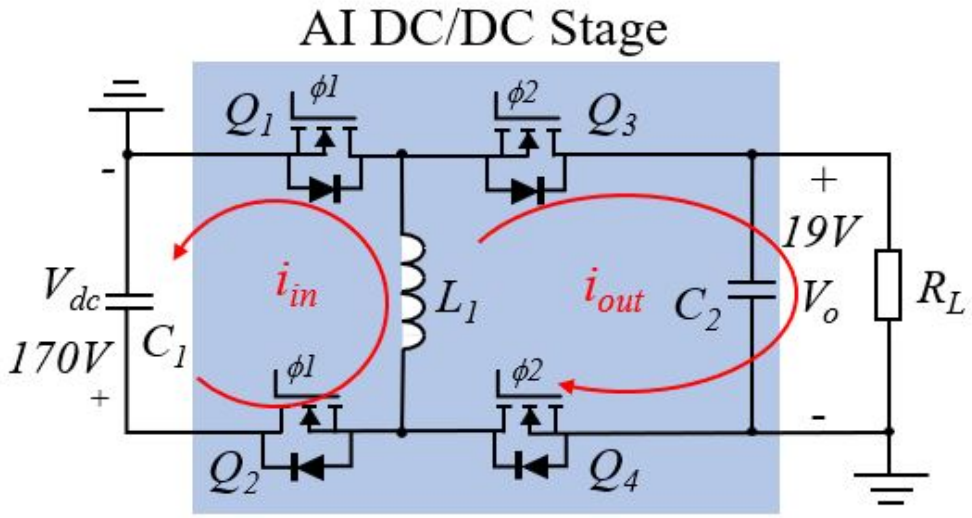


Figure 5.21: Non-isolated ac/dc converter consisting of diode bridge cascaded with non-isolated buck-boost converter

AI buck-boost topology, as shown in Figure 5.22. Power transfer from V_{dc} to L_1 occurs during mode 1 ($\phi 1$ high) with switch devices $Q_1 - Q_2$ closed and charges inductor L_1. During mode 2 ($\phi 2$ high), switch devices $Q_3 - Q_4$ are closed and the current in inductor L_1 is delivered to the load C_2 and R_L. This process occurs during both positive and negative grid voltage cycles, however, the location of the ground connection on the DC bus capacitor C_1 alternates from positive to negative ground, as shown in Figure 5.22. A sufficient deadtime exists (Figure 5.17a) between mode 1 and 2 so the input and output are not galvanically connected simultaneously. This provides the required galvanic isolation between input and output so that the common-ground output connection at the load is possible. This operation is fundamentally different than previous SC-based attempts at transformerless isolation since the conversion ratio is based on traditional inductor volt-second balancing instead of capacitor charge balancing [20, 21, 22, 24, 23]. The converter is referred to as being "unipolar" since switch devices $Q_1 - Q_4$ are reverse blocking in only one direction. In this case, unipolar operation is justified since the switch common-mode potential is always uni-directional.



(a) Negative AC grid voltage cycle



(b) Positive AC grid voltage cycle

Figure 5.22: Unipolar AI buck-boost topology during positive and negative cycles of the AV input grid voltage

5.3.3 Modeling of AI Buck-Boost Converter

The frequency-domain circuit model for an AI buck-boost converter is shown in Figure 5.23. The circuit model is based on the diferential-mode model in [27] except that the common-mode path consisting of Z_{cm} and V_{cm} has been added along with isolation resistance R_{cossT} and R_{cossB} representing the top and bottom isolation re-

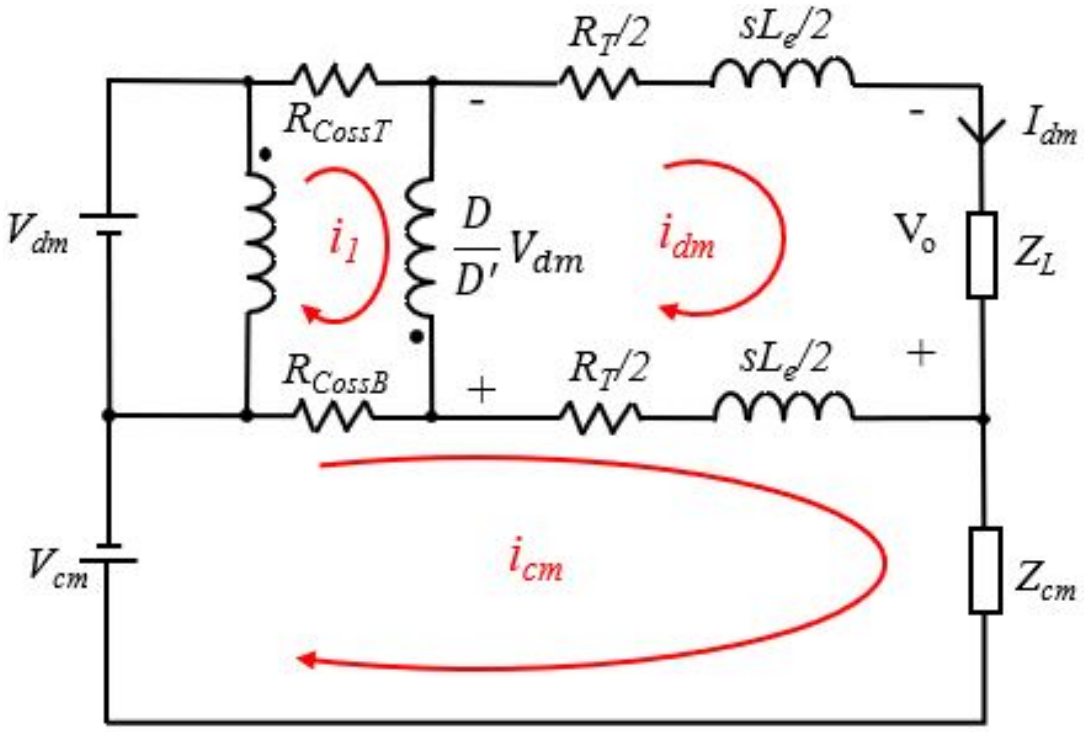


Figure 5.23: AI Buck-boost frequency-domain differential- and common-mode model [38]

sistance, respectively. The isolation resistances R_{cossN} (where N is T for "top" or B for "bottom") quantify the average current that flows through a commutating pair of switched-capacitor devices, as discussed in [40]. The parameters for the model are then:

$$R_{CossT} = \frac{1}{2C_{ossT}f_{sw}} \tag{5.1}$$

$$R_{CossB} = \frac{1}{2C_{ossB}f_{sw}} \tag{5.2}$$

$$Z_L = \frac{1}{sC}//R_L \tag{5.3}$$

$$L_e = \frac{L}{D'^2} \tag{5.4}$$

$$R_T = (\frac{D}{D'})^2 Re_1 + \frac{1}{D'} Re_2 \tag{5.5}$$

$$Re_1 = R_{ds1} + R_{ds2} + R_l \tag{5.6}$$

$$Re_2 = R_l + R_{ds3} + R_{ds4} \tag{5.7}$$

Circuit mesh analysis and solving for i_{cm} results in the following frequency-domain linear equation:

$$i_{cm} = \frac{A + B}{C - D}. \tag{5.8}$$

Where,

$$A = R_{CossB}(V_{dm} + \frac{D}{D'}V_{dm}) \tag{5.9}$$

$$B = (R_{CossT} + R_{CossB})[\frac{R_T + sL_e}{2}i_{dm} - V_{cm}] \tag{5.10}$$

$$C = (R_{CossT} + R_{CossB})(R_{CossB} + \frac{R_T + sL_e}{2} + Z_{cm}) \tag{5.11}$$

$$D = {R_{CossB}}^2 \tag{5.12}$$

If $R_{CossB} = R_{CossT} = R_{Coss}$, then Equation 4.39 simplifies to the following:

$$i_{cm} = \frac{V_{dm} + \frac{D}{D'}V_{dm} + (R_T + sL_e)i_{dm} - 2V_{cm}}{(R_{Coss} + R_T + sL_e + 2Z_{cm})}. \tag{5.13}$$

To obtain a practical approximation for the differential-mode current (i_{dm}), i_{cm} is set to zero (since in practice $i_{cm} \ll i_{dm}$) which gives us:

$$i_{dm} = \frac{\frac{D}{D'}V_{dm}}{sL_e + Z_L + R_T}. \tag{5.14}$$

Together, Equation 5.13 and Equation 5.14 are used to determine all voltages and currents of interest in the AI buck-boost converter when used in various applications. Equation 5.13 is plotted vs. switch output capacitance for three different wide bandgap devices [35, 33, 36] using MATLAB with parameter values given in Table 5.4

and Table 5.5 as shown in Figure 5.24. Based on these equations and the plot shown, switch devices should be selected to minimize the parasitic output capacitance (C_{oss}) of the isolation switches. As such, GaN devices are used for the converters in this dissertation since they have relatively low C_{oss} values. Comparison of Equation 5.13 to circuit diagram in Figure 5.22 reveals that, for this example, the common-ground connection at the output clamps the common-mode voltage to zero during the negative AC grid cycle and clamps it to negative one-hundred seventy (-170) volts during the positive AC grid cycle. The common-mode voltage will thus be a square wave at grid frequency with amplitude equal to V_{dm}.

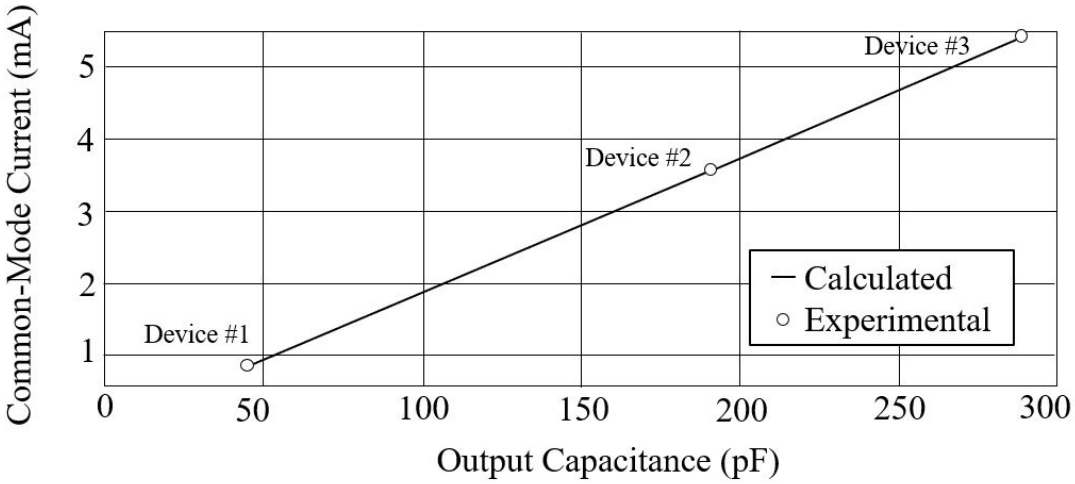


Figure 5.24: Plot of AI Buck-boost average (s=0) common-mode current during negative AC grid cycle for circuit shown in Figure 5.22a using Equation 4.44 for parameters give in Table 5.4

The equation derived for differential mode current, Equation 4.45, is used to calculated conducted efficiency losses in the converter using MATLAB. With switching losses added an efficiency curve is generated as shown in Figure 5.25 for the converter of Figure 5.22 with parameters given in Table 5.4 using switch device #2. Device #2 is selected since it offers the best trade-off between low common-mode current and relatively high efficiency.

Table 5.4: Component values used in simulation of the unipolar AI buck-boost converter shown in schematic of Figure 5.22a.

Parameter	**Value**
f_{sw}	50kHz
V_{dm}	-170V
V_o	19V
Z_L	50 Ω
L	500μH
R_l	22mΩ
R_{dsN}	35mΩ
R_{cm}	0Ω
V_{cm}	0V

Table 5.5: Wide bandgap switch device parameter values

Identifier	**Part Number**	C_{oss}	$R_{ds(on)}$
Device #1	TPH3206PSB	46pF	150mΩ
Device #2	TP65H035WS	190pF	35mΩ
Device #3	C3M0015065D	289pF	15mΩ

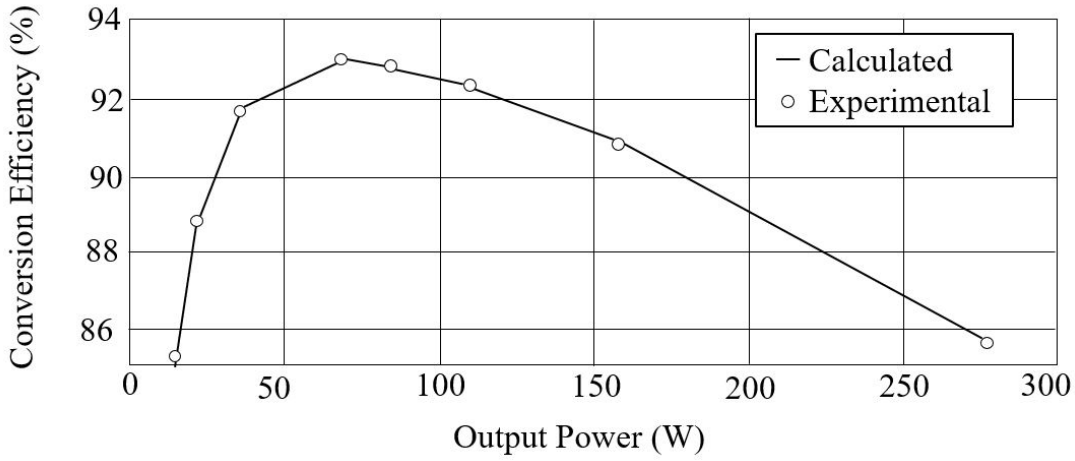
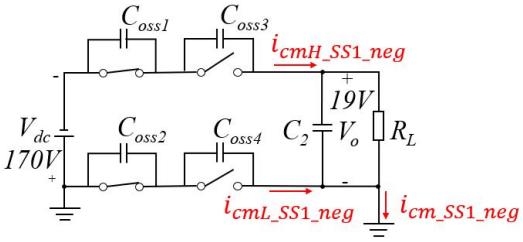


Figure 5.25: Efficiency plot of AI Buck-boost converter for circuit shown in Figure 5.22 using Equation 4.45 for parameters given in Table 5.4 and Table 5.5 for switch device #2

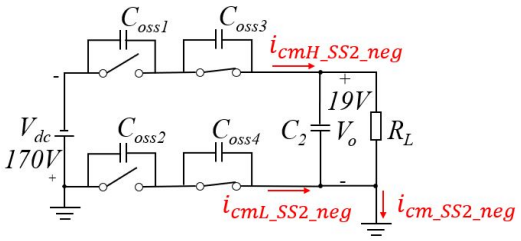
5.3.4 Fault Detection and Protection in Common-Ground Transformerless Converter

This section details the change in common-mode leakage current during fault conditions, that is, in the event that a switch device (Q_{1-4}) is shorted during normal

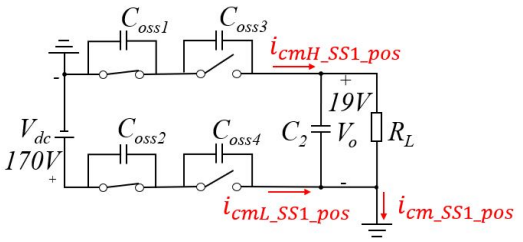
operation. The goal is to provide protection to users in the event of device failures since normally switch short protection is provided by transformer isolation. Note however that transformer winding insulation failure is also a safety concern for transformer isolated converters but is less common than transistor device failure.



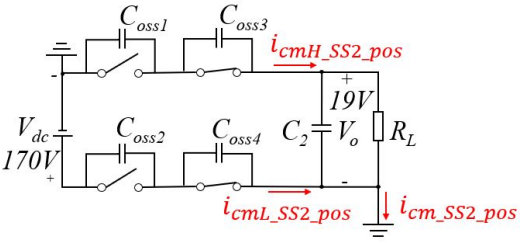
(a) Negative AC grid voltage cycle during mode 1



(b) Negative AC grid voltage cycle during mode 2



(c) Positive AC grid voltage cycle during mode 1



(d) Positive AC grid voltage cycle during mode 2

Figure 5.26: Simplified circuit diagram illustrating common-mode current path in AI buck-boost converter during positive/negative AC grid cycle during mode 1 and 2 of operation showing charging of switch parasitic output capacitors (C_{ossN})

The charging of MOSFET output parasitic capacitors CossN (with N=1-4) of the DC/DC isolation second stage causes a small steady-state common-mode current (i_{cm_SS}) to flow. This current will flow through the output ground connection. There will be a high-side (i_{cmH_SS}) and low-side (i_{cmL_SS}) contribution given by:

$$i_{cm\_SS} = i_{cmH\_SS} + i_{cmL\_SS}. \tag{5.15}$$

This current can be different during the positive and negative cycles and during mode 1 or 2, as shown in Figure 5.26. The current during the negative AC cycle during mode 1 is given by:

$$i_{cmL\_SS1\_neg} = 0 \tag{5.16}$$

for the low-side since the capacitor voltage is shorted to zero by the common-ground connection. The high-side common-mode leakage current is given by:

$$Q = CV \tag{5.17}$$

$$Q_{cmH\_SS1\_neg} = -C_{oss3}(V_{dc} + V_o) \tag{5.18}$$

$$i_{cmH\_SS1\_neg} = -\frac{\Delta Q}{\Delta t} \tag{5.19}$$

$$= -\frac{C_{oss3}(V_{dc} + V_o)}{1/f_{sw}} \tag{5.20}$$

$$= -f_{sw}C_{oss3}(V_{dc} + V_o), \tag{5.21}$$

as shown in Figure 5.26a.

The common-mode leakage current during the negative AC cycle for mode 2 at the low-side is given by:

$$i_{cmL\_SS2\_neg} = 0. \tag{5.22}$$

since the capacitor voltage is shorted to zero by the common-ground connection. The common-mode leakage current at the high-side is given by:

$$i_{cmH\_SS2\_neg} = -f_{sw}C_{oss1}(V_{dc} + V_o), \tag{5.23}$$

as shown in Figure 5.26b.

Thus the total common-mode leakage current during mode 2 of the negative cycle is:

$$i_{cm\_SS2\_neg} = -f_{sw}C_{oss1}(V_{dc} + V_o). \tag{5.24}$$

Combining these two current during the negative AC cycle for the entire switching period (modes 1 and 2) gives:

$$i_{cm\_SS\_neg} = i_{cm\_SS1\_neg} + i_{cm\_SS2\_neg} \tag{5.25}$$

$$= -f_{sw}C_{oss3}(V_{dc} + V_o) - f_{sw}C_{oss1}(V_{dc} + V_o). \tag{5.26}$$

If we let $C_{oss1} = C_{oss3} = C_{oss}$, then:

$$i_{cm\_SS\_neg} = -2f_{sw}C_{oss}(V_{dc} + V_o). \tag{5.27}$$

During the positive AC cycle, the high-side DC link capacitance is grounded as shown in Figure 5.26c and Figure 5.26d. Application of the same approach for the positive cycle results in:

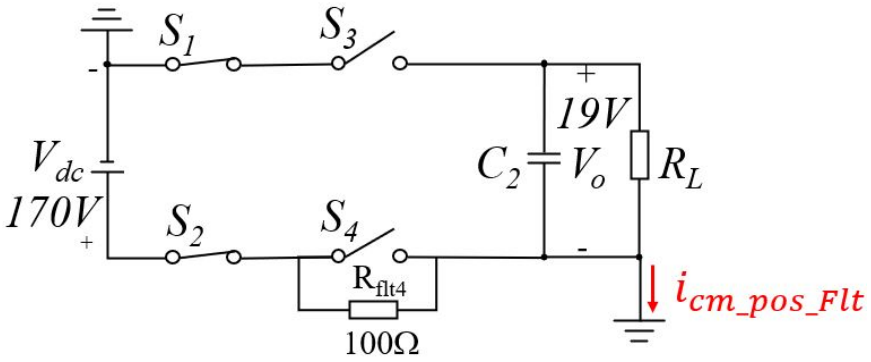
$$i_{cm\_SS\_pos} = -2f_{sw}C_{oss}(V_{dc} + V_o). \tag{5.28}$$

The total steady-state common-mode leakage current is the union of these two currents, and is given by:

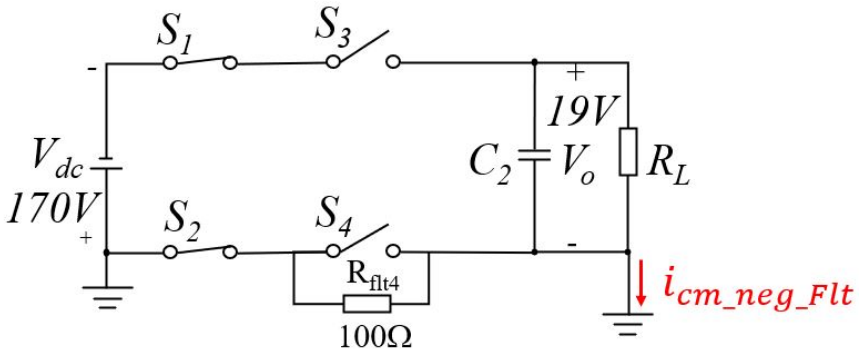
$$i_{cm\_SS} = -2f_{sw}C_{oss}(V_{dc} + V_o). \tag{5.29}$$

Substituting the parameters from Table 5.4 into Equation 5.29 gives $i_{cm\_SS} = -3.59$ mA, which agrees with the value given in Equation 4.44 and plot in Figure 5.24 from the previous subsection.

Of interest now, however, is to determine how the common-mode leakage current changes during a switch fault (short) condition. As seen in Figure 5.27b for a 100 Ω



(a) During negative AC grid voltage cycle during mode 1



(b) During positive AC grid voltage cycle during mode 1

Figure 5.27: Common-mode leakage current in DC/DC stage of transformerless common-ground converter during 100 Ω fault on switch device Q_4 (S_4)

fault, the common-mode leakage current is expected to increase and is given by:

$$i_{cm\_neg\_Flt} = 0 \tag{5.30}$$

$$i_{cm\_pos\_Flt} = \frac{V_{dc}}{R_{flt4}} \frac{1}{2} D \tag{5.31}$$

$$i_{cm\_Flt} = \frac{V_{dc}}{R_{flt4}} \frac{1}{2} D. \tag{5.32}$$

Using Equation 5.32 and the converter parameters given in Table 5.4, the common-mode leakage fault current is increased by:

$$i_{cm\_Flt} = \frac{170}{100} \frac{1}{2} 0.12 = 102mA. \tag{5.33}$$

The circuit shown in Figure 5.19 can thus be used to monitor the common-mode leakage current and open protection switches SW_{Brk1-4} in the event of a fault, i.e., if the fault current exceeds 30mA according to various standards [5, 6]. According to Equation 5.33, a fault resistor inserted across a switch device Q_4 should cause a sufficient fault to trigger protection switches (SW_{Brk1-4}) to open and protect the output. It is found that shorting 100Ω resistors across other switch devices (Q_{1-4}) in the circuit cause a similar increase in common-mode leakage current, and thus the proposed circuit given in Figure 5.19 will protect the output under all fault conditions.

5.3.5 Experimental Results

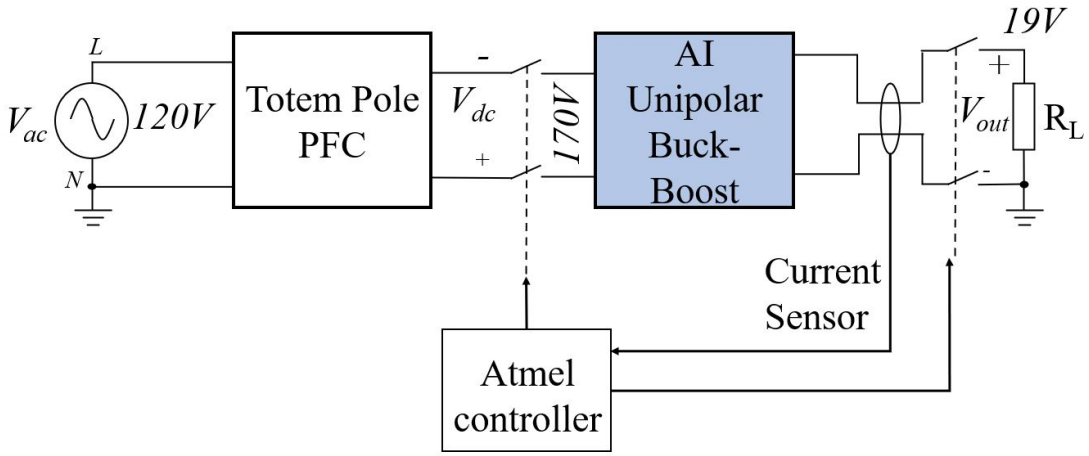
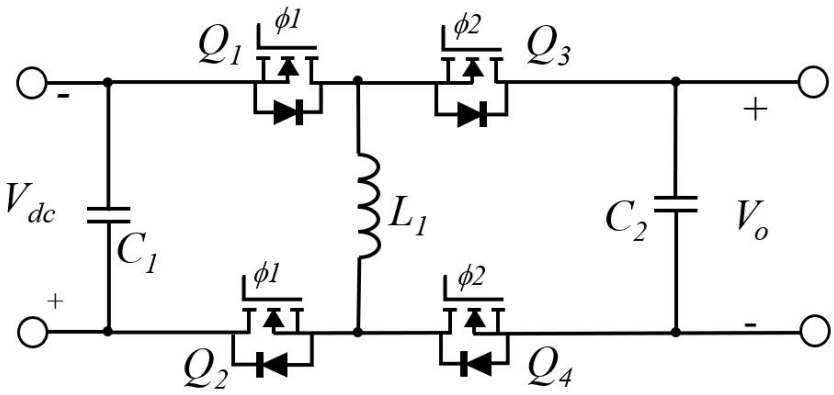


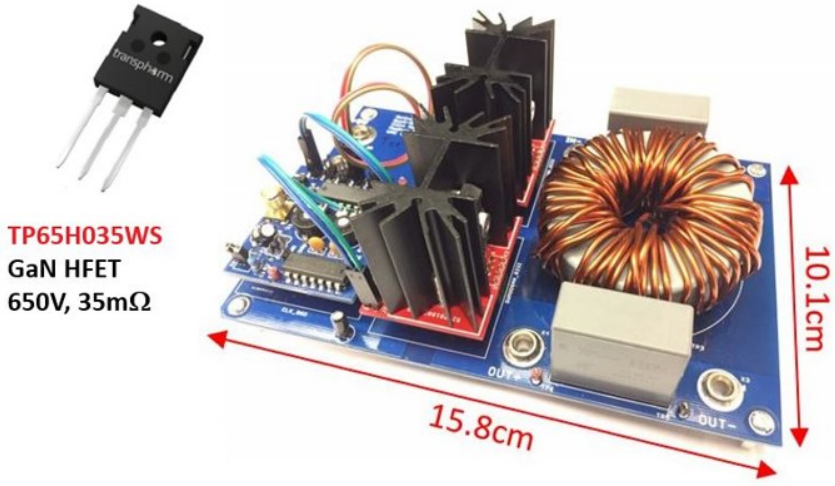
Figure 5.28: Block diagram of proposed transformerless common-ground AC/DC converter consisting of Transphorm bridgless totem-pole PFC [37] cascaded with unipolar AI buck-boost converter

This section demonstrates experimental results of a 300W 120Vac-to-19Vdc PFC for laptop adapter applications. The converter is built by cascading a 2.5kW GaN-based totem-pole PFC (designed by Transphorm Inc. [37]) with a 300W GaN-based unipolar AI buck-boost DC/DC converter, as shown in Figure 5.28. Although the DC/DC converter second stage is capable of operating at 1kW, only 300W operation is recommended for this application due to lower efficiency at higher output power.

The circuit diagram of the unipolar AI buck-boost DC/DC second stage is shown



(a) Circuit diagram



(b) GaN-based PCB board implementation

Figure 5.29: Prototype of 300W 170Vac-to-19Vdc unipolar AI buck-boost converter

in Figure 5.29a with 650V GaN-based printed circuit board (PCB) implementation shown in Figure 5.29b. The converter parameters are given in Table 5.6. The measured efficiency of the converter is shown in Figure 5.25 and has a maximum value of 93% at around 70W (close to the rated power of laptop power adapters).

The oscilloscope waveform shown in Figure 5.30 shows the experimental results of a 100Ω short fault applied to switch Q_4 of the second stage DC/DC circuit as shown in Figure 5.29a. As shown, the relay switches (SW_{Brk1-4}) open within 300ms to disconnect the converter from input and output circuits, thus protecting the user from potential shock. Fault shorts across switch devices Q_{1-3} show similar results

Table 5.6: Parameter values used in testing of the 300W unipolar active isolated buck-boost converter shown in schematic of Figure 5.29a and PCB shown in Figure 5.29b

Parameter	Value
L_1	500μH
$C_1 - C_2$	12.5μF
$Q_1 - Q_4$	TP65H035WS
Heatsink	530002B02500G
Thermal Pads	4169G
$duty\ cycle, D$	0.12
f_{sw}	50 kHz
R_{ds-on}	35mΩ

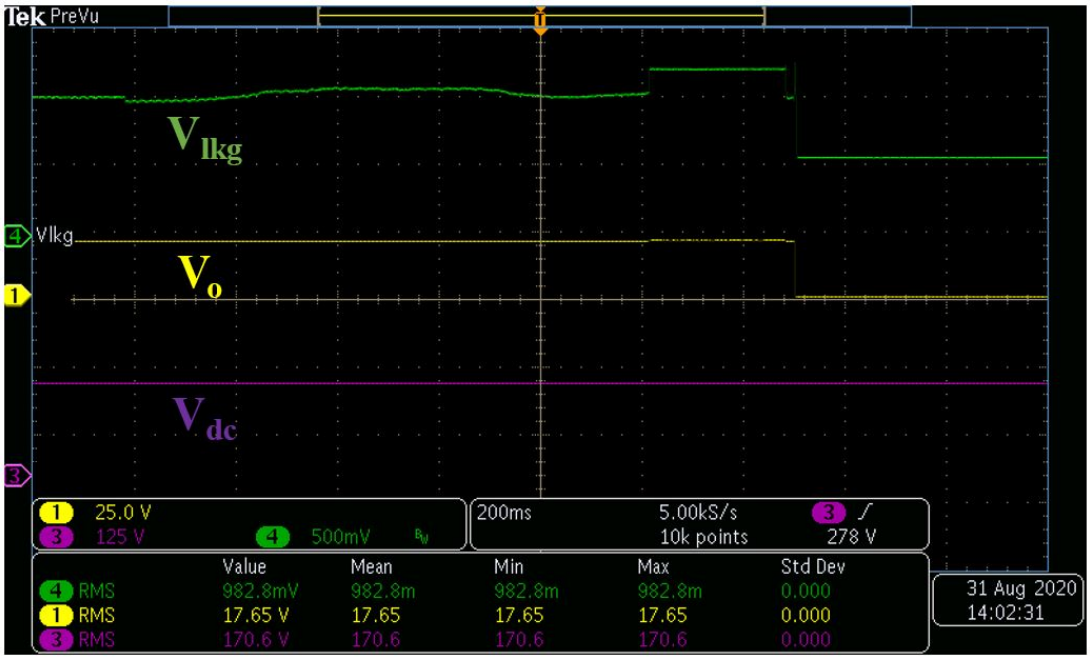


Figure 5.30: Oscilloscope waveform showing common-mode leakage current increase with 100Ω fault short across Q4 device

with relay protection provided within the required 300ms time frame.

5.3.6 Discussion

In this section, a new common-ground transformerless 300W, 120Vac-to-19Vdc AC/DC converter was proposed for application in laptop power adapters. However, since the solution is transformerless, a fault in the DC/DC unipolar isolation stage could result in a potential shock hazard to the user. In other applications, GFCI and

RCD devices are used to mitigate these concerns and protect against electrical shock; a similar approach is proposed for this solution where the common-mode current of the output DC/DC second stage is measured and relay contacts open to protect if the measured output common-mode leakage current exceeds 30mA. The proposed solution was found to disconnect in less than 300ms, which complies with applicable safety standards [5, 6]. The 300W, 120Vac-to-19Vdc common-ground transformerless PFC AC/DC converter was found to have peek efficiency of 93% at 70W.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

In this dissertation, a new set of galvanically isolated switching converters are developed mathematically and demonstrated experimentally. In total, thirty-six new AI converters are developed of which two optimum converters, the buck-boost and boost-buck, are found to require the fewest components for the required operation of either pulsating or non-pulsating input/output current, respectively. Also, the AI converter component count can be reduced by replacing the bidirectional switches with unidirectional switches thus producing a unipolar AI converter. Unipolar isolated converters are justified since in many applications, the common-mode voltage across the converter is unipolar, i.e., common-ground pv inverter and common-ground offline power supply. A mathematical model of the two optimum AI converters was developed and validated with experimental results. Prototypes of a 500W common-ground PV microinverter and 300W laptop ac-to-dc power adapter ac-to-dc are developed and experimental results show high peak efficiencies of 97% and 93%, respectively.

Some of the importaint contributions of this dissertation are: 1) proposed new set of galvanicaly isolated switching converters known as Active Isolation (AI), 2) thirty-six new proposed AI topologies including two optimum topologies: buck-boost and boost-buck, 3) demonstration of fully isolated (bipolar) boost-buck converter, 4) demonstration of AI boost-buck converter in generation of dual supplies for use in inverter application, 5) demonstration of small (mA range) common-mode leakage current in active isoalted converter, 6) demonstration that the common-mode leakage current in AI converters is due only to charging and discharging of Coss paracitic capacitance of the isolation switch devices, 7) development of mathematical model to fully describe the transient and steady-state contribution of the switch parasitic

Coss capacitance to common-mode leakage current and coorelation to experimental results, 8) demonstration that wide bandgap devices enable the possibility to meet safety standards on "touch current" requements in IEC and VDE standards [6, 2, 3], 9) demonstration of AI buck-boost converter in common-ground PV microinverter application, 10) demonstration of zero common-mode leakage current in unipolar AI buck-boost converter in common-ground PV microinverter application, 11) demonstration of unipolar AI buck-boost converter in common-ground offline power supply for laptop power adapter applications, 12) concept of unipolar and bipolar active isolation for use in specialized applications, 13) demonstration of common-mode current monitoring for fault detection in AI converter applications.

Future work in active isolation includes expanded applications of unipolar active isolation to other AC/DC isolation applications such as onboard electric vehicle (EV) battery charger, various other off-line power adapters, and server power for data center. Use of active isolation in these applications has the opportunity to improve cost, size and efficiency by elimination of the transformer. Additional research is needed in power semiconductor devices to achieve even lower power switch output parasitic capacitance (Coss) values. A 10x reduction is still needed in higher power (>1KW) applications to reduce common-mode current without the need for methods to reduce this current, e.g. common-grounding and leakage current suppression. Continued efforts in transformerless active isolated converter technologies should be explored with this technology. This has the potential to reduce microinverter sizes so that AC modules (microinverter integrated with PV module) are more feasible. The unipolar active isolated microinveter has great potential since the common-mode leakage current is zero and there is complete elimination of the isolation transformer. Continued research into the proposed AC/DC laptop power adapter is needed to measure touch currents at all operating points and to field test the prototype with integral fault protection circuitry over various environmental and electrical conditions for stability and

reliability. New control algorithms are needed to commutate the power switch devices for full isolation. The majority of the work in this dissertation has focused on application of unipolar active isolation due to simplicity and cost savings, however, more research efforts are needed into fully isolated converters. As power switch devices become larger, the parasitic output capacitance (Coss) values get larger proportionally. This makes active isolation more difficult at higher power levels. As such, power switch devices need to maintain Coss values ($<$ 15pF) at higher power levels; this is a difficult challenge to overcome. Continued efforts and research is needed to realize higher power ($>$1kW) fully active-isolated converters. Additionally, more effort and research should go into the fully isolated boost-buck topology. Even though this topology is more complicated since it requires more switch devices and an additional inductor, the smooth input and output current requires smaller output and input EMI filters and more closely approximates an ideal isolated DC transformer. It is expected, that with the passage of time, more power converters will be transformerless and follow the trend of the inverter market. A major challenge to overcome is the fear from designers and consumers in loosing the perceived value of safety with transformerless topologies. Future work should be done to find ways to make customers feel good about transformerless topologies or the growth of this technology will be delayed for many years to come. Even still, the growth of transformerless technologies are likely to trend upwards first in the lower power applications since lower power switch devices have lower Coss values than larger devices. Active isolation and wide-bandgap devices are likely to play are large roll in making transformerless topologies realizable for future generations.

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