CONTROL STRATEGIES FOR SOLAR PANEL COMPANION INVERTERS

by

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ABSTRACT

PRASANTH KUMAR SAHU. Control strategies of solar panel companion inverters.
(Under the direction of Dr. MADHAV MANJREKAR)

This thesis investigates a unique methodology that converts the conventional dc voltage output of a photovoltaic solar panel to switched quasi-square wave voltages with variable pulse width, which when aggregated realize a superior quality multilevel waveform that can be directly interfaced with the power grid. Termed Solar Panel Companion Inverters, this alternative approach offers advantages of micro-inverters in realizing panel-level maximum power point transfer and realization of system-level cost benefits of a central inverter approach. Various control strategies such as Unsorted Pulse Width Modulation, Sorted Stair Case Modulation and Sorted Pulse Width Modulation for these Solar Panel Companion Inverters are presented and analyzed in the paper. These control schemes are evaluated against a variety of solar irradiance operating scenarios with varying co-efficient of variation and varying mean irradiance levels. The resultant energy yields are documented for each control scheme. It is shown that the proposed structure of Solar Panel Companion Inverters is able to collectively perform as a conventional central inverter when irradiance conditions are uniform. However, under non-uniform irradiance conditions, proposed structure surpasses performance of central inverter in terms of power throughout and can be a commercially competitive solution when compared to micro-inverters for interfacing solar panels with the power grid.

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LIST OF ABBREVIATIONS

CSP	concentrating solar power
DOE	department of energy
SPCI	solar panel companion inverter
MPPT	maximum power point tracking
UPWM	unsorted pulse width modulation
SSCM	sorted stair case modulation
SPWM	sorted pulse width modulation
PLL	phase locked loop
THD	total harmonic distortion
MSHE	multilevel selective harmonic elimination
MSVM	multilevel space vector modulation
JFET	junction field effect transistor
MPP	maximum power point
MOSFET	metal oxide semiconductor field effect transistor
STC	standard test conditions

CHAPTER 1 : INTRODUCTION

1.1. Introduction

This chapter presents a brief introduction and organization of the thesis. Importance of renewable power generation is presented in Section 1.2. Section 1.3 presents utilization of solar energy. Motivation for the thesis is presented in Section 1.4. Section 1.5 presents the organization of the thesis.

1.2. Renewable Power

The standard of living has been increasing, with the continuous advancement in technology. Thus, there is an ever increasing demand of energy in various sectors such as electric power generation, transportation, industrial, residential, and commercial. History of energy consumption in United States is shown in Figure 1.1 [1]. It may be seen that wood was the major source of energy till the mid of nineteenth century. With industrialization and requirement of electric power towards the mid of twentieth century, coal, petroleum, natural gas emerged to be the dominant sources of energy. Towards the end of the twentieth century, nuclear energy made a significant contribution towards electric power generation. With the emergence of fossil fuels as energy sources, the carbon dioxide emissions increased and the problem of global warming started. However, there were other sources called renewable energy sources such as solar, wind, water etc. which hardly produce any carbon dioxide emissions. Towards the end of twentieth century and the beginning of twenty first century, renewable energy sources such as solar, and wind

started making a significant contribution towards electric power generation. Figure 1.2 shows the contribution to the electric power generation by various sources in the recent past [2]. It may be seen that although there is an increasing trend in the contribution of renewable energy sources towards electric power generation, coal, natural gas, and nuclear are still the major sources of energy. According to Oregon Department of Energy, the carbon dioxide emissions due to electric power generation constitutes 42% of the total carbon dioxide emissions [3]. This is because of the domination of fossil fuels as energy sources for electric power generation. Thus, electric power generation has been one of the primary reasons for the global warming. Because of the usage of fossil fuels as the energy source, there has been a constant decline in their reserves. This will lead to the extinction of fossil fuels in the years to come. To reduce the constantly declining fossil fuel reserves, and to combat the hazards of global warming it is essential to reduce the electric power generation by fossil fuels, and start relying on renewable power.

1.3. Solar Power

This section provides a brief description of solar power generation. Solar power can be generated using the technologies explained in the following sections.

1.3.1. Concentrating Solar Power

In Concentrating Solar Power (CSP) technology, the sunlight is allowed to concentrate at one place [4]. The heat generated by the concentration of energy at this place is used to heat solids or fluids, to generate electricity using steam. This technology consists of two major units namely: reflector, and receiver. The reflector unit consists of a number of mirrors that reflect the sunlight and concentrate it onto the receiver. The thermal energy is then used to generate electricity by driving steam turbines or heat engines which are

mechanically coupled to the generators. Based on the way solar power is collected, CSP is classified as follows:

1. Power tower system

   As shown in Figure 1.4, power tower system consists of a number of flat sun – tracking mirrors called heliostats. These heliostats are used to concentrate the sunlight onto the receiver which is on the top of a tower.

2. Linear concentrator system

   As shown in Figure 1.5, linear concentrator system consists of large parabolic mirrors called parabolic troughs. These parabolic troughs are used to concentrate the sunlight onto a linear tube receiver which is placed along the axis of each parabolic trough.

3. Dish/engine system

   As shown in Figure 1.6, dish/engine system consists of parabolic dishes that is used to concentrate sunlight onto a central engine that is used to generate electricity.

1.3.2. Photovoltaic Power Generation

In photovoltaic power generation, photovoltaic cells are used to generate electricity. A photovoltaic cell is a p – n junction diode when exposed to light, generates charge carriers. If the photovoltaic cell is short circuited, there is a flow of current. Typically, the output voltage of each photovoltaic cell is 0.6 – 0.7 V dc. In order to obtain larger dc voltages, a number of such photovoltaic cells are connected in series to form a photovoltaic panel. The output power of the photovoltaic panel is dc. Because the end application of electric power is ac, the output of the photovoltaic panels are connected to power converters. The power converters can be either dc/dc converters, or dc/ac converters, or a combination of both

dc/dc converters and dc/ac converters. Figure 1.7 shows schematic of a typical photovoltaic power generation system [5].

1.4. Thesis Motivation

According to the U.S. Department of Energy (DOE) a photovoltaic system installed at 1$/W, equivalent to 5 cents/kWh, would make solar energy competitive with the wholesale rate of electricity without additional subsidies. Preliminary DOE analysis of required component costs to reach $1/W installed PV system implies the following breakdown: 50 cents/W for the module, 40 cents/W for the balance of system and installation, and 10 cents/W for power electronics [6]. A typical commercially available solar panel [7] rated for ~30Vdc/8Adc when operating at its maximum power point, thus establishes a target cost for power electronics at $25-$30 per panel. Towards optimizing capital costs of power electronics on a per watt basis, central photovoltaic inverters have been designed for bulk applications [8]. Strings of solar panels are connected in series to build up dc voltage and then connected in parallel to scale up to required power level before feeding into a single inverter. An alternative approach is to employ a micro-inverter for every solar panel [9]. Such small inverters convert dc electricity produced by a single solar panel and synthesize required ac voltage. Recently, string inverters have been proposed for residential and small commercial systems [10]. They are smaller than central inverters and process power from only one string of solar panels. However, they are larger than micro-inverters and do not interface with each panel on an individual basis. Historically, it has been observed that employment of central inverters for solar power conversion limits energy yields, whereas employment of micro-inverters has not been commercially attractive for larger volumes [9]. This thesis investigates a unique methodology that converts the conventional dc

voltage output of a photovoltaic solar panel to switched quasi-square wave voltage with variable pulse width, which when aggregated realizes a superior quality multilevel waveform that can be directly interfaced with the power grid. This alternative approach, termed Solar Panel Companion Inverter (SPCI), offers advantages of micro-inverters in realizing panel-level Maximum Power Point Transfer (MPPT) and enhanced controllability. Furthermore, bill of materials for each quasi-square wave H-bridge inverter is fractional as compared to micro-inverter, thus enabling realization of system-level cost benefits of a central inverter approach. However, the barrier for this approach is in synthesis and sequencing of individual quasi-square wave outputs in real time based on a) grid synchronization requirements, and b) employment of varying dc voltage/current levels dictated by MPPT algorithms. Despite these challenges associated with control complexity and power circuit minimization, the motive of this thesis is to investigate a game-changing mechanism for interfacing solar panels with power grid.

1.5. Organization of Thesis

This section presents an overview of the organization of thesis as follows.

Chapter 1: Introduction

This chapter starts by stressing the importance of renewable power generation in Section 1.2. In Section 1.3, it presents Concentrating Solar Power (CSP), and Photovoltaic Power generation as the two ways in which solar energy can be harvested. Section 1.4 presents the motivation for the thesis, and Section 1.5 presents the organization of the thesis.

Chapter 2: Literature Review of Photovoltaic Inverters

In this chapter, a survey of scholarly publications of various photovoltaic power conversion technologies are presented. This chapter starts with a review of central inverter, string

inverter, micro inverter, and multilevel inverter topologies presented in Section 2.2, Section 2.3, Section 2.4, and Section 2.5 respectively. Section 2.6 presents a review of various special photovoltaic power conversion techniques. A review of maximum power point tracking schemes is presented in Section 2.7.

Chapter 3: Solar Panel Companion Inverter

In this chapter, topology and circuit schematic of the proposed Solar Panel Companion Inverter (SPCI) is presented. In Section 3.2, a methodology to synthesize an output ac voltage is described. Detailed circuit schematic of SPCI and its operation is described in the Section 3.3.

Chapter 4: Control Strategies for Solar Panel Companion Inverter

In this chapter, detailed descriptions of various control strategies namely: Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM) are explained in Section 4.2, Section 4.3, and Section 4.4 respectively.

Chapter 5: Modeling of a Grid Connected Solar Panel Companion Inverter

This chapter presents the model of a grid connected Solar Panel Companion Inverter (SPCI). Section 5.2 describes a block diagram of grid connected SPCI. Matlab Simulink model of solar panel, power grid, Phase Locked Loop (PLL), reference voltage construction, and SPCI are explained in Section 5.3, Section 5.4, Section 5.5, Section 5.6, and Section 5.7 respectively. Master controllers for Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM) control strategies are described in Section 5.8, Section 5.9 and Section 5.10 respectively.

Chapter 6: Simulation Results

In this chapter, operating scenarios of Solar Panel Companion Inverter (SPCI), and simulation results for various scenarios and control strategies are presented. Section 6.2 describes the operating scenarios and explains the terms such as mean, coefficient of variation, and percentage yield, that are used to evaluate the control strategies, namely: Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM). An example showing the calculation of mean and coefficient of variation is also presented. In Section 6.3, simulation results for various operating scenarios corresponding to UPWM, SSCM, and SPWM, along with a discussion of the simulation results are presented.

Chapter 7: Comparative Analysis of Control Strategies and Master Selector

In this chapter, a comparative analysis of the control strategies for Solar Panel Companion Inverter, namely Unsorted Pulse Width Modulation, Sorted Stair Case Modulation, and Sorted Pulse Width Modulation is done for various operating scenarios. This analysis is performed to identify the optimal control strategy for a given operating scenario. Operating space of Solar Panel Companion Inverter (SPCI) is described in Section 7.2. Comparative analysis of the control strategies is explained in Section 7.3. Advantage of SPCI as compared to existing solar power converters as reviewed in Chapter 2 are explained in Section 7.4. Implementation of control strategy selection is presented in Section 7.5, and its simulation results are presented in Section 7.6.

Chapter 8: Conclusion

This chapter presents the conclusions drawn from the simulation results presented in Chapter 6, and comparative evaluation of control strategies performed in chapter 8. Future scope and the recommendations are also presented.

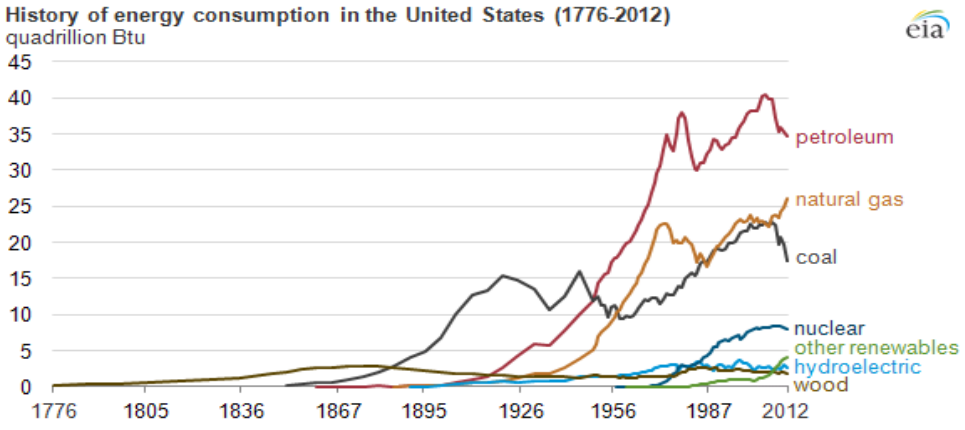


FIGURE 1.1: History of energy consumption in United States, source: U.S. energy information administration (July 2013) [1].

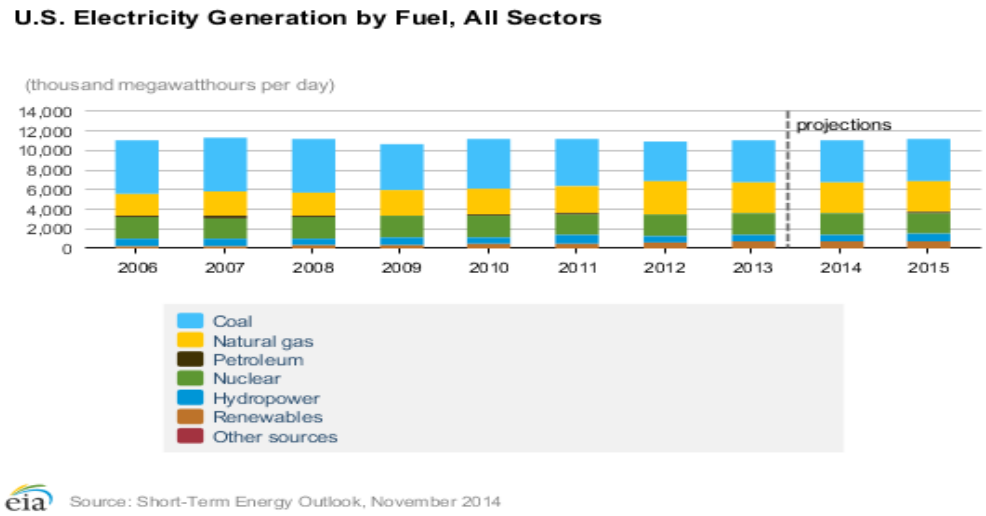


FIGURE 1.2: Electricity generation in United States, by the source of energy, source: short – term energy outlook (November 2014) [2].

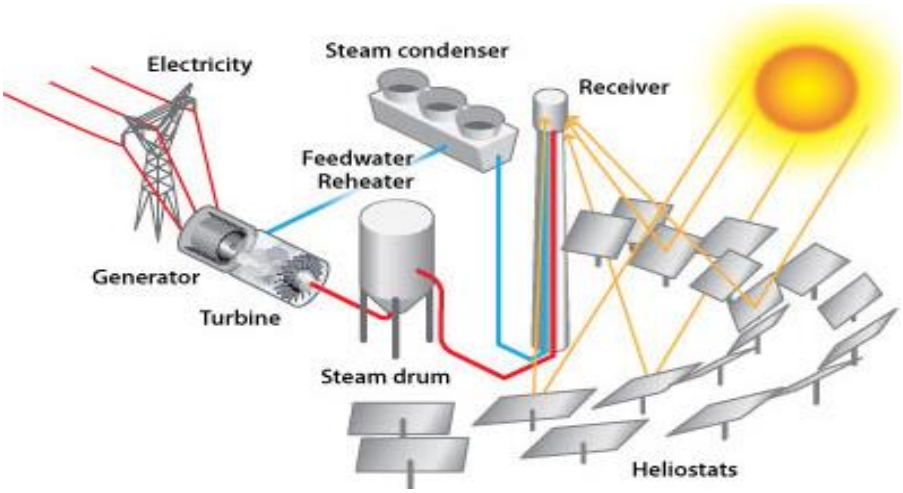


FIGURE 1.3: Schematic showing a power tower system for solar power generation using concentrating solar power technology [4].

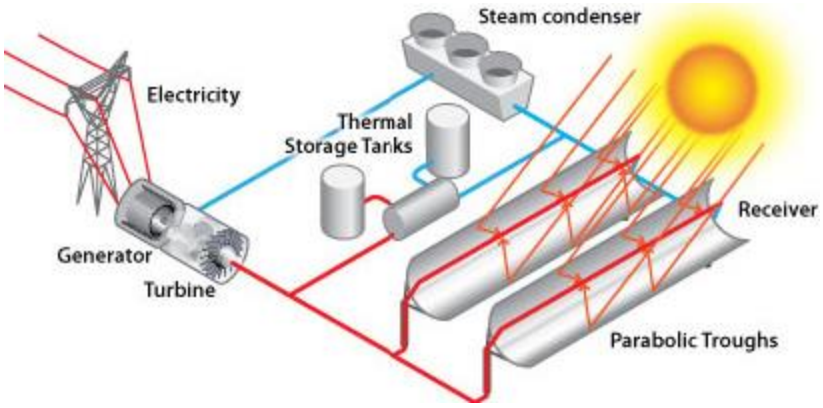


FIGURE 1.4: Schematic showing a linear concentrator system for solar power generation using concentrating solar power technology [4].

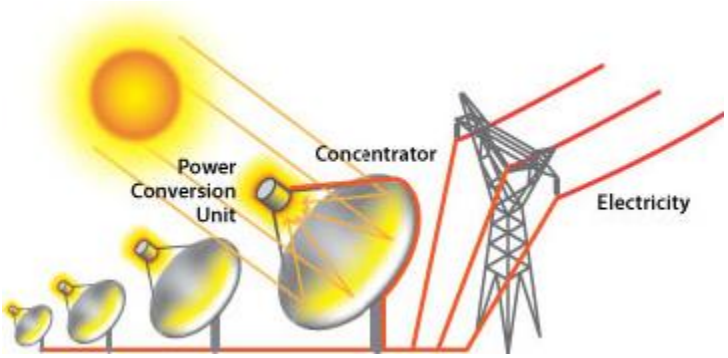


FIGURE 1.5: Schematic showing a dish/engine system for solar power generation using concentrating solar power technology [4].

FIGURE 1.6: Schematic showing a photovoltaic power generation system [5].

CHAPTER 2 : LITERATURE REVIEW OF PHOTOVOLTAIC INVERTERS

2.1. Introduction

This chapter includes a survey of scholarly publications of various photovoltaic power conversion technologies. A review of central inverter, string inverter, micro inverter, and multilevel inverter topologies are presented in Section 2.2, Section 2.3, Section 2.4, and Section 2.5 respectively. Section 2.6 presents a review of various special photovoltaic power conversion techniques. A review of maximum power point tracking schemes is presented in Section 2.7.

2.2. Central Inverter

Central inverter photovoltaic inverter topology is termed as the past technology of photovoltaic inverters [11]. Figure 2.1 shows the topology of a central inverter, wherein a number of photovoltaic panel modules are connected in series (called a string), to build up the dc voltage. A number of such strings are connected in parallel to scale up to the required power level before feeding it into a single inverter [8][12].

A standard control scheme to drive the central inverter in order to ensure maximum dc power extraction is shown in Figure 2.2 [13]. This strategy is based on two cascaded control loops using pulse width modulation scheme. In this methodology, there is an inner current loop which establishes the duty ratio to generate a sinusoidal output current that is in phase with the grid voltage. Irrespective of the variations in temperature and solar irradiance, the output voltage loop has to settle the operating point of the photovoltaic array at its

maximum power value. This can be performed by implementing Perturb and Observe Maximum Power Point Tracking (MPPT) algorithm [14]. The outer loop delivers the amplitude of reference current corresponding to maximum power point operation of photovoltaic array.

The advantage of central inverter topology is low cost per watt, high overall efficiency and easy to install due to the presence of only one inverter system [12]. The main drawback of central inverter is that it offers low yield of dc power output from the solar panels when there is an irradiance mismatch, as there is no panel level Maximum Power Point Tracking (MPPT). Also this configuration suffers from a drawback arising from a single point of failure [15]. Another drawback of this topology is that high voltage dc cables are necessary for connecting the modules and the inverter.

Figure 2.3 shows central inverter with a dc/dc conversion stage at module level [9]. A buck – boost dc/dc converter is employed in this scheme, as it allows each module to operate at maximum power point by simultaneously maintaining a constant string dc voltage. The output current for all dc/dc converters is the same. Depending on the available solar power of the connected module, the output voltage of each dc/dc converter is adjusted. Buck conversion is employed for the modules with low available power, while boost conversion is employed for modules with high available power. The output voltage of each dc/dc converter is added up to a constant string dc voltage. The issue of reduced power extraction due to irradiance mismatch is resolved, since there is a maximum power point operation at module level. However, the drawbacks arising from single point of failure, and the necessity of high voltage dc cables for connecting the modules with the inverter still prevails in this configuration.

2.3. String Inverter

String inverter topology is termed as the present technology of photovoltaic inverters [11]. Figure 2.4 shows the topology of a string inverter, wherein a number of photovoltaic panel modules are connected in series to build up dc voltage and form a string [15]. In this topology, the string voltage must be higher than the peak value of the grid voltage. Each string is connected to an inverter, and a number of such string inverters can be connected to the grid. Maximum power point tracking is applied to each string. Thus, this methodology offers better yield when compared to that of a central inverter, whenever there is a power mismatch.

Figure 2.5 shows the schematic of inverter current control strategy adopted for string inverter topology [16]. In this strategy, incremental conductance method is employed for maximum power point tracking, and generate a reference current. This reference current is used by the proportional – resonant controller for controlling the inverter. The disadvantage of String inverter topology is the cost of installation is more than central inverters, because of the usage of several inverters.

String inverter topology is extended to multi – string inverter topology as shown in figure 2.6 [9][15]. In multi – string inverter topology, each string consists of a dc/dc converter that performs maximum power point tracking at string level. Though the string inverters, and multi – string inverters offer better yield than central inverters, the problem of reduction in the yield still persists due to the power mismatch.

2.4. Micro Inverter

Module – level dc/ac conversion is termed as the future technology of photovoltaic inverters [11]. Module – level dc/ac conversion is implemented using micro inverter

topology [9]. Figure 2.7 shows the simplified schematic of a micro inverter system. This topology consists of a dc/dc boost conversion stage, to step up the module voltage of 30 – 35 V at maximum power point operation. This is done because the module voltage is low when compared the rms ac voltage of the utility grid. The dc/dc boost converter makes sure that the panel is operating at maximum power point.

With micro inverter topology, usage of dc wiring is eliminated, since the inverters are directly connected to the photovoltaic modules, and the output coming from the inverter is ac. Furthermore, the system is modular because, additional modules when required can be added to the system by connecting them in parallel to the already installed modules. This topology also offers better yield than central and string topologies because, in micro inverter maximum power point tracking can be performed at module level. The issue related to single point of failure can be mitigated in this system [17].The disadvantage of this topology is that the price per watt is more than central and string inverter topologies because of the employment of more dc/dc converters, and inverters [15].

2.5. Multilevel Inverter

An overview of different multilevel inverter topologies, along with the investigation of their stability for single phase grid connected photovoltaic systems is presented in [18]. The topologies that are presented are as follows:

(i) Half – bridge diode clamped inverter topology

A grid connected photovoltaic system with half – bridge diode clamped three level inverter is shown in Figure 2.8. A positive voltage can be generated at the inverter output terminal by simultaneously turning on the switches S1 and S2. By simultaneously turning on the switches S2 and S3, a zero voltage can be generated.

Negative voltage can be generated by simultaneously turning on the switches S3 and S4. For the power to transfer from the photovoltaic system into the grid, dc bus voltages of the solar panels must be higher than the magnitude of grid voltage. The advantage of this topology is that the grounded photovoltaic array eliminates capacitive earth currents.

The three – level inverter can be expanded to a five – level inverter as shown in Figure 2.9. By increasing the number of levels, the harmonic content can be reduced in the output voltage waveform. The disadvantage of five – level topology is that more number of switches are required. Also, the loading on the outer photovoltaic sub array (solar panel1 and solar panel4) is different from that of the photovoltaic sub array (solar panel2 and solar panel3). Thus, care should be taken while sizing each sub array to ensure maximum power extraction from each sub array.

(ii) Full – bridge single leg clamped inverter topology

Figure 2.10 shows a grid connected photovoltaic system with full – bridge single leg switch clamped inverter topology. This topology consists a full – bridge (realized with the switches Sa1, Sa2, Sb1, Sb2), and a bi – directional switch (realized with the switches Sa3, Sa4, Da1, Da2). This bi – directional switch controls the flow of current flow from the mid – point of the dc bus. The diodes Da1 and Da2, and the switches Sa3 and Sa4 can be rated for half the blocking voltages of the remaining switches (Sa1, Sa2, Sb1, and Sb2).

Figure 2.11 shows a photovoltaic system connected to the grid with full – bridge single leg diode clamped inverter topology. In this topology, the diodes Da1 and Da2, along with the switches Sa1, Sa2, Sa3, and Sa4 can be rated for half the blocking

voltages of the switches Sb1 and Sb2. In both the topologies shown in Figure 2.10 and Figure 2.11, the photovoltaic sub arrays are symmetrically loaded.

(iii) Cascaded inverter topology

A five – level full bridge cascaded inverter topology is shown in Figure 2.12. This topology consists of two full bridges, connected with a solar panel each on the dc side. Three – level ac output voltage can be synthesized from each full bridge. Outputs of the two bridges are connected in series so as synthesize a five – level ac output voltage. The advantage of this topology is its modularity. The Solar Panel Companion Inverter presented in this thesis can be categorized under the cascaded inverter topology.

(iv) Step converter topology

Step converter topology for grid connected photovoltaic system is shown in Figure 2.13. It consists of five arrays with nominal voltages of 11V, 22V, 44V, 88V, 176V. The power conversion consists of two stages. In the first stage, a rectified ac voltage waveform with 32 different voltage levels is generated. In the second stage, the polarity of every second half wave is switched to generate a 63 – level ac output voltage. For maximum power extraction, the sizing of each photovoltaic sub array has to be different.

(v) Magnetic coupled inverter topology

Figure 2.14 shows a grid connected photovoltaic system with magnetic coupled inverter topology. This inverter consists of three full bridges. Each full bridge can generate three different voltage levels. The output of each full bridge is connected to the primary winding of a transformer. The secondary windings of all the three transformers are connected in series. The turns ratio of the transformers are different.

Thus an ac output voltage comprising of 27 levels can be synthesized. The advantage of this topology is that an accurate replica of sine wave can be synthesized. The drawback is that it requires three transformers.

(vi) Flying capacitor inverter topology

A grid connected photovoltaic system with half bridge three – level flying capacitor inverter is shown in Figure 2.15. For the inverter operation, it is essential that the voltage across each solar panel should be equal to the voltage across the capacitor, C2.Thus it should be made sure that the average current of the capacitor C2 is zero, by applying suitable control methods.

A single phase, multistring 5 – level inverter topology for grid connected photovoltaic system is presented in [19]. As shown in Figure 2.16, this topology consists of three photovoltaic strings. Each string consists of a dc/dc boost converter connected to a common dc bus. The proposed configuration generates output voltage in five levels (0, $+V_{dc}/2$, V_{dc}, $-V_{dc}/2$, $-V_{dc,}$ where V_{dc} is the dc bus voltage of the inverter). The auxiliary circuit consisting of four diodes (D4, D5, D6, and D7) and a switch (S4) is used to generate $+V_{dc}/2$ and $-V_{dc}/2$ voltage levels. Carrier based sinusoidal pulse width modulation is employed in this topology. Switches S4, S5, and S6 are operated at the frequency of carrier wave. Switches S7, and S8 are operated at fundamental frequency. String level maximum power point tracking is performed by the dc/dc boost converters. A comparison between 3 – level and 5 – level inverter topologies is performed in terms of efficiency and Total Harmonic Distortion (THD). The reported efficiency of a 3 – level topology is 90%, while that of a 5 – level topology is 86% at an operating power of 960 W. For an operating power of 360W, the efficiency of 3 – level topology reduced to 89%, whereas for 5 – level topology the

efficiency reduced to 84%. The decrease in the efficiency is attributed to the increase in switching losses because of the increase in number of switches. The percentage THD for 3 – level topology is reported as 9.5%, while that of 5 – level topology is 5.7%. Thus, with the increase in the number of voltage levels in the inverter output, the percentage THD also decreases.

An eleven – level grid connected inverter interfaced with solar panels is presented in [20]. Figure 2.17 shows an overview of a grid tied eleven - level inverter interfaced with solar panels. The dc output power of each solar panel is proportional to solar irradiance incident on each of the solar panel. With an assumption that there is a mismatch in irradiance incident on all the panels, level shifted sinusoidal pulse width modulation strategy, which is improved and called Sorted Pulse Width Modulation strategy (discussed in Section 4.4 of Chapter 4) is implemented. For an N – level inverter, the control strategy shifts the carrier signal over ((N – 1)/2 cycles. Synchronization between the inverter and grid is achieved by sensing the grid voltage through Phase Locked Loop (PLL). Optimal point of operation of the panel is determined by calculating the output power and phase angle variation. The MPPT algorithm monitors the output voltage and current parameters by applying small changes to the phase angle and checking the power variation, in order to track the maximum power point.

Reference [21] presented the control strategies that can be applied to a multilevel inverter. Multilevel Selective Harmonic Elimination (MSHE), Multilevel Level Shifted Carrier – Based Pulse Width Modulation, Multilevel Phase Shifted Carrier – Based Pulse Width Modulation, and Multilevel Space Vector Modulation (MSVM) are discussed. Implementing MSHE by considering one commutation angle per cycle would result in a

modulation strategy similar to Sorted Stair Case Modulation (SSCM) which is discussed in Section 4.3 of Chapter 4. Multilevel Level Shifted Carrier – Based Pulse Width Modulation strategy is similar to Sorted Pulse Width Modulation (SPWM) strategy explained in Section 4.4 of Chapter 4.

2.6. Special Photovoltaic Power Conversion Technologies

In this section, a review of special photovoltaic conversion technologies is presented.

(i) Single – phase current source inverter in three leg configuration

A current source inverter topology for photovoltaic applications which eliminates low frequency (100 Hz /120 Hz) current ripples (common in single phase voltage source inverter) is proposed in [22]. The topology consists of six bidirectional switches (Sa1, Sa2, Sb1, Sb2, Sc1, and Sc2) in three leg configuration as shown in Figure 2.18. Each bidirectional switch is a series combination of an Insulated – gate Bipolar Transistor (IGBT), and a diode. Leg a and leg b of the inverter are connected to the grid through an LC filter (Lf and Cf). The leg b is connected to the leg c through a capacitor, Cb. Maintenance of a constant instantaneous power flow across the bridge by controlling the current flowing through leg b has been proposed. The magnitude and phase of the current flowing through leg b, in order to ensure constant power flow is given by Equation (2.1).

$$I_b = \sqrt{\omega C_b V_a I_a} \; ; \; \phi_{ib} = \frac{1}{2}(\phi - \frac{\pi}{2}) \tag{2.1}$$

(ii) Photovoltaic inverter with Silicon Carbide transistors

Photovoltaic inverter using Silicon Carbide (SiC) is implemented in [23]. SiC Normally – off Junction Fields Effect Transistors (JFETs) offer great potential for reducing the overall cost of the inverter by increasing efficiency and decreasing the size of heat sink and inductive components. It claims that because of low switching losses SiC transistors, the

switching frequency of SiC transistor based photovoltaic inverters can be raised by three – nine times compared to the conventional inverters. Thus a simultaneous reduction (almost by the same factor) in the size inductive components can be achieved. The topology is reported to be 99% efficient, which is 1 – 1.5% more than the commercially available single phase inverters could be reached.

(iii) Half – bridge inverter with generation control circuit

Half – bridge inverter with generation control circuit is shown in Figure 2.19 [24]. With this topology it is possible to synthesize a grid synchronized sinusoidal ac output current and also operate photovoltaic modules independently, at maximum power point. The generation control circuit consists of multi – stage buck – boost circuit. Each buck – boost stage is connected in parallel with a photovoltaic module. The generation control circuit makes it possible to operate each photovoltaic module, independently at maximum power point. Thus the proposed topology can compensate for the reduction in output power caused by the shadow partially covering the photovoltaic modules. The generation control circuit on each of the photovoltaic modules is executed by detecting the total output power of the photovoltaic system. MPPT algorithm for the proposed system makes each of the photovoltaic modules able to generate its maximum power by simply detecting the output power of the total generation system, and hence the number of power detectors can be reduced compared with conventional system.

(iv) Zero current switching inverter

Reference [25] proposes a zero current switching inverter for grid connected photovoltaic inverter system as shown in Figure 2.20. It is claimed that in this topology, a

zero current switching condition is provided for all the switches which reduces the switching losses. A full load efficiency of 97.5% is reported for a 1.2kW prototype.

2.7. Maximum Power Point Tracking Schemes

The following Maximum Power Point Tracking (MPPT) techniques are presented in reference [14]:

(i) Perturb and Observe (P&O)

In P&O, a perturbation in the duty ratio of the power converter is performed in order to change the operating voltage and the operating current. Figure 2.21 shows typical P – V characteristics of a photovoltaic module. The operating point where the output power is maximum is shown by the point MPP. When the photovoltaic module is operating towards the left of MPP, an increase in voltage increases the operating power whereas, a decrease in voltage decreases the operating power. When the photovoltaic module is operating towards the right of MPP, an increase in voltage decreases the operating power whereas, a decrease in voltage increases the operating power. Thus, towards reaching MPP, if there is an increase in operating power, the subsequent perturbation should be kept the same. The perturbation should be reversed, if there is a decrease in operating power. The perturbation is done till the photovoltaic module operates at MPP.

(ii) Incremental Conductance

Incremental Conductance technique is based on Equations (2.2), (2.3), and (2.4).

$$\text{At MPP, } dP/dV=0 \tag{2.2}$$

$$\text{Left of MPP, } dP/dV>0 \tag{2.3}$$

$$\text{Right of MPP, } dP/dV<0 \tag{2.4}$$

where V is the instantaneous operating voltage, P is the instantaneous operating power, dP/dV is the slope of the P – V curve shown in Figure 2.21. If operating point of the photovoltaic module MPP, the slope is zero. If the operating point is to the left of MPP, the slope is positive. And if the operating point is to the right of MPP, the slope is negative.

If I is the instantaneous operating current, since P=IV,

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \cong I + V\frac{\Delta I}{\Delta V} \tag{2.5}$$

Therefore Equations (2.2), (2.3), (2.4) can be written as

$$\text{At MPP, } \Delta I / \Delta V = -I / V \tag{2.6}$$

$$\text{Left of MPP, } \Delta I / \Delta V > -I / V \tag{2.7}$$

$$\text{Right of MPP, } \Delta I / \Delta V < -I / V \tag{2.8}$$

where I/V is the instantaneous conductance, and ΔI/ΔV is the incremental conductance. Figure 2.22 shows the flow chart of incremental conductance algorithm to track the maximum power point, where the MPP is tracked by comparing instantaneous conductance with the incremental conductance.

(iii) Fractional Open – Circuit Voltage

Fractional Open – Circuit Voltage scheme is based on an approximation that the voltage at maximum power point, V_{MPP} is directly proportional to the open circuit voltage, V_{OC}. Equation (2.9) describes the relation between V_{MPP} and V_{OC}.

$$V_{MPP} = k_1 V_{OC} \tag{2.9}$$

where k_1 is proportionality constant which depends on the characteristics of the photovoltaic system. The value of k_1 for a photovoltaic system is computed by empirically determining V_{MPP} and V_{OC} at different temperatures and solar irradiance. After determining

the V_{MPP} from Equation (2.9), a closed loop control can be implemented on the power converter, to reach the desired operating MPP voltage.

(iv) Fractional Short – Circuit Current

Similar to Fractional Open – Circuit Voltage scheme, Fractional Short – Circuit Current scheme is based on the approximation that the current at maximum power point, I_{MPP} is directly proportional to the short circuit current, I_{SC}. Equation (2.10) describes the relation between I_{MPP} and I_{SC}.

$$I_{MPP} = k_2 I_{SC} \tag{2.10}$$

where k_2 is proportionality constant which depends on the characteristics of the photovoltaic system. The value of k_2 for a photovoltaic system is computed by empirically determining the I_{MPP} and I_{SC} at different temperatures and solar irradiance. In order to reach the desired operating MPP current, a closed loop current control can be implemented on the power converter.

(v) Current Sweep

In Current Sweep Maximum Power Point Tracking (MPPT) scheme, the I – V characteristic of the photovoltaic array is obtained and updated at fixed intervals by using a current sweep waveform for photovoltaic array. Voltage at maximum power point is computed from the I – V characteristic at the same interval. Equation (2.11) shows the function for the current sweep waveform.

$$f(t) = k_3 \frac{df(t)}{dt} \tag{2.11}$$

It can be seen in the Equation (2.11) that the current sweep function is directly proportional to its derivative, and k_3 is the proportionality constant. The photovoltaic array power can be written as:

$$p(t) = v(t)i(t) = v(t)f(t) \tag{2.12}$$

At maximum power point,

$$\frac{dp(t)}{dt} = 0 \tag{2.13}$$

$$\frac{dp(t)}{dt} = v(t)\frac{df(t)}{dt} + f(t)\frac{dv(t)}{dt} = 0 \tag{2.14}$$

Substituting Equation (2.11) in Equation (2.14),

$$\frac{dp(t)}{dt} = \left[v(t) + k_3 \frac{dv(t)}{dt} \right] \frac{df(t)}{dt} = 0 \tag{2.15}$$

The solution to the differential equation obtained in Equation (2.15) can be written as:

$$f(t) = I_{max} \exp(t / k_3) \tag{2.16}$$

where I_{max} is the maximum current in the photovoltaic array. Since i(t)= f(t), diving Equation (2.15) with di(t)/dt,

$$\frac{dp(t)}{di(t)} = v(t) + k_3 \frac{dv(t)}{dt} = 0 \tag{2.17}$$

After the voltage at maximum power point is computed using current sweep, Equation (2.17) can be used to verify whether the maximum power point has been reached.

(vi) DC – Link Capacitor Droop Control

For photovoltaic systems connected in parallel with the grid, as shown in Figure 2.23, DC – Link Capacitor Droop Control is used. If V is the voltage across the photovoltaic array, V_{link} is the voltage across the dc link, then Equation (2.18) describes the duty ratio for a boost converter.

$$d = 1 - \frac{V}{V_{link}} \tag{2.18}$$

Keeping V_{link} constant, if the inverter current increases, the output power of the photovoltaic array increases. With the increase in inverter current, if the power required by the inverter exceeds the maximum power point of the photovoltaic array, V_{link} starts drooping. The current I_{peak} is kept at maximum power point by a feedback line current control, to optimize the duty ratio, d, and prevent V_{link} from drooping.

2.8. Discussion

From the literature review, it can be inferred that there are topologies like the central inverter configuration which are economical. However, these offer a very low yield under non – uniform irradiance conditions because of the absence of panel level maximum power point tracking realization. On the other hand, there are topologies like the micro – inverter which offer a very good yield under non – uniform irradiance conditions because of the panel level maximum power point tracking realization. However, such configurations are not economical. Thus there appears to be a configuration where a panel level maximum power point can be realized, by simultaneously reducing the installation costs. But, there exists a complexity in the realization of control scheme for the configuration. This thesis investigates the possibility of existence of such a configuration.

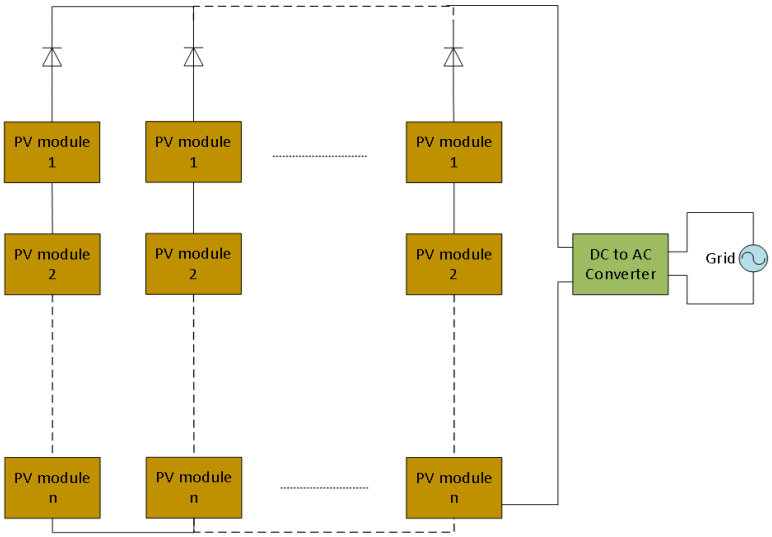


FIGURE 2.1: Simplified block schematic showing grid connected central inverter topology [8][12].

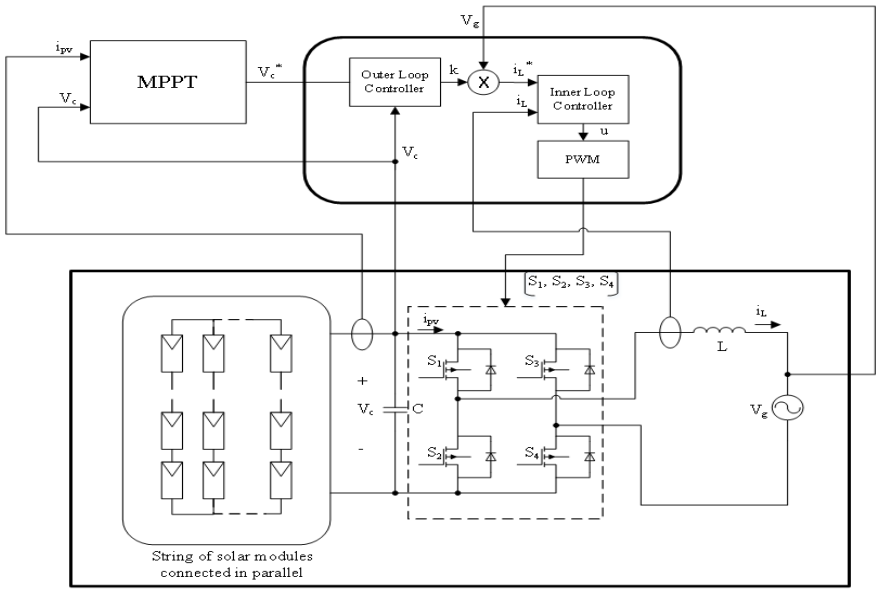


FIGURE 2.2: Control schematic for central inverter topology [13].

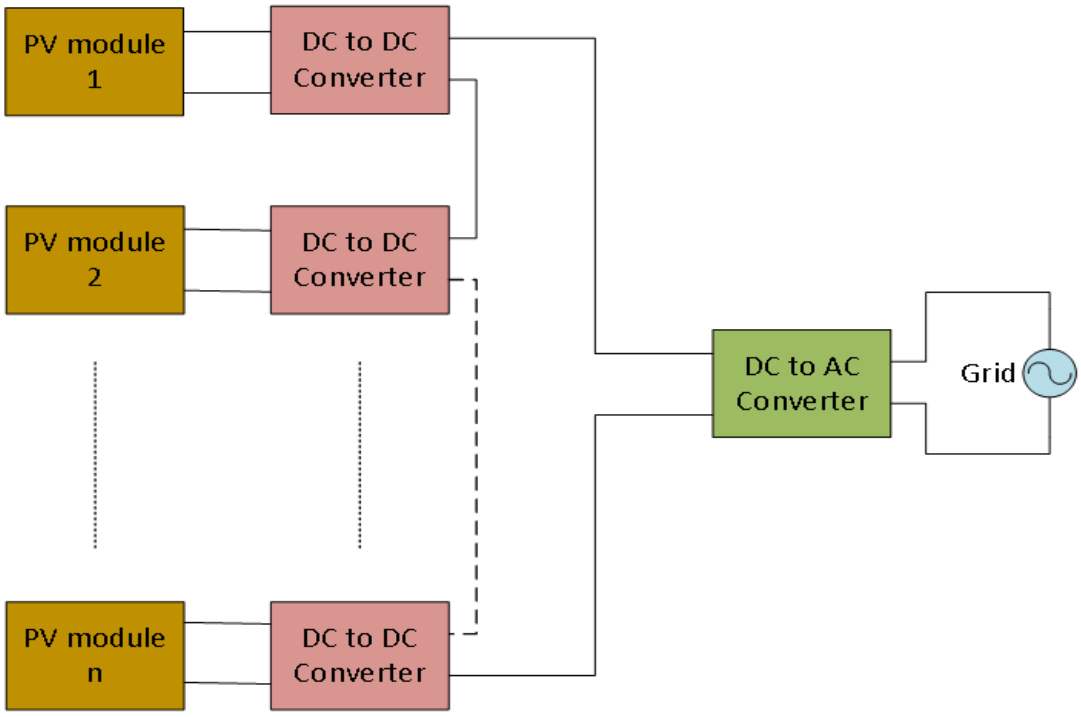


FIGURE 2.3: Simplified block schematic showing grid connected central inverter topology with panel level dc-dc buck – boost converters [9].

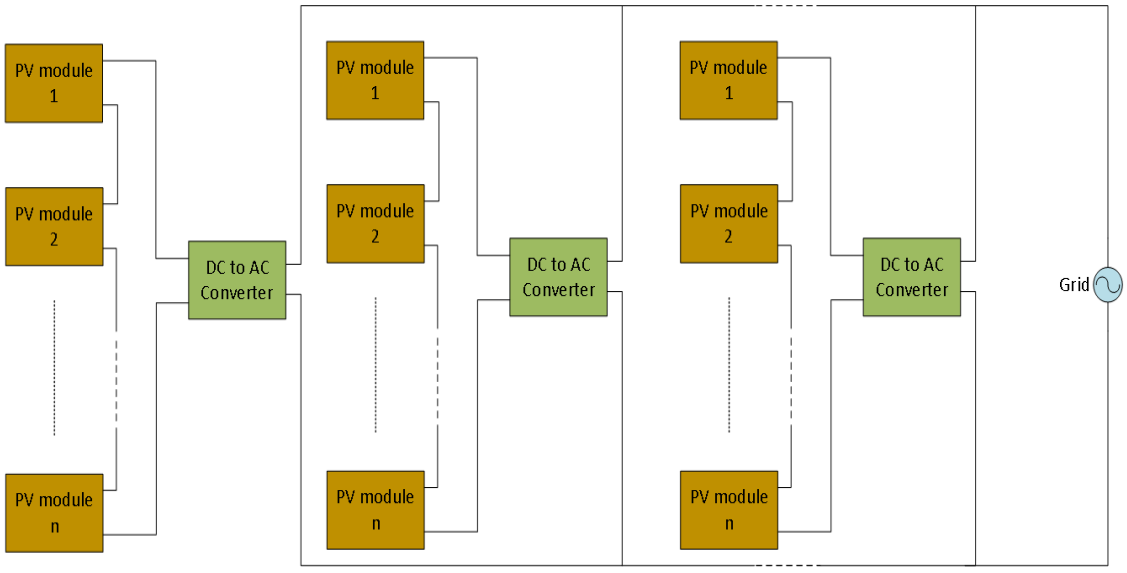


FIGURE 2.4: Simplified block schematic showing grid connected string inverter topology [15].

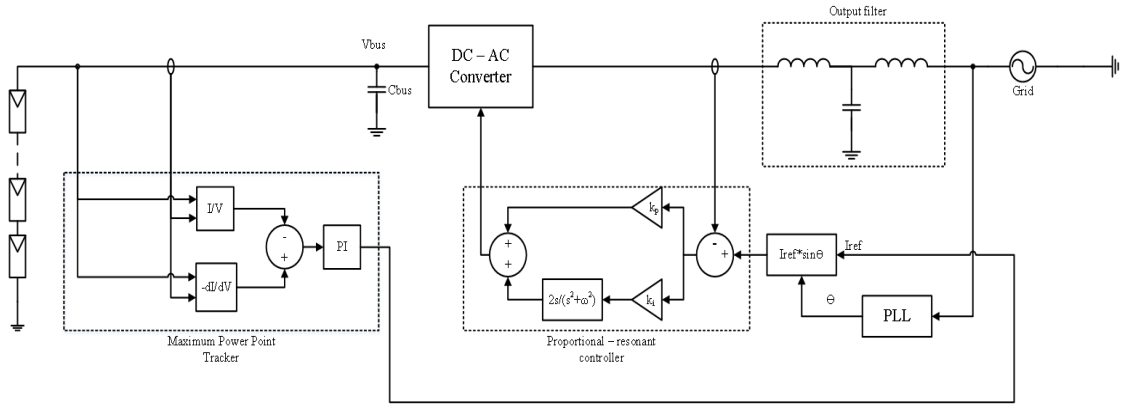


FIGURE 2.5: Control schematic for string inverter topology [16].

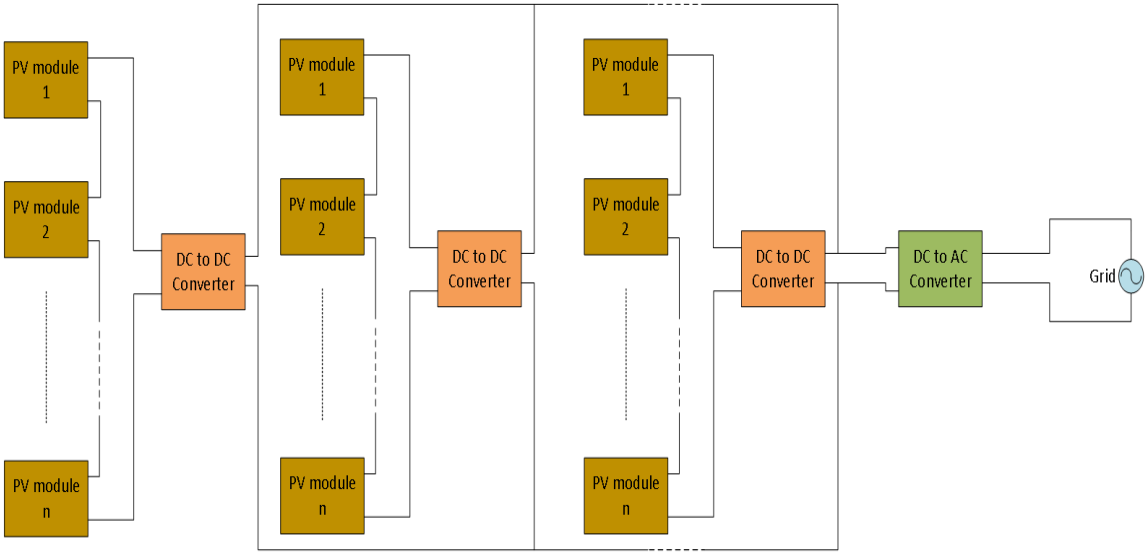


FIGURE 2.6: Simplified block schematic showing grid connected string inverter topology with a dc/dc conversion stage at string – level [9][15].

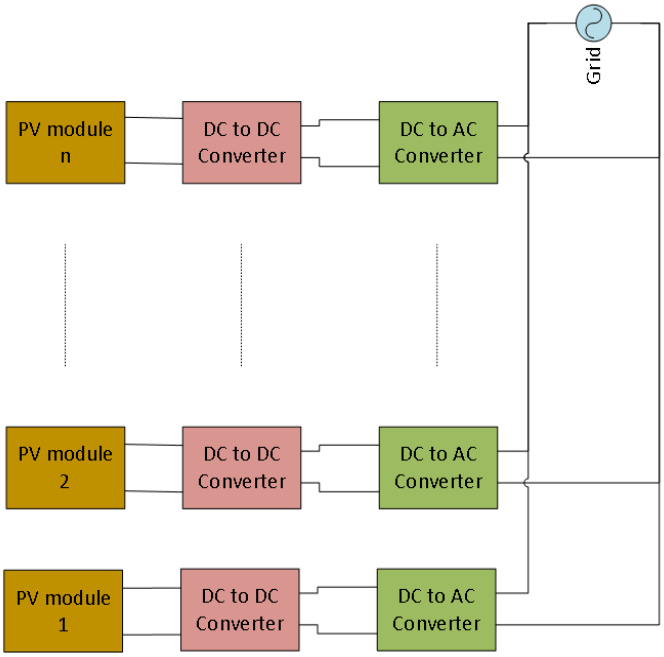


FIGURE 2.7: Simplified block schematic showing grid connected micro inverter topology [9].

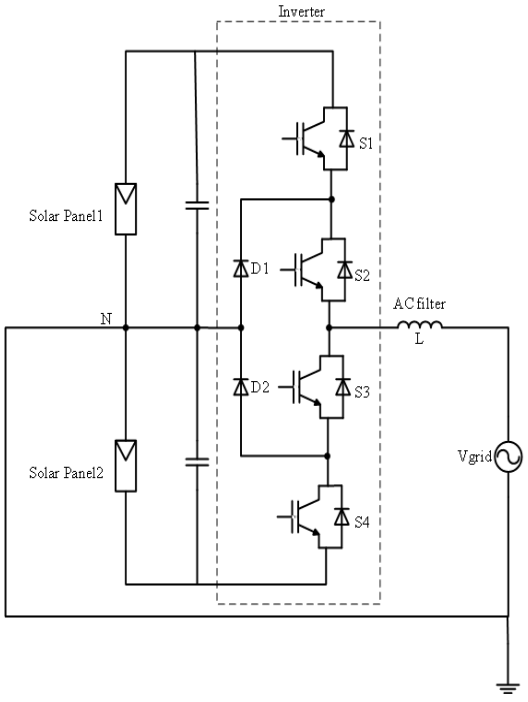


FIGURE 2.8: Circuit schematic of grid connected photovoltaic system with half – bridge diode clamped three – level inverter [18].

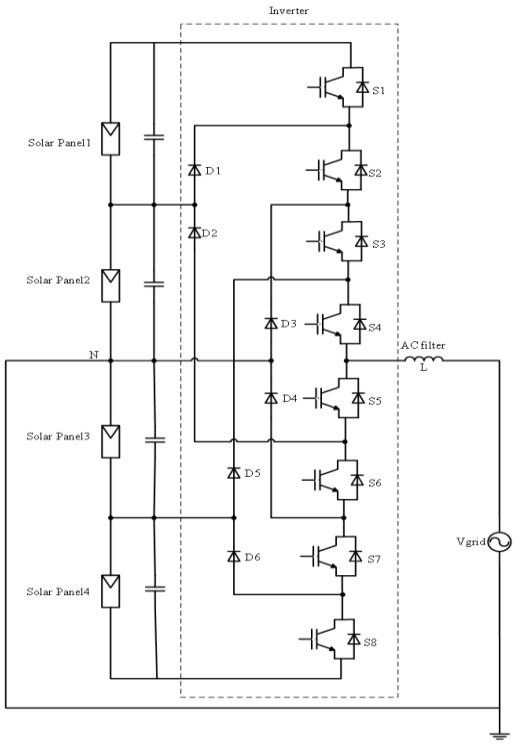


FIGURE 2.9: Circuit schematic of grid connected photovoltaic system with half – bridge diode clamped five – level inverter [18].

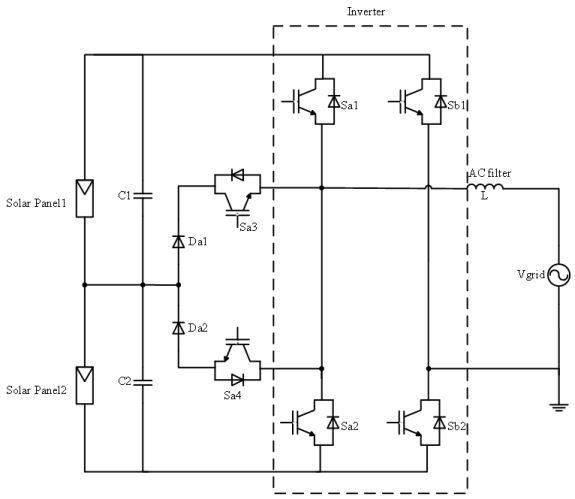


FIGURE 2.10: Circuit schematic of grid connected photovoltaic system with full – bridge single leg switch clamped inverter [18].

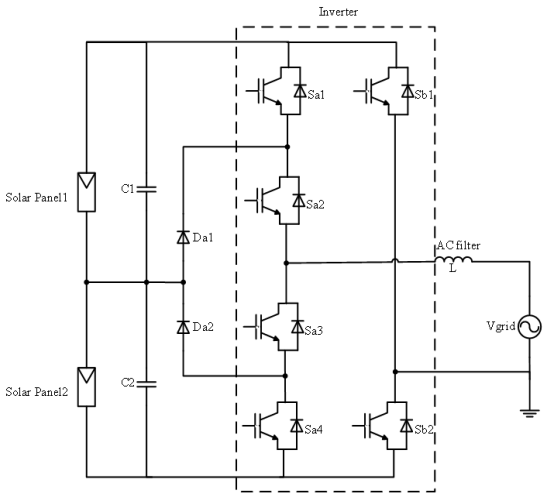


FIGURE 2.11: Circuit schematic of grid connected photovoltaic system with full – bridge single leg diode clamped inverter [18].

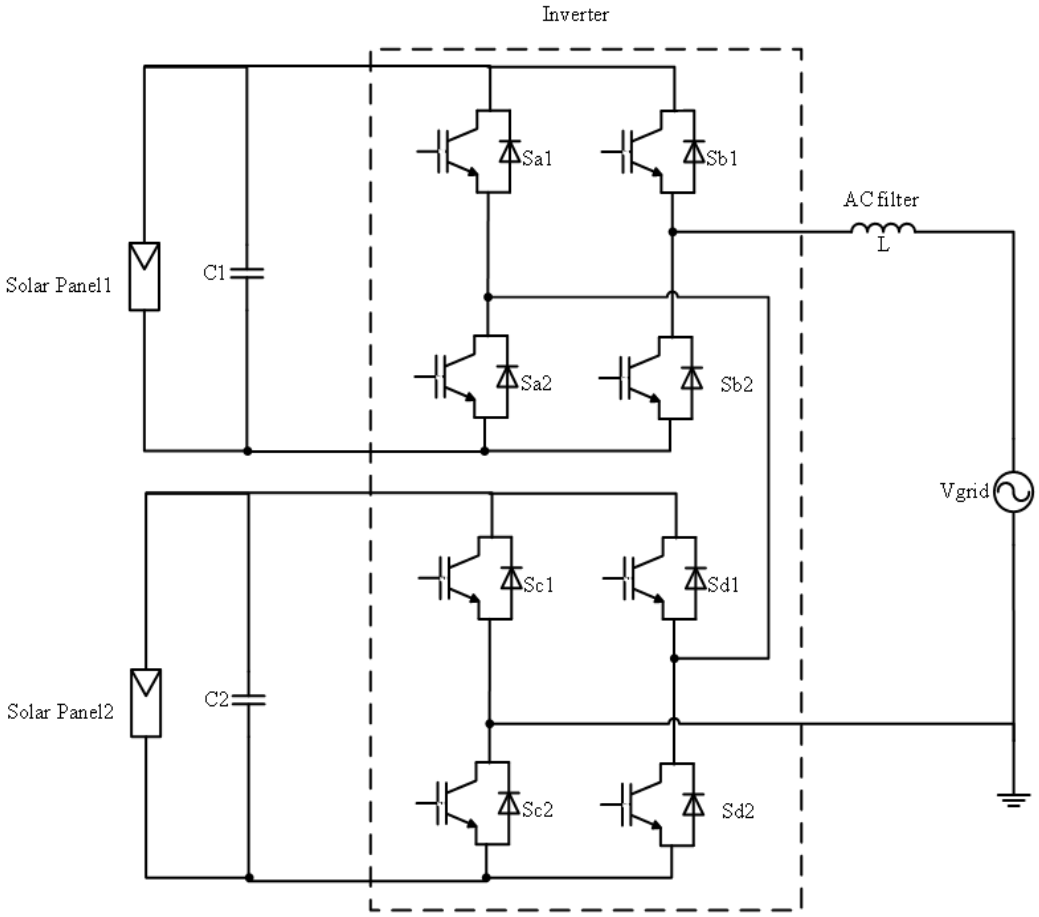


FIGURE 2.12: Circuit schematic of grid connected photovoltaic system with cascaded inverter [18].

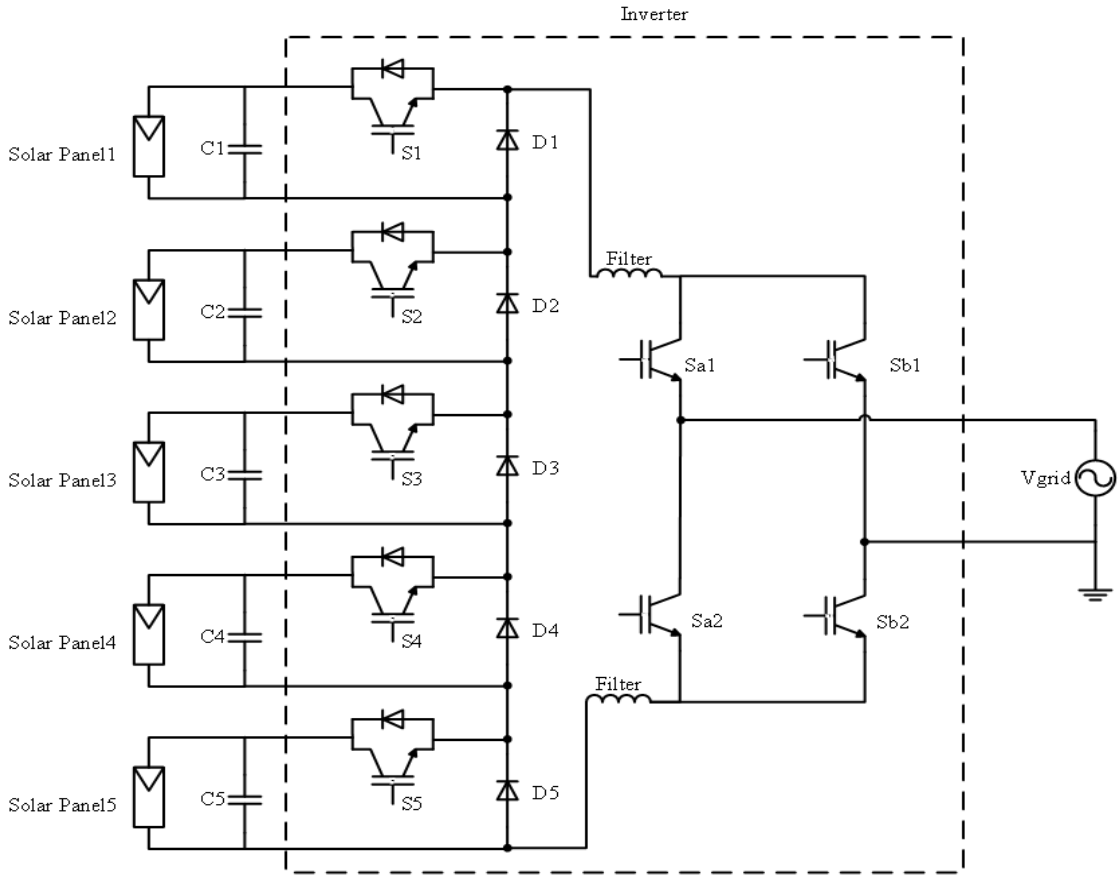


FIGURE 2.13: Circuit schematic of grid connected photovoltaic system with step inverter [18].

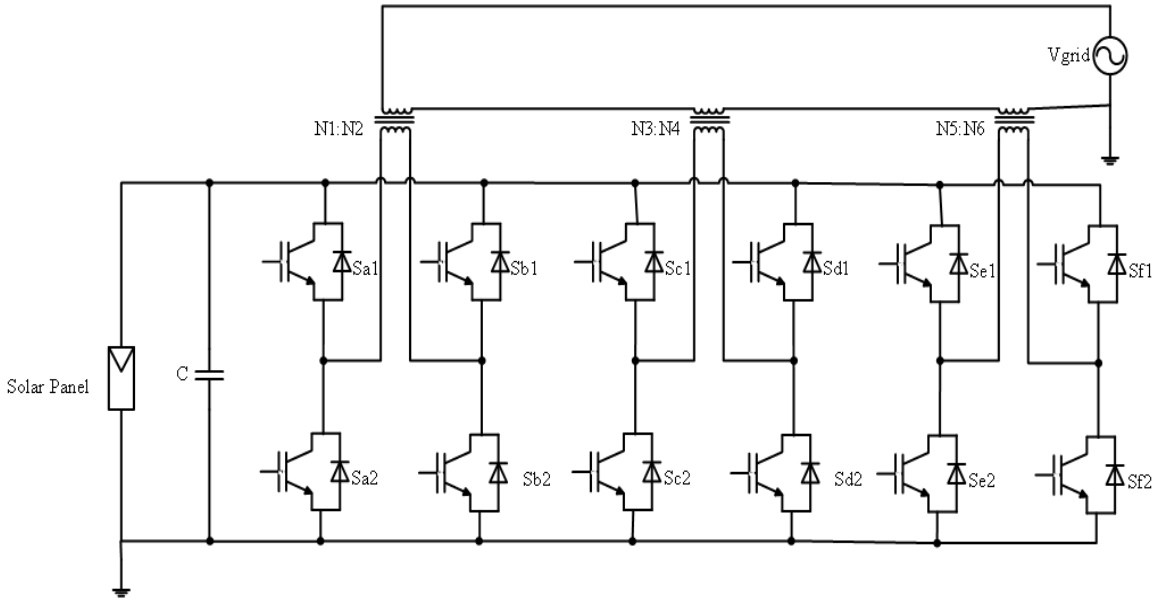


FIGURE 2.14: Circuit schematic of grid tied photovoltaic system with magnetic coupled inverter [18].

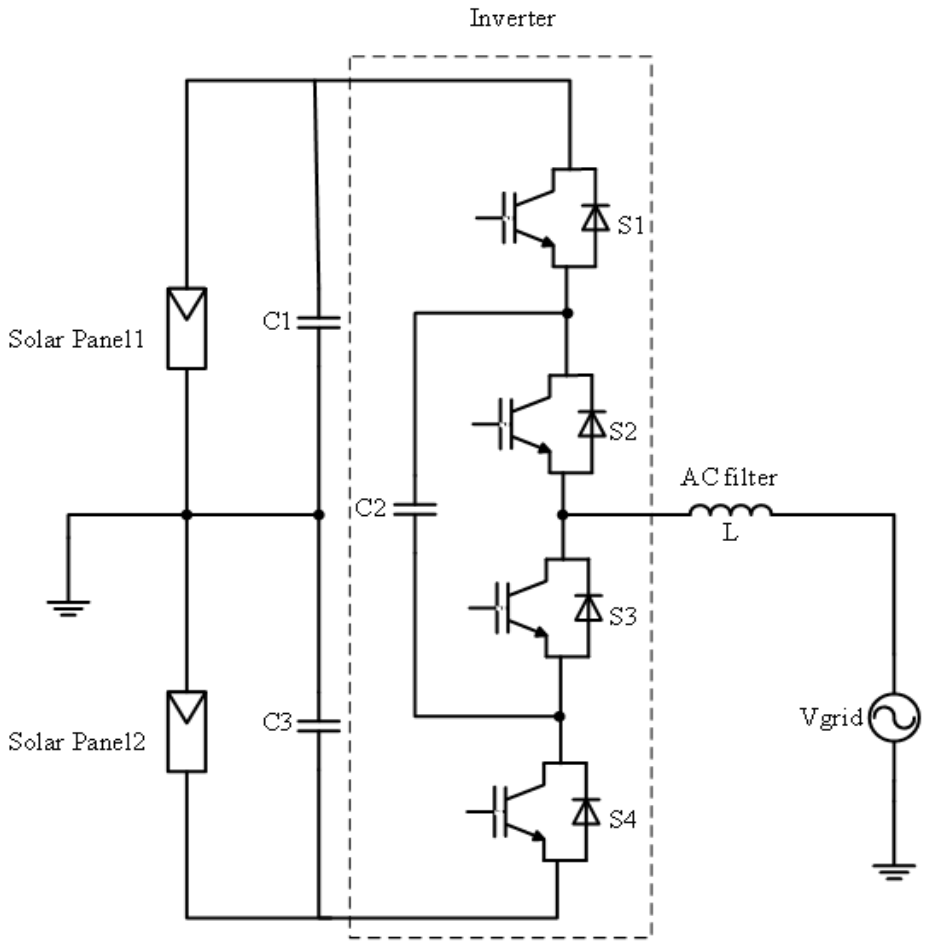


FIGURE 2.15: Circuit schematic of grid connected photovoltaic system with half – bridge [18].

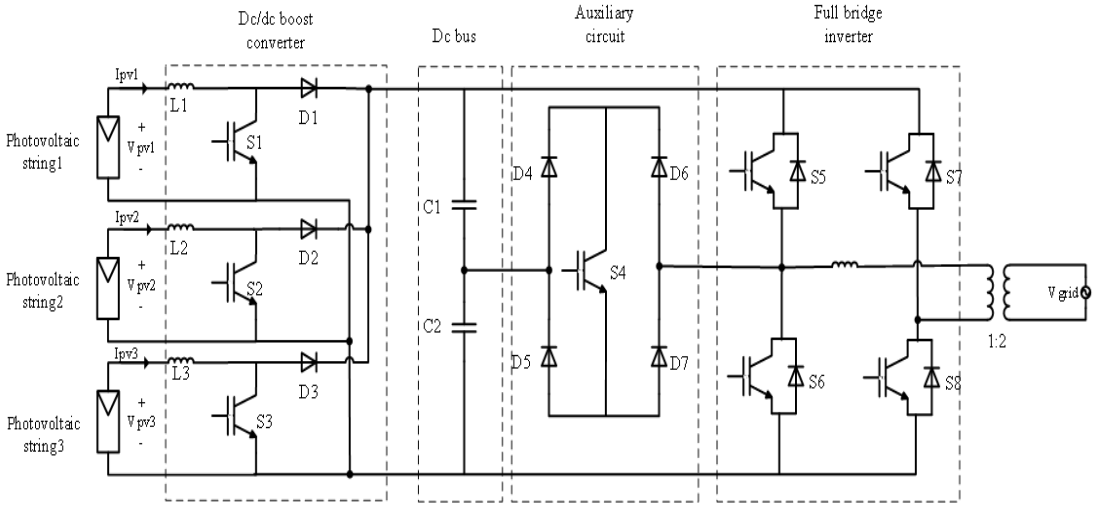


FIGURE 2.16: Schematic of multistring five – level inverter circuit [19].

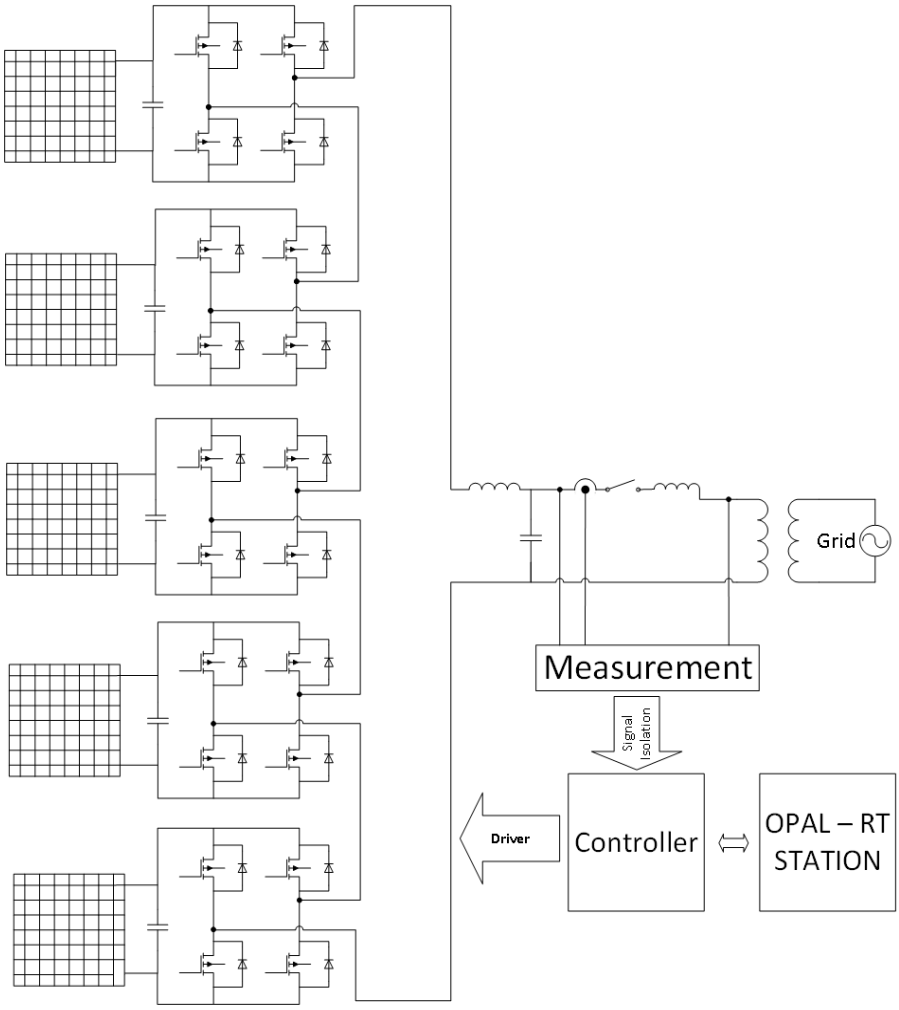


FIGURE 2.17: Simplified schematic of grid connected eleven – level photovoltaic inverter [20].

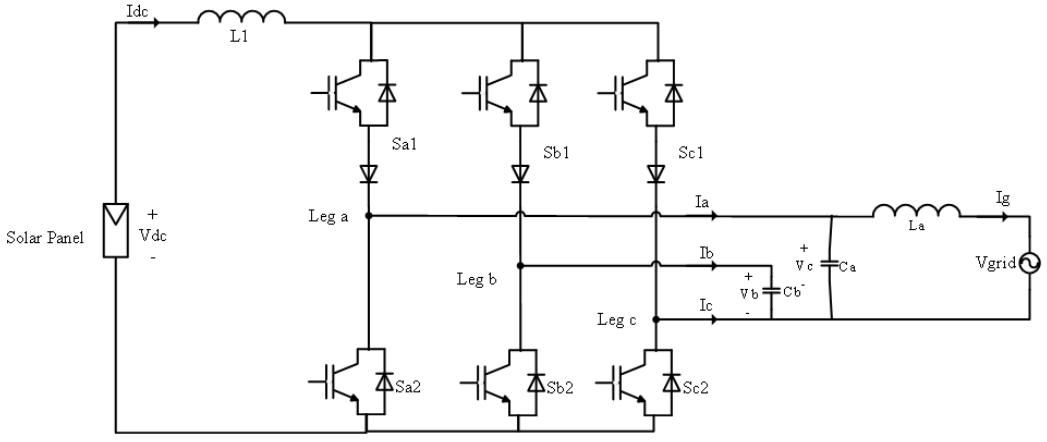


FIGURE 2.18: Simplified schematic of a single – phase current source inverter which mitigates low frequency current ripples [22].

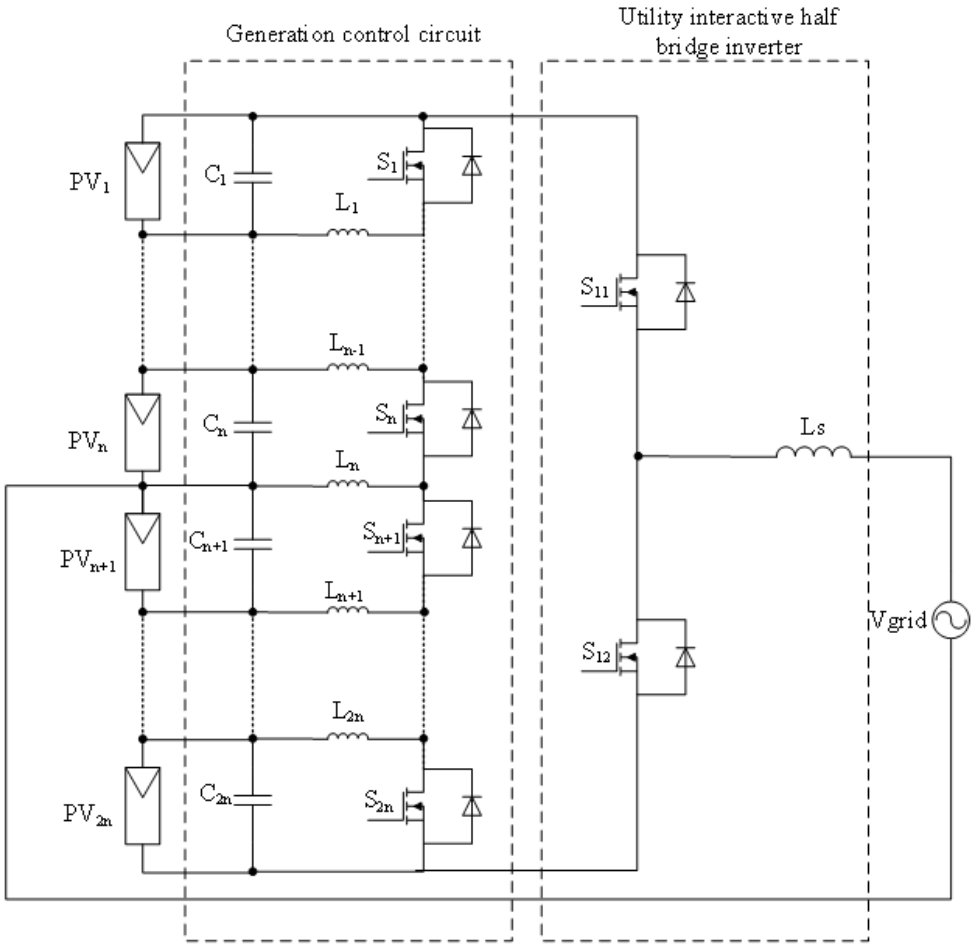


FIGURE 2.19: Simplified circuit schematic of half – bridge inverter with generation control circuit [24].

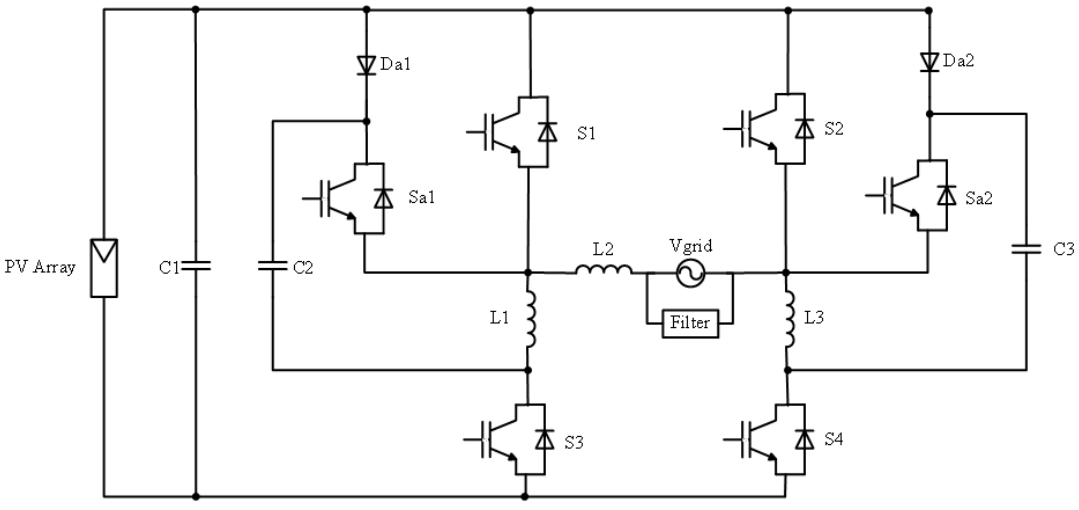


FIGURE 2.20: Simplified schematic of zero current switch inverter [25].

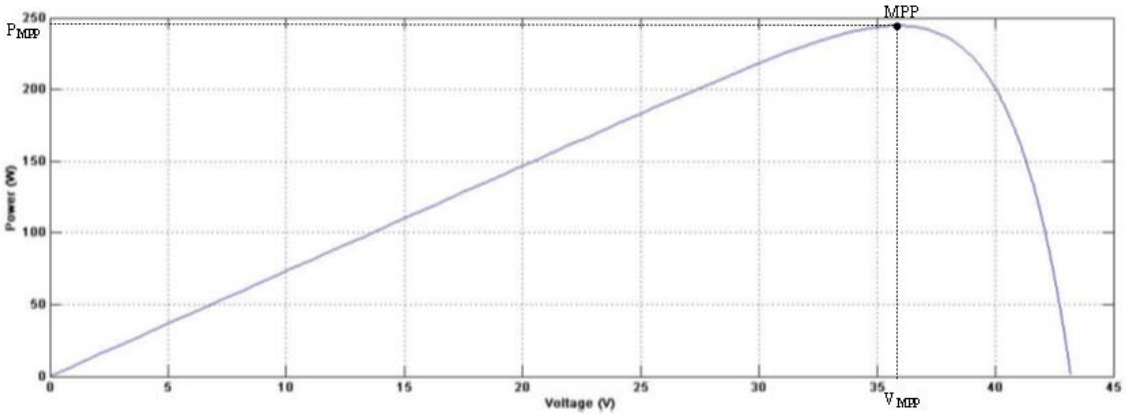


FIGURE 2.21: Typical P – V characteristics of a solar panel showing maximum power point (MPP) [14].

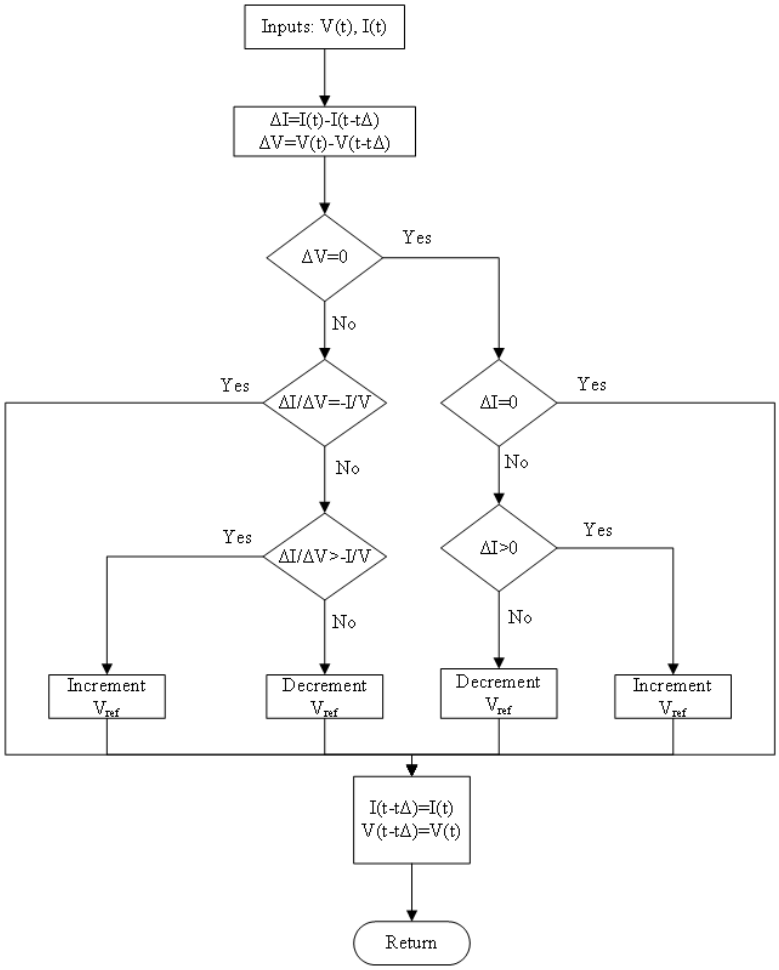


FIGURE 2.22: Flowchart for incremental conductance maximum power point tracking [14].

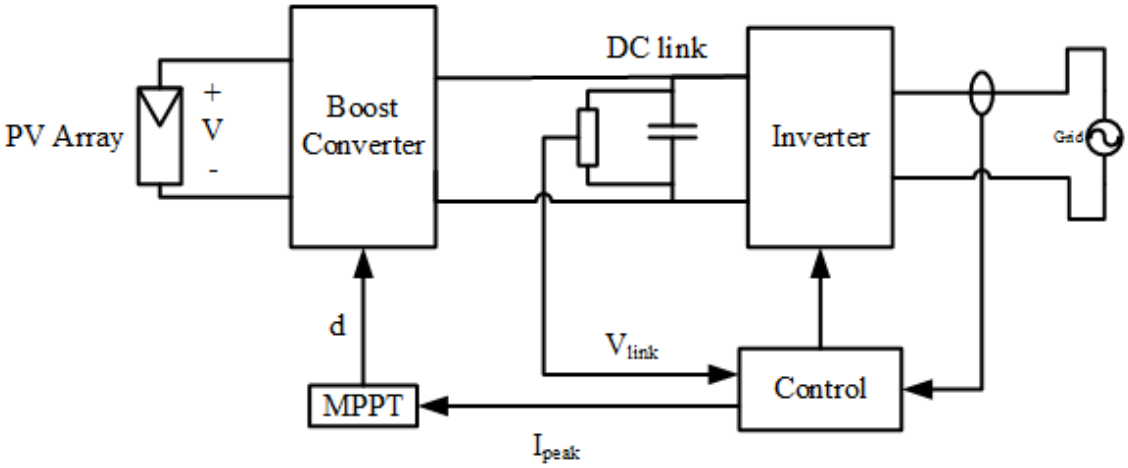


FIGURE 2.23: Topology for dc – link capacitor droop control [14].

CHAPTER 3 : SOLAR PANEL COMPANION INVERTER

3.1. Introduction

In this chapter, topology and circuit schematic of the proposed Solar Panel Companion Inverter (SPCI) is presented. In Section 3.2, a methodology to synthesize an output ac voltage is described. Detailed circuit schematic of SPCI and its operation is described in the Section 3.3.

3.2. Solar Panel Companion Inverter Topology

SPCI is topologically identical to cascaded H – bridge multilevel inverter [20]. However, it is fundamentally different in the way it is being implemented. Driven by aggressive cost targets of 10 cents/W, each H – bridge inverter module is reduced to four power electronics devices, preferably Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), one mechanical bypass switch, one dc link capacitor, one microcontroller and a parasitic power supply harvesting energy from the solar panel itself. This inverter module is integrated with the solar panel (hence the name Solar Panel Companion Inverter), and depending on the dc voltage of the panel, a quasi – square wave of required duration is synthesized. To realize a required ac voltage, a number of such panels are connected in series through their companion inverters. The schematic to synthesize a 120V ac rms voltage is shown in Figure 3.1, wherein six panels, each capable of producing a dc voltage of about 35V are connected in series through their corresponding companion inverters and are interfaced with the distribution grid via an isolation transformer.

The magnitude of the output ac waveform, mag(V_o), to be synthesized by the Photo Voltaic (PV) generation system is a function of the distribution grid voltage and the voltage drop across the interfacing transformer. Typically, magnitudes of ac voltages on both sides of the transformer are synchronized such that only real power is supplied from the panels to the grid. However, it is also possible to add a component for reactive power required to support the grid in the process of determining mag(V_o). The phase of the output ac waveform, ph(V_o), is synchronized with the grid and governed by the available maximum power in the PV generation system. Once such reference output ac voltage V_o is determined from the mag(V_o) and ph(V_o), the SPCI controller constructs the required waveform from multiple panel level quasi – square voltages. Towards this, maximum power point of operation (both voltage and current) for ambient irradiance and temperature is calculated for each panel. A reference output ac current is determined from the available maximum power and reference V_o. The reference current is multiplied with the impedance of the interfacing transformer, to obtain the voltage drop across it. Phasor sum of voltage drop across the transformer and the grid voltage is done to obtain the reference voltage. Furthermore, based on individual panel dc voltages, all H – bridge inverter outputs are sorted and sequenced in real – time such that overall ac output voltage follows the required reference V_o.

3.3. Operation of Solar Panel Companion Inverter

Detailed circuit schematic of Solar Panel Companion Inverter (SPCI) is shown in Figure 3.2. The schematic consists of an SPCI connected to a 120V ac rms grid, a Phase Locked Loop (PLL) block which is used as a means to synchronize the output voltage of SPCI with the grid. The grid voltage is measured and fed into the PLL to construct the

image of grid voltage, $V_{gridpll}$. As discussed in Section 3.2, six panels are connected in series through their individual H – bridges. Each H – bridge consists of four MOSFETs, which are closed/opened by means of the triggering pulses given to their gate terminals. G_{11}, G_{12}, G_{13}, and $G_{14,}$ through G_{61}, G_{62}, G_{63}, and G_{64} are the gate signals applied to the MOSFETs in H – bridges connected to Solar Panel1 through Solar Panel6. The master controller controls the pulse generation to close/open the MOSFETs and it is programmed to generate pulses for triggering the MOSFETs. Timing and width of the pulses is determined by the controller, based on input parameters. The input signals to the master controller V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, and V_{dc6} are the dc voltages measured across Solar Panel1, Solar Panel2, Solar Panel3, Solar Panel4, Solar Panel5, and Solar Panel6 respectively. $V_{gridpll}$, and reference current, I_{ref}, are the two other input signals to the master controller. These eight input signals of the controller are processed in real time and pulses are generated. Its outputs are gate pulses, G_{11} through G_{64}. I_{ref} is the parameter which determines operation of the system at maximum power point. The value of I_{ref} which determines the maximum power point operation varies with the operating scenarios of the SPCI system. The various operating scenarios and the terms associated with the operating scenarios are explained in Chapter 6.

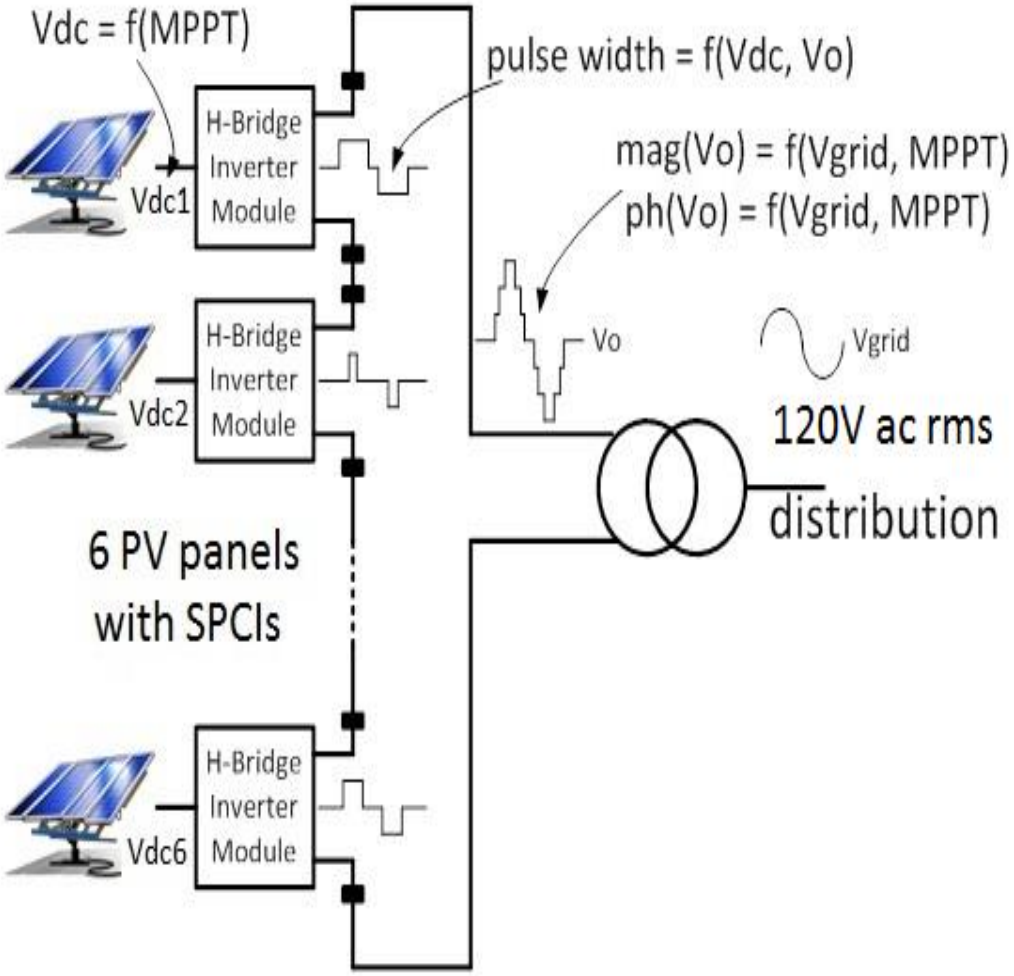


FIGURE 3.1: Simplified schematic of solar panel companion inverter.

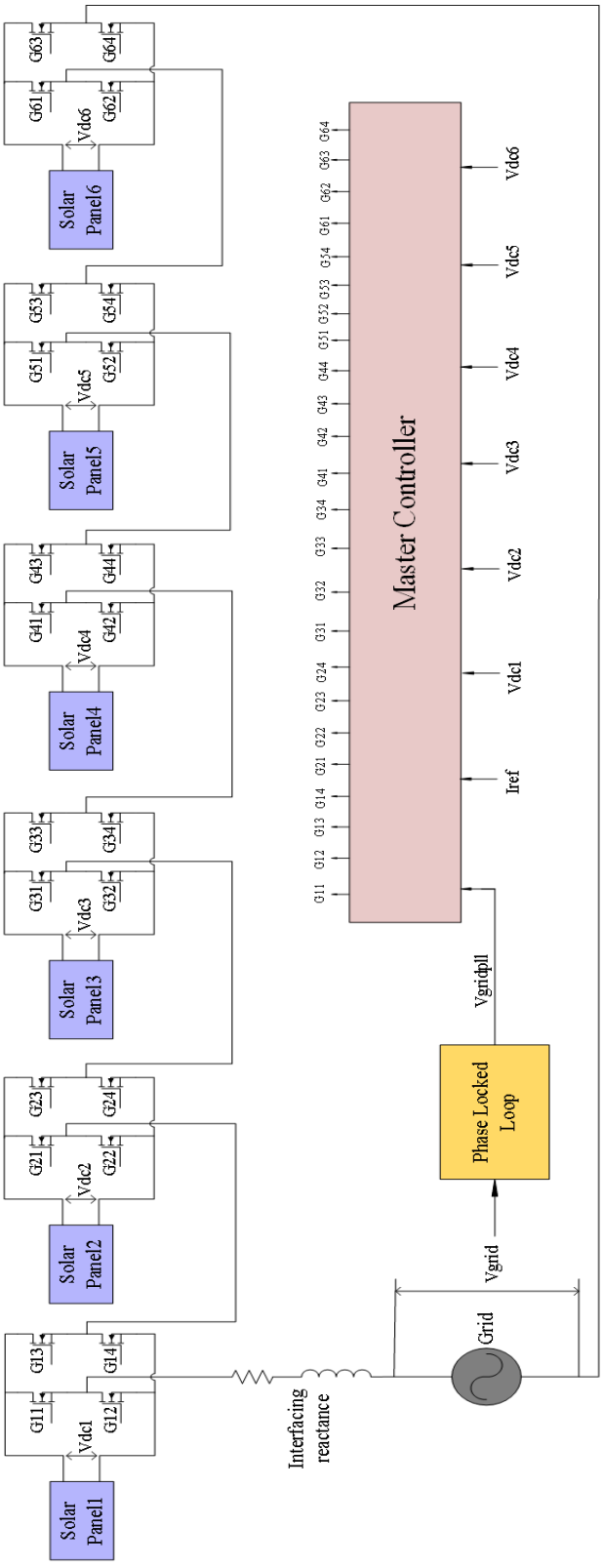


FIGURE 3.2: Detailed circuit schematic of grid tied solar panel companion inverter model capable of synthesizing 120V ac rms voltage.

CHAPTER 4 : CONTROL STRATEGIES FOR SOLAR PANEL COMPANION INVERTER

4.1. Introduction

In this chapter, detailed descriptions of various control strategies namely: Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM) are explained in Sections 4.2, 4.3 and 4.4 respectively. These control strategies are studied in order to make a comparative evaluation of yields derived from the solar panels under various operating conditions, which are discussed in Chapter 7.

4.2. Unsorted Pulse Width Modulation

In Unsorted Pulse Width Modulation (UPWM), a comparison is made between sinusoidal reference wave and a high frequency (6 kHz) triangular wave, also called carrier wave, and a pulse width modulated alternating voltage is produced. The amplitude of the triangular wave is set to the sum of voltages across all the solar panels. Synthesized unsorted pulse width modulated output ac voltage with its sinusoidal reference is shown in Figure 4.1. UPWM is implemented to make a comparative analysis of yields for the Solar Panel Companion Inverter (SPCI) and central inverter topologies. The UPWM which is implemented for central inverter topology can also be identically implemented for SPCI (described in Section 5.8 of Chapter 5), wherein each H – bridge module is provided with the corresponding UPWM signals. Since all the H – bridges are connected in series, at any switching instance, pulse width modulated output voltage similar to the one shown in

Figure 4.1 can be synthesized with SPCI. Comparison of sinusoidal reference wave with high frequency triangular wave, and the output voltage across each H – bridge in SPCI is shown in Figure 4.2.

4.3. Sorted Stair Case Modulation

To synthesize an ac wave as shown in Figure 4.3, Sorted Stair Case Modulation (SSCM) is implemented for Solar Panel Companion Inverter (SPCI) topology. In this strategy, the dc voltages of all the panels are measured and are sorted in descending order. Then the inverter connected to the panel with largest dc voltage is selected to synthesize the first quasi – square wave of the output staircase waveform. Because the width of the step of this bottom quasi – square wave is longest of all, this action results in drawing maximum current from this particular panel, thereby consequently decreasing the voltage on the I – V curve of the solar panel. The inverter connected to the panel with the second largest voltage is selected to synthesize the next step on the output waveform and this sequence is repeated for all the available inverters. The width of each step is a function of the switching instance in the resulting quasi – square wave. This switching time instance is determined to be that moment of time when the reference voltage is more than the sum of all previous steps plus half of existing step. Such logic results in a symmetrical staircase waveform around any sinusoidal reference. Switching instances for all the steps is shown by a dot on the sine wave, in Figure 4.4.

4.4. Sorted Pulse Width Modulation

To synthesize an ac wave as shown in Figure 4.5, Sorted Pulse Width Modulation (SPWM) is implemented for (Solar Panel Companion Inverter) SPCI topology. SPWM is a combination of both SSCM and UPWM strategies. Similar to SSCM, in SPWM strategy

also the dc voltages of all the panels are measured, sorted in descending order and the one with the largest voltage is selected to synthesize the first pulse width modulated quasi – square wave. In order to synthesize this, a triangular wave having high frequency (6 kHz) and an amplitude equal to the value of the selected dc bus voltage, is compared to the sine wave reference, as shown in Figure 4.6. The inverter connected to the second largest panel is selected to synthesize the second pulse width modulated step. In this case, the carrier frequency is shifted in level by a value equal to magnitude of the first step. The sequence is repeated for all the available inverters and in doing so, the carrier frequency is shifted in level by a value equal to the sum of magnitudes of all the previous steps.

4.5. Summary

Implementing Unsorted Pulse Width Modulation (UPWM) for a Solar Panel Companion Inverter (SPCI) generates an unsorted pulse width modulated sinusoidal output voltage. Sorted Stair Case Modulation (SSCM) is based on sorting the dc voltages of all panels to generate voltage levels at fundamental frequency (60Hz). When SSCM is implemented for SPCI, it generates a sorted staircase output voltage. Sorted Pulse Width Modulation (SPWM) is a combination of UPWM and SSCM, when implemented for SPCI, generates a sorted pulse width modulated output waveform. For an operating scenario, only one of the control strategies yields the best (as will be discussed in Chapter 7). Since all the three control strategies can be implemented for SPCI, depending on the yield, one control strategy which yields the best is selected.

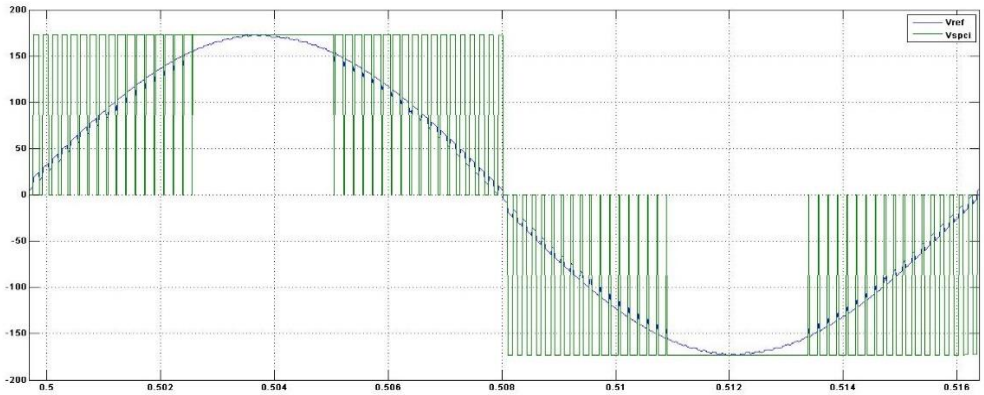


FIGURE 4.1: Unsorted pulse width modulation ac waveform with its sinusoidal ac reference.

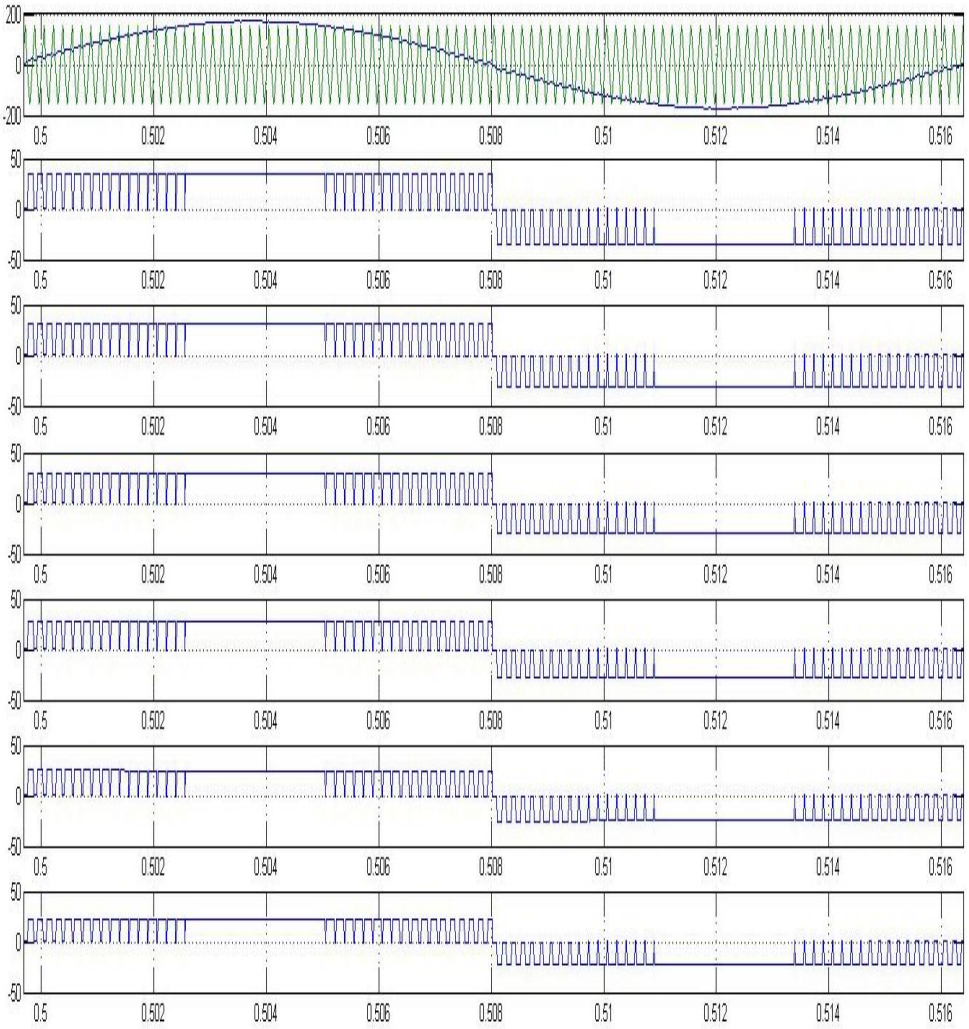


FIGURE 4.2: Unsorted pulse width modulation for a six panel solar panel companion inverter showing synthesis of each step and the corresponding switching instances.

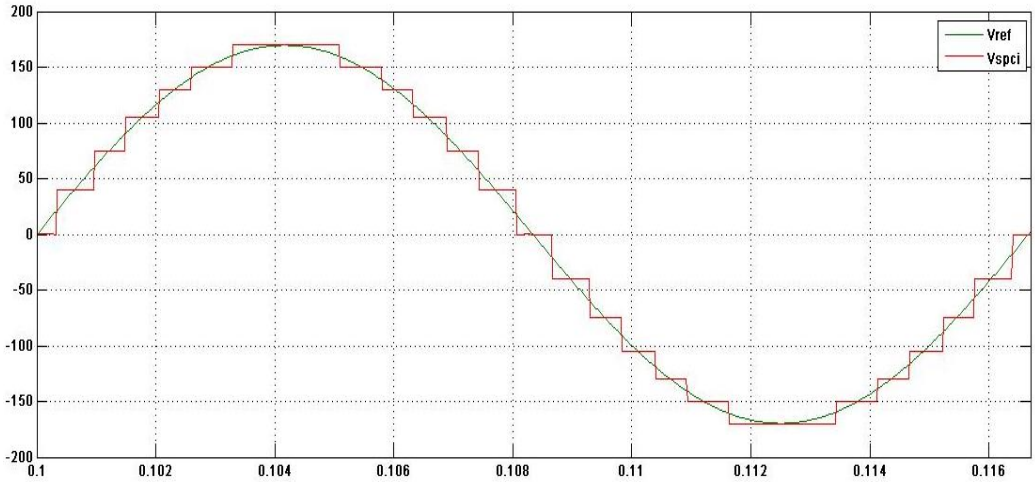


FIGURE 4.3: Sorted stair case modulation ac waveform with its sinusoidal ac reference.

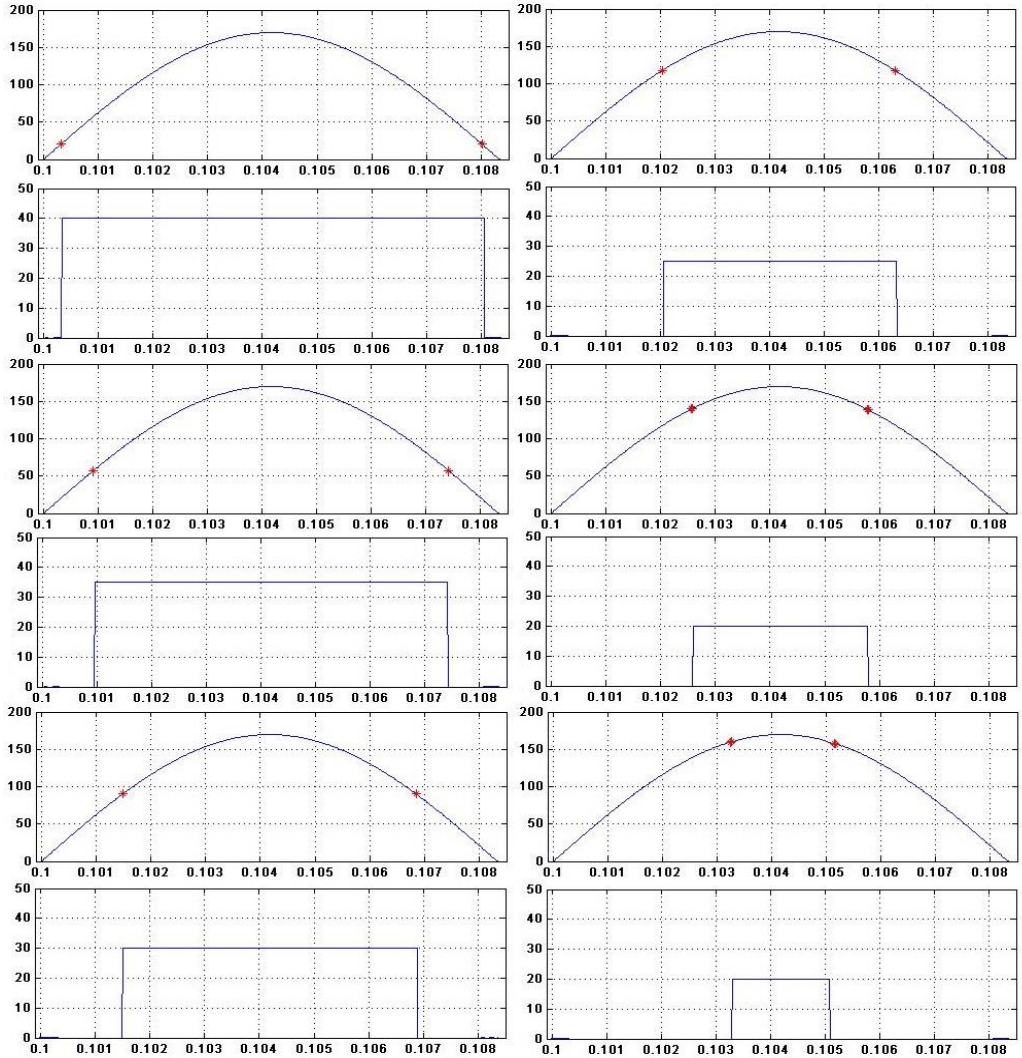


FIGURE 4.4: Sorted stair case modulation for a six panel solar panel companion inverter showing synthesis of each step and the corresponding switching instances.

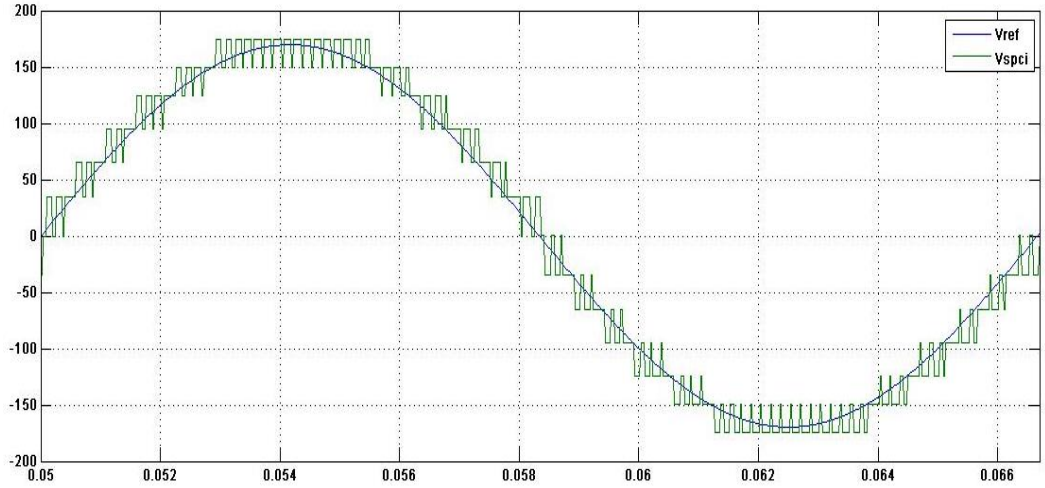


FIGURE 4.5: Sorted pulse width modulation ac waveform with its sinusoidal ac reference.

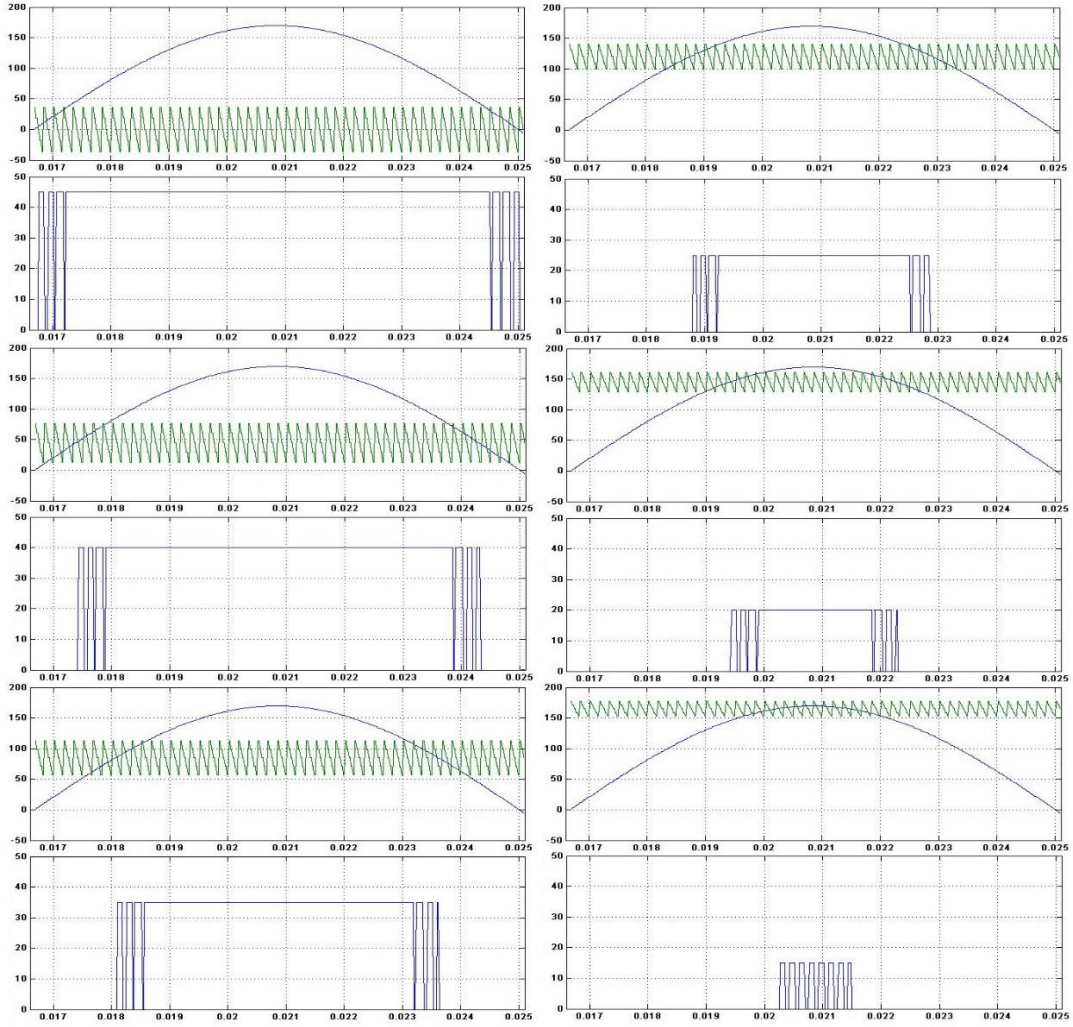


FIGURE 4.6: Sorted pulse width modulation for a six panel solar panel companion inverter showing synthesis of each step and the corresponding switching instances.

CHAPTER 5 : MODELING OF A GRID CONNECTED SOLAR PANEL COMPANION INVERTER

5.1. Introduction

This chapter presents the model of a grid connected Solar Panel Companion Inverter (SPCI). Section 5.2 describes a block diagram of grid connected SPCI. Matlab Simulink model of solar panel, power grid, Phase Locked Loop (PLL), reference voltage construction, and SPCI are explained in Sections 5.3, 5.4, 5.5, 5.6, and 5.7 respectively. Master controllers for Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM) control strategies are described in Sections 5.8, 5.9 and 5.10 respectively.

5.2. Block Diagram of Grid Connected Solar Panel Companion Inverter

A simplified block diagram of grid connected Solar Panel Companion Inverter (SPCI) is shown in Figure 5.1. As discussed in Chapter 3, six solar panels having similar ratings are selected. Each solar panel is connected to an H – bridge and the ac output terminals of all the H – bridges are connected in series to form a two terminal ac output. This two terminal ac output is connected to the grid via an interfacing transformer. Phase Locked Loop (PLL) is used to construct an image of the grid voltage and its phase. Vector addition of the constructed grid voltage and the voltage drop across the interfacing reactance is done to generate a reference voltage. DC bus voltage signals and reference voltage signal are fed as inputs into the controller block. The controller block is programmed to process the input signals and synthesize the desired ac output voltage.

5.3. Model of Solar Panel

Figure 5.2 shows solar cell block available in SimElectronics library which is used as a fundamental building block to construct the solar panel module in Matlab Simulink. It consists of three terminals. The arrow headed terminal is used as a means to set the desired solar irradiance, and dc output power can be tapped from other two terminals. Each cell is configured to their default values, with an open circuit voltage of 0.6V and a short circuit current of 7.34A at an irradiance of 1000W/m^2, which is the irradiance under Standard Testing Conditions (STC) [26]. A variable load is connected across the output terminals, I – V and P – V characteristics for single cell are obtained as may be seen in Figure 5.3. The open circuit voltage from the output characteristics is found to be V_{oc} = 0.6V, short circuit current is I_{sc} = 7.34A, voltage at maximum power point is V_{mpp} = 0.498V, current at maximum power point, I_{mpp} = 6.813A, and maximum power, P_{mpp} = 3.396W. Towards constructing the model a solar panel which gives a dc voltage of 36V, a six cell subsystem as seen in Figure 5.4 is created by connecting six configured solar cells. PSA-280 [7] from Solar Fennel Corp. is used as reference to constrcut the Simulink model. Twelve such subsystems are then connected in series to form a complete solar panel, that gives current and voltage in physical domain. As shown in Figure 5.5, the modelled photovoltaic module is connected to a variable resistance in physical domain, and associated current flowing through it is measured. This measured current is converted to SimPowerSystems and is used to operate a controlled current source in the power domain. The voltage across this current source is measured and impedance is calculated, which is then fed back to the variable resistance in the physical domain. Thus a realistic photovoltaic panel is modelled in Simulink and the performance of the model is confirmed by plotting I – V characteristics

and comparing it with real panel parameters as shown in Figure 5.6. Six such photovoltaic panel models are used in the overall grid connected Solar Panel Companion Inverter (SPCI) Simulink model.

5.4. Model of Power Grid

Power grid is modelled in Matlab Simulink as an ideal ac voltage source, with a series impedance. The ac voltage is set to 120Vac rms and the frequency is set to 60Hz. Interfacing impedance consists of resistive and inductive components (modelled for the resistance and leakage reactance of the interfacing transformer), as shown in Figure 5.7. The source impedance and the interfacing impedance is calculated as follows.

Dc output power that can be produced by each panel, P_{dc} = 244.53W (5.1)

Total dc output power that can be produced by six panels,

P_{total} = 244.53*6 = 1467.18W (5.2)

RMS Grid ac voltage, V_{grid} = 120V (5.3)

Base impedance, $Z_{base} = \frac{V^2}{P} = \frac{120^2}{1467.18} \approx 10\Omega$ (5.4)

Inductance equivalent to 10Ω, $L_{base} = \frac{Z_{base}}{2*\pi*60} = \frac{10}{120*\pi} = 0.026\,\mathrm{H}$ (5.5)

2% of base inductance is chosen as the source inductance. Therefore, source inductance is chosen to be 0.02*0.026, which is 0.5mH.

0.1% of base impedance is chosen as the source resistance. Therefore, source resistance is 10mΩ.

35% of base inductance is selected as interfacing inductance (modelled for leakage reactance of the interfacing transformer), which is approximately 9mH.

1% of base impedance is selected as interfacing resistance (modelled for resistance of the interfacing transformer), which is 100mΩ.

5.5. Model of Phase Locked Loop

Construction of the image of grid voltage waveform, both magnitude and phase is done using Phase Locked Loop (PLL). Figure 5.8 shows the block diagram of the process involved in realization of grid voltage using PLL. The grid voltage say Asin (ωt + θ) is measured and fed into the PLL block. Magnitude 'A', of the grid voltage waveform, and grid voltage waveform having unit amplitude is obtained from the box. Figure 5.9 shows the block diagram of PLL modelled in Simulink. The input to the PLL subsystem is measured grid voltage, 'Vgrid'. The two output signals are 'Vgridpll', which is grid voltage waveform, and 'Ugrid', which is grid voltage waveform having unit amplitude. As maybe seen in Figure 5.10, the grid voltage waveform obtained from PLL is in synshronism with the grid voltage after eight complete cycles. This confirms the working of the PLL block modelled in Matlab Simulink.

5.6. Reference Voltage Generation

The output from Solar Panel Companion Inverter (SPCI) is an alternating sinusoidal voltage. So, SPCI is considered as an ac voltage source, connected to the grid via an interfacing reactance, 'X_L' as shown in Figure 5.11. To transfer power from SPCI to grid, the output ac voltage to be synthesized should be equal to the phasor sum of grid voltage, $V_{grid,}$ and the voltage drop across the interfacing reactance, V_x. To synthesize an ac output voltage, V_{spci}, the reference voltage required is given by the Equation 5.1.

$$\overrightarrow{V_{ref}} = \overrightarrow{V_{grid}} + \overrightarrow{V_X} \tag{5.6}$$

If X_L is the interfacing reactance and I_{grid} is the grid current, then the voltage drop across the interfacing reactance is given by:

$$\overrightarrow{V_X} = \overrightarrow{I_{grid}} * jX_L \quad (5.7)$$

From Equations 5.6 and 5.7, the reference voltage is written as:

$$\overrightarrow{V_{ref}} = \overrightarrow{V_{grid}} + \overrightarrow{I_{grid}} * jX_L \quad (5.8)$$

Since, $X_L = 2*\pi*f*L$ where f is fundamental frequency of grid voltage = 60Hz, L is the inductance of the interfacing reactance = 9e-3H. (5.9)

$$\overrightarrow{V_{ref}} = \overrightarrow{V_{grid}} + \overrightarrow{I_{grid}} * j(2*\pi*f*L) \quad (5.10)$$

But, angular frequency, $\omega = 2*\pi*f$ (5.11)

Therefore, reference voltage, $\overrightarrow{V_{ref}} = \overrightarrow{V_{grid}} + \overrightarrow{I_{grid}} * j\omega L$ (5.12)

Figure 5.12 shows the phasor diagram wherein V_{grid} is the reference phasor. I_{grid} is the phasor current 180 degrees out of phase with the grid voltage, when direction of power flow is into the grid. $I_{grid}*X_L$ is the interfacing reactance drop, lagging the grid current phasor by 90 degrees. V_{ref} is the resultant phasor obtained by the phasor addition of V_{grid} and interfacing reactance drop. By varying the magnitude of I_{grid}, the magnitude and phase angle of V_{ref} is varied and hence operating points of all the solar panels is varied. Thus, by controlling magnitude of grid current, the yield point obtained from the connected solar panels can be varied. The Simulink block diagram to generate sinusoidal reference voltage is shown in Figure 5.13. The grid voltage obtained from PLL is used to make the phasor addition. To get the voltage drop across the interfacing reactance, one of the output signals from the PLL subsystem, Ugrid, which is the grid voltage waveform having unit amplitude is taken and delayed in phase by 90 degrees, which is a quarter of a cycle or 1/(4*60) s, is

multiplied by -1 times the reference current magnitude and 2*π*60*9e-3 which gives the voltage drop across the reactance. The voltage drop across the resistance, obtained by multiplying the reference current magnitude with the interfacing resistance which is 100mΩ, is also added to the phasor sum of grid voltage from PLL, and the voltage drop across the reactance. The resultant gives the reference voltage required to generate sinusoidal ac voltage from SPCI. As maybe seen in Figure 5.14, the reference voltage, V_{ref} has a magnitude greater than the magnitude of the grid voltage and it lags in phase with respect to the grid voltage.

5.7. Solar Panel Companion Inverter Model

Simplified circuit schematic of Solar Panel Companion Inverter (SPCI) which can produce a three level output ac voltage is shown in Figure 5.15. SPCI system model is built to be able to produce ac output voltage of 120V ac rms. To be able to reach the peak voltage of 120√2 V, six solar panel models built in simulink are connected to six H – bridges. As may be seen from Figure 5.16, six H-bridge inverters are connected in series to form a two-wire single phase output. Each H-bridge inverter consists of four MOSFETs. Each module derives power from the PV module that is modelled in Simulink. Each MOSFET is closed/opened by the high/low pulse received at the gate terminal. The twenty four MOSFETs in the proposed system are driven by a master controller. The working of the controller varies with the type of control strategy employed for SPCI. These controller models are described in the following sections.

5.8. Master Controller for Unsorted Pulse Width Modulation

Figure 5.17 shows the logic employed for Unsorted Pulse Width Modulation (UPWM). The master controller for UPWM is shown in Figure 5.18. The inputs to this controller are,

sum of dc bus voltages of all the solar panels, a reference ac voltage, and a triangular wave having unit amplitude and a frequency of 6 kHz. Figure 5.19 shows the contents of the subsystem of master controller for UPWM. In order to generate unsorted pulse width modulated signals for driving the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) of the inverter, a unit triangular wave is multiplied with the sum of dc bus voltages of all the solar panels, V_{sum}, and then compared with sinusoidal reference to generate the unsorted pulse width modulated signals. The outputs of the controller are four gate signals that are given to individual (MOSFETs) of a central inverter. This modulation strategy can also be implemented for a Solar Panel Companion Inverter (SPCI), wherein each H – bridge module is provided with the corresponding UPWM signals. Figure 5.20 shows the circuit schematic of central inverter for the instance when S1, and S4 are closed. It also shows the circuit schematic of SPCI for the instance when the switches S11, and S14 through S61, and S64 are closed, and at this instance all the solar panels are connected in series. The output voltage at this instance for both the topologies is the sum of dc bus voltages across all the panels, $V_{dc1} + V_{dc2} + V_{dc3} + V_{dc4} + V_{dc5} + V_{dc6}$. This shows that when UPWM strategy is applied to an SPCI, its output voltage imitates the output voltage of a central inverter.

5.9. Master Controller for Sorted Stair Case Modulation

Figure 5.21 shows the logic employed for Sorted Stair Case Modulation (SSCM). The master controller for SSCM is modelled as a triggered system to reproduce effects of a digital controller. As maybe seen in Figure 5.22, the inputs to this controller are six dc bus voltages of the solar panels, a reference ac voltage and derivative of the reference ac

voltage. The outputs of the controller are twenty four gate signals that are given to individual MOSFETs.

The master controller consists of logic circuits employed to sort the dc bus voltages, generate pulses for individual H – bridges, and identify the panel inverters corresponding to the sorted dc bus voltages. As shown in Figure 5.23, triggered sort is one of the subsystems inside the master controller wherein dc bus voltages of the solar panels are taken as input and are sorted in descending order, whenever the system is triggered. The system is triggered either when the reference voltage is zero or when the slope of the reference voltage is zero i.e., the sorting is done for every quarter cycle of the reference voltage. The outputs of triggered sort subsystem are arrays of sorted dc bus voltages, and the indices corresponding to the dc bus voltages. Sorted dc bus voltages from large to small, say V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6} and the corresponding voltage indices coming out from the triggered sort subsystem is fed into another subsystem named "switching". As seen in Figure 5.24, the switching subsystem takes in reference voltage, slope of reference voltage, arrays of dc bus voltages and the corresponding indices as the input. This subsystem is a triggered subsystem, sampled at a frequency of 30 kHz.

The switching subsystem comprises of switching logic1 through switching logic6, for switching individual H – bridges. The subsystem, switching logic1 takes V_{dc1}, instantaneous reference voltage, instantaneous slope of the reference voltage, and $V_{dc1}/2$ as the input signals. The output signals are the gate pulses SLG11, SLG12, SLG13, SLG14 which are the signals corresponding to the inverter having the largest dc bus voltage. Logic employed for switching individual H – bridges is shown in Figure 5.25. Switching logic2 takes V_{dc2}, (V_{dc1}+$V_{dc2}/2$), instantaneous reference voltage, and instantaneous slope of the

reference voltage as inputs and outputs are gate pulses corresponding to the inverter with second largest dc bus voltage. Similar trend for the input signals is applied for the subsystems switching logic3 through switching logic6. Signal redirecting logic is a subsystem of switching subsystem, for identifying the inverters corresponding to the sorted dc bus voltages. The switching pulses generated from each switching logic subsystem and the indices of the dc bus voltages are multiplexed and sent as inputs into the signal redirecting logic subsystem where the logic to match pulses with the indices is applied. The processed signals are the signals used to drive inverter MOSFETs.

As maybe seen in Figure 5.26 the input signals are de – multiplexed, all gate signals and voltage indices are sent as inputs to subsystems containing signal redirecting logic to each inverter. Each subsystem inside signal redirecting logic has a unique input signal which is a constant. For example, for the first box the unique signal is a constant '1', second box has constant '2' and so on for all the subsystems. Output signals of first subsystem correspond to gate signals of inverter fed with the largest dc bus voltage, output signal of second subsystem correspond to gate signals of inverter fed with the second largest dc bus voltage. The contents of each subsystem of signal redirecting logic is shown in Figure 5.27.

5.10. Master Controller for Sorted Pulse Width Modulation

Figure 5.28 shows the logic employed for Sorted Pulse Width Modulation (SPWM). The master controller for SPWM is modelled as a triggered system to reproduce effects of a digital controller. As maybe seen from Figure 5.29, the inputs to this controller are dc bus voltages of all the solar panels, a reference ac voltage and a triangular wave having unit amplitude with a frequency of 6 kHz. The outputs of the controller are twenty four gate signals that are given to individual MOSFETs. Similar to SSCM master controller, SPWM

controller also consists of logics for sorting the dc bus voltages every quarter cycle, generating pulses for individual H – bridges, and identifying the panel inverters corresponding to the sorted dc bus voltages. Triggered sort subsystem present in SSCM controller is also present in SPWM controller. Sorted dc bus voltages from large to small, say V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6} and the corresponding voltage indices coming out from the triggered sort subsystem is fed into another subsystem named "switching". As maybe seen in Figure 5.30, the switching subsystem takes in reference voltage, triangular wave having unit amplitude at a frequency of 6 kHz, arrays of dc bus voltages and the corresponding indices as the input. The output signals are the gate signals. This subsystem is triggered at a frequency of 30 kHz. This consists of two subsystems, one which generates sinusoidal pulse width modulated signals at different levels and the other which redirects these pulse width modulated signals to the inverters corresponding to the sorted dc bus voltages.

The contents of PWM subsystem maybe seen in Figure 5.31. Reference sinusoidal voltage, array of dc bus voltages, and triangular wave at a frequency of 6 kHz are input signals to the subsystem. Input dc bus voltages are de – multiplexed and are used as inputs to six other subsystems PWM1, PWM2, PWM3, PWM4, PWM5, and PWM6. Output signals are pwm signals, arrays of indicators that indicate whether the reference voltage is in positive half cycle or negative half cycle and an array of indicators indicating whether the dc bus voltages tend to zero or less than zero.

To produce pulse width modulated signals for driving the MOSFETs corresponding to the inverter connected to the solar panel having largest dc bus voltage, input signals taken by PWM1 subsystem are reference voltage, unit triangular wave, largest dc bus voltage,

$V_{dc1,}$ and sum of dc bus voltages greater than V_{dc1} say V_{sum}, which is zero in this case. Unit triangular wave is multiplied with V_{dc1}, added to V_{sum}, and then compared with sinusoidal reference to generate pulse width modulated signals along with indicators for positive half cycle, negative half cycle and negative dc bus voltage indicator as output signals of the subsystem as maybe seen in Figure 5.32. Similarly, to generate pulse width modulated signals for inverter corresponding to second largest dc bus voltage, the inputs to PWM2 subsystem are reference voltage, unit triangular wave, second largest dc bus voltage, V_{dc2}, and sum of dc bus voltages greater than V_{dc2} which is V_{dc1}. The logic applied for generating pulse width modulated signals for PWM2 is same as that of PWM1 subsystem. Input signals having a trend similar to that of PWM1 and PWM2 is applied to the remaining PWM3, PWM4, PWM5, and PWM6 subsystems present in the PWM subsystem, to generate pulse width modulated signals at different levels.

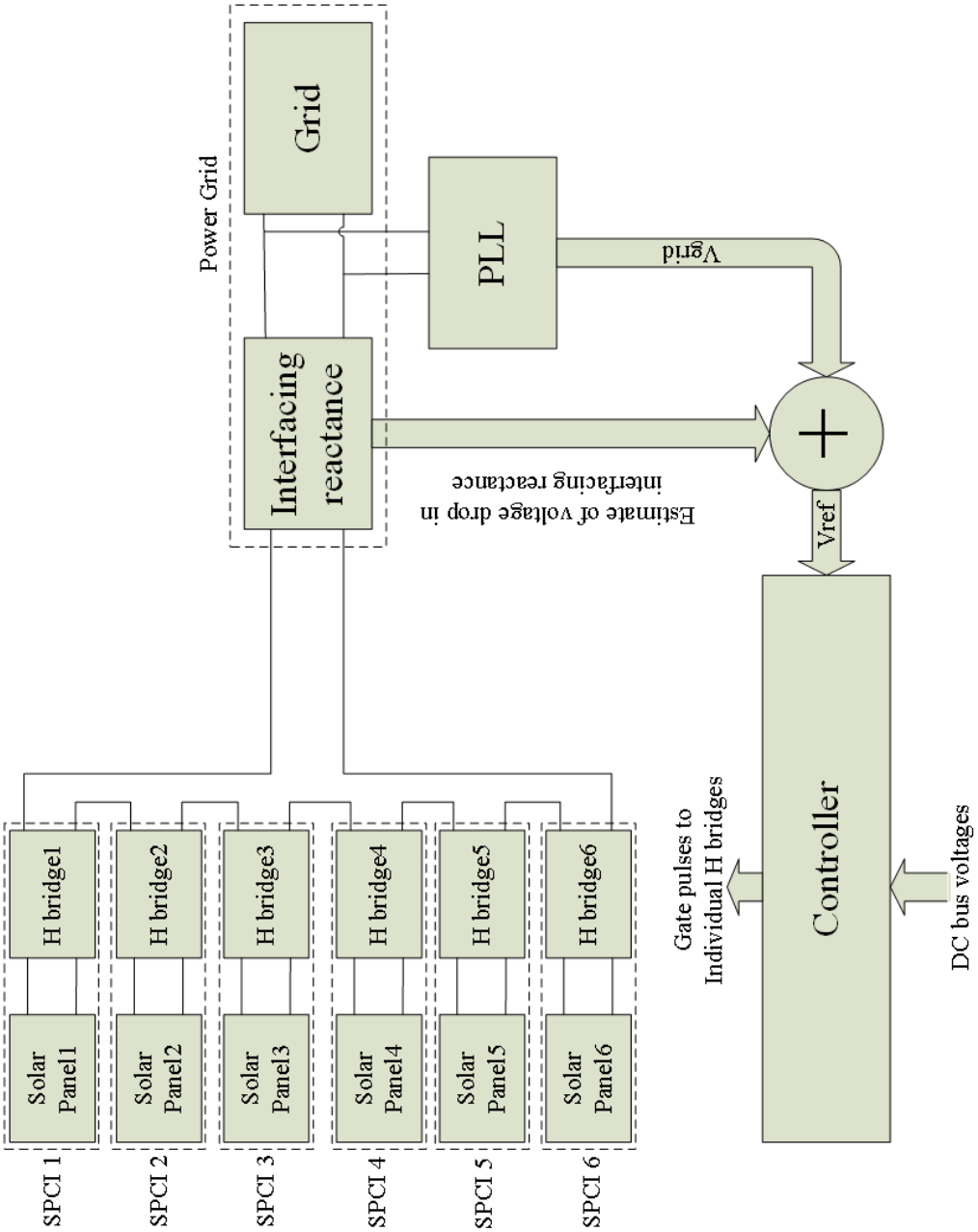


FIGURE 5.1: Simplified block diagram of grid connected solar panel companion inverter.

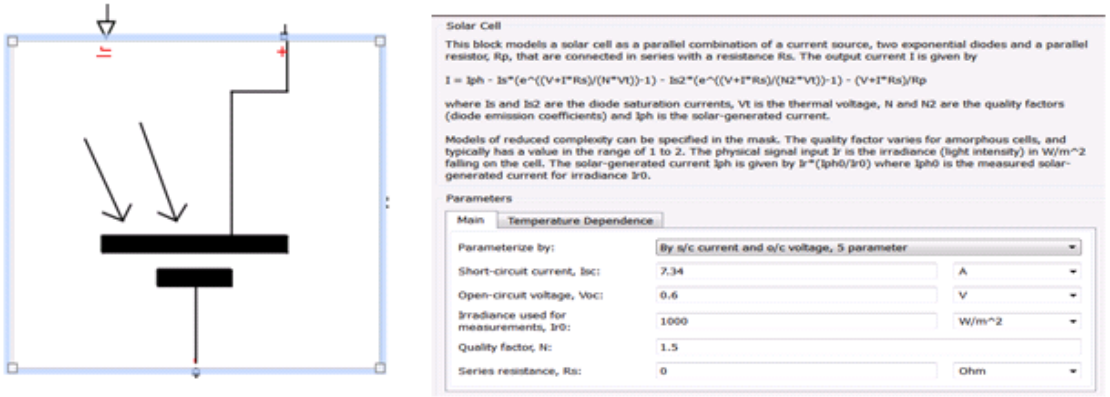


FIGURE 5.2: Simplified schematic of matlab-simulink block of a solar cell available in simelectronics.

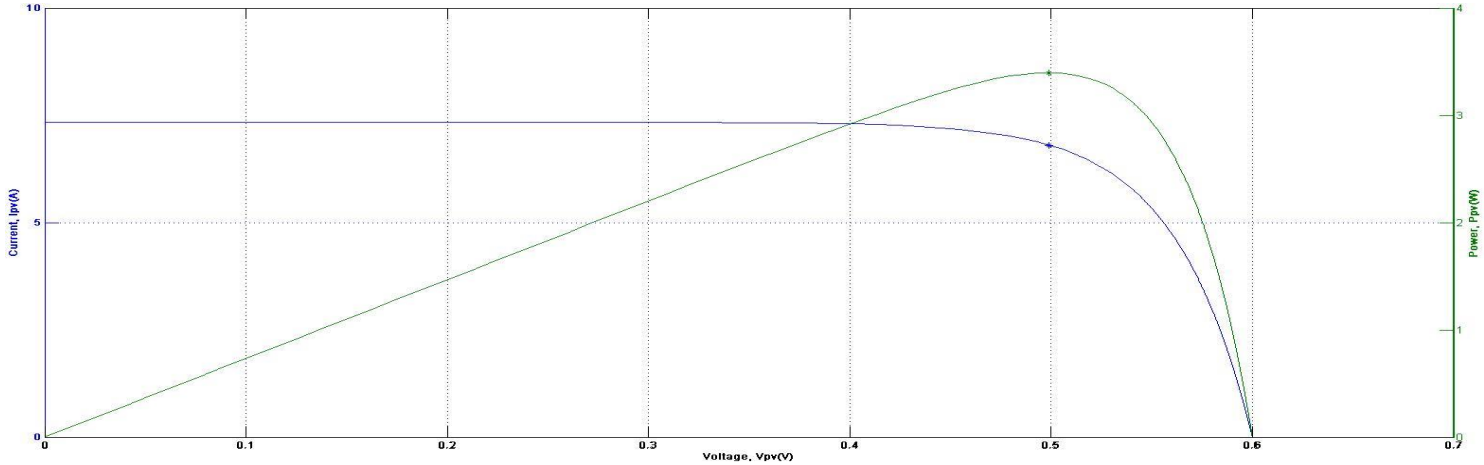


FIGURE 5.3: IV and PV characteristics of the configured solar cell, showing Voc = 0.6V, Isc = 7.34A, Voc = 0.6V,

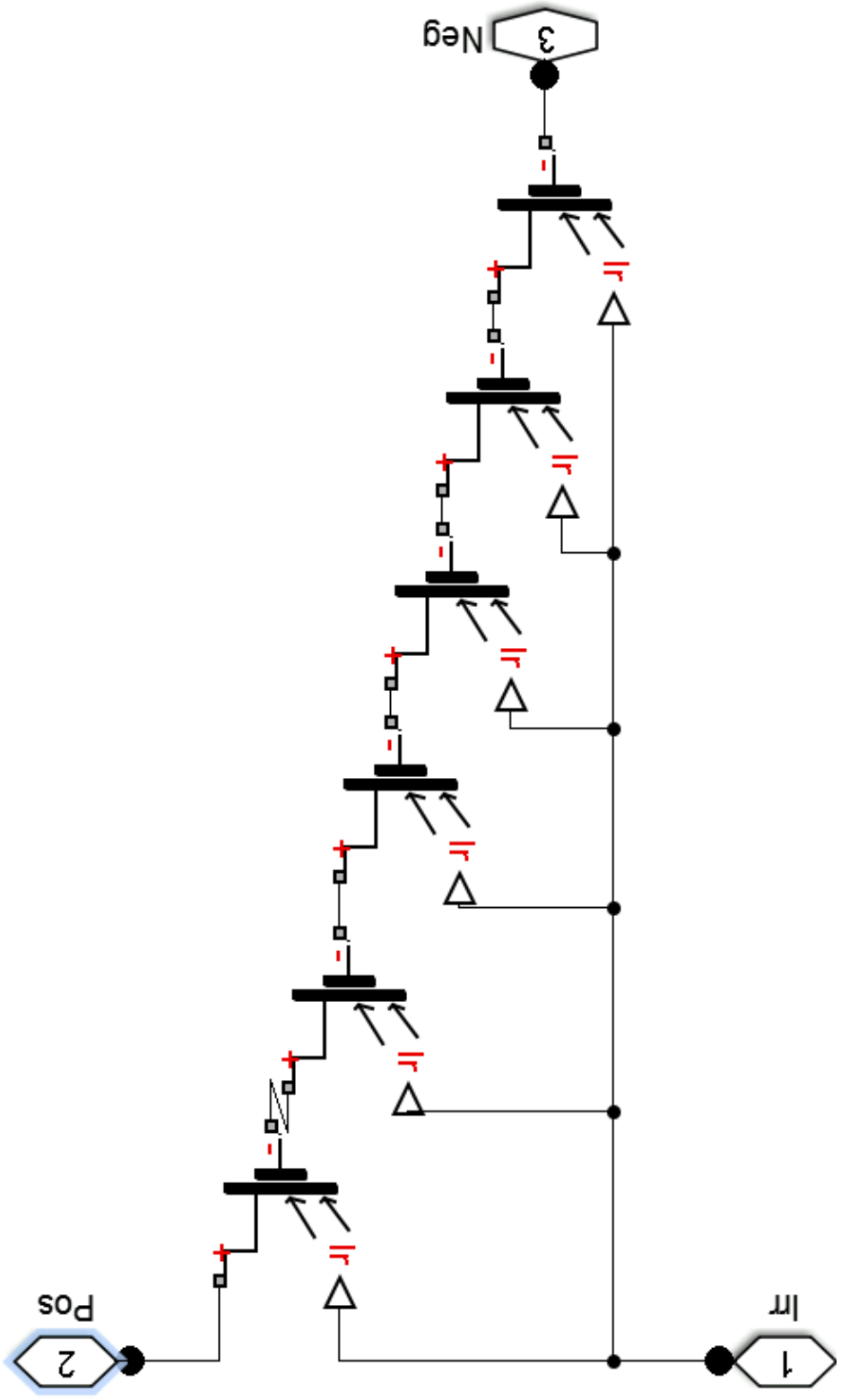


FIGURE 5.4: Circuit schematic showing six solar cells connected in series.

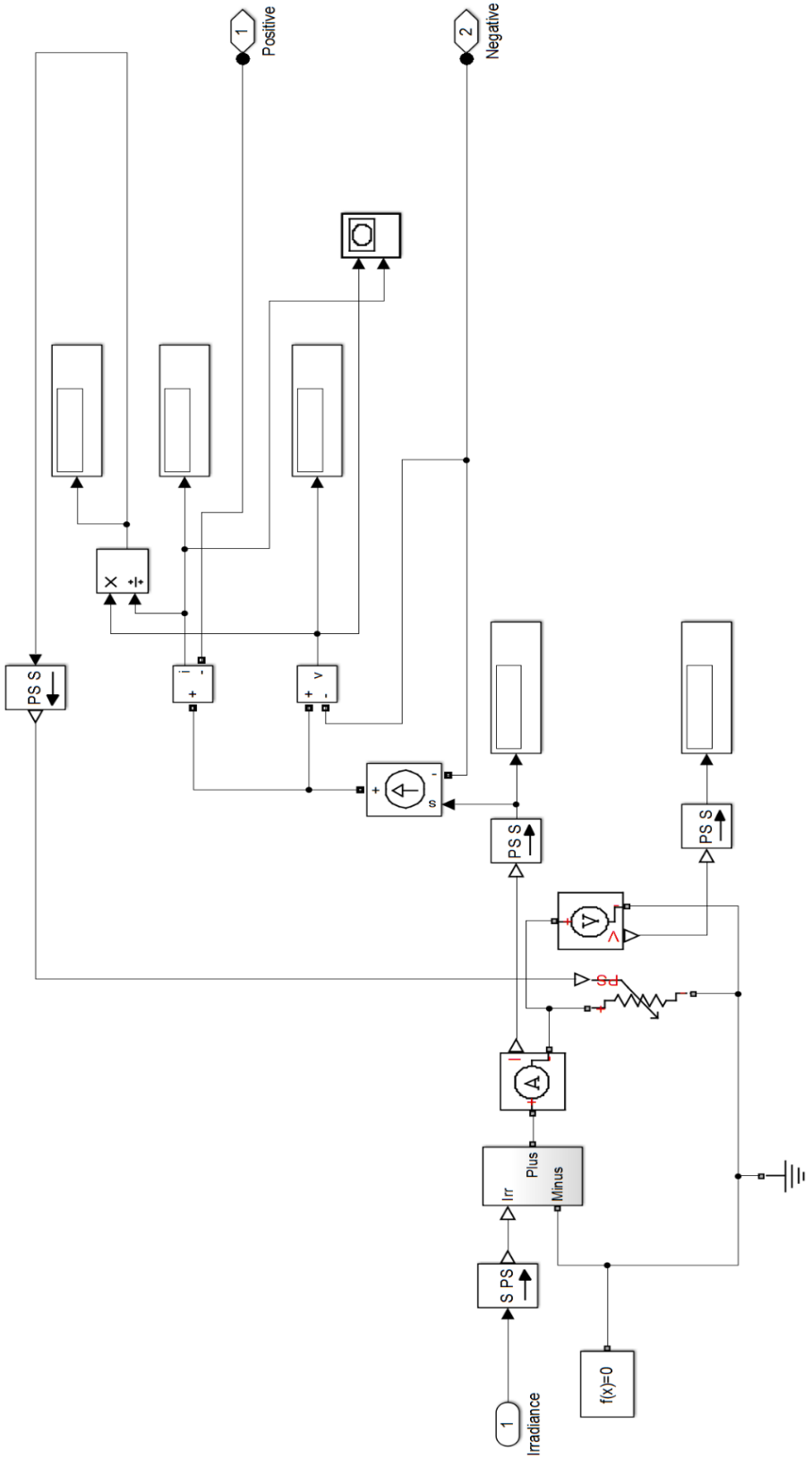


FIGURE 5.5: Simplified circuit schematic of a matlab-simulink model of a photovoltaic panel modeled in simelectronics that is capable of interfacing with a power electronic converter in simpowersystems.

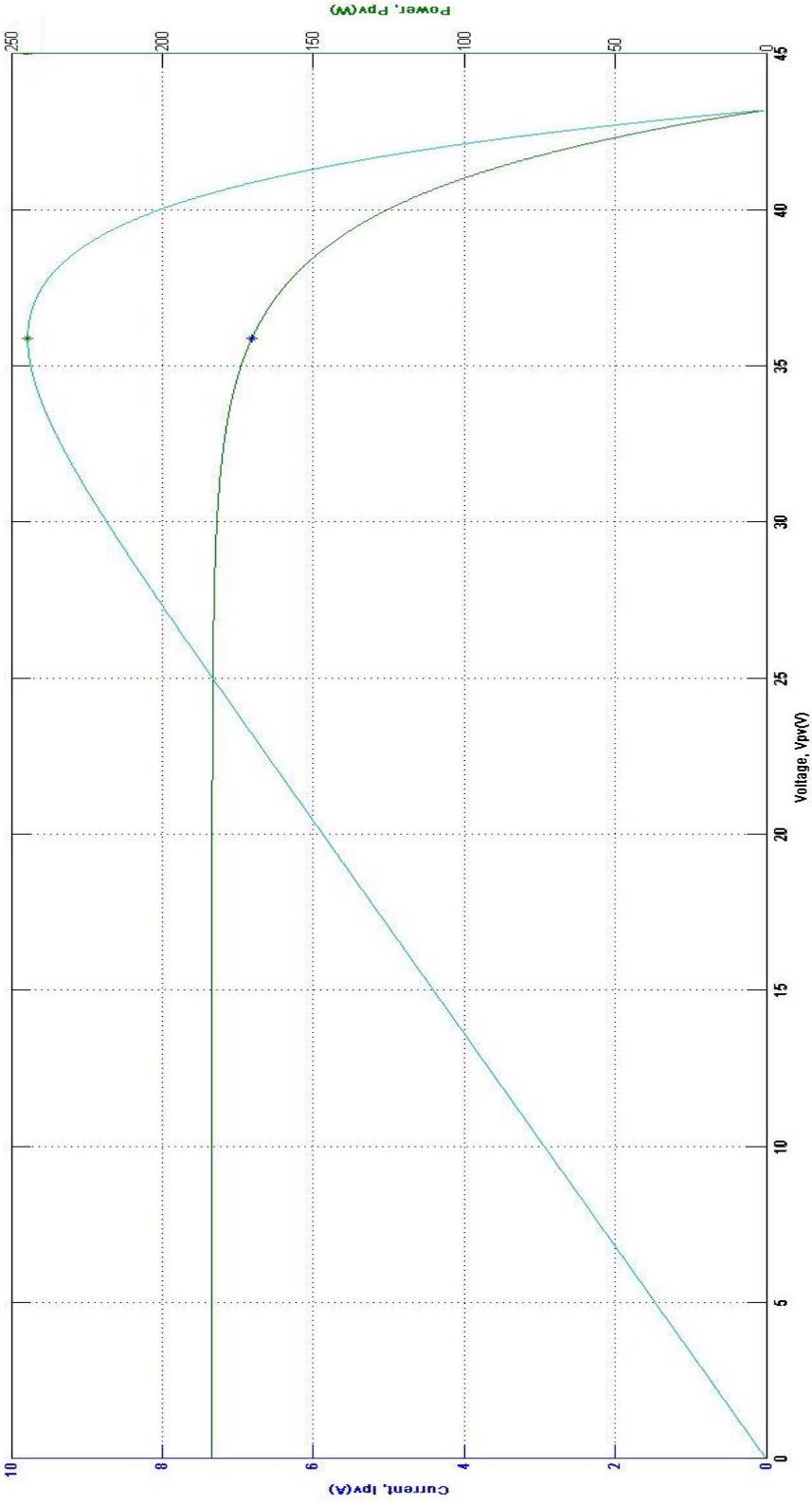


FIGURE 5.6: I-V and P – V characteristics obtained with the solar panel model shown in Figure 5.5, confirming Voc = 43Vdc, Isc = 7.34Adc, Vmpp = 36Vdc, Impp = 6.8Adc and Pmpp = 244.53W.

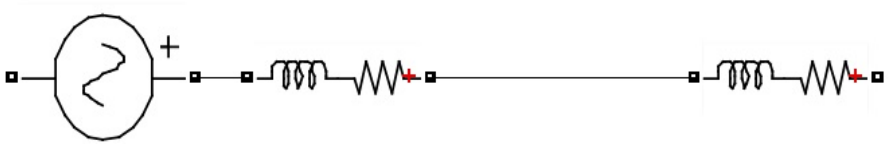


FIGURE 5.7: Simplified circuit schematic showing ac grid modelled as an ideal ac voltage source with a series impedance, connected to an interfacing impedance.

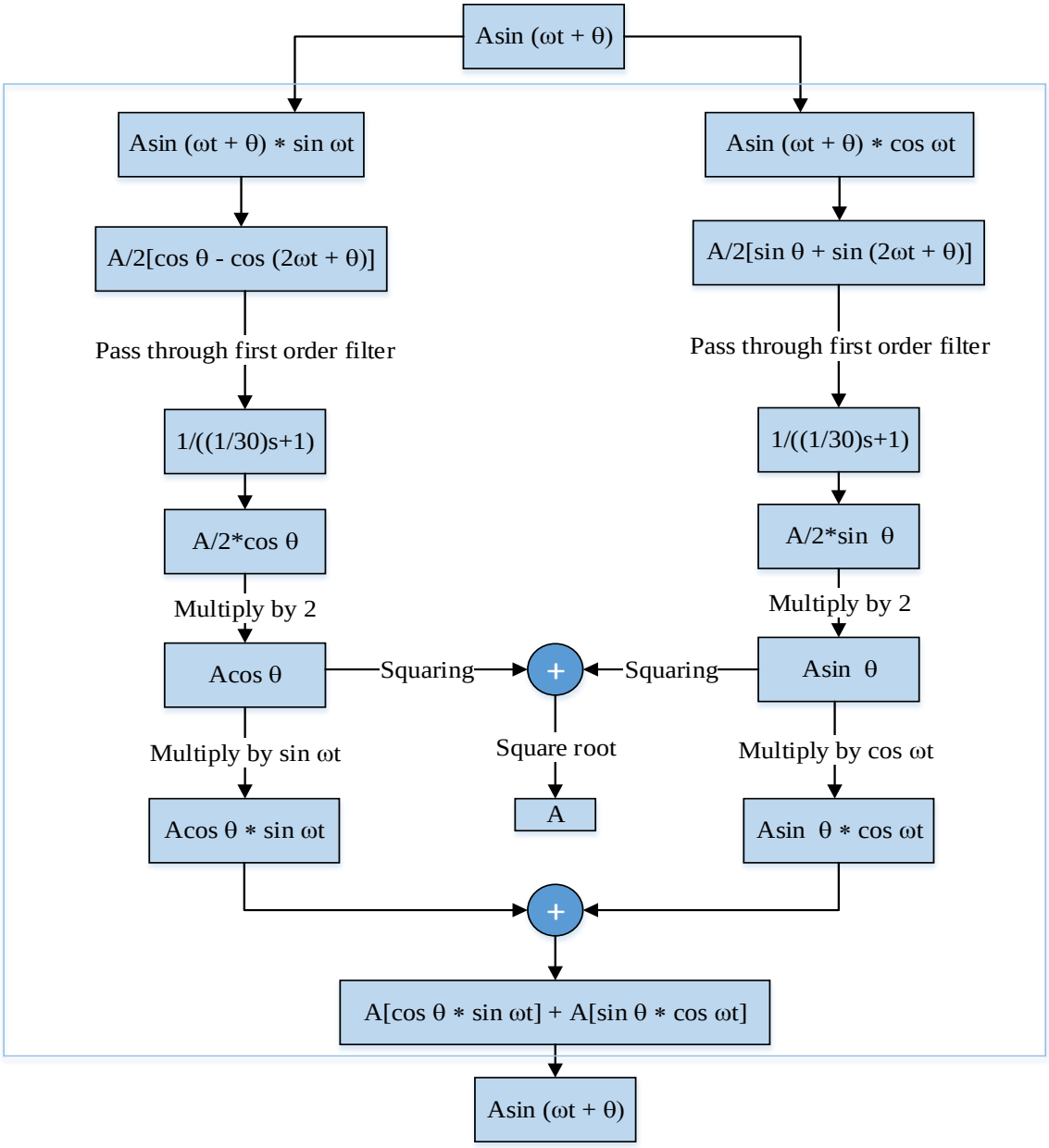


FIGURE 5.8: Simplified block diagram showing the process involved in realization of grid voltage using phase locked loop.

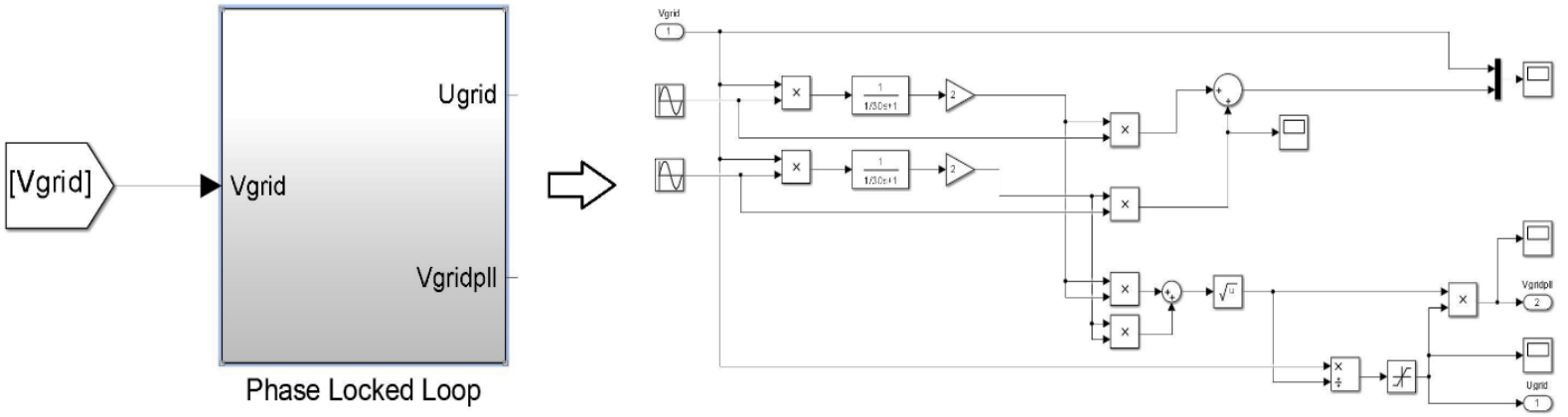


FIGURE 5.9: Simplified schematic showing the phase locked loop subsystem and its contents modelled in simulink.

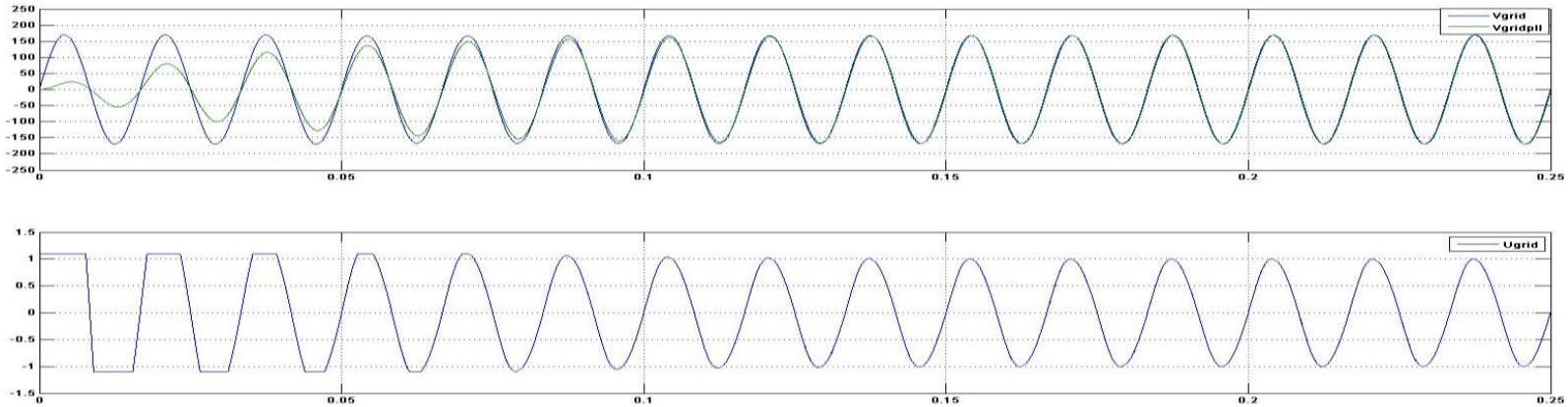


FIGURE 5.10: Simulation results showing grid voltage and grid voltage waveform having unit amplitude.

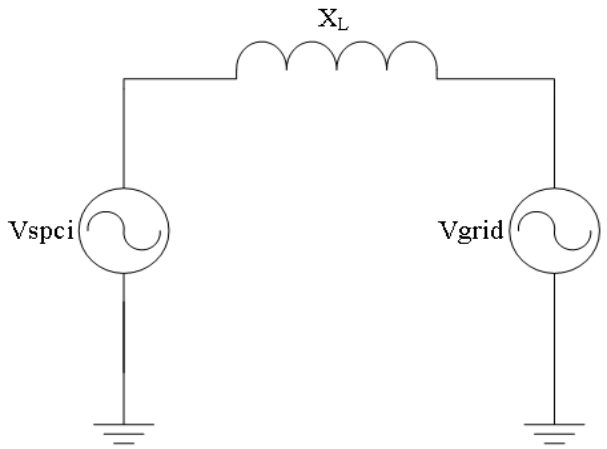


FIGURE 5.11: Simplified circuit schematic showing Solar Panel Companion Inverter as an ac voltage source connected to the grid via interfacing reactance.

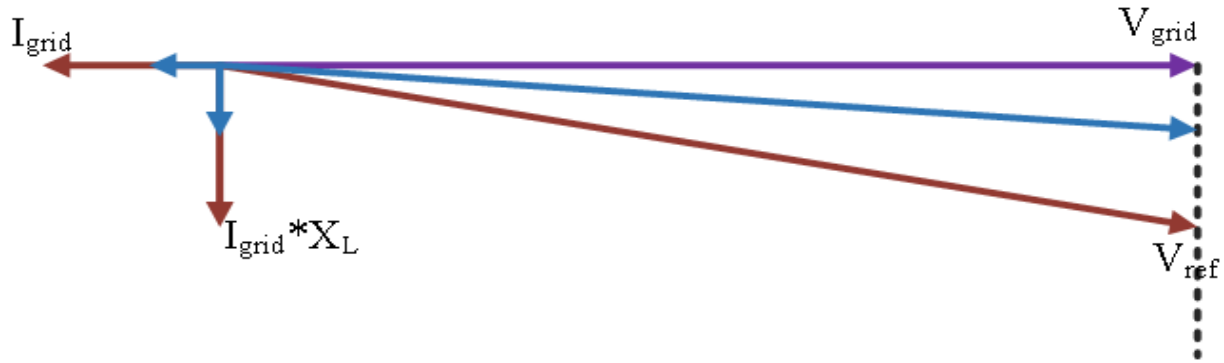


FIGURE 5.12: Phasor diagram showing the phasors of grid voltage, Vgrid, grid current, Igrid, reference voltage, Vref.

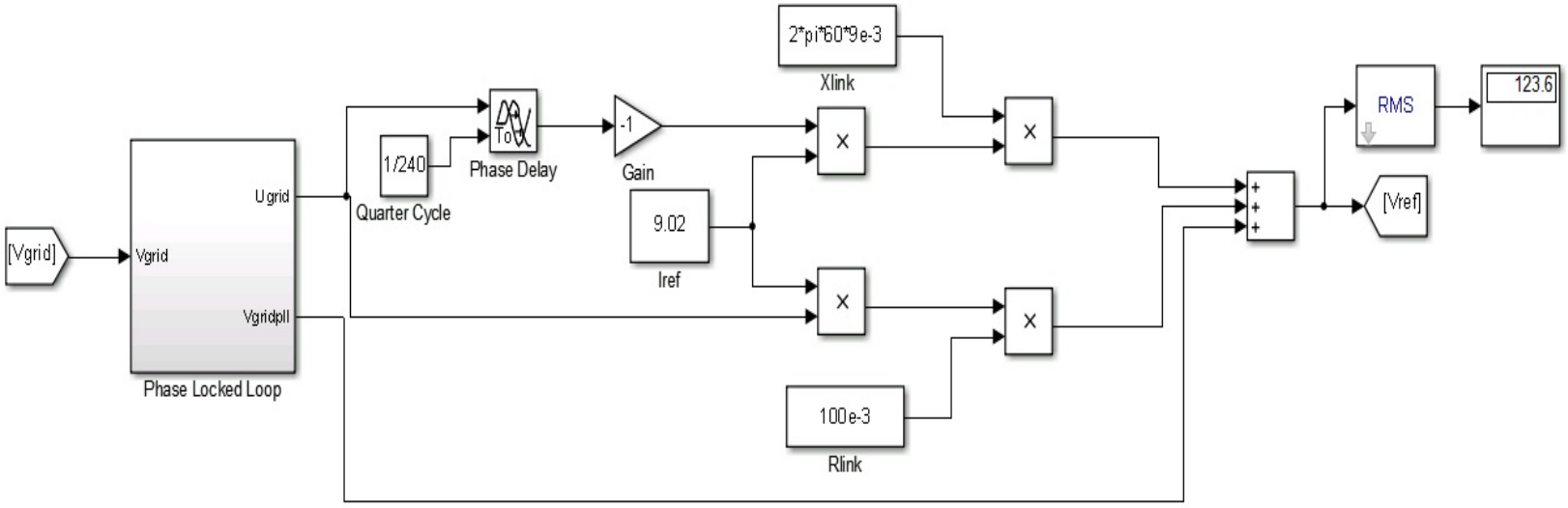


FIGURE 5.13: Simplified block schematic showing the simulink model to obtain the reference voltage.

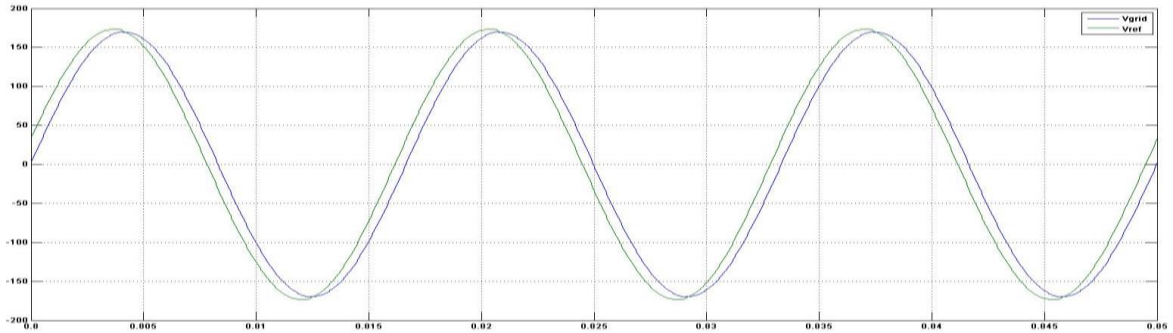


FIGURE 5.14: Simulation results showing grid voltage and reference voltage waveforms obtained from the PLL subsystem.

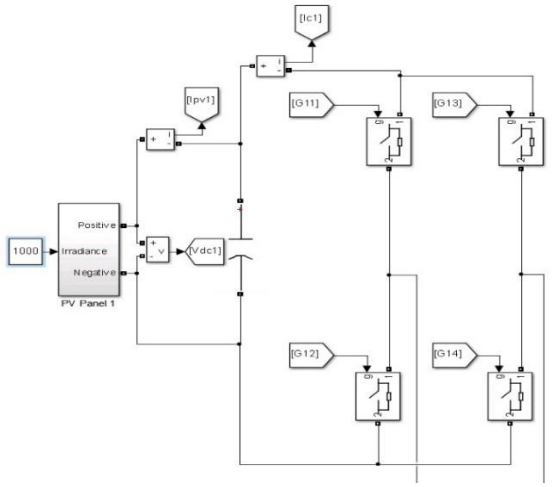


FIGURE 5.15: Simplified circuit schematic of a solar panel companion inverter.

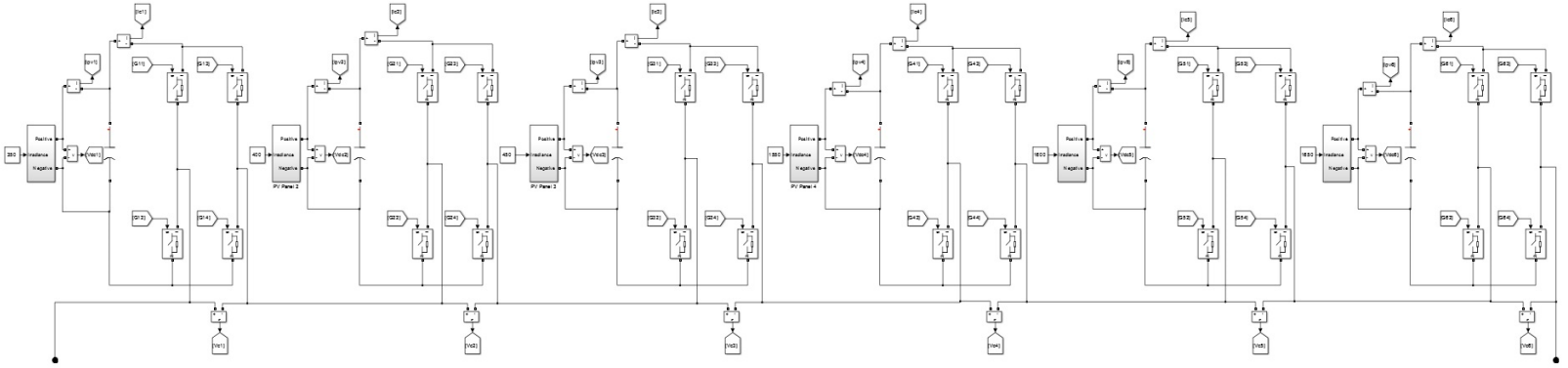


Figure 5.16: Simplified circuit schematic of a proposed 13-level solar panel companion inverter system for 120Vac applications.

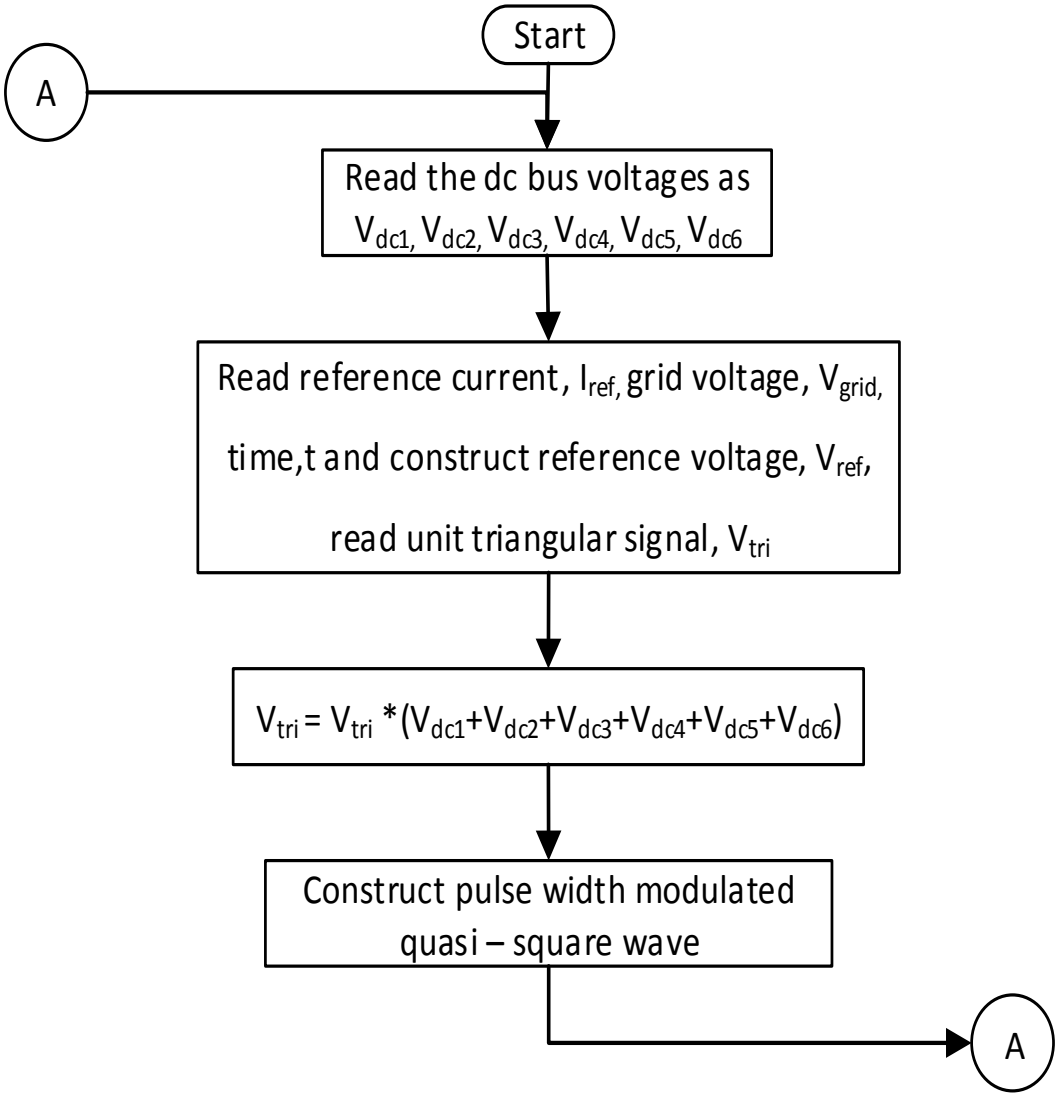


FIGURE 5.17: Flowchart for implementation of unsorted pulse width modulation.

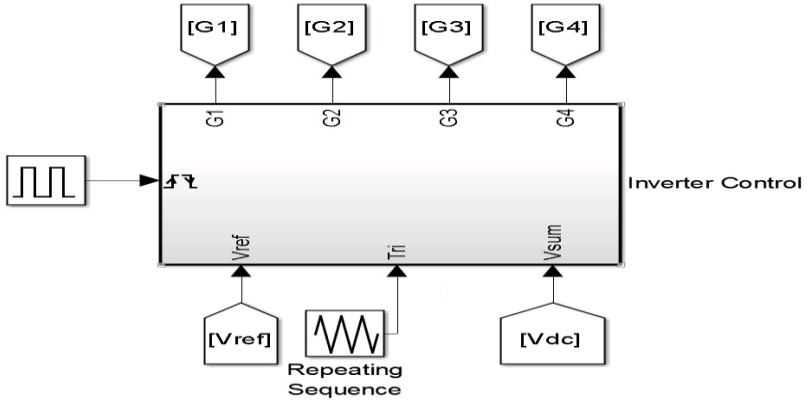


FIGURE 5.18: Master controller for unsorted pulse width modulation.

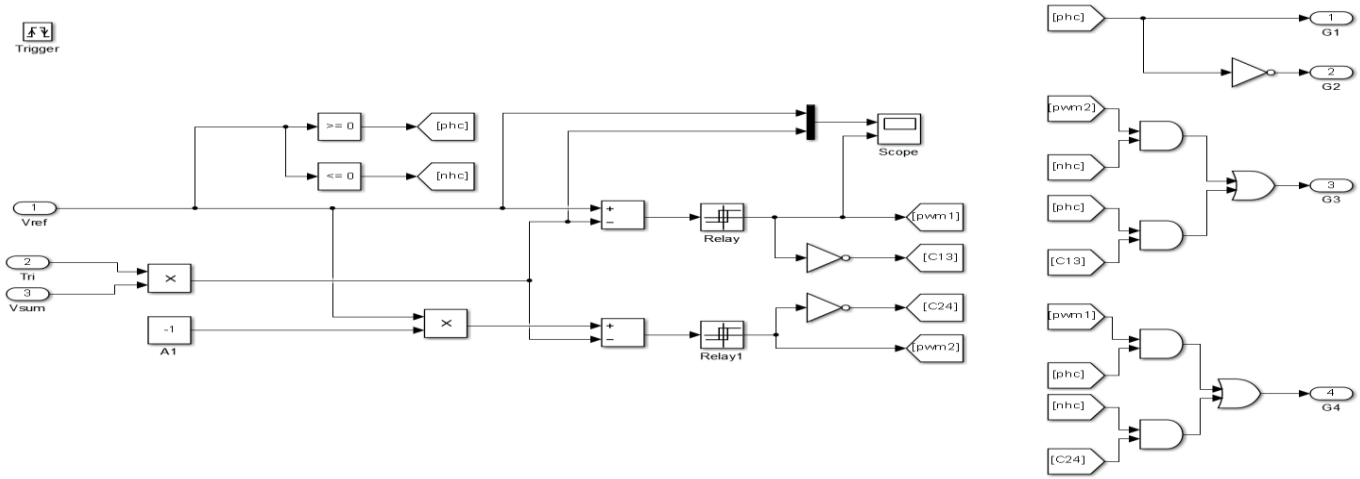


FIGURE 5.19: Simplified logical schematic showing the contents of unsorted pulse width modulation controller.

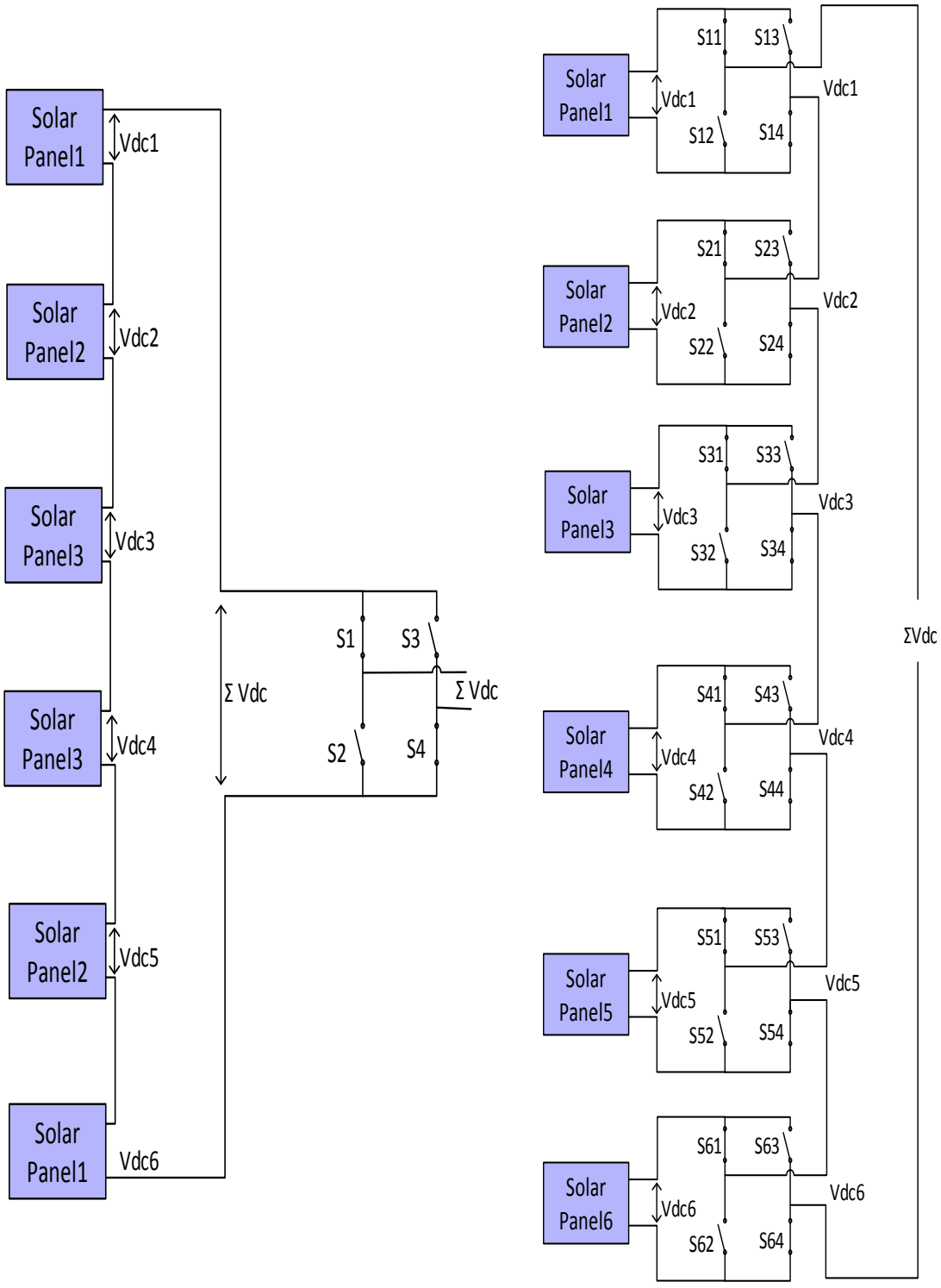


FIGURE 5.20: Simplified circuit schematic showing similarity in the operation of solar panel companion inverter and central inverter operated with unsorted pulse width modulation strategy. At any switching instance, sum of dc bus voltages across all the solar panel is equal.

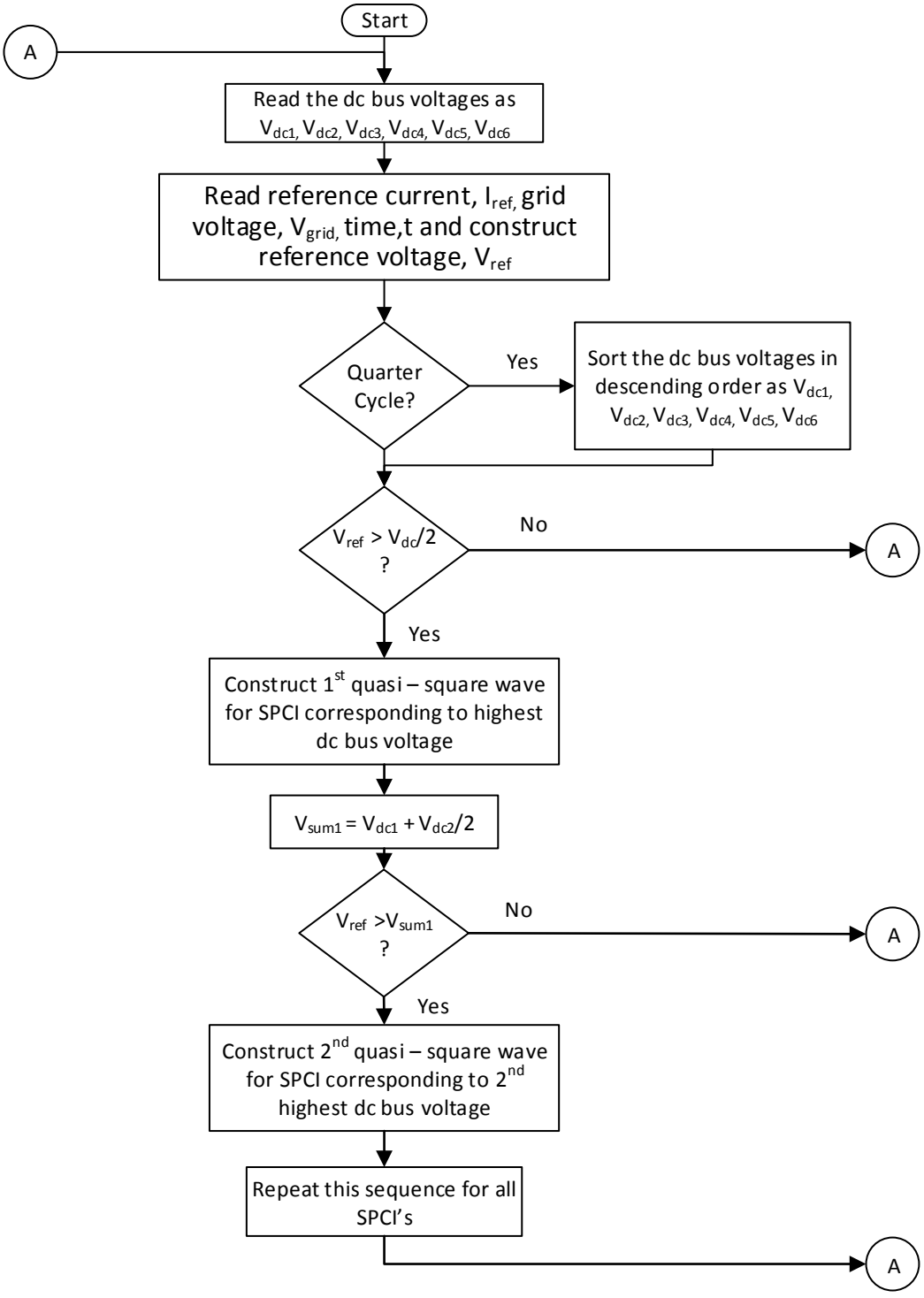


FIGURE 5.21: Flow chart for implementation of sorted stair case modulation.

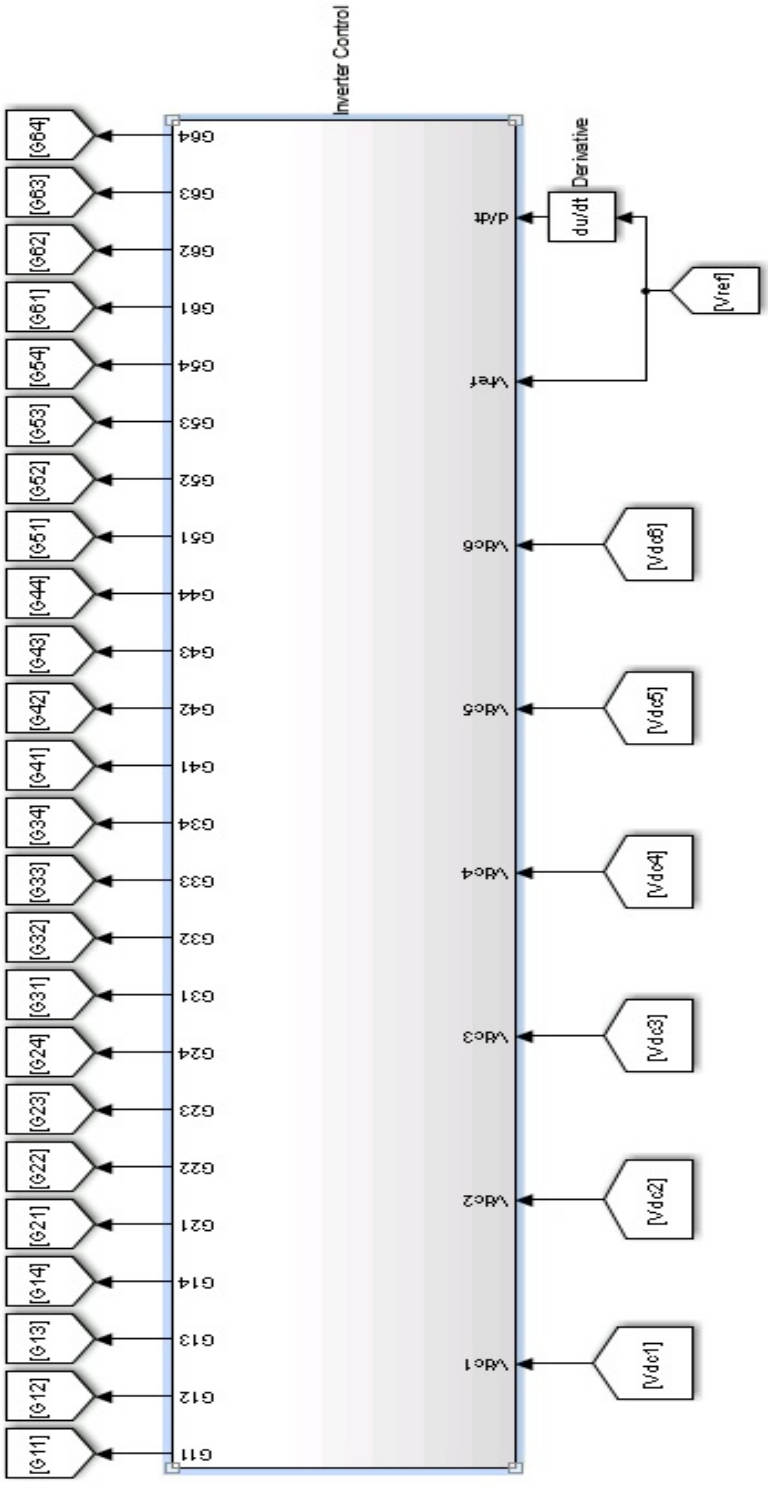


FIGURE 5.22: Master controller for sorted stair case modulation.

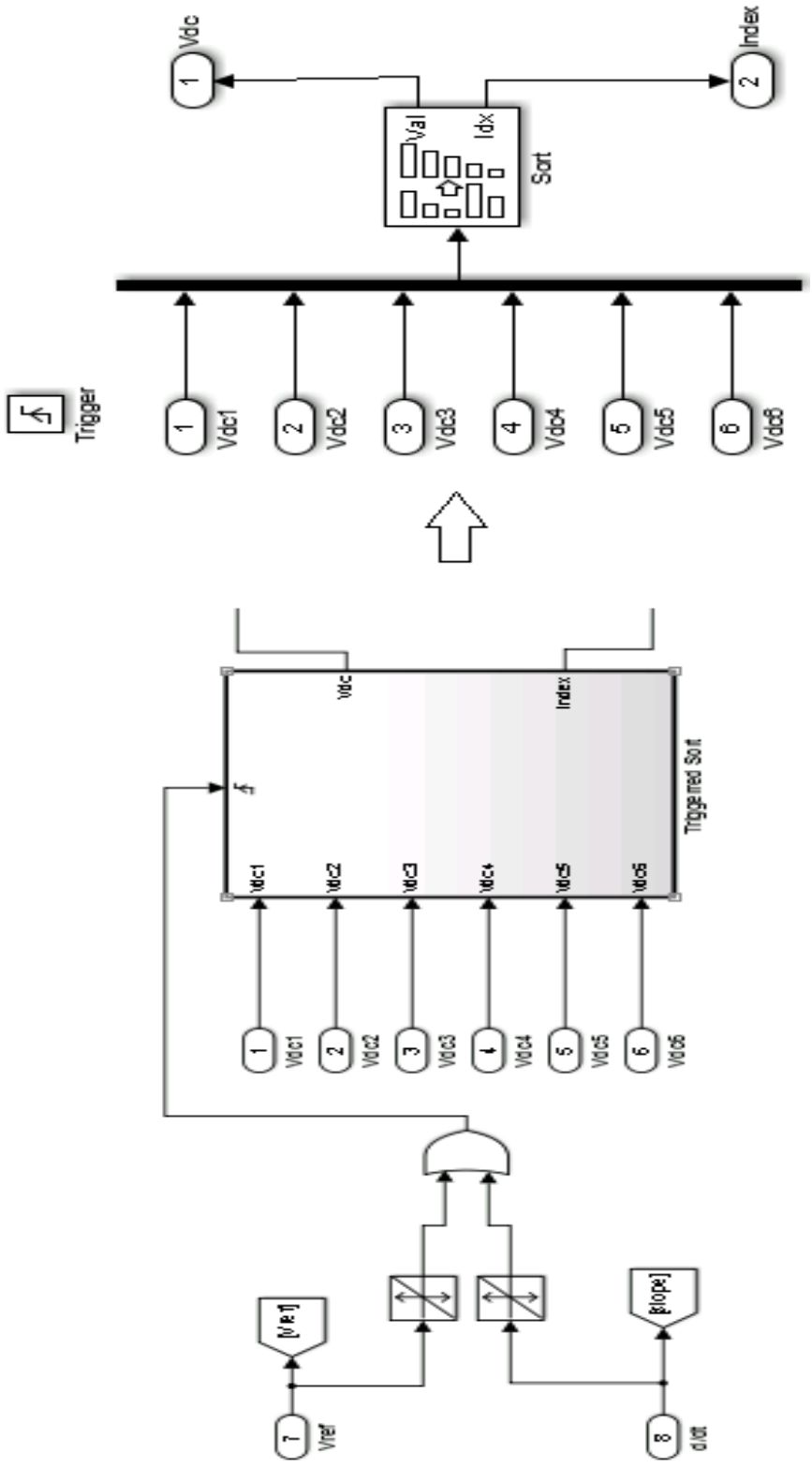


FIGURE 5.23: Simplified block schematic showing simulink subsystem of sorting logic and its contents.

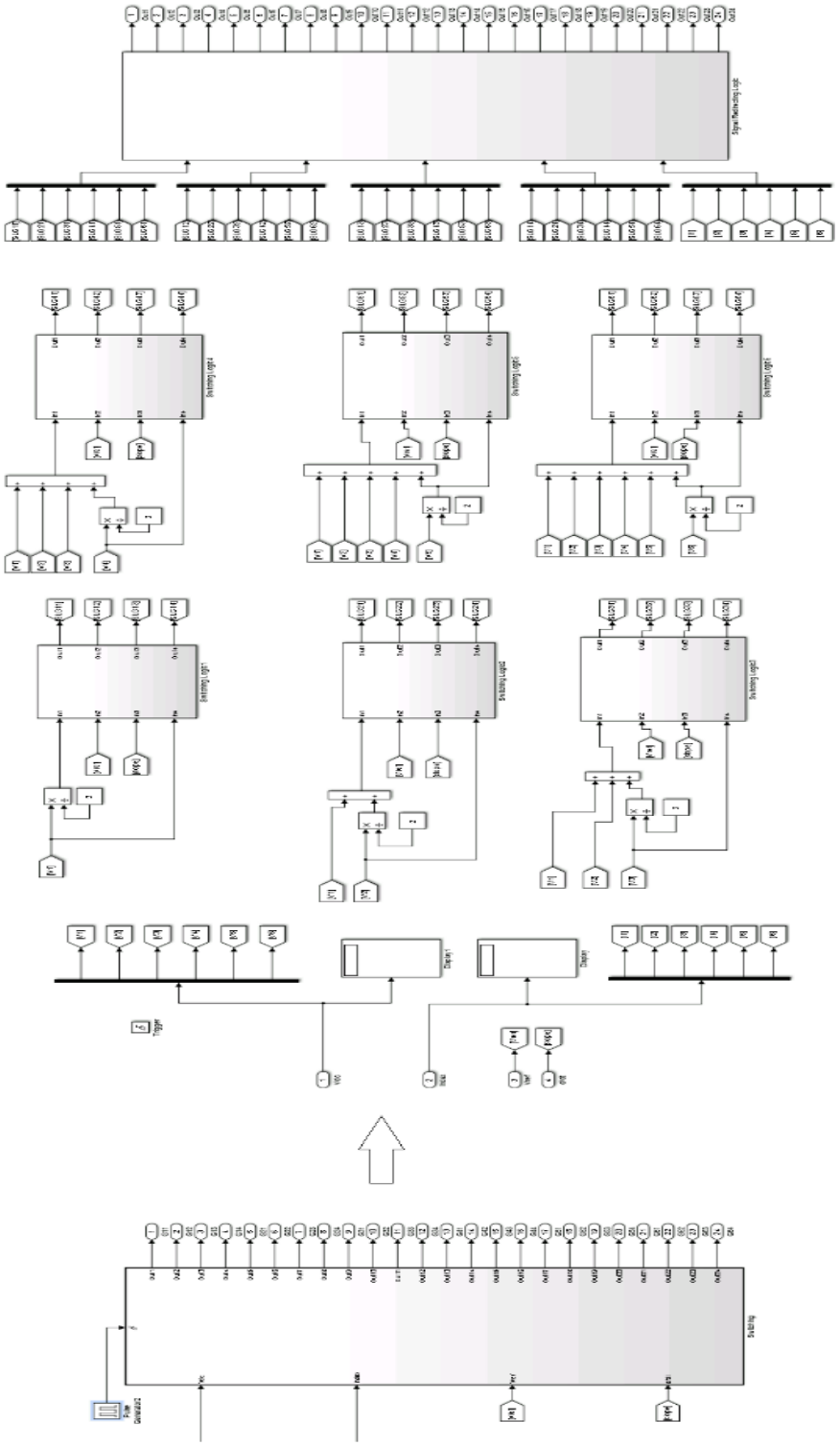


FIGURE 5.24 : Simplified block schematic showing the switching subsystem and its contents, for sorted stair case modulation controller.

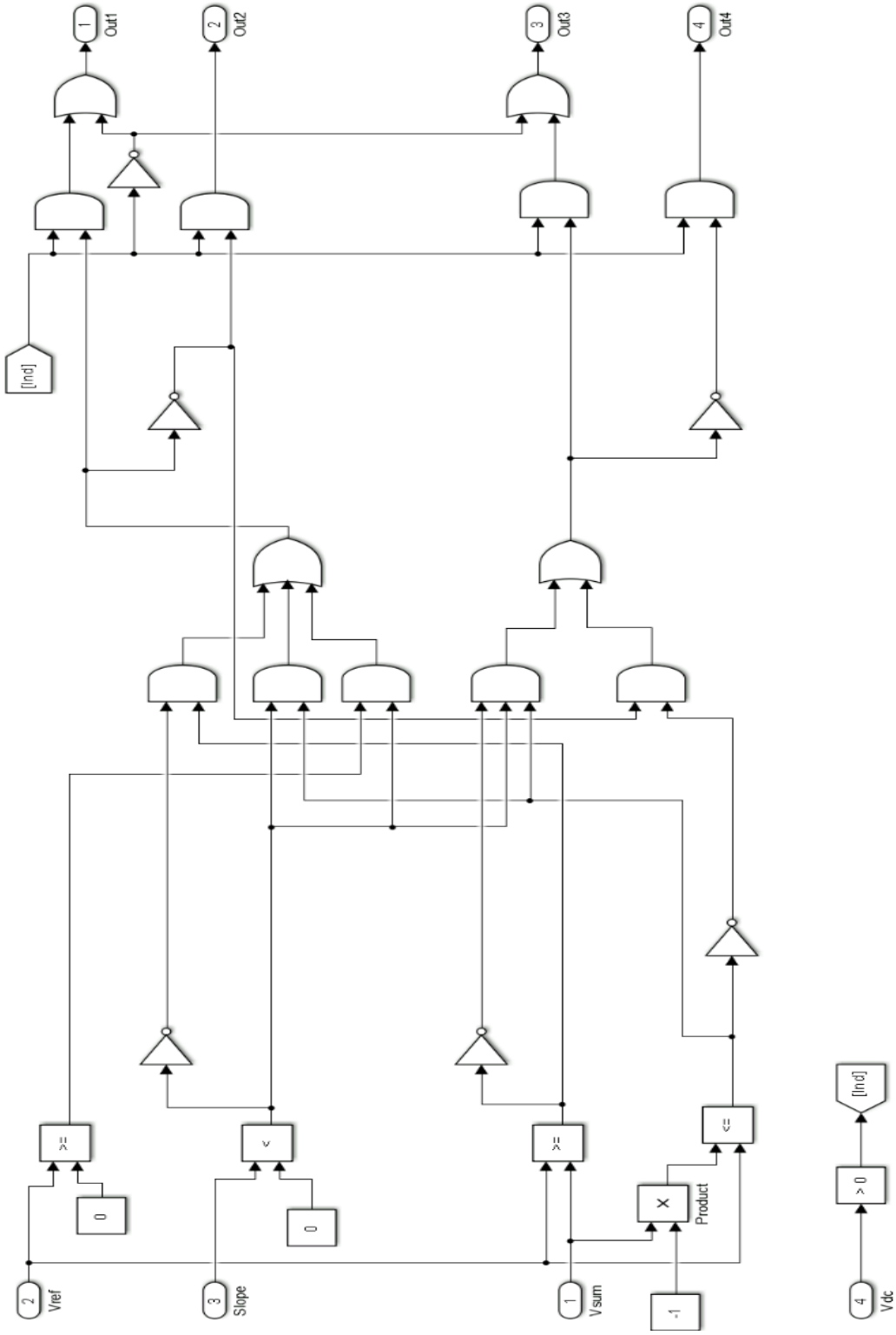


FIGURE 5.25: simplified schematic showing the switching logic for individual H – bridges.

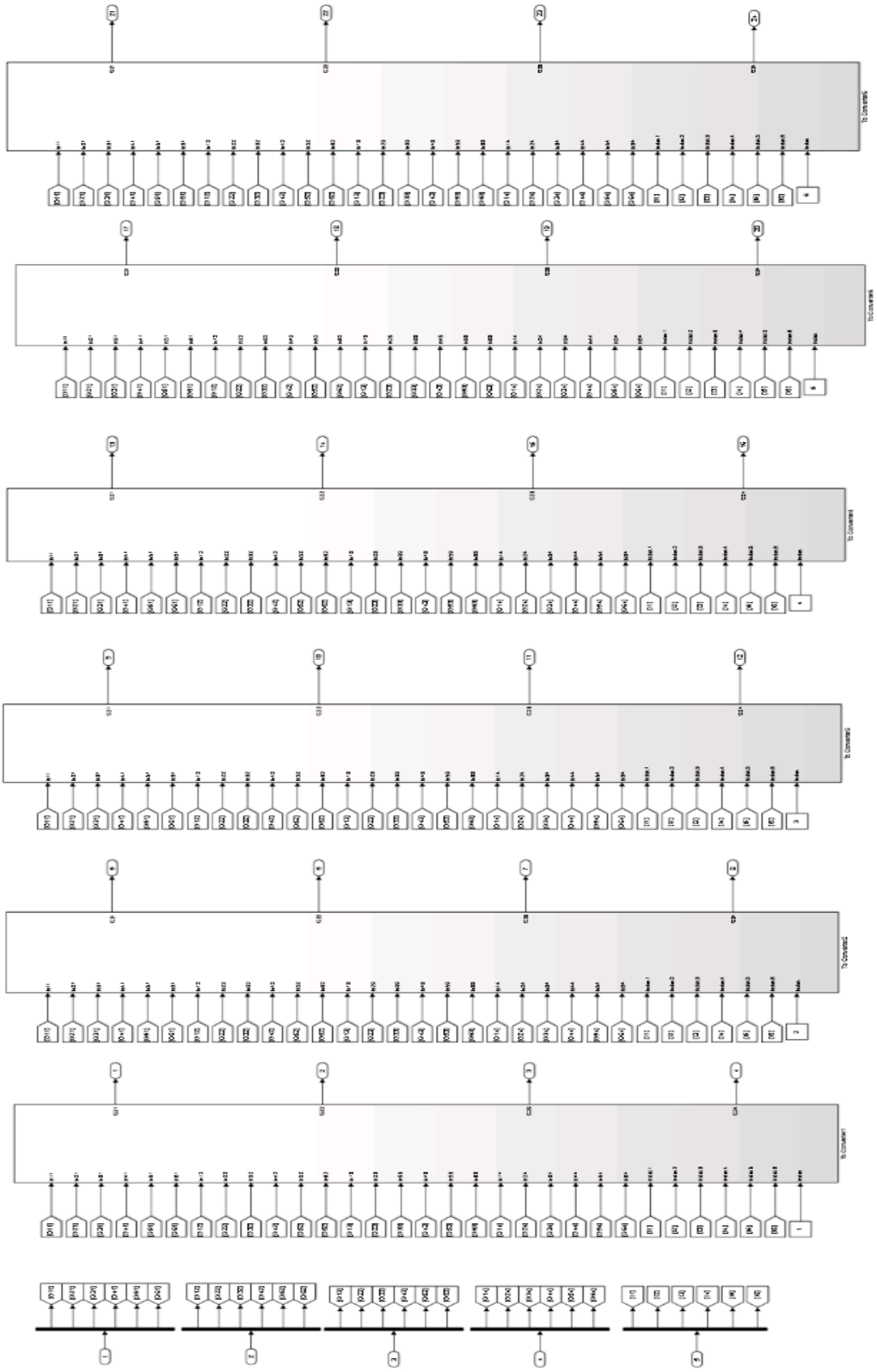


FIGURE 5.26: Simplified schematic showing the contents of signal redirecting logic.

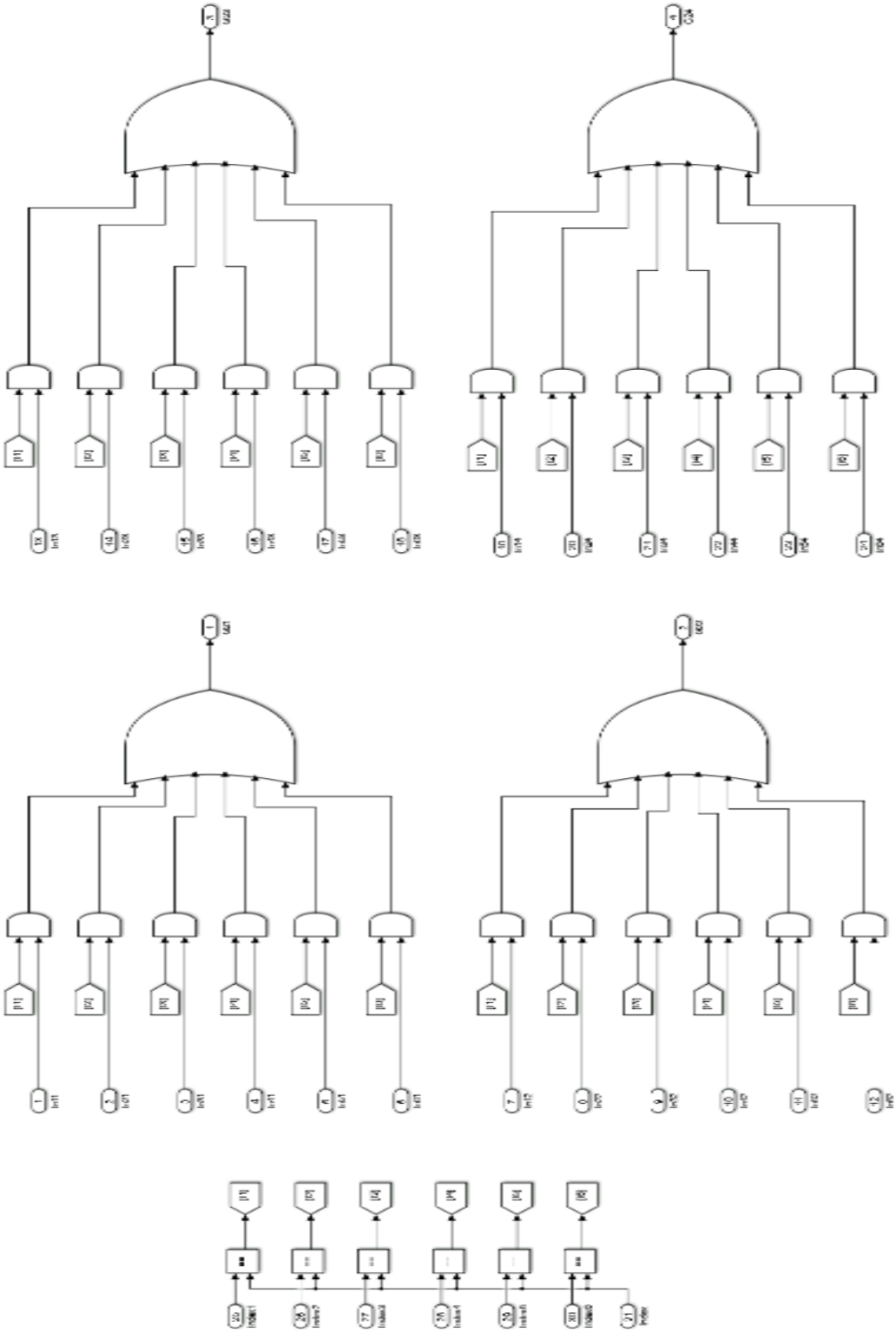


FIGURE 5.27: Simplified schematic showing the contents of signal redirecting logic for each h - bridge.

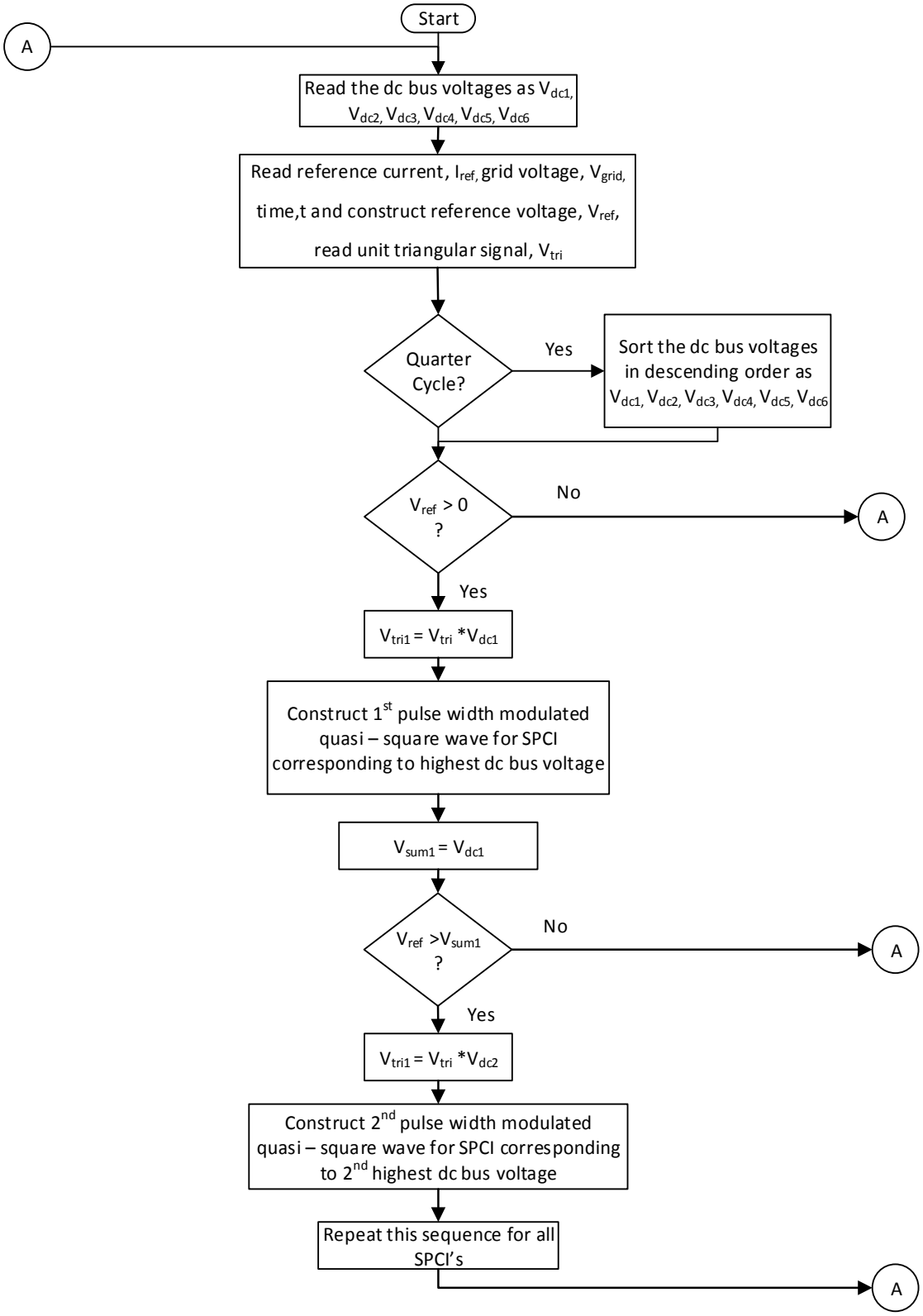


FIGURE 5.28: Flow chart for implementation of sorted pulse width modulation.

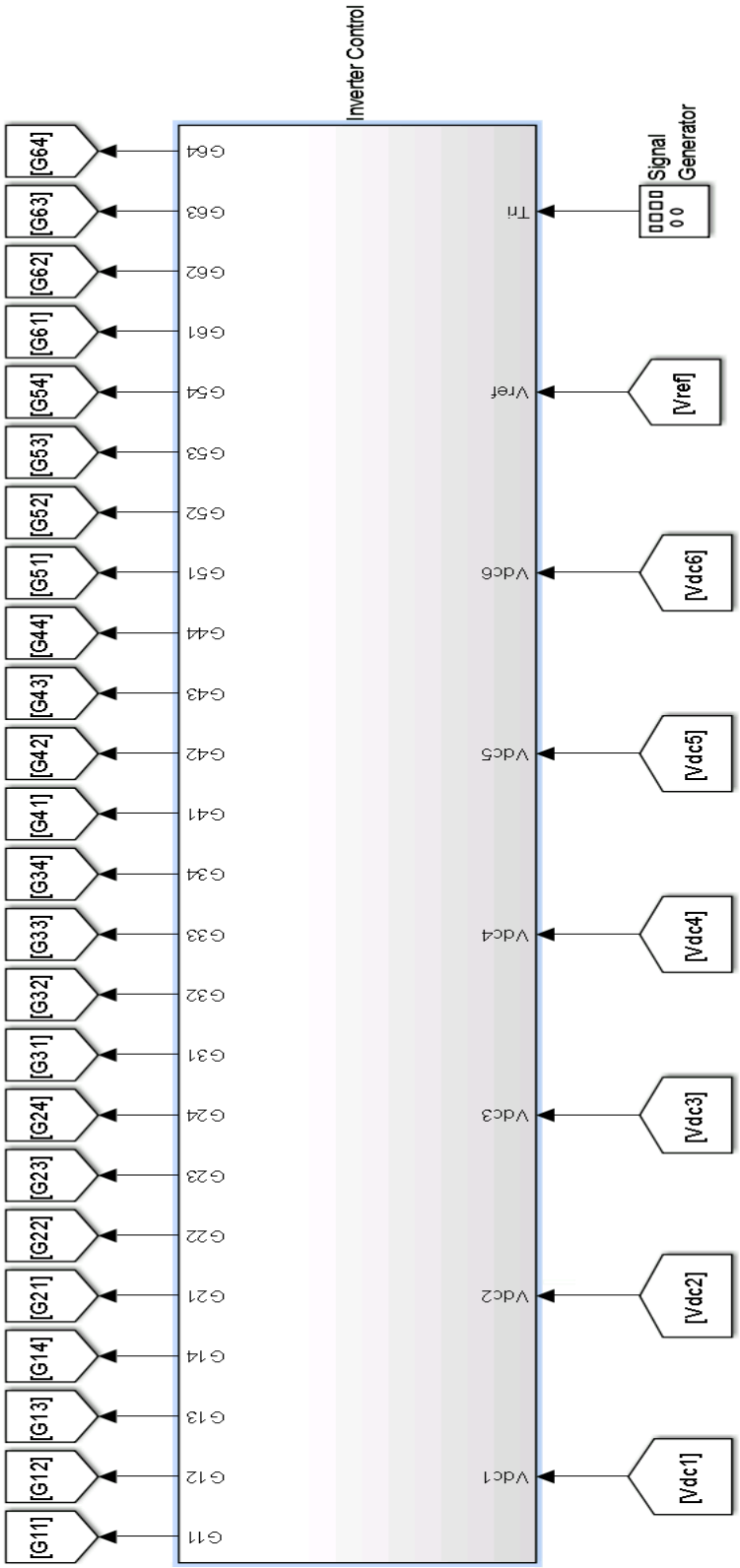


FIGURE 5.29: Master controller for sorted pulse width modulation.

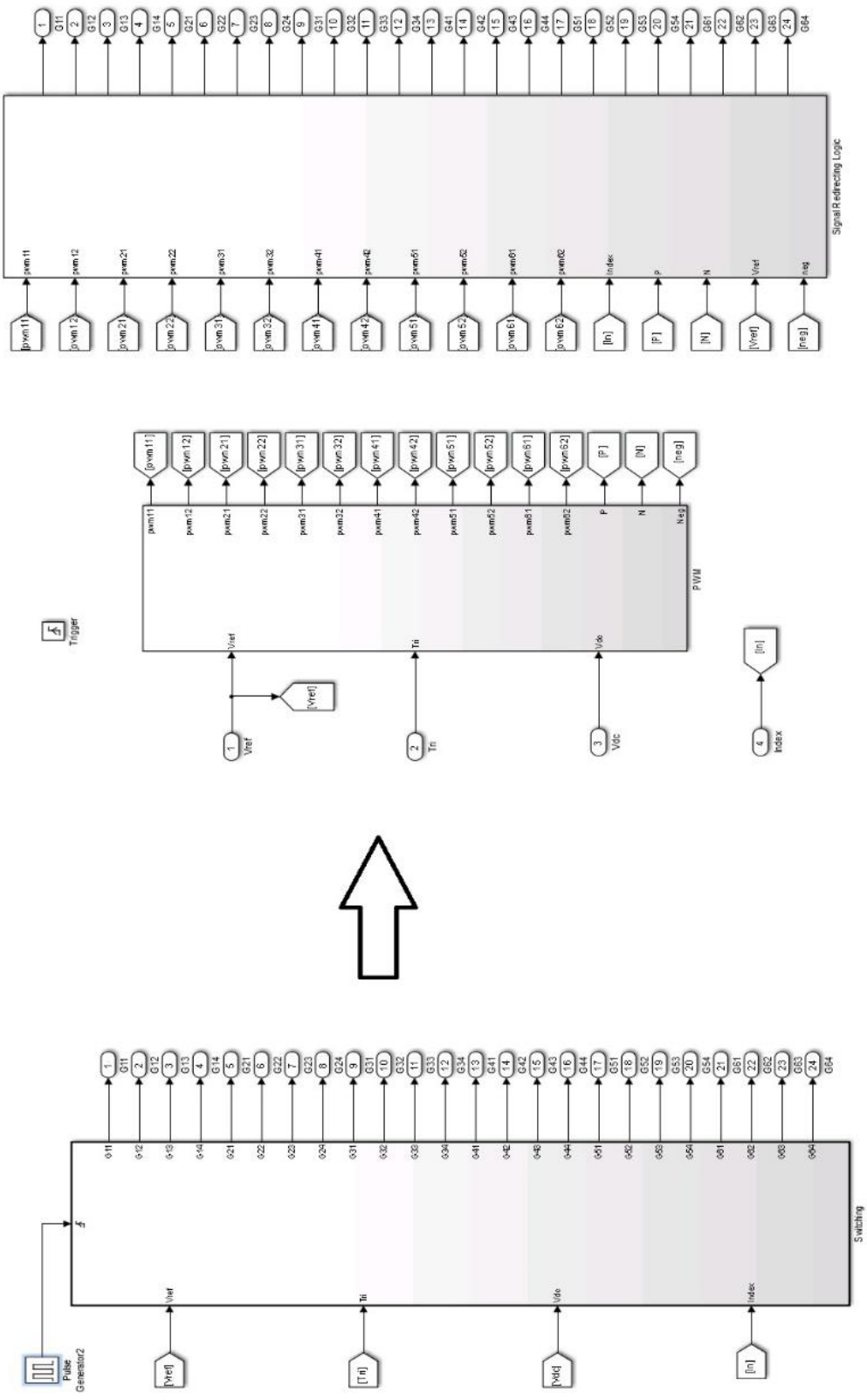


FIGURE 5.30: Simulink block schematic showing switching subsystem and its contents, for sorted pulse width modulation controller.

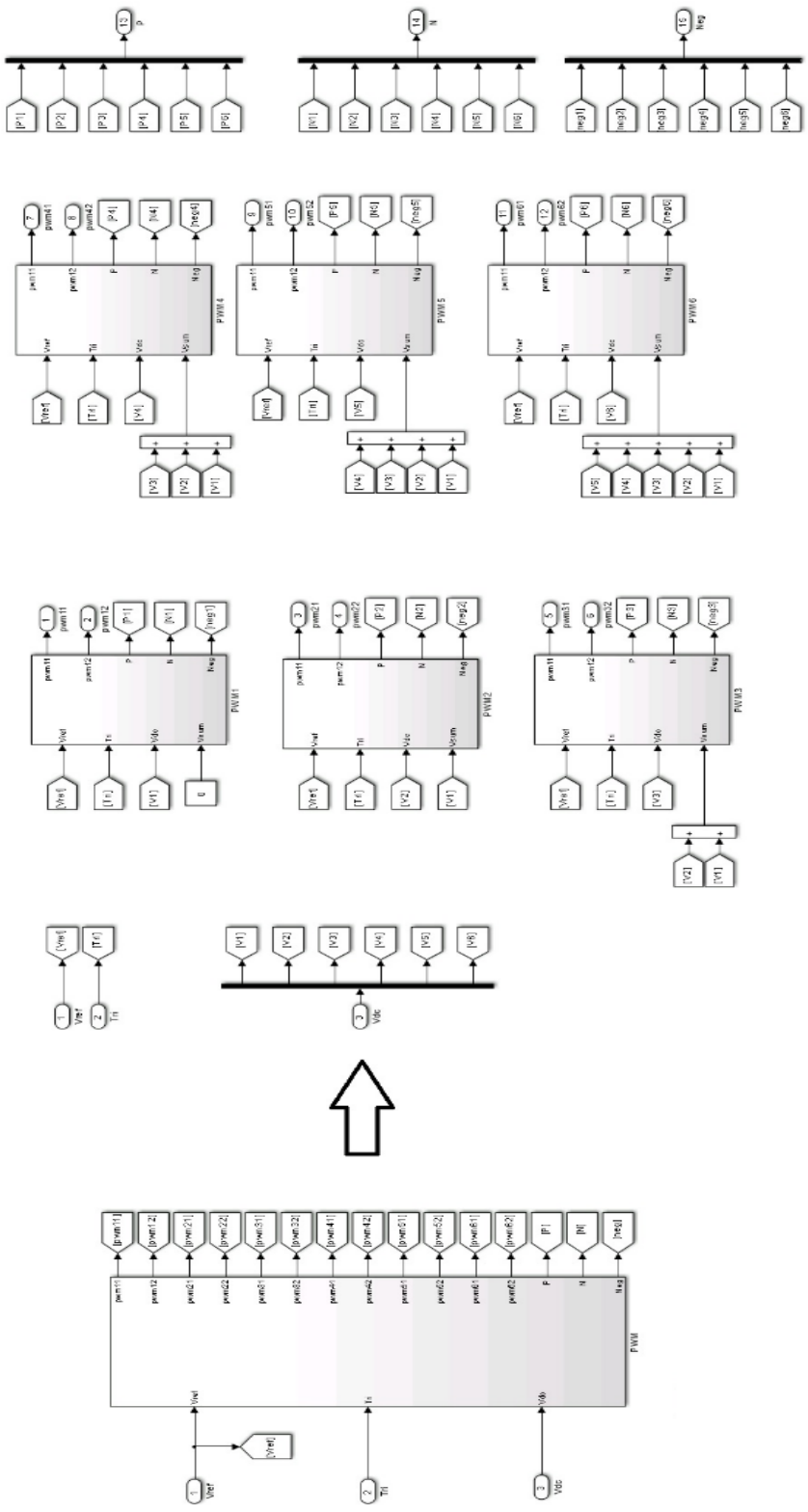


FIGURE 5.31: Simplified schematic showing the contents of PWM block.

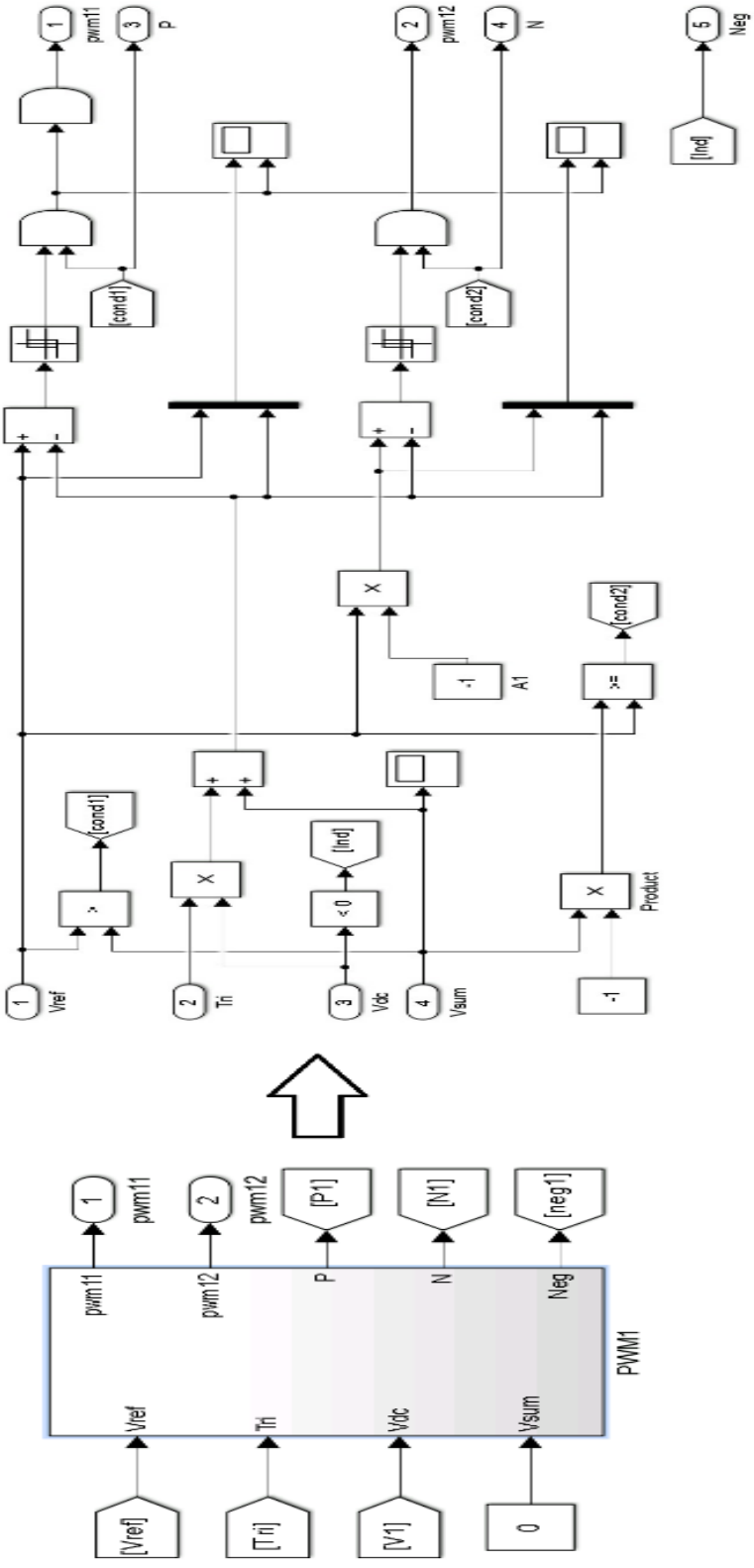


FIGURE 5.32: Simplified schematic showing the switching logic for individual H – bridges.

CHAPTER 6 : SIMULATION RESULTS

6.1. Introduction

In this chapter, operating scenarios of Solar Panel Companion Inverter (SPCI), and simulation results for various scenarios and control strategies are presented. Section 6.2 describes the operating scenarios and explains the terms such as mean, coefficient of variation, and percentage yield, that are used to evaluate the control strategies, namely: Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), Sorted Pulse Width Modulation (SPWM). An example showing the calculation of mean and coefficient of variation is also presented. In Section 6.3, simulation results for various operating scenarios corresponding to UPWM, SSCM, and SPWM, along with a discussion of the simulation results are presented.

6.2. Operating Scenarios

The maximum power that can be generated by a solar panel depends on the solar irradiance. In order to perform comparative analysis of the control strategies (discussed in Chapter 7), various operating scenarios are created for the SPCI using the following terms.

1. Percentage Yield (Y): Percentage yield for an operating scenario is defined as the ratio of actual dc power output of the solar panel for an operating scenario to the available dc power output for the same operating scenario.

$$\text{Percentage Yield (Y)} = \frac{\text{Extracted dc power output}}{\text{Available dc power output}} \tag{6.1}$$

2. Mean Irradiance (μ): Mean Irradiance is defined as the average irradiance incident on all the solar panels. For a solar system consisting of 'N' solar panels, if Irr_1, Irr_2,..., Irr_N are the irradiance incident on each solar panel, mean irradiance of the solar system can be written in the form of Equation 6.2.

Therefore,

$$\text{Mean Irradiance } (\mu) = \frac{\sum_{i=1}^{N} Irr_i}{N} \tag{6.2}$$

If all the panels have same irradiance value, then mean will be equal to the irradiance value of each panel. With an increase in the value of mean, the maximum power that is available in the photovoltaic system increases.

3. Coefficient of Variation (γ): If 'σ' is the standard deviation of irradiance, then coefficient of variation is defined as the ratio of standard deviation of irradiance to the mean of irradiance. This parameter quantifies the digression of irradiance from the mean value.

Therefore,

$$\text{Coefficient of Variation } (\gamma) = \frac{\sigma}{\mu} \tag{6.3}$$

where,

$$\text{Standard Deviation } (\sigma) = \sqrt{\frac{\sum_{i=1}^{N} (Irr_i - \mu)^2}{N}} \tag{6.4}$$

If all the panels have same irradiance value, then $I_{rri} = \mu$, therefore σ is zero and hence γ is zero. Consider an irradiance distribution, with I_{rr1} = 400 W/m^2, I_{rr2} = 500 W/m^2, I_{rr3} = 600 W/m^2, I_{rr4} = 700 W/m^2, I_{rr5}= 800 W/m^2, I_{rr6} = 1000 W/m^2. From Equation (6.1),

$$\text{Mean Irradiance } (\mu) = \frac{Irr_1 + Irr_2 + Irr_3 + Irr_4 + Irr_5 + Irr_6}{N} \tag{6.5}$$

Therefore,

$$\text{Mean Irradiance } (\mu) = \frac{400 + 500 + 600 + 700 + 800 + 1000}{6} \tag{6.6}$$

Therefore,

$$\text{Mean Irradiance } (\mu) = 666.67 \text{ W/m}^2 \tag{6.7}$$

From Equation 6.4, Standard deviation (σ) =

$$\sqrt{\frac{(1000-666.67)^2 + (800-666.67)^2 + (700-666.67)^2}{(600-666.67)^2 + (500-666.67)^2 + (400-666.67)^2}{6}} \tag{6.8}$$

Therefore,

$$\text{Standard deviation } (\sigma) = 197.2 \tag{6.9}$$

From Equation (6.3), Coefficient of Variation (γ) = $\frac{\sigma}{\mu} = \frac{197.2}{666.67}$

Therefore,

$$\text{Coefficient of Variation } (\gamma) = 0.3 \tag{6.10}$$

Figure 6.1 and Figure 6.2 shows I – V and P – V curves for uniform and non - uniform irradiance behaviors respectively. It may be seen from I – V curves that higher the value of irradiance, higher is the value of the corresponding short circuit current. From the P – V curves it may be seen that higher the value of irradiance, higher is the maximum power that can be extracted. Coefficient of variation together with the mean irradiance forms an operating scenario. Depending on the sunlight that is incident on the surface of a panel, an operating scenario can be of two types:

1. Uniform Irradiance: The system is said to be operating in uniform irradiance scenario, if the incident light on all the solar panels have the same irradiance. In this case, I – V and P – V characteristics of all panels are the same for all the panels as shown in Figure 6.1. The coefficient of variation is zero for uniform irradiance.

2. Non – Uniform Irradiance: The system is said to be operating in non – uniform irradiance scenario, if there is a disparity in irradiance of the light incident on the solar panels, and in this case, the I – V and the P – V characteristics of all the panels are similar to that of Figure 6.2. Coefficient of variation for non – uniform irradiance is any value between 0 and 1.

6.3. Simulation Results

Simulations using Unsorted Pulse Width Modulation, Sorted Stair Case Modulation, and Sorted Pulse Width Modulation control strategies are performed for various scenarios of uniform and non – uniform irradiance. Three representative operating scenarios are selected to illustrate the behavior of control strategies as applied to Solar Panel Companion Inverter (SPCI) are summarized in Table 6.1. One scenario where the coefficient of irradiance is zero represents uniform irradiance and the other two scenarios represent cases of non – uniform irradiance behavior. In Sections 6.3.1 and 6.3.2, output waveforms of all the three control strategies corresponding to three scenarios mentioned in Table 6.1 are presented. The main area of focus is operating the SPCI at maximum power point. This is performed with the help of an open loop current control. The reference current is tuned each time a simulation is performed, to make sure that the SPCI is operated at maximum power point, and the results corresponding to the maximum power point operation is presented.

6.3.1. Unsorted Pulse Width Modulation

Unsorted pulse width modulated output ac voltage waveform of Solar Panel Companion Inverter (SPCI) is shown in Figure 6.3, Figure 6.4, and Figure 6.5. For each operating scenario, the waveforms are generated by applying Unsorted Pulse Width Modulation (UPWM) explained in Section 4.2 of Chapter 4. Figure 6.3 shows the simulation results for coefficient of variation, $\gamma = 0$ and mean irradiance, $\mu = 200$. Table 6.2 shows the simulation results for this scenario. The first plot shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles in a single plot, for scenario 1. The second plot shows the grid current waveform for three cycles. The plot for dc output power of solar panels shows that all the panels are operating at maximum power point. Since this is a scenario for uniform irradiance, the dc output power of the panels and the dc bus voltages of all the panels are oscillating about the same maximum power operating point.

Figure 6.4 shows the simulation results for coefficient of variation, $\gamma = 0.2$ and mean irradiance, $\mu = 600$. Table 6.3 shows the simulation results for this scenario. The first plot shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles in a single plot, for scenario 2. As compared to scenario one, since the mean of irradiance in this scenario is greater, the output power availability and hence the actual output power generated is also greater than the previous scenario. The magnitude of reference current is also greater than that of the reference current in scenario 1, because of greater mean irradiance. It can be seen in Table 6.3, that magnitude of ac reference grid current provided is 5.66 A. From the plot for dc power output of all the panels, it can be seen that only the panel with lowest irradiance is

operating at its maximum power point. The remaining panels are not operating at their maximum power points.

Figure 6.5 shows the simulation results for coefficient of variation, $\gamma = 0.4$ and mean irradiance, $\mu = 1000$. Table 6.4 shows the simulation results for this scenario. The first plot shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles in a single plot, for scenario 3. Since the mean of irradiance in this scenario is greatest of scenario 1, scenario 2 and scenario 3, the output power availability and hence the actual output power generated is also greatest of the three scenarios. The magnitude of reference current is also greatest because of greatest mean irradiance. It can be seen in Table 6.4, that magnitude of ac reference grid current provided is 7A. From the plot for dc power output of all the panels, it can be seen that only the panel with lowest irradiance is operating at its maximum power point. The remaining panels are not operating at their maximum power points.

6.3.2. Sorted Stair Case Modulation

Sorted stair case modulated output ac voltage waveform of Solar Panel Companion Inverter as shown in Figure 6.6, Figure 6.7, and Figure 6.8 for each operating scenario, is generated by applying Sorted Stair Case Modulation explained in Section 4.2 of Chapter 4. Figure 6.6 shows the simulation results for coefficient of variation, $\gamma = 0$ and mean irradiance, $\mu = 200$. Table 6.5 shows the simulation results for this scenario. The first plot shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles are shown in a single plot, for scenario 1. It can be seen in Table 6.5, that magnitude of ac reference grid current provided is 2.99A and in grid current plot for three cycles, which is plot 2 of Figure 6.6, it may be

seen that the magnitude of grid current is approximately 3A. The plot for dc output power of solar panels shows that all the panels are operating at their maximum power points. Since this is a scenario for uniform irradiance, the dc output power of the panels and the dc bus voltages of all the panels are oscillating about the same maximum power operating point.

Figure 6.7 shows the simulation results for coefficient of variation, $\gamma = 0.2$ and mean irradiance, $\mu = 600$. Table 6.6 shows the simulation results for this scenario. The first plot shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles are shown in a single plot, for scenario 2. As compared to scenario 1, since the mean of irradiance in this scenario is greater, the output power availability and hence the actual output power generated is also greater than the previous scenario. The magnitude of reference current is also greater than that of the reference current in scenario 1, because of greater mean irradiance. It can be seen in Table 6.6, that magnitude of ac reference grid current provided is 9.375A and in grid current plot for three cycles, which is plot 2 of Figure 6.7, it may be seen that the magnitude of grid current is approximately 10A. Because of low coefficient of variation, there is no much variation in the voltage at maximum power point of the solar panels, as may be seen in Table 6.1, and hence, the dc bus voltages of all the panels are oscillating about the same point. However, the dc output power of the panels are oscillating about their corresponding maximum power points which is not the same, because of the disparity in irradiance.

Figure 6.8 shows the simulation results for coefficient of variation, $\gamma = 0.4$ and mean irradiance, $\mu = 1000$. Table 6.7 shows the simulation results for this scenario. The first plot

shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles are shown in a single plot, for scenario 3. Since the mean of irradiance in this scenario is greatest of scenario 1, scenario 2 and scenario 3, the output power availability and hence the actual output power generated is also greatest of the three scenarios. The magnitude of reference current is also greatest because of greatest mean irradiance. It can be seen in Table 6.7, that magnitude of ac reference grid current provided is 14.18A and in grid current plot for three cycles, which is plot 2 of Figure 6.8, it may be seen that the magnitude of grid current is approximately 13.9A. Because of coefficient of variation more than that of scenario 1 and scenario 2, there is a significant variation in the voltage at maximum power point of the solar panels, as may be seen in Table 6.1, and hence, the dc bus voltages of all the panels are oscillating about the different points and similar to scenario 2, the dc output power of the panels are oscillating about their corresponding maximum power points which is not the same, because of the disparity in irradiance. It can also be seen that the magnitude of oscillations in dc output power is for scenario 3 is very high, because of which, the percentage yield got affected.

6.3.3. Sorted Pulse Width Modulation

Sorted pulse width modulated output ac voltage waveform of Solar Panel Companion Inverter as shown in Figure 6.9, Figure 6.10, and Figure 6.11 for each operating scenario, is generated by applying Sorted Pulse Width Modulation explained in Section 4.4 of Chapter 4. Figure 6.9 shows the simulation results for coefficient of variation, $\gamma = 0$ and mean irradiance, $\mu = 200$. Table 6.8 shows the simulation results for this scenario. The first plot shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized

output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles are shown in a single plot, for scenario 1. It can be seen in Table 6.8, that magnitude of ac reference grid current provided is 3.226A and in grid current plot for three cycles, which is plot 2 of Figure 6.9, it may be seen that the magnitude of grid current is approximately 3A. Similar to scenario 1 of Sorted Stair Case Modulation, the plot for dc output power of solar panels shows that all the panels are operating at maximum power point. Since this is a scenario for uniform irradiance, the dc output power of the panels and the dc bus voltages of all the panels are oscillating about the same maximum power operating point.

Figure 6.10 shows the simulation results for coefficient of variation, $\gamma = 0.2$ and mean irradiance, $\mu = 600$. Table 6.9 shows the simulation results for this scenario. The first plot shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles are shown in a single plot, for scenario 2. As compared to scenario 1, since the mean of irradiance in this scenario is greater, the output power availability and hence the actual output power generated is also greater than the previous scenario. The magnitude of reference current is also greater than that of the reference current in scenario 1, because of greater mean irradiance. It can be seen in Table 6.9, that magnitude of ac reference grid current provided is 9.64A and in grid current plot for three cycles, which is plot 2 of Figure 6.10, it may be seen that the magnitude of grid current is approximately 9.8A. Because of low coefficient of variation, there is no much variation in the voltage at maximum power point of the solar panels, as may be seen in Table 6.1, and hence, the dc bus voltages of all the panels are oscillating about the same point. However, the dc output power of the panels are oscillating about

their corresponding maximum power points which is not the same, because of the non - uniformity in irradiance.

Figure 6.11 shows the simulation results for coefficient of variation, $\gamma = 0.4$ and mean irradiance, $\mu = 1000$. Table 6.10 shows the simulation results for this scenario. The first plot shows the waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for three cycles are shown in a single plot, for scenario 3. Since the mean of irradiance in this scenario is greatest of scenario 1, scenario 2 and scenario 3, the output power availability and hence the actual output power generated is also greatest of the three scenarios. The magnitude of reference current is also greatest because of greatest mean irradiance. It can be seen in Table 6.10, that magnitude of ac reference grid current provided is 14.18A and in grid current plot for three cycles, which is plot 2 of Figure 6.11, it may be seen that the magnitude of grid current is approximately 14A. Because of coefficient of variation more than that of scenario 1 and scenario 2, there is a reasonable variation in the voltage at maximum power point of the solar panels, as may be seen in Table 6.1, and hence, the dc bus voltages of all the panels are oscillating about the different points and similar to scenario 2, the dc output power of the panels are oscillating about their corresponding maximum power points which is not the same, because of the disparity in irradiance. It can also be seen that the magnitude of oscillations in dc output power is for scenario 3 is very high, because of which, the percentage yield got affected.

From the simulation results of plots corresponding to dc output power, it can be seen that the magnitude of dc output power oscillations for, $\gamma = 0.2$ is greater than the magnitude of dc output power oscillations of all the panels as the coefficient of variation, $\gamma = 0$, and

the magnitude of dc output power oscillations for $\gamma = 0.4$ is the greatest of the three operating scenarios, 1, 2, and 3. Therefore, as the disparity in solar irradiance increases, the magnitude of dc output power oscillations for each panel also increases, which decreases the average dc power output of each panel and ultimately the average total dc power output.

6.3.4. Discussion on Simulation Results

The consolidated result showing the percentage yield for the three operating scenarios: ($\gamma = 0$, $\mu = 200$), ($\gamma = 0.2$, $\mu = 600$), and ($\gamma = 0.4$, $\mu = 1000$), using Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM) is tabulated in Table 6.11. From this table, it can be seen that for $\gamma=0$, UPWM offers the best energy yield. The operating region of the solar panels for the operating scenario $\gamma = 0$, and $\mu = 200$ is shown a by thick line in Figure 6.12. For a moderate value of $\gamma =0.2$, SSCM offers the best energy yield. The operating region of the solar panels for the operating scenario $\gamma = 0$, and $\mu = 200$ is shown a by thick line in Figure 6.13. And as γ increases to an extreme value of 0.4, SPWM offers the best energy yield. We extend this analysis to a broader range of coefficient of variation, γ ($0\leq \gamma\leq 0.4$), and mean irradiance, μ ($200\leq \mu\leq 1000$) and the results are presented in Chapter 8.

TABLE 6.1: Operating scenarios for which the simulation results are presented.							
Scenario #	Coefficient of Variation (γ)	Mean Irradiance (μ)	Irradiance (W/m^2)	Maximum Power Point Voltage , V_{mpp} (V)	Maximum Power Point Current , I_{mpp} (A)	Maximum available power in each panel (W)	Total maximum available power (W)
1	0	200	200	31.73	1.35	42.85	257.10
2	0.2	600	450	33.85	3.05	103.26	847
			480	33.93	3.26	110.73	
			510	34.21	3.46	118.23	
			690	34.82	4.71	163.88	
			720	35.15	4.88	171.58	
			750	35.18	5.1	179.32	
3	0.4	1000	550	34.54	3.734	128.284	1476.51
			600	34.61	4.071	140.929	
			650	34.84	4.41	153.652	
			1350	36.756	9.189	337.763	
			1400	36.529	9.613	351.148	
			1450	36.735	9.928	364.734	

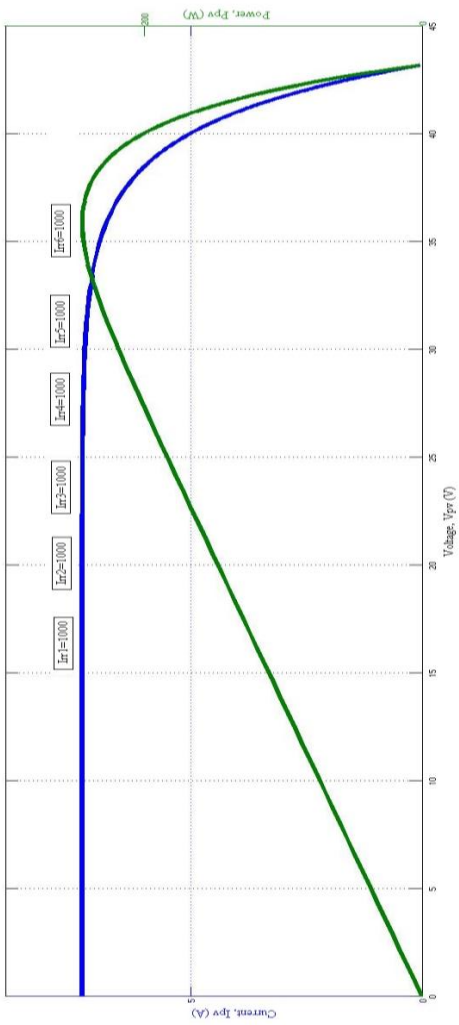


FIGURE 6.1: I-V and P –V characteristics under uniform irradiance behavior of 1000 W/m2.

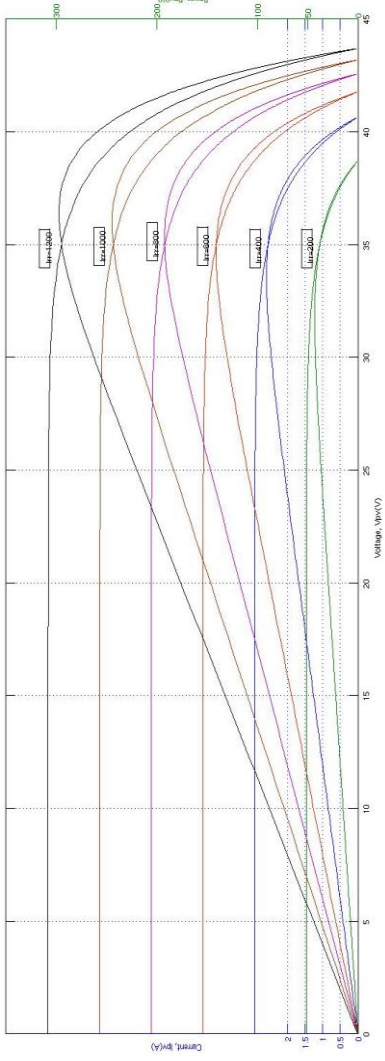


FIGURE 6.2: I – V and P – V characteristics for irradiance of Irr1 = 400 W/m2, Irr2 = 500 W/m2, Irr3 = 600 W/m2, Irr4 = 700 W/m2, Irr5= 800 W/m2, Irr6 = 1000 W/m2.

TABLE 6.2: Simulation results for Unsorted Pulse Width Modulation with coefficient of variation, $\gamma = 0$ and mean irradiance, $\mu = 200$.

Reference current (A)	Available power (W)	Extracted Power (W)	%Yield (Y)
2.41	257.10	254.5	98.99

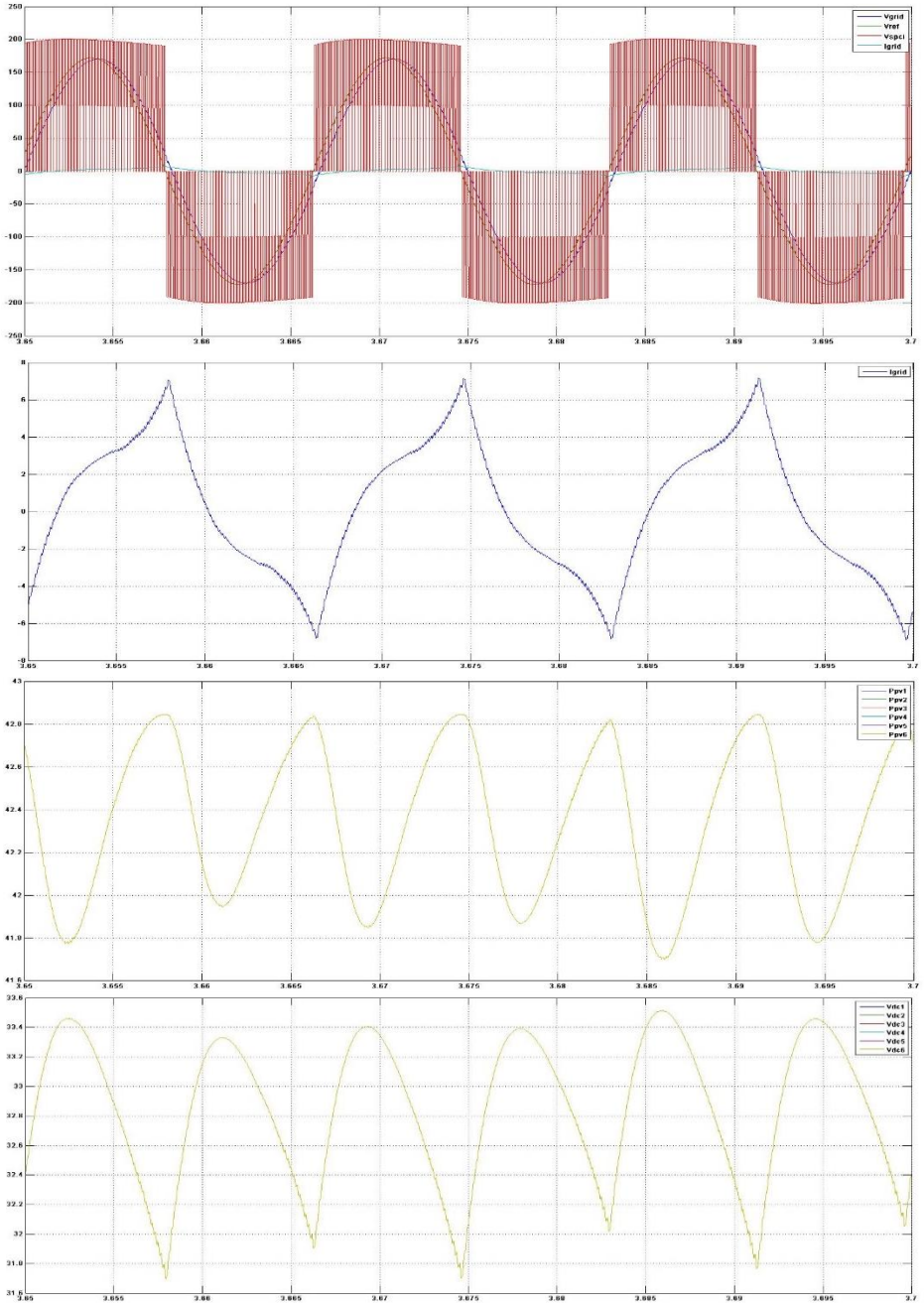


FIGURE 6.3: Unsorted pulse width modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0, mean irradiance = 200) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.3: Simulation results for Unsorted Pulse Width Modulation with coefficient of variation, $\gamma = 0.2$ and mean irradiance, $\mu = 600$.

Reference current (A)	Available power (W)	Extracted Power (W)	%Yield (Y)
5.66	847	595	70.25

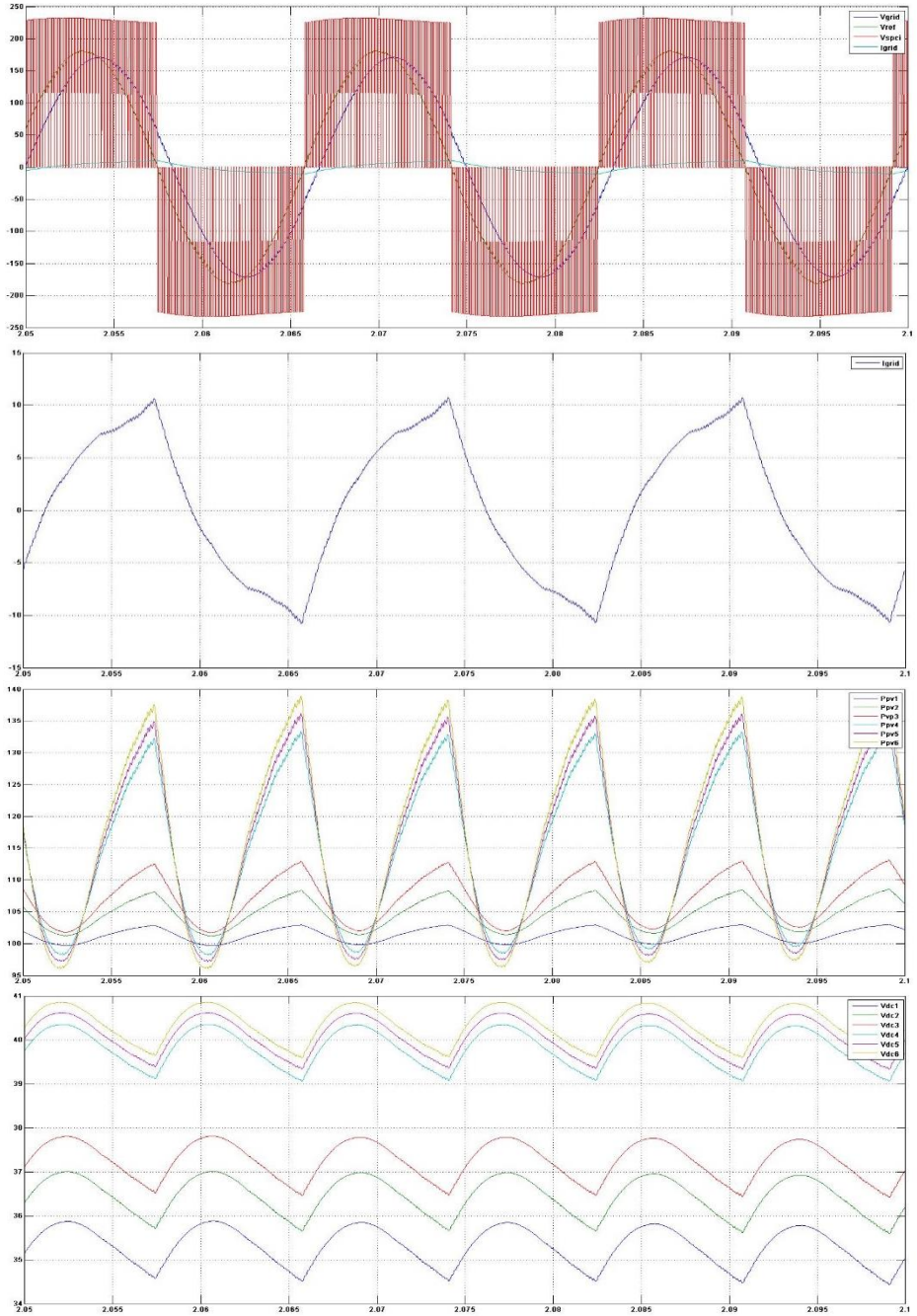


FIGURE 6.4: Unsorted pulse width modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0.2, mean irradiance = 600) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.4: Simulation results for Unsorted Pulse Width Modulation with coefficient of variation, $\gamma = 0.4$ and mean irradiance, $\mu = 1000$.

Reference current (A)	Available power (W)	Extracted Power (W)	%Yield (Y)
7	1476.51	818.6	55.44

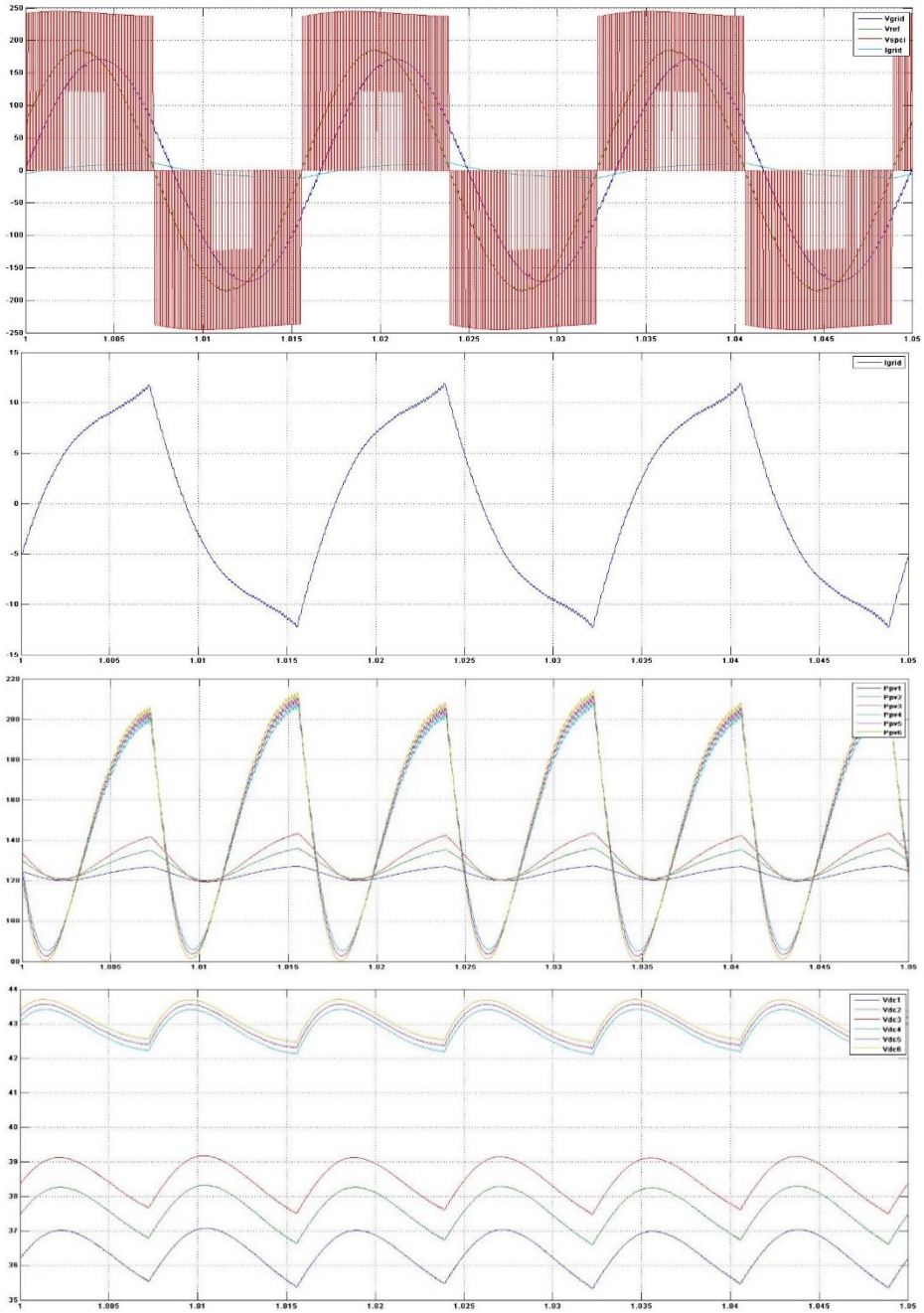


FIGURE 6.5: Unsorted pulse width modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0.4, mean irradiance = 1000) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.5: Simulation results for Sorted Stair Case Modulation with coefficient of variation, $\gamma = 0$ and mean irradiance, $\mu = 200$.

Reference current (A)	Available power (W)	Extracted Power (W)	%Yield (Y)
2.99	257.10	246	95.68

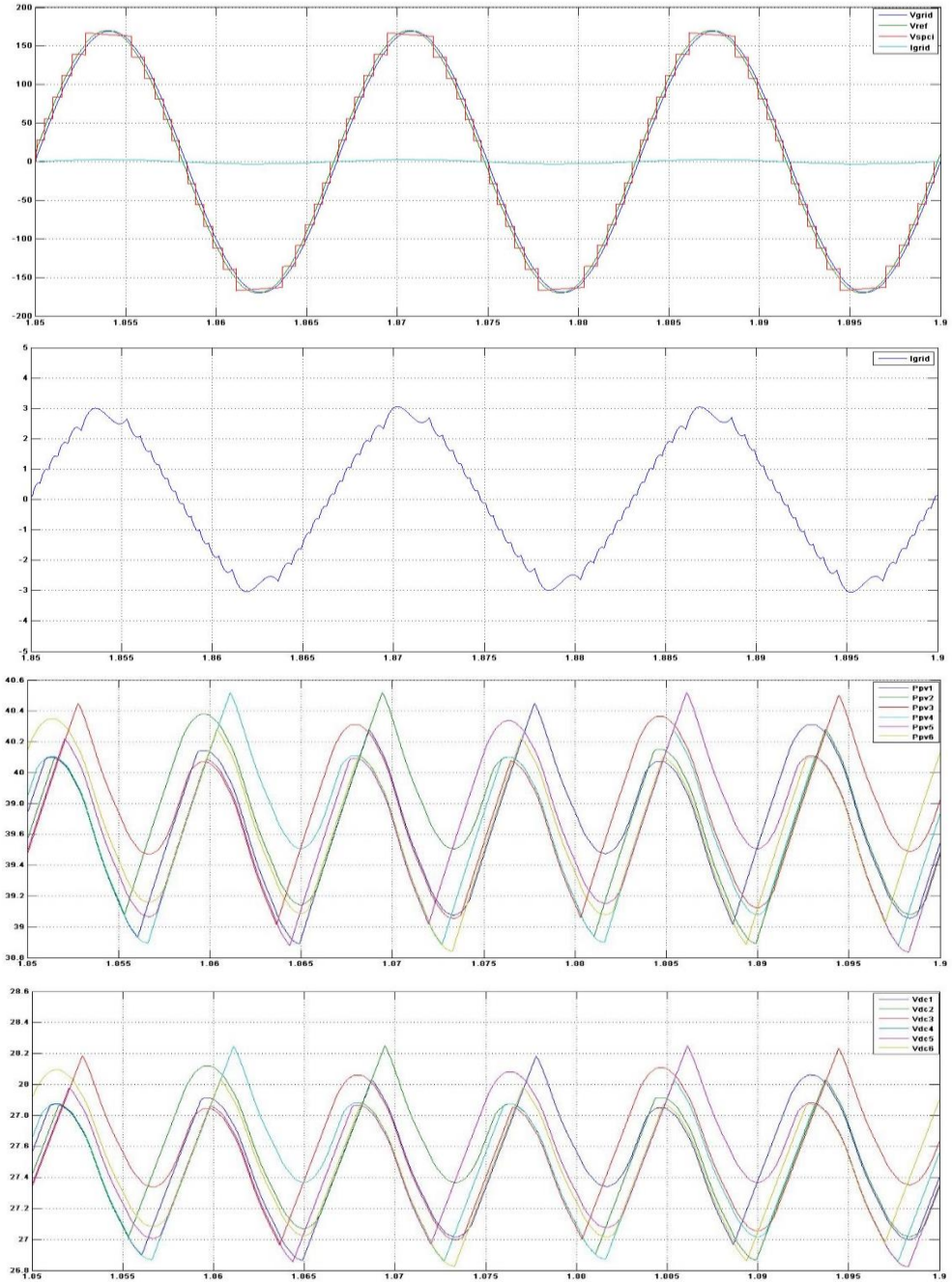


FIGURE 6.6: Sorted stair case modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0, mean irradiance = 200) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.6: Simulation results for Sorted Stair Case Modulation with coefficient of variation, $\gamma = 0.2$ and mean irradiance, $\mu = 600$.

Reference current (A)	Available power (W)	Extracted Power (W)	%Yield (Y)
9.375	847	838.2	98.96

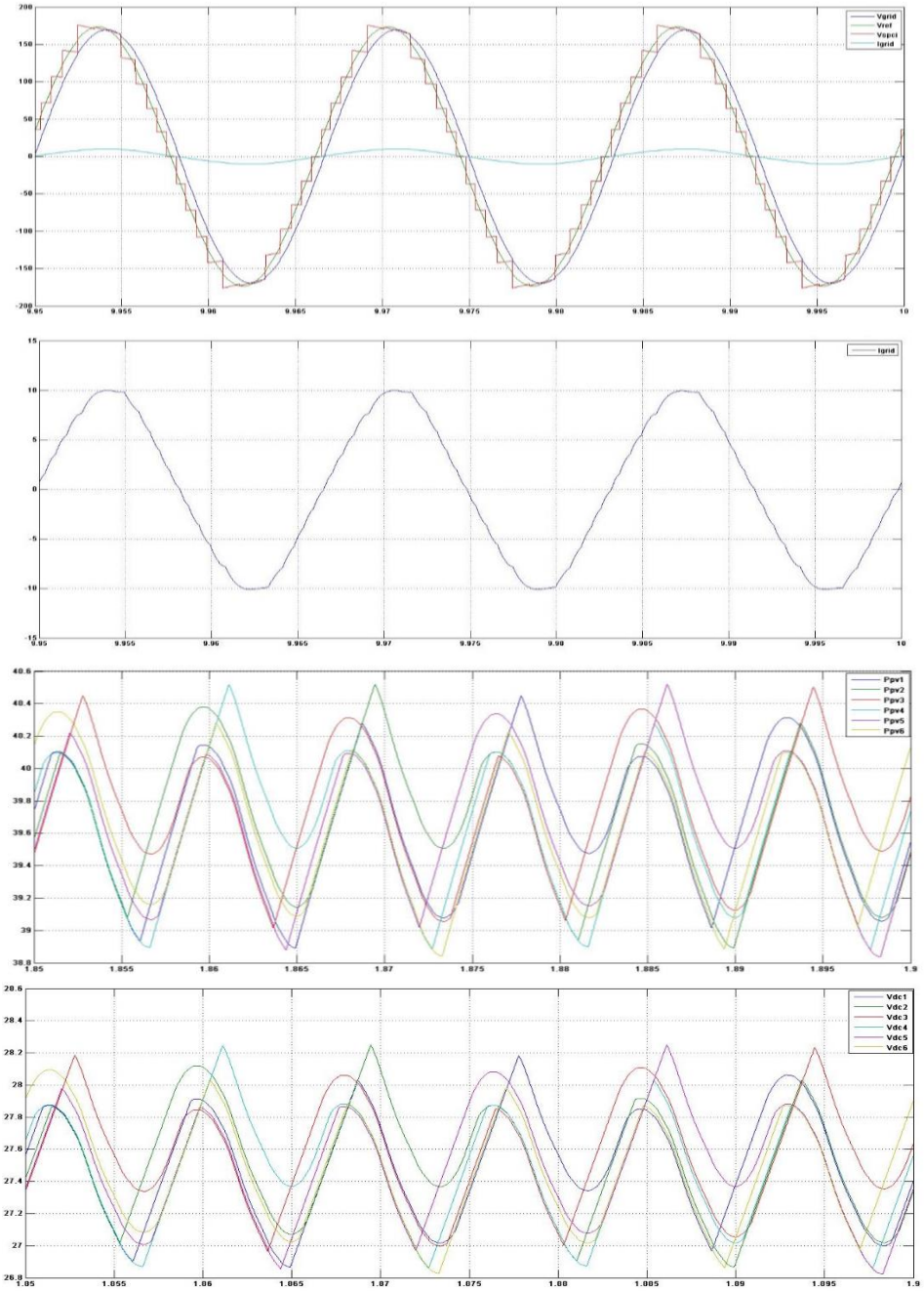


FIGURE 6.7: Sorted stair case modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0.2, mean irradiance = 600) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.7: Simulation results for Sorted Stair Case Modulation with coefficient of variation, $\gamma = 0.4$ and mean irradiance, $\mu = 1000$.

Reference current (A)	Available power (W)	Extracted Power (W)	%Yield (Y)
14.18	1476.51	1167	79.04

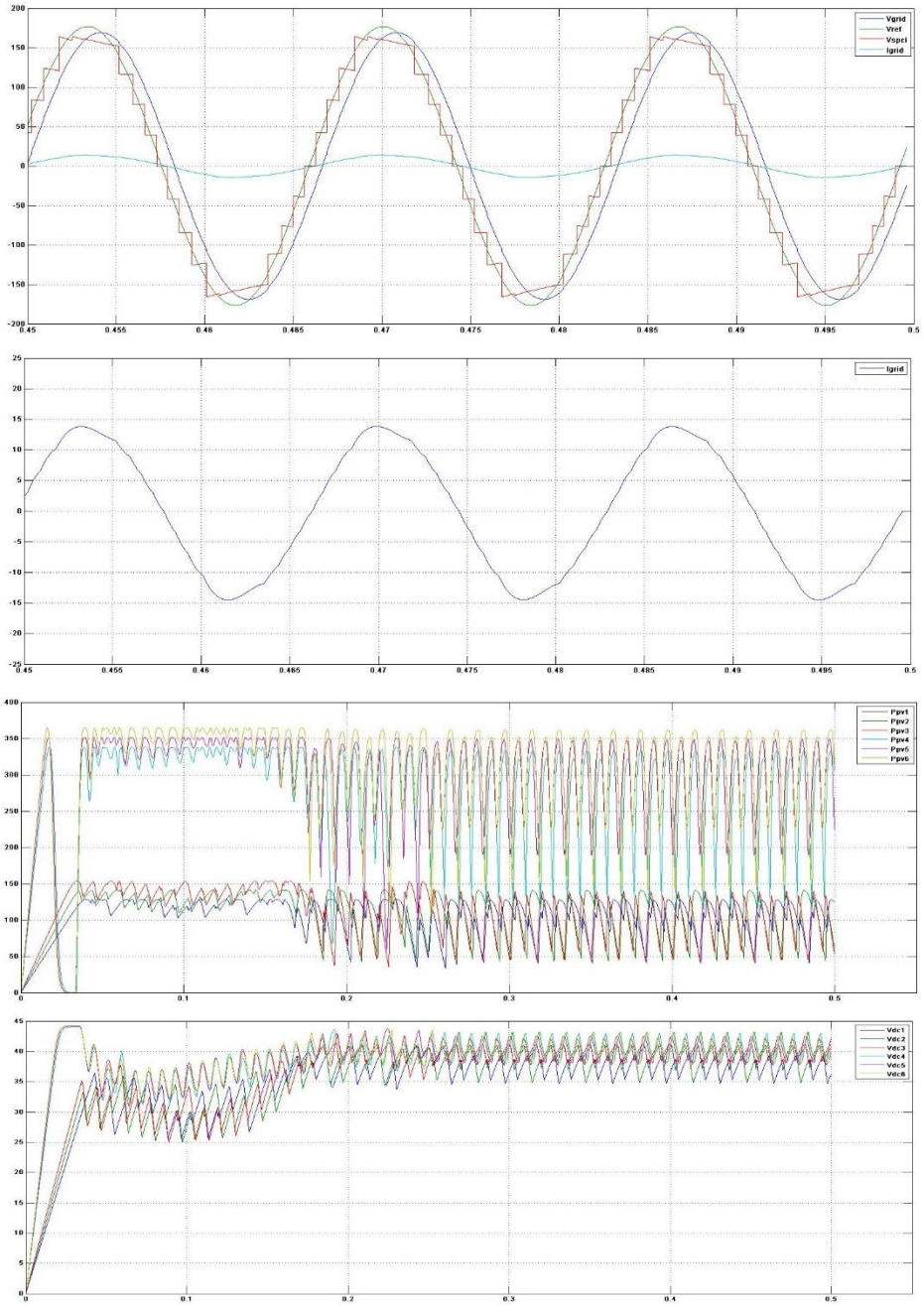


FIGURE 6.8: Sorted stair case modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0.4, mean irradiance = 1000) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.8: Simulation results for Sorted Pulse Width Modulation with coefficient of variation, $\gamma = 0$ and mean irradiance, $\mu = 200$.

Reference current (A)	Available power (W)	Extracted Power (W)	%Yield (Y)
3.226	257.10	244	94.90

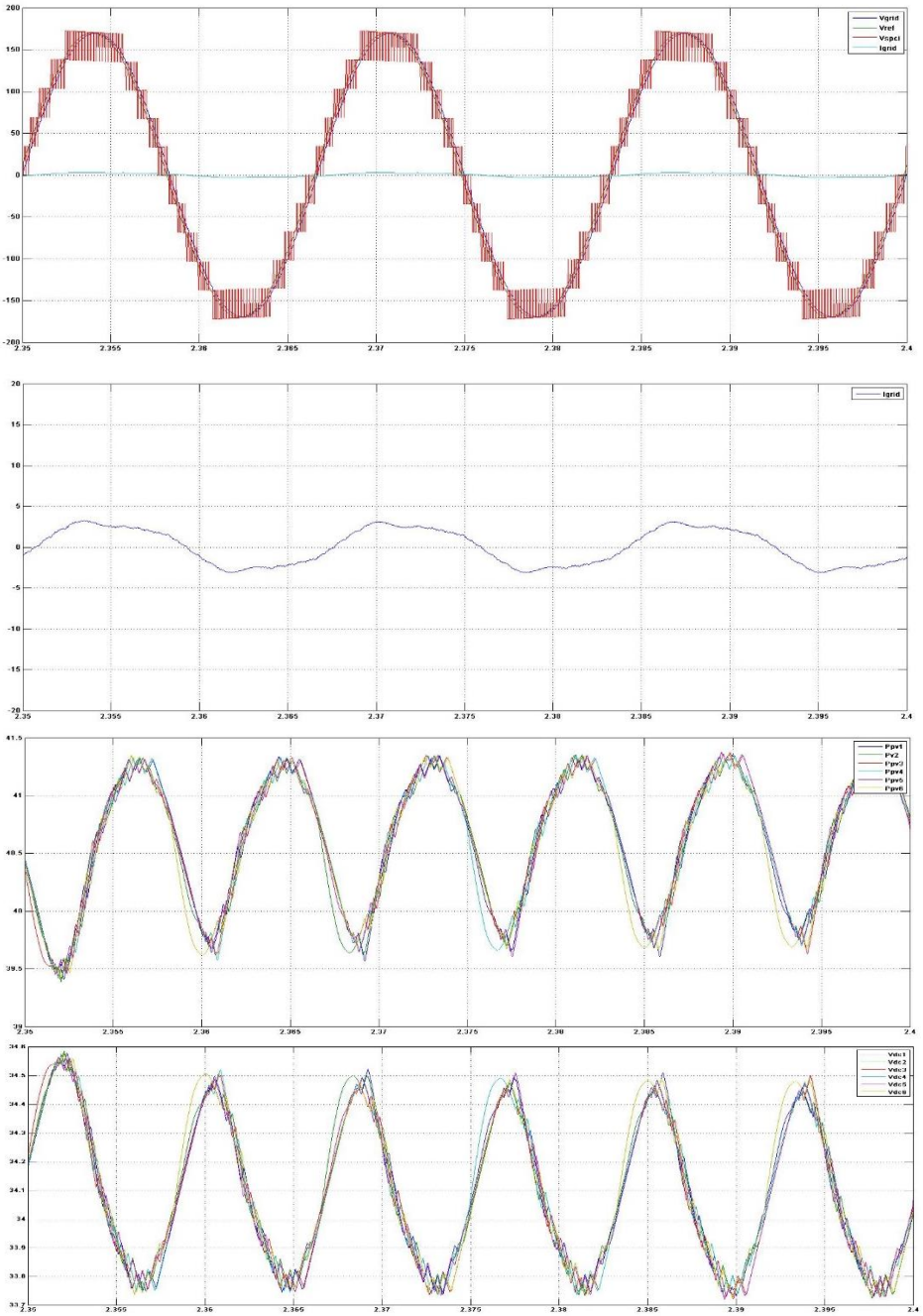


FIGURE 6.9: Sorted pulse width modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0.0, mean irradiance = 200) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.9: Simulation results for Sorted Pulse Width Modulation with coefficient of variation, $\gamma = 0.2$ and mean irradiance, $\mu = 600$.

Reference current (A)	Available power (W)	Output Power (W)	%Yield (Y)
9.64	847	809.2	95.54

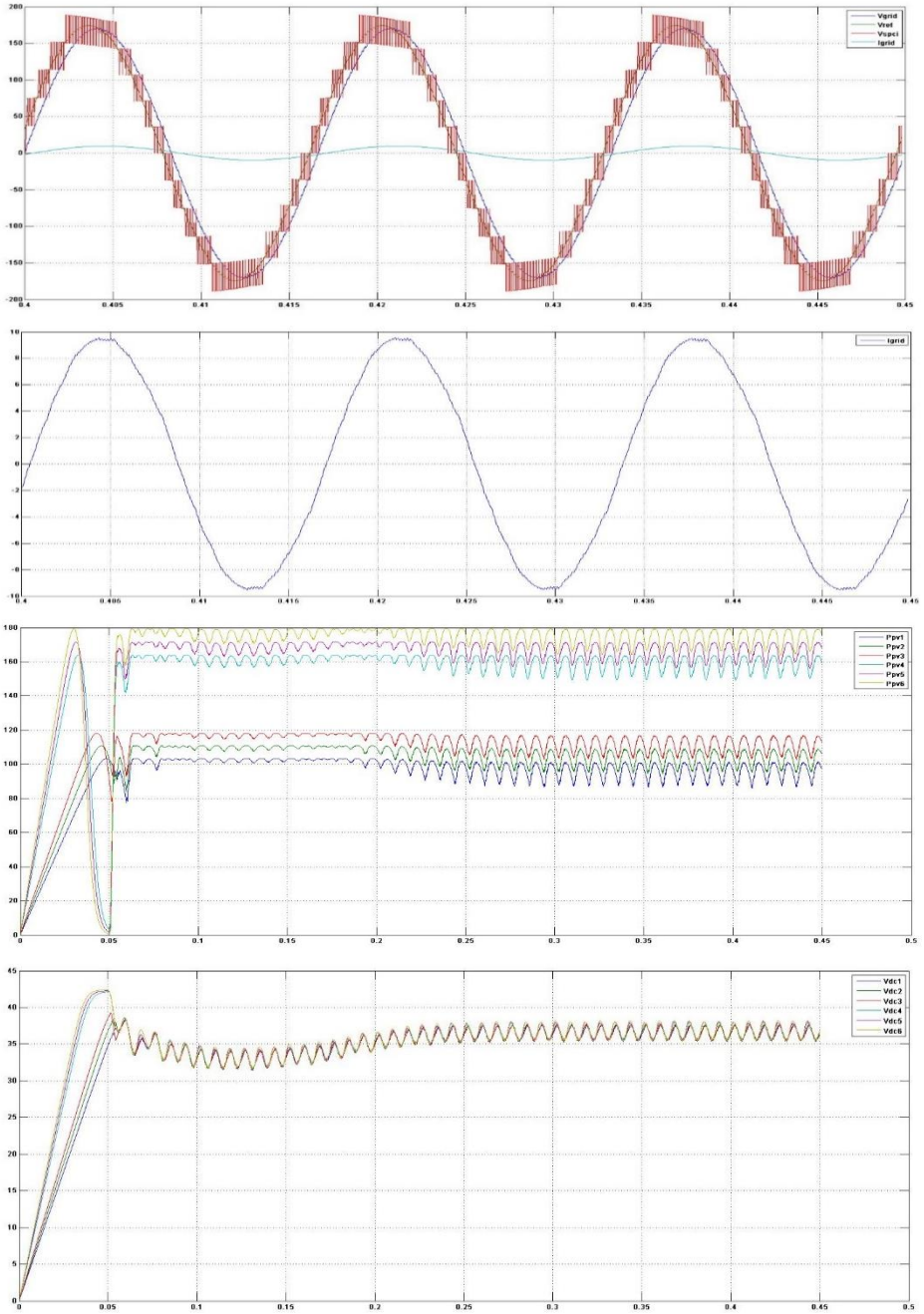


FIGURE 6.10: Sorted pulse width modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0.2, mean irradiance = 400) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.10: Simulation results for Sorted Pulse Width Modulation with coefficient of variation, $\gamma = 0.4$ and mean irradiance, $\mu = 1000$.

Reference current (A)	Available power (W)	Extracted Power (W)	%Yield (Y)
13.50	1476.51	1206	81.68

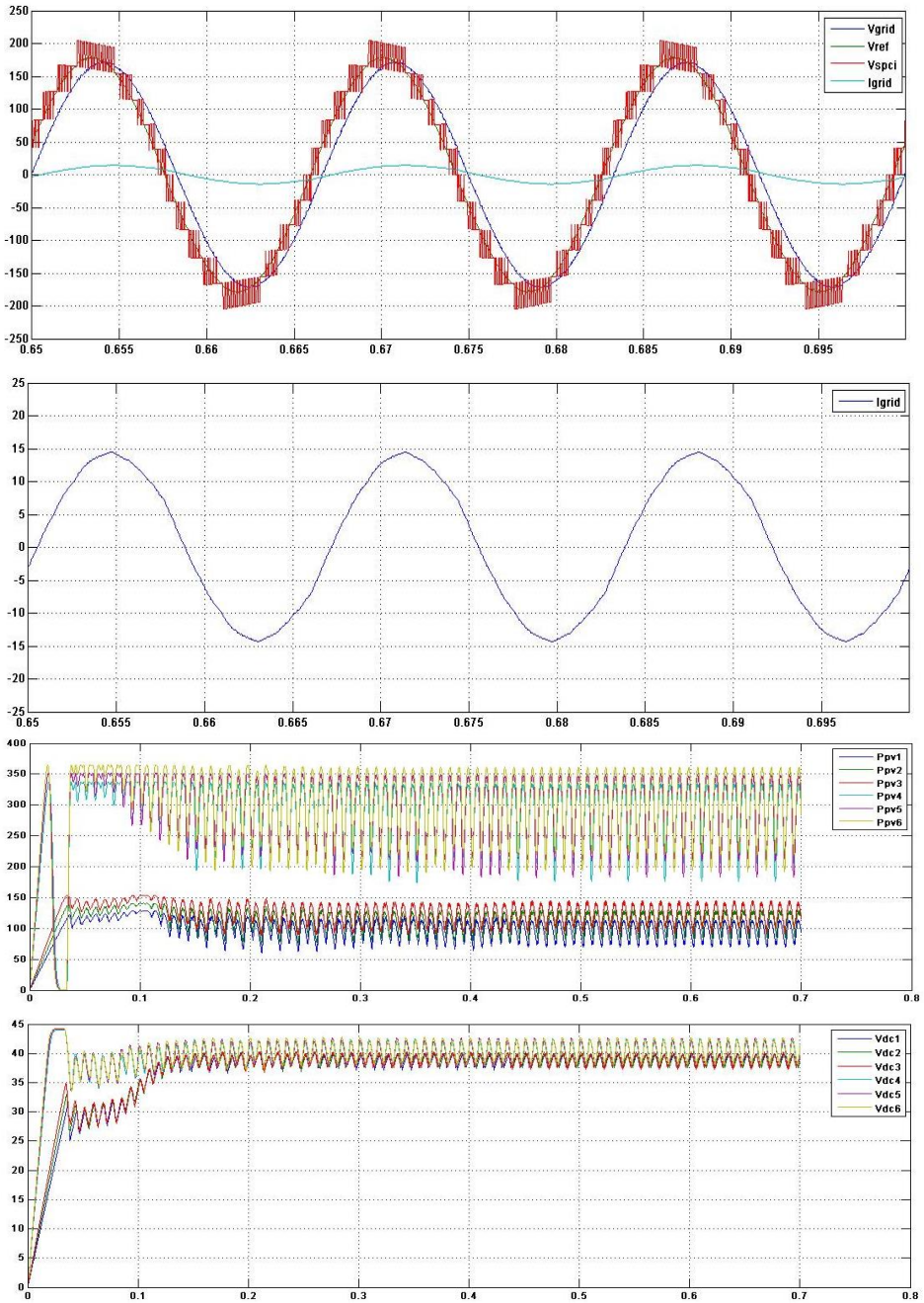


FIGURE 6.11: Sorted pulse width modulation strategy simulation waveforms (for operating scenario having coefficient of variation = 0.4, mean irradiance = 1000) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.

TABLE 6.11: Consolidated simulation results for operating scenarios:
($\gamma = 0$, $\mu = 200$), ($\gamma = 0.2$, $\mu = 600$), and ($\gamma = 0.4$, $\mu = 1000$)

Control Strategy	Percentage yield = (Total dc output power/ Total available dc power)*100		
	$\gamma = 0$, $\mu = 200$	$\gamma = 0.2$, $\mu = 600$	$\gamma = 0.4$, $\mu = 1000$
Unsorted Pulse Width Modulation (UPWM)	100	95.68	94.90
Sorted Stair Case Modulation (SSCM)	81.56	98.96	95.54
Sorted Pulse Width Modulation (SPWM)	60.34	79.04	81.68

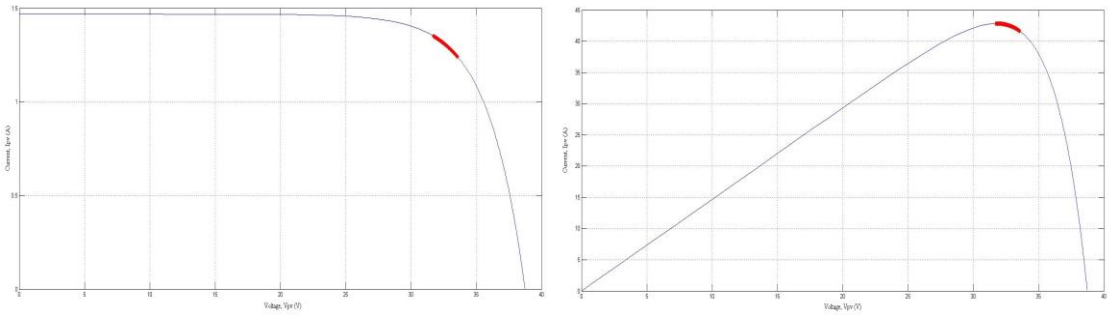


FIGURE 6.12: I – V, and P – V graphs for operating scenario ($\gamma = 0$, $\mu = 200$), showing each solar panel operating region at maximum power point, with unsorted pulse width modulation.

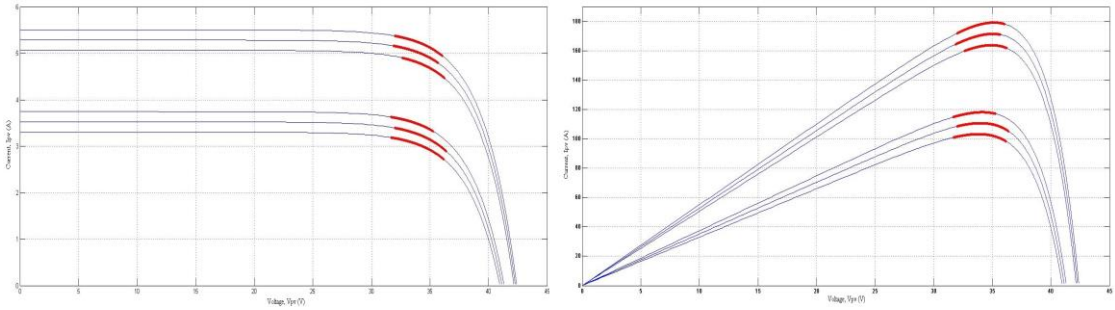


FIGURE 6.13: I – V, and P – V graphs for operating scenario ($\gamma = 0.2$, $\mu = 600$), showing each solar panel operating region at maximum power point, with sorted stair case modulation.

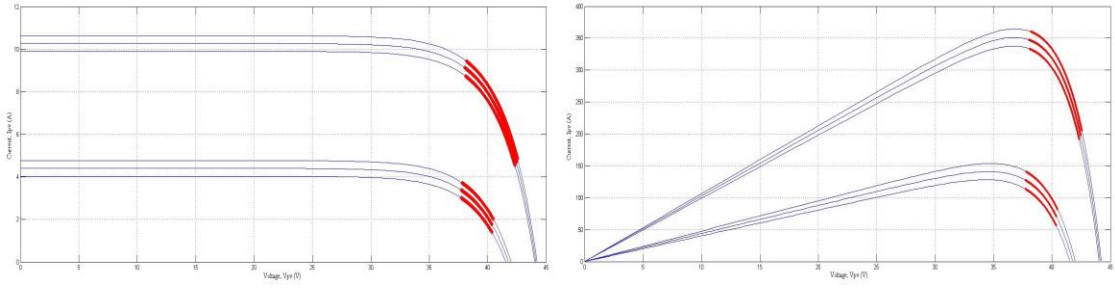


FIGURE 6.14: I – V, and P – V graphs for operating scenario ($\gamma = 0.4$, $\mu = 1000$), showing each solar panel operating region at maximum power point, with sorted pulse width modulation.

CHAPTER 7 : COMPARATIVE ANALYSIS OF CONTROL STRATEGIES AND MASTER SELECTOR

7.1. Introduction

In this chapter, a comparative analysis of the control strategies for Solar Panel Companion Inverter, namely Unsorted Pulse Width Modulation, Sorted Stair Case Modulation, and Sorted Pulse Width Modulation is done for various operating scenarios. This analysis is performed to identify the optimal control strategy for a given operating scenario. Operating space of Solar Panel Companion Inverter (SPCI) is described in Section 7.2. Comparative analysis of the control strategies is explained in Section 7.3. Advantage of SPCI as compared to existing solar power converters as reviewed in Chapter 2 are explained in Section 7.4. Implementation of control strategy selection is presented in Section 7.5, and its simulation results are presented in Section 7.6.

7.2. Operating Space

In this section, operating space of Solar Panel Companion Inverter (SPCI) is explained. Operating space is the range of operating scenarios of SPCI i.e., range of pairs of coefficient of variation, γ, and mean irradiance, μ, for which the comparative analysis is performed. Since $1000W/m^2$ is the irradiance value at Standard Test Conditions (STC) [20], $1000W/m^2$ is considered to be the upper limit of μ. $\mu = 200W/m^2$ is considered to be the lower limit. For selecting the range of γ, the power mismatch and difference in the current contribution of the solar panels at maximum power point is taken into consideration. To decide on the range of γ, six operating scenarios shown in Table 7.1 are

considered. From Figure 7.1 and Figure 7.2, which show the I – V curves for scenario 1 and scenario 2 respectively, it may be seen that the curves are spread in the plot not far away from each other. This indicates that the power mismatch between the solar panels is less significant for these two scenarios. The difference between the current contributions of solar panels at maximum power point as may be seen in Table 7.2 and Table 7.3, is also not significant. Hence, $\gamma = 0.1$ is included in the operating space. Figure 7.3 and Figure 7.4 shows the I – V curves for scenario 3 and scenario 4 respectively, wherein the I – V curves are spread in a plot, at significant distance. Table 7.4 shows the operating points of the solar panel for scenario 3, where the current contribution for the panel with highest solar irradiance is 2.09 A, whereas that of the panel with lowest solar irradiance contributes 0.6 A, which is a significant difference. Same is the case with scenario 4, which may be seen in Table 7.5, where panel with highest irradiance contributes 10.58 A and the one with lowest irradiance contributes 3.05 A. Also, such high disparity in irradiance values is uncommon. Hence, $\gamma = 0.5$ is not considered in the operating space. Figure 7.5 and Figure 7.6 shows the I – V curves for scenario 5 and scenario 6 respectively. In these two scenarios, the I – V curves are spread over a very wide area and hence power mismatch is very high in this case. In Table 7.6, it may be seen that the current contribution by highest and lowest irradiance solar panels are 2.64 A and 0.07 A respectively. The difference between the current contributions between the two panels is very high. Same is the case with operating scenario 7, as may be seen in Table 7.7. The current contribution by the panel having highest solar irradiance is 13.38 A whereas that of the lowest solar irradiance is 0.33 A. The difference in current contribution is very high. Hence, $\gamma = 0.9$ is also not

considered in the operating space. Therefore, the operating space is limited to $0 \leq \gamma \leq 0.4$ and $0 \leq \mu \leq 1000$ W/m^2.

7.3. Comparative Evaluation of Control Strategies

Figure 7.7 shows the comparative analysis of simulation results for Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM) strategies. Percentage yields are determined for various operating scenarios ("coefficient of variation – mean irradiance" pairs), and 3D surface plots are plotted in excel, with mean irradiance, μ along x – axis, coefficient of variation, γ along z – axis and percentage yield along y – axis. It may be seen that for UPWM, the percentage yield is 100% for uniform irradiance, i.e. when $\gamma = 0$. The cells are highlighted in green to show that UPWM offers the maximum yield for uniform irradiance. As γ increases from 0 to 0.4, the yield in case of UPWM falls by about 10% for an increase in γ by a step of 0.1. SSCM control strategy offers maximum yield for the operating scenarios: $\gamma = 0.1$ and $\mu = 200$, $\gamma = 0.3$ and $\mu = 200$, $\gamma = 0.4$ and $\mu = 200$, $\gamma = 0.1$ and $\mu = 600$, $\gamma = 0.2$ and $\mu = 600$, and, $\gamma = 0.3$ and $\mu = 600$ and the cells are highlighted in green. SPWM control strategy offers maximum yield for the operating scenarios: $\gamma = 0.2$ and $\mu = 200$, $\gamma = 0.4$ and $\mu = 600$, $\gamma = 0.1$ and $\mu = 1000$, $\gamma = 0.2$ and $\mu = 1000$, $\gamma = 0.3$ and $\mu = 1000$, and, $\gamma = 0.4$ and $\mu = 1000$ and the cells are highlighted in green.

7.4. Advantage of Solar Panel Companion Inverter

Table 7.8 shows the control strategies which offers the best yield of energy for various operating scenarios. The mean irradiance (μ) represents the available solar power. This available power increases with the irradiance. Therefore, $\mu = 1000$ corresponds to a high intensity of sunlight and hence more available power. Similarly, $\mu = 200$ corresponds

to less available power. Coefficient of variation (γ) represents the disparity in the irradiance distributed on all the solar panels. $\gamma = 0$ corresponds to a uniformly distributed irradiance on all the solar panels. It may be seen in Table 7.8 that irrespective of available power (whether more available power or less available power), if there is a uniform irradiance distribution, Unsorted Pulse Width Modulation (UPWM) gives the maximum energy yield. For a non – uniform irradiance distribution with less available power, Sorted Stair Case Modulation (SSCM) gives the maximum energy yield. And for a non – uniform irradiance distribution with more available power, Sorted Pulse Width Modulation (SPWM) gives the maximum energy yield. As discussed in Chapter 4, with a Solar Panel Companion Inverter (SPCI) UPWM, SSCM, and SPWM control strategies can be implemented. Since, only one of the control strategies yields the best for an operating scenario, SPCI offers the advantage of selecting one control strategy, to ensure that the yield is maximum. As discussed in Chapter 2, though central inverter topology cost is less, offers low yield for non – uniform irradiance conditions. Although string inverter offers a higher yield of energy compared to central inverters, it is still not the best, since there is no panel level maximum power point tracking. Micro inverter is the best in terms of the energy yield because of its ability to stay in the region of maximum power point at panel level, but the cost is high. SPCI can be an optimal solution for photovoltaic power conversion in terms of cost and yield, as it can give high yield under both uniform and non – uniform irradiance conditions, by using one of the three control strategies.

7.5. Master Selector

Master Selector is implemented for the selecting the control scheme which offers maximum yield for a given operating scenario. Figure 7.8 shows the flow chart

implementation of the logic for master selector. The master selection cycle starts by verifying whether the irradiance distribution over all the solar panels is uniform or non – uniform. Such an action is performed by measuring the dc bus voltages across all the panels and verifying whether they are equal. If the dc bus voltages across all panels is same, then Unsorted Pulse Width Modulation (UPWM) strategy is implemented, until there is a change in operating scenario, since it offers maximum yield for uniform irradiance distribution. If there is a change in operating scenario, then the master selection cycle repeats by checking for the uniformity of irradiance distribution over the solar panels. If the dc bus voltages across all the panels are unequal, then Sorted Stair Case Modulation (SSCM) strategy is implemented for ten cycles. The total dc power output is measured after SSCM is implemented for first ten cycles, and it is stored in the memory as PSSCM. Thereafter, for next ten cycles Sorted Pulse Width Modulation (SPWM) strategy is implemented. The total dc power output is measured and stored in the memory as PSPWM. At this instant, the total dc power output for SSCM, PSSCM is compared with that of the total dc power output for SPWM, PSPWM. If PSSCM is greater than PSPWM, then SSCM is implemented until there is a change in operating scenario. If there is a change in operating scenario, then the master selection cycle repeats by checking for the uniformity of irradiance distribution over the solar panels. If PSSCM is lesser than PSPWM, then SPWM is implemented until there is a change in operating scenario. If there is a change in operating scenario, then the master selection cycle repeats by checking for the uniformity of irradiance distribution over the solar panels.

7.6. Simulation Results

Simulations using master selector is performed for the operating scenarios discussed in Chapter 6. Figure 7.9 and Figure 7.10 shows the simulation results for scenario 1, i.e. coefficient of variation, $\gamma = 0$ and mean irradiance, $\mu = 200$, using master selector. Since the operating scenario corresponds to uniform irradiation, Unsorted Pulse Width Modulation (UPWM) is selected and implemented. Figure 7.9 shows the maximum power point operation on I – V and P – V characteristics, in red. Simulation is performed for scenario 2 i.e. coefficient of variation, $\gamma = 0.2$ and mean irradiance, $\mu = 600$, using master selector. Figure 7.11(a) shows the Sorted Stair Case Modulation (SSCM) strategy output waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for ten cycles are in a single plot. Figure 7.11(b) shows the Sorted Pulse Width Modulation (SPWM) strategy output waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for ten cycles are in a single plot. Figure 7.12 shows the operating region of the solar panels when SSCM is implemented in red color. The operating region of the solar panels when SPWM is implemented is shown in blue color. SSCM is selected by the master selector, since it offers the maximum yield. Figure 7.13 shows simulation waveforms after SSCM is selected by the master selector for the operating scenario 2. Simulation is performed for scenario 3 i.e. coefficient of variation, $\gamma = 0.4$ and mean irradiance, $\mu = 1000$, using master selector. Figure 7.14(a) shows the Sorted Stair Case Modulation (SSCM) strategy output waveforms of grid voltage, V_{grid}, reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for ten cycles are in a single plot. Figure 7.14(b) shows the Sorted Pulse Width Modulation (SPWM) strategy output waveforms of grid voltage, V_{grid},

reference voltage, V_{ref}, synthesized output ac voltage of SPCI, V_{spci}, grid current, I_{grid}, for ten cycles are in a single plot. Figure 7.15 shows the operating region of the solar panels when SSCM is implemented in red color. The operating region of the solar panels when SPWM is implemented is shown in blue color. SPWM is selected by the master selector, since it offers the maximum yield for operating scenario 3. Figure 7.16 shows simulation waveforms after SPWM is selected by the master selector for the operating scenario 3. All the simulation waveforms are identical to the waveforms obtained in Chapter 6.

TABLE 7.1: Operating scenarios considered to explain the operating space

Scenario #	Coefficient of variation (γ)	Mean irradiance (μ)
1	0.1	200
2	0.1	1000
3	0.5	200
4	0.5	1000
5	0.9	200
6	0.9	1000

TABLE 7.2: Operating points of the Solar Panels for scenario 1, mean irradiance = 200 and coefficient of variation = 0.1

	Irradiance	Vmpp(V)	Impp(A)	Pmpp(W)
	170	31.31	1.15	35.90
	180	31.46	1.21	38.20
	200	31.73	1.35	42.85
	205	31.82	1.38	44.01
	215	313.93	1.45	46.35
	230	32.13	1.55	49.88
Mean Irradiance (μ)	200	Ptotal (W)		257.20
Coefficient of Variation(γ)	0.1			

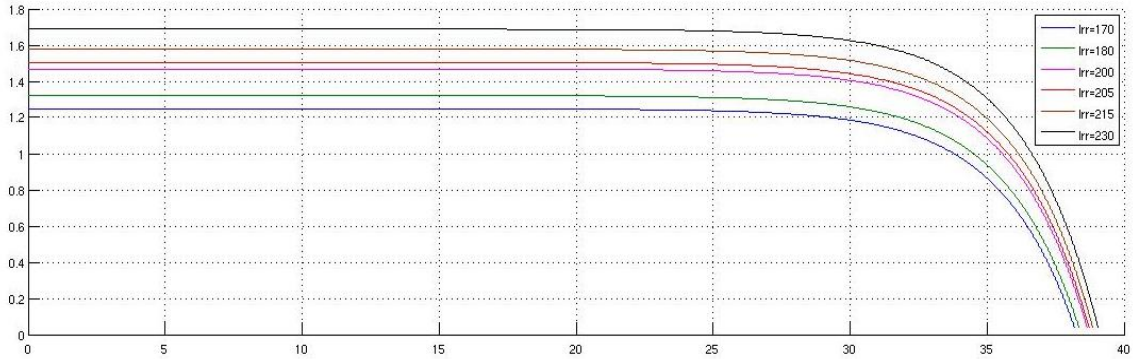


FIGURE 7.1: I – V curves of solar panels for mean irradiance = 200 and coefficient of variation = 0.1.

TABLE 7.3: Operating points of the Solar Panels for scenario 1, mean irradiance = 1000 and coefficient of variation = 0.1

	Irradiance	Vmpp(V)	Impp(A)	Pmpp(W)
	850	35.38	5.8	205.23
	900	35.38	6.13	218.28
	1000	35.99	6.79	244.51
	1025	35.78	7.02	251.08
	1075	35.99	7.34	264.33
	1150	36.16	7.86	284.23
Mean Irradiance (μ)	1000	Ptotal (W)		1467.70
Coefficient of Variation(γ)	0.1			

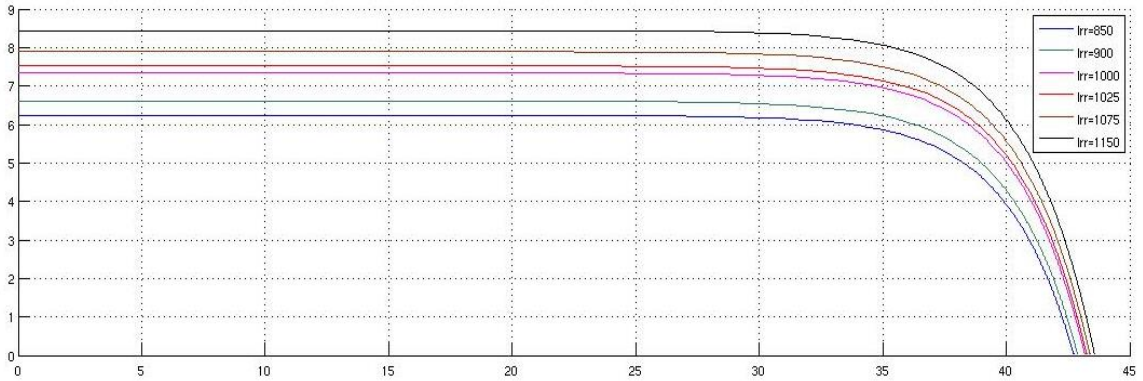


FIGURE 7.2: I – V curves of solar panels for mean irradiance = 1000 and coefficient of variation = 0.1.

TABLE 7.4: Operating points of the Solar Panels for scenario 3, mean irradiance = 200 and coefficient of variation = 0.5

	Irradiance	Vmpp(V)	Impp(A)	Pmpp(W)
	90	29.68	0.6	17.94
	100	29.96	0.6	20.13
	110	30.19	0.74	22.34
	290	32.73	1.96	64.15
	300	32.73	2.03	66.55
	310	32.9	2.09	68.96
Mean Irradiance (μ)	200	Ptotal (W)		260.06
Coefficient of Variation(γ)	0.5			

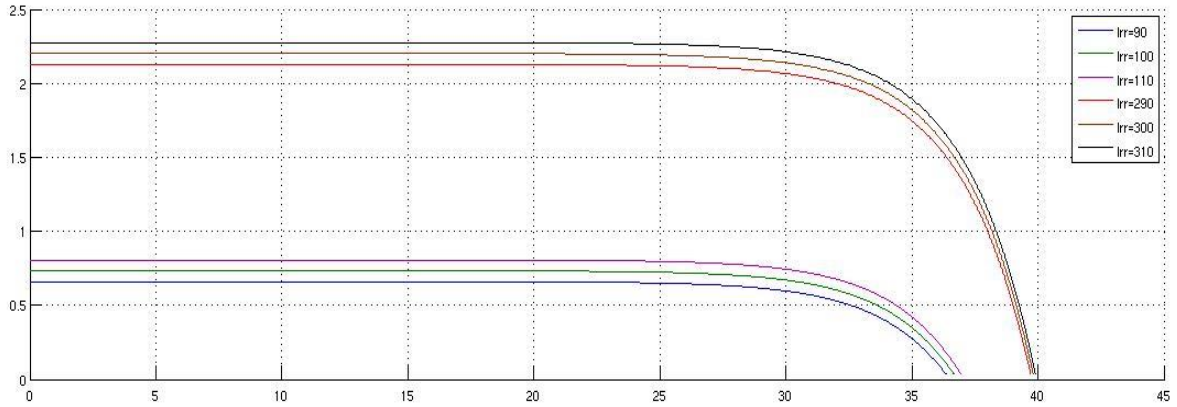


FIGURE 7.3: I – V curves of solar panels for mean irradiance = 200 and coefficient of variation = 0.5.

TABLE 7.5: Operating points of the Solar Panels for scenario 4, mean irradiance = 1000 and coefficient of variation = 0.5

	Irradiance	Vmpp(V)	Impp(A)	Pmpp(W)
	450	33.86	3.05	103.26
	500	34.01	3.40	115.72
	550	.34.35	3.73	128.28
	1450	36.74	9.93	364.73
	1500	36.9	10.25	378.30
	1550	37.03	10.58	391.86
Mean Irradiance (μ)	1000	Ptotal (W)		1482.20
Coefficient of Variation(γ)	0.5			

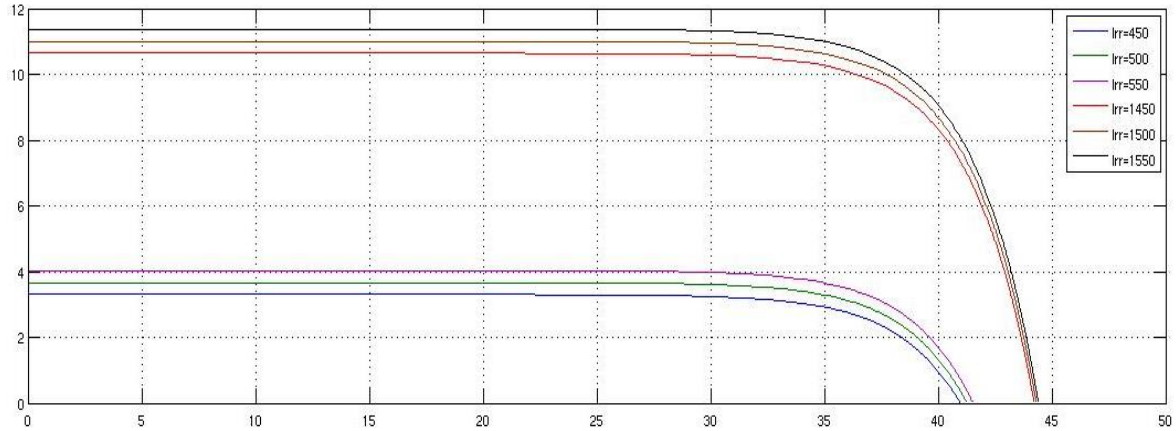


FIGURE 7.4: I – V curves of solar panels for mean irradiance = 1000 and coefficient of variation = 0.5.

TABLE 7.6: Operating points of the Solar Panels for scenario 5, mean irradiance = 200 and coefficient of variation = 0.9

	Irradiance	Vmpp(V)	Impp(A)	Pmpp(W)
	10	24.12	0.007	1.59
	20	25.87	0.13	3.43
	30	26.89	0.2	5.37
	370	33.33	2.51	83.54
	380	33.43	2.57	85.99
	390	33.51	2.64	88.44
Mean Irradiance (μ)	200	Ptotal (W)		268.35
Coefficient of Variation(γ)	0.9			

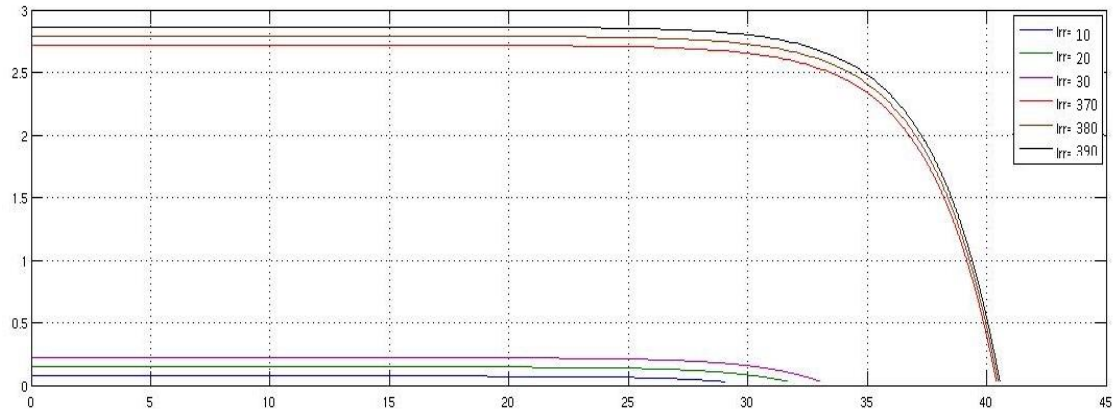


FIGURE 7.5: I – V curves of solar panels for mean irradiance = 200 and coefficient of variation = 0.9.

TABLE 7.7: Operating points of the Solar Panels for scenario 6, mean irradiance = 1000 and coefficient of variation = 0.9

	Irradiance	Vmpp(V)	Impp(A)	Pmpp(W)
	50	2802	0.33	9.42
	100	29.96	0.67	20.13
	150	31.01	1.01	31.33
	1850	37.7	12.57	473.8
	1900	37.61	12.97	487.69
	1950	37.47	13.38	501.43
Mean Irradiance (μ)	1000	Ptotal (W)		1523.8
Coefficient of Variation(γ)	0.9			

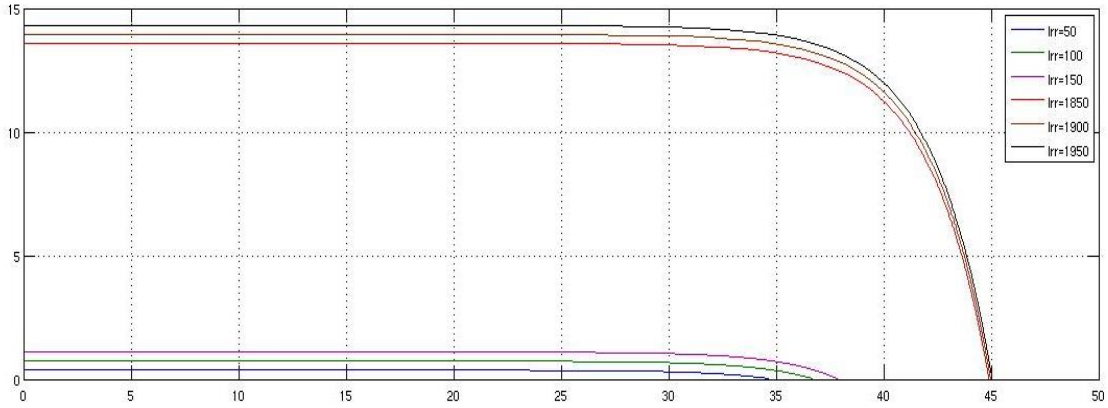


FIGURE 7.6: I – V curves of solar panels for mean irradiance = 1000 and coefficient of variation = 0.9.

Unsorted Pulse Width Modulation (Analytical)			
Mean (μ) / Coefficient of Variation (γ)	200	600	1000
0	100.00%	100.00%	100.00%
0.1	91.38%	91.37%	91.49%
0.2	81.56%	81.35%	81.44%
0.3	71.16%	70.92%	70.88%
0.4	60.34%	60.07%	60.15%

Sorted Stair Case Modulation			
Mean (μ) / Coefficient of Variation (γ)	200	600	1000
0	95.68%	87.06%	78.19%
0.1	92.61%	98.59%	79.04%
0.2	94.42%	98.96%	78.40%
0.3	89.10%	97.03%	80.70%
0.4	80.90%	70.19%	79.04%

Sorted Pulse Width Modulation			
Mean (μ) / Coefficient of Variation (γ)	200	600	1000
0	94.90%	93.63%	90.39%
0.1	89.04%	95.01%	82.17%
0.2	96.13%	95.54%	89.22%
0.3	83.58%	93.47%	89.82%
0.4	78.66%	93.00%	81.68%

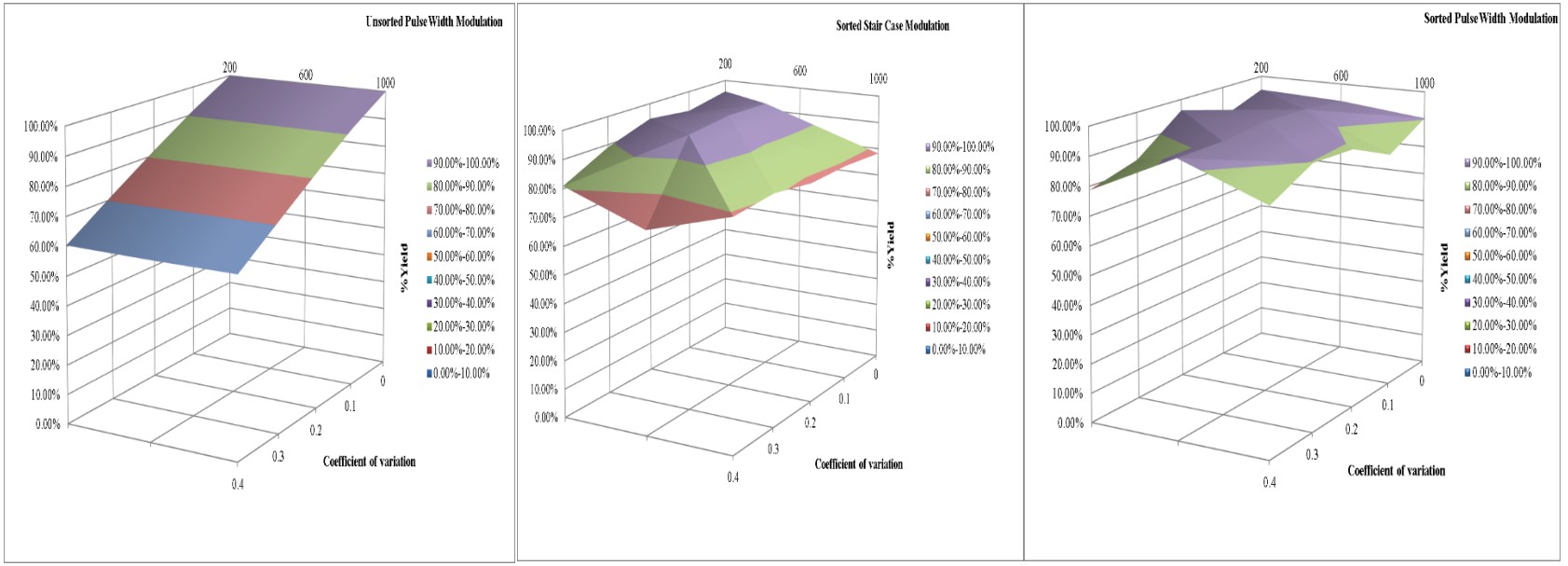


FIGURE 7.7: 3D surface plot showing mean irradiance along x – axis, percentage yield along y – axis, coefficient of variation along z – axis.

Table 7.8: Consolidated simulation results showing control strategy suitable for a given operating scenario, so as to offer maximum yield

Mean (μ) / Coefficient of Variation (γ)	200	600	1000
0	100%	100%	100%
0.1	92.61%	98.59%	82.17%
0.2	96.13%	98.96%	89.22%
0.3	89.10%	97.03%	89.82%
0.4	80.90%	93.00%	81.68%

UPWM
SSCM
SPWM

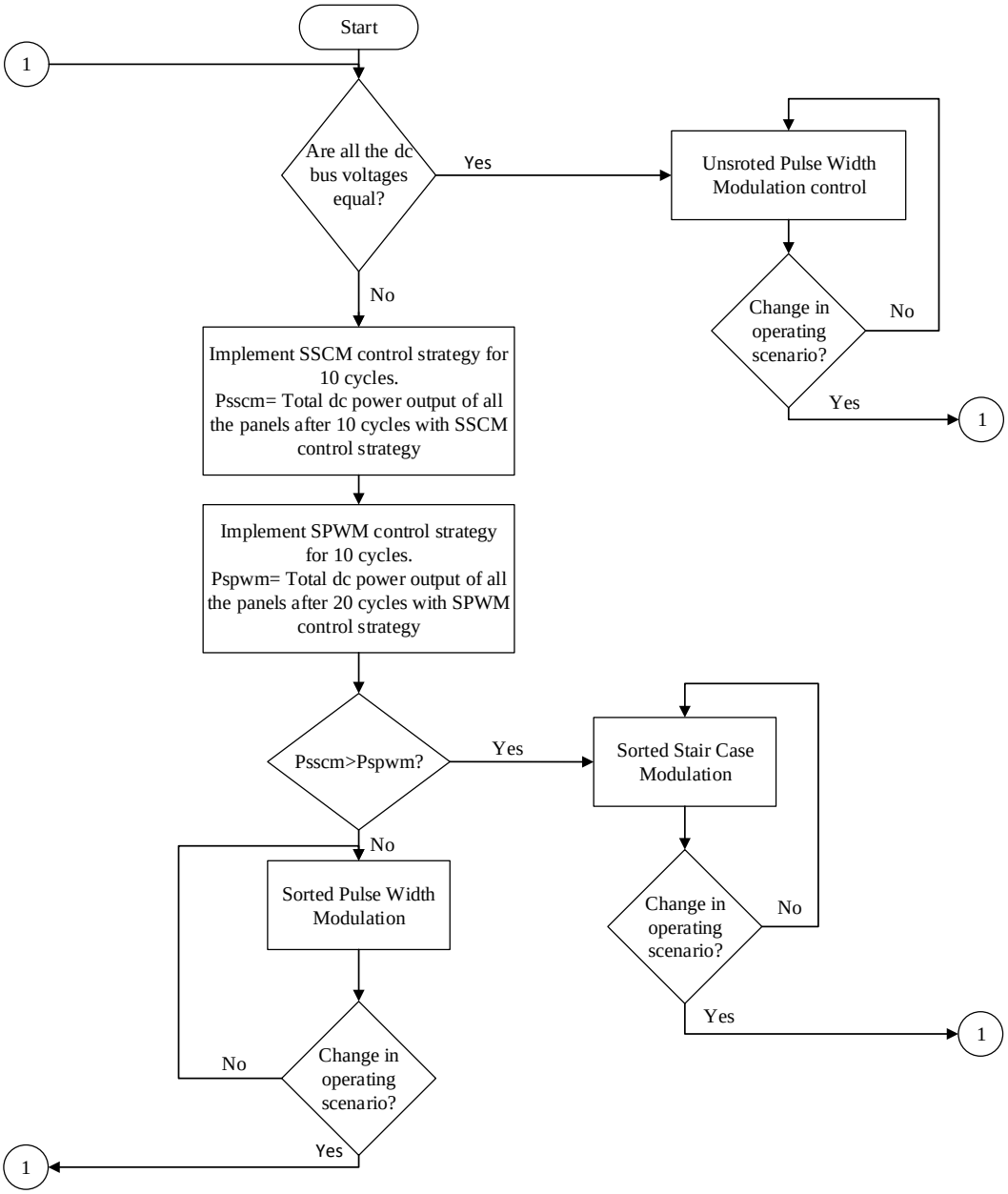


FIGURE 7.8: Flow Chart showing the implementation of master selector logic.

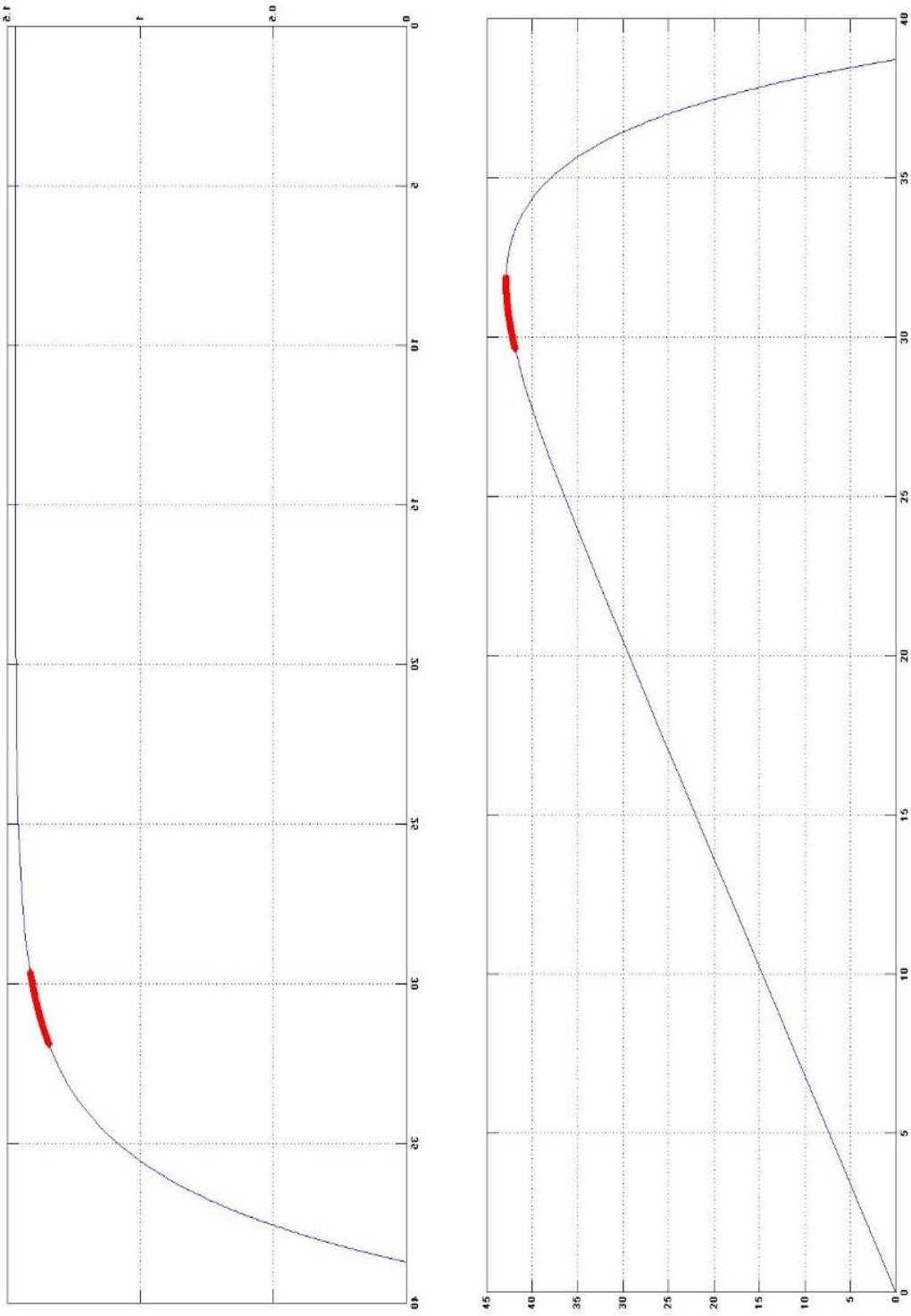


FIGURE 7.9: I – V, and P – V graphs for operating scenario ($\gamma = 0$, $\mu = 200$), showing each solar panel operating region at maximum power point, with unsorted pulse width modulation strategy selected using master selector.

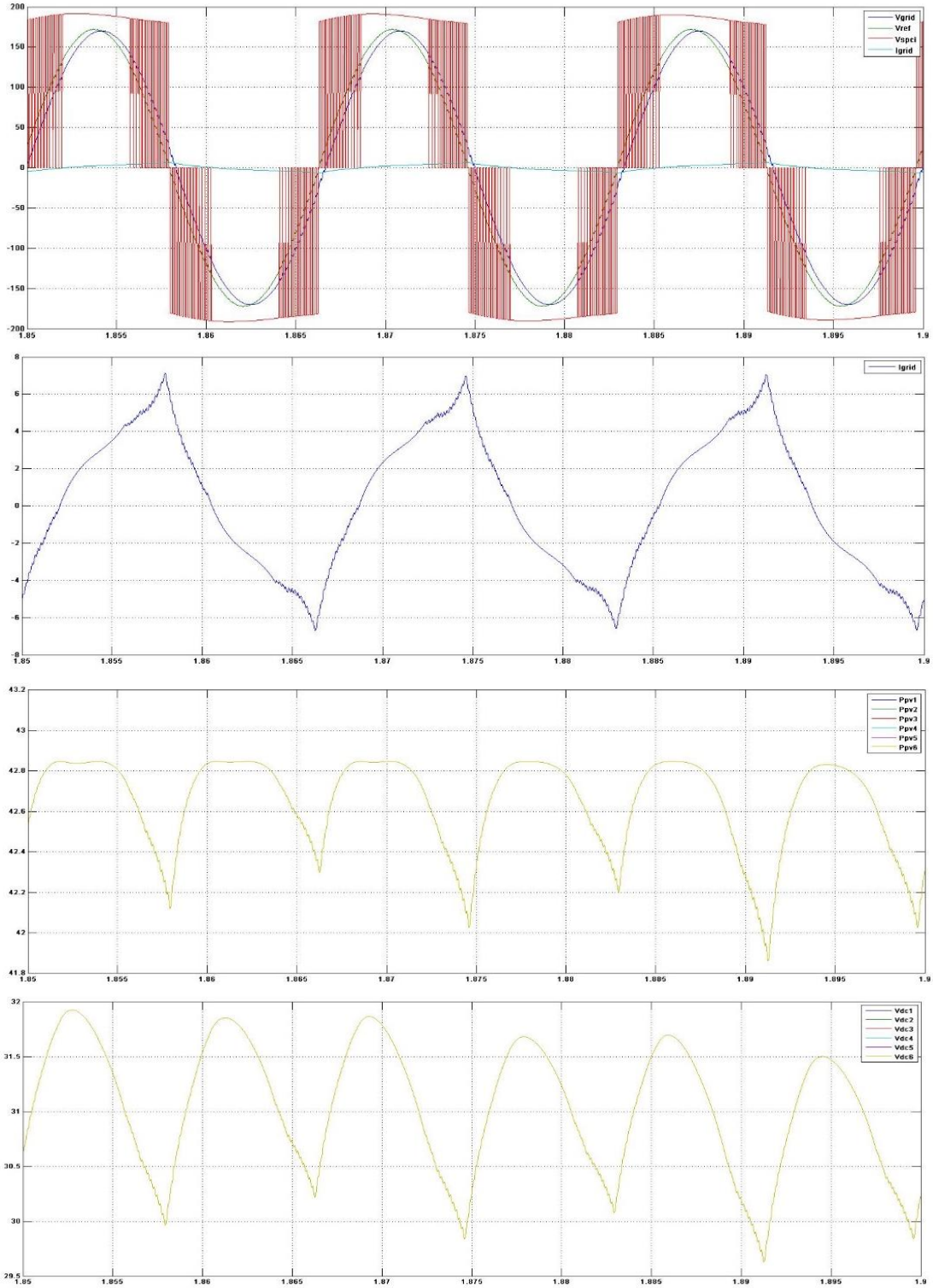
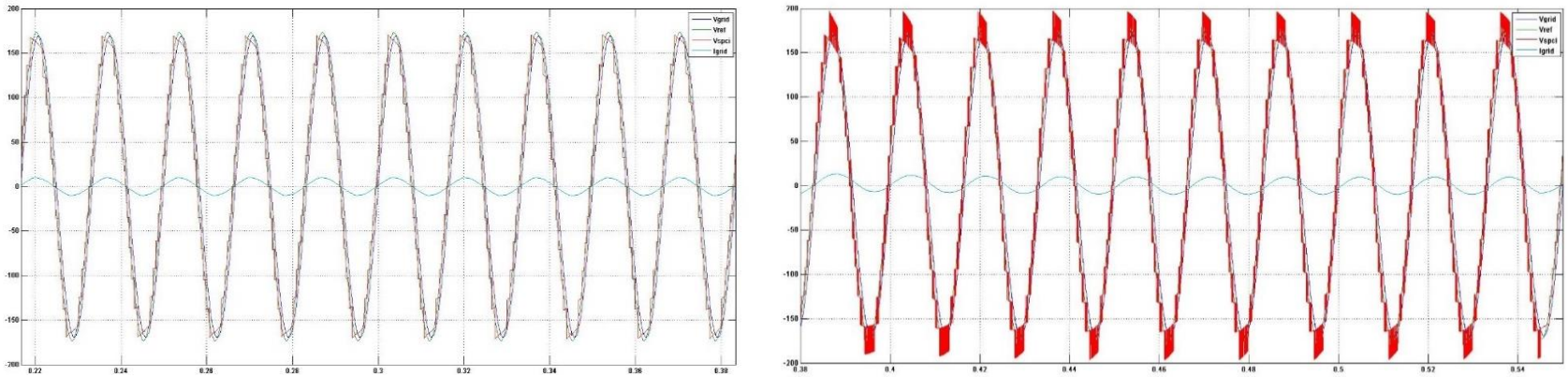


FIGURE 7.10: Unsorted pulse width modulation strategy simulation waveforms using master selector, (for operating scenario having coefficient of variation = 0, mean irradiance = 200) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}.



(a) (b)

FIGURE 7.11: Master Selector simulation results for operating scenario ($\gamma = 0.2$, $\mu = 600$).
(a): Sorted Stair Case Modulation strategy simulation waveforms for 10 cycles, showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}.
(b): Sorted Pulse Width Modulation strategy simulation waveforms for 10 cycles, showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}.

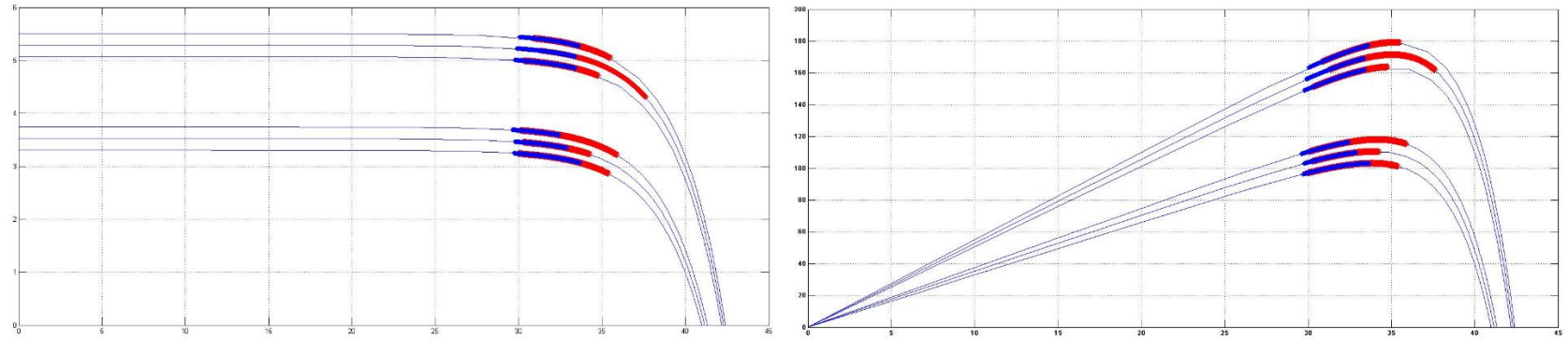


FIGURE 7.12: I – V, and P – V graphs for operating scenario ($\gamma = 0.2$, $\mu = 600$), showing each solar panel operating region in blue for sorted pulse width modulation strategy, and the operating region is red for sorted stair case modulation strategy.

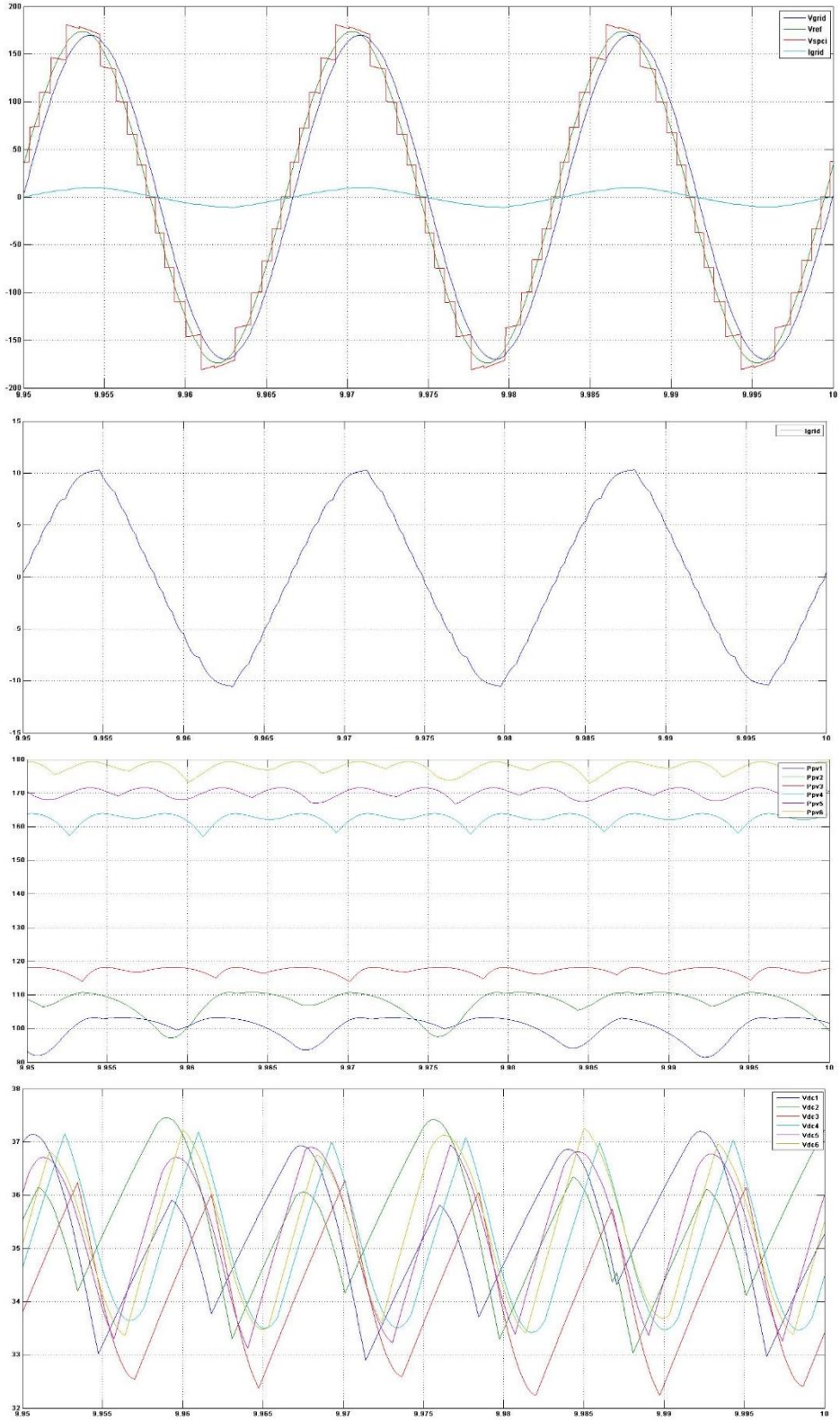
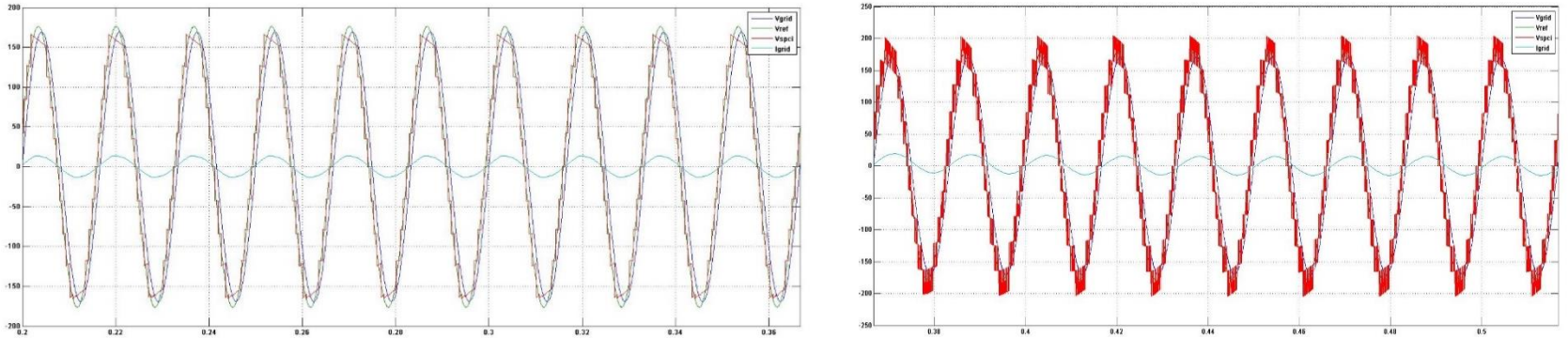


FIGURE 7.13: Sorted stair case modulation strategy simulation waveforms using master selector, (for operating scenario having coefficient of variation = 0.2, mean irradiance = 600) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}



(a) (b)

FIGURE 7.14: Master Selector simulation results for operating scenario ($\gamma = 0.4$, $\mu = 1000$).
(a): Sorted Stair Case Modulation strategy simulation waveforms for 10 cycles, showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}.
(b): Sorted Pulse Width Modulation strategy simulation waveforms for 10 cycles, showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}.

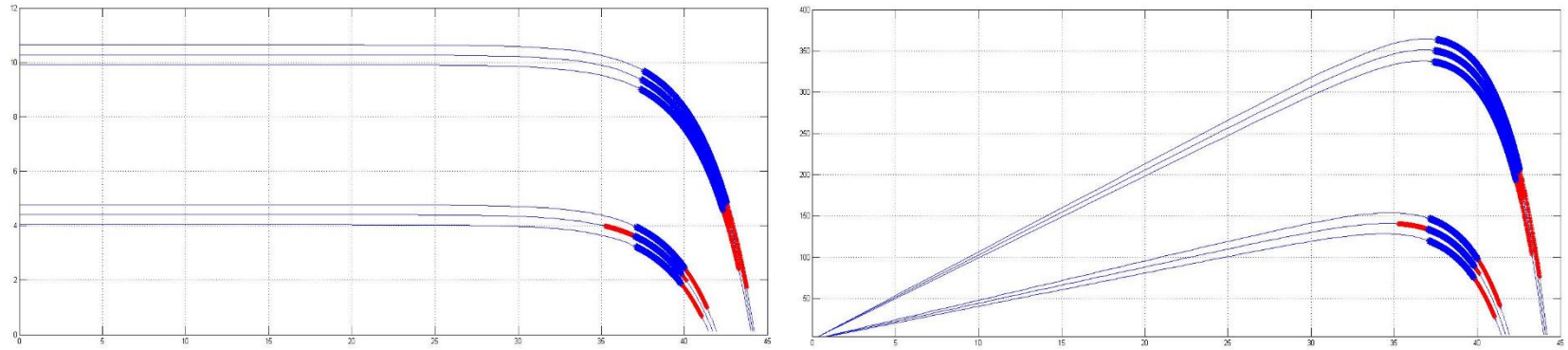


FIGURE 7.15: I – V, and P – V graphs for operating scenario ($\gamma = 0.4$, $\mu = 1000$), showing each solar panel operating region in blue for sorted pulse width modulation strategy, and the operating region is red for sorted stair case modulation strategy.

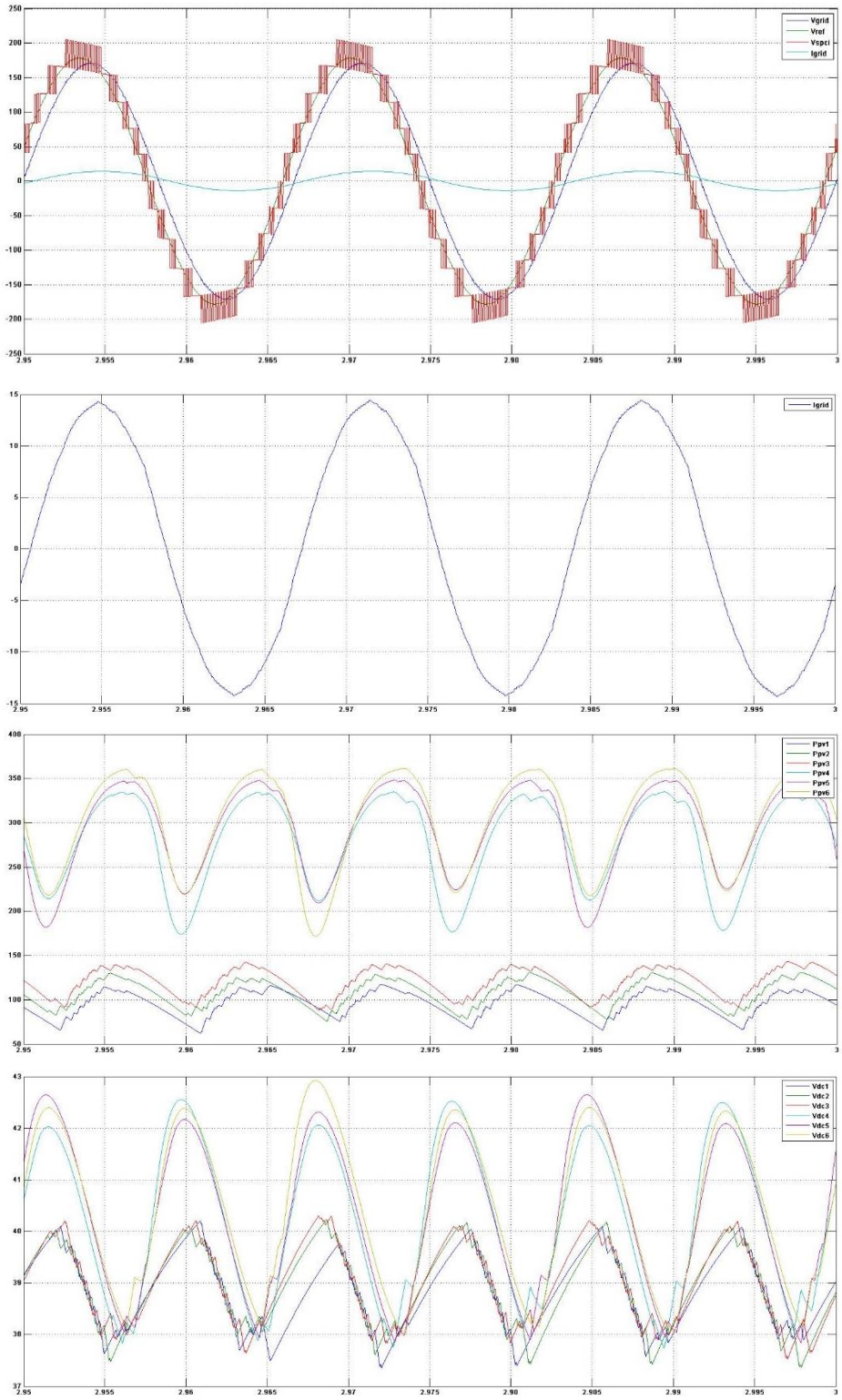


FIGURE 7.16: Sorted pulse width modulation strategy simulation waveforms using master selector, (for operating scenario having coefficient of variation = 0.4, mean irradiance = 1000) showing grid voltage, V_{grid}, reference voltage, V_{ref}, output ac voltage, V_{spci}, grid current, I_{grid}, dc power output of the solar panels P_{pv1}, P_{pv2}, P_{pv3}, P_{pv4}, P_{pv5}, P_{pv6}, dc bus voltages V_{dc1}, V_{dc2}, V_{dc3}, V_{dc4}, V_{dc5}, V_{dc6}

CHAPTER 8 : CONCLUSION

8.1. Overview

A unique methodology that converts the conventional dc voltage output of a solar panel to quasi-square wave ac voltage, which when aggregated realizes a superior quality multilevel waveform that can be directly interfaced with the power grid has been proposed. This alternative approach, termed Solar Panel Companion Inverters (SPCI), offers advantages of micro-inverters in realizing panel-level MPPT and enhanced controllability. The proposed SPCI topology along with the three control strategies namely: Unsorted Pulse Width Modulation (UPWM), Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM) have been discussed. Matlab Simulink model of photovoltaic panel has been presented. Grid tied SPCI model in Matlab Simulink has been presented. Construction of reference voltage using Phase Locked Loop (PLL) has been achieved in Matlab Simulink. Matlab Simulink models of master controllers for UPWM, SSCM, and SPWM have been presented. Simulations are performed for operating scenarios corresponding to uniform and non – uniform irradiance, and for low available power and high available power. The following are the important observations from the simulation results:

- UPWM strategy offers best yield of energy for uniform irradiance.
- SSCM offers the best yield of energy for non – uniform irradiance and low available power.

- MPWM offers the best yield of energy for non – uniform irradiance and more available power.
- UPWM control strategy can be implemented for SPCI under uniform irradiance conditions.

The observations made in the simulation results were confirmed, after a comparative analysis of control strategies has been performed. A master selector which can select the appropriate control strategy depending on the operating scenario has been proposed.

8.2. Recommendations and Future Work

The comparative evaluation of the control strategies performed in this thesis can be extended to an experimental setup. The sorting operation performed for Sorted Stair Case Modulation (SSCM), and Sorted Pulse Width Modulation (SPWM) can be implemented on a real time basis. A closed loop algorithm for implementation of Maximum Power Point Tracking (MPPT) is recommended. A Fourier analysis to study the Total Harmonic Distortion (THD) for all the three control strategies, and a comparative analysis of THD for the three control strategies can be performed. The controller design can be extended to make sure that the system is compliant with IEEE 1547 standard for interconnecting distributed resources with electrical power systems.

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