AN INTEGRATED CIRCUIT WITH SINGLE FUNCTIONAL UNIT LEVEL INTEGRATION OF ELECTRONIC AND PHOTONIC ELEMENTS: DESIGN OF THE FET - LET HYBRID 6T SRAM AND THE ELEMENTS

by

Antardipan Pal

A dissertation submitted to the faculty of
The University of North Carolina at Charlotte
in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in
Electrical Engineering

Charlotte

2022

Approved by:

_____
Dr. Yong Zhang

_____
Dr. Mohamad-Ali Hasan

_____
Dr. Jeremy Holleman

_____
Dr. Yasin Raja

ABSTRACT

ANTARDIPAN PAL. An Integrated Circuit With Single Functional Unit Level Integration Of Electronic And Photonic Elements: Design Of The FET - LET Hybrid 6T SRAM And The Elements
(Under the direction of DR. YONG ZHANG)

Continuous scaling of complementary metal-oxide-semiconductor (CMOS) transistor technology over the past few decades following Moore's law has led to significant enhancement in the speed and performance of computing architectures. In today's world with high demand in data processing, CMOS scaling is focusing more on low power, cost-effective processes, and high performance to meet the requirements of high-end computations. To meet the high computation demands, reengineered, high performance, and low power device structures were necessary, and hence field effect transistors (FET) structures have evolved from planner to multi-gate, and gate all around (GAA) structures. Also, other than the very well matured silicon electronics, advanced technologies allowing heterogeneous integration of different materials systems (e.g., Si, Ge, III–V, and II-VI groups) have been developed. Though heterogeneous integration of silicon electronics with compound semiconductors can be beneficial, such developments in hybrid integration cannot address the fundamental limitations of the pure CMOS circuits, the resistive capacitive (RC) delay associated with metallic wires, and the dielectric gate delay associated with FETs. These delays ultimately limit the data speed and energy consumption.

In this research work we have explored novel applications in electronic-photonic integrated circuits of a special type of metal-semiconductor-metal (MSM) photoconductive structure known as the light effect transistor (LET) which can emulate the current voltage characteristics of a FET but with much better performances in terms of switching speed (considering carrier transit delay), energy consumption per switch and I_{on}/I_{off} ratio, and also other optoelectronic functions like optical

logic gates, optical summation, optical amplification, and optoelectronic analog operation using LETs, which cannot be done using FETs. The LET can provide extremely fast optoelectronic switching (of the order of ~ ps), and its simplistic structure does-not add unwanted parasitic and leakages which are common in all gated FETs.

To understand the superiority of LETs over FETs, particularly the potential vast performance improvement in a hybrid integrated circuit of the two types of devices, we have explored the possibilities of LETs to replace some FETs in various pure electronic circuits. Using analytical relations and simulations, we have extensively studied the effect of replacing the access FETs in a 6T SRAM (six transistor static random-access memory) structure with LETs and have made some drastic changes in the hybrid 6T FET - LET structure by replacing the whole electrical wordline with an optical waveguide (OWG). We have also proposed a prototype novel hybrid 3D integration scheme for the 6T SRAM architecture where all the typical electronic and optoelectronic components (4T FET latch, access LETs, bit lines, peripherals, etc.) will be placed on a single electronic layer while photonic components (OWGs, on-chip lasers to drive the OWGs, etc.) will be placed separately on the photonic layer with regularly spaced openings that provide the optical signal for switching four LETs grouped together from two adjacent hybrid 6T cells in the electronic layer. Also, a fully functional FET - LET hybrid SRAM bit cell with superior performance has been designed and implemented using the *mixed-mode* design environment of Synopsys Sentaurus TCAD.

DEDICATION

To my father and my uncle, in their loving memory.

ACKNOWLEDGEMENTS

I would like to express my heartfelt gratitude and sincerely thank to my advisor, Dr. Yong Zhang for his continuous and undiminished support throughout my research. His constant motivation, enthusiasm, and guidance helped me significantly in developing logical and reasoning capabilities that are critical for research. Also, many thanks to Dr. Zhang for supporting me financially with research assistantships. Without his support, this work would not have been possible.

Along with Dr. Zhang, I would like to sincerely thank the ECE department and the department of Physics and Optical Science, for providing me with the necessary infrastructure and necessary software required for my research work. I would also like to extend my heartiest appreciation to my colleagues Jose and Tang for their support. I would like to express my sincere gratitude and thanks to my committee members, Dr. Jeremy Holleman, Dr. Mohamad-Ali Hasan, and Dr. Yasin Raja for their continuous encouragement. Also special thanks to Dr. Holleman, and Dr. Hasan for their valuable comments and suggestions during the research aptitude test which have helped me a lot to progress this research. I am very grateful to Mr. Dennis D. Yau for providing invaluable suggestions and comments on the published paper and this work in general.

Special thanks to Dr. Yasin Raja for agreeing to preside over my research as an external committee member. I would opportunity to express my gratitude to the ECE department of UNC Charlotte, for providing me with the opportunity to pursue my Ph.D., for assisting me financially with GASP and assistantships, and for allowing me to use the lab and research facilities in the department. Finally, I would like to thank my family, especially my late father for standing by me through all the good and tough times.

TABLE OF CONTENTS

LIST OF FIGURES

LIST of TABLES

CHAPTER 1: Introduction

1.1 Motivation

Over the last decade, there has been a huge boom in CMOS photonics, and it has opened up whole new paths toward advancements in integrated circuits (ICs) and integrated systems in the post-Moore scaling era. Over the last decade, the improvements in photonic integrated circuits are mostly due to the heterogeneous integration of novel optoelectronic devices with standard CMOS circuits. Figure 1.1 [1] shows the optoelectronic signal flow in a typical electronic – photonic integrated circuit (EPIC), where the active photonic devices (for instance photodetector) can act as an optoelectronic switch and can be placed in the photodetector section such that its electrical output can drive the CMOS circuit.

.

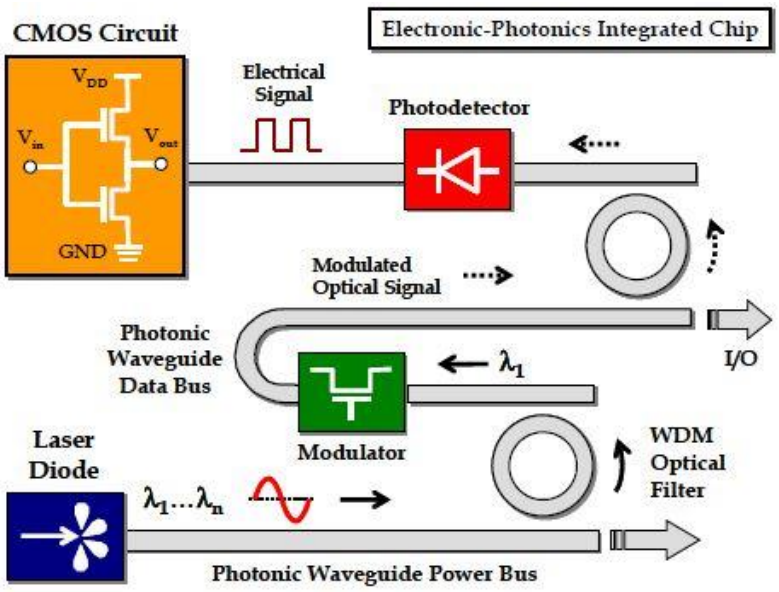


Figure 1.1: Signal flow path in an Electronic-Photonic Integrated Circuit [1]

To significantly ameliorate the energy-efficiency and data capacity of communication systems and ICs, and high preformation computing circuits, the combined use of hybrid electronic-photonic ICs have become extremely important [2-4]. The main advantage of using photons in place of electrons to process and transfer data at speeds reaching Terabits/s, over longer distances, is the much lower energy dissipation in purely photonic systems, as compared to the dissipative metal electrical wires. Among all platforms for building photonic integrated circuits (PICs), silicon on-insulator (SOI) is the most promising due to the CMOS compatible process enabled by low-cost and large-volume manufacturing. Silicon photonics integrated circuits (SiPICs) have become a potentially matured technology that can satisfy the exponentially increasing need for higher data rates with very small energy consumption, compact size, and significantly lower cost compared to discrete photonics or III-V or II-VI materials and systems [5, 6].

Some important electronic design goals are: (1) reduction of gate latency, (2) ultra-low energy consumption per bit, and (3) simplified circuit topology (for instance logic operations using optoelectronic logic circuits require a lesser number of active devices compared to all FET based CMOS circuit) and layout architecture for many complex computation structures [3]. Compared to computation, logic operation, and switching with optics, optical interconnects have been more intensively investigated due to their advantages over metal interconnects especially in intra and inter-chip communications [1]. Though over the last decade optical interconnects have been of most interest, it is also possible to have optical computations and logic operations such as implementing basic Boolean operations like the (N)AND, (N)OR, and X(N)OR logic gates and even more complex functionalities such as 1-bit half and full adders [3, 4]. Moreover, most recently,

an ultra-fast low-power deep learning network has been implemented by optical mach-mehnder interferometers (MZIs) and has consolidated the position of computation with photonics [7].

In recent times silicon photonics has been leveraging the CMOS infrastructure to address the growing demands for optical communications for internet and data center networks. The close integration of silicon photonics with CMOS promises to transform electronic–photonic technologies, enabling processor and memory chips with high-bandwidth optical input/output as discussed in [8, 9]. In the real world, photonic devices need to be integrated with a variety of nanoelectronic functions (digital, analog, memory, storage, and so on) on a single silicon die (chip). Monolithic (that is on a single chip) integration of photonic devices in close proximity to typical electronic devices like FETs is mainly crucial for reasons like allowing to achieve of high levels of performance, scalability, and complexity simultaneously for electronic–photonic systems [8, 9].

In conventional logic gates, data loss is a significant issue, and it is mainly caused since the number of inputs and outputs are not equal. It was shown by Landauer [10, 11] that the traditional Boolean logic gate for its regular operation, must dissipate energy at least kTln2 per bit loss, where k is the Boltzmann constant and T is the absolute temperature. In today's electronic systems, Ohmic loss (I^2R) is inevitable and occurs due to the flow of electrons through a conducting/semiconducting medium. Hence, in today's data centric era, an increase in power consumption is becoming a bottleneck for high performance VLSI circuits and systems. Even though CMOS technology is the most widely used in a VLSI circuit because of its low power consumption, the energy dissipated during charging and discharging operations cannot be abolished without sacrificing the circuit operation, since it is proportional to the clock frequency of the circuits [12]. On the other hand, photon being the ultimate unit of information traveling with the speed of light (with a bandwidth of THz), and with data packets of zero effective mass forming

an optical signal, the techniques of computing with light may provide a way out of the limitations of computational speed, bandwidth limitations, power dissipation and complexity inherent in traditional electronic computing methods [4]. Also, in principle, it would be possible to emulate the functions of the electronic gates in a computational digital circuit with optical logic gates where the optoelectronic counterparts of the FETs (say a light effect transistor (LET) which an M-S-M structure based photodetector that can emulate the characteristics of a FET as will be discussed in detail in Chapter 3) will perform the optically controlled logic switching, and the electrical metal wires can be replaced with optical waveguides [13, 14].

1.2 Objective

Photonic devices can provide advantages in speed and switching energy as compared to electronic counterparts, however, there are three major challenges that photonic devices face when they are directly integrated with electronic devices: size mismatch, energy data rate (EDR), and cascadability [15, 16]. Even though photoconductive devices may potentially offer advantages in switching speed [17] and switching energy [13, 14, 18, 19], it has a major drawback, and hence a photonic device such as the LETs [13, 20], cannot be directly used to drive another LET based circuit since the electrical output of the LET cannot provide the optical input signal that is used drive a similar device. So to simultaneously take advantage of the photonic devices and at the same time avoid the cascading issue in computing applications [20], a hybrid approach has been proposed wherein an integrated circuit only the switching FETs are replaced by LETs. A good example of such a circuit is a 6T static random access memory (SRAM) cell where the access FETs are replaced by LETs, and accordingly the metallic word lines by optical waveguides (OWGs) [14]. Also, this application not only improves the performance of the SRAM but also alleviates

the challenges of size mismatch and EDR (EDR ≤ 10 fJ/bit is desirable for on-chip communication) [15, 16]. This is possible with this approach because it is not required to illuminate each photonic individually, but they can be grouped together and (all access LETs in a row of the 6T array) simultaneously illuminated [14, 20] as in the operation of conventional SRAMs [21].

A novel OWG architecture embedded inside a dielectric layer in the photonic layer with multiple openings into the electronic layer has been designed and simulated using the Synopsys Photonic Design suite, *RSoft* which shows that the proposed OWG system can perform similar functions as the word line of a regular 6T array, by efficiently transmitting optical energy to the LET access devices in the same row. Moreover, the design and implementation of a fully functional hybrid 6T SRAM cell with better noise characteristics compared to the regular 6T cell confirm that the proposed hybrid structure is not only high performing (lesser delay and energy consumption) but also very robust (higher noise stability), which makes the hybrid 6T SRAM a felicitous candidate for cache applications in high performance computing systems.

CHAPTER 2: Optoelectronic Devices

2.1 Overview

Optoelectronics is the combination of optics and electronics which includes the study, design, and manufacture of a hardware device that converts electrical energy into light and vice versa through semiconductors [22]. Optoelectronic devices rely on light-matter interactions and electronic properties of matter to convert light into electrical signals or vice versa. There has always been a drive to improve light-matter interactions in semiconductor materials to make better optoelectronic devices.

In the last decade, one-dimensional or quasi-one-dimensional nanostructures (e.g., nanowires) have been widely researched as potential building blocks for nanoelectronics circuits. Due to their excellent electronic and photonic properties (due to their high surface to volume ratio as a result of a reduction in volume) semiconductor nanostructures (especially nanowires) are being used extensively for photodetectors, optoelectronic switches, optical interconnects, and photovoltaics [23-27]. The optical properties of nanostructures are particularly sensitive to their physical dimensions, and the high surface to volume ratio not only allows for enhanced optical absorption but also enhances carrier confinement which in turn results in a high gain in photodetectors [28, 29]. Due to their excellent electronic and optical properties, and reduced sizes, semiconductor nanowires based electronic-photonic devices are very important building modules for the monolithic integration of nanoelectronic and nanophotonic devices.

Silicon (Si) is the most widely used semiconductor in the IC technology, and silicon nanowires (SiNW) are the most extensively studied for electronic applications. Since Si is the main building block of IC technology, Si-based photodetectors are a lucrative choice for on-chip integration with other electronic devices (for instance FETs), since the whole process flow is

CMOS compatible [23, 24, 30], and the Si photodetectors and other Si-based optical components can be readily fabricated alongside the standard Si FET ICs as shown in Figure 2.1 [30].

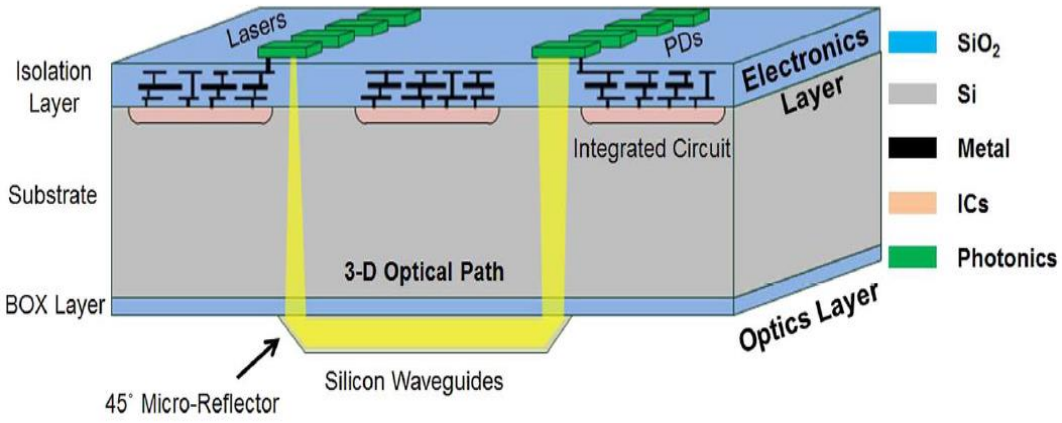


Figure 2.1: SOI-based chip-level optical interconnect module with lasers and photodetectors using 3-D guided-wave path for multi-core processor or memory-to-processor interface [30].

2.2 Nanowire Photodetectors

Photoconductivity is the process of modulation of the electrical conductivity of a device/material due to incident radiation of a suitable wavelength. In the process of photoconductivity, there are several successive or simultaneous mechanisms like the absorption of the incident light depending on the absorptivity of the material, carrier photogeneration, and carrier transport (including carrier trapping, de-trapping, and recombination) through the device to give the photocurrent governed by various physical models [24, 25, 31]. The change in conductivity of a device due to the absorption of radiation of a suitable wavelength mainly depends upon the number of carriers produced per photon absorbed (carrier generation quantum yield), and the mobility of photogenerated carriers (both majority and minority). The duration of the

photoconductive effect leading to the modulation of conductivity depends on the electronic structure of the material (like the presence of traps and defects) which in turn dictates the carrier lifetime of the photogenerated carriers [24]. The high photoresponsivity and gain observed in semiconductor nanowires, and the recent advancement in capturing and understanding the physics behind the photoconduction mechanism in low dimensional systems and materials with a high density of surface states and traps are of huge interest in the potential use of NWs as photo sensing elements in highly integrated optoelectronic devices, optical interconnects, and transceivers. The optical properties of NWs are mainly dependent upon the dielectric functions of bulk materials, with some additional effects like optical birefringence, light scattering, and waveguiding effects (light funneling). However, variations in properties arising from the NW geometry and the low dimensionality leading to carrier confinement also play an important role in the total photoconductivity [24, 31]. The optical birefringence effect mainly depends on the modulation or change of the and also due to the variation of the optical matrix elements due to the quantization of carries and is mainly predominant in very thin NWs with diameter < 10 nm, and due to the confinement of the optical electric field inside the NW's dielectric material. In the case of thin NWs (typically when NW diameter < light wavelength (λ)) the electric field vector's perpendicular component is generally non-dominant while the parallel component dominates, while for thick NWs the electric field distribution inside the NW is non-uniform [24]. Also, enhanced scattering of light happens in NWs when the physical dimension is comparable to or much lesser than the wavelength of incident radiation [24, 31]. It is evident from rigorous numerical calculations that the Silicon NW arrays have a very high absorption of incident light when the wavelength is much greater than that of the fundamental bandgap due to the very high confinement of the electromagnetic energy into the high refractive index of the NW material and its reduced volume,

which is known as light funneling, and thus outperforming their thin film counterparts made from the same material [24, 31].

2.3 Working Mechanism and Carrier Transport

The carrier dynamics and transport phenomena in photodetectors can be described by the combination of Poisson's equation, carrier continuity equations, and the drift diffusion equations as shown below [25, 32, 33]:

$$\nabla^2 \Psi = -\frac{q}{\varepsilon}(p - n + N_D - N_A) \qquad (2.1)$$

$$-\frac{1}{q}\nabla . J_n - g + r_n + \frac{\partial n}{\partial t} = 0 \qquad (2.2)$$

$$\frac{1}{q}\nabla . J_p - g + r_p + \frac{\partial p}{\partial t} = 0 \qquad (2.3)$$

$$J_n = q\mu_n nF + qD_n \nabla \mathrm{n} \qquad (2.4)$$

$$J_p = q\mu_p pF - qD_p \nabla \mathrm{p} \qquad (2.5)$$

where Ψ is the electrostatic potential; p and n are the total hole and electron concentration after illumination; g is the optical generation rate and $r_{n/p}$ is the electron/hole recombination rate; $\mu_{n/p}$ is the electron/hole mobility; $D_{n/p}$ is the electron/hole diffusion constant, and F is the applied electric field. Under illumination (considering an n-type device), the change in conductivity of the device occurs either due to the change in carrier concertation or change in carrier mobility due to scattering effects is shown [24, 31]:

$$\Delta\sigma = \sigma_{light} - \sigma_{dark} = e(\mu\Delta n + n\Delta\mu) \qquad (2.6)$$

Generally, the change in carrier concentration (Δn) due to illumination is much higher than the change in mobility ($\Delta\mu$), and hence neglecting the change in mobility effect, and considering only the recycling gain theory [28], the photocurrent density in an n-type device can be written as:

$$J_{PC} = eF\mu\Delta n \qquad (2.7)$$

The excess carrier depends on the amount of photogenerated carrier which in turn depends on the optical generation rate (number of photo carriers generated per unit volume per unit time due to optical absorption) given by [24, 34]:

$$g = \eta^* \frac{(\frac{P_{opt}}{\hbar\omega})}{volume} \qquad (2.8)$$

where P_{opt} is the absorbed optical power, and it depends on the surface area of the device exposed to illumination and the absorption coefficient of the material, $\hbar\omega$ is the energy of a photon, and η^* is the effective carrier photogeneration quantum efficiency which takes into account the effect of reflection, scattering, and low dimensionality of the NW on optical absorption. Now under steady state and constant illumination, neglecting the effects of excess carrier confinement at the device contacts, and the non-uniform distribution of excess carriers due to the applied electric field [28], the excess carrier concentration may be given as [24, 28]:

$$\Delta n = g\tau \qquad (2.9)$$

where τ is the carrier lifetime and mainly depends on the material properties and the quality of the material used in the device. By combining Equations 2.7 through 2.9, the steady-state photocurrent density for a given wavelength can be written as:

$$J_{PC} = \eta^* \frac{(\frac{P_{opt}}{\hbar\omega})}{volume} eF\mu\tau \qquad (2.10)$$

It is observed from Equation 2.10 that along with other parameters, the photocurrent depends on the quality of the material (τ is generally higher for good quality materials) used in the device. If the effects of both electrons and holes are to be considered, then the total photocurrent density can be written as:

$$J_{PC} = \eta^* \frac{\left(\frac{P_{opt}}{\hbar\omega}\right)}{volume} eF(\mu_n\tau_n + \mu_p\tau_p) \quad (2.11)$$

For a, strictly speaking, MSM photoconductor device, the carrier dynamics under bias are dependent on the potential barrier heights at the two MS contacts, and the voltage drop at the two metal contacts [25, 28, 29]. The asymmetry in the *I–V* curve of these M-S-M structures mainly arises from the difference in potential barrier heights at the two M-S contacts. Under illumination, the increase in current is not only due to the excess carrier concentration (which decreases the series resistance of the NW) but also due to the reduction of the barrier heights at the two M-S contacts [25]. Hence the observation of very high current in single NW-based MSM devices has contribution both from photoconductivity as well as the reduction of the potential barriers at the contacts [25] due to local carrier generation. Also, the recombination at the junctions can be suppressed by the illumination which enhances the photocurrent. It has also been reported that the contribution of contact barrier reduction due to illumination is more pronounced on the photocurrent of the MSM structure than the photoconductive reduction of NW resistance due to the generated excess carriers [25].

Zero bias photo response, similar to that in a solar cell, has been observed in M-S-M structures. The reason may be the formation of a built-in potential barrier at the two contacts due to band bending at the two M-S interfaces which are due to the work functions difference between the metal and the semiconductor contacts [25] at the two ends of the device. In the NW-based M-

S-M device, if the device's active region is much lesser in length than the device depletion width, then there is a possibility of the existence of an axial field in the middle of the NW without any application of bias voltage, and this phenomenon can collect the carriers giving rise to zero bias photocurrent [25]. For exactly symmetrical MS junctions, the net zero bias photo current will be zero. The zero bias photocurrent increases non-linearly with incident power following a relation $I_{ph} \alpha P_{\mathrm{opt}}^{\gamma}$ [24, 25]. Generally, the photocurrent depends on photo-generated carriers, which in turn depends on the trap state dynamics and trap occupation probability around the Fermi level, and is often empirically related to absorbed optical power P_{opt} with an exponent γ. The exponent depends on the distribution of carrier traps and carrier recombination that happens inside the active region of the device [28, 29].

.

CHAPTER 3: Light Effect Transistor

3.1 Device Overview and Comparison with FETs

A FET is principally a voltage-controlled device with four terminals: source (S), drain (D), gate (G), and body (B), where the S-D conductivity is modulated by the application of a voltage at the G to create a layer of free charges which conducts current between the S-D terminals [35]. FETs are the most widely used electronic device in ICs and are used for analog, logical, and memory operations. Although FETs have evolved structurally from the early planar to the multi-gate 3D structures (like DG FET, FinFET, etc.) with continuous shrinkage in device dimensions, the basic operating principle remains the same. These multi-gate structures have led to greater fabrication complexity, and ultimately to challenges in gate fabrication and precise doping control [36-38]. Though various new technologies, like FinFETs tunnel-FETs (TFETs) [39, 40] have been developed in recent years to enable the continuation of Moore's law [41], further development with such technologies is not very promising. Also, more sophisticated structures like semiconductor nanowire (SNW) based FETs [42, 43], FETs comprising of 2D channel materials, [44, 45], and FETs with multiple independent gates have been exploited, however, no clear pathway for overcoming a FET's intrinsic physical limitations [46-48] dictated by its operation mechanisms, such as random dopant fluctuations, gate fabrication complexities, and inherent parasitic capacitances and resistances, and no viable revival technologies exist so far.

A LET as shown in Figure 3.1 [13, 14] is a two-terminal M-S-M structure with a semiconductor nanowire (SNW) placed on an insulating substrate with two M-S junctions at the ends forming the S and D contacts. Figure 3.1 brings out the structural simplicity of the LET

without a physical gate over conventional gated FETs. The working mechanism of a LET is different from that of a traditional FET in that the source-drain conductivity of a LET is

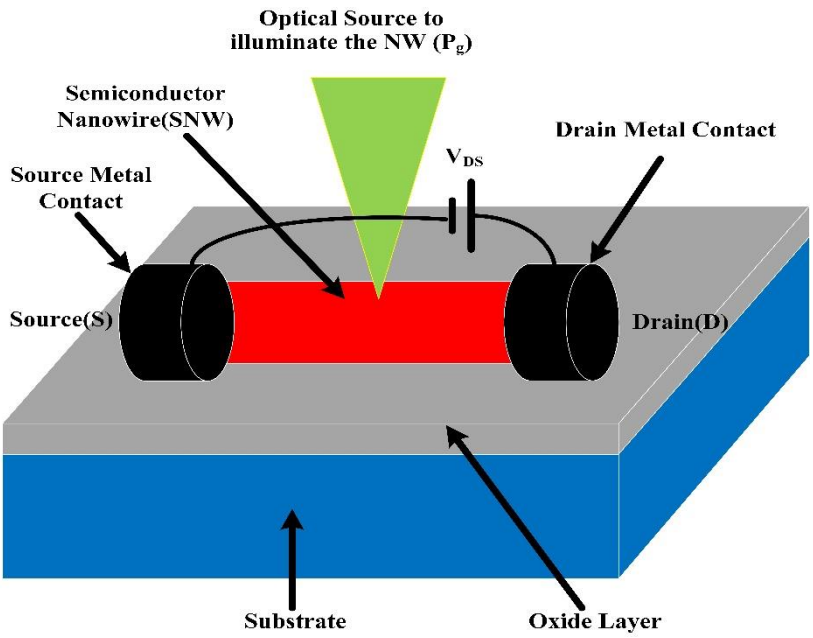


Figure 3.1: A Light Effect Transistor (LET) [14].

modulated by light or electromagnetic radiation of a suitable wavelength as in a photoconductive mechanism [49] as opposed to electrostatic control by the gate, and the current carriers are generated through optical absorption rather than thermal activation of the dopants. The advantage of an LET over an FET stems from various factors such as the removal of the physical gate, thus minimizing the complex gate fabrication process and random dopant fluctuations in FETs [36]. Hence, the LET can be scaled down to the quantum regime without the problem of short-channel effects (SCEs) that are common in nanoscale FETs [50]. Also, because the LET structure does not have a physical gate, the device speed is expected to be only limited by the carrier transit time or lifetime, whichever is smaller, rather than the capacitive delay as in the gated FETs.

While the LET can readily emulate the current-voltage (I-V) relationship of a FET (as shown in the next section) under a single beam illumination (as in a photodetector), it offers functions not readily achievable by either a FET or a photodetector [51, 52], when it operates differently than a typical photodetector under multiple independent beam illumination. It is to be noted that a traditional p-n junction-based photodetector (though superior to the M-S-M counterparts in terms of bias voltage requirements) cannot emulate the I-V of a conventional FET under illumination, while a photoconductive-based M-S-M structure like the LET under illumination can resemble a FET with gate voltage [13]. Under simultaneous multiple beam illumination (which is usually for photoconductive function), the LET can further function as optical AND and OR gates, perform optical amplification [13], and other optical analog functions that are not possible by a photodetector or single FET device.

3.2 LET Device Characterization

For the LET operation under illumination, the optical gating process has two control parameters: λ_g and P_g under single CW illumination. For the LET transfer and output characteristics studied in [13], a single beam focused CW illumination where the center of the SNW was illuminated with 633, 532, 442, or 325 nm light; and a uniform illumination of the SNW with white light from a halogen lamp was used. The LETs output characteristic was studied as a variation of the drain current with drain-source voltage (I_d vs V_{ds}) under a constant optical power and wavelength, $P_g(\lambda_g)$, which is analogous to the FET's output characteristics under a constant gate bias; while the transfer characteristic was studied as the variation of drain current with the optical power shined on the SNW (I_d vs $P_g(\lambda_g)$) at a constant V_{ds}, analogous to FET's transfer

characteristic where the gate voltage for the FET has been replaced by the control optical power in case of LET.

In the previous study using a CdSe NW of 5.5 µm in length and 80 nm in diameter with Indium (In) contacts at two ends, the illumination optically modulates the electrical conductivity of the NW between "on" and "off" states resembling that of FETs, with the measured output characteristics shown in Figure 3.2a [13]. It is to be noted that the high values of V_{ds} requirement are due to the very long length of NW used in the experiment, while for LET applications if NW of lesser lengths is used V_{ds} scales down accordingly [14]. As seen in the previous study [13], the current varies with changing the wavelength of light used for the gating purpose, fundamentally due to wavelength dependent light-matter interactions, which also gives the LET more flexibility in achieving gating-dependent optoelectronic functions as compared to FETs.

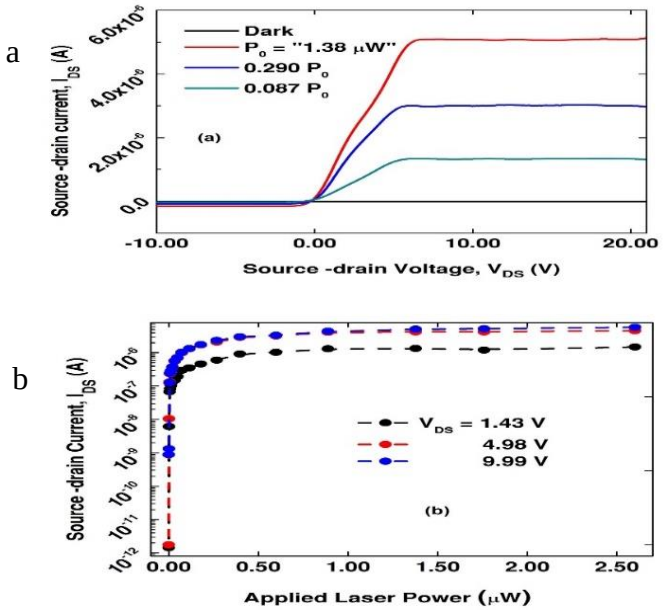


Figure 3.2: (a) Output and (b) transfer characteristics of a prototype LET based on a CdSe nanowire [13].

In the measured transfer characteristics (variation of I_d with P_g for different V_{ds}) of the LET as shown in Figure 3.2b [13], the threshold power (P_T) corresponds to the onset of the liner $I_d - P_g$ region for a given value of λ_g. A LET can employ the subthreshold region to function as optical AND gates or for optical amplification purposes. It is to be noted that in the experimental results, the power actually absorbed by the NW is ~ 10% of the applied power, since the laser spot size is considerably larger than the NW diameter, hence reducing the beam size closer to the NW diameter could drastically reduce the P_g requirement [13]. Also, the asymmetry in the measured output characteristics is probably due to the asymmetry in the In/CdSe contacts at the two ends of the NW, where one is close to ohmic and the other is close to a Schottky contact.

3.2.1 Estimation of LET Parameters

Since very long M-S-M devices are not very useful for VLSI circuit applications, and hence for performance estimation, a more practical NW length of 100 nm – 500 nm has been assumed. Although the demonstrated prototype LETs were based on CdSe NWs, there is no limit to the material system per the device mechanism. At room temperature, many semiconductors (e.g., Si, SiC, InAs, InP, GaAs, CdSe) have saturation electron velocities in the range of 10^7 - 10^8 cm/s when the electrical field is of the order of 100 kV/cm [53, 54] which implies a carrier transit time of the order of 1 – 0.1 ps and 5 - 0.5 ps for a 100 nm and 500 nm long NW respectively. Also, it is to be noted that 100 nm is the typical length scale of ballistic transport where the saturation velocity can be achieved. For longer NWs in the non-ballistic transport regime, the electron transit time depends on the electrical field. For Si at E = 10 kV/cm, electron velocity is around 7 x 10^6 cm/s [53, 54], and the carrier transit time (t_{LET}) can be estimated to be 4.3 and 7.1 ps respectively for 300 nm and 500 nm long Si NW. If the NW in the LET can be scaled down to operate in the

ballistic regime (typically ≤ 100 nm), then ultrafast switching (of the order of 1 ps or faster) can be obtained which implies ultrasmall switching energy for the LET. The photocurrent current in the LET device may be written as [13]:

$$I_d = \frac{e\eta N_{ph} G}{t_{LET}} \qquad (3.1)$$

where η is the illumination efficiency, N_{ph} is the number of photons absorbed and G is the photoconductive gain between the carriers generated by light and the total carriers in the current as given by the recycling gain theory [24, 28]:

$$G = \frac{F\mu\tau}{L} \qquad (3.2)$$

where F is the applied Electric field (depends on the D-S voltage), τ is the photocarrier lifetime which depends on the quality (traps and defects, surface states, etc.) of the material; L is the length of the device. In Equation 3.1, considering the photon flux = N_{ph}/t_{LET}, the optical power (P_g) needed to have a current of I_d at a gain of G is then given by:

$$P_g = \frac{E_{ph} I_d}{e\eta G} \qquad (3.3)$$

Assuming I_d = 1μA (a good assumption for digital VLSI circuits); $G = 10^3$ (gain of the M-S-M photodetectors increases as NW length is decreased); $\eta = 1$, and the photon energy for 532 nm illumination, $E_{ph} \approx 2.33$ eV, the needed optical power will be, P_g = 2.3 nW. For a LET the electrical switching energy due to the transit of carriers and the S-D current can be estimated by:

$$E_{el} = I_d V_{ds} t_{LET} \qquad (3.4)$$

Assuming a switching time (carrier transit time) t_{LET} = 1 ps (for a ballistic device), and an on-current of I_d = 1 μA under a D-S bias, V_{sd} = 1 V, the electrical switching energy E_{el} will be 1

aJ/switch. However, in the LET, optical gating power also contributes to the switching energy and the optical switching energy is. given by:

$$E_{op} = P_g t_{LET} = \frac{E_{ph} I_d}{e\eta G} t_{LET} \qquad (3.5)$$

Plugin in the values of P_g = 2.3 nW and t_{LTT} = 1 ps, E_{op} = 2.3 x 10^{-3} aJ/switch ≪ *Eel*, which leaves sufficient room allowing for lower gain and below 100% light power delivery efficiency. Hence the total switching energy $(E_{el} + E_{op})$ will be ≈ 1 aJ/switch which is almost more than two orders of magnitude lesser than advanced FETs having switching energy in the range of 0.1 – 1 fJ/switch.

Even considering a non-ballistic device of length 300 nm with t_{LET} = 4.3 ps, with I_d = 5 μA (more suitable for circuit purposes as will be seen in the next chapter), at a V_{ds} = 1.5 V, the E_{el} ≈ 32 aJ/switch and E_{op} ≈ 3.95 x 10^{-2} aJ/switch, which gives total switching energy of ≈ 32 aJ/switch, which is still at least three times lesser than FET's minimum switching energy.

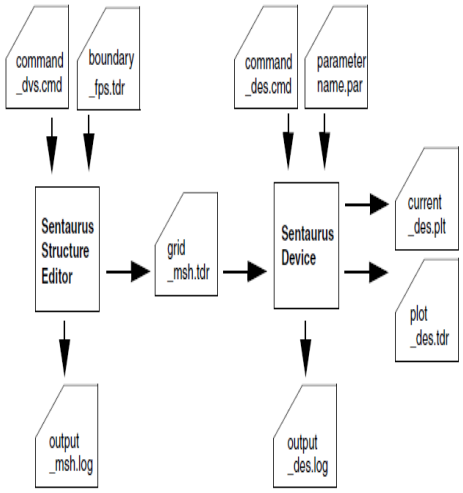
In an even more idealistic case, assuming a ballistic device with a quantum impedance of 12.9 kΩ [55], transit time of 0.1 ps, S-D current of 1 μA, and no voltage loss at the contacts, the electrical switching energy can be as low as 1.3 x 10^{-21} J/switch at an extremely low V_{sd} of only 13 mV [13]. Also, the large prototype device (CdSe NW of length 5.5 μm and diameter of 80 nm) studied experimentally under 532 nm illumination of 110 nW (only about 6% of the power was actually absorbed), yielded I_d = 0.35 μA at V_{ds} = 1.43 V; while in dark condition, I_d ~ 1 pA, which corresponds to about 1.5 pW off power. Estimating the total switching energy for such a large device using the typical room temperature carrier lifetime in a II-VI semiconductor of the order of 100 ps is $E_{el} + E_{op}$ ≈ 0.06 fJ/switch, which would still be better than typical FETs. In FETs, the gate related RC delays predominate over the carrier transit-time delay; but in the LET, the carrier

transit time through the NW channel is expected to be the predominant factor for determining the switching speed and energy of a discrete LET [14, 20].

3.2.2 TCAD Modelling of the FET and LET Devices

The FET and LET devices have been modeled using the Sentaurus TCAD modeling suite from SYNOPSYS [56] [57]. A typical *Senataurus Workbench* (SWB) workflow for device design in Synopsys Sentaurus TCAD is shown in Figure 3.3. In the Sentaurus Structure Editor (*SDE*) tool, the device structure is made, all the various doping profiles are added, all electrical contacts are made and finally, the meshing (for the active region with high carrier density and high electric field, generally fine meshing is needed) is done for the device. Once the *SDE* simulation is complete the control automatically flows to the *SDEVICE* module in the workbench, where the meshing information from the *SDE* module is incorporated; all the physical models describing the device nonidealities and depending on the device's working mechanism are added, and then various mathematical solvers are run iteratively to solve the Poisson's equation along with the carrier transport equations to obtain the outputs which are then viewed in the SVISUAL module. The meshing and other device parameters (I-V) are also viewed in SVISUAL module. A FinFET structure as shown in Figure 3.4 [58] has been simulated with the following device parameters: physical gate length (L_g) = 22 nm; fin width (F_w) = 10 nm; fin height (F_h) = 10 nm; source length = 15 nm; drain length = 15 nm; drain contact length = source contact length = 15 nm. For the n-FinFET the channel has been doped with boron @ $10^{15}/cm^3$, while the source, drain, and their respective contacts have been doped with arsenic @ $10^{18}/cm^3$. Similarly, for the p-FinFET, the channel has been doped with arsenic @ $10^{15}/cm^3$, while the source, drain, and their respective contacts have been doped with boron @ $10^{18}/cm^3$.

a



b

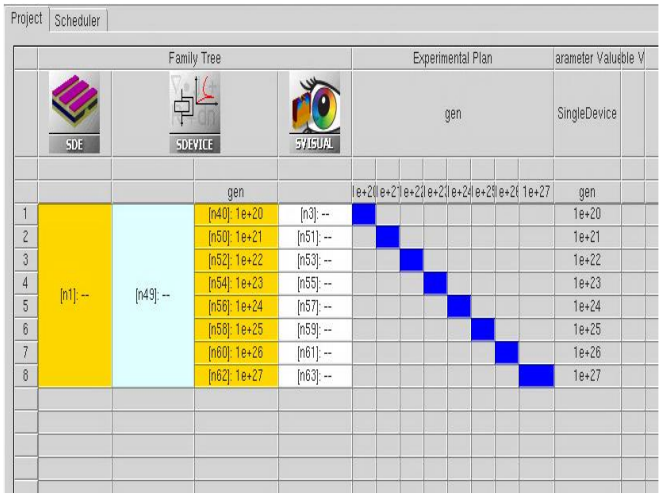


Figure 3.3: Typical (a) file structure (b) design flow in Synopsys Sentaurus TCAD.

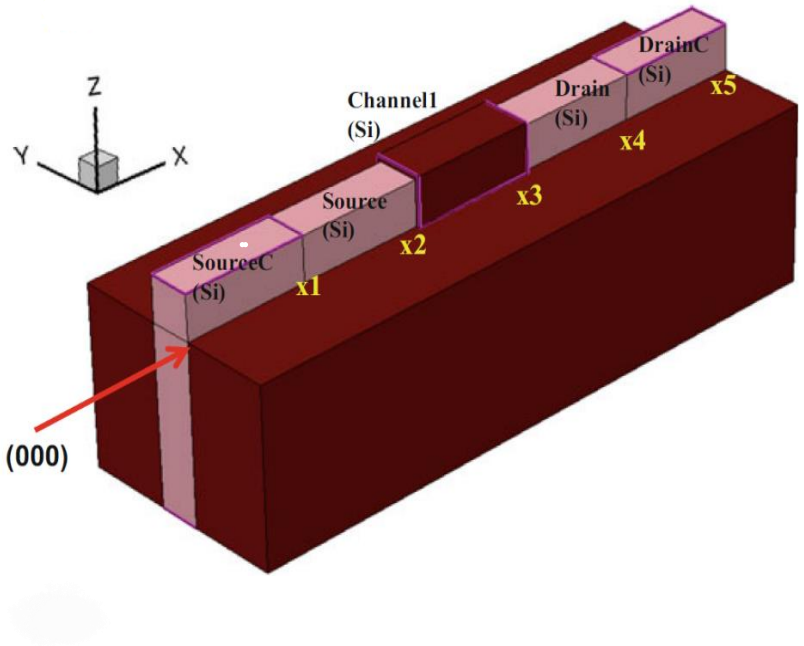


Figure 3.4: Schematic of a FinFET showing the different regions and interfaces [58].

For the simulation purpose, the meshing of the device structure generated from the *SDE* module is shown in Figure 3.5 which shows fine meshing in the channel and interface regions. To model the device's non-idealities, doping dependent, high field saturation, and normal electric field dependent mobility degradation models along with carrier recombination models are included for carrier transport in the FinFET in the *SDEVICE* module [56, 57]. Also, some advanced models like the density gradient quantum correction model (if the device dimension is < 10 nm) and carrier tunneling model [56, 57] for tunneling of carriers from the drain and source into the channel have been included in the *SDEVICE* module. For the carrier transport phenomena, the standard drift diffusion model has been used [57].

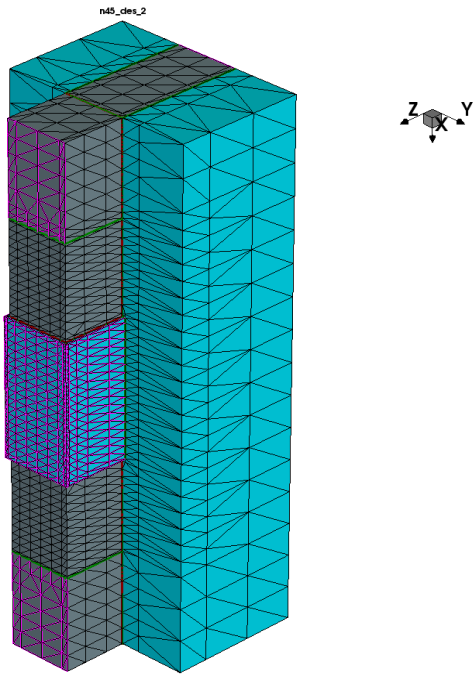


Figure 3.5: Simulated meshing structure of the FinFET in Synopsys TCAD.

For both the FinFET device and the LET device shown next, at the metal contacts Dirichlet boundary condition has been assumed [57, 59]. At metal–semiconductor interfaces, by default, there is an Ohmic boundary condition (in our case no specific metal was specified, but just set the two MS contacts to be ohmic. However, it is possible to choose the metals for Ohmic/Schottky contacts, and even set workfunctions for the contact metals or the potential barrier height at the MS contacts) which has been used in the simulation [57]. In this simulation, the potential barrier at the MS contact is computed automatically by the software, and carrier tunneling models such as the *Nonlocal Tunneling* [57, 59] at material interfaces, MS contacts, and junctions are incorporated in the simulation with carrier tunneling mass for Silicon and oxide from their respective parameter files [57]. The simulated current density in various regions of the device is shown in Figure 3.6, with gate voltage (V_g) varying from 0 to 1.5 V and at a V_{ds} of 1.4 V., and all the standard material parameters for Silicon were considered in the simulation. It is observed that there is also a very

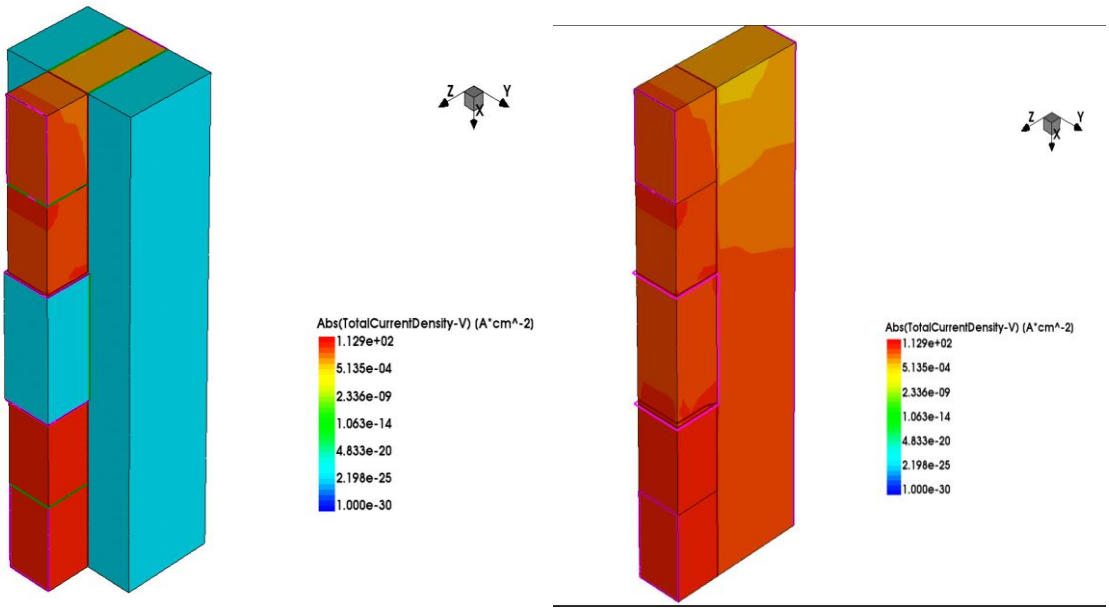


Figure 3.6: Simulated current density in various regions of the FinFET.

high current density on the body of the device. Though in a FET structure, the current is only expected to flow in the channel between the drain and source terminals, the body also has an appreciable current since it has an electrical connection and also due to the vertical electric field from the gate terminal. This unexpected current will not be present in the case of a LET structure since the body neither has any electrical connection nor is there any gate that creates the vertical electric field. The transfer and output characteristics for the FinFET device at different V_{ds} and V_g values respectively are shown in Figure 3.7, and from the TCAD analysis section the threshold voltage (V_{th}) of the device is around 0.35 V and the off current (at V_g = 0 V and V_{ds} ~ 0 V, which is equivalent to the dark current in the LET) is of the order of 10^{-10} A.

In the case of the LET, the structure is very simple with no precise doping requirements and no gate electrode requirement. A NW of 300 nm in length and 50 nm in diameter is considered. Two metal contacts were taken from the two ends of the NW to form the source and drain. For the optical switching part, various constant optical generation rates were assumed which can emulate the optical gating in the NW for various optical powers shined on the NW, since optical generation rate (g) $\propto P_g$. Contrary to the case of FinFET, only the high field mobility degradation model has been incorporated in the LET since principally the NW is undoped (however if the NW is to be doped then doping dependent mobility modification and recombination models should be considered), and also there will not be any mobility degradation due to normal (perpendicular to the NW channel) electric field, but only due to longitudinal electric filed [56, 57] since there is

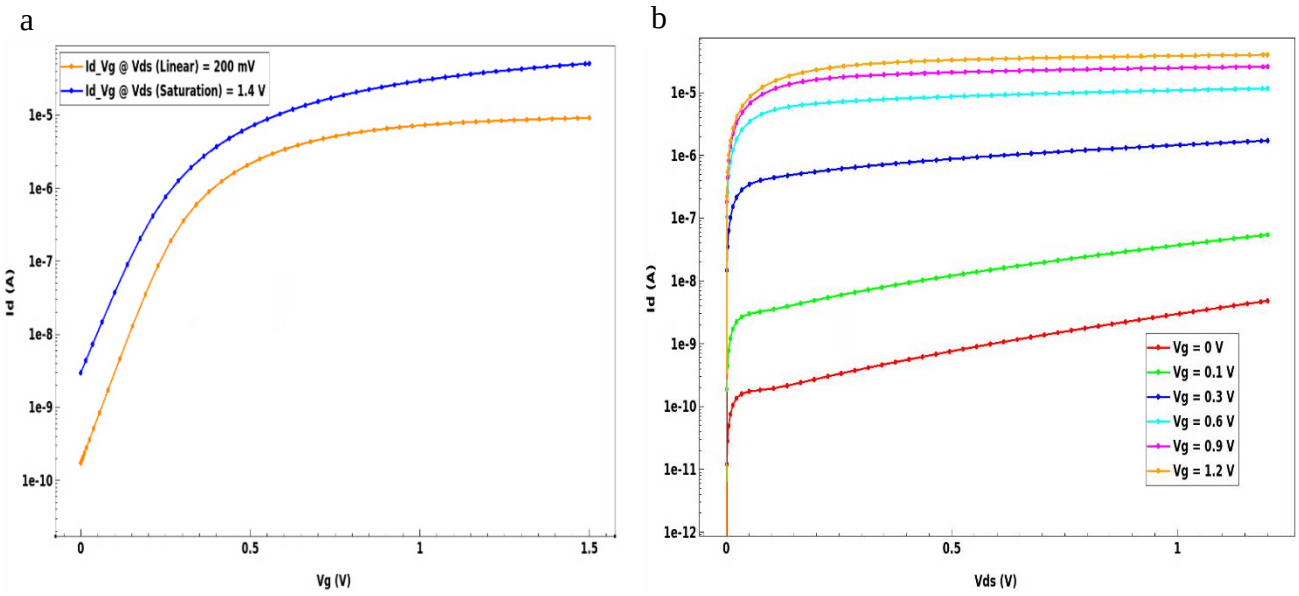


Figure 3.7: Simulated (a) $I_d - V_g$ and (b) $I_d - V_{ds}$ plots for the FinFET for various V_{ds} and V_g values, respectively.

no gate control on the NW channel electrostatic. SRH and Auger recombination models with standard parameters for Silicon were included in the NW region as well as the Si/SiO_2 interface with standard parameters for Silicon and SiO_2 [57]. Also, the carrier tunneling model for tunneling of carriers from the two contacts into the NW channel under illumination and applied electric field has been included. For carrier transport, the standard drift-diffusion model has been used. The meshing of the LET structure in the *SDE* tool and the structure showing the current density in different regions of the device are shown in Figures 3.8 and 3.9, respectively. From Figure 3.9, it can be seen that in contrast to the simulated FinFET structure, the LET does not have any current flowing through the device substrate since the NW is placed on a thick insulator and the substrate has no electrical connection, and hence body related leakage will not be there in the case of LETs.

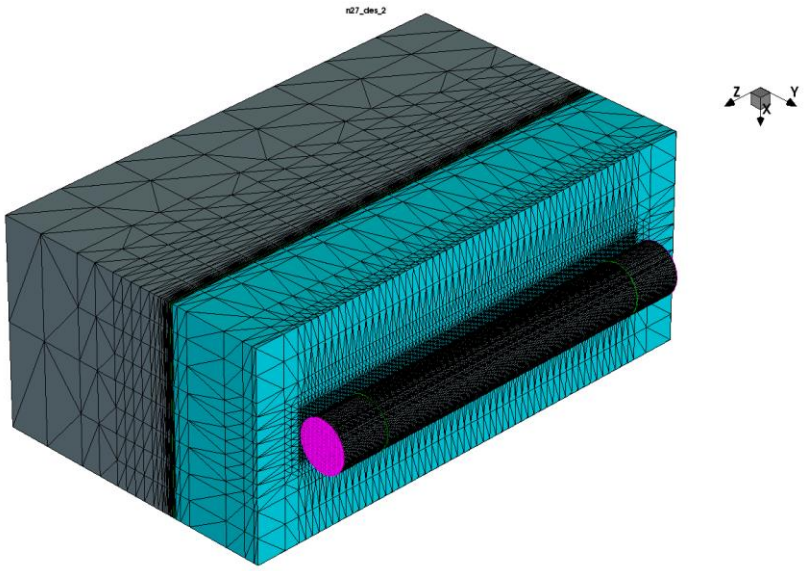


Figure 3.8: Simulated meshing structure of the LET in Synopsys TCAD.

The output characteristics ($I_d - V_{ds}$) plot of the LET device under illumination for various optical generation rates g = 10^{21} - 10^{29} /cm^3/sec (which signifies the various optical gating powers P_g), and the I_d - V_{ds} under dark conditions (g = 0) are shown in Figure 3.10:

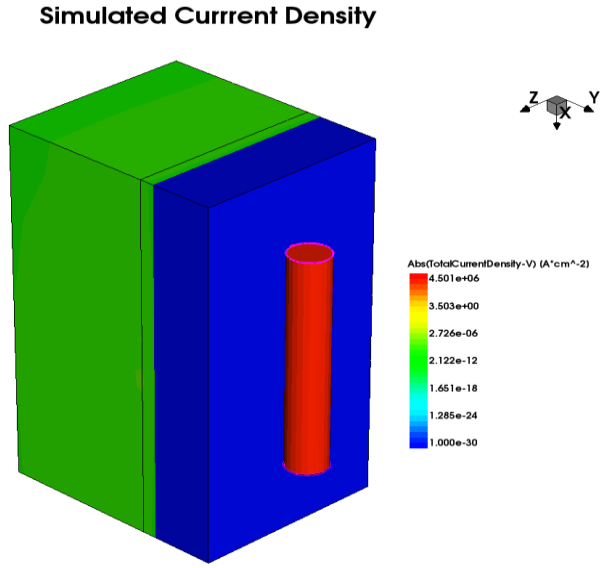


Figure 3.9: Simulated current density of the LET in Synopsys TCAD.

It is well established from Figure 3.10 that the output characteristics of the LET under different illumination powers (in the simulation it is represented by different generation rates) are very similar to that of conventional FET's output characteristic with different gate voltages. Also, the transfer characteristics, I_d (drain current) – P_g (P_g equivalent to optical generation rates since $P_g \propto$ photon flux at a particular wavelength) plot for the LET under different V_{ds} values

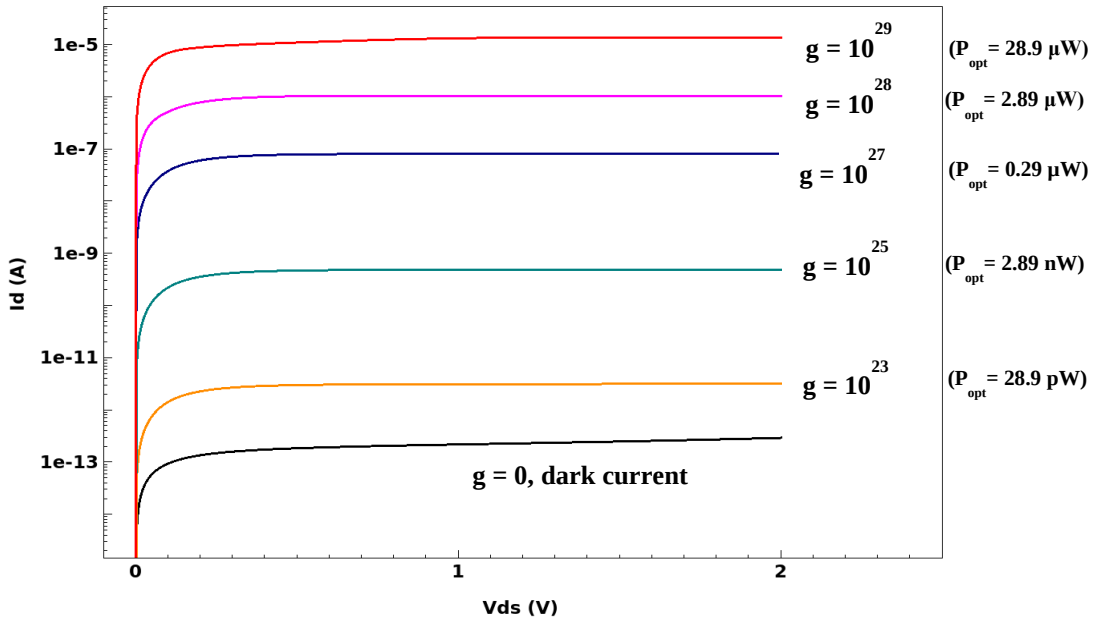


Figure 3.10: Simulated output characteristics (I_d – V_{ds}) of the LET, g in /cm^3/sec.

is shown in Figure 3.11, where in Figure 3.11a the optical generations are also in log scale to accommodate for the wide range of values, and in Figure 3.11b the optical generations are in linear scale which resembles the FET's transfer characteristics with a subthreshold slope. In the low power region, the I_d - P_g (optical generation) is sublinear but quickly becomes linear as seen in Figures 3.11 and 3.13.

Moreover, a ballistic LET with a much small dimension (length = 100 nm and diameter = 30 nm) has also been designed and simulated using Synopsys TCAD. To incorporate the ballistic transport, the ballistic mobility model has been used in the simulation which considers the carrier dynamics in the ballistic regime [57].

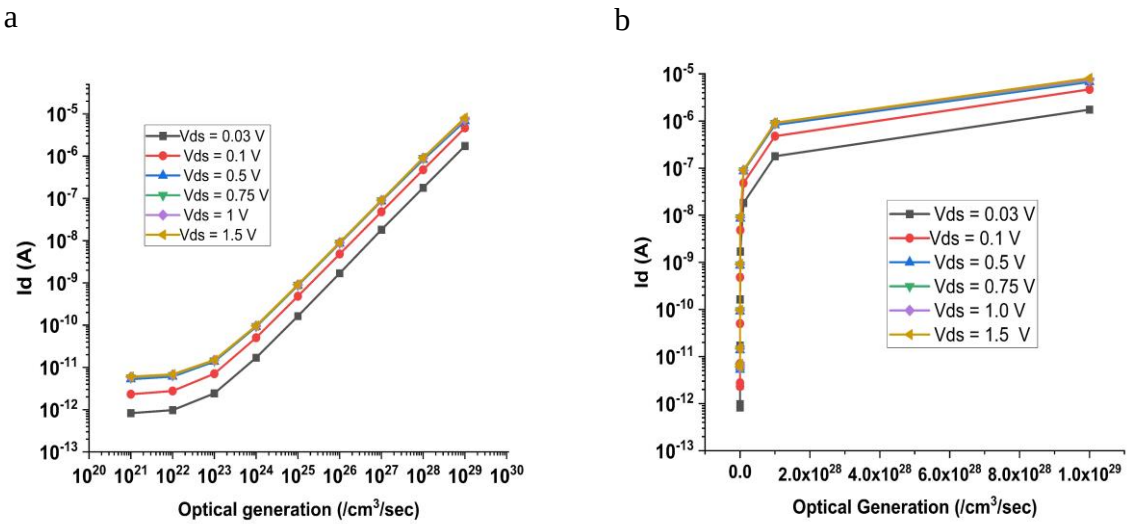


Figure 3.11: Simulated transfer characteristics (I_d – Optical Generation) of the LET (a) both axes in log scale, (b) only I_d in log scale.

Also, the dark current (for both regular and ballistic LET) is extremely low (of the order of 10^{-13} A) mainly due to the lack of background doping in the NW (undoped NW). Moreover, asymmetrical MS contacts by using contact metals with different work functions such that one contact is close to ohmic (by default in Sentaurus *SDEVICE* module) and the other is close to a Schottky contact [60] (metal with workfunction > that of Silicon) can further reduce the dark current. The output and transfer characteristics of the ballistic device are shown in Figures 3.12 and 3.13, respectively. As evident from the figure, the ballistic device needs an extremely low

drain-source bias of around 30 mV (as also mentioned in [13]) to have a similar range of on-currents (10^{-6} A) as the regular device, in the comparable range of the generation rates, $10^{21} – 10^{29}$/ $cm^{-3}s^{-1}$, and hence it will be very suitable for ultra-low power applications.

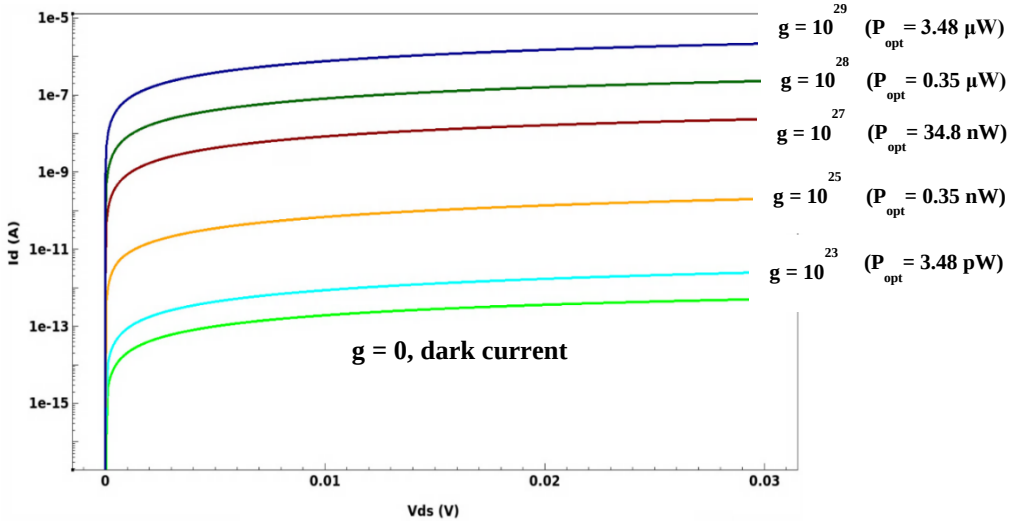


Figure 3.12: Simulated output characteristics ($I_d – V_{ds}$) of the ballistic LET, g in /cm^3/sec.

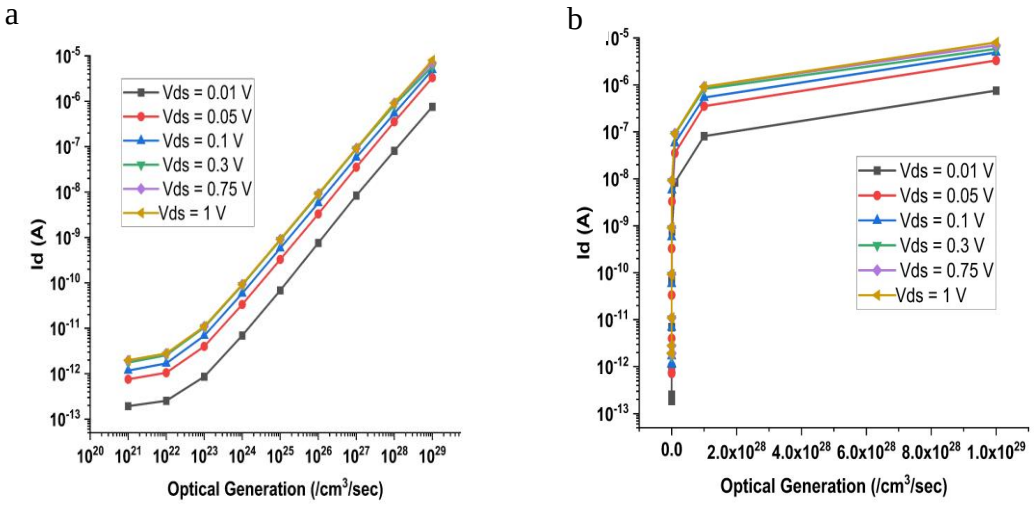


Figure 3.13: Simulated transfer characteristics (I_d – Optical Generation) of the ballistic LET (a) both axes in log scale, (b) only I_d in log scale.

Also, photoconductive gain of the device defined as the ratio of the total carriers in the current to the carriers generated by optical excitation [24, 29] is calculated for the regular LET using the simulated I_d and optical generation values from Figure 3.11 and the gain is plotted for the regular LET with respect to the optical generation rates as shown in Figure 3.14.

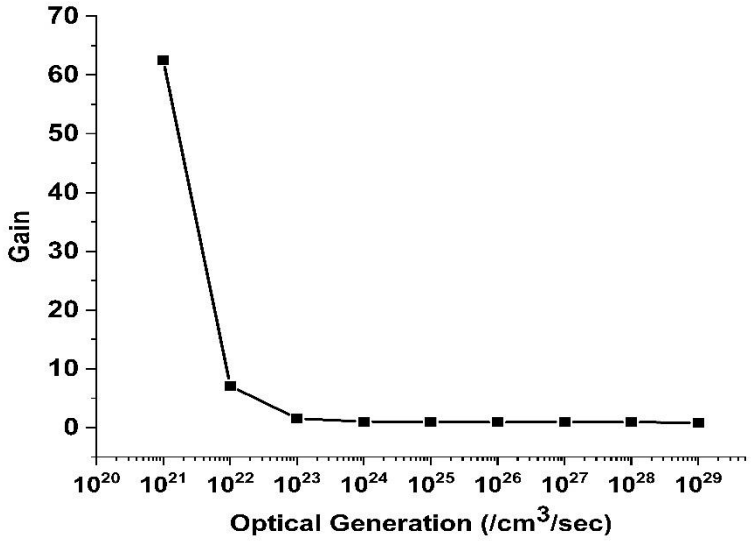


Figure 3.14: Gain vs optical generation (P_g) for the regular LET.

It is seen from the Figure 3.14 that there is some gain for the LET device at lower optical generations rates (10^{20} – 10^{22} /cm^3/sec) which rapidly falls to values ~ < 1 as generation rates increase. The observed gain at lower optical generation rates (the reason for gain needs further investigation) may be due to the more pronounced effect of the externally injected carriers from the M-S Ohmic contacts on the total current giving rise to a gain, and the contribution of injected carriers from the M-S Ohmic contacts fall rapidly (due to carrier saturation maybe due to the effect of traps) at higher optical generation rates as the huge number of excess carriers generated from the external optical illumination dominate the total current and hence gain also falls rapidly and saturates to a value ~ 1.

Now, considering I_d = 1 μA, at V_{ds} = 1.5 V at an optical generation g = 10^{28}/cm^3/sec (from Figures 3.10 and Figure 3.11) and using the (photoconductive gain) G = 0.98 (for g = 10^{28}/cm^3/sec form Figure 3.14), and using the Equations 3.3 and 3.5 (and other parameters exactly same as used in Equations 3.3 and 3.5), P_g = 2.38 μW and E_{op} = 10.2 aJ respectively, and also the calculated P_g is very similar to what is shown in Figure 3.10. Now using Equation 3.4 and considering the exact same parameters as used above, E_{el} = 6.45 aJ, which is comparable to the E_{op} calculated above, and $E_{op} << E_{el}$ as discussed in Section 3.2.1 does not hold since the simulated LET gains are ~ 1 (G values are not high) for the generating rates considered in the calculation. Also, it is to be noted that having no gain is not necessarily bad, because high gain typically means low speed (bandwidth, since gain-bandwidth product is constant for a device), although no gain means higher optical gating power (*Pg*) to produce the same photo current as seen in the above calculations.

3.3 Conclusion

In this chapter, the details of the LET device, its optoelectrical characteristics, performance matrices, and also its possible application in digital circuits are discussed. The I-V curve shows that a LET under single beam illumination can emulate the I-V (both the output and transfer characteristics) of a standard FET, the only difference is that the gate voltage in the case of the FET is replaced by the optical power in the case of the LET. Moreover, it has been found from TCAD simulation that since the LET does not have any electrical connection to the body (which just provides mechanical support), there is no unwanted leakage path to the body and hence the body current in the LET is almost ten orders of magnitude lesser than the body current in the simulated FinFETs. Since the nanowire in the LET is undoped the dark current is extremely low, of the order of 10^{-13} A for the Silicon NW used in the simulation, an on-

current of the order of 10^{-6} A yields an on-off ratio of 10^{7}. Moreover, the ballistic device (length = 100 nm, diameter = 30 nm) also has similar values of the on-off ratio with only a slightly lower dark current of about 4 x 10^{-13} A (the regular LET has a dark current of about 7 x 10^{-13} A), and it needs only around 30 mV – 50 mV of drain-source bias to achieve such high on-off ratios, which makes the ballistic devices extremely energy efficient and a very useful candidate for ultra-low voltage electronic circuits.

CHAPTER 4: Conventional and Hybrid 6T SRAM

This Chapter reused the contents from the articles below:

Reprinted with permission from *A. Pal, Y. Zhang, and D. D. Yau, "Monolithic and single-functional-unit level integration of electronic and photonic elements: FET-LET hybrid 6T SRAM," Photon. Res., vol. 9, no. 7, pp. 1369-1378, 2021/07/01 2021, doi: 10.1364/PRJ.420887.*

Reprinted with permission from *A. Pal, Y. Zhang, and D. D. Yau, "Light Effect Transistors for High-Speed and Low-Energy Electronic and Photonic Integrated Circuits," in 2021 IEEE Research and Applications of Photonics in Defense Conference (RAPID), 2-4 Aug. 2021 2021, pp. 1-2, doi: 10.1109/RAPID51799.2021.9521451.*

4.1 Survey of SRAMs

High speed, low power, low leakage, and low noise Static Random-Access Memory (SRAM) are in high demand for high-performance cache memories in computing systems. Memories are the most power-hungry blocks and consume most of the area on a chip due to their high capacity [61, 62]. Therefore, the performance and energy efficiency of SRAM is extremely important in both high-performance and ultralow-power portable, battery-operated electronic systems. SRAMs being the fastest of all memories are generally used as high-speed cache memories which have a direct connection with the CPU as shown in the processor - memory architecture of Figure 4.1 [63], and such high-speed memory-processor interfacing is not possible to attain with other memory architectures. Since on-chip caches typically consume 25% – 45% of the total energy of a chip [64, 65], and hence it is imperative to design high-speed, energy-efficient, low leakage embedded memories that are desirable for a modern electronic system.

Many techniques have been exploited at both device and circuit levels to improve the performance of the SRAM on an incremental level, particularly in speed and energy consumption

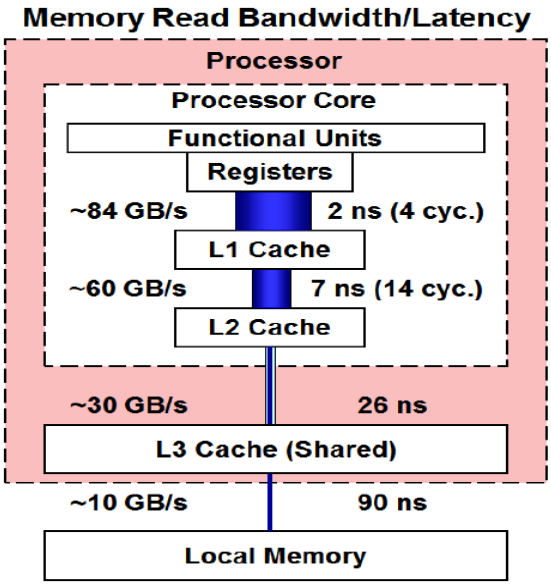


Figure: 4.1 Memory levels in a processor showing the memory bandwidth and latency. Width of blue lines indicates relative access speed [63].

[66-68]. It is possible to design a low leakage SRAM cell with supply voltage scaled down in which the voltage swing per switching activity per cell can be reduced (in both read or write operation), which will reduce the overall dynamic power consumption of the circuit. However, lowering supply voltage is fundamentally limited by various design issues like degradation in cell stability, noise margin, reduced on-current-to-off-current ratio, and strong sensitivity to process, voltage, and temperature variations [62, 69, 70]. Also, various other detrimental effects like degradation of the noise margin, an exponential increase of the leakage current, SCEs resulting from aggressive scaling of CMOS memory cells into the nanometer regime, especially in less than 32 nm technology [69, 70]. Moreover, to worsen things, excessive scaling of device dimensions and using ultrathin gate oxide in advanced technology nodes have resulted in an alarming amount of gate oxide tunneling current [62, 70] which adversely affects the circuit leakage. Also, the parameter fluctuation effects like line-edge roughness, random dopant fluctuation, and gate-oxide-

thickness fluctuation reduce the stability of SRAM cells and hence adversely affect the data storage capacity and the read and write operation (degraded noise margins and hence the stability), [62, 70]. Though the sub-threshold design for low-power applications has been carried out, the successful operation of such memory circuits is very challenging since the performance of SRAMs and the noise margins degrade at very low voltages [62, 70].

Double gate (DG) MOSFET, tunnel FETs (TFET), and FinFETs with better control of channel electrostatics have emerged as lucrative choices in the last decade to improve the performance of SRAM cells in terms of leakage current reduction, speed enhancement and mitigate various SCEs which are predominant in highly scaled bulk MOSFETs [50, 67, 71]. With the increase of SCEs with reduced technology nodes in highly scaled planar FETs, the most feasible device with reduced SCEs that is compatible with the standard CMOS technology is the tri-gate device structure, the FinFET. Various device and circuit techniques have been implemented to enhance the performance of FinFET based SRAM cells/arrays [67, 72, 73]. Different circuit techniques, such as using additional devices to improve SRAM cell stability and the usage of the back gate feature of independent gate FinFETs in the access paths of the SRAM cell to reduce environmental variation and leakage, have been used to boost the overall performance of the SRAM cell [67, 74, 75]. Techniques including the usage of reduced gate voltage (word line voltage) for the access transistors, using negative ground under the idle condition, employing dual threshold voltage devices, and transistor stacking have been reported to minimize the leakage currents and increase speed [76]. The ways to improve the read and write access time as well as reduce leakage many techniques have been proposed; like forward body biasing technique and self-controllable-voltage-level switch techniques are used to better the

performance of the SRAM cell in terms of speed improvement in the active mode, whereas a reversed body biasing technique is used to reduce the leakage in the standby mode [77].

Moreover, it has been well established that 6T SRAMs made from nanowire (NW) based structures (e.g., gate-all-around, band-to-band tunneling FETs) have much better noise margin, lesser variability, and much better leakage suppression due to lesser SCEs as compared to FinFET based structures [78-80]. It has also been reported that scaling down to more advanced technology nodes (far below 22 nm), NW based device structures offer much better SCEs, drain induced barrier lowering (DIBL), subthreshold slopes, higher switching speeds, and less variability in device performance with scaling [81], which enhances the robustness of the circuits made from them.

Above-mentioned efforts primarily focus on improving the FET performance on the single device level to bring about the improvement for the 6T SRAM cell. However, the primary factors limiting the read and write speeds and the corresponding energy consumptions are the characteristics of the access transistors (rather than the transistors of the inverters) and the capacitances of the word lines and bit lines. The hybrid FET-LET 6T SRAM [14, 18] discussed in this chapter can offer a major improvement in performance with better energy efficiency by replacing the two access FETs with two LETs and also replacing the electrical word line wires with dielectric optical waveguides (OWGs). This hybrid structure offers a very close monolithic integration of the electronic and photonic components at the chip level offering a hybrid EPIC structure. Additionally, this application avoids the well-known energy-data rate (EDR) challenge (EDR $\leq$ 10 fJ/bit for on-chip communication) [15, 16], because it does not require using light to address photonic devices individually, but in a group simultaneously through an optical waveguide, for example, simultaneously illuminating all the access devices in a row of the hybrid array [14].

Although photoconductive devices are superior in compared to electronic devices in switching speed [13, 14] and switching energy [13, 20], they have a major drawback of directly cascading with another similar device. Likewise, LETs (with their electrical output) cannot be used to directly drive another LET-based logic gate (which needs optical input) efficiently without going through relatively inefficient electrical to optical energy conversion.

4.2 6T SRAM

4.2.1 Working Mechanism

In this section, the roles of access transistors in determining the overall speed and total energy consumption of a conventional 6T SRAM cell/array with 6 FETs are analyzed to highlight the needs and directions for improvement. The three main operations of a 6T SRAM cell are writing data into the cell, reading data from the cell, and holding or storing data.

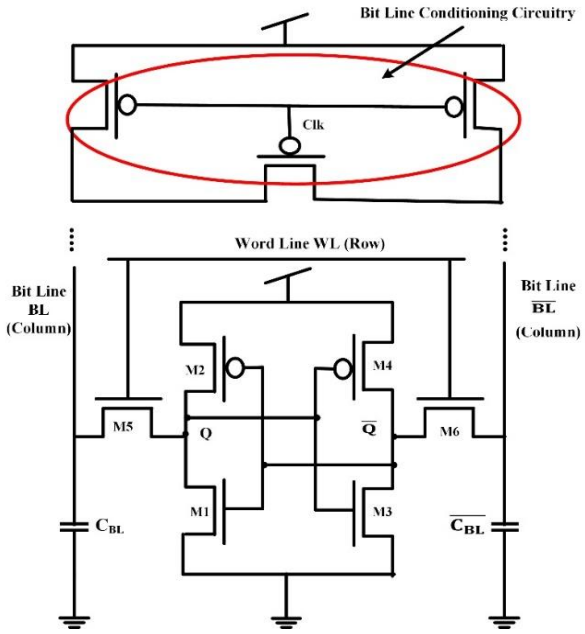


Figure 4.2: A conventional 6T SRAM cell [14].

As shown schematically in Figure 4.2, a conventional 6T SRAM has two cross-coupled latches formed of FETs M1-M4, along with two access devices M5 and M6 that allows to access the cross-coupled latch for the read and write operations. The two access transistors along with the word line (WL) and bit lines (BL/$\overline{BL}$) play an extremely crucial role in determining the overall speed, power dissipation, and stability of the cell [21, 82, 83]. Encircled in red in Figure 4.2 are the three p-FET devices which serve as the bit line conditioning elements, and their role is to pre-charge and make the bit line voltages equal to each other before each read and write operation, and they also play a crucial role in the read and write processes of the SRAM array [84].

The dynamic energy consumptions of the 6T SRAM that occur during either the write or read process. are analyzed assuming that the SRAM cell is initially at logic 0 (i.e., Q = 0, $\overline{Q}$ = 1), as shown in Figures 4.3a and 4.3b. Before the 6T cell read operation the bit line capacitances C_{BL} and $\overline{C_{BL}}$ are pre-charged to V_{DD} via the pre-charge circuitry; then after the word line turns on the access devices M5 and M6, the bit line BL is partially discharged through the path M5 and M1 as shown in Figure 4.3a, while the bit line $\overline{BL}$ remains at V_{DD}, which allows the sense circuitry to read

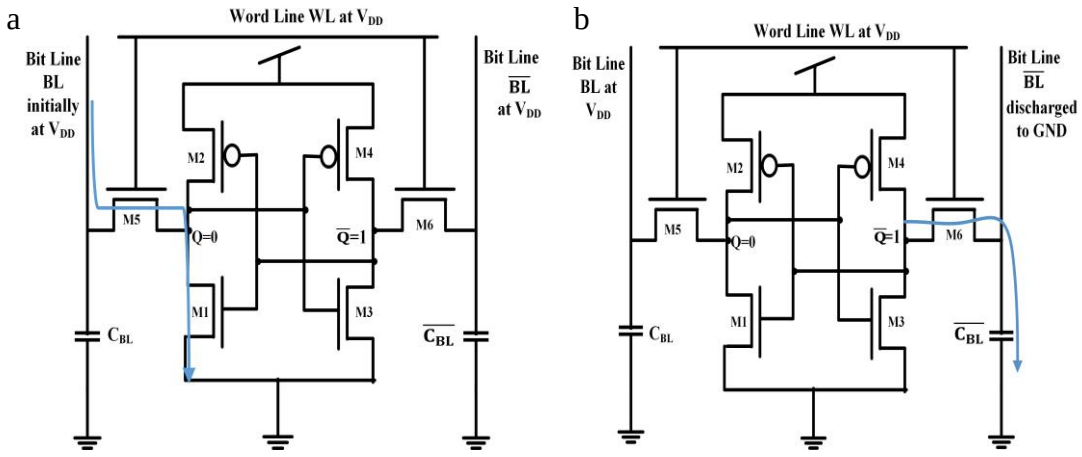


Figure: 4.3 (a) 6T SRAM cell showing the read operation (b) write operation.

the state based on the voltage difference between bit lines BL and $\overline{BL}$. Similarly for the write operation as shown in Figure 4.3b, one of the already pre-charged bit lines, $\overline{BL}$ is fully discharged via the write circuitry (not shown in the figure), then the node $\overline{Q}$ which was initially at logic 1 is discharged through the access device M6 such that M1 and M4 turn off while M2 and M3 turn on, and a cell flipping occurs such that Q = 1, $\overline{Q}$ = 0 and hence a write-1 operation takes place. As can be seen from Figure 4.3, the bit line and the word line capacitances mainly depend on the drain/source capacitance and gate capacitance respectively of the access transistors, along with bit line and word line wire capacitances. Hence, as evident the access devices play a crucial role in determining the overall SRAM cell performance.

4.2.2 Delay and Energy Estimation of 6T SRAM Array

A regular 6T SRAM array (without considering the various peripherals and assist circuits) is shown in Figure 4.4 it is evident that the word line capacitance (C_{WL}) consists of the gate capacitances (C_{gate}) of all the access FETs in a row along with the horizontal wire capacitance and is calculated as following [21, 83]:

$$C_{WL} = n_C(2C_{gate} + C_{wire,row}) \qquad (4.1)$$

where n_C is the number of columns in the 6T array and $C_{wire,row}$ is the horizontal wire capacitance, and is given as:

$$C_{wire,row} = 5P_{metal}C_w \qquad (4.2)$$

where P_{metal} and C_w are the technology dependent metal pitch and wire capacitance per unit length, respectively.

The bit line capacitance (C_{BL}) consisting of the drain/source capacitance (C_{drain}) of the access FETs and the vertical wire capacitance is calculated as:

$$C_{BL} = n_R(C_{drain} + C_{wire,col}) \qquad (4.3)$$

Where n_R is the number of rows in the array, and the vertical wire capacitance, $C_{wire,col}$ is calculated as [82]:

$$C_{wire,col} = 0.4C_{wire,row} \qquad (4.4)$$

The capacitance at the output node (node Q in Figure 4.2) is the summation of the output capacitance of the (M1-M2) inverter, gate capacitance of the (M3-M4) inverter, and the drain capacitance of the access device M5, and is calculated as follows [21, 85].

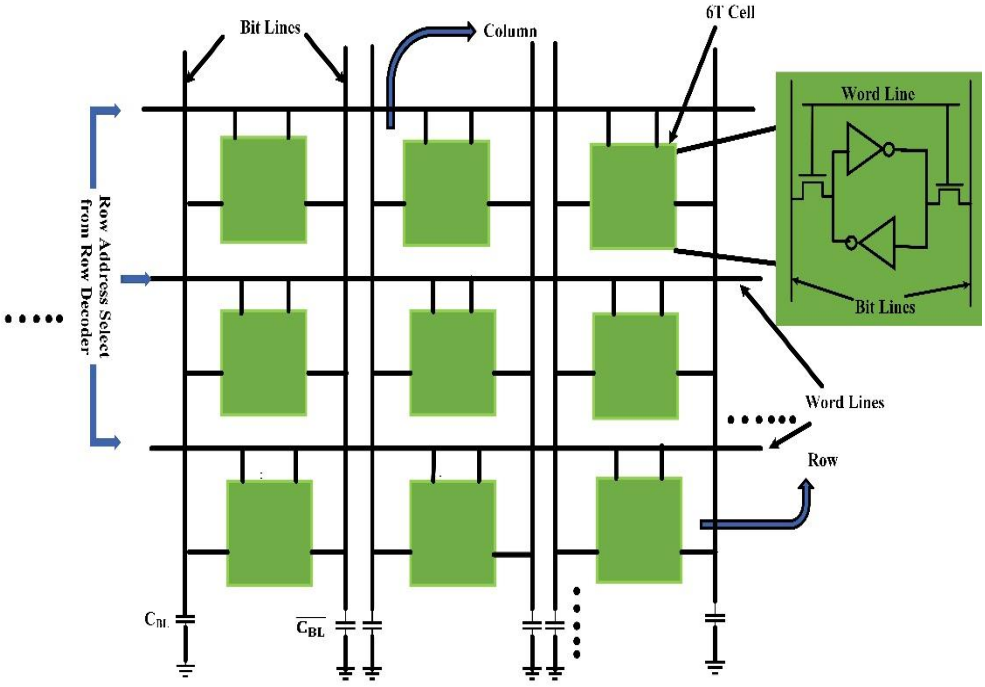


Figure 4.4: A conventional 6T SRAM array.

$$C_{out} = C_{drain,M1} + C_{drain,M2} + C_{gate,M3} + C_{gate,M4} + C_{drain,M5} \quad (4.5)$$

The read delay and energy of the 6T array are calculated as follows [82]:

$$T_{read} = \frac{C_{WL}V_{DD}}{I_{WL,drive}} + \frac{C_{BL}\Delta V_{read}}{I_{read}} \quad (4.6)$$

$$E_{read} = C_{WL}V_{DD}^2 + C_{BL}V_{DD}\Delta V_{read} \quad (4.7)$$

where V_{DD} and ΔV_{read} are the supply voltage and the change of the bit line voltage at the end of the read operation respectively, and $I_{WL,drive}$ and I_{read} are the word line driver current and 6T cell read current, respectively. Similarly, the write delay and energy are calculated as [82]:

$$T_{write} = max\left(\frac{C_{WL}V_{WL}}{I_{WL}}, \frac{C_{BL}V_{DD}}{I_{write,ckt}}\right) + \frac{C_{out}\Delta V_{out}}{I_{write}} \quad (4.8)$$

$$E_{write} = C_{WL}V_{DD}V_{WL} + C_{BL}V_{DD}^2 + C_{out}V_{DD}\Delta V_{out} \quad (4.9)$$

where $V_{WL} = V_{DD}$ is the word line voltage when it is on, ΔV_{out} is the change of output node voltage during the cell flipping operation, I_{WL}, $I_{write,ckt}$, and I_{write} are respectively the word line current when on, write assist circuitry current and 6T cell write current.

In the analytical relations for delay and energy, the carrier transit delay, and switching energy related to the transit delay of carriers through the FET channel are ignored as they are negligible compared to the RC delays and energies. The above relations clearly show that the read and write delay and energy of the 6T array structure depend on the critical capacitances related to the access transistors, although the wire capacitances of the word and bit lines also play a role. Therefore, it is highly desirable to have the access FETs replaced by some gateless devices, for instance, LETs (described in Chapter 3) with a different working mechanism as compared to gated FETs.

4.2.3 Peripherals and Assist Circuits in the SRAM Array

In a 6T SRAM array other than the core memory elements (the 6T bit cells along with the word and bit lines) there are various peripheral and assist circuitries that assist in the proper functioning (generating the timing signals, control signals, decoding and multiplexing the input and output signals etc.) of the whole SRAM array in writing data into the array, reading data from the array and storing data in the array. The various peripherals and assist circuits in a 6T array are shown in Figure 4.5 [86].

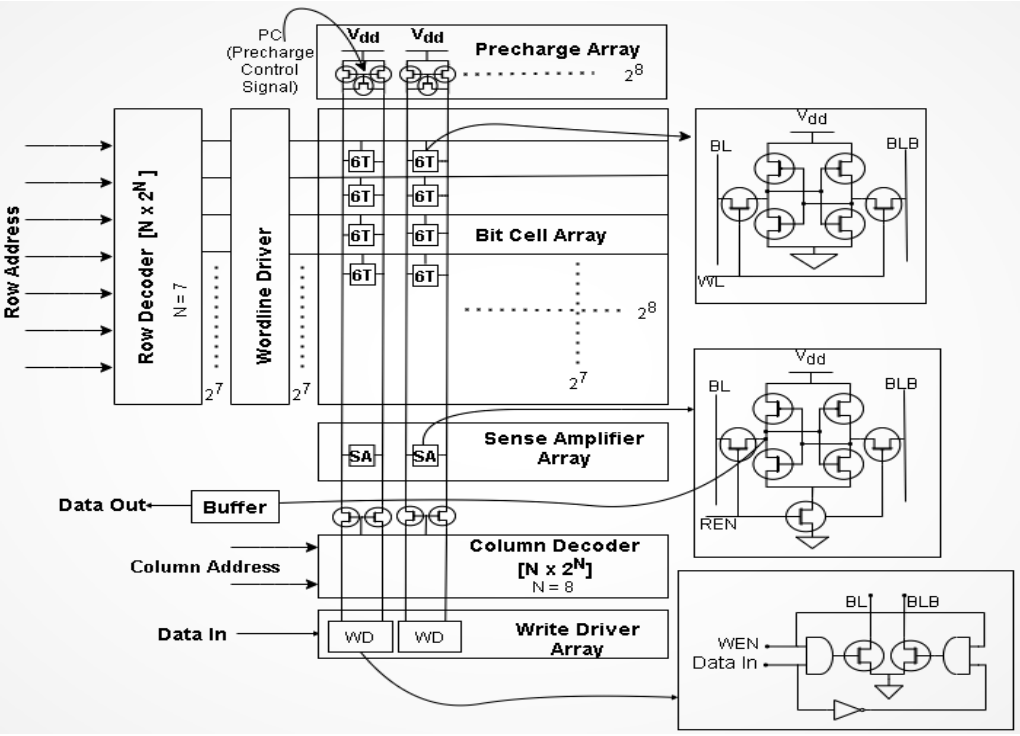


Figure 4.5: A 6T SRAM array with all the peripherals [86].

As can be seen from Figure 4.5 the main peripherals are a row decoder, word line driver, sense amplifier, write circuitry, a column decoder, and pre-charge circuitry [87, 88]. Even though the peripherals (some of them performing analog operations) may be more power hungry and with higher latencies than the core memory 6T cells, however, the number of such peripheral circuits needed for the array is much lesser as compared to the number of 6T cells, for instance only one sense amplifier per column is needed. So, for a 64 KB array, with 1024 columns and 512 rows a total of 1024 sense amplifiers will be needed, while the total number of 6T cells for the array will be ~ 524 x 10^3. Moreover, for the hybrid array the word line driver circuit block shown in Figure 4.5 will not be needed since the OWGs do not add to capacitive loading as will be discussed in Section 4.3.3. Also, it is to be noted that the number of active devices (FETs for the regular array) which predominantly contribute to the delay and energy consumption of the peripheral circuits are much (orders of magnitude in number) lesser as compared to the number of active devices in the core array. For instance, for an array of size 32 kb discussed in [89] the number of transistors needed in the decoder circuitry (which needs one of the highest numbers of active devices for logic operation, and is one of the most power hungry with the highest delay among all the peripherals) is around 546 [89] while for the same array size, the number of 6T cells will be 32 x 10^3 amounting to 192 x 10^3 transistors (each cell has 6 transistors) in the core memory array. Moreover, the same decoder (with 546 transistors) reported in [89] has an average delay and power consumption of the order of a few picoseconds (ps) and a few micro-watts (μW) respectively resulting in average energy consumption of the order of aJ (10^{-18} J) [89], while for the similar array size the average dynamic energy consumption in the core array elements (6T cells and the word lines and the bit lines) without considering the peripherals and also not considering the effect of leakage in the 6T cells is of the order of few tens of fJ (10^{-15} J) [14]. So even though individual peripheral circuits

maybe be more power hungry and have higher latencies than a single 6T cell, but in an array with large number of 6T cells and even larger number of active devices (6 transistors/cell) the energy and delay of the core array elements (6T cells, word lines, bit lines) is more predominant and has a much higher contribution to the overall delay/energy of the whole array circuit. So, ameliorating the delay and energy consumption of the core array elements by a large factor (by replacing the whole electrical word line with OWGs and removing the WL drivers as will be seen subsequently) even keeping the peripherals untouched is expected to improve the performance of the whole SRAM array by a major amount as will be seen in the next section.

4.3 6T Hybrid SRAM

In the hybrid 6T structure, the two access transistors (M5 and M6) in the 6T cell of Figure 4.2 are replaced by two LETs (L1 and L2), and the word line is replaced by the OWG that illuminates the nanowire in the LETs as shown in the prototype 6T cell of Figure 4.6 [14, 18, 19]. The LET has a very simple structure, with no polysilicon/metal gate embedded in a dielectric material which contributes to the oxide related part of the gate capacitance in FETs [85]; also no gate-drain or gate-source overlap capacitance, which also forms a part of the total gate capacitance and drain/source capacitance in gated FETs [85]. Though a thin oxide layer may be formed on the NW surface due to environmental oxidation, it does not contribute to any oxide related capacitance as in FETs, since there is no metallic gate electrode wrapping around the NW in a LET. Since the substrate in the LET just provides mechanical support without any electrical connection, there will also be no M-S junction to substrate capacitance which is equivalent to the drain-to-substrate or

source-to-substrate junction capacitance of conventional FETs in which the substrate generally has an electrical connection.

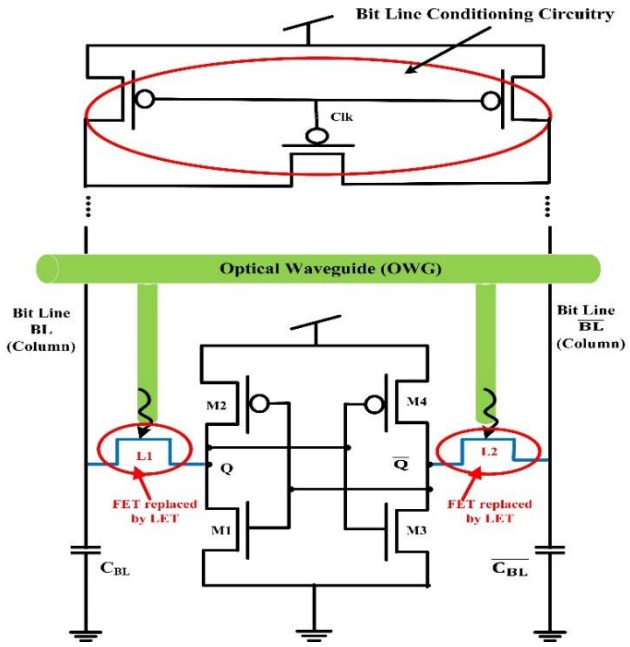


Figure 4.6: Prototype hybrid 6T SRAM cell with LET access [14].

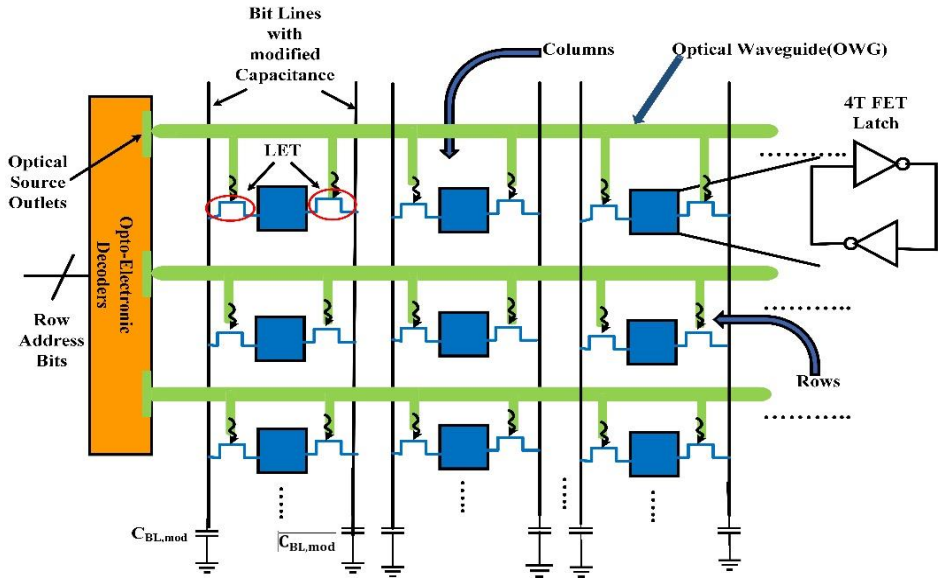


Figure 4.7: Prototype hybrid 6T SRAM array [14].

However, a very small M-S junction contact capacitance and capacitance due to the NW itself may be present which can be neglected for all practical calculations. For the analytical calculations in this chapter two separate LET based on generic semiconductor nanowires are considered: one with length (L) = 300 nm, diameter (D) = 50 nm, and another with L = 500 nm and D = 70 nm and drive currents of 5 µA and 25 µA, respectively (the plots in Figure 4.8 are considering the smaller LET with 5 µA drive current). A prototype hybrid 6T array is shown in Figure 4.7 [14] in which the FET access devices are replaced by LETs and electrical word lines (WLs) by OWGs, keeping the core FETs and other peripherals almost unchanged. The OWGs have to be illuminated by appropriate on-chip optical sources like nanoscale lasers [16] which form a part of the optoelectronic row decoding system.

4.3.1 Delay and Energy Estimation of the Hybrid SRAM Array

The LET structure has no M-S junction capacitance and hence the bit line capacitance for the hybrid array will predominantly consist of only the vertical wire capacitance. Therefore, Equation 4.3 can be modified as follows:

$$C_{BL,mod} = n_R(C_{wire,col}) \qquad (4.10)$$

The internal node (output node) capacitance given by Equation 4.5 may be modified as follows, where the drain equivalent capacitance of M5 ($C_{drain,M5}$) would not be present due to the same reason.

$$C_{out,mod} = C_{drain,M1} + C_{drain,M2} + C_{gate,M3} + C_{gate,M4} \qquad (4.11)$$

Also, most importantly, the hybrid 6T structure should not have any word line capacitance which for a regular 6T array depends on the gate capacitance of the access FETs and the capacitance of the electrical wordline. This is because LETs neither have any physical dielectric or metal gate nor any electrical wordlines to control the gates as in access FETs of regular 6T array. Instead, the light is brought in through an OWG that will contribute no practical delay or capacitance. To incorporate the effects of the LET access devices and OWGs in the hybrid 6T structure, delay, and energy Equations 4.6 – 4.9 for the regular structure are modified to Equations 4.12 – 4.15 for the hybrid array as follows:

$$T_{read,mod} = t_{WG} + max\left(\frac{C_{BL,mod}\Delta V_{read}}{I_{read,mod}}, t_{LET}\right) \qquad (4.12)$$

where $C_{BL,mod}$ is the modified bit line capacitance as shown in Equation 4.10, and $I_{read,mod}$ is the modified cell read current for the hybrid structure with LET access devices. The RC-word-line delay term (first term) in Equation 4.6 is replaced by the time taken by the EM signal to propagate through the optical waveguide (t_{WG}) and illuminate the access LETs, the second term in Equation 4.6 is modified to include the larger of the modified RC-bit line delay during read, and the LET carrier transit delay (t_{LET}) as discussed previously.

$$E_{read,mod} = 2n_C E_{op} + \max\left(C_{BL,mod} V_{DD} \Delta V_{read}, E_{el}\right) \qquad (4.13)$$

where the RC energy of the word line in the case of the regular array in Equation 4.7 will not be present because OWGs practically do not consume or dissipate any energy while the light is being transmitted through them. The first term in Equation 4.13 is due to the optical gating switching energy for a LET (E_{op}) described in Section 3.2.1, and for a whole row, it is multiplied by $2n_C$, since there is n_C number of 6T cells per row and each 6T cell has two access LETs. The second

term is the larger of the modified bit-line RC-energy during the read and the transit time electrical switching energy (E_{el}) for the LET access device.

$$T_{write,mod} = \max\left(t_{WG}, \frac{C_{BL,mod}V_{DD}}{I_{write,ckt}}\right) + \max\left(\frac{C_{out,mod}\Delta V_{out}}{I_{write,mod}}, t_{LET}\right) \qquad (4.14)$$

where $C_{out,mod}$ is the modified internal node capacitance and is described in Equation 4.11, and $I_{write,mod}$, is the cell write current for the hybrid 6T cell. The RC word line delay term (1st term in Equation 4.8) during the write operation is replaced by t_{WG}, and the first term in Equation 4.14 is the larger of the terms t_{WG} and the modified bit line delay during write, and the second term is the larger term of the modified 6T cell flipping delay during the write operation and the LET carrier transit delay (t_{LET}).

$$E_{write,mod} = 2n_C E_{op} + C_{BL,mod}V_{DD}^2 + \max\left(C_{out,mod}V_{DD}\Delta V_{out}, E_{el}\right) \qquad (4.15)$$

where the first term is identical to Equation 4.13, the second term in Equation 4.15 is the modified bit line RC energy during write, and the last term is the larger of the hybrid 6T cell modified flipping energy during write, and the transit time electrical switching energy of the LET access device.

4.3.2 Performance Evaluation of the Hybrid SRAM Array

Using analytical relations, Equations 4.6 – 4.9 and 4.12 – 4.15, a set of delays and energies for various 6T array sizes (256 bytes – 512 KB) are calculated for the regular array, hybrid array, and hybrid array with the ballistic LET access device. Note that in the energy expressions in Equations 4.7 and 4.9 for the regular 6T array and Equations 4.13 and 4.15 for the hybrid array, energy consumption due to leakage has not been considered, which will be discussed elaborately in Section 4.3.4. The various currents used in the analytical relations for the regular SRAM are

assumed to be 25 μA [90], $\Delta V_{read} \approx 120$ mV, and $\Delta V_{out} \approx V_{DD}/2$ [82]. For direct comparison, the various analytical results are plotted in Figure 4.8a – 4.8d, and the results for the 256 KB and 512 KB arrays are summarized in Table 4.1, from where it is evident that the hybrid array is capable of giving much better performance than the regular array even at lesser energy consumption. It is noted from the various plots of Figure 4.8, that though on a single device level the ballistic LET has much lesser carrier transit delay and switching energy as compared to the regular LET, the results for the hybrid arrays are coinciding. This is because for an array, the overall RC delay and energy will dominate over the carrier transit delay and switching energy of the individual LETs. In the plots of Figure 4.8, for increasing array sizes, both the number of cells along the word line (n_C) as well as the number of cells along the bit line (n_R) are increased, which is different from the case if the number of cells along the bit line is fixed to 512, where only the cells/word line will increase to meet the array size as discussed later in the chapter. As evident from Figure 4.8, the read delay and energy on average are improved by factors of 3 and 16 respectively, while the write delay and write energy on average are improved by factors of 2 and 3, respectively.

Analyzing the read delay equations for the regular (Equation 4.6) and hybrid (Equation 4.12) arrays it can be stated that the improvement is primarily due to the replacement of the large RC-word line delay in the regular structure by the much smaller optical waveguide delay (t_{WG}) in the hybrid structure. Also, the highest reduction achieved in the read energy is mainly due to the replacement of the large RC word line energy consumption in the regular array (Equation 4.7) by a much smaller optical gating energy term (E_{op}) in the hybrid array (Equation 4.13).

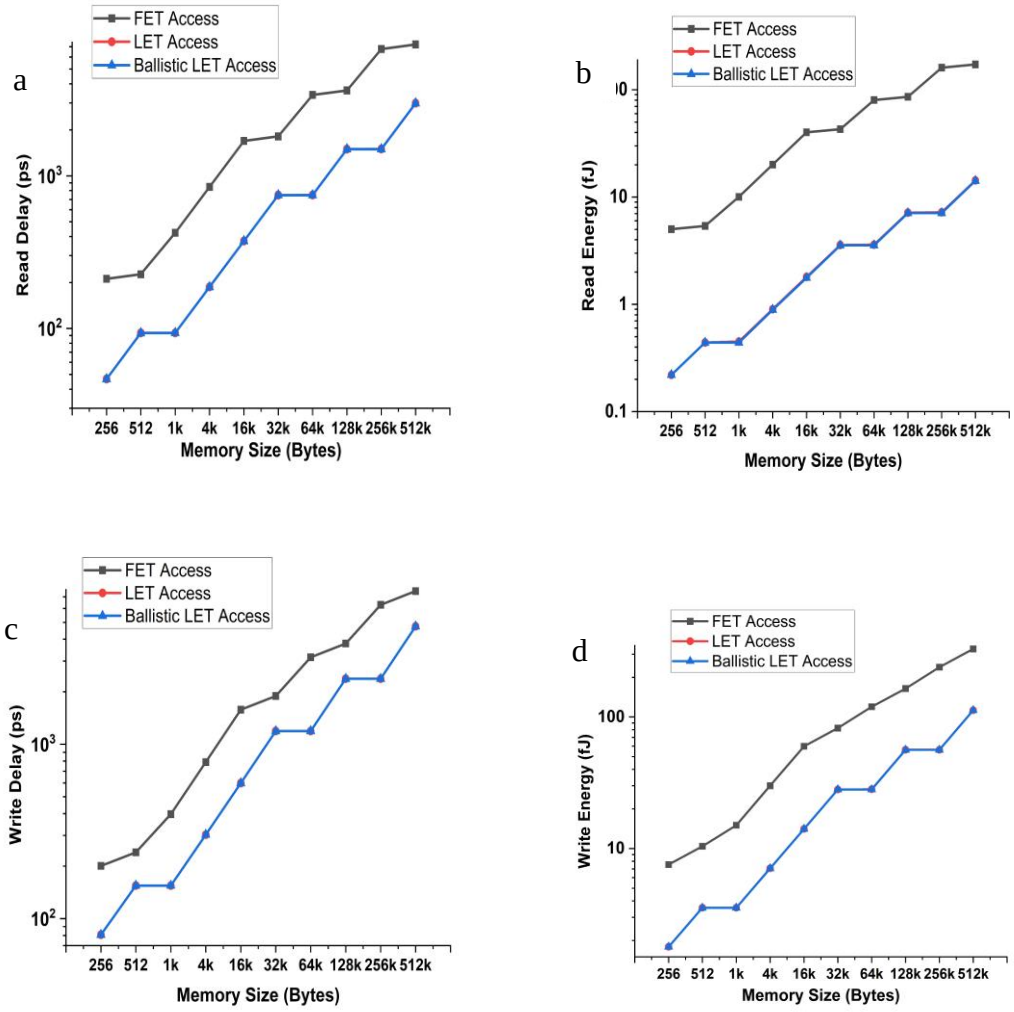


Figure 4.8: Read and write delay and energy for various SRAM arrays with FET, LET, and ballistic LET access devices. (a) Read delay, (b) read energy, (c) write delay, (d) write energy. The curves with LETs and ballistic LETs are indistinguishable.

Table 4.1 Comparison of various performance metrics of 256 – KB and 512 – KB 6T SRAM array with FET, LET and ballistic LET access devices

	256 - KB SRAM array			512 - KB SRAM array		
	FET access devices	LET access devices	Ballistic LET access devices	FET access devices	LET access devices	Ballistic LET access devices
Read delay (ps)	6768	1496.8	1495.8	7244.7	2991	2990
Write delay (ps)	6295.3	2372.7	2372.7	7552.1	4738.5	4738.5
Read energy (fJ)	160.7	7.2	7.1	172.1	14.3	14.2
Write energy (fJ)	239.1	56.32	56.2	328.8	112.5	112.4

So, the ultra-small carrier transit delay (high switching speed) and extremely low switching energy of individual LETs do not affect much the overall delay and energy of the array Also as seen from plots of Figures 4.8a and 4.8c, the improvement in write delay is lesser compared to read delay because the first max term in Equation 4.14 shadows the effect of replacing the RC word line delay with t_{WG}. Similarly, as evident from plots of Figure 4.8b and 4.8d, the improvement in the write energy for the hybrid structure is lesser than the read energy, because $V_{DD} > \Delta V_{out} > \Delta V_{read}$, and thus $C_{BL,mod}V_{DD}^2 > max(C_{BL,mod}V_{DD}\Delta V_{read}, E_{el})$ in Equations 4.15 and 4.13 respectively.

Moreover, the kinks in the plots of Figure 4.8 (and the EDP plot of Figure 4.9) are related to the array configurations (number of rows and columns) considered in the calculations because those properties have different sensitivities in varying the row and column size. For instance, considering the read delay plot (Figure 4.8a), values for the 256 B and 512 B array in the case of

the regular structure are similar because for both cases the number of columns n_C = 32 (and n_R differs by a factor of 2) and hence the C_{WL} values are same as evident from Equation 4.1. Now from the read delay expression in Equation 4.6, the first term dominates (since $C_{WL}V_{DD} > C_{BL}\Delta V_{read}$ and the current value are considered the same), and hence for both cases, the read delay values are similar (differ by only about 6%), as the first term in Equation 4.6 are same, while the slight increase is due to the greater 2nd term in Equation 4.6 in case of the 512 B array as n_R doubles. While for the hybrid array, as seen from Equation 4.12, the read delay is dominated by the second term (since t_{WG} term is very small), and hence the delay value increases with n_R (t_{LET} term is also very small) as evident from the Equation 4.12, and the delay remains similar for two arrays with same n_R values (for instance 512 B and 1 KB hybrid arrays). Other kinks in the delay and energy plots for both the regular and hybrid array can be similarly explained.

The overall delay and energy consumptions of the SRAM array with either FET or LET access devices can be modeled as in Equations 4.16 and 4.17 [82], where $T_{array(FET/LET\ access)}$ is the overall delay of the SRAM array with FET or LET access devices, $T_{read(FET/LET\ access)}$ and $T_{write(FET/LET\ access)}$, are respectively, the read and write delay of the SRAM array with FET or LET access devices. Similarly, $E_{array(FET/LET\ aceess)}$ in Equation 4.17 is the overall switching energy consumption of the SRAM array with FET or LET access devices (note energy due to leakage has not been considered here and will be discussed in Section 4.3.4), $E_{read(FET/LET\ access)}$ and $E_{write(FET/LET\ access)}$ are, respectively, the read and write energy of the array with FET or LET access devices. β = 0.5 is the ratio of the read accesses to the total accesses, which is the number of times a 6T array is accessed for the read operation compared to the total number of times the array is accessed in a full cycle.

$$T_{array(FET/LET\ access)} = \max\left(T_{read(FET/LETaccess)}, T_{write(FET/LETaccess)}\right) \quad (4.16)$$

$$E_{array(FET/LET\ access)} = \beta E_{read(FET/LET\ access)} + (1-\beta)E_{write(FET/LET\ access)} \quad (4.17)$$

The figure of merit (FOM) of the SRAM array can be found from the energy-delay product (EDP) as shown by Equation 4.18 [82]:

$$EDP_{array(FET/LET\ access)} = \alpha E_{array(FET/LET\ access)}.T_{array(FET/LET\ access)} \quad (4.18)$$

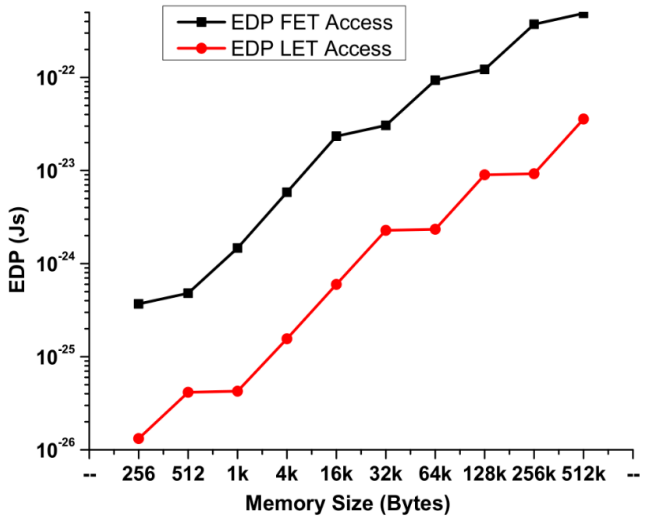


Figure 4.9: EDP for various SRAM arrays with FET and LET access devices [19].

Considering 50% probability (α = 0.5 is the array activation factor) of the array being accessed in a cycle, and 50% probability for each of the read and write operations [82], and using Equations 4.16 through 4.18, the EDPs (not considering leakage energy) for both the regular and hybrid arrays are calculated and plotted in Figure 4.9 for various array sizes [19]. It can be roughly

estimated from the plot that the hybrid SRAM array on average exhibit more than one order of magnitude lesser EDP, as compared to the regular SRAM arrays.

Considering a larger drive current (25 μA, 5 times the previous case) and larger device dimensions (L = 500 nm, D = 70 nm) for the access LETs in the hybrid structure, it has been found that the improvement in the read delay is drastically increased (almost by a factor of 5) as compared to the case of using lesser drive current for LETs. The average improvement in the case of write delay is almost the same since for large arrays it is predominantly dependent on the current from the write circuitry; while there is a very slight increase in the average read and write energies due to the increase of the transit time electrical switching energy (E_{el}) and optical gating energy (E_{op}) per LET device, and consequently, the average EDP also increase slightly with larger LET drive current and LET dimensions.

Moreover, in larger 6T arrays, the bit line length is generally capped to a maximum of 512 cells/column, because of the increasing bit line loading which slows down the sense amplifier [91]. In such a case the word line length must be longer to accommodate the necessary number of 6T cells to meet a specific memory size (for example for a 128 KB array, if the number of 6T cells along the bit line is 512, then there will be 2048 cells along the word line). However, if the word line becomes too large (generally > 1024 cells/WL) then for a conventional SRAM array, it will lead to deteriorating performance, since it will further increase the capacitive load over the already high capacitance of the word line, leading to more increase in the delay and the energy of the regular array. Then, the common practice is to memory banking as discussed in [91, 92] In the case of the hybrid 6T array capping the number of cells/bit line to 512 and elongating the word line length will not much affect the delay and energy since for the hybrid array there will be OWGs along the word lines, which even elongated by tens or hundreds of microns will only slightly

increase the delay since OWGs practically do not contribute to any capacitance and the optical signal travels almost at the same order of magnitude as the speed of light (more accurately the group velocity of the waveguide). Using Equations 4.6 – 4.9 and 4.12 – 4.15 and capping the number of cells/bit lines to n_R = 512 and considering array sizes 32 KB – 2MB or n_C = 512 – 31,250, a set of delays and energies are plotted for the regular and the hybrid array as shown in Figure 4.10. All the parameters are assumed to be exactly same as used in the analytical expressions to plot Figure 4.8, except the cells/bit lines are fixed to a maximum of 512.

Analyzing the delay and energy plots of Figure 4.10, it is found that using the hybrid array is more advantageous in case the number of cells/bit line is fixed to a certain number while the number of cells/word line is increased accordingly This is because for a regular array considering a planar layout (without any array partitioning or memory banking [91, 92]) as the word line length is increased, keeping the bit line length fixed to 512, the C_{WL} term increases in Equations 4.6 – 4.9 (n_C increases in Equation 4.1) while the C_{BL} term remains constant. Hence the delays and energies for the regular array given by Equations 4.6 - 4.9 increase linearly with the increase of the 6T array size which is solely due to the increase of the number of cells/word line as seen in Figure 4.10. While for the hybrid array increasing the number of cells/wordline (n_C increases, while n_R is constant and set to 512) increases the length of the OWG, which does not increase any capacitive loading, but only slightly the t_{WG} term in Equations 4.12 – 4.15. For the read delay of the hybrid array (Figure 4.10a) the slight increase in the delay for higher memory sizes is mainly due to the increase of the t_{WG} term in Equation 4.12 which becomes significant for very long OWGs, while for the write delay (Figure 4.10c) the curve is almost flat due to the max terms in Equation 4.14 which takes the larger of the two terms.

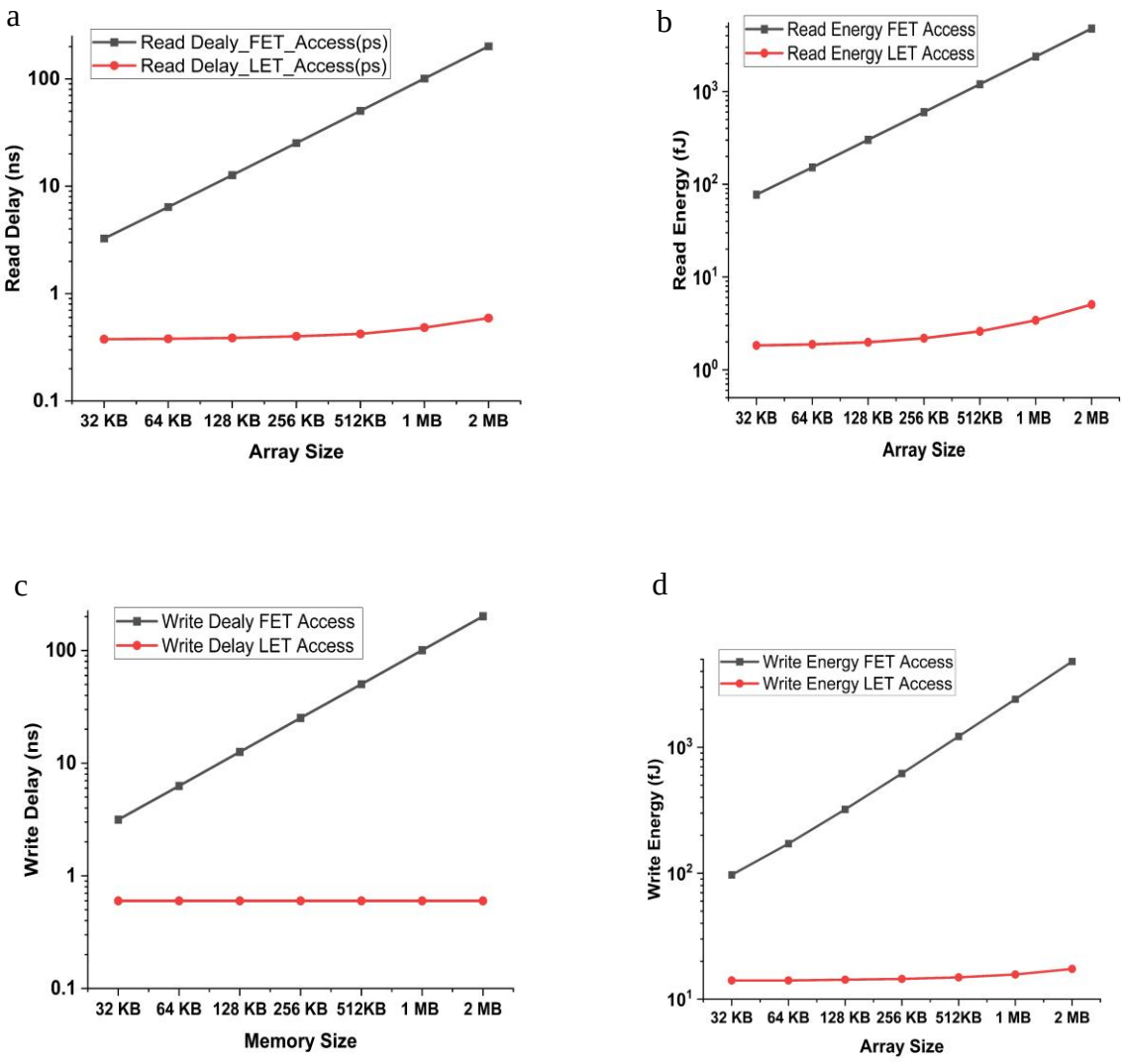


Figure 4.10: Read and write delay and energy for various SRAM arrays with FET, LET access devices and a maximum of 512 cells/bit line. (a) Read delay, (b) read energy, (c) write delay, (d) write energy.

For the read and write energies of the hybrid array (Figures 4.10b and 4.10d respectively) the curves slightly increase for higher array sizes, due to the increase of the first term ($2n_C E_{op}$) in Equations 4.13 and 4.15 which only becomes significant for a very large number of hybrid cells/word line, while the other terms are constants since the bit line length is fixed. It is to be noted from Figure 4.10 that for the hybrid array the delays and energies do not increase much even with increasing the array size from 32 KB to 2 MB, which can be a huge design advantage for larger arrays, which gives room to design large arrays without much penalty in delay or energy consumption.

Although the length of the OWG is not an issue from the signal delay point of view, other considerations will limit the practical length of the OWG, which will be discussed in Chapter 5. For a large capacity array (e.g., 2 MB), the OWG opening numbers will become very large. It is possible and in fact preferred to reduce the effective optical wordline opening numbers and thus length by grouping multiple cells of the same wordline together under the same OWG opening, which will be discussed in the Section 4.3.5. Beyond that, a similar approach as adopted for the conventional SRAM array might be necessary to limit the OWG length.

4.3.3 Probable Effects on the Peripherals

In this section, the effects of the hybrid SRAM structure on word line driver circuitry, which is a chain of CMOS buffers of increasing size as shown in Figure 4.11 of the 6T array, are analyzed. In the hybrid structure, since the access LETs have a different turn-on mechanism, electrical word lines are replaced by OWGs, and hence large electrical word line drivers to drive long electrical word lines are not needed, which not only minimizes the extra circuitry but also reduces the word line capacitance (note that the output capacitance of the buffer stages also add up to the total word

line capacitance if WL drivers are considered during the read/write delay and energy calculations) and RC- energy consumption to almost negligible. For the hybrid array without the electrical wordlines and drivers, the equivalent of the RC-WL delay and energy will be the light propagation delay (t_{WG}) through the OWG, and the total optical gating energy consumption of a whole 6T array row, when all the LETs are simultaneously illuminated by the OWG.

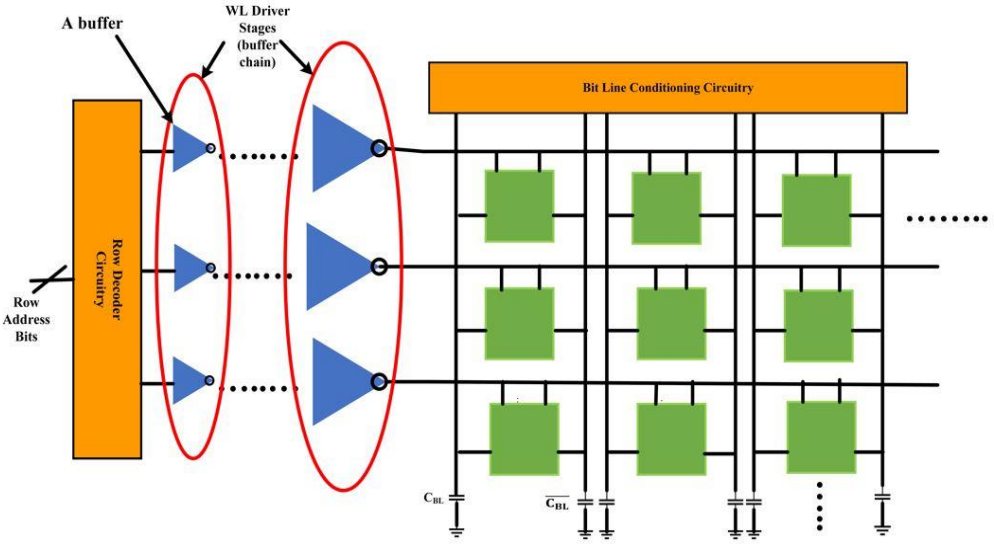


Figure 4.11: Conventional 6T SRAM array with word line driver buffers.

It can be roughly estimated as shown in Figure 4.12a that for the regular array with WL drivers, the RC-WL delay ranges between a few tens of ps to hundreds of ps over various array sizes (256 bytes – 512 KB), while for the hybrid array the equivalent delay approximately ranges between one-tenth of a ps to few ps, which gives on an average almost more than two orders of

magnitude reduction in the WL equivalent delay in case of the hybrid array. Similarly, from Figure 4.12b, the WL energy consumption with WL drivers for the regular array ranges between a few fJ to tens of fJ, while for the hybrid array the equivalent optical energy consumption is between one-hundredths of fJ to one-tenth of fJ, which gives on an average almost three orders of magnitude reduction in the WL equivalent energy consumption in the hybrid structure. Also, it may be possible to replace the three p-FETs of the bit line conditioning circuitry as shown in Figure 4.2 with LETs, which will reduce the bit line capacitances and hence bitline-related delays and energy

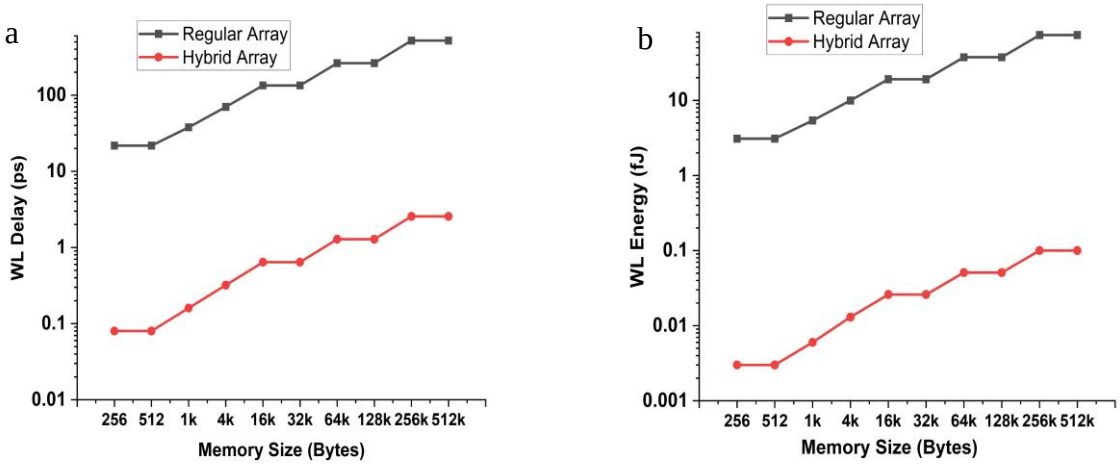


Figure 4.12: (a) Word line delay (b) word line energy
for the regular array with WL - drivers and the hybrid SRAM array.

4.3.4 Leakage and Possible Improvements

On the single component level, the off currents in a FET predominantly depend on the supply voltage, the threshold voltage, channel length, channel doping profile, drain and source junction depth, and gate oxide thickness [93-95]. Various types of leakage currents in a conventional n-FET are shown in Figure 4.13 [93] which include: sub-threshold leakage current (I_{sub}), gate-

induced drain and source leakage current (I_{GIDL}, I_{GISL}), punch-through leakage current ($I_{punchthrough}$), gate tunneling leakage current through the bulk (I_{GB}), source (I_{GS}) and drain(I_{GD}) summed up as, $I_{gate} = I_{GB} + I_{GS} + I_{GD}$, and p-n junction leakage currents ($I_{junction} = I_{drain,junc} + I_{source,junc}$) at the drain-substrate junction ($I_{drain,junc}$) and the source-substrate junction ($I_{source,junc}$) [95]. Thus, the total leakage current of an individual FET in the 6T SRAM cell may be empirically modeled as the sum of gate, subthreshold, and junction leakage currents.

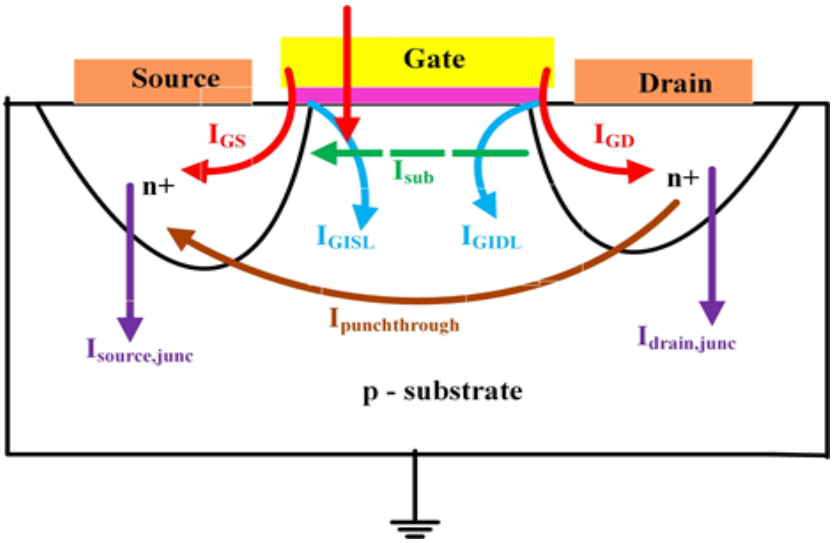


Figure 4.13: Leakage mechanism in a MOSFET.

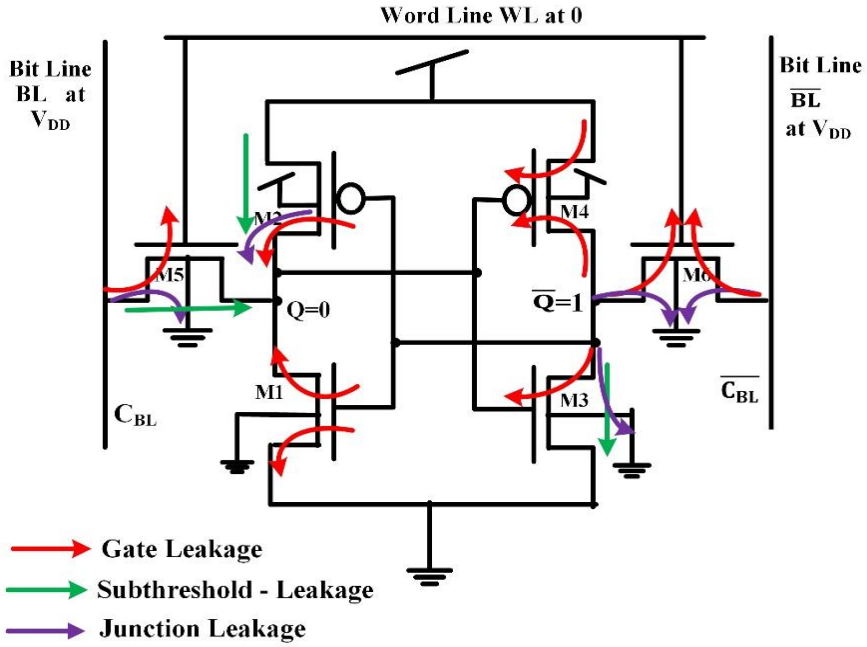


Figure 4.14: Leakage currents in a conventional 6T cell just prior to a read or write operation.

The leakage in a 6T cell depends on the logic state of the cell, the logic level of the word line, and the type of operation performed. In Figure 4.14, the 6T cell shown is in the state just before the read or write operation (reading 0 or writing 1) [94]. Both the bit lines BL and $\overline{BL}$ are precharged to V_{DD}, but the word line WL is still at 0, and M5 and M6 are off, and hence subthreshold leakage may occur in the access devices. The arrows in Figure 4.14 show the various leakage currents in each FET depending on their operating conditions (drain, source, gate, substrate voltages, and conduction state). For instance, M5 is off (gate is at 0), the drain is at 1, and the source and substrate are at 0, and hence there will be a component of the gate leakage from drain to the gate (I_{GD}), sub-threshold leakage (I_{sub}) from drain to source and a component of

junction leakage ($I_{drain,junc}$) from the drain to the substrate as shown in Figure 4.14. Similarly, for M6, the gate is at 0, the drain and source are at 1 and the substrate is at 0, and hence there will be two components of the gate leakage (I_{GD}+I_{GS}) from the drain and source to the gate, and the junction leakages ($I_{junction}$=$I_{drain,junc}$+ $I_{source,junc}$) from the drain and source to the substrate as shown in Figure 4.14. There will be no I_{sub} between the drain and source since both are at logic 1. It is to be noted that the energy consumption due to these leakage currents, will add to the total switching energy consumption of the whole array given by Equation 4.17 to give the overall energy consumption of the array including leakage. If these leakages are severe, it may lead to a false read or write operation and affect the reliability of the 6T cell Analyzing Figure 4.14 it can be qualitatively estimated that about 40 % of the total number of leakage components in a 6T cell are in the access paths.

The hybrid 6T structure showing the various leakage components is shown in Figure 4.15, where the access LETs L1 and L2 are initially off such that the 6T cell is in the hold condition. It can be seen there are almost no leakages in the access paths except the subthreshold leakage in L1.

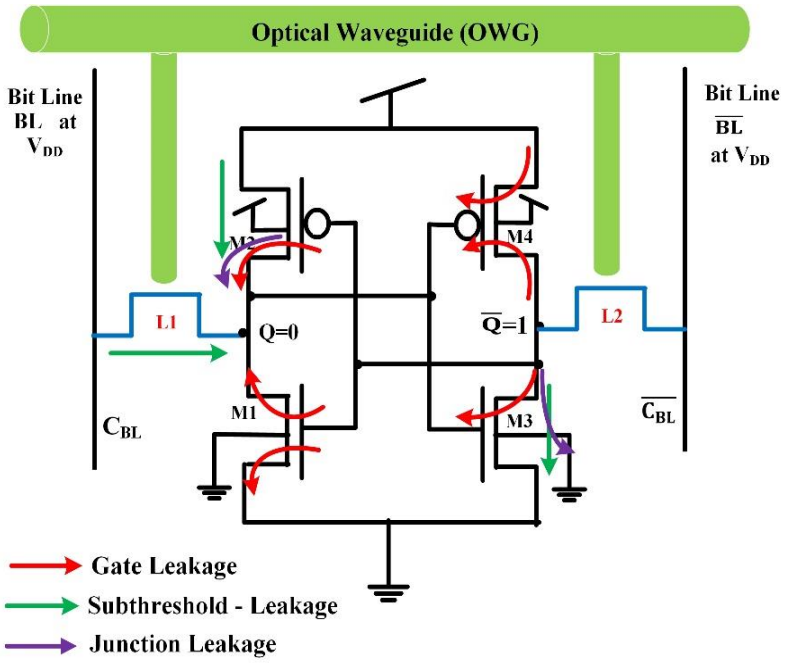


Figure 4.15: Leakage currents in a hybrid 6T cell just prior to read or write operation.

LETs have a different turn-on mechanism and no SCEs as discussed previously and have minimal subthreshold leakage (e.g., an off current as low as 10^{-13} A at a V_{ds} of 30 mV for the ballistic device in Section 3.2.2, and an off current of the order of 1 pA at a V_{ds} of 1.43 V and an off the power of 1.5 pW even for a large LET device discussed in [13]), and hence hybrid 6T cells will have almost negligible subthreshold leakage in the access paths. Gate tunneling leakage current is one of the most critical sources of leakage in FETs as device dimensions are scaled down and ultra-thin gate oxides are used [93-95]. Gate leakages (independent of the conduction state of the device) in FETs in the access paths, as shown in Figure 4.14 increase the total leakage energy consumption of a 6T cell and more severely in an array having a large number of 6T cells. In the hybrid structure, there will be neither any gate related nor any SCE-induced leakage, in the access paths as shown in Figure 4.15 and so the leakage power consumption in the hybrid cell will be much reduced and

will be more beneficial for an array that has many such 6T cells. Also, junction leakage occurs across the p and n junctions to the ground (formed between the source, drain, and substrate regions) in FETs [95] in the access paths (as shown in Figure 4.14), which severely increases the leakage power consumption in arrays that have a large number of such p-n junctions to ground. Since LETs do not have any such p-n junctions or paths to the ground (the insulating substrate does not have any electrical connection and only provides mechanical support), the hybrid 6T cell and the array will have no junction leakage in the access paths as shown in Figure 4.15. So, considering no gate and junction leakages, but still having subthreshold leakage (the dark current in the LETs) in the LETs in access paths, (as shown in Figure 4.15), there will be an overall reduction of roughly about 35 % in the total number of leakage current components in a single hybrid 6T cell, which will be more advantageous in case of a hybrid 6T arrays which have a large number of such 6T cells.

4.3.5 Proposal of a Novel Integration Scheme for the Hybrid 6T SRAM Array

The hybrid structure shown in Figure 4.7 presents an intimate integration of both electronic and photonic components to operate synergistically as a system. For the layout of the hybrid array, both LETs and FETs can be laid out together on a single layer (the electronic layer) along with the electrical bit lines, and the OWG along with the optical sources can be placed on a different layer (the photonic layer) above the electronic layer leading to a 3D stacking (integration) structure as shown in the prototype 3D structure of Figure 4.16. As seen in Figure 4.16, the OWGs in the photonic layer are placed parallel to each other (just like electrical wordlines in the regular arrays) with many openings into the electronic layer to illuminate the LETs depending on the signal from the optoelectronic decoder, such that when a particular OWG is illuminated it shines light on all

the LETs in that particular row through the openings into the electronic layer. It is to be noted that in the schematic shown in Figure 4.16 the OWGs are shown along with the multiple openings just for clarity and a better understanding of the 3D integration scheme. However, the OWGs will have a square or rectangular cross-section, and neither the OWGs nor the openings will be visible since the whole OWG structure will be embedded inside a dielectric layer very close to the electronic layer with just the openings not enclosed inside the dielectric layer. A more realistic picture of the OWG system and the photonic layer is shown in Figure 5.19 of the next chapter.

We also propose a novel scheme to increase the illumination efficiency of the LETs from the OWG openings. From a typical SRAM array operation, when a word line is switched on, all the access devices in that row are turned on, so to increase the illumination efficiency for the hybrid array, which is fundamentally related to the size mismatch between the light wavelength and the electronic components, four (or possibly more) LET access devices from two (or more) adjacent hybrid 6T cells in the same row can be grouped together and simultaneously illuminated from a single OWG opening as shown in Figure 4.17 and the cross-sectional view of Figure 4.18 [18].

This scheme not only minimizes the illumination loss from each OWG opening into the electronic layer, and the total chip area but also drastically reduces the number of OWG openings by a factor of 4 (because 2 LETs/cell) per row. Since photonic properties are scalable with wavelength, and hence for the LETs operating in visible wavelengths, the OWG dimension can be made significantly small (e.g., to around 200 nm cross-section at 405 nm illumination as will be seen in the next chapter) which enables on-chip integration of the OWG with electronic components.

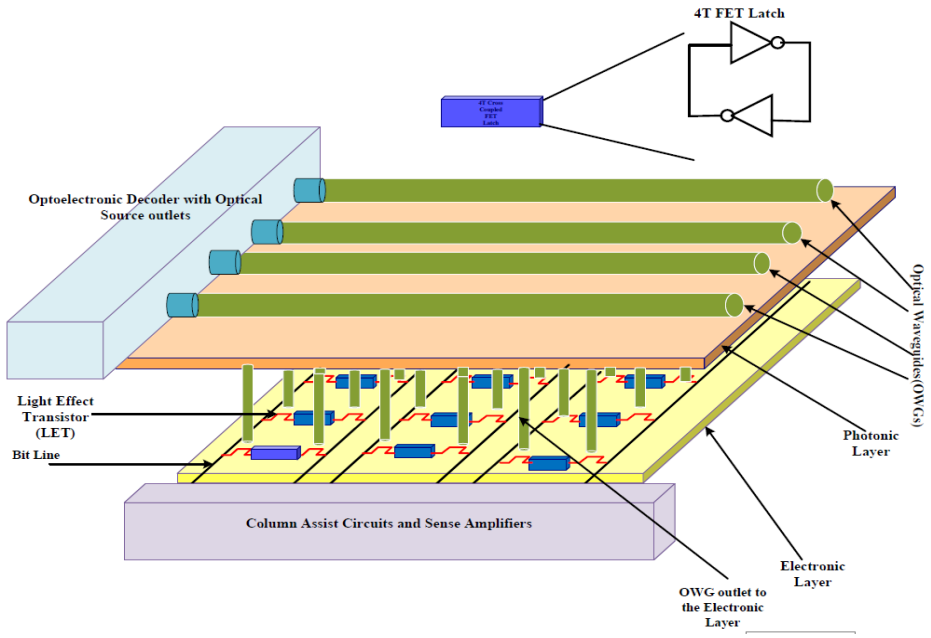


Figure 4.16: A prototype 3D integration scheme for the FET-LET hybrid 6T SRAM array.

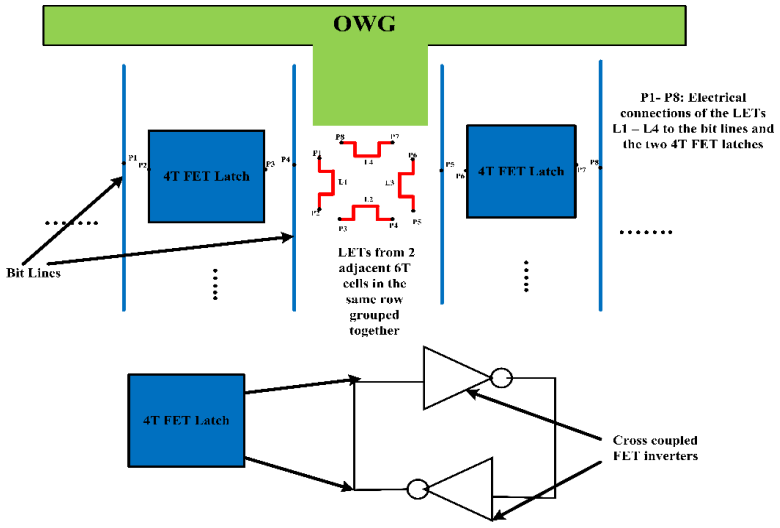


Figure 4.17: A 2D schematic of the hybrid 6T array layout with 4 LETs grouped together and illuminated for a single OWG opening [18].

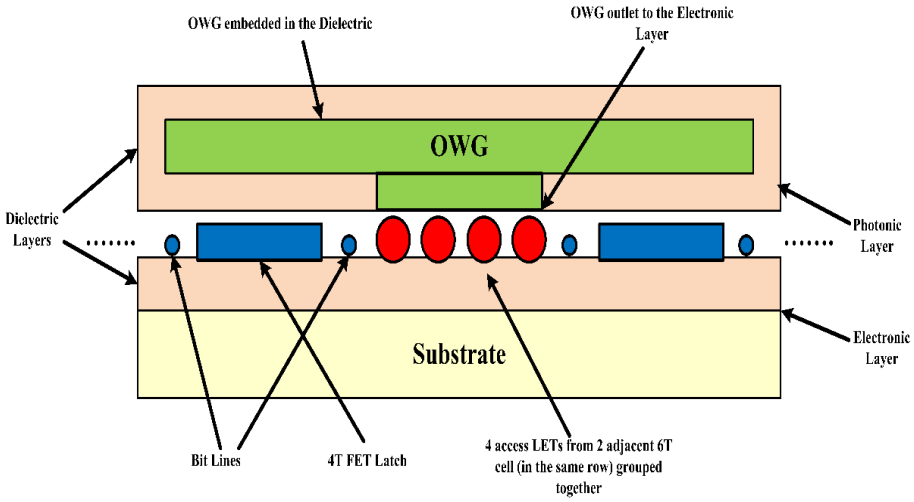


Figure 4.18: A cross sectional view of the novel integration scheme showing the electronic and photonic layers and the 4 LETs from 2 adjacent 6T cells grouped together and simultaneously illuminated [18].

4.3.6 Compatibility with CMOS and Scalability

In electronic-photonic integrated circuits, there are various ways for integrating the optical transport layer in a standard CMOS system, out of which possibly the most promising approach would be the use of hybrid (3D) integration of the optical layer above a complete CMOS integrated circuit, where the basic CMOS process flow would remain the same since the optical layer can be fabricated independently [96]. For a few years now heterogeneous integration of Si electronics with electronic and photonic components/structures has been carried out where the photonic components are made from compound semiconductors and other dielectric materials that are compatible with the standard with CMOS process flows [30, 97, 98]. For instance, the necessary technologies have largely been demonstrated for different applications, like in the hybrid InGaAs/SiGe 6T SRAM [99], where the two InGaAs access transistors can be replaced with LETs,

and $LiNbO_3$ photonic waveguide cavity on Silicon [100] which all can be easily transferred to the proposed new electronic-photonic hybrid integration scheme.

In the context of a 6T SRAM array, for a typical circuit layout, the word-line spacing is generally of the order of 2 poly pitches, which is of the order of 200 nm for the 22 nm technology node and 100 nm for 7 nm technology node [101, 102]. OWGs fabricated on an insulating substrate can be scaled to achieve subwavelength lateral size, and can be made to have very low loss, for instance, a Si waveguide of width 400 nm for light at 1.55 μm can have loss as low as 2.8 dB/cm [103]. For the LETs operating in visible wavelengths, the OWG dimension can be significantly reduced (e.g., 200 nm at 405 nm illumination), since photonic properties are scalable with wavelength. Further miniaturization is possible by using plasmonic-dielectric hybrid waveguides, though the loss in such a case may be somewhat higher [97].

For cases where the space requirement is not very stringent, but SRAM performance is of paramount importance, larger waveguide spacing can easily be allowed. Since OWGs are typically designed for interconnection in photonic circuits for inter-chip or intra-chip they are long, while in the hybrid SRAM, the optical paths will be substantially shorter for on-chip operation. Thus, for the OWG structure, it will not be a problem to cover hundreds or even one thousand cells/WL and can illuminate them efficiently as will be seen in Chapter 5. For illuminating an OWG, the minimum light power output required from the optical decoder can be estimated to be in the order of only 76.5 μW per OWG for 1024 cells/WL, considering a propagation loss of 2.8 dB/cm, and an overestimated OWG length of 1 mm (the actual OWG length for 1024 cells will be lesser than 1mm, signifying lesser optical power requirement than estimated), and using the optical gating power estimate of ~ 35 nW/LET (for the ballistic LET) from Section 3.2.2. This leaves a large room even for less efficient implementation or absorption of optical energy even with a large loss.

4.4 Conclusion

In this chapter, the analytical designs of the regular and hybrid 6T SRAM array have been described in detail. The main advantage of the hybrid 6T array over the regular array from replacing the FET access devices with LETs is that the gate, source, and drain related capacitance for the FETs, and the electrical wordline are no longer present, which removes the word line delay and reduces the energy consumption. From the above delay and energy plots of the regular and hybrid 6T SRAM, it can be concluded that the new hybrid 6T SRAM array is much more energy efficient with lesser read and write delays than the regular 6T array. Moreover, it was also found that in case the bit line length is capped to a maximum of 512 cells, the performance of the regular 6T array worsens as the word line length has to be very large to accommodate for the memory size. However, in such a case, the performance of the hybrid array is almost not affected (while the performance margin gets better) since increasing the OWG length neither affects the delay much nor affects the capacitive loading at all. In addition, LETs are expected to have much lower leakage currents (LETs only have the ref which is equivalent to the subthreshold leakage in FETs) than conventional FETs, and thus the hybrid 6T cell and the array will have much lower leakage power dissipation compared to the regular arrays. Also, in terms of affecting the peripherals, the use of OWG waveguide-based architecture abolishes the need for any electrical wordline drivers, which will drastically reduce the total word line capacitance, RC-delay, and energy consumption to almost negligible compared to that in the conventional SRAM array. Thus, the proposed hybrid SRAM architecture offers an example of a hybrid electronic–photonic integrated circuit with both electronic and photonic devices playing active roles synergistically.

CHAPTER 5 Design of a Low Loss Optical Waveguide

This Chapter reused some of the contents from the article below:

Reprinted with permission from *A. Pal, Y. Zhang, and D. D. Yau, "Light Effect Transistors for High-Speed and Low-Energy Electronic and Photonic Integrated Circuits," in 2021 IEEE Research and Applications of Photonics in Defense Conference (RAPID), 2-4 Aug. 2021 2021, pp. 1-2, doi: 10.1109/RAPID51799.2021.9521451.*

5.1. On Chip Electronic Photonic Integration

On-chip electronic–photonic integration refers to the placement of purely electronic components like FETs, resistors, capacitors, etc., and optoelectronic components like photodetectors, on-chip lasers, and purely passive optical components like couplers, waveguides, etc. inside the same die package such that the combination functions as a system-on-a-chip (SOC) as shown Figure 5.1 [8]. Many common optical devices are implemented by using hybrid integration technologies. However, as the physical characteristics (such as thermal expansion coefficient, and lattice constants) and packaging requirements of the materials are different, the optimal materials used for active and passive optical and optoelectronic devices are not the same, which makes it very complicated to integrate multiple discrete components made from different materials and ensure reliable device performance as a whole, especially in the implementation of the large-scale electronic-photonic integrated circuits [8, 9], even more challenging for the single-functional-unit level integration of electronic and photonic elements [14]. While in a monolithic photonic integration scheme, various active and passive electronic and optoelectronic components are made from one material or combination of the materials with similar properties (from the same group), for example, III-V (e.g., InAs/GaAs) or II-VI (e.g., CdTe/CdSe) compound semiconductors such

that there are no adaptation issues between different materials. Compared to the integration of different materials together for on-chip electronic-photonic applications like III-V or II-V devices on silicon/germanium (group IV) substrates, monolithic electronic–photonic integration of similar materials like silicon photonic devices on group IV substrates have advantages in terms of energy-saving and reliability [8, 104, 105].

Past efforts of electronic photonic integrated circuits (EPICs) are largely limited to using photonic components for exchanging data/information between electronic sub-systems, for instance, providing communication between the CPU and Memory Banks [2]. The incorporation of photonics into bulk silicon CMOS chips using a layer of polycrystalline silicon deposited on silicon oxide islands fabricated alongside transistors is described in [8]. In [8] a photonic platform was directly integrated with a 65-nanometre-transistor bulk CMOS process technology in a 300 mm diameter wafer microelectronics foundry and then a high-speed optical transceiver was implemented in this platform that operated at ten gigabits per second. By decoupling the formation of photonic devices from that of transistors, the integration approach described in [8] can achieve many of the goals of multi-chip solutions, but with the performance, complexity, and scalability of systems on a chip. We instead explore EPICs with a higher-level integration - a single-functional-unit level integration of electronic and photonic elements [14].

Among the various monolithic or hybrid integration schemes available, the use of silicon-based electronic and photonic components for SOC applications as well as optical transmission are the most popular due to the versatility of silicon (also other group IV elements) in the electronic chip manufacturing industry [105]. Silicon photonics utilizes the optical properties of the group IV semiconductor (mainly silicon) and involves the design and fabrication of devices for generating, manipulating, detecting, and transmitting light. Silicon photonic devices can be made

using existing semiconductor fabrication techniques, and because silicon is already used as the substrate for most integrated circuits, it is possible to create hybrid devices in which the optical and electronic components are integrated into a single microchip [8, 104]. Silicon Photonics is compatible with CMOS (electronic) fabrication, which allows silicon EPICs to be manufactured using established foundry infrastructure.

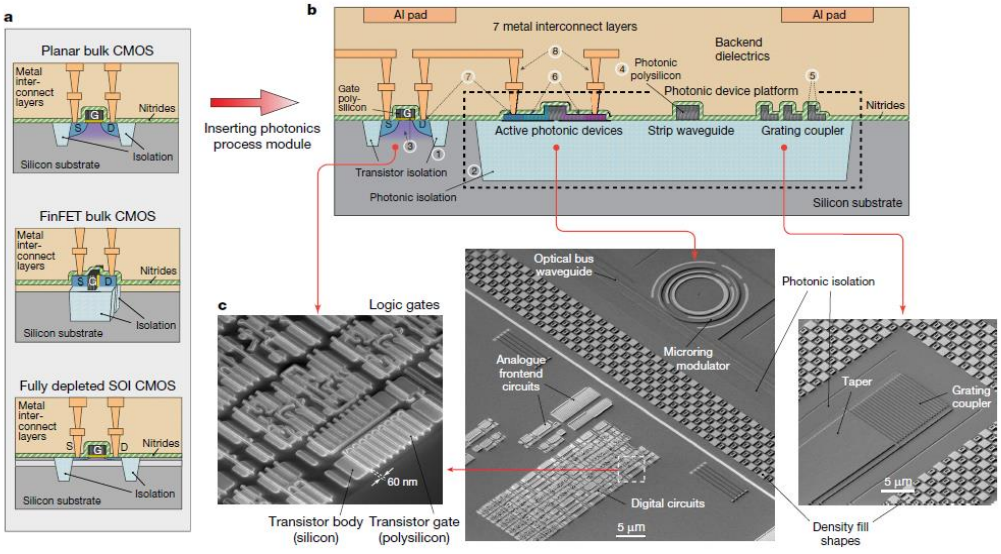


Figure 5.1: Integration of a photonics process module into planar bulk CMOS with photonic devices implemented in an optimized polysilicon film (220 nm) deposited on a photonic trench filled with silicon oxide (about 1.5 µm). The numbers indicate major fabrication steps in the order appearing in the process [8].

Given the physics of photonics, older CMOS nodes can be perfectly suitable for pattern and fabricating photonic devices and circuits. Waveguides, the interconnects between photonic devices in the circuit, are made with a silicon core and come in different styles: for instance, a rib

or strip that has the oxide from the SOI substrate as bottom cladding and air or another layer of silicon oxide as top cladding [8, 104]. The light is transported in these waveguides. Given the material properties of the silicon, only a certain range of wavelength (below its bandgap, not in the visible spectrum) signals can be transported without significant losses. Nowadays, silicon photonic PIC processes often include additional waveguides built from silicon nitride as the core material, this opens the ability to carry wavelengths over a wider range, including visible light. Light sources (lasers, the "power supply" of photonic circuits and systems) are today impossible to manufacture with silicon due to the indirect bandgap of the material. For light to be efficiently generated, a material needs to have a direct bandgap, and various techniques exist to integrate III-V materials and or complete lasers in the Si photonics wafer (chip) to drive the photonic components within the photonic circuits [106]. The monolithic silicon photonics integration provides photonic circuits with low parasitic capacitance, reduced power consumption, improved reliability, and better portability, with the industrial feasibility for mass production.

5.2 Silicon Nitride Waveguides for Silicon Photonic Integrated Circuits

The silicon nitride (Si_3N_4/SiN) waveguide platform has enabled a broad class of low-loss planar-integrated devices and chip-scale solutions for on-chip photonic integration, which benefit from transparency over a wide wavelength range (300 nm – 2350 nm) and fabrication using the standard CMOS wafer-scale process [104, 107, 108]. Though basic Si_3N_4 waveguide structures with silica cladding were demonstrated as early as the 1970s, integrated Si_3N_4 photonic devices were first demonstrated in the 1990s [107, 109]. In the last two decades, the development of Si_3N_4 photonics has achieved a synergy of low waveguide loss (compared to III-V or Si waveguides) and compactness (compared to SiO_2 planar optical circuits) that is attractive for a wide variety of

applications. Several key demonstrations of Si_3N_4 photonic integration are summarized in Figure. 5.2 [109], highlighting the evolution of three different integration schemes, i.e., monolithic passive integration, hybrid active integration, and heterogeneous active integration. The main advantages of silicon nitride over silicon waveguides are its broader transparency window down to UV wavelengths, a range not accessible with the other platforms, no suffering from two-photon, and free carrier absorption over the telecommunication wavelength ranges and easier for 3D monolithic integration [104, 107].

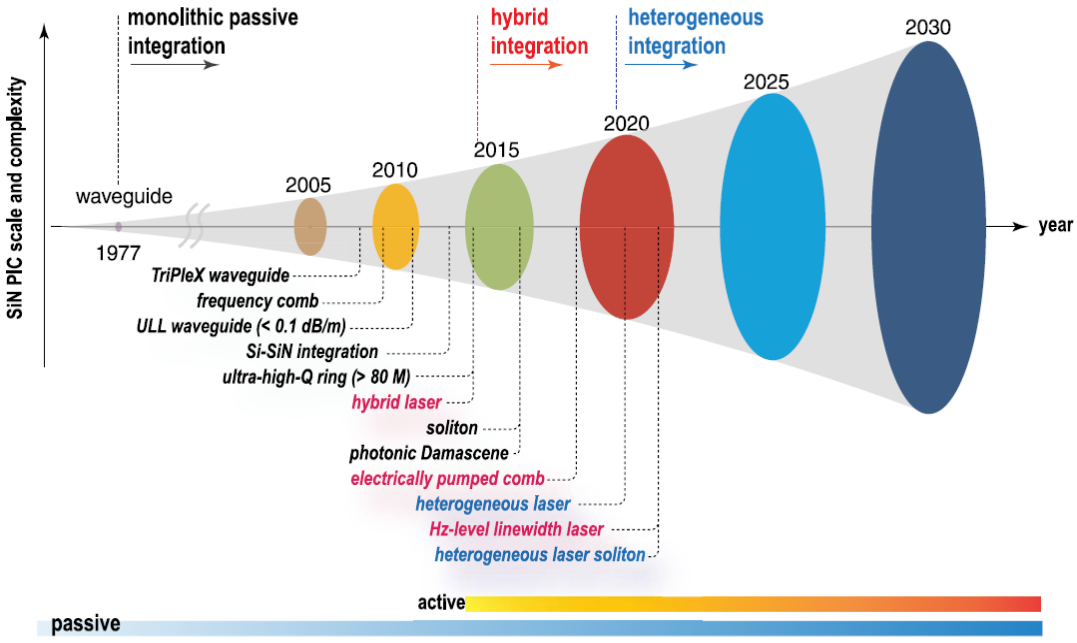


Figure 5.2: Progress of silicon nitride-based photonic integration with key demonstrations labeled with the release year [109].

As a complimentary platform to silicon-on-insulator (SOI) and III–V photonics, Si_3N_4 waveguide technology along with its low propagation loss as well as low bending loss and signal dispersion as shown in Figure 5.3 [109] opens a new generation of system-on-chip applications not achievable with the other platforms alone. The availability of low-loss waveguides (<1 dB/m) [107] that can handle high optical power can be engineered for linear and nonlinear optical functions, and that support a variety of passive and active building blocks opens new avenues for system-on-chip implementations. As signal bandwidth and data rates continue to increase, the optical circuit functions and complexity are made possible with Si_3N_4

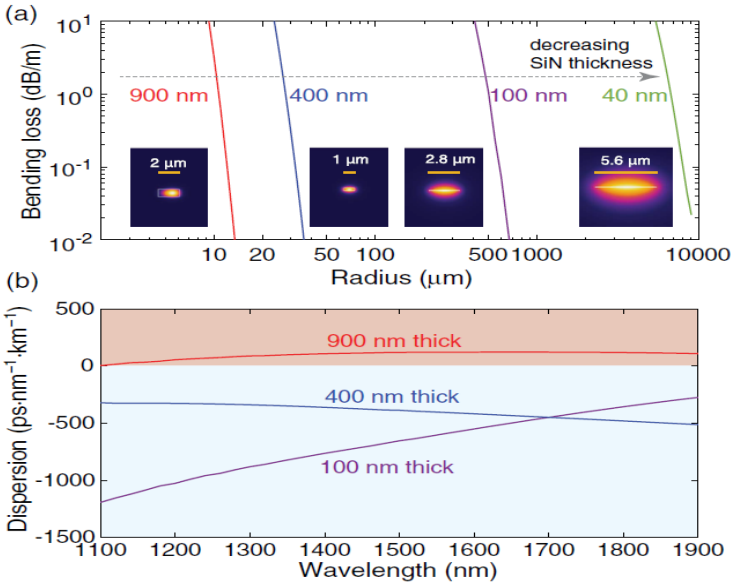


Figure 5.3: (a) Si_3N_4 waveguide bending loss versus bending radius of the fundamental optical mode for four different Si_3N_4 core thicknesses. Insets show the mode profiles for each waveguide geometry with negligible bending loss at 20 µm, 50 µm, 1 mm, and 10 mm respectively. (b) Waveguide dispersion (spreading of the optical pulse in time per unit wavelength band width and per unit propagation distance) for waveguides with Si_3N_4 core thickness and width selected from (a) [109].

has expanded the practical application of optical signal processing functions that can reduce energy consumption, size, and cost over today's digital electronic solutions. Today, SOI offers large volume photonic integration through traditional complementary metal–oxide semiconductor (CMOS) infrastructure. Traditional SOI photonics employs high-contrast waveguides formed from a silicon core surrounded by oxide cladding, keeping the light tightly confined to the core. These strongly confining waveguides lead to very compact photonic circuits with small bend radii and moderate waveguide losses on the order of 0.1 dB/cm [107, 109]. The widely used group III–V photonics material indium phosphide (InP) is a foundry scale process that provides waveguides with optical gain and efficient signal modulation in telecommunications wavebands [106]. InP is used in many standalone PIC applications and as a gain block for SOI PICs with a tradeoff in higher waveguide losses (0.4 to 2 dB/cm) and larger bend radii, as compared to SOI [107]. Si_3N_4 PIC technology provides lower loss waveguides and

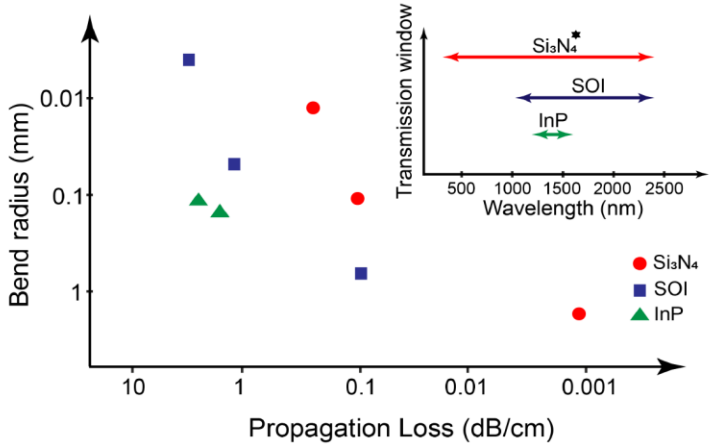


Figure 5.4: Bend radii, propagation loss, and window of transparency for Si_3N_4, SOI, and InP waveguides [107].

building blocks complimentary to SOI and III–V PICs [104, 107, 109]. Si_3N_4 is traditionally used in standard CMOS processes to insulate individual transistors, known as local oxidation of silicon (LOCOS), and is also used as gate material in ion-sensitive field-effect transistors (ISFETs) purposes [107]. Optical waveguides employ a core layer of Si_3N_4 embedded in a surrounding silicon dioxide (SiO_2) cladding material. The refractive indexes at 1.55-μm wavelength of the cladding (1.04 for SiO_2) and core (2.02 for Si_3N_4) allow for designs that range from low- to high-contrast waveguides with low propagation losses in the range of 0.3 dB/cm to 1.0 dB/cm over the wavelength range from $\sim$400 to – 2350 nm [107]. In general, the waveguide loss and minimum bend radius are design trade-offs based on desired performance, footprint, and optical power density, and vary for each integration platform. Figure 5.4 summarizes the data on waveguide propagation loss, minimum bend radius, and wavelength operating range for Si_3N_4, SOI, and InP waveguides [107].

5.3 Design of Si_3N_4/SiO_2 Low Loss Optical Waveguide

This section describes the design of a low loss Si_3N_4 optical waveguide embedded in SiO_2 dielectric which serves as the cladding material. For the design of the waveguide structure with a rectangular or square cross section, either a channel type cross section or a rib ridge type [104, 110] cross-section can be chosen from the Synopsys *RSoft CAD* photonic design suite as shown in Figure 5.5 below [110].

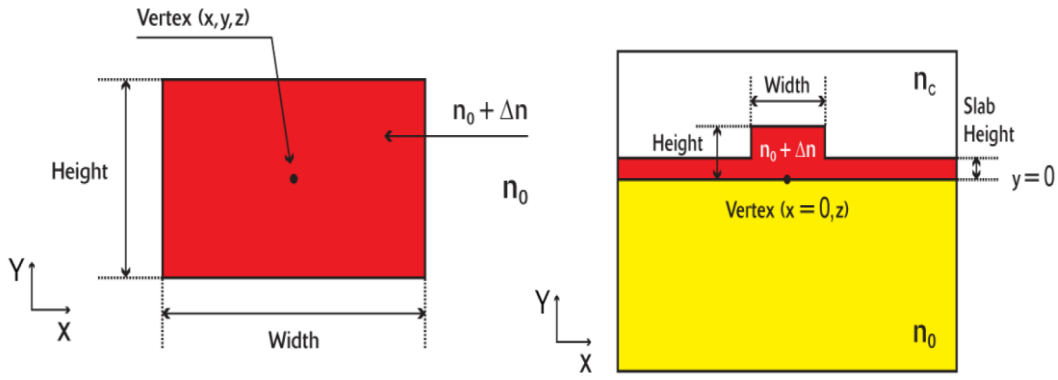


Figure 5.5: Channel type (left) and rib ridge type (right) OWG cross section structure in Synopsys *RSoft* CAD [110].

The designed OWG structure has a rectangular/square channel type cross section (the cross-section dimensions will be discussed subsequently) with a length comparable to the word lines in a regular 6T array such that the OWGs can illuminate the whole row of the hybrid 6T array structure shown in Figure 4.5 of chapter 4. For a large 512 KB array, with the number of hybrids 6T cells along the word line n_c = 1024 and the overestimated width of each hybrid 6T cell to be ~ 1 µm, the total required length of the OWG to illuminate all the cells in a row will be 1024 µm. Moreover, if we consider a 64 KB SRAM array (L1 caches are typically of the size of tens to a few hundred KBs) with n_c = 512, then the total length of OWG required is 512 µm. Also, considering a different array layout where we cap the number of cells/bit line (column) to 512 (as discussed in Section 4.3.2) then for such a layout, considering a 64 KB array, n_c = 1024 will again need a maximum OWG length of 1024 µm. In the conventional SRAM, the word line size n_c is typically kept below 1024 cells/word line by using memory banking (array partitioning), a 3D stacking technique where large arrays are divided into multiple memory banks and stacked together [91, 92], and only the particular bank that contains the required data is accessed [91, 92],

which may also be adopted for the OWG based word line if needed. Thus, it is evident that theoretically, the maximum possible OWG length will be of the order of 1100 µm, though in reality, it will be much lesser. In this design, we will simulate the maximum possible OWG length of 1100 µm that may be needed for the hybrid array.

For the novel 3D integration scheme discussed in Section 4.3.5 and [18], the OWGs should have multiple openings such that each opening should be enough wide to illuminate the group of 4 LETs from two adjacent SRAM cells [18]. The access LET dimensions considered as discussed previously are 100 nm (length) x 30 nm (diameter) and each OWG opening cross-section should fully illuminate 4 of them placed together as a group as discussed in Section 4.3.5. Also, to avoid interference and cross-talk the minimum distance between two adjacent metallic word lines in the conventional SRAM should be at least 2 poly pitches which are around 200 nm for the 22 nm technology node [102]. For the hybrid SRAM, enough spacing is required to avoid interference between the adjacent OWGs. Moreover, to avoid interference between optical energy coming out from two adjacent OWG openings into the electronic layer, the openings should be placed far enough from each other and the minimum distance between two adjacent OWG openings can be roughly estimated from Figure 5.6 [18].

The minimum opening between two adjacent OWG openings (center-center) as seen in Figure 5.6 is given by:

2(1/2 (each opening width)) + 2(distance between OWG edge and bit lines) + 4(spacing between 4T latch and bit line) + 2(width of each 4T cell) + (spacing between the two-bit lines of two adjacent cells) = 2(opening_width/2) + 2(2d_BL_4Tlatch) + 4(d_BL_4Tlatch) + 2(w_4Tlatch) + d_BL.

Where, opening_width = the width of each OWG opening = 300 nm (for one of the cases)

d_BL_4Tlatch = minimum spacing between the 4T FET latch and the electrical bit line = minimum contact spacing = 1.4λ = 30.8 nm for 22 nm technology (λ is 22 nm) [111].

w_4Tlatch = width of the 4T cross coupled latch in 22 nm technology, and considering the FET dimensions for the hybrid 6T cell and layout from [111] it is ~ 400 nm

d_BL = is the minimum spacing between two metal bit lines = metal pitch = 2.8λ = 61.6 nm for 22 nm technology [111].

Plugging in the above-mentioned values the center-to-center distance between two adjacent OWG openings = **1.5 µm,** which is used in the design of the structure in *RSoft CAD.*

The OWG is designed in Synopsys *RSoft* Photonic Design Suite and considering a channel type OWG cross-section [110] where the core Si_3N_4 OWG is enclosed in a SiO_2 dielectric which serves as the cladding and the Si_3N_4-SiO_2 provides good confinement to the light of wavelength 405 nm (the most commonly available short-wavelength semiconductor laser based on InGaN) used for simulation. The refractive index profile of Si_3N_4 with respect to the wavelength of light is shown below in Figure 5.7 [110].

Material loss (absorption by the material) depends on the imaginary part (dotted line as shown in Figure 5.7) of the refractive index (RI), and the imaginary part of RI for Si_3N_4 is almost zero for any wavelength > 300 nm as seen in Figure 5.7, and hence for our wavelength of interest (blue light of 405 nm), there is no material absorption (loss), while for wavelength below 300 nm Si_3N_4 is highly absorptive as λ nears the band gap energy for Si_3N_4.

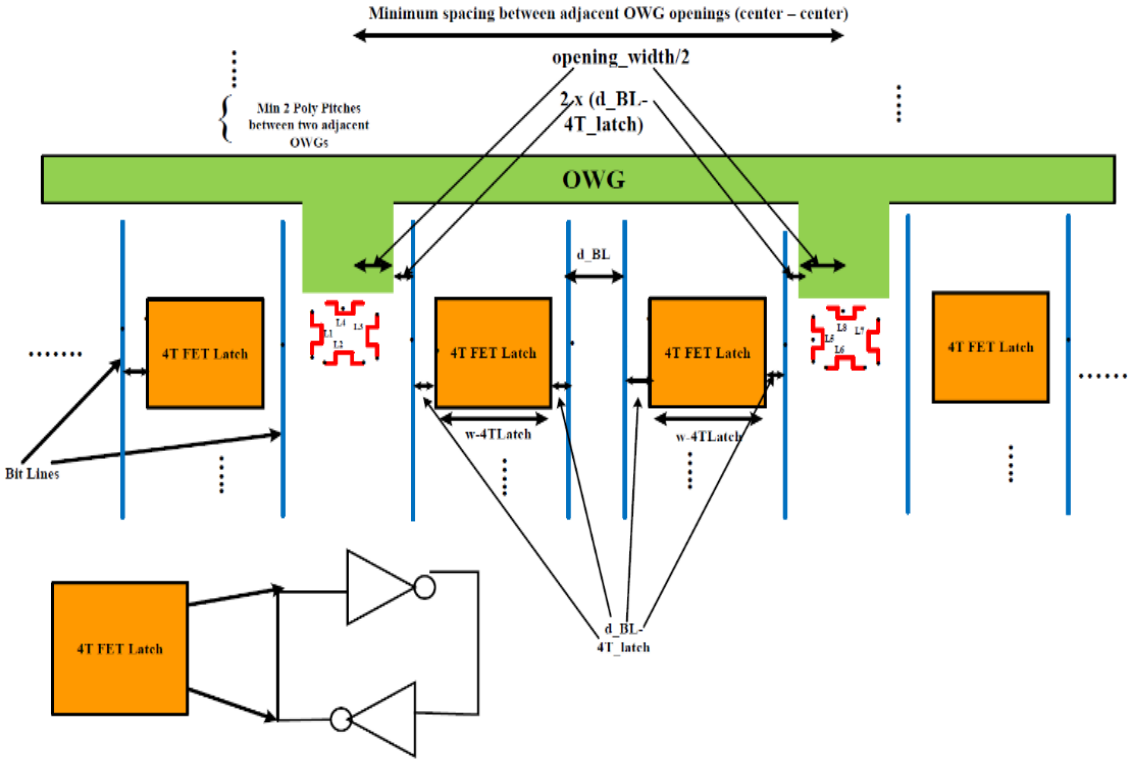


Figure 5.6: 2D schematic of portion of the hybrid 6T array layout showing minimum distance required between two adjacent OWG openings.

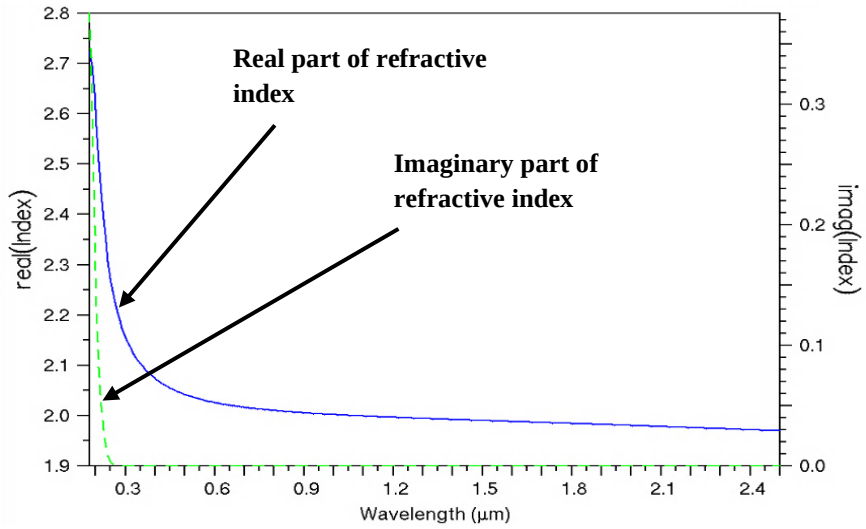


Figure 5.7: Refractive index profile (real and imaginary) of Si_3N_4 with variation of optical wavelength [110].

The schematic of the simulated OWG is shown in Figure 5.8 and the simulation has been carried out in the *Beam-Propagation simulation engine* [110] to capture the energy transfer in the OWG along the propagation direction well as the energy coming out from the various OWG openings as shown in Figure 5.8. OWGs of length 1100 µm and three cross sections dimensions of 200 nm x 200 nm, 400 nm x 400 nm, and 800 nm x 800 nm., were considered for the simulation, with opening cross sections of about 120 nm x 120 nm for the first case, and 300 nm x 300 nm for the last two cases to bring out light to illuminate the LETs.

The Si_3N_4 OWG core structure shown in Figure 5.8 is fully encapsulated by a SiO_2 cladding layer such that only the openings through which light comes out into the electronic layer are not enclosed as shown by the YZ and XY cross-section of the encapsulated OWG structure in Figure 5.9 [18].

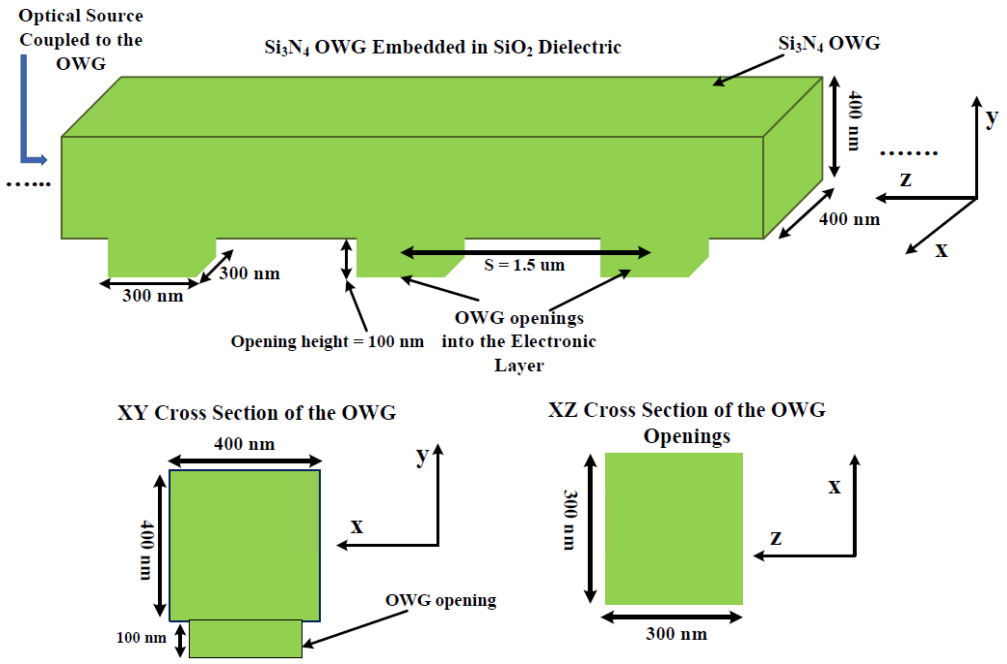


Figure 5.8: 3D schematic of the OWG structure showing the cross section and the openings (not drawn to scale) perpendicular to the direction of light injection.

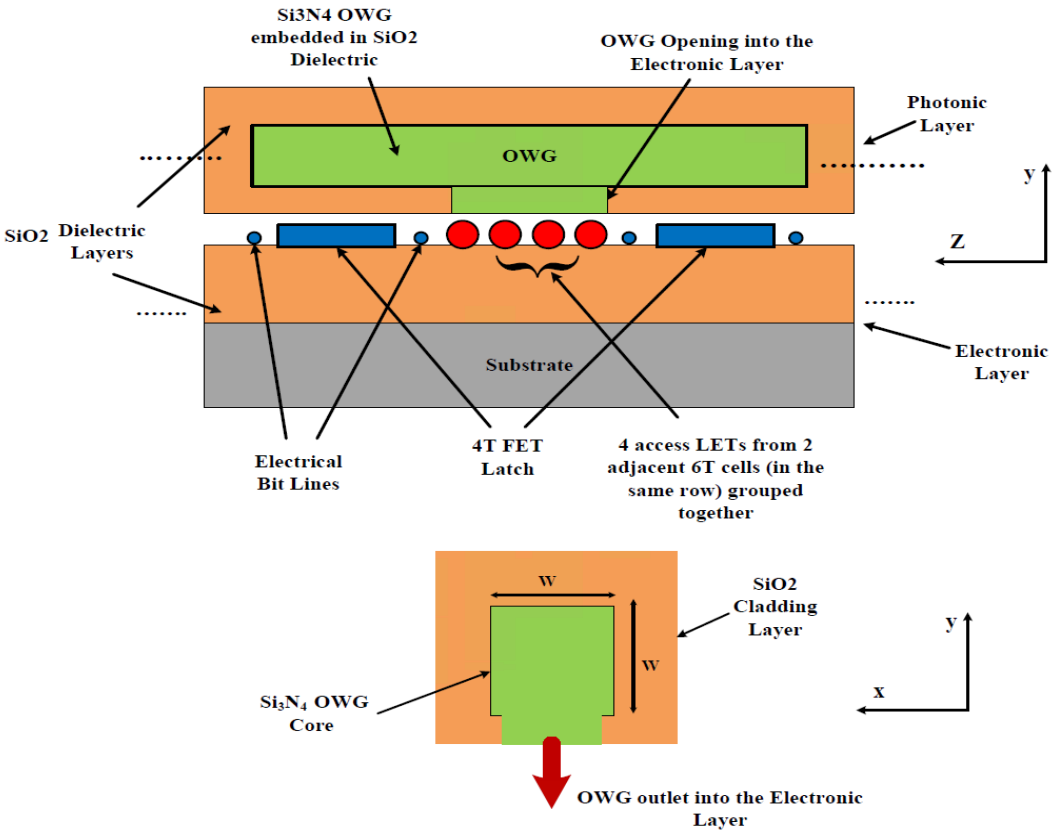


Figure 5.9: The YZ and XY cross sections of the hybrid structure showing the SiO_2 encapsulating the Si_3N_4 OWG.

5.3.1 Simulation of the Si_3N_4/SiO_2 OWG

Simulation results for the 400 nm x 400 nm cross section OWG

Light is injected into the OWG structure along Z – the direction of light propagation, while the OWG openings are perpendicular to the XZ plane i.e., perpendicular to the direction of propagation as shown in Figure 5.8. A Gaussian incidence beam is assumed with a beam width equal to the component width (that is 200 nm, 400 nm, and 800 nm cross-section OWGs) by default in the simulation engine [110]. As seen in Figure 5.10, the optical energy propagation.

through the OWG along Z without the OWG openings is almost nonattenuated in magnitude, i.e., almost all the incident energy propagates through the OWG, emerging from the other end of the waveguide. The small loss is caused by the leakage and some coupling loss between OWG and the optical source. With the OWG openings, as seen in Figure 5.11, the optical power along Z falls as light is coming out through the OWG openings, which is very much essential to illuminate the LET group of LETs in the layer beneath.

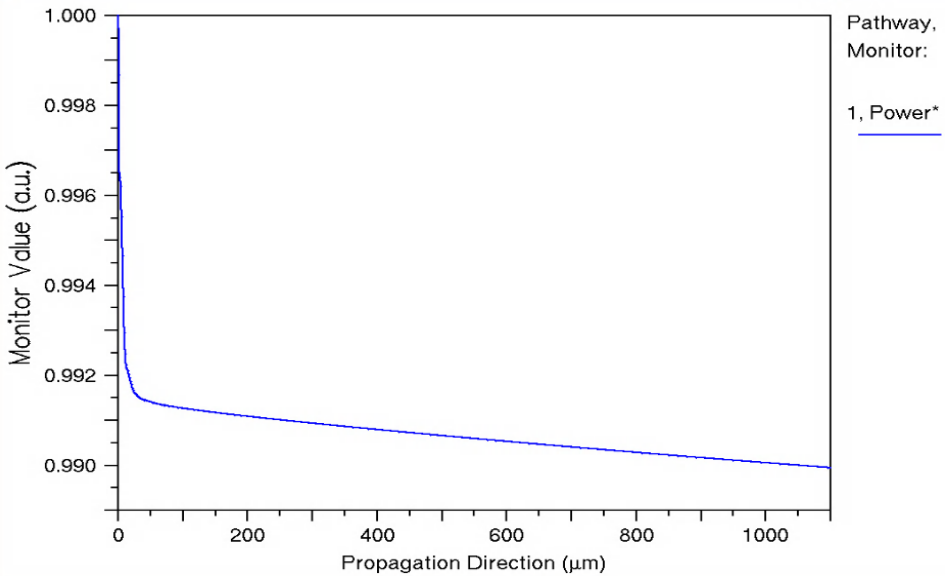


Figure 5.10: Optical energy propagation through the 400 nm OWG along Z without the OWG openings.

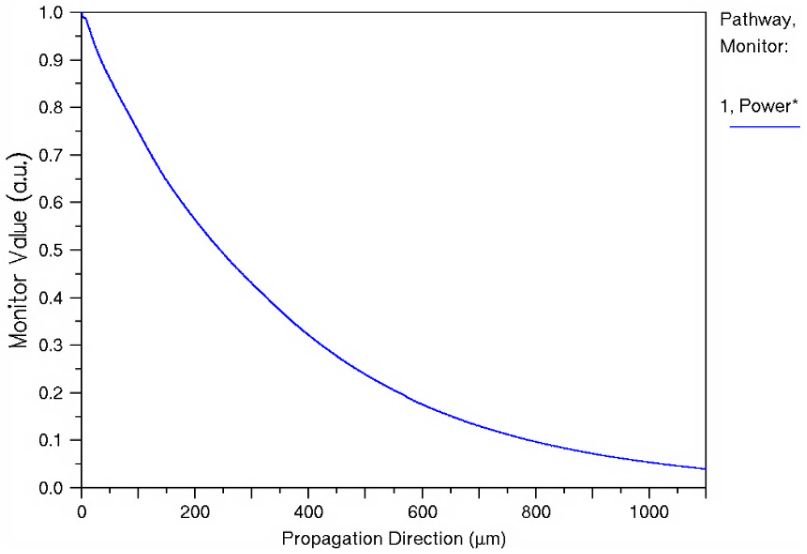


Figure 5.11: Optical energy propagation through the 400 nm OWG along Z with the OWG openings downward into the XZ plane. The power along Z falls as light is coming out through the OWG openings.

Figure 5.12 shows the fundamental mode profile of light propagating through the OWG which shows that the optical energy is very well confined inside the Si_3N_4 core (when there is no opening).

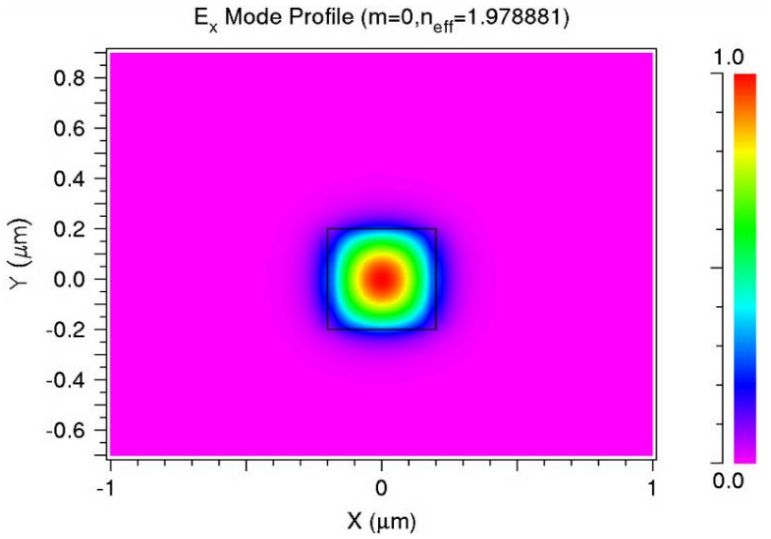


Figure 5.12: Mode profile (XY cross section of the 400 nm OWG) of the fundamental mode.

Simulation results for the 800 nm x 800 nm cross-section OWG

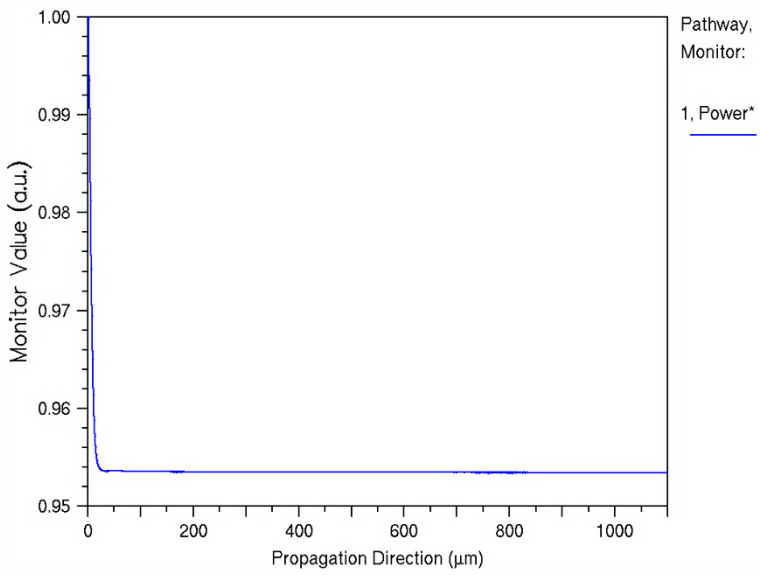


Figure 5.13: Optical energy propagation through the 800 nm OWG along Z without the OWG openings.

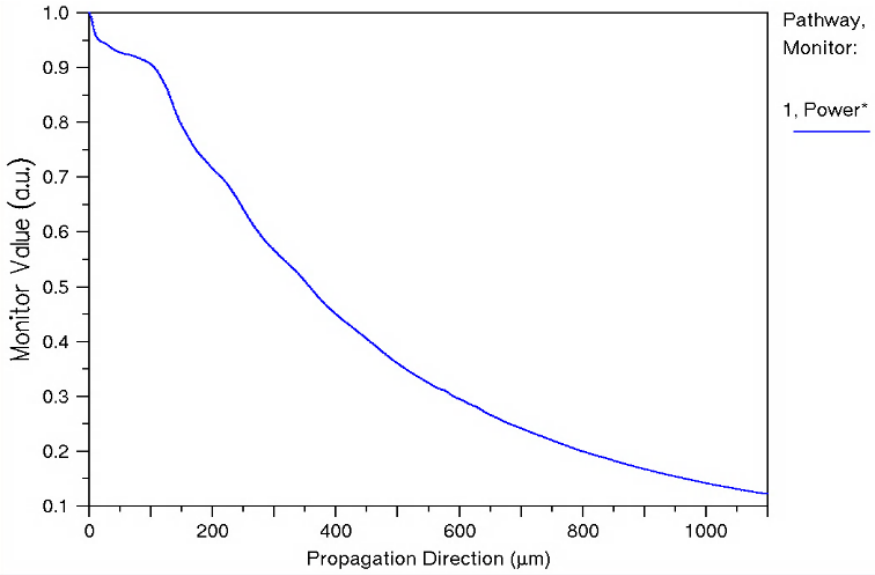


Figure 5.14: Optical energy propagation through the OWG with 800 nm cross section along Z with the OWG openings downward into the XZ plane. The power along Z falls as light is coming out through the OWG openings.

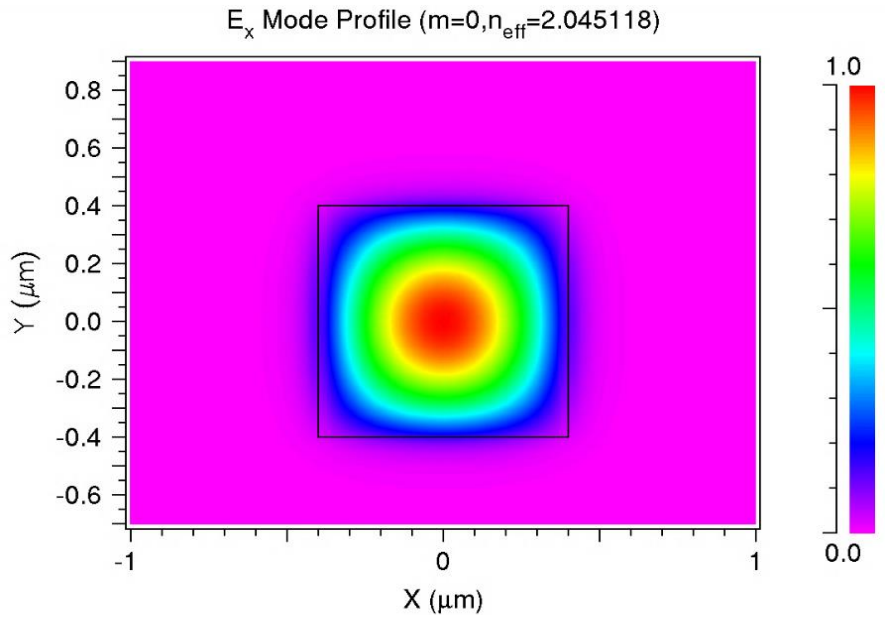


Figure 5.15: Mode profile (XY cross section of the 800 nm OWG) of the fundamental mode.

Simulation results for the 200 nm x 200 nm cross section OWG

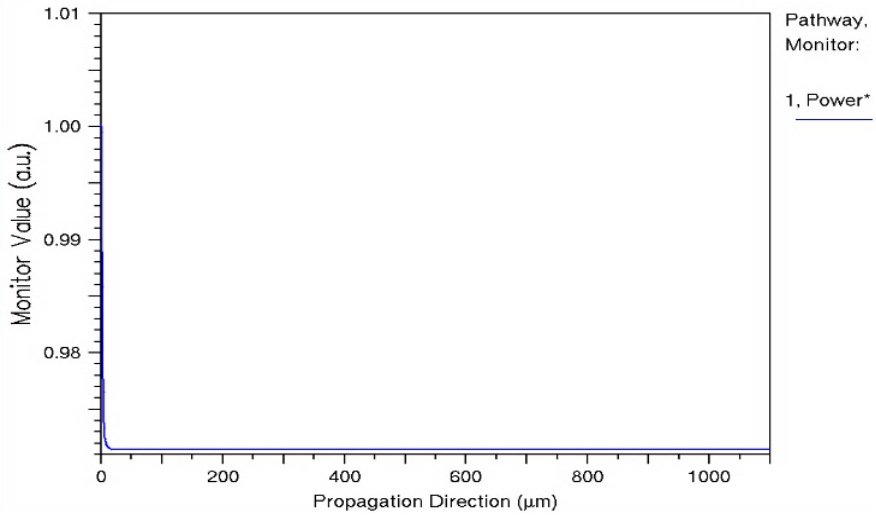


Figure 5.16: Optical energy propagation through the 200 nm cross section OWG along Z without the OWG openings.

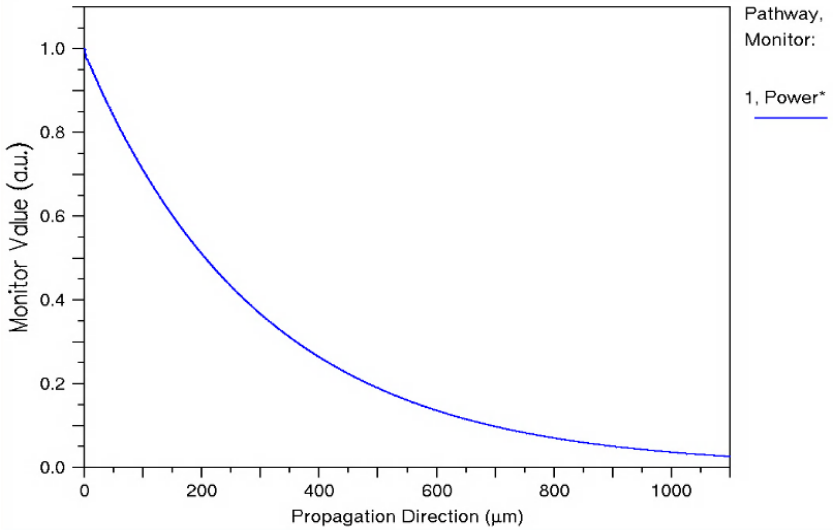


Figure 5.17: Optical energy propagation through the 200 nm cross section OWG along Z with the OWG openings downward into the XZ plane. The power along Z falls as light is coming out through the OWG openings.

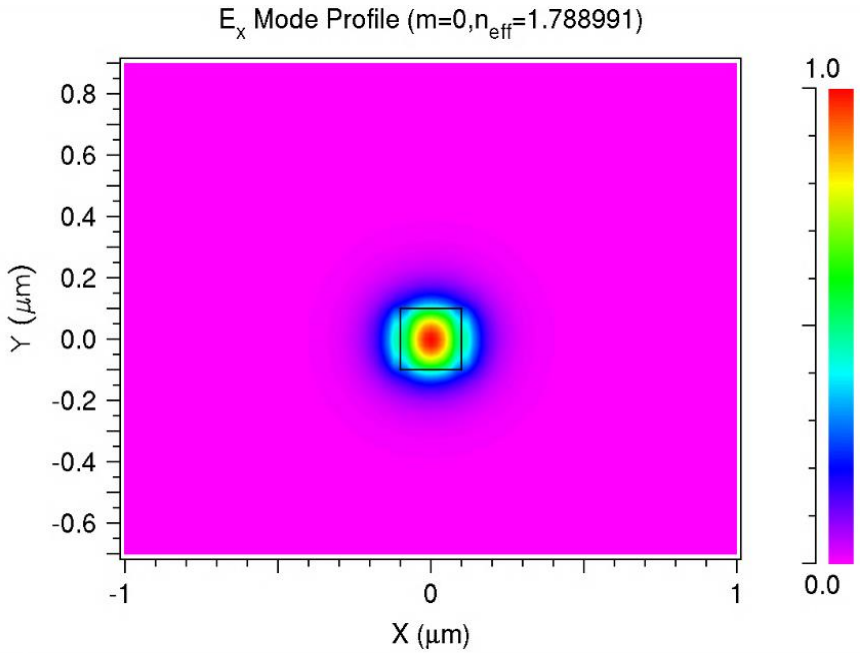


Figure 5.18: Mode profile (XY cross section of the 200 nm OWG) of the fundamental mode.

5.3.2 Analyzing the Waveguide Design

The requirement for single mode propagation in an OWG is given by [112, 113]:

$$\frac{2\pi a}{\lambda_c}\sqrt{n_1^2 - n_2^2} < 2.405 \qquad (5.1)$$

Where a = total width of the square cross section, λ_c = cutoff wavelength, n_1, and n_2 are respectively the refractive indices of the core and cladding materials.

Equation 5.1can be written to calculate the cut-off wavelength as:

$$\lambda_c = \frac{2\pi a}{2.405}\sqrt{n_1^2 - n_2^2} \qquad (5.2)$$

For a given cross-section, for all operating wavelengths λ,> λ_c the OWG will behave as a single mode while for wavelengths $\lambda < \lambda_c$ the OWG will be multimode. Considering the three different

cross sections of 200 nm, 400 nm, and 800 nm, and n_1 = 2.072 for Si_3N_4 core and n_2 = 1.47 for SiO_2 cladding, the cut-off wavelengths are respectively ~ 381 nm, ~ 763 nm, and ~1.53 μm. So, for the 405 nm wavelength that has been used, the 200 nm cross-section OWG behaves as a single mode, the 400 nm cross-section OWG is very close to being a single mode, while the 800 nm cross-section OWG behaves as a multimode OWG, which generally transmits optical energy more efficiently as compared to single mode. The OWG with a higher cross-section should be the most efficient in propagating optical energy, however as seen from the simulation results for the OWGs, the 400 nm x 400 nm cross-section structure seems to be already highly efficient and hence the most suitable structure for the propagation of the optical energy at the wavelength of interest, and hence an 1100 μm long, and 400 nm cross-section OWG will be used for the hybrid SRAM array. This may be due to the better confinement of the optical modes in the 400 nm cross-section rather than in the 800 nm cross-section. Moreover, the 200 nm cross-section OWG structure is a single mode for the 405 nm wavelength used for the simulation and though principally it should be less efficient for optical energy propagation than multimode cases, however, due to better confinement of optical energy in its core, the 200 nm cross-section OWG seems to propagate optical energy more efficiently as compared to the 800 nm cross-section structure as seen from the simulation results of Figures 5.15 and 5.16. Since one of the main drawbacks of this hybrid integration of electronics and photonics is the requirement of a large area mainly for fabricating the photonics components, using an OWG with a lesser cross-section (200 nm) will be much more beneficial in terms of area for large hybrid arrays. In the typical SRAM architecture, the minimum spacing between two adjacent word lines is around 2 poly pitches (200 nm edge to edge spacing for 22 nm technology). For the hybrid SRAM, the optical word line or OWG spacing should be adequate to minimize the optical coupling between the adjacent OWGs. Reducing the OWG dimensions will

play a huge role in compactly laying out the photonic components in a hybrid integration scheme as shown in Figure 5.19. In Figure 5.19 the layout of the photonic layer with parallel OWGs is shown as well as a XY cross-section of the layer is shown with adjacent OWGs. It is to be noted that, though actually the OWGs will be embedded in the SiO_2 dielectric layer as shown in Figure 5.9 [18] and hence would not be visible, the top of the OWGs is still shown in Figure 5.19 just for clarity. The above simulation results have shown that the leakage depends on the OWG size. For instance, for the 200 nm OWG, the lateral leakage into the SiO_2 encapsulation is less than 100 nm, as shown in Figure 5.19, thus, a 200 nm spacing would be adequate to isolate the two OWGs. For the 400 nm OWG, the leakage into the encapsulation layer is reduced, as shown in Figure 5.10, thus, a smaller spacing (around 100 nm) could be used.

As seen in Figure 5.19, W is the dimension of the OWG cross section, which can be 200 nm, 400 nm, or 800 nm. However, if a 800 nm cross section is used then the period width of two adjacent OWGs considering a spacing of 200 nm between the two adjacent OWGs will be, 800 nm + 200 nm = 1 µm. Now if there are 1024 (512 pairs of OWGs) such waveguides in parallel then the approximate total width of the photonic layer along X direction (shown in Figure 5.19) will be approximately = (1.0 µm x 1024) ~ 1024 µm, which is approximate 5 times the dimension needed for a regular array with 1024 word lines in 22 nm technology following the layout used in [111] and hence impractical to be put inside a single chip. However, if a 200 nm cross-section OWG is used, then the total width (period will be 200 nm + 200 nm = 400 nm) of the photonic layer along X direction with 1024 parallel OWGs will be ~ 409.6 µm, which is about 2 times the dimension needed for a regular array with 1024 electrical wordlines, and hence much more feasible for on chip integration.

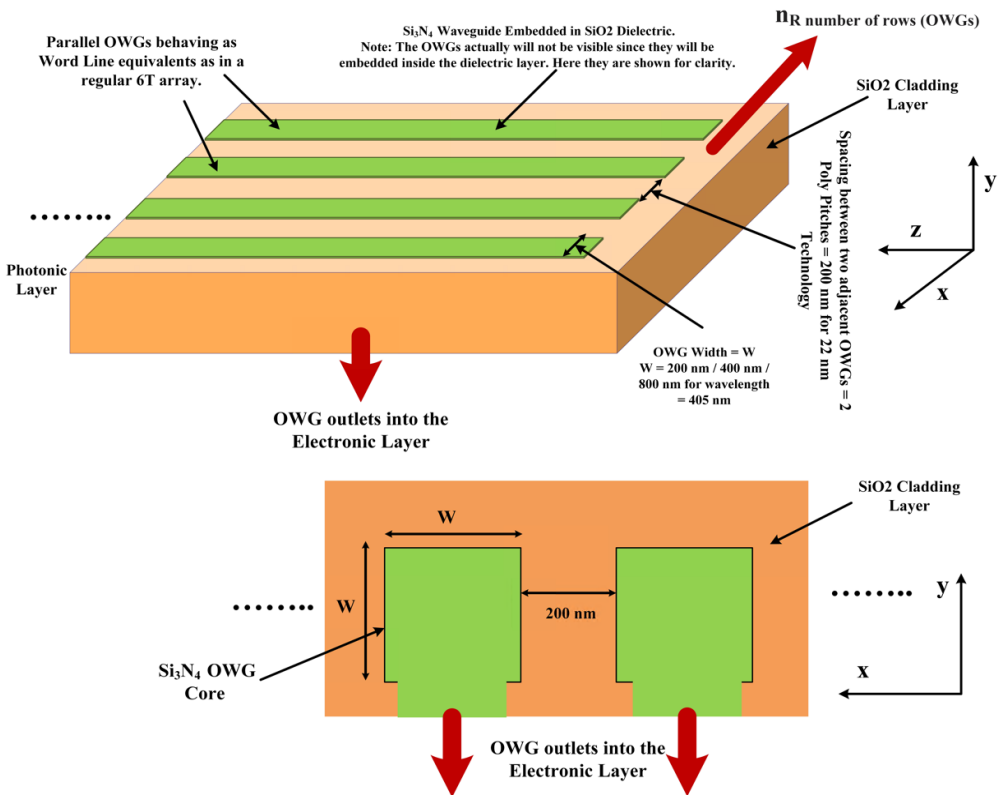


Figure 5.19: 3D layout of the photonic layer showing the parallel OWGs with minimum spacing between adjacent OWGs (Note: The OWGs will be embedded inside the dielectric and hence will not be visible in the 3D view). The XY cross section of the photonic layer showing the OWG encapsulation and minimum spacing between two adjacent OWGs.

However, if the OWG cross-section is further reduced to around 100 nm then the transmission efficiency falls drastically (< 50 %) as shown in Figures 5.20 and 5.21, and hence may not be suitable for the hybrid array. However, the initial loss may be the insertion loss due to the source in-coupling to the OWG (any maybe the propagation loss is not that high) because of size mismatch between the source and the OWG due to diffraction limit beam size (minimum beam size possible

for 405 nm illumination is 1.22 x 405 nm/NA = 494 nm with NA = 1). Typically, people used tapered waveguide (coupling structures) to improve the in-coupling efficiency due to size mismatch between the source and the OWG [114, 115]. Very large initial loss of > 50% for the 100 nm cross section OWG is probably due to this coupling loss. This also implies the 100 nm OWG could still be useful for a shorter array (propagation loss may not be that high), as long as the in-coupling loss can be improved using various techniques, for instances, by using tapered OWG structures [114, 115]. In this sense, a 100 nm size may be still usable for a smaller hybrid array size. Figure. 5.21 suggest that the 100 nm cross section may be used for a smaller array (of size few KBs) where the total word line (OWG) length will be lesser than or equal to 400 µm.

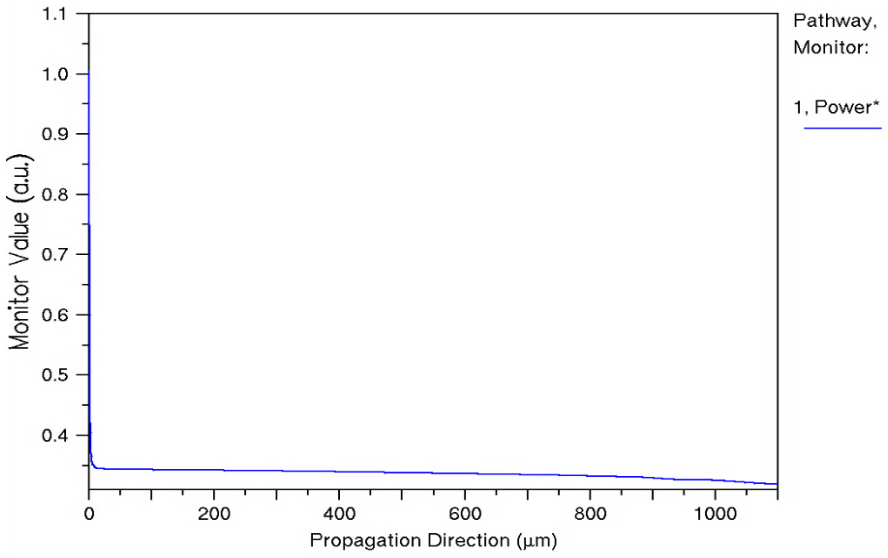


Figure 5.20: Optical energy propagation through the 100 nm cross section OWG along Z without the OWG openings.

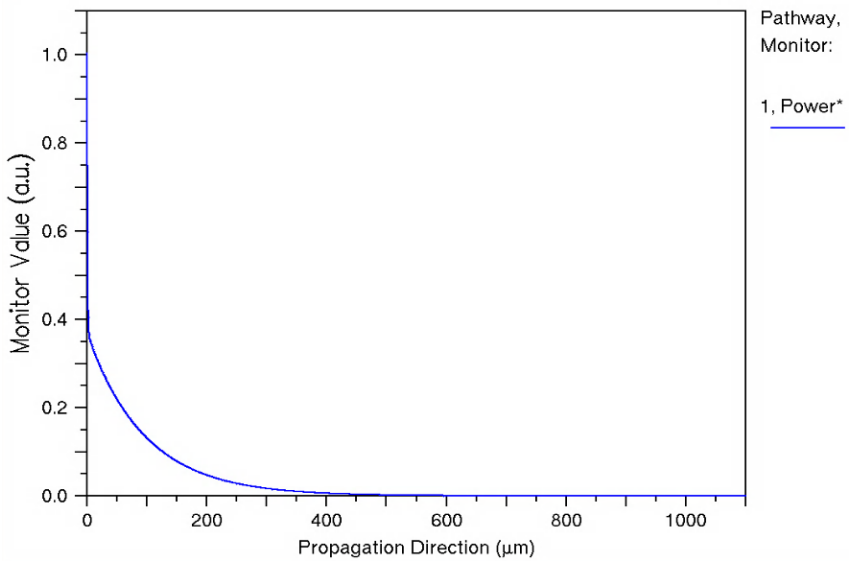


Figure 5.21: Optical energy propagation through the 100 nm cross section OWG along Z with the OWG openings downward into the XZ plane. The power along Z falls as light is coming out through the OWG openings.

5.4 Conclusion

This chapter elaborates on the design of optical OWG for the hybrid FET-LET 6T array. Though various OWG technologies compatible with silicon photonics are possible, here we have described the design of a Si_3N_4 OWG embedded in SiO_2 dielectric, primarily because due to the huge transparency window of Si_3N_4, extremely low absorption loss in the wavelength of interest, and compatibility of its fabrication on a standard CMOS process. To incorporate the novel 3D integration scheme discussed in the chapter, the OWGs not only need to have multiple openings perpendicular to the direction of light injection but also precise spacings between adjacent openings so that the structure is neither too area inefficient, nor suffer from interference due to

light coming from two adjacent openings. To be suitable for large arrays (with long word lines) OWGs of length 550 µm and as long as 1100 µm with different cross sections were designed and simulated in Synopsys *RSoft* CAD, which shows that an OWG with a 400 nm cross-section has the highest transmission efficiency. Though all three cross sections (200 nm, 400 nm, and 800 nm) are equivalently efficient in transmitting optical energy with very less difference, keeping in mind the area parameter, the 200 nm cross-section will be the most viable option in the 3D integration scheme for the best possible compact structure. Further smaller OWG cross section (e.g., 100 nm) could still be usable for smaller SRAM arrays, which is appropriate for level 1 cache memory of the size of a few KBs.

CHAPTER 6: Design of a Fully Functional Hybrid FET-LET 6T SRAM Bit Cell

6.1. Noise Margins in 6T SRAM Cells

With the scaling down of device dimensions to sub-micron ranges, and as device variability increases in the nanometer scale technologies, SRAMs become increasingly prone to noise perturbations. To reduce the dynamic power dissipation in large SRAM arrays, the supply voltage is also scaled down with the technology node, which adversely affects the noise margins of the SRAM cells making the cells very much prone to noise and reducing their reliability [116-118]. The analysis of SRAM read/write margin is extremely crucial for low-power SRAMs and recently research on SRAMs operating in the sub-threshold regime has shown prospects for the design of energy-efficient and ultra-low-power caches for different applications, mainly portable devices[119, 120]. It is a huge challenge to design a SRAM operating in the sub-threshold region (operating at very low voltages) due to its compromised reliability and noise immunity. It is extremely important to have a good read/write margins for all kinds of SRAM designs. Static noise margins (SNMs) are widely used as the criteria for stability for SRAM cells. The traditional butterfly SNM approach is the most popular one, although recent studies on the N-curves (Noise-Curve, is one of the practical inline measurement techniques used to determine SRAM cell stability In this technique set of noise parameters like, static voltage noise margin write trip voltage, static current noise margin, and write trip current [121] are measured from the I-V curves. The N-curves are extracted from the cell I-V by sweeping the voltage at the internal node with logic 0 on it. [122]) have demonstrated their benefits as an alternative metric for understanding SRAM cell stability [116, 123]. As SRAM cells are scaled down to nanometer regimes, they are constrained to operate at very low supply voltage since sub-nanometer MOSFETs operate at very low bias voltage to reduce power dissipation in the circuits, and to increase the reliability of the device against the

gate oxide dielectric breakdown due to hot carrier effects. However, as the device dimensions are scaled down, the transconductance of the devices decreases (mainly due to mobility degradation and parasitic contact resistance) which adversely affects the noise margin of the memory cell [123, 124]. The noise margin arising from process variations and due to the effect of soft errors does not scale down with the supply voltage. So, the design of an SRAM cell at a low supply voltage with sufficient noise margin s more challenging as compared to the design of a SRAM cell at a nominal supply voltage.

To ensure both read stability and writability, the transistors must satisfy ratio constraints, i.e., the ratio of strengths between the pull-down, access, and pull-up transistors in the SRAM cell [21, 125]. The nMOS pulldown transistor (M1 and M3 in Figure 4.1) in the cross-coupled inverters must be the strongest, followed by the access transistors (M5 and M6 in Figure 4.1) are of intermediate strength, and the pMOS pull-up transistors (M2 and M4 in Figure 4.1) must be weaker. The static noise margin of the SRAM cell determines the SRAM cell stability, writability, and readability. Matrices for determining the SNM are given by the hold margin, the read margin, and the write margin, in various modes of operation of the SRAM cell. Quantitatively the SNM measures how much noise can be applied to the inputs of the two cross-coupled inverters before a stable state is lost (i.e., stored data is lost during a hold state or there is a false read) [85].

6.1.1 Measuring SNMs in 6T SRAM Cells

A test circuit for determining the SNM of the 6T cell is shown in Figure 6.1a where an external noise source V_n is applied to each of the cross-coupled inverters and the SNM is determined graphically from the butterfly curve, which is the voltage transfer characteristic (VTC is the output voltage versus input voltage curve) of the two cross-coupled inverter pairs plotted on the same

graph, while an analytical way for determining SNM will be discussed in the next section. The SNM for the circuit in Figure 6.1a is obtained from the butterfly curve of Figure 6.1b by setting V_n = 0 and plotting the variation of V_2 with respect to V_1 and V_1 with respect to V_2, or plotting either of them and flipping the other with respect to the line of symmetry [85]. Curve I shown in Figure 6.1b is the VTC of the top inverter of Figure 6.1a, while curve II is the VTC of the bottom inverter of Figure 6.1a. As can be seen from the butterfly plot of Figure 6.1b, there are two stable states (with one output low and the other high) and one metastable state (with $V_1 = V_2$) [85]. A positive value of noise at the input of the cross-coupled inverters in Figure 6.1 shifts curve I left and curve II up. Excessive noise eliminates the stable state of V_1 = logic 0 and V_2 = logic 1, and hence destroys the stable state of operation [85].

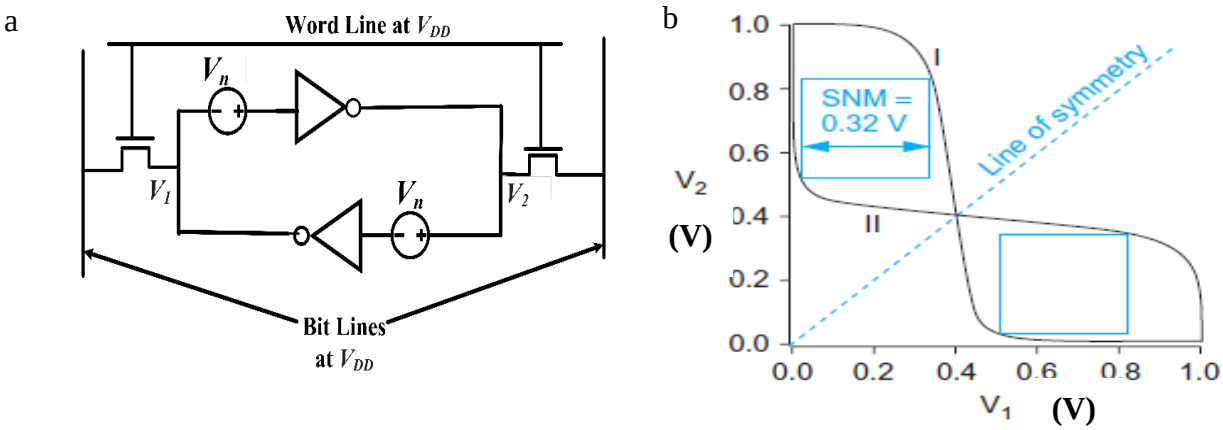


Figure 6.1: (a) 6T SRAM Cell with noise source to determine SNM.

(b) Butterfly diagram showing hold SNM [85].

The length of the side of the largest square that can be inscribed inside the butterfly curves quantitatively determines the SNM of the 6T cell [21, 85]. For asymmetric butterfly diagrams with respect to the line $V_1 = V_2$, the SNM is always the lesser of the two values that can be obtained from the curve. The noise margin increases with V_{DD} and threshold voltage (V_{th}) of the FET devices as will be seen in the analytic expression in the next section. During the 6T cell read operation, the bit lines are initially charged, and one of the nodes (depending on the data stored in it) is discharged via the access transistor. This operation perturbs the voltage transfer characteristics (VTC) of the cross-coupled inverter latches and the amount of voltage perturbation that can be tolerated without sacrificing the read operation is known as the read SNM. The relative strength (ratio of device widths which is also known as the beta ratio or the cell ratio) of the pull-down transistor to the access transistor determines the read SNM. [85, 126]. As the beta ratio for a 6T cell increases, the read margin improves, however, this increases the total 6T cell area, and hence there is a clear trade-off. A few other techniques generally adopted to improve the read SNMs are, increasing V_{DD} or V_{th} or reducing the word line voltage drive relative to V_{DD}. During the cell write operation, for proper stability of the cell, the strength of the access device must be greater than the pull-up device to create a single stable state [85]. Similar to the read SNM simulation, the write SNM is qualitatively determined, with one access transistor moving towards logic 1 and the other towards logic 0. As in the case of read SNM, the write SNM is also the smallest of the two squares inscribed in the butterfly curve of the VTC. The write SNM depends on the relative strengths of the pull-up device to the access device and it improves with a more powerful access device as compared to the pull-up device and also with the increase of the word line voltage [85, 126].

Read write and hold SNMs are also affected by the threshold voltage mismatch which is caused by random dopant fluctuations mostly in the advanced nanometer semiconductor

fabrication processes [120, 124]. However, the variations in technology parameters, such as threshold voltage, effective channel length, gate oxide thickness as well as supply scaling, and operating temperature heavily affects the stability of 6T cell in submicron technologies [85, 116, 124]. It is interesting to note that the SNMs only depend on the ratio of the transconductance parameters (ratio of the relative device strengths) of the pull-down, access, and pull-up transistors, and not on the absolute values of the transconductance of the transistors.

6.1.2 Analytical Calculation of the SNM in Regular 6T Cells

The regular 6T cell of Figure 4.1 with two noise voltage sources V_n is shown in Figure 6.2 where it is assumed that the voltage at node Q is logic 1 while at node $\overline{Q}$ it is logic 0.

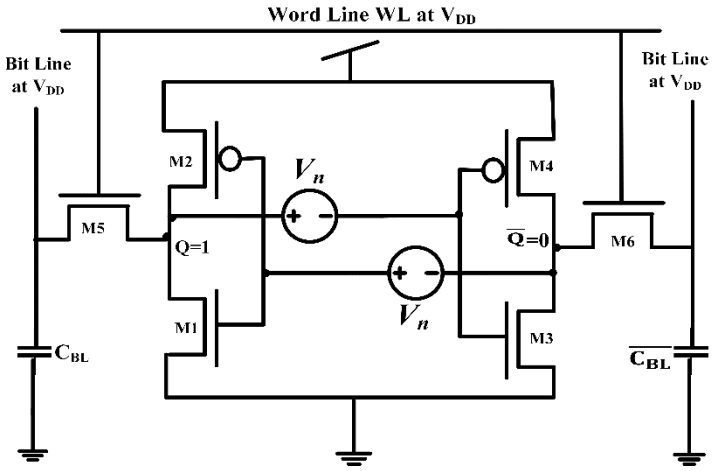


Figure 6.2: A regular 6T cell with noise sources for analytical estimation of SNM.

For the voltage conditions shown in Figure 6.2, M1 and M6 are in saturation while M2 and M3 operate in the linear region. Equating the drain currents of M1 and M2 and M3 and M6 we get [126]:

$$(V_{GSM1} - V_{th})^2 = \frac{2q}{r} V_{DSM2}(V_{GSM2} - V_{th} - \frac{1}{2}V_{DSM2}) \quad (6.1)$$

$$(V_{GSM6} - V_{th})^2 = 2rV_{DSM3}(V_{GSM3} - V_{th} - \frac{1}{2}V_{DSM3}) \quad (6.2)$$

where V_{GS} and V_{DS} are the gate-source and drain-source voltages respectively of the FETs M1-M6, V_{th} is the threshold voltage of the FETs and they are assumed to be equal; $\beta = \mu c_{ox}'(W/L)$ is the transconductance parameter for the FET devices, and $r = \beta_{pulldown}/\beta_{access}$, and $q = \beta_{pullup}/\beta_{access}$ [126].

Using Kirchhoff's Voltage Law (KVL) to the circuit in Figure 6.2 the voltage equations are:

$$V_{GSM1} = V_n + V_{DSM3} \quad (6.3)$$

$$V_{DSM2} = V_{DD} - V_n - V_{GSM3} \quad (6.4)$$

$$V_{GSM2} = V_{DD} - V_n - V_{DSM3} \quad (6.5)$$

$$V_{GSM6} = V_{DD} - V_{DSM3} \quad (6.6)$$

Substituting Equations 6.3 – 6.6 into Equations 6.1 and 6.2 gives:

$$(V_{DSM3} + V_n - V_{th})^2 = \frac{q}{r}(V_{DD} - V_n - V_{DSM3})\,(V_s - V_{th} - V_n - 2V_{DSM3} + V_{GSM3}) \quad (6.7)$$

$$(V_S + V_{DSM3})^2 = 2rV_{DSM3}(V_{GSM3} - V_{th} - \frac{1}{2}V_{DSM3}), \quad (6.8)$$

where $V_s = V_{DD} - V_{th}$

Eliminating $V_{DSM3/GSM3}$ from Equations 6.7 and 6.8 leads to a fourth-degree non-linear equation. Linearizing the equation at around the operating point of the FET leads to a linear approximation given by, $V_{DSM3} = V_0 - kV_{GSM3}$, where k is the slope of the linear approximation. Three variables are defined as follows [126]:

$$V_r = V_s - (\frac{r}{r+1})\,V_{th} \quad (6.9)$$

$$k = \left(\frac{r}{r+1}\right)\sqrt{\frac{r+1}{r+1-\frac{V_s^2}{V_s^2}}} - 1, \quad (6.10)$$

and

$$V_0 = kV_s + \left(\frac{1+r}{r+1+r/k}\right) V_r \quad (6.11)$$

Using Equations 6.7 – 6.11, eliminating V_{DSM3} from Equations 6.7, using the double root stability criteria [126], and then solving for V_n, the SNM is obtained as follows [126]:

$$\mathbf{SNM_{6T\_Cell}} = \boldsymbol{V_{th} - A\left(\frac{B}{C} - \frac{V_{DD}-2V_{th}}{D+E}\right)} \quad (6.12)$$

where $A = \frac{1}{1+k}$, $B = V_{DD} - \frac{2r+1}{r+1}V_{th}$, $C = 1 + \frac{r}{k(r+1)}$, $D = 1 + k\frac{r}{q}$, *and* $E = \sqrt{\frac{r}{q}\left(1 + 2k + \frac{rk^2}{q}\right)}$.

Now for the regular 6T cell, designed and simulated in the mixed mode environment of Sentaurus TCAD, the FinFET and 6T cell parameters are as follows: V_{th} = 350 mV, r = 2, q = 0.375, and V_{DD} = 1 V. Plugging in these values into Equations 6.9 through 6.12, the SNM_{6T_Cell} is calculated to be around ~ 230 mV which is very similar to values obtained from mixed mode TCAD simulation as shown in the next section. It is to be noted that for the hybrid 6T cell, an expression like Equation 6.12 cannot be derived analytically, since, for the hybrid cell, all the voltage equations governing the regular 6T cell operation are not applicable due to the presence of the access LETs which are not a voltage-controlled device like FETs. However, *mixed mode* TCAD simulation as discussed in the next section can be a powerful tool to capture the SNMs for both the regular and the hybrid 6T cell.

6.2 Mixed Mode TCAD simulation of Regular and Hybrid 6T Cells

The FinFET and LET devices designed and modeled in chapter 3 are used to design a regular and hybrid 6T cell in a *mixed mode* simulation environment by directly establishing the netlist in the system section of the *SDEVICE* module of Sentaurus TCAD [56, 57]. A series of parametric

simulations are run for various r and q ratios describing relative strengths for pull up, pull down, and access FET devices, and it was found that the best SNM for the regular cell was obtained for $r = 2$ and $q = 0.375$, i.e., the pull-down FETs should be stronger than the access FETs by a factor of 2, while the pull-up FETs should be weaker than the access FETs. For the hybrid 6T cell since the LETs are optically controlled devices, optical gating power (generation rate) can be a controlling parameter, and varying the generation rate for the two access LETs will give different SNM curves for different generation rates, and the best optimized SNM is obtained at an optical generation rate of ~ $10^{25}/cm^3/sec$.

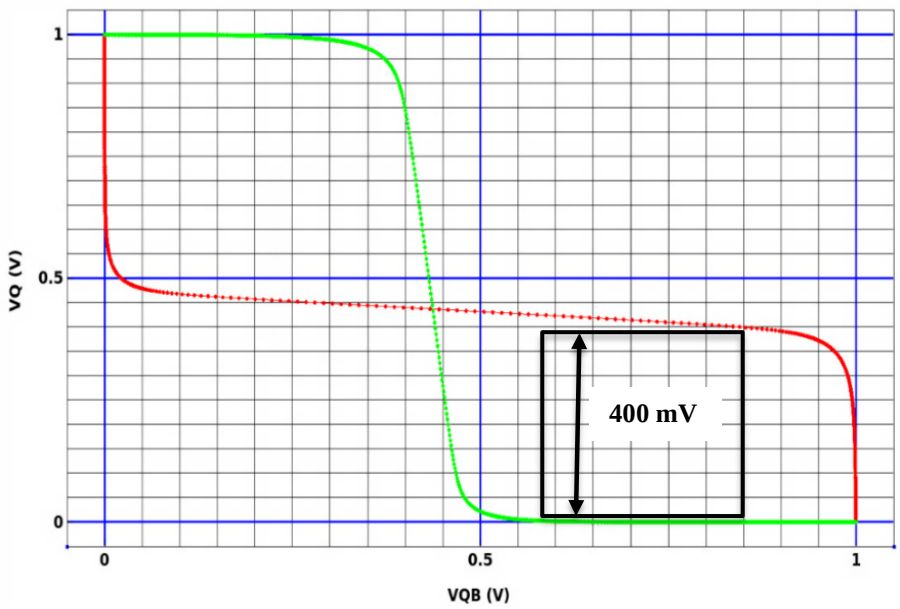


Figure 6.3: Simulated (mixed mode) hold SNM for a regular 6T SRAM cell.

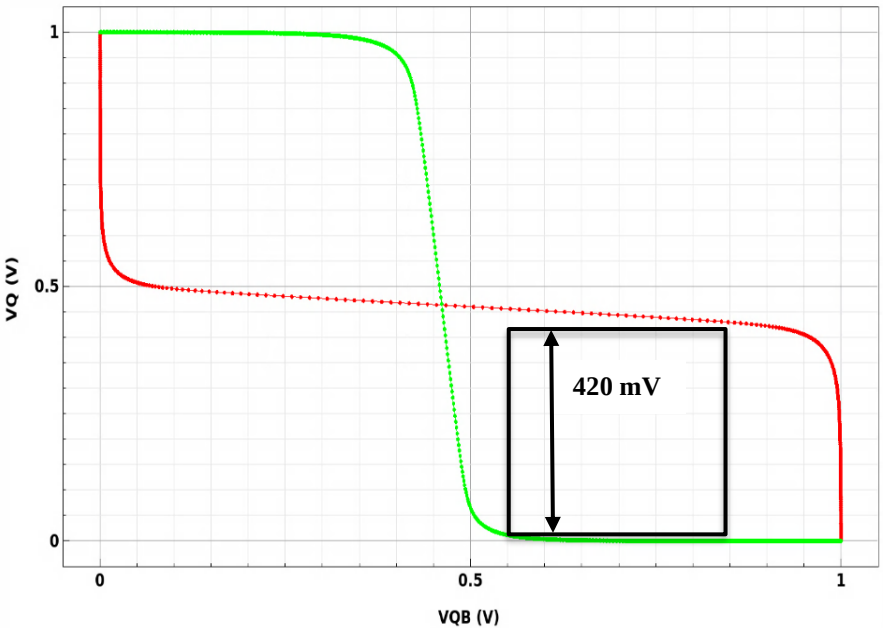


Figure 6.4: Simulated (mixed mode) hold SNM for a hybrid 6T SRAM cell.

Figures 6.3 and 6.4 show the hold SNM for a regular 6T cell and hybrid 6T cell, respectively. The SNM values are measured by the length of the side of the largest square that can be fitted inside the butterfly curve as shown in Figure 6.1b. For the regular case, the hold SNM is ~ 400 mV, while for the hybrid 6T cell it is around 420 mV.

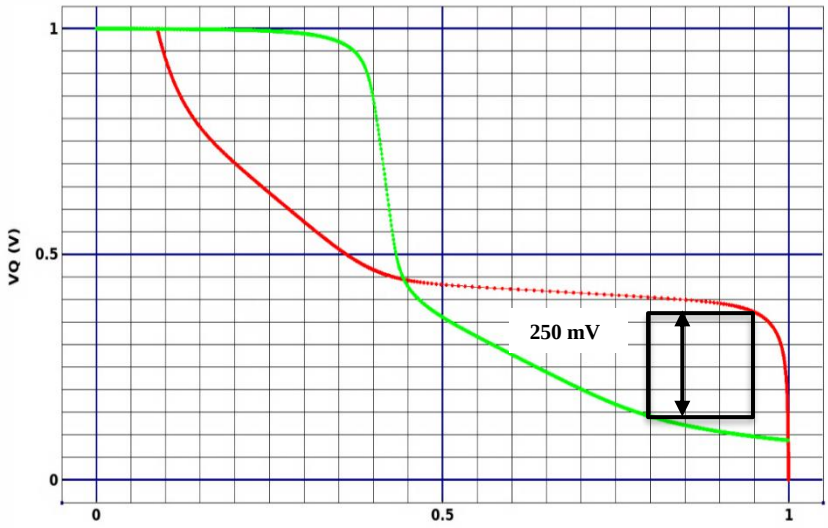


Figure 6.5: Simulated (mixed mode) read SNM for a regular 6T SRAM cell.

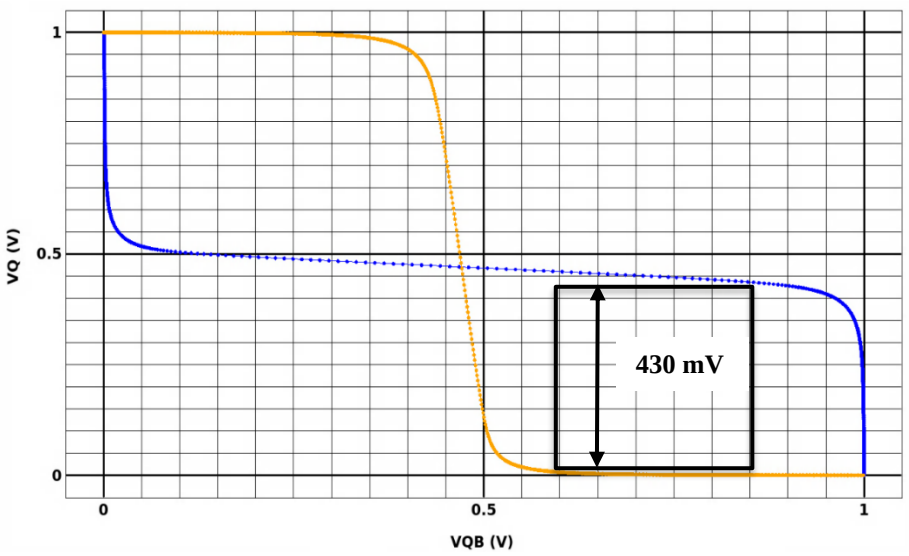


Figure 6.6: Simulated (mixed mode) read SNM for a hybrid 6T SRAM cell.

Figures 6.5 and 6.6 show the read SNM for a regular 6T cell and hybrid 6T cell, respectively. The read SNM values as seen from the figures are approximately 250 mV and 430 mV respectively for the regular 6T cell and hybrid 6T cell.

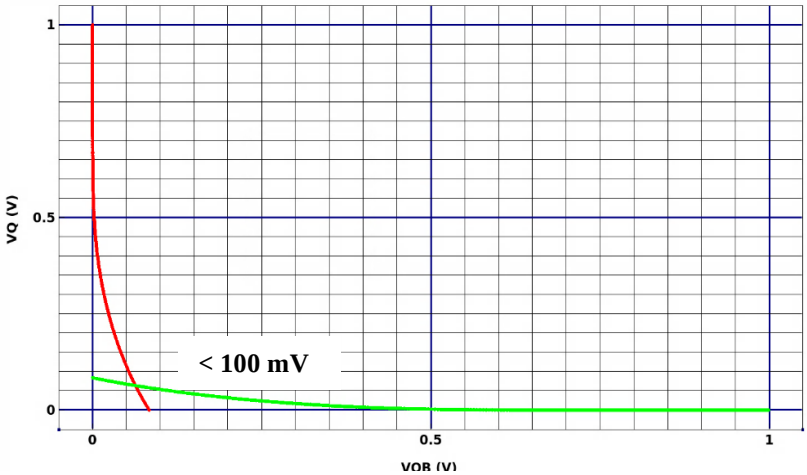


Figure 6.7: Simulated (mixed mode) write SNM for a regular 6T SRAM cell.

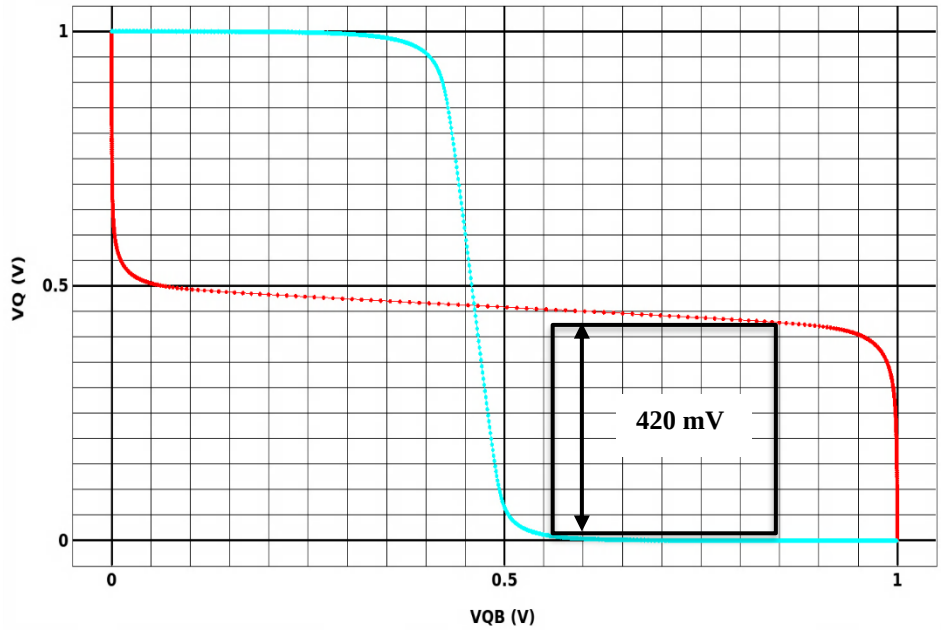


Figure 6.8: Simulated (mixed mode) write SNM for a hybrid 6T SRAM cell.

Figures 6.7 and 6.8 show the write SNM for a regular 6T cell and a hybrid 6T cell, respectively. The SNM values as seen from the figures are approximately < 100 mV and 420 mV respectively for the regular 6T cell and hybrid 6T cell.

6.3 Analyzing the Results and SNM Variation in the Hybrid 6T Cell

From the butterfly SNM plots, it is very clear that the SNMs for the hybrid 6T cell are better than the regular 6T cell (especially for the read and write cases). This can be attributed to the reason that fundamentally the LETs operate using a different mechanism which gives them better switching characteristics compared to the FETs. It is evident from the simulated output and transfer characteristics of the LETs as shown in Figures 3.10 and 3.11b and also from measured results [13] (the output and transfer characteristics plots for the LET are steeper as compared to FETs) the threshold power (threshold power P_g in Watts) and the subthreshold swing (S_{LET} in Watts/dec), are

much smaller as compared to the equivalent of the threshold power (threshold voltage in case of FETs) and subthreshold swing (in mV/decade in case of FETs) of FETs of similar size FETs. This is fundamentally due to the simple structure of the LET that does not add any unwanted capacitances to the structure due to the lack of any unwanted pn junctions and a physical gate [14]. Also, for the access FETs in the 6T cell to operate in either the liner or saturation region (for the read or write operation) precise voltage conditions like $V_{DS} >= V_{GS} - V_{th}$ or $V_{DS} < V_{GS} - V_{th}$ must be satisfied [127], which, if not strongly satisfied, leaves the FETs in marginal saturation or liner region, also affecting the noise margin for the cell. However, for the hybrid 6T cell where LETs are under single beam illumination, it does not have such distinctive regions of operation and acts as a more idealistic switch than the FETs, which improves the noise margins. Moreover, the stability condition for a 6T SRAM cell [21, 125] is very well satisfied for the hybrid structure since the pull-down n-FinFETs used in the cell have a stronger current drive capability as compared to the access LETs, while the access LETs have a stronger current drive as compared to the pull-up p-FinFETs, as discussed later. SNM butterfly curves are plotted for the hybrid 6T cell for various optical generation rates for the access LETs as shown in Figure 6.9. It is observed that the SNMs distorts at higher optical generations rates because at higher generation the LETs sink more current as compared to the pull-down FETs that have a fixed gate voltage and hence cannot drive more current which affects the stable operating point of the hybrid 6T cell. Considering the hybrid 6T cell of Figure 4.4 in Chapter 4, for stability analysis of the hybrid cell just as in the case of a regular 6T cell, the drain current of M1 should be equal to the current through LET L1 for the read 0 operation and drain current of M2 should be equal to the current through L1 for write 0 operation. Since the current through the n-FinFET M1 and current through LET L1 should be equal during

the read 0 process, and current through p-FinFET M2 and LET L1 should be equal during the write 0 process, equating the currents for the FinFETs and the access LETs we get:

$$\frac{W\,\mu_{eff}}{L_{eff}}\left[(Q_s - Q_D)\left(\frac{Q_s+Q_D+Q_L}{4C_{ox}}\right) + \frac{8k^2T^2C_{Si}}{q^2}\log\left(\frac{Q_D+8(\frac{kT}{q})C_{Si}}{Q_s+8(\frac{kT}{q})C_{Si}}\right)\right] = \frac{\eta\left(\frac{P_{opt}}{\hbar\omega}\right)}{volume}eE(\mu_n\tau_n + \mu_p\tau_p)\pi R^2 \tag{6.13}$$

Where the LHS of the equation represents the current through the FinFET [128, 129] where Q_s and Q_D are the mobile charge densities at the source and drain respectively; C_{Si} is the silicon film capacitance [128]. The RHS of the equation represents the current through the LET [13], where $\frac{\eta\left(\frac{P_{opt}}{\hbar\omega}\right)}{volume}$ is the optical generation rate = g, and R is the radius of the nanowire. Now, for proper stable read operation it is needed that voltage at node Q does not get above the V_{th} of n-FET M3 and accidentally turn it on, and unwantedly flips the cell. To stop the cell from flipping during the read, the current drive strength of the n-FET M1 should be greater than LET L1 so that the node voltage Q does not go above V_{th} of M3. While for write 0 operation, i.e., changing the data stored in node Q (assuming initially a 1 was stored), the access LET L1 should be stronger than p-FET M2 such that L1 can effectively pull down the node voltage at Q so that the cell flips and there is a successful write operation [21]. So, considering the factors for both read and write operations, it can be concluded that for the best-optimized noise margin for both read and write cases, the strength of the transistors should be as follows: *pull down n-FETs > access LETs > pull up p-FETs.*

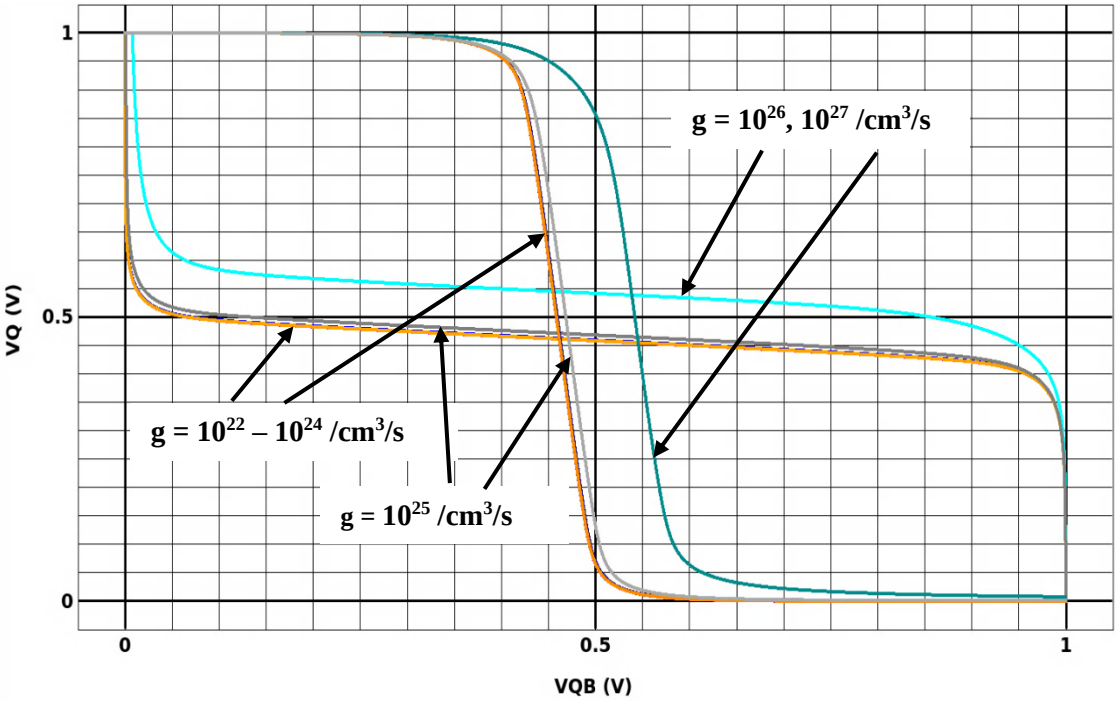


Figure 6.9: Butterfly curves for a hybrid 6T SRAM cell for various optical generation rates for the access LETs.

This is easy to achieve in the case of the hybrid 6Tcell since, for similar dimensions, the n-FinFETs have a higher current driving capability that the optically controlled LET, while the p-FinFETs have lower current drive capability than the LET due to the lower majority carrier mobility for p-FETs. Keeping all the parameters of the FinFET same from Equation 6.13, the design parameters for the current drive in the FinFET is the ratio of W/L_{eff} (where W is the total width of the device, and L_{eff} is the effective channel length) and similarly, for the LET keeping all the other parameters same as in Equation 6.13, R and g are the two current tuning parameters. In this work, we only used the optical generation rate (g) as a tuning parameter at a fixed value of R to modulate the conductivity and the current through the LET L1 and hence the SNMs. The SNM butterfly curves

were plotted for various generation rates, keeping all the other parameters for both the LETs and FinFETs to be constant. It was found from the various SNM curves that for a set of *g* values (10^{22} - 10^{25}/cm^3/sec) the SNM butterfly curves somewhat coincide and give the best possible optimized SNMs, while for other generation rates the butterfly curves are very skewed (asymmetrical) since the stability condition related to the relative strengths of the pull-down, access, and pull up transistors are not satisfied, and thereby worsening the SNMs to some extent.

6.4 Conclusion

This chapter depicts the potential of a hybrid FET-LET 6T cell to function properly as a 1-bit SRAM. Though the superiority of a 6T hybrid array in terms of the overall delay and energy consumption over a regular 6T array has been clearly shown in chapter 4, it was not certain whether the hybrid 6T cell with LET access devices will satisfactorily perform the function of a SRAM bit cell in terms of SNM which is estimated from the butterfly curves of the 6T cell. It is evident from this chapter that the hybrid 6T cell not only performs satisfactorily (as evident from the non-collapsing butterfly curves) but also has better noise immunity (evident from better SNMs) as compared to the regular 6T cell. This is mostly because the LET under single illumination serves as a better switch as compared to a FET as discussed in the chapter. Moreover, it is also found that the hybrid 6T cell along with the LET dimension and the optical generation rate can also be a control knob to modulate the SNMs and hence the performance of the hybrid 6T cell.

CHAPTER 7: Conclusion and Future Possibilities

7.1 Conclusion

LETs open up a whole new avenue for electronic-photonic integrated circuits where both the electronic and photonic components play the roles synergistically, and the photonic components directly play the roles in the computing process, not only beyond serving high-speed communication links between various electronic modules but also offering much better performance with higher energy efficiency as compared to ICs with pure FETs. Though typical MSM photoconductors require large bias voltage across their two ends for efficient carrier transport, the LETs require significantly lesser voltages (~ 1V to a few tens of mV for the ballistic structure) due to the reduction of the nanowire lengths to a few hundred nanometers. Also, to avoid the cascading issues of the LETs directly driving another LET, only switching FETs are replaced with LETs like the access FETs in the case of a 6T SRAM cell. In gated FETs, generally, RC switching delay and energy predominate over the transit delay of carriers through the channel, and hence it is much less energy efficient. In the hybrid array, the main advantage stems from the fact that the gate, source, and drain-related capacitance of the access FETs and electrical word line are no longer present, which removes the word line delay and greatly reduces the energy consumption, and thus the overall structure is much more energy efficient with better performance as compared to the regular 6T structure. In addition, due to their simple gateless structure, LETs can be expected to have much lower leakage currents than conventional FETs, and thus the hybrid 6T array will have much lesser leakage compared to the regular 6T array. The use of the optical waveguide-based word line architecture in the hybrid SRAM array abolishes the need for electrical wordlines and also the word line drivers, which drastically reduces the total word line capacitance, RC-delay, and energy loss to almost negligible compared to regular array structure. Also, the proposal of

grouping the four access LETs from 2 adjacent hybrid SRAM cells and illuminating them from a single OWG opening not only reduces the number of OWG openings by a factor of 4 but also reduces the energy loss due to each OWG opening. Moreover, despite the hybrid 6T cell being much superior compared to the regular SRAM in terms of speed and energy consumption, it has to also function satisfactorily as a memory storing unit which is determined by the noise margins (the butterfly curve of the two cross-coupled inverters) of the cell. The mixed mode TCAD simulation of a fully functional FET-LET hybrid 6T cell shows excellent noise margins as evident from the butterfly curve. Hence the proposed hybrid 6T SRAM is not only superior in terms of delay and energy as compared to a regular 6T SRAM, but also it is a more stable bit cell as compared to a regular 6T cell. So, the 6T hybrid SRAM structure offers a much closer on-chip electronic–photonic integration where both the components play active roles in the performance and efficiency of the overall photonic integrated circuit (PIC).

7.2 Future Directions

In the future, it will be great research to develop a compact analytical SPICE model for the LET which will take into account all the device physics like ballistic transport, carrier recombination, tunneling of carriers at MS contacts, and so on. Once the SPICE model for the LET has been created, the electrical model for passive OWG can also be developed in either Synopsys or Lumerical, and then the compact SPICE mode for the LET, optical OWG, along with the compact SPICE model of a FinFET can be used together to create a netlist for the whole hybrid SRAM array (say for example the 64 KB hybrid array) and a SPICE simulation can be run (maybe in Synopsys HSPICE or Cadence) to calculate the delay and energy consumption of the whole array. Furthermore, LETs may find useful applications in other peripheral and assist circuits of the

SRAM array like the bit line conditioning circuit for improvement in speed and energy consumption. Lastly, a prototype FET - LET-based 6T array (of small capacity maybe 4 KB) may be monolithically fabricated and put inside a die and interfaced with other off-chip CMOS peripherals to build a whole prototype functional hybrid FET - LET 6T SRAM array.

7.3 Publications

Research Papers:

1. A. Pal, Y. Zhang, and D. D. Yau, "Monolithic and single-functional-unit level integration of electronic and photonic elements: FET-LET hybrid 6T SRAM," *Photon. Res.*, vol. 9, no. 7, pp. 1369-1378, 2021/07/01 2021.

2. A. Pal, Y. Zhang, and D. D. Yau, "Light Effect Transistors for High-Speed and Low-Energy Electronic and Photonic Integrated Circuits," in *2021 IEEE Research and Applications of Photonics in Defense Conference (RAPID)*, 2-4 Aug. 2021 2021, pp. 1-2.

3. A. P. Y. Z. D. D. Yau, "Hybrid Electronic-Photonic Integrated Circuits: Hybrid FET-LET SRAM," presented at the 20th International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD 2020), Italy, Sept 2020, 2020. [Online]. Available: https://nusod.com/.

4. A. Pal, Y. Zhang, D.D. Yau, “Single-Functional-Unit Level Integration of Electronic and Photonic Elements: FET-LET Hybrid 6T SRAM with Greatly Improved Performance in Speed and Energy”, in Frontiers in Optics and Laser Science, Oct 2022 (Poster).

5. A. Pal, Y. Zhang, "TCAD simulation of light effect transistor," presented at the 2nd iiScience International Conference 2021, March 29-30, 2021, 2021. [Online]. Available: https://iiscience-intl-conference.org/.

Book Chapter (In press):

1. A. Pal, et al., "Light-Effect Transistors and their Applications in Electronic-Photonic Integrated Circuits," in *Modeling, Characterization, and Production of Nanomaterials: Electronics, Photonics, and Energy Applications*, V. K. Tewary, Y. Zhang Ed., 2nd ed.: Elsevier, 2022.

U.S. Patent (Filed):

- Y. Zhang, A. Pal, and D. D. Yau, “Integrated Circuits with Single-Functional-Unit Level Integration of Electronic and Photonic Elements,” **U.S. patent 22-1144-US.**

REFERENCES

[1] K. W. Ang *et al.*, "Silicon photonics technologies for monolithic electronic-photonic integrated circuit (EPIC) applications: Current progress and future outlook," in *2009 IEEE International Electron Devices Meeting (IEDM)*, 7-9 Dec. 2009 2009, pp. 1-4, doi: 10.1109/IEDM.2009.5424294.

[2] A. V. Krishnamoorthy and K. W. Goossen, "Optoelectronic-VLSI: photonics integrated with VLSI circuits," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 4, no. 6, pp. 899-912, 1998, doi: 10.1109/2944.736073.

[3] Z. Zhao, Z. Wang, Z. Ying, S. Dhar, R. T. Chen, and D. Z. Pan, "Logic synthesis for energy-efficient photonic integrated circuits," in *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, 22-25 Jan. 2018 2018, pp. 355-360, doi: 10.1109/ASPDAC.2018.8297349.

[4] T. Chattopadhyay, "Optical logic circuits using double controlled logic gate," *IET Optoelectronics*, vol. 7, no. 5, pp. 99-109, 2013, doi: https://doi.org/10.1049/iet-opt.2013.0063.

[5] M. U. Khan, Y. Xing, Y. Ye, and W. Bogaerts, "Photonic Integrated Circuit Design in a Foundry+Fabless Ecosystem," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 25, no. 5, pp. 1-14, 2019, doi: 10.1109/JSTQE.2019.2918949.

[6] M. J. Shawon and V. Saxena, "Rapid Simulation of Photonic Integrated Circuits using Verilog-A Compact Models," in *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, 4-7 Aug. 2019 2019, pp. 424-427, doi: 10.1109/MWSCAS.2019.8885372.

[7] Y. Shen *et al.*, "Deep learning with coherent nanophotonic circuits," *Nature Photonics*, vol. 11, no. 7, pp. 441-446, 2017/07/01 2017, doi: 10.1038/nphoton.2017.93.

[8] A. H. Atabaki *et al.*, "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," *Nature*, vol. 556, no. 7701, pp. 349-354, 2018/04/01 2018, doi: 10.1038/s41586-018-0028-z.

[9] C. Sun *et al.*, "Single-chip microprocessor that communicates directly using light," *Nature*, Letter vol. 528, no. 7583, pp. 534-538, 12/24/print 2015, doi: 10.1038/nature16454

http://www.nature.com/nature/journal/v528/n7583/abs/nature16454.html#supplementary information.

[10] R. Landauer, "Irreversibility and Heat Generation in the Computing Process," *IBM Journal of Research and Development*, vol. 5, no. 3, pp. 183-191, 1961, doi: 10.1147/rd.53.0183.

[11] R. Landauer, "Energy requirements in communication," *Applied Physics Letters*, vol. 51, no. 24, pp. 2056-2058, 1987, doi: 10.1063/1.98291.

[12] P. R. Panda, Silpa, B.V.N., Shrivastava, A., Gummidipudi, K., *Power-efficient System Design*. New York Dordrecht Heidelberg London,: Springer, 2010.

[13] J. K. Marmon, S. C. Rai, K. Wang, W. Zhou, and Y. Zhang, "Light-Effect Transistor (LET) with Multiple Independent Gating Controls for Optical Logic Gates and Optical Amplification," (in English), *Frontiers in Physics*, Original Research vol. 4, no. 8, 2016-March-21 2016, doi: 10.3389/fphy.2016.00008.

[14] A. Pal, Y. Zhang, and D. D. Yau, "Monolithic and single-functional-unit level integration of electronic and photonic elements: FET-LET hybrid 6T SRAM," *Photon. Res.*, vol. 9, no. 7, pp. 1369-1378, 2021/07/01 2021, doi: 10.1364/PRJ.420887.

[15] D. A. B. Miller, "Optical interconnects to electronic chips," *Appl Opt*, vol. 49, no. 25, pp. F59-F70, 2010/09/01 2010, doi: 10.1364/AO.49.000F59.

[16] C.-Z. Ning, "Semiconductor nanolasers and the size-energy-efficiency challenge: a review," *Advanced Photonics*, vol. 1, no. 1, p. 014002, 2019. [Online]. Available: https://doi.org/10.1117/1.AP.1.1.014002.

[17] S. Y. Chou and M. Y. Liu, "Nanoscale tera-hertz metal-semiconductor-metal photodetectors," *IEEE Journal of Quantum Electronics*, vol. 28, no. 10, pp. 2358-2368, 1992, doi: 10.1109/3.159542.

[18] A. Pal, Y. Zhang, and D. D. Yau, "Light Effect Transistors for High-Speed and Low-Energy Electronic and Photonic Integrated Circuits," in *2021 IEEE Research and Applications of Photonics in Defense Conference (RAPID)*, 2-4 Aug. 2021 2021, pp. 1-2, doi: 10.1109/RAPID51799.2021.9521451.

[19] A. P. Y. Z. D. D. Yau, "Hybrid Electronic-Photonic Integrated Circuits: Hybrid FET-LET SRAM," presented at the 20th International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD 2020), Italy, Sept 2020, 2020. [Online]. Available: https://nusod.com/.

[20] Y. Zhang, "Light effect transistors for high speed and low energy switching and beyond," *Journal of Physics: Conference Series*, vol. 1537, p. 012004, 2020/05 2020, doi: 10.1088/1742-6596/1537/1/012004.

[21] a. Y. L. Sung-MO (Steve) Kang *CMOS Digital Integrated Circuits*. McGraw-Hill.

[22] S. Mokkapati, D. Saxena, H. H. Tan, and C. Jagadish, "Chapter One - Semiconductor Nanowire Optoelectronic Devices," in *Semiconductors and Semimetals*, vol. 94, S. A. Dayeh, A. Fontcuberta i Morral, and C. Jagadish Eds.: Elsevier, 2016, pp. 1-15.

[23] V. J. L *et al.*, "A Perspective on Nanowire Photodetectors: Current Status, Future Challenges, and Opportunities," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 4, pp. 1002-1032, 2011, doi: 10.1109/JSTQE.2010.2093508.

[24] C. Soci, A. Zhang, X.-Y. Bao, H. Kim, Y. Lo, and D. Wang, "Nanowire Photodetectors," *Journal of Nanoscience and Nanotechnology*, vol. 10, no. 3, pp. 1430-1449, // 2010, doi: 10.1166/jnn.2010.2157.

[25] K. Das, S. Samanta, P. Kumar, K. S. Narayan, and A. K. Raychaudhuri, "Fabrication of Single Si Nanowire Metal–Semiconductor–Metal Device for Photodetection," *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1444-1450, 2014, doi: 10.1109/TED.2014.2312234.

[26] D. Hall, Y. Liu, L. Yan, Y. Yu, and Y. Lo, "Approaching the Quantum Limit of Photodetection in Solid-State Photodetectors," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 4812-4822, 2017, doi: 10.1109/TED.2017.2762722.

[27] L. Shen, E. Y. B. Pun, and J. C. Ho, "Recent developments in III–V semiconducting nanowires for high-performance photodetectors," *Materials Chemistry Frontiers*, 10.1039/C6QM00279J vol. 1, no. 4, pp. 630-645, 2017, doi: 10.1039/C6QM00279J.

[28] Y. Dan, X. Zhao, and A. Mesli, "A Photoconductor Intrinsically Has No Gain," *ACS Photonics*, vol. 5, 11/10 2015, doi: 10.1021/acsphotonics.8b00805.

[29] K. Chen, X. Zhao, A. Mesli, Y. He, and Y. Dan, "Dynamics of Charge Carriers in Silicon Nanowire Photoconductors Revealed by Photo Hall Effect Measurements," *ACS nano,* vol. 12 4, pp. 3436-3441, 2018.

[30] P. Shen *et al.,* "Implementation of Chip-Level Optical Interconnect With Laser and Photodetector Using SOI-Based 3-D Guided-Wave Path," *IEEE Photonics Journal,* vol. 6, no. 6, pp. 1-10, 2014, doi: 10.1109/JPHOT.2014.2366165.

[31] A. C. Farrell, "Design and Performance of Near-Infrared Nanowire Photodetectors," Doctor of Philosophy, Electrical Engineering, University of California, Los Angeles

Los Angeles, California, 2017.

[32] W. Shu and K. Sung-Mo, "Modeling and simulation of metal-semiconductor-metal photodetector using VHDL-AMS," in *Proceedings of the 2004 IEEE International Behavioral Modeling and Simulation Conference, 2004. BMAS 2004.*, 22-22 Oct. 2004 2004, pp. 59-63, doi: 10.1109/BMAS.2004.1393983.

[33] X. Zhang and S. T. Pantelides, "Theory of space charge limited currents," (in English), *Physical Review Letters,* vol. 108, p. Medium: X; Size: 266602, 2012, doi: 10.1103/PhysRevLett.108.266602.

[34] C. Soci *et al.,* "ZnO Nanowire UV Photodetectors with High Internal Gain," *Nano Letters,* vol. 7, no. 4, pp. 1003-1009, 2007/04/01 2007, doi: 10.1021/nl070111x.

[35] N. K. Sze SM, *Physics of Semiconductor Devices.* New York: Wiley & Sons, 2007.

[36] T. Shinada, S. Okamoto, T. Kobayashi, and I. Ohdomari, "Enhancing semiconductor device performance using ordered dopant arrays," *Nature,* vol. 437, no. 7062, pp. 1128-1131, 2005/10/01 2005, doi: 10.1038/nature04086.

[37] M. D. Marchi *et al.,* "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in *2012 International Electron Devices Meeting*, 10-13 Dec. 2012 2012, pp. 8.4.1-8.4.4, doi: 10.1109/IEDM.2012.6479004.

[38] T. Ernst, "Controlling the Polarity of Silicon Nanowire Transistors," *Science,* vol. 340, no. 6139, pp. 1414-1415, 2013, doi: doi:10.1126/science.1238630.

[39] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors," *Nature,* vol. 479, no. 7373, pp. 310-316, 2011/11/01 2011, doi: 10.1038/nature10676.

[40] A. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature,* vol. 479, pp. 329-37, 11/16 2011, doi: 10.1038/nature10679.

[41] G. E. Moore, "Cramming More Components Onto Integrated Circuits," *Proceedings of the IEEE,* vol. 86, no. 1, pp. 82-85, 1998, doi: 10.1109/JPROC.1998.658762.

[42] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High Performance Silicon Nanowire Field Effect Transistors," *Nano Letters,* vol. 3, p. 149, February 01, 2003 2003, doi: 10.1021/nl025875l.

[43] P. Kuo, Y. Lu, and T. Chao, "High-Performance GAA Sidewall-Damascened Sub-10-nm <italic>In Situ</italic> n⁺-Doped Poly-Si NWs Channels Junctionless FETs," *IEEE Transactions on Electron Devices,* vol. 61, no. 11, pp. 3821-3826, 2014, doi: 10.1109/TED.2014.2354436.

[44] H. Ko *et al.,* "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," *Nature,* vol. 468, no. 7321, pp. 286-289, 2010/11/01 2010, doi: 10.1038/nature09541.

[45] H. Afzali-Kusha, A. Shafaei, and M. Pedram, "A 125mV 2ns-access-time 16Kb SRAM design based on a 6T hybrid TFET-FinFET cell," in *2018 19th International Symposium on Quality Electronic Design (ISQED)*, 13-14 March 2018 2018, pp. 280-285, doi: 10.1109/ISQED.2018.8357301.

[46] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and W. Hon-Sum Philip, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259-288, 2001, doi: 10.1109/5.915374.

[47] K. Bernstein *et al.*, "High-performance CMOS variability in the 65-nm regime and beyond," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 433-449, 2006, doi: 10.1147/rd.504.0433.

[48] W. Haensch *et al.*, "Silicon CMOS devices beyond scaling," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 339-361, 2006, doi: 10.1147/rd.504.0339.

[49] N. F. G. Mott, R.W *Electronic Processes in Ionic Crystals*, 2nd ed. Oxford, London: Oxford University Press, 1948.

[50] X. Zhang, D. Connelly, H. Takeuchi, M. Hytha, R. J. Mears, and T. K. Liu, "Comparison of SOI Versus Bulk FinFET Technologies for 6T-SRAM Voltage Scaling at the 7-/8-nm Node," *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 329-332, 2017, doi: 10.1109/TED.2016.2626397.

[51] M. Mongillo, P. Spathis, G. Katsaros, P. Gentile, and S. De Franceschi, "Multifunctional Devices and Logic Gates With Undoped Silicon Nanowires," *Nano Letters*, vol. 12, no. 6, pp. 3074-3079, 2012/06/13 2012, doi: 10.1021/nl300930m.

[52] H. Kind, H. Yan, B. Messer, M. Law, and P. Yang, "Nanowire Ultraviolet Photodetectors and Optical Switches," *Advanced Materials*, vol. 14, no. 2, pp. 158-160, 2002, doi: 10.1002/1521-4095(20020116)14:2<158::Aid-adma158>3.0.Co;2-w.

[53] O. Madelung, *Semiconductors: Data Handbook*, 3rd ed. ed. Springer, 2004.

[54] M. S. M. E. Levinstein, and S. L. Rumyantsev, *Handbook Series on Semiconductor Parameters*. World Scientific, 1996.

[55] R. Landauer, "Spatial Variation of Currents and Fields Due to Localized Scatterers in Metallic Conduction," *IBM Journal of Research and Development*, vol. 1, no. 3, pp. 223-231, 1957.

[56] Synopsys Sentaurus TCAD [Online] Available: https://www.synopsys.com/silicon/tcad/device-simulation/sentaurus-device.html

[57] Synopsys. Sentaurus™ Device User Guide [Online] Available: https://www.synopsys.com/silicon/tcad/device-simulation/sentaurus-device.html

[58] Y.-C. W. Y.-R. Jhan, *3D TCAD Simulation for CMOS Nanoeletronic Devices*. Springer, 2018.

[59] A. Schenk and S. Müller, "Analytical Model of the Metal-Semiconductor Contact for Device Simulation," 1993.

[60] C. Chi On, A. K. Okyay, and K. C. Saraswat, "Effective dark current suppression with asymmetric MSM photodetectors in Group IV semiconductors," *IEEE Photonics Technology Letters*, vol. 15, no. 11, pp. 1585-1587, 2003, doi: 10.1109/LPT.2003.818683.

[61] A. Garg and T. T. Kim, "SRAM Array Structures for Energy Efficiency Enhancement," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 6, pp. 351-355, 2013, doi: 10.1109/TCSII.2013.2258247.

[62] N. Kaur, N. Gupta, H. Pahuja, B. Singh, and S. Panday, "Low Power FinFET based 10T SRAM cell," in *2016 Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH)*, 18-19 Nov. 2016 2016, pp. 227-233, doi: 10.1109/CIPECH.2016.7918772.

[63] C. U. V. Workshop). Code Optimization: Memory Hierarchy [Online] Available: https://cvw.cac.cornell.edu/codeopt/memhier

[64] S. Gu, E. H. Sha, Q. Zhuge, Y. Chen, and J. Hu, "A Time, Energy, and Area Efficient Domain Wall Memory-Based SPM for Embedded Systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 12, pp. 2008-2017, Dec. 2016, doi: 10.1109/TCAD.2016.2547903, doi: 10.1109/TCAD.2016.2547903.

[65] F. Menichelli and M. Olivieri, "Static Minimization of Total Energy Consumption in Memory Subsystem for Scratchpad-Based Systems-on-Chips," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 2, pp. 161-171, 2009, doi: 10.1109/TVLSI.2008.2001940.

[66] R. Sinha and P. Samanta, "Analysis of stability and different speed boosting assist techniques towards the design and optimization of high speed SRAM cell," in *2015 19th International Symposium on VLSI Design and Test*, 26-29 June 2015 2015, pp. 1-6, doi: 10.1109/ISVDAT.2015.7208097.

[67] K. Ma *et al.*, "Independently-Controlled-Gate FinFET 6T SRAM Cell Design for Leakage Current Reduction and Enhanced Read Access Speed," in *2014 IEEE Computer Society Annual Symposium on VLSI*, 9-11 July 2014 2014, pp. 296-301, doi: 10.1109/ISVLSI.2014.25.

[68] R. M. Premavathi, Q. Tong, K. Choi, and Y. Lee, "A low power, high speed FinFET based 6T SRAM cell with enhanced write ability and read stability," in *2016 International SoC Design Conference (ISOCC)*, 23-26 Oct. 2016 2016, pp. 311-312, doi: 10.1109/ISOCC.2016.7799802.

[69] M. Rahaman and R. Mahapatra, "Design of a 32nm independent gate FinFET based SRAM cell with improved noise margin for low power application," in *2014 International Conference on Electronics and Communication Systems (ICECS)*, 13-14 Feb. 2014 2014, pp. 1-5, doi: 10.1109/ECS.2014.6892721.

[70] S. Saxena and R. Mehra, "Low-power and high-speed 13T SRAM cell using FinFETs," *IET Circuits, Devices & Systems*, vol. 11, no. 3, pp. 250-255, 2017, doi: 10.1049/iet-cds.2016.0287.

[71] S. Strangio, P. Palestri, D. Esseni, L. Selmi, and F. Crupi, "Analysis of TFET based 6T SRAM cells implemented with state of the art silicon nanowires," in *2014 44th European Solid State Device Research Conference (ESSDERC)*, 22-26 Sept. 2014 2014, pp. 282-285, doi: 10.1109/ESSDERC.2014.6948815.

[72] M. Yabuuchi *et al.*, "16 nm FinFET High-k/Metal-gate 256-kbit 6T SRAM macros with wordline overdriven assist," in *2014 IEEE International Electron Devices Meeting*, 15-17 Dec. 2014 2014, pp. 3.3.1-3.3.3, doi: 10.1109/IEDM.2014.7046972.

[73] X. Zhang *et al.*, "Analysis of 7/8-nm Bulk-Si FinFET Technologies for 6T-SRAM Scaling," *IEEE Transactions on Electron Devices*, vol. 63, no. 4, pp. 1502-1507, 2016, doi: 10.1109/TED.2016.2523885.

[74] M. Chen *et al.*, "A 10 nm Si-based bulk FinFETs 6T SRAM with multiple fin heights technology for 25% better static noise margin," in *2013 Symposium on VLSI Technology*, 11-13 June 2013 2013, pp. T218-T219.

[75] Z. Jakšić and R. Canal, "Enhancing 6T SRAM cell stability by back gate biasing techniques for10nm SOI FinFETs under process and environmental variations," in *Proceedings of the 19th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2012*, 24-26 May 2012 2012, pp. 103-108.

[76] S. Ranganath, M. S. Bhat, and A. C. Fernandes, "Design of low leakage SRAM bit-cell and array," in *International Conference on Circuits, Communication, Control and Computing*, 21-22 Nov. 2014 2014, pp. 5-8, doi: 10.1109/CIMCA.2014.7057744.

[77] P. K. Sahu, Sunny, Y. Kumar, and V. N. Mishra, "Design and simulation of low leakage SRAM cell," in *2016 3rd International Conference on Devices, Circuits and Systems (ICDCS)*, 3-5 March 2016 2016, pp. 73-77, doi: 10.1109/ICDCSyst.2016.7570628.

[78] N. N. Mojumder and K. Roy, "Band-to-Band Tunneling Ballistic Nanowire FET: Circuit-Compatible Device Modeling and Design of Ultra-Low-Power Digital Circuits and Memories," *IEEE Transactions on Electron Devices*, vol. 56, no. 10, pp. 2193-2201, 2009, doi: 10.1109/TED.2009.2028394.

[79] L. Wang, A. Shafaei, and M. Pedram, "Gate-all-around FET based 6T SRAM design using a device-circuit co-optimization framework," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 6-9 Aug. 2017 2017, pp. 1113-1116, doi: 10.1109/MWSCAS.2017.8053123.

[80] O. Prakash, S. Maheshwaram, M. Sharma, A. Bulusu, and S. K. Manhas, "Performance and Variability Analysis of SiNW 6T-SRAM Cell Using Compact Model With Parasitics," *IEEE Transactions on Nanotechnology*, vol. 16, no. 6, pp. 965-973, 2017, doi: 10.1109/TNANO.2017.2735900.

[81] D. Nagy, G. Indalecio, A. J. García-Loureiro, M. A. Elmessary, K. Kalna, and N. Seoane, "FinFET Versus Gate-All-Around Nanowire FET: Performance, Scaling, and Variability," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 332-340, 2018, doi: 10.1109/JEDS.2018.2804383.

[82] A. Shafaei, H. Afzali-Kusha, and M. Pedram, "Minimizing the energy-delay product of SRAM arrays using a device-circuit-architecture co-optimization framework," in *2016 53nd ACM/EDAC/IEEE Design Automation Conference (DAC)*, 5-9 June 2016 2016, pp. 1-6, doi: 10.1145/2897937.2898044.

[83] H. J. David Hodges, Resve Saleh, r. Edition, Ed. *Analysis and Design of Digital Integrated Circuits*. Mc Graw Hill Higher Education, 2004.

[84] R. J. Evans and P. D. Franzon, "Energy consumption modeling and optimization for SRAM's," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 5, pp. 571-579, 1995, doi: 10.1109/4.384170.

[85] D. M. H. Neil H. E. Weste, *CMOS VLSI Design A Circuit and Systems Perspective*, Fourth ed. Addison-Wesley Pearson, 2011.

[86] D. E. Gautam Kumar, Sevya Multimedia Technologies Pvt. Ltd. "Design and Simulation of 1K * 32 bit SRAM memory design." https://github.com/gautam19499/6T-SRAM_cell_design (accessed.

[87] I. U. STMicro. Array Structured Memories [Online] Available: https://www.slideserve.com/tasya/array-structured-memories

[88] S. E. Adapted from Rabaey's Digital Integrated Circuits, ©2003 J. Rabaey, A. Chandrakasan, B. Nikolic. Lecture: Peripheral Memory Circuits; Pennsylvania State University [Online] Available: https://www.cse.psu.edu/~kxc104/class/cmpen411/14f/lec/C411L24MemoryPeripheral.pdf

[89] A. K. Singh, M.-S. Saadatzi, and C. Venkataseshaiah, "Design of Peripheral Circuits for the Implementation of Memory Array Using Data-Aware (DA) SRAM Cell in 65 nm CMOS Technology for Low Power Consumption," *Journal of Low Power Electronics*, vol. 12, no. 1, pp. 9-20, // 2016, doi: 10.1166/jolpe.2016.1417.

[90] E. Sicard, "Introducing 10-nm FinFET technology in Microwind," 2017-06-06, 2017.

[91] K. Puttaswamy and G. H. Loh, "3D-Integrated SRAM Components for High-Performance Microprocessors," *IEEE Transactions on Computers*, vol. 58, no. 10, pp. 1369-1381, 2009, doi: 10.1109/TC.2009.92.

[92] R. A. Burange and G. H. Agrawal, "Optimization of 1KByte 6T SRAM using block partitioning method and gated Vdd concept," 2019.

[93] A. Calimera, A. Macii, E. Macii, and M. Poncino, "Design Techniques and Architectures for Low-Leakage SRAMs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 9, pp. 1992-2007, 2012, doi: 10.1109/TCSI.2012.2185303.

[94] P. a. K. Bikki, P., "SRAM Cell Leakage Control Techniques for Ultra Low Power Application: A survey," *Circuits and Systems*, vol. 8, pp. 23-52, Feb. 2017, doi: 10.4236/cs.2017.82003.

[95] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305-327, 2003, doi: 10.1109/JPROC.2002.808156.

[96] K. Ohashi *et al.*, "On-Chip Optical Interconnect," *Proceedings of the IEEE*, vol. 97, no. 7, pp. 1186-1198, 2009, doi: 10.1109/JPROC.2009.2020331.

[97] J. T. Kim and S. Park, "The Design and Analysis of Monolithic Integration of CMOS-Compatible Plasmonic Waveguides for On-Chip Electronic–Photonic Integrated Circuits," *Journal of Lightwave Technology*, vol. 31, no. 18, pp. 2974-2981, 2013, doi: 10.1109/JLT.2013.2276761.

[98] T. Spuesens, J. Bauwelinck, P. Regreny, and D. V. Thourhout, "Realization of a Compact Optical Interconnect on Silicon by Heterogeneous Integration of III–V," *IEEE Photonics Technology Letters*, vol. 25, no. 14, pp. 1332-1335, 2013, doi: 10.1109/LPT.2013.2264664.

[99] L. Czornomaz *et al.*, "First demonstration of InGaAs/SiGe CMOS inverters and dense SRAM arrays on Si using selective epitaxy and standard FEOL processes," in *2016 IEEE Symposium on VLSI Technology*, 14-16 June 2016 2016, pp. 1-2, doi: 10.1109/VLSIT.2016.7573391.

[100] M. Li, J. Ling, Y. He, U. A. Javid, S. Xue, and Q. Lin, "Lithium niobate photonic-crystal electro-optic modulator," *Nature Communications*, vol. 11, no. 1, p. 4123, 2020/08/17 2020, doi: 10.1038/s41467-020-17950-7.

[101] B. Nikolić. Advanced Digital Circuits Lecture 2 – Scaling Trends [Online] Available: https://inst.eecs.berkeley.edu/~ee241/sp20/Lectures/Lecture1-Intro-annotated.pdf

[102] W. C. Jeong *et al.*, "True 7nm Platform Technology featuring Smallest FinFET and Smallest SRAM cell by EUV, Special Constructs and 3rd Generation Single Diffusion

Break," in *2018 IEEE Symposium on VLSI Technology*, 18-22 June 2018 2018, pp. 59-60, doi: 10.1109/VLSIT.2018.8510682.

[103] T. Tsuchizawa *et al.*, "Microphotonics devices based on silicon microfabrication technology," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 11, no. 1, pp. 232-240, 2005, doi: 10.1109/JSTQE.2004.841479.

[104] W. D. Sacher *et al.*, "Monolithically Integrated Multilayer Silicon Nitride-on-Silicon Waveguide Platforms for 3-D Photonic Circuits and Devices," *Proceedings of the IEEE,* vol. 106, no. 12, pp. 2232-2245, 2018, doi: 10.1109/JPROC.2018.2860994.

[105] W. Xiong *et al.*, "Integration of silicon nitride waveguide in Ge-on-insulator substrates for monolithic solutions in optoelectronics," *Journal of Materials Science: Materials in Electronics,* vol. 32, no. 5, pp. 6133-6140, 2021/03/01 2021, doi: 10.1007/s10854-021-05331-9.

[106] Z. Yan *et al.*, "A monolithic InP/SOI platform for integrated photonics," *Light: Science & Applications,* vol. 10, no. 1, p. 200, 2021/09/26 2021, doi: 10.1038/s41377-021-00636-0.

[107] D. J. Blumenthal, R. Heideman, D. Geuzebroek, A. Leinse, and C. Roeloffzen, "Silicon Nitride in Silicon Photonics," *Proceedings of the IEEE,* vol. 106, no. 12, pp. 2209-2231, 2018, doi: 10.1109/JPROC.2018.2861576.

[108] P. Muñoz *et al.*, "Foundry Developments Toward Silicon Nitride Photonics From Visible to the Mid-Infrared," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 25, no. 5, pp. 1-13, 2019, doi: 10.1109/JSTQE.2019.2902903.

[109] C. Xiang, W. Jin, and J. E. Bowers, "Silicon nitride passive and active photonic integrated circuits: trends and prospects," *Photon. Res.,* vol. 10, no. 6, pp. A82-A96, 2022/06/01 2022, doi: 10.1364/PRJ.452936.

[110] I. Synopsys. Photonic Solutions, RSoft CAD, User Guide [Online] Available: https://www.synopsys.com/photonic-solutions/rsoft-photonic-device-tools/rsoft-products.html

[111] R. W. Mann and B. H. Calhoun, "New category of ultra-thin notchless 6T SRAM cell layout topologies for sub-22nm," in *2011 12th International Symposium on Quality Electronic Design*, 14-16 March 2011 2011, pp. 1-6, doi: 10.1109/ISQED.2011.5770761.

[112] R. S. Quimby, *Photonics and Lasers An Introduction*. JOHN WILEY & SONS, INC., 2006.

[113] J.-m. Liu, *Photonic Devices*. Cambridge: Cambridge University Press, 2005.

[114] S. Khan, S. M. Buckley, J. Chiles, R. P. Mirin, S. W. Nam, and J. M. Shainline, "Low-loss, high-bandwidth fiber-to-chip coupling using capped adiabatic tapered fibers," *APL Photonics,* vol. 5, no. 5, p. 056101, 2020, doi: 10.1063/1.5145105.

[115] J. Fu, Y. Chen, Y. Huang, Y. Han, L. Yang, and J. Yu, "A High-efficiency Waveguide Coupling Structure Using Hybrid Multi-core Layer," in *2020 Opto-Electronics and Communications Conference (OECC)*, 4-8 Oct. 2020 2020, pp. 1-3, doi: 10.1109/OECC48412.2020.9273732.

[116] S. Gupta, K. Gupta, and N. Pandey, "Performance evaluation of SRAM cells for deep submicron technologies," in *2016 Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH)*, 18-19 Nov. 2016 2016, pp. 292-296, doi: 10.1109/CIPECH.2016.7918785.

[117] J. Wang, S. Nalam, and B. H. Calhoun, "Analyzing static and dynamic write margin for nanometer SRAMs," in *Proceeding of the 13th international symposium on Low power*

electronics and design (ISLPED '08), 11-13 Aug. 2008 2008, pp. 129-134, doi: 10.1145/1393921.1393954.

[118] C. D. C. Arandilla, A. B. Alvarez, and C. R. K. Roque, "Static Noise Margin of 6T SRAM Cell in 90-nm CMOS," in *2011 UkSim 13th International Conference on Computer Modelling and Simulation*, 30 March-1 April 2011 2011, pp. 534-539, doi: 10.1109/UKSIM.2011.108.

[119] R. Saeidi, M. Sharifkhani, and K. Hajsadeghi, "Statistical Analysis of Read Static Noise Margin for Near/Sub-Threshold SRAM Cell," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 12, pp. 3386-3393, 2014, doi: 10.1109/TCSI.2014.2327334.

[120] G. Cihun-Siyong Alex, H. Ci-Tong, Y. Kai-Wen, S. Muh-Tian, and C. Kuo-Hsing, "A compact and low-power SRAM with improved read static noise margin," in *2008 15th IEEE International Conference on Electronics, Circuits and Systems*, 31 Aug.-3 Sept. 2008 2008, pp. 546-549, doi: 10.1109/ICECS.2008.4674911.

[121] V. MalleshaiahG., "Study of SRAM Cell for Balancing Read and Write Margins in Sub-100nm Technology using Noise-Curve Method," 2018.

[122] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2577-2588, 2006, doi: 10.1109/JSSC.2006.883344.

[123] N. Rahman and B. P. Singh, "Static-Noise-Margin Analysis of Conventional 6T SRAM Cell at 45nm Technology," *International Journal of Computer Applications*, vol. 66, pp. 19-23, 2013.

[124] T. Y. Li, C. H. Hwang, and Y. Li, "Process-variation- and random-dopant-induced static noise margin fluctuation in nanoscale CMOS and FinFET SRAM cells," in *2009 1st Asia Symposium on Quality Electronic Design*, 15-16 July 2009 2009, pp. 24-27, doi: 10.1109/ASQED.2009.5206305.

[125] A. Sachdeva and V. K. Tomar, "Noise margin enhancement of Conventional 6T SRAM Cell by aspect Ratio Optimization," in *2021 10th IEEE International Conference on Communication Systems and Network Technologies (CSNT)*, 18-19 June 2021 2021, pp. 264-268, doi: 10.1109/CSNT51715.2021.9509552.

[126] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, 1987, doi: 10.1109/JSSC.1987.1052809.

[127] C. Galup and M. Schneider, "The compact all-region MOSFET model: theory and applications," in *2018 16th IEEE International New Circuits and Systems Conference (NEWCAS)*, 24-27 June 2018 2018, pp. 166-169, doi: 10.1109/NEWCAS.2018.8585657.

[128] X. Liu *et al.*, "An Improved Drain-Current Model for FinFETs," in *2020 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, 7-9 Dec. 2020 2020, pp. 1-3, doi: 10.1109/NEMO49486.2020.9343580.

[129] A. Tsormpatzoglou, N. Fasarakis, D. H. Tassis, I. Pappas, K. Papathanasiou, and C. A. Dimitriadis, "Analytical unified drain current model of long-channel tri-gate FinFETs," in *2012 28th International Conference on Microelectronics Proceedings*, 13-16 May 2012 2012, pp. 115-118, doi: 10.1109/MIEL.2012.6222810.