# FUNDAMENTALS OF SOLAR CELLS AND ADVANCEMENTS IN COPPER CONTACTS

by

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A thesis submitted to the faculty of
The University of North Carolina at Charlotte
in partial fulfillment of the requirements
for the degree of Master of Science in
Electrical Engineering

Charlotte

2021

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# ABSTRACT

SARAH JULIANA GREMPELS. Fundamentals of Solar Cells and Advancements in Copper Contacts. (Under the direction of DR. ABASIFREKE EBONG)

Almost all energy on Earth comes from the sun. Plants use it for photosynthesis, producing nourishment for animals and humans, who not only need the sun for food but also warmth. The sun is sustainable and inexhaustible, making it a renewable energy source. Solar Cells are photovoltaic devices, which harness the light given off by the sun and directly convert it into electricity. They are made up of P-N junctions from semiconductor materials. This material is able to absorb photons given off by the sunlight, which in turn raises an electron in the material to a higher energy state. This electron moves into an exterior circuit, where its energy dissipates and is harnessed. The electron then returns to the solar cell and the process is repeated.

This thesis fundamentally establishes an understanding of a solar cell by determining the characterization of a solar cell through open-circuit voltage, short circuit current, and fill factor. These factors are how efficiency is calculated and how different designs are evaluated. The focus is set on improving front metallization designs of solar cells. Griddler 2.5 is used to simulate different designs and compare their resulting numerical analysis. These designs focus on increasing efficiency and decreasing the amount of metal per unit cell by comparing uneven and even busbars, as well as tapered fingers and uniform fingers.

Finally, experimental data regarding the replacement of the traditional screen-printing Silver paste with atmospheric Copper paste will be discussed. The challenges of utilizing Cu due to oxidation, diffusion and degradation were overcome and the results show proof of successful contact between the Cu paste and the semiconductor material.

# DEDICATION

To my mom, the most inspiring person in my life. To my dad, for always supporting and believing in me. To my brother, serving as a Marine in Japan, for being so incredibly strong. And to Lucas, for listening and questioning everything I researched and helping me understand brand new concepts.

# ACKNOWLEDGEMENTS

First and foremost, I would like to thank Dr. Abasifreke Ebong, my mentor, who has greatly influenced this research. His passion, knowledge, and teachings of Solar Cells have been incredibly inspiring. I am so blessed to have had the opportunity to learn and be supported by him. Secondly, I would like to thank my thesis committee members, Dr. Farid Tranjan, and Dr. Yong Zhang that I have had the honor to work with. And lastly I would like to thank the Electrical Engineering Department of UNC Charlotte for supporting both my Bachelor and Masters of Science Degree in Electrical Engineering.

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# LIST OF ABBREVIATIONS

Ag An abbreviation for Silver

AM An acronym for Air Mass

BB An acronym for Bus Bar

Cu An abbreviation for Copper

ECE An acronym for Electrical and Computer Engineering.

EL An abbreviation for Electroluminescence

FF An acronym for Fill Factor

FGA An acronym for Forming Gas Anneal

Isc An abbreviation for short circuit Current

LED An acronym for Light Emitting Diode

Rs An abbreviation for series resistance

Rsh An abbreviation for shunt resistance

Si An abbreviation for Silicon

SRH An acronym for Shockley-Read-Hall

Voc An abbreviation for open circuit Voltage

# PREFACE

Climate change has been a hot topic around the world recently. The environment is being destroyed by the depletion of earth's resources due to population growth, new innovations, and the need to acquire more things. Industrialization has polluted the earth, plastics are filling the oceans, and animal agriculture has caused 91% of the deforestation of the Amazon. It is time to focus on taking action to reverse the damage that has been done. There are small actions that each person can take, like avoiding the utilization of single-use plastics, thinking more sustainably, buying long-term products, producing less trash, eating a more plant-based diet, and reducing energy consumption. While these are great starting points, leaders of the world need to make large-scale changes as well. Since technology is constantly evolving and gaining popularity, the need for electricity has increased. To respond to this consumer need, more research and development should be focused on renewable energy. This way consumers' needs can be answered, while simultaneously using a renewable resource that will help the planet, rather than abusing depleting resources in order to satisfy short-term gratification.

This leads to the proposal of this thesis which explores the intricate details of solar cells. How does a Solar Cell work, not only on the surface level but also the inner workings of the device and how one can manipulate the different variables and design highly efficient Solar Cells. The two focal points of research in solar cells are how to increase efficiency and how to decrease cost. The second most expensive portion of producing solar cells, is the silver paste used as front metallization. The research in this thesis will discuss how silver can be replaced with a much more affordable option, like copper. [20] Therefore, advancements on a atmospheric Cu paste for PERC solar cells are discussed, with details on why it works and how it is still efficient at converting sunlight into energy.

# CHAPTER 1: INTRODUCTION TO PHOTOVOLTAICS

Solar cells have come a long way from when they were first developed by Bell Laboratories in 1954 with only 6% efficiency to the National Renewable Energy Laboratory achieving a new world record for solar cell efficiency at 47.1% in 2019 [21] [22]. One of the key steps focused on is the metallization in the fabrication of crystalline silicon solar cells. Silver has been the most common metal used for metallization and the International Technology Roadmap for Photovoltaic (ITRPV) predicts it will continue to remain the trend in the years to come. [1]

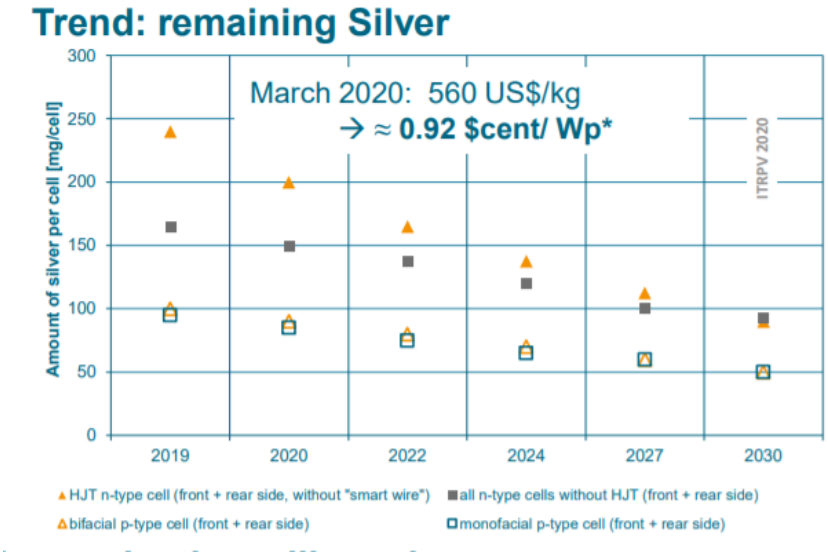



Figure 1.1: ITRPV Silver Trend Prediction [1]

Efficiency and cost are the two main challenges focused on in photovoltaic research. Since silver is a relatively expensive material, decreasing the amount utilized in each cell, or replacing it with a more affordable material, could decrease overall production costs. In Fig.1.1, ITRPV predicts that the amount of silver per cell will drop to approximately half of what it is now by the year 2030. Decreasing the amount of

Silver is possible through modifying the front metallization design. This is done by decreasing finger width from 40um to 20um and adding segmented bus bars. [1] ITRPV also predicts that the 3/4 BB designs will phase out, and 5BB+ is becoming more mainstream. This trend is shown in Fig.1.2, showing that by 2030 the 6BB+ design will have the largest world market share.

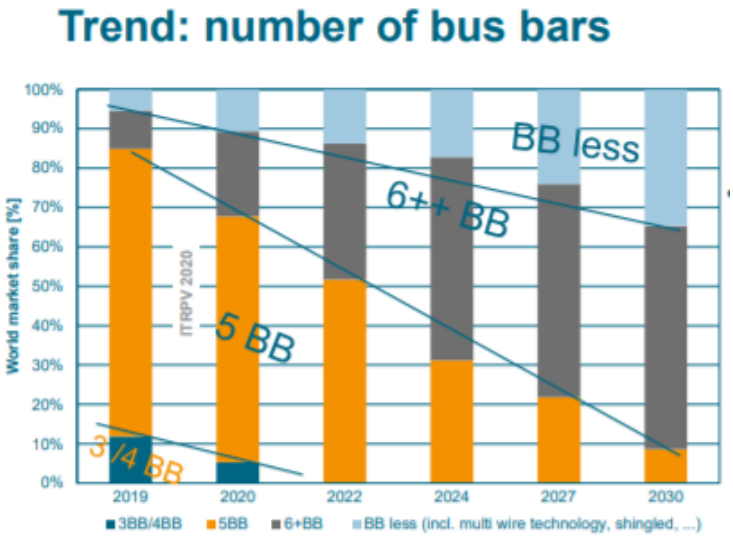



Figure 1.2: ITRPV Busbar Trend Prediction [1]

## 1.1 Semiconductors

A solar cell is a semiconductor device that converts sunlight into electricity without any polluting by-product. Semiconductors are made up of materials that can be formed from a variety of different element groups of the periodic table. The most common element, silicon, is a group IV element. Other semiconductor materials, compound semiconductors, can be made up of a combination of group III and group V elements (III-V semiconductors) or group II and group VI elements (II-VI semiconductors). Figure 1.3 displays the Periodic Table of Elements showing the various elements that can be used to make the different semiconductor materials.

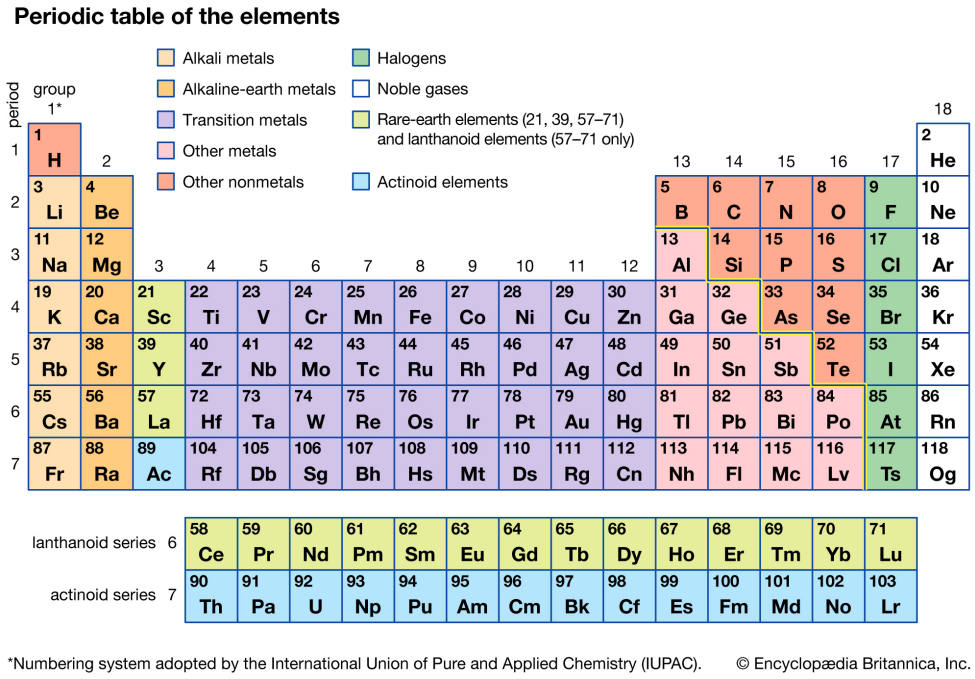



Figure 1.3: Periodic Table of Elements [2]

The conductivity of a semiconductor enables these materials to be used as electrical devices. As the temperature of the material increases, the electrons around the semiconductor atoms break free from their covalent band and move freely around the lattice. The band gap, the number of electrons or holes, and the recombination of electrons or holes in response to light are the most important parameters of a semiconductor. [23] Figure 1.4 displays a band diagram of a typical semiconductor with conduction and valence band edge, Ec and Ev, respectively. The minimum amount of energy needed for an electron to break free is the band gap.

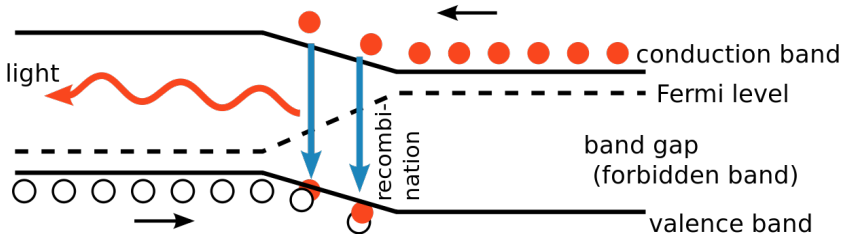



Figure 1.4: Band Diagram of a typical semiconductor [3]

The valence band is the lower energy level and the conduction band is where the electrons are considered to be free. The gap between the valence band and the conduction band is called the forbidden band. When an electron moves from the valence band to the conduction band, not only is it considered "free" and able to participate in conduction, but it also leaves behind a hole. This hole is an open space in which a neighboring atom can move into. The electrons and holes that are taking part in the conduction process are called intrinsic carriers. The temperature and the band gap of the semiconductor material determine the concentration of the intrinsic carriers, denoted by $n_i$. Figure 1.5 compares the band gap of a variety of semiconductor materials to its efficiency limits.

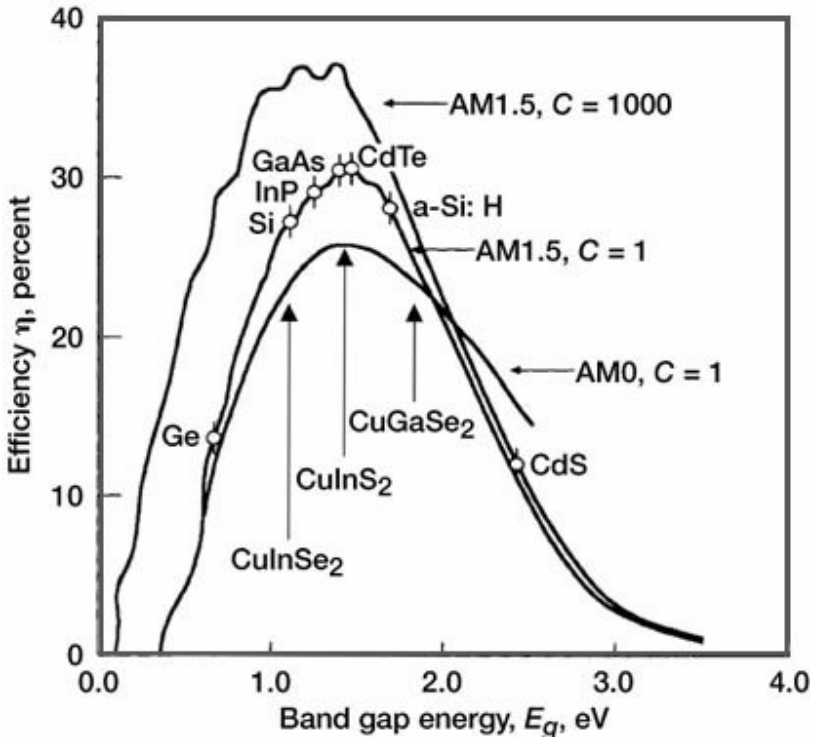



Figure 1.5: Efficiency as a function of band gap for a variety of semiconductor materials [4]

One method that can be used to change the natural number of electrons and holes in semiconductors is by doping the materials with other atoms. Doping can create N-type materials or P-type materials. N-type materials are produced by doping group IV semiconductors with group V atoms. By increasing the number of available electrons, the conductivity of the semiconductor increases. P-type materials are produced by doping group IV semiconductors with group III atoms. By increasing the number of holes, the conductivity of the semiconductor increases. [5] A schematic of both N-type and P-type doped semiconductor materials can be seen in Fig.1.6.

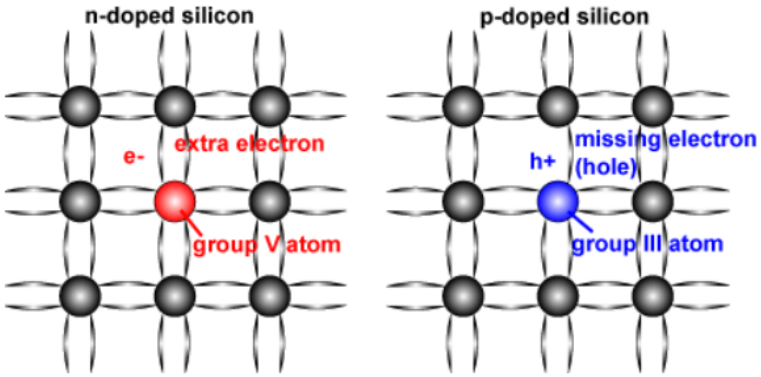



Figure 1.6: Schematic of N-type and P-type semiconductor material [5]

### 1.1.1 Energy Generation

For an electron to be excited into the conduction band, a photon of equal or greater energy than the band gap of the material needs to be absorbed by the material. Once this photon is absorbed, not only does it excite electrons but it also generates majority and minority carriers. This generation of carriers by photons is the basis of photovoltaics.

- $E_{ph} < E_G$ The interaction of photons with less energy $E_{ph}$ than the band gap energy $E_G$. These photons interact faintly with the semiconductor, mainly passing through the semiconductor as if they were transparent.

- $E_{ph} = E_G$ The interaction of photons with equal energy to the band gap have enough energy to create an electron-hole pair and absorb efficiently.

- $E_{ph} > E_G$ The interaction of photons with greater than energy to the band gap are actively absorbed. This is not ideal for photovoltaic devices since the photon energy greater than the band gap is wasted. These electrons quickly thermalize back down to the conduction band. [24]

Light has a variety of wavelengths. Therefore, light of different wavelengths can enter the material at different depths before it is absorbed. This property of semiconductors is the absorption coefficient, $\alpha$. The higher the absorption coefficient, the higher the probability of the absorption of photons. The wavelength ($\lambda$) and the extinction coefficient ($k$) are both used in Eq. 1.1 to calculate the absorption coefficient of a material. Figure 1.7 compares the wavelength in $nm$ of a variety of semiconductor materials with its absorption coefficient in $cm^{-1}$. The inverse of the absorption coefficient is the absorption depth. Blue light photons have a shorter absorption depth and red light photons have a greater absorption depth. This affects the thickness of the semiconductor material when designing a solar cell.

$$\alpha = \frac{4\pi k}{\lambda} \tag{1.1}$$

At any location within the solar cell, with any wavelength of light, the generation rate of producing an electron-hole pair can be calculated. Equation 1.2 is utilized to calculate the generation rate (G). X is the distance into the materials, and $N_0$ is the photon flux at the surface. This equation demonstrates that the highest generation rate is at the top surface of the solar cell.

$$G = \alpha N_0 e^{\alpha x} \tag{1.2}$$

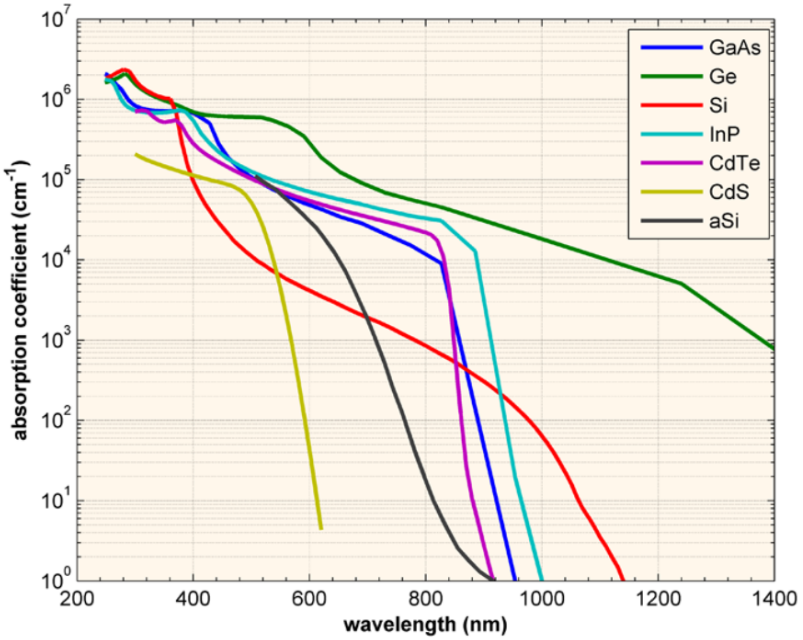



Figure 1.7: "The absorption coefficient, $\alpha$, in a variety of semiconductor materials at 300K as a function of the vacuum wavelength of light." [6]

### 1.1.2 Recombination

The opposite process of generation is recombination. Recombination occurs when energy is produced for either heat or light when an electron recombines with a hole. Recombination is a key component of a solar cell as it plays a role in the material's lifetime. There are three main types of recombination: Radiative recombination, Shockley-Read-Hall recombination, and Auger recombination. These three types of recombination are displayed in Fig.1.8.

Radiative recombination is also known as band-to-band recombination. It occurs when an electron from the conduction band combines with a hole in the valence band and then releases a photon. This recombination most commonly occurs in direct band gaps. Solar cells are made up of silicon which has indirect band gaps; therefore, the radiative recombination can usually be neglected. The most common semiconductor device in which radiative recombination occurs is a light-emitting diode (LED). Light

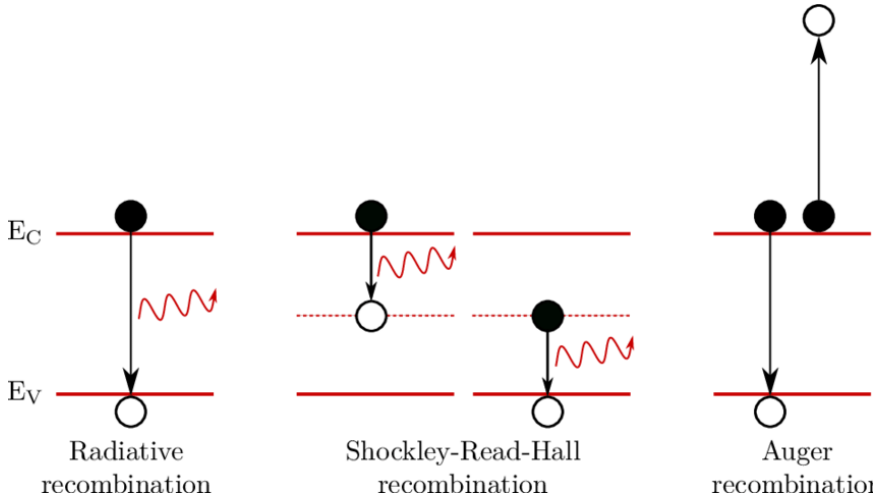



Figure 1.8: Radiative-, Shockley-Read-Hall-, and Auger recombination. [7]

is produced from the released photon. [25]

Shockley-Read-Hall (SRH) recombination occurs through defects in a material. Defects in the crystal lattice of the material cause an energy state to form in the forbidden region of the band gap. These defects can occur unintentionally or they can be created intentionally through doping. The energy state in the forbidden region causes electrons (or holes) to get trapped in the middle of the band gap. If another hole (or electron) moves to the same energy state, then the electron returns to the conduction band and recombines. [25]

Auger recombination is similar to radiative recombination. Though an electron and hole recombine, instead of releasing a photon, the energy is given to a different electron in the conduction band. This process is the most popular recombination within the silicon solar cells as it limits the lifetime and essentially the efficiency that can be produced. [25]

Lifetime is another important parameter of solar cells, as it directly impacts efficiency and is affected by recombination; specifically, the concentration of minority carriers. "The minority carrier lifetime of a material, denoted by $\tau_n$ or $\tau_p$, is the average time which a carrier can spend in an excited state after electron-hole generation

before it recombines" [26] Lifetime can be calculated in two different ways. In Eq.1.3 lifetime ($\tau$) is found by dividing the excess minority carrier concentration ($\Delta n$) by the recombination rate (R).

$$\tau = \frac{\Delta n}{R} \tag{1.3}$$

Since the lifetime is a combination of all the different recombination types, it can also be found using Eq.1.4.

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{Radiative}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} \tag{1.4}$$

The average length a carrier moves from being generated until it recombines is called the diffusion length (L). Higher diffusion lengths indicate a longer lifetime of a material. Diffusion length can be calculated by taking the square root of the product of diffusivity (D) and lifetime ($\tau$), see Eq.1.5. Diffusivity quantifies how fast a space is filled up with by a group of particles.

$$L = \sqrt{D\tau} \tag{1.5}$$

### 1.1.3 P-N Junctions

A P-N junction is formed when p-type and n-type semiconductor materials are joined together, forming a semiconductor diode. This formation causes surplus electrons in the n-type material to diffuse into the p-type material and surplus holes in the p-type material to diffuse into the n-type material. The diffusion of electrons into the n-type material leaves positive ions behind, and the diffusion of holes into the p-type material leaves negative ions behind. The ions left behind then create an electric field at the junction of these materials called the depletion region. This formation of the electric field produces a voltage. Figure 1.9 displays this P-N junction, in which the depletion region is referenced too as the space charge region.

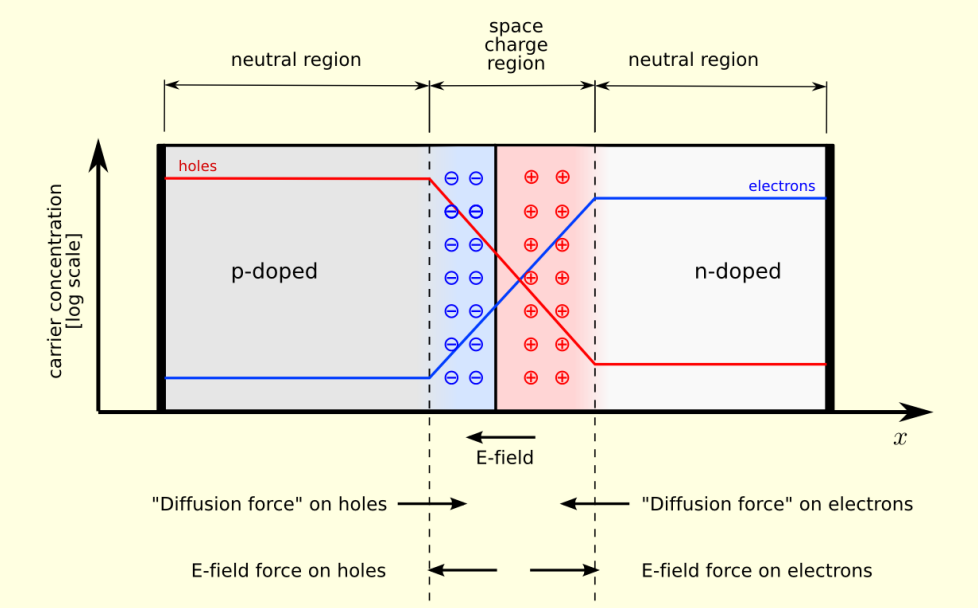



Figure 1.9: P-N Junction [8]

To generate power, current and voltage are needed. The photovoltaic effect is how a solar cell produces voltage. At the depletion region, diffusion and drift current can occur at equilibrium. Diffusion current occurs if carriers have sufficient energy to cross the depletion region and becoming minority carriers before they recombine. Drift current is the process of minority carriers being swept across the depletion region by the electric field when they reach the edge of the junction.

P-N junction diodes are the basis of operation for all electronic devices [27]. It is used for all forms of carrier transport, generation and recombination. There are three different modes that semiconductors operate in: thermal equilibrium, steady-state, and transient. Thermal equilibrium mode occurs when there is no net current within the device due to the currents balancing each other out. This occurs when there are no external inputs applied to the circuit. External inputs can include anything that alters the device, like light or voltage. Steady state is a mode in which the conditions of a device do not change over time, even though an external input is applied. Transient mode occurs when the applied voltage of the device changes quickly, causing a short

delay in the response of the device. Since solar cells generally have constant light, an external input, applied to them, they are considered steady state devices.

## 1.2 Fundamentals of Solar Cells

As sunlight enters the atmosphere, the sunlight gets absorbed, reflected, scattered, and diffused; reference Fig.1.10. A solar cell functions by absorbing direct sunlight from the sun and converting it into electricity.

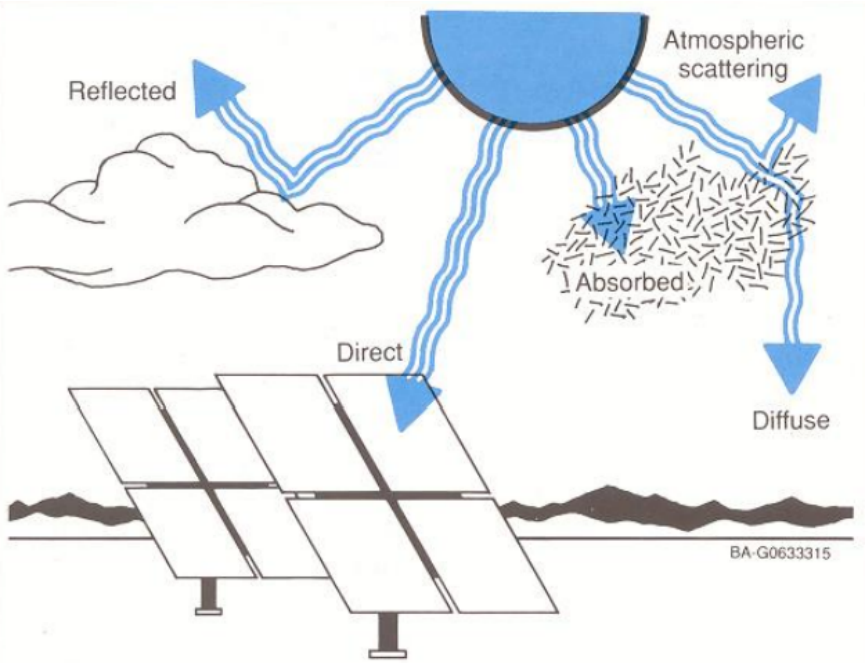



Figure 1.10: Absorption and Scattering of Sunlight by the Earth's Atmosphere [9]

There are four main steps to the operation of a Solar cell; these are light absorption, charge excitation, charge separation, and charge collection. The first step is for the sunlight to hit the solar cell. The photons from the sunlight then get absorbed by silicon, which is the semiconductor material used for solar cells. If the energy of the photons is equal to the energy of the band gap, the photons get absorbed to create free electrons. If the energy of the photon is less than the energy of the band gap, then the photons pass through the material. The free electrons form electron-hole pairs, leading to diffusion at the junction of the emitter (n-type) and base (p-type).

This charge separation causes the negatively charged electrons to separate from their atoms, creating an electric potential difference. This electric field pushes electrons in one direction and holes into the other direction to avoid recombination. To stabilize the electric potential difference, the current starts flowing through the material. The current is the free electron created in the base traveling through the wire, powering the external load. It continues traveling through the wire until it reaches the emitter, in which it recombines with a hole. [28] This is essentially how a solar cell converts sunlight to electricity, see Fig.1.11 for a cross-section of a solar cell.

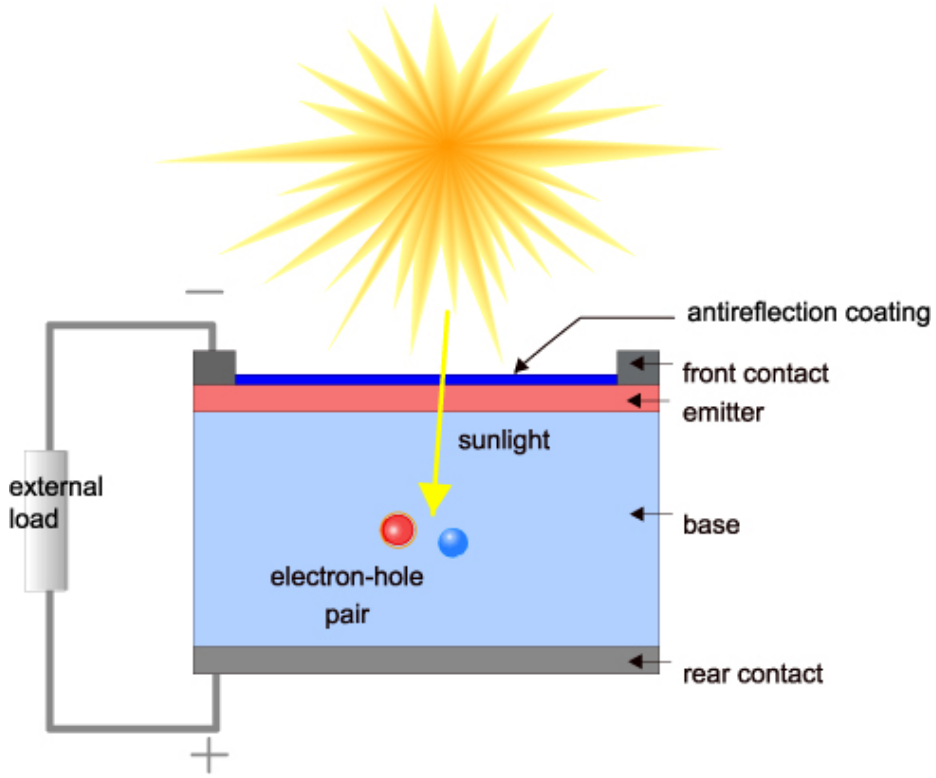



Figure 1.11: Cross-section of a solar cell [10]

## 1.3 Solar Cell Structures

The type of solar cell structure that will be focused on in this thesis is the passivated emitter and rear contacts (PERC) silicon solar cell. Figure 1.12 displays the structure of a PERC silicon solar cell on a p-type substrate. The PERC design offers a 21-

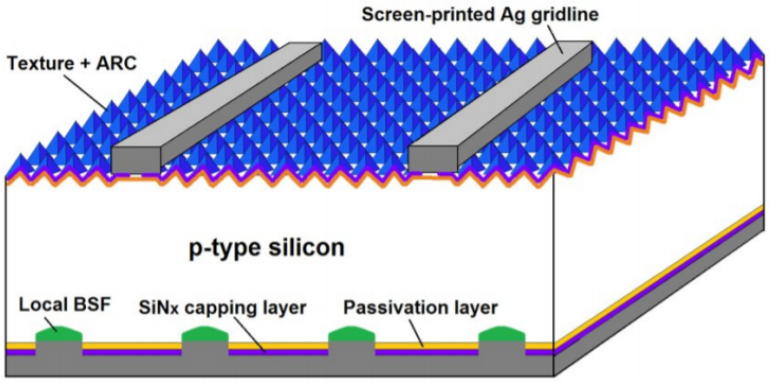



Figure 1.12: PERC Structure [11]

24% efficiency of commercial solar cells and according to the ITRPV, 20% of the PV industry in 2017 was comprised of PERC cells. Figure. 1.13 shows the road map that PERC cells will increase to take over 50% of the PV industries in the 2020s. [12] Alternatively, to the aluminum back surface field (Al-BSF) design shown in Fig. 1.14, the PERC design has an improved efficiency due to reduced rear-surface recombination and improved rear surface reflectivity. [29]

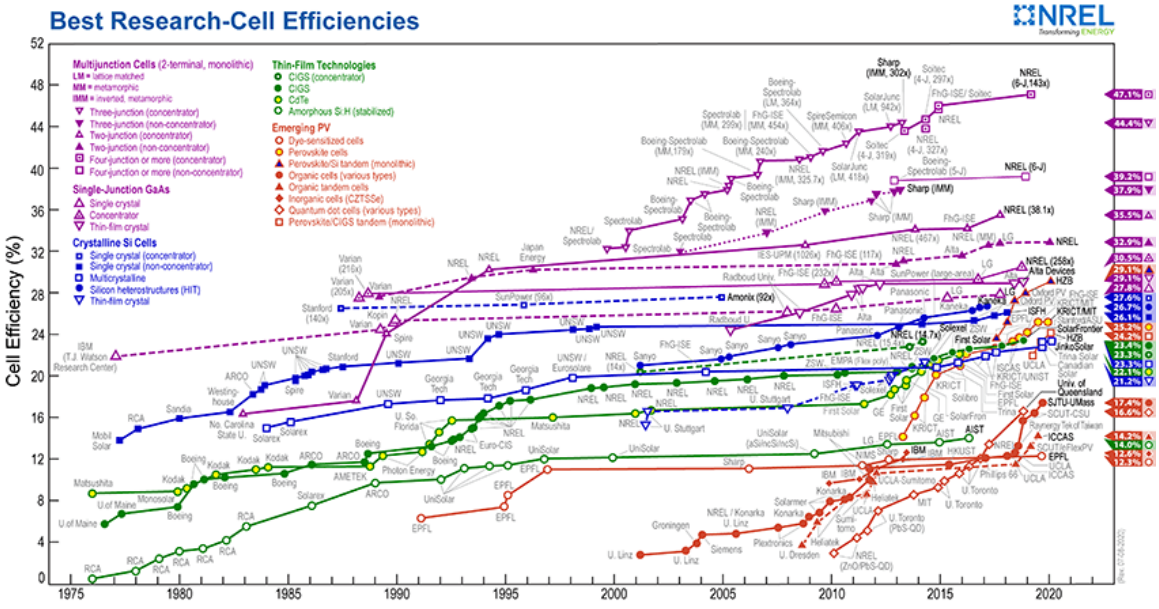



Figure 1.13: Best Research-Cell Efficiencies [12]

As described by Blaker's in the *Development of the PERC Solar Cell*, by using an aluminum reflector atop a rear passivation dielectric, the optical and recombination losses were greatly reduced in the PERC design compared to the Al-BSF.[29] Through an array of small holes in the dielectric covering of the rear surface, contact was accomplished between the silicon and aluminum. To reduce front surface reflectance losses, inverted pyramid texturing was added on the top of the cell through photolithography. This texturing produced a scattering of lights between the inverted pyramids, which improved light trapping. [29] A phosphorus emitter was also added to the front surface, which is heavier beneath the metal contacts and lowers the contact resistance, see Fig.1.22. Anti-reflective coating and thermal oxide passivation was also added to the front surface. By utilizing aluminum annealing or forming gas annealing (FGA) at 400°C, the oxide passivation of the front and rear surfaces was improved. [29]

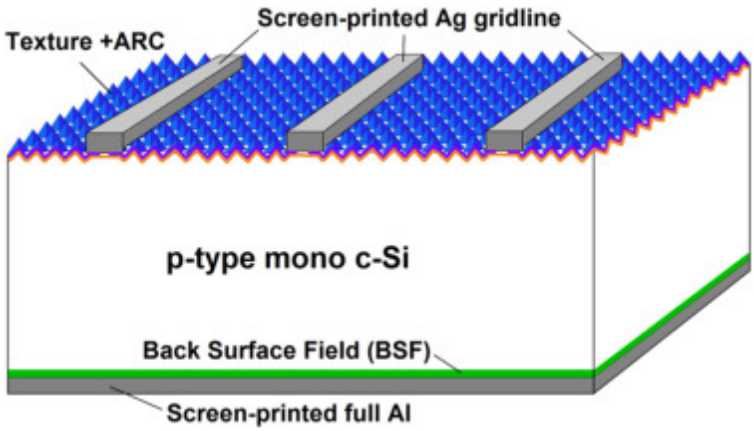



Figure 1.14: Al-BSF Structure [13]

## 1.4 Characterization of Solar Cells

Efficiency is the main characterization of a solar cell, but efficiency can be broken down into three main components. These are the fill factor (FF), the short circuit current ($I_{SC}$), and the open-circuit voltage ($V_{OC}$). These three components break up into many different variables as displayed by the fishbone diagram in Fig. 1.15. The

efficiency is the product of FF, $I_{SC}$, and $V_{OC}$ divided by the total input power, see Eq.1.6.

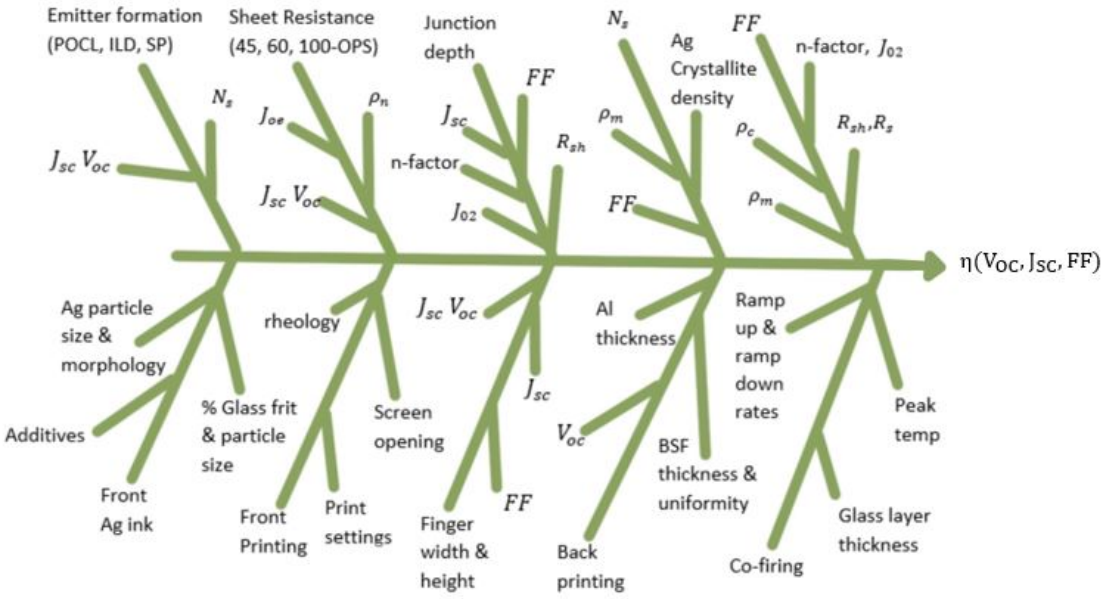



Figure 1.15: Parameters affecting efficiency [14]

$$\eta = \frac{Voc * Isc * FF}{Pin} \tag{1.6}$$

The $V_{OC}$ is at its maximum voltage point when the current is zero, and the $I_{SC}$ is at its maximum current point when the voltage is zero. The FF is a measure of the squareness of the IV-curve, see Fig.1.16. It is calculated by multiplying the maximum power voltage and maximum power current density and dividing it by the product of the open-circuit voltage and short circuit current, see Eq. 1.7.

$$FF = \frac{Vmp * Jmp}{Voc * Isc} \tag{1.7}$$

To achieve high efficiency, the values of $V_{OC}$, $I_{SC}$, and FF must be high. A way to increase the open-circuit voltage is to increase the shunt resistance ($R_{SH}$). Figure 1.17

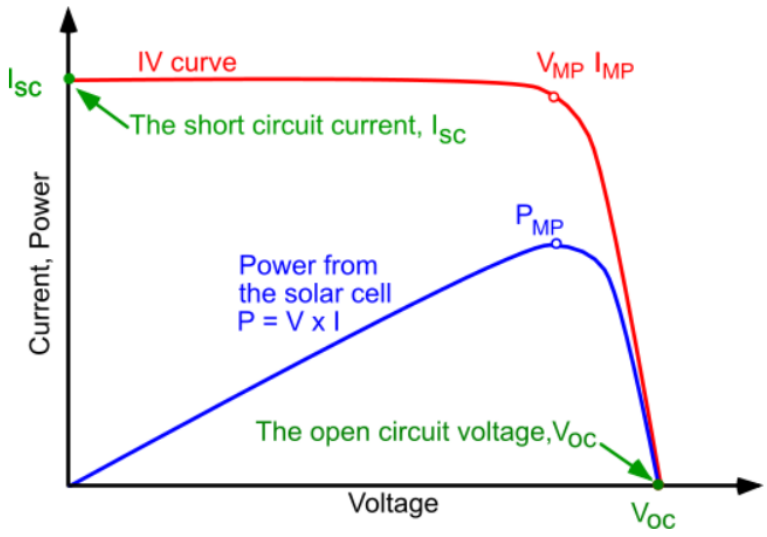



Figure 1.16: IV-Curve

shows an equivalent circuit diagram of a solar cell [15]. The circuit displays the P-N junction's shunt resistance and series resistance. Current will always take the path of least resistance, therefore increasing the shunt resistance will lead all current to flow through the series resistance ($R_S$) and avoid any voltage drops. A way to increase the shunt resistance is to ensure both the front and back surfaces of the solar cell have exceptional contact [15]. Good contact prevents any physical shorts of the p-type and n-type semiconductor material.

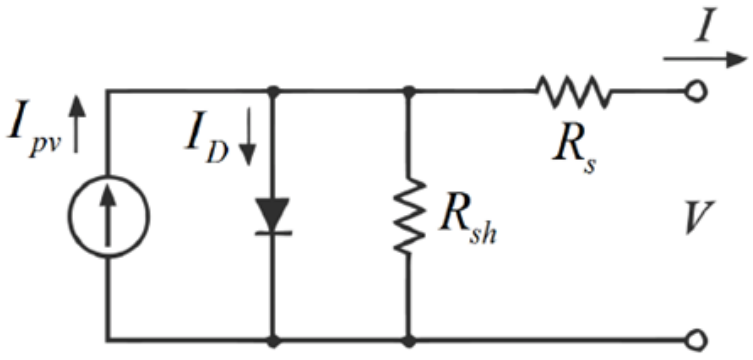



Figure 1.17: Solar Cell Equivalent Circuit

Fill factor is affected by the shunt and series resistance. To produce a high fill

factor, the series resistance should be low and the shunt resistance should be high. If the series resistance is low, the voltage drop across it will be low, reducing the Voc.

### 1.4.1 Series Resistance

Series resistance is made up of six different components: $R_1$- back contact resistance, $R_2$ - bulk semiconductor resistance, $R_3$ - emitter resistance, $R_4$ - contact resistance, $R_5$ - grid line resistance, $R_6$ - busbar resistance. These resistance values are displayed in Fig. 1.18.

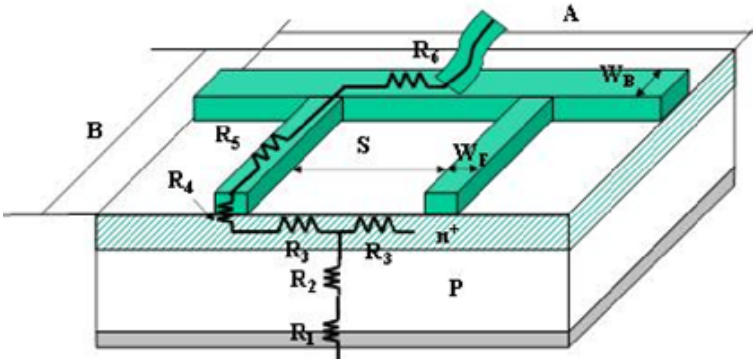



Figure 1.18: Series Resistance Components [15]

The back contact resistance is dependent on the aluminum (Al) alloys with the silicon (Si), and the architecture of the cells [14]. The bulk semiconductor resistance is the resistivity of the bulk cell material. For a typical Si solar cell, this value lies in between $0.5 - 5.0\Omega cm$ [30]. From the bulk resistivity ($\rho_b$), the base resistance can be calculated using Eq.1.8 in which, W is the width of the bulk region of the cell and A is the cell area. The base resistance ($R_b$) is the resistance the current experiences at the bulk component of the cell [30].

$$R_b = \frac{\rho_b W}{A} \tag{1.8}$$

The emitter resistance depends on two different variables. It takes the gridline spacing into account as well as the emitter sheet resistance. The shorter the distance

between the gridlines, the shorter the travel distance for carriers [14]. For a low emitter resistance and to reduce the power loss from the emitter, a shorter distance between gridline spacing is desirable. The emitter sheet resistance depends on both the resistivity and the thickness of the top surface n-type layer. For a uniformly doped n-type layer, the sheet resistivity can be calculated by using Eq. 1.9, in which $\rho$ is the resistivity of the material, $t$ is the thickness of the layer, and $\rho_{square}$ is the sheet resistivity measured in ohms/square [31]. Equation 1.10 can be used to calculate the sheet resistivity for a non-uniformly doped n-type layer.

$$\rho_{square} = \frac{\rho}{t} \tag{1.9}$$

$$\rho_{square} = \frac{1}{\int_0^t \frac{1}{\rho(x)} dx} \tag{1.10}$$

Contact resistance happens at the contact point between the silicon solar cell and the metal contact. Its resistance depends on the composition of the metal paste for the top contact design. One way to minimize contact resistance is to dope underneath the metal contact heavier than its surrounding area. In Section 1.4.2, contact resistance will be discussed in more detail.

Grid line resistance is dependent upon the bulk metal conductivity [14]. The usage of silver (Ag) in the gridline geometry, the layout of metal fingers and busbars, of the solar cell determines the amount of gridline resistance that exists. Bus bar resistance is similar to the gridline resistance. It also depends on the bulk metal conductivity, generally Ag, and the layout of the metal grid pattern. The layout and design of the metal fingers matter, as it affects the finger resistance. The average design of a metal finger mimics the drawing in Fig. 1.19.

An easy way to decrease resistance is to design tapered fingers rather than rectangular fingers. However, due to technological limits in the industry, this may not

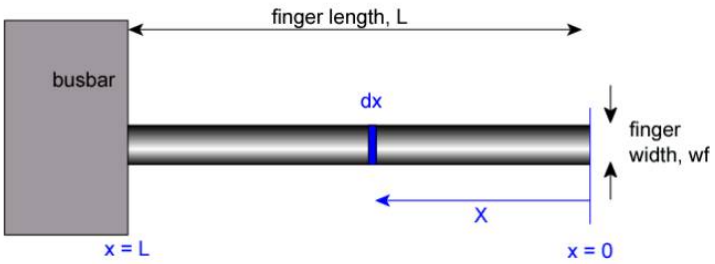



Figure 1.19: Uniform Metal Finger Design [16]

always be the most cost-efficient solution. In Chapter 2, different top contact designs are simulated to show the difference tapered fingers have on a completed solar cell.

### 1.4.2 Contact Resistance

Contact resistance occurs at the metal-semiconductor barrier. Contact related parameters are $R_S$, $R_{SH}$, ideality factor ($n$) and reverse saturation current density ($J_{02}$) [14]. A high contact resistance can prevent the flow of electrons in solar cells. A low contact resistance will allow for the electrons to directly tunnel through the potential barrier, creating an ohmic contact [14]. There are three different conduction mechanisms for metal to semiconductor contacts: thermionic emission, thermionic-field emission, and field emission. Thermionic emission has a high series resistance and a low fill factor. Thermionic means the electrons are stimulated by heat and jump over the p-n junction barrier. It is composed of low doping, $N_D < 10e17cm^{-3}$, causing the electrons to emit over the contact barrier and resulting in a schottky IV curve [14]. A schottky contact is what results in high resistance. The thermionic-field emission has medium series resistance and fill factor. It is composed of medium doping, $10e17cm^{-3} < N_D < 10e19cm^{-3}$, causing the electrons to thermally tunnel through the thin barrier in the upper end [14]. The field emission has low contact resistance and high fill factor. It is highly doped, $N_D > 10e19cm^{-3}$, creating a much thinner barrier causing direct tunneling of the electrons through the contact barrier and creating an ohmic IV curve [14]. These conduction mechanisms are visually

represented in Fig. 1.20.

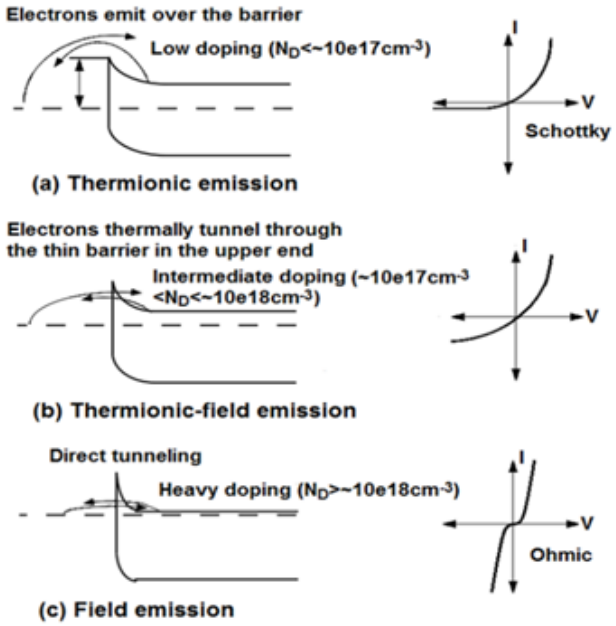



Figure 1.20: Conduction mechanism for metal-semiconductor contacts [14]

Contact resistance is measured as contact resistivity, $\rho_c$ in $\Omega - cm^2$. In Fig. 1.21, the barrier height of n-type Si and p-type Si is displayed as a function of metal work function [32]. $\Phi_B$ measured in eV is the barrier height while $\Phi_M$ displays the metal work function. The work function of a metal is the minimum amount of energy required to extract one electron from the metal [33]. The barrier height is the difference between the work function of the metal and the electron affinity of the semiconductor [14]. Therefore one should select a metal with a work function close to that of the semiconductor to reduce the barrier height between the metal-semiconductor contact, for the electrons to tunnel through the potential barrier; creating an ohmic contact [14].

For an n-type semiconductor, the work function of the metal should be similar or smaller than the electron affinity of the semiconductor, to achieve a close to ohmic contact. For a p-type semiconductor, the sum of the electron affinity and the band

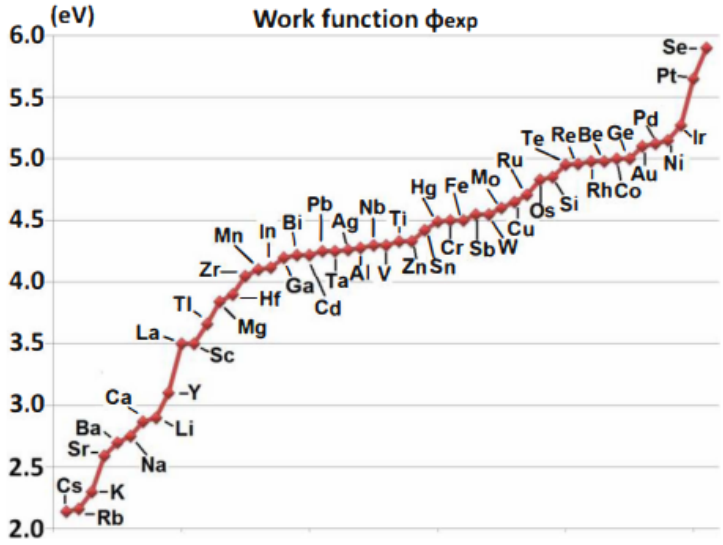



Figure 1.21: Work functions of a variety of elements [14]

gap energy of the semiconductor should be close to or larger than the work function of the metal, to achieve a close to ohmic contact [14]. Creating an ohmic contact with a p-type semiconductor with a large bandgap is relatively difficult since the metal work function is <5eV for most metals [34].

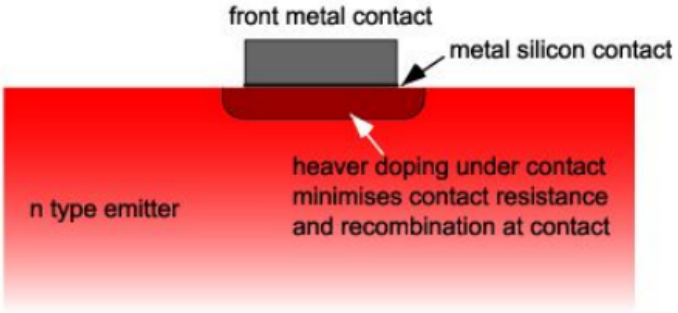



Figure 1.22: High doping of metal contact underside [17]

# CHAPTER 2: MODELING AND SIMULATIONS OF FRONT METALLIZATION DESIGNS

PC1D (Personal Computer 1 Dimensional) is a one-dimensional semiconductor program that is used to study the solar cell parameters. Since the focus of this thesis work is on the design of the gridlines and the associated series resistance, it is important to assess the impact of the series resistance on the fill factor that impacts the efficiency. Figure 2.1 shows the fill factor as a function of the series resistance. The results displayed in Fig.2.1, show that as the series resistance increases, the fill factor decreases. This correlated trend presents the fill factor as a strong function of the series resistance. In order to maintain a low resistance in a solar cell, the four components of the series resistance including the contact, gridline, busbar and emitter must decrease. By properly designing the front gridlines of a solar cell, the emitter resistance can be decreased. The contact resistance is a strong function of the glass frits in the front silver paste. While the gridline and busbar resistances depend on the Ag morphology and particle size, and solid loading in the silver paste. However, in this chapter, the 2D computer modeling (Griddler 2.5) is used to assess the impact of different front gridline designs with the initiative to minimize the overall series resistance.

## 2.1 Griddler 2.5 Modeling

To properly assess the impact of gridline design on the efficiency of a solar cell, the 2-D modeling program, Griddler 2.5 was used. Griddler 2.5 is a software developed by the Solar Energy Research Institute of Singapore (SERIS) that operates as a finite element solver that simulates solar cells. It serves as a platform to (i) design

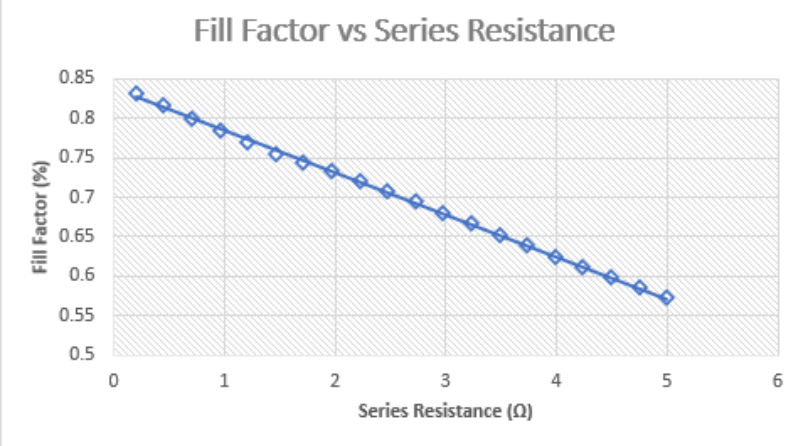



Figure 2.1: Fill Factors vs Series Resistance

solar cells, (ii) calculate their efficiencies, (iii) measure limiting factors, (iv) predict improvements through different design changes, and (v) store a database of published cell parameters from all over the world that can be utilized for personal designs. It also works seamlessly with SolarEYE, which is a luminescence imaging platform that images and analyzes lab-based cells and wafer samples. It provides the understanding needed to improve the production cells that are made in the manufacturing environment. Griddler is easy to use, practical, rigorous, and powerful. [35] It is able to solve the voltage distribution across the plane of a solar cell and then convert it into photoluminescence (PL) imaging. This is feasible by determining a calibration factor from a probed voltage at low illumination of the solar cells H-pattern. The photoluminescence images show areas of higher and lower series resistance, by corresponding higher or lower luminescence intensity. [36]

## 2.2 Design of front pattern using Griddler 2.5

Once Griddler 2.5 is opened, the handy 2D solar cell simulator, the *Design in Pattern* is chosen. The parameters needed as input into the simulation are given in Table 2.1. The style for even bus bars (EBB) is *straight*, and the style for uneven bus bars (UEBB) is *digital* with a=5mm, b=0.36mm, c=0.36mm. The parameters

for the *digital* bus bar design is demonstrated in Fig. 2.2.

Table 2.1: Solar Cell Parameters

| DESCRIPTION | PARAMETERS |
|---|---|
| Wafer Shape | pseudo-square |
| Wafer Length and Width | 15.675 cm |
| Ingot Diameter | 21 cm |
| Solder/Probe points | 15 |
| BB width | 0.72 mm |
| Number of BB | 5-10 |
| BB Style | EBB/UEBB |
| Number of Fingers | 89 |
| Finger width | varied from 10-40 um |

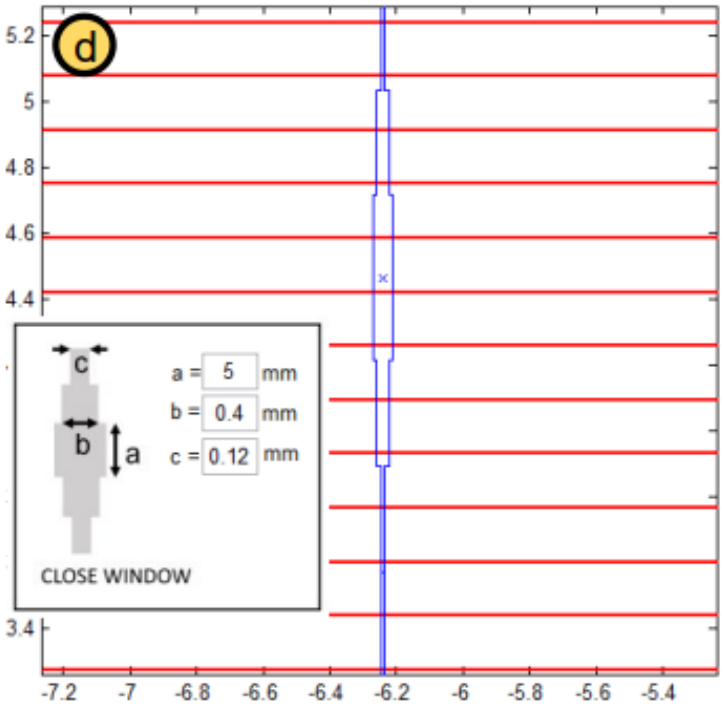



Figure 2.2: UEBB - Digital Design Parameters

Once the parameters in Table 2.1 are supplied to Griddler, it generates the cell shown in Figure 2.3. Next, the front grid mesh is analyzed and kept as a medium (Figure 2.4-A). The rear grid is also meshed and kept at medium (Figure 2.4-B).

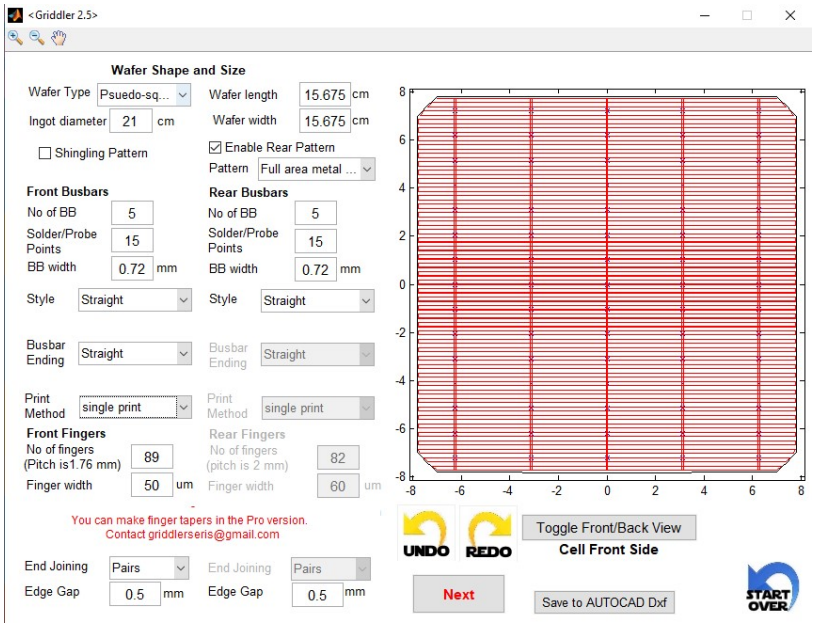



Figure 2.3: Wafer Shape and Size Parameters

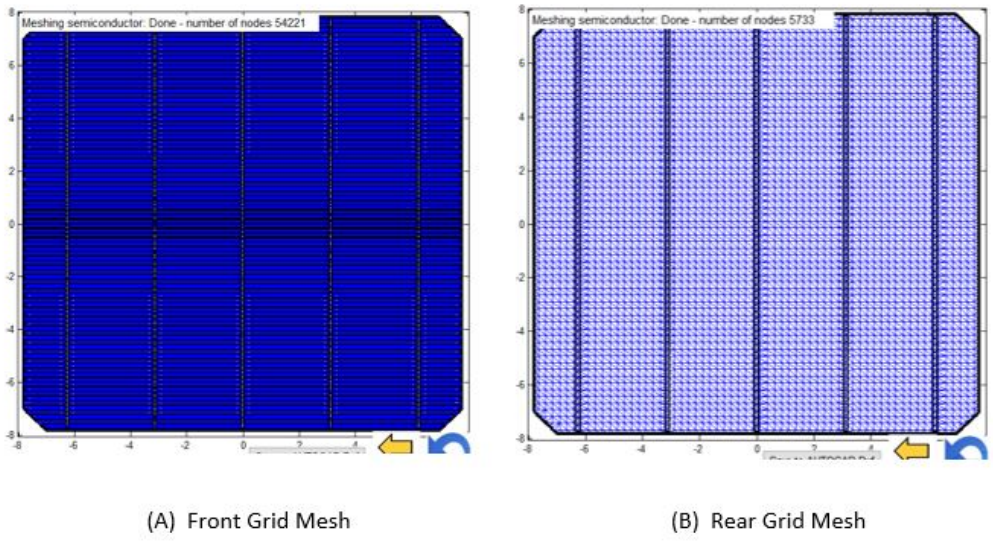



Figure 2.4: (A) Front grid mesh (B) Rear grid mesh

After the front and the back mesh have been created, the parameters that can be altered are displayed as shown in Fig. 2.5. Once the solar cell design is complete (front and rear meshes are created and satisfactory), the short circuit current, the open-circuit voltage, the maximum PowerPoint, and the JV sweep can be simulated.

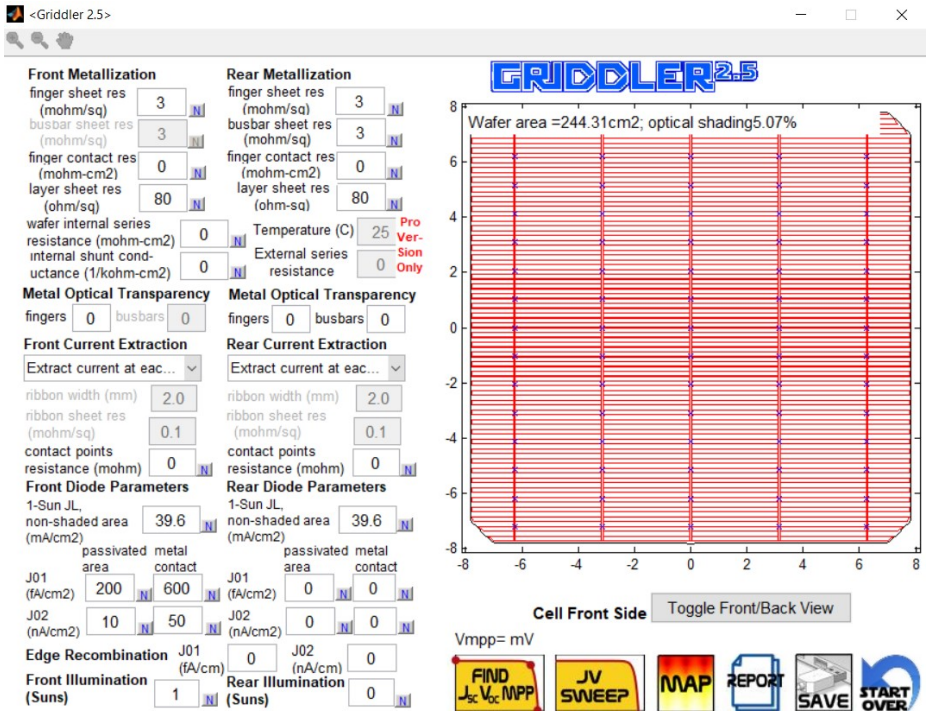



Figure 2.5: Metallization Parameters

In this work, four different designs were evaluated: (i) even bus bars (EBB), (ii) uneven bus bars (UEBB), (iii) tapered fingers (TPF) and (iv) non-tapered fingers (NTPF). Each of these designs, in addition to varying finger width, was simulated with the bus bars varying from 5-10. The combinations can be summarized as

- NTPF/EBB (conventional design)
- NTPF/UEBB (not common)
- TPF/EBB (unique to this work)
- TPF/UEBB (unique to this work)

The output parameters investigated were (i) efficiency, (ii) open-circuit voltage, (iii) short circuit current, and (iv) fill factor.

# CHAPTER 3: SIMULATION RESULTS AND DISCUSSION

A total of 133 different designs were simulated. The designs focused mainly on the number of bus bars, EBB/UEBB, the width of the metal fingers, and NTPF/TPF. Figure 3.1 shows a comparison of EBB and UEBB. In the UEBB design, the wider section is referred to as the major part and the smaller section as the minor part, respectively. To compare these design features with each other, one variable was modified at a time and for each design a simulation was run to determine its potential $V_{OC}$, $J_{SC}$, Fill Factor (FF), and efficiency.

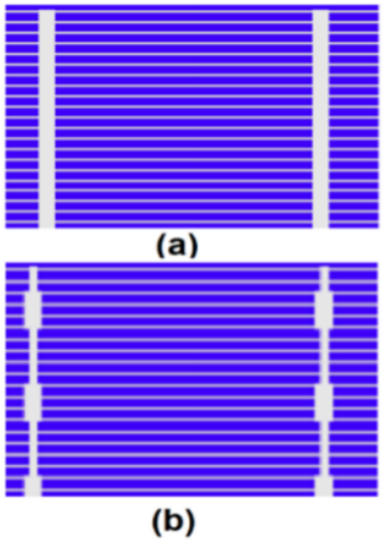



Figure 3.1: a) EBB Design b) UEB design

Metallization has an optical and electrical impact on a solar cells operation. The $J_{SC}$ is affected by the shading that is created by the width of the gridline, and the FF is affected by the series resistance due to contact and grid line resistances [14]. The emitter, gridline, and busbar resistances dominate the impact on series resistance. There are three main design changes to the front grid pattern that can decrease series

resistance. These are increasing the number of gridlines, decreasing contact resistance, and increasing the number of busbars. While increasing the number of gridlines and busbars, the total metal coverage is critical to avoid shading loss and reduction in $J_{SC}$. Thus, as the number of gridlines increases, the geometry is decreased to finer lines and the bus bars coverage stays constant as the number increases.

Griddler was used to find the best combination of the front grid design, for a screen printable fire through dielectric solar cells, that would give the best electrical output parameters. These front gridline designs are universal for all screen printable pastes.

## 3.1 Impact of gridline width on electrical output parameters with 5BB

Since the state-of-the-art number of busbars is 5 for the industrial solar cells, the modeling started with 5 and went up to 10. Figure 3.2 shows the electrical output data for a 5EBB and 5UEBB as a function of NTPF width. While Fig. 3.3 shows the 5EBB and 5UEBB as a function of TPF gridline width. The NTPF width varied from 10um to 40um, while all other variables were kept constant. The major part of the bus bar measured 0.72mm and the minor part 0.36mm. Figure 3.2 shows the most efficient cell at 20.50% with a combination of 20um gridline width and UEBB. Figure 3.3 shows a slight edge in efficiency over the NTPF/UEBB when the TPF width range of 30-10um in conjunction with the UEBB is used.

The corresponding FF and $J_{SC}$ are shown in Fig. 3.4 and 3.5, and Fig. 3.6 and 3.7, respectively. As expected, the FF decreases as the gridline width decreases irrespective of the combination (EBB/NTPF, UEBB/NTPF, EBB/TPF, UEBB/NTPF), On the other hand, the $J_{SC}$ increases as the gridline decreases in width for all the combinations. This is due to the decrease in shading losses associated with thinner gridlines low metal coverage. The FF decreases, mainly due to increased contact resistance, which cross-sectional are related. The electroluminescence for these combinations is shown in Fig. 3.8, however, it is not obvious, qualitatively which design combination

exhibits higher series resistance. The FF variation with the decreased gridline width (EBB or UEBB), seem to decrease steadily with the TPF but slightly steeper for the NTPF.

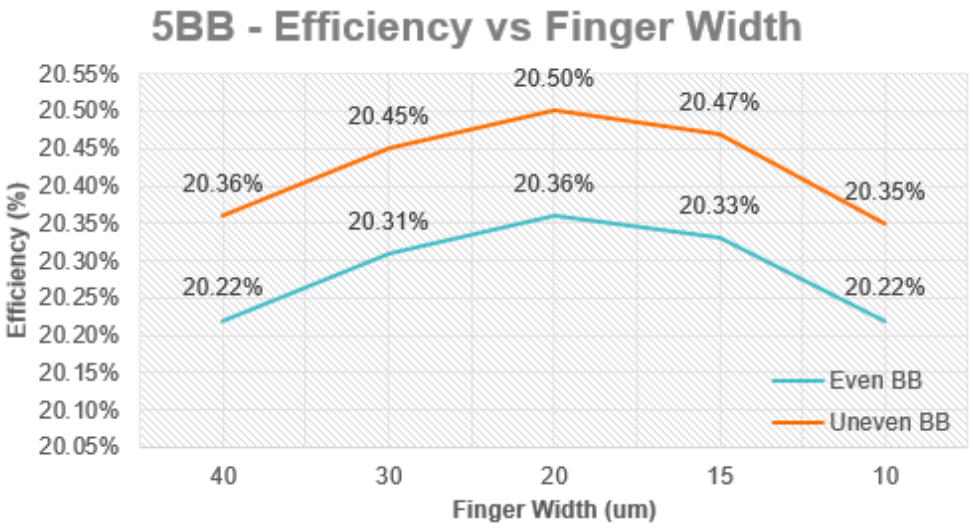



Figure 3.2: 5BB - Efficiency as a function of NTPF width with EBB and UEBB

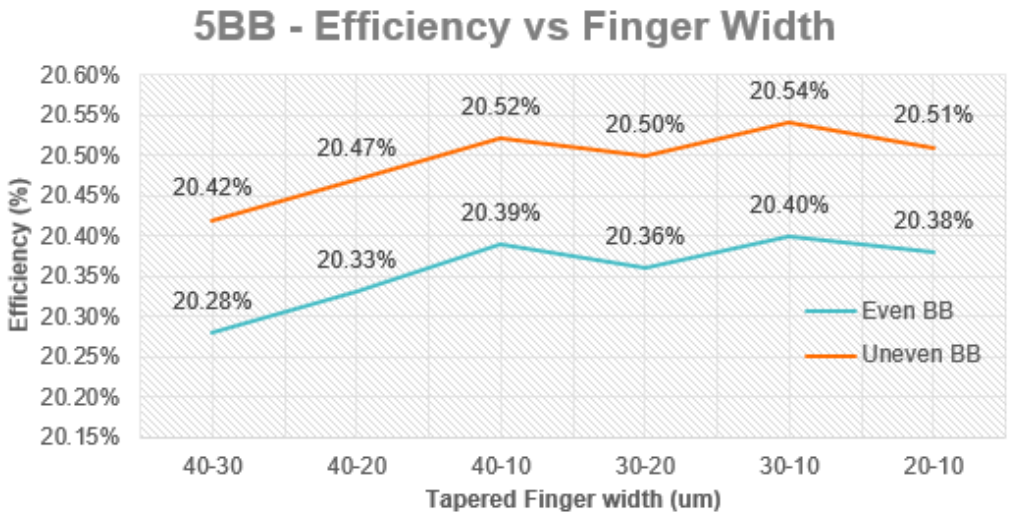



Figure 3.3: 5BB - Efficiency as a function of TPF width with EBB and UEBB.

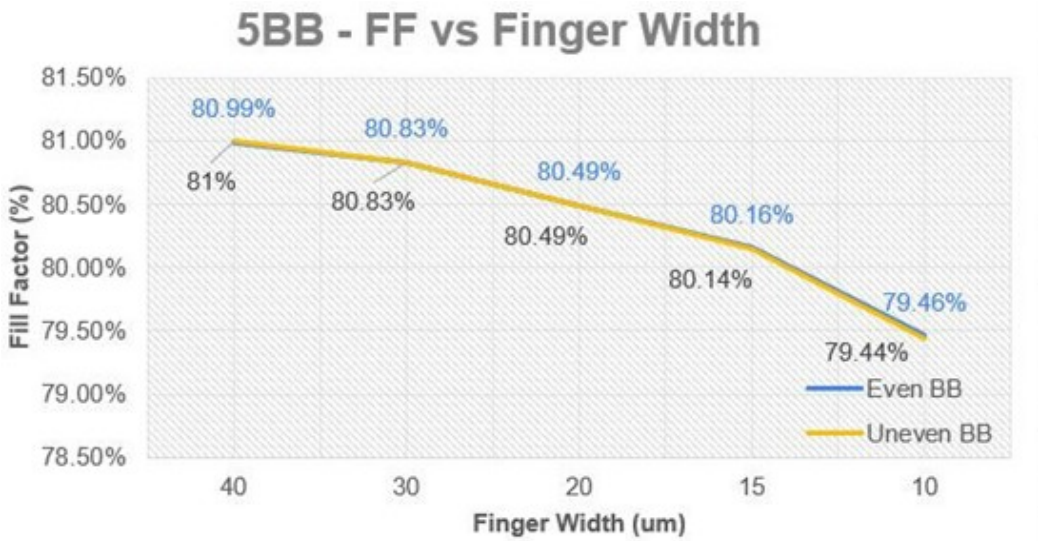



Figure 3.4: 5BB - Fill Factor as a function of NTPF width with EBB and UEBB

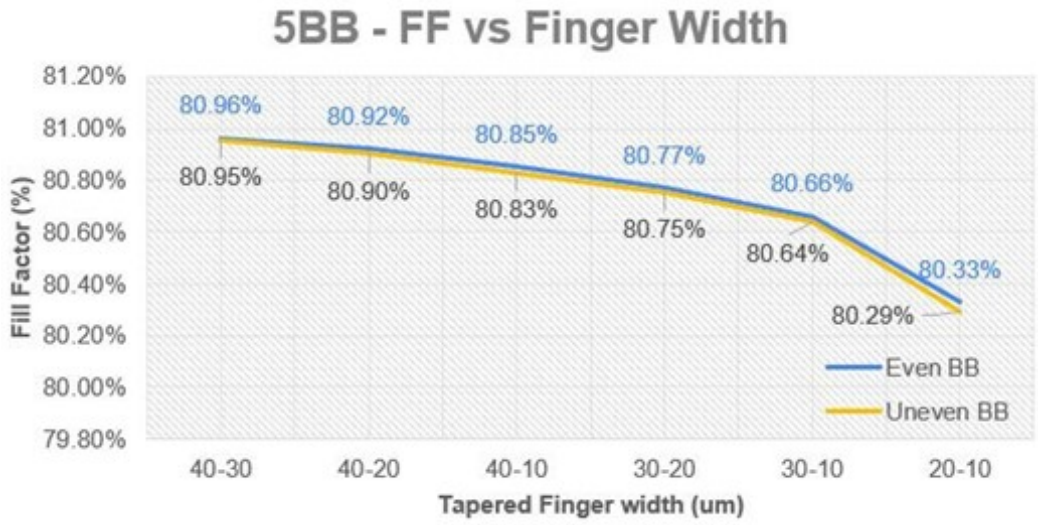



Figure 3.5: 5BB - Fill Factor as a function of TPF width with EBB and UEBB

The $J_{SC}$ for the UEBB/NTPF combination is superior by $0.23mA/cm^2$ to the NTPF/EBB. This current can be attributed to less metal coverage due to the narrow width of the minor part of the UEBB design. Also, for the TPF/UEBB, same $J_{SC}$ value was observed at 20-10um width. This means that either gridline combination can be used without loosing current.


Figure 3.6: 5BB - Short Circuit Current as a function of NTPF width with EBB and UEBB


Figure 3.7: 5BB - Short Circuit Current as a function of TPF width with EBB and UEBB

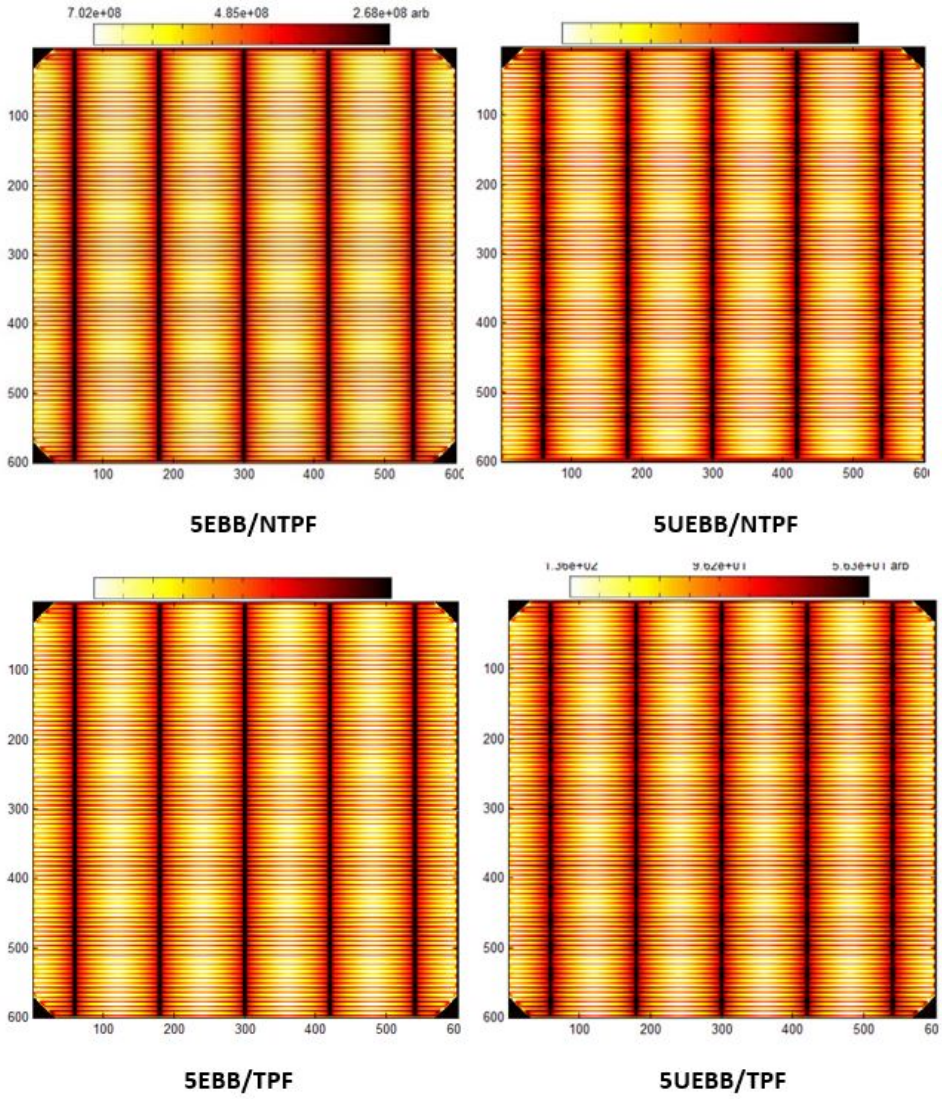



Figure 3.8: 5BB Luminescence Images

Figure 3.8 displays a map of luminescence imaging that was created to compare the four different designs of 5BB's. The lighter areas reflect lower series resistance, and the darker areas reflect high series resistance. The highest resistance is found along the BB's; the further away one gets from the BB's the lower the resistance becomes.

## 3.2 Impact of gridline width on electrical output parameters with 10BB

As the number of bus bars increases to 10, there is a marked difference in the front grid design with respect to the different combinations. For instance, Fig. 3.9 and 3.10 show a 0.38% absolute efficiency gain with the use of UEBB, irrespective of the finger design (NTPF or TPF)

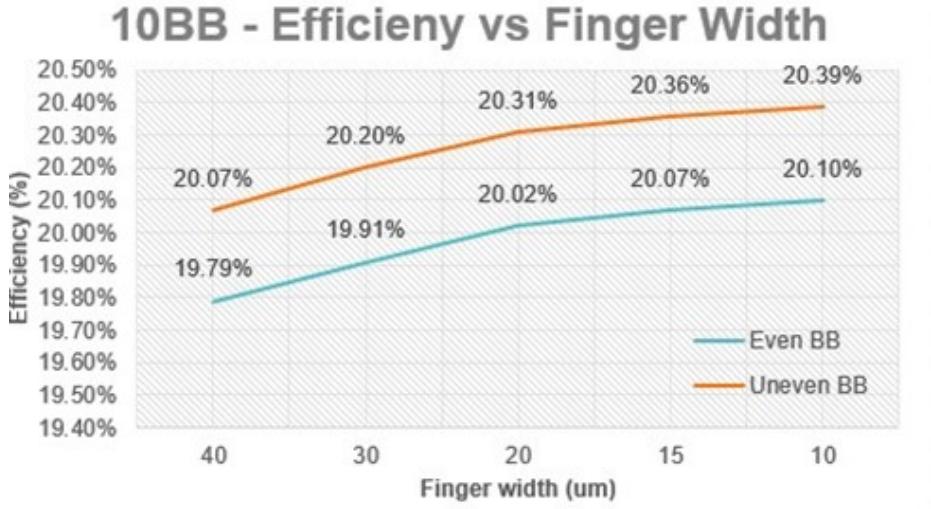



Figure 3.9: 10BB - Efficiency as a function of NTPF width with EBB and UEBB

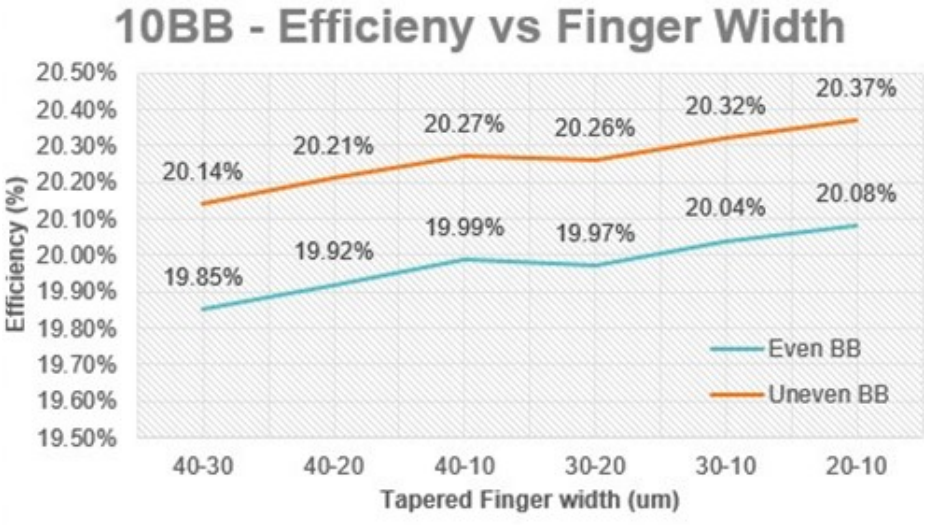



Figure 3.10: 10BB - Efficiency as a function of TPF width with EBB and UEBB

Also, the FF (Fig. 3.11 and 3.12) for NTPF and TPF with respect to EBB and UEBB are similar and no preference. This is due to reduction in the gridline resistance as the current path length is decreased with more busbars. The major difference is in the $J_{SC}$ (Fig. 3.13 and 3.14) gain as a result of the reduced shading with the UEBB due to the minor width being smaller. Thus, the superior efficiency seen in the design can be attributed to the gain in $J_{SC}$ when combining the UEBB with TPF.

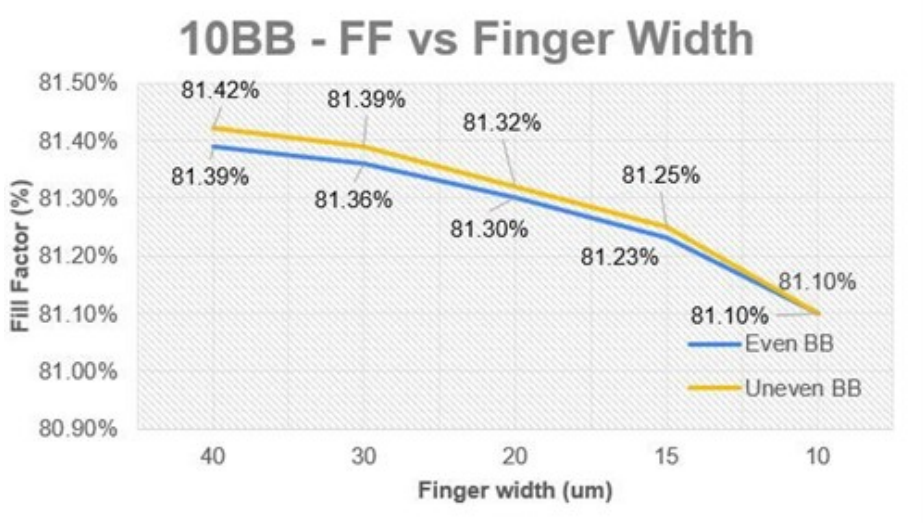



Figure 3.11: 10BB - Fill Factor as a function of NTPF width with EBB and UEBB

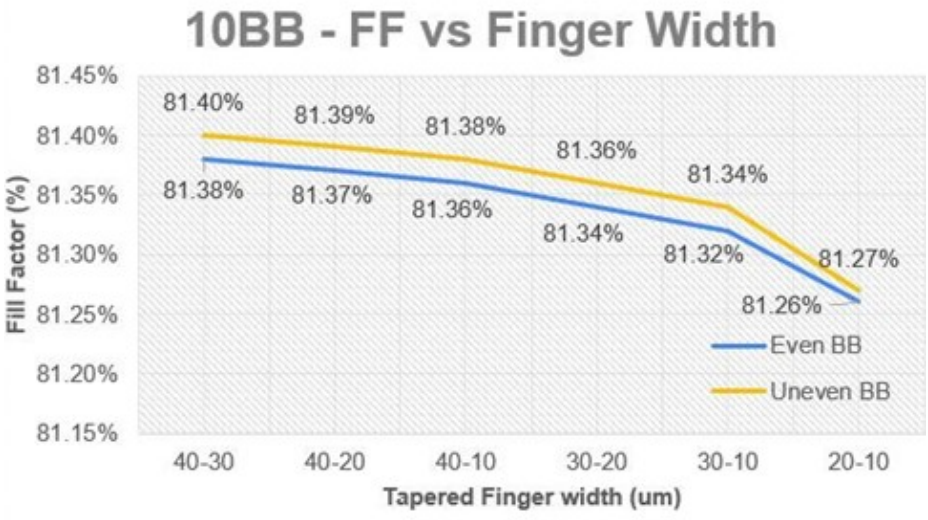



Figure 3.12: 10BB - Fill Factor as a function of TPF width with EBB and UEBB

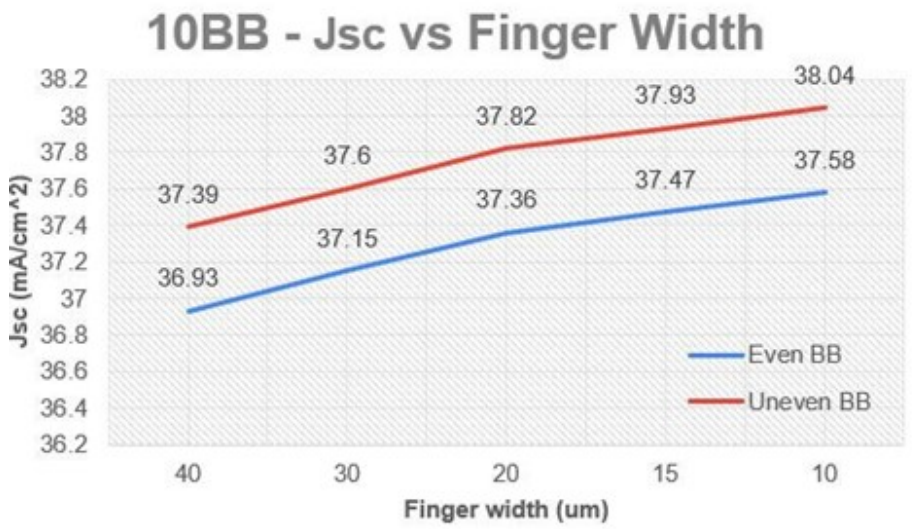



Figure 3.13: 10BB - Short Circuit Current as a function of NTPF width with EBB and UEBB

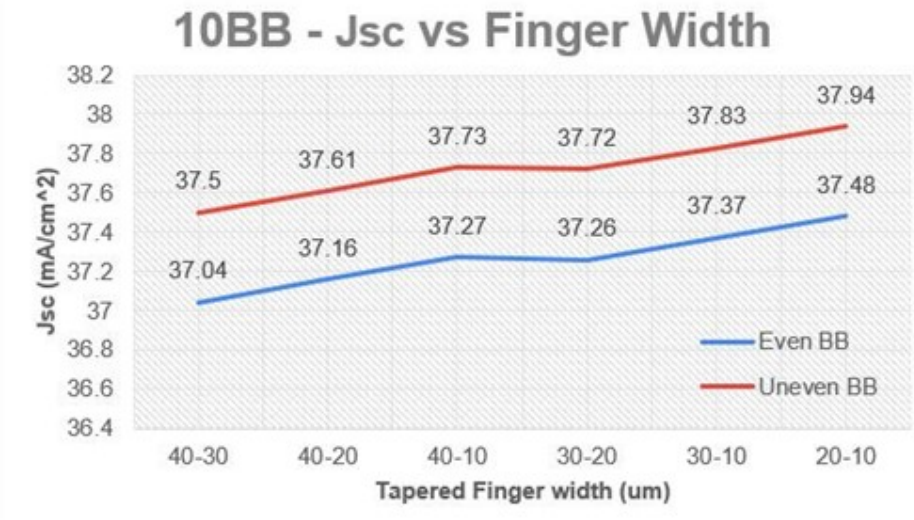



Figure 3.14: 10BB - Short Circuit Current as a function of TPF width with EBB and UEBB

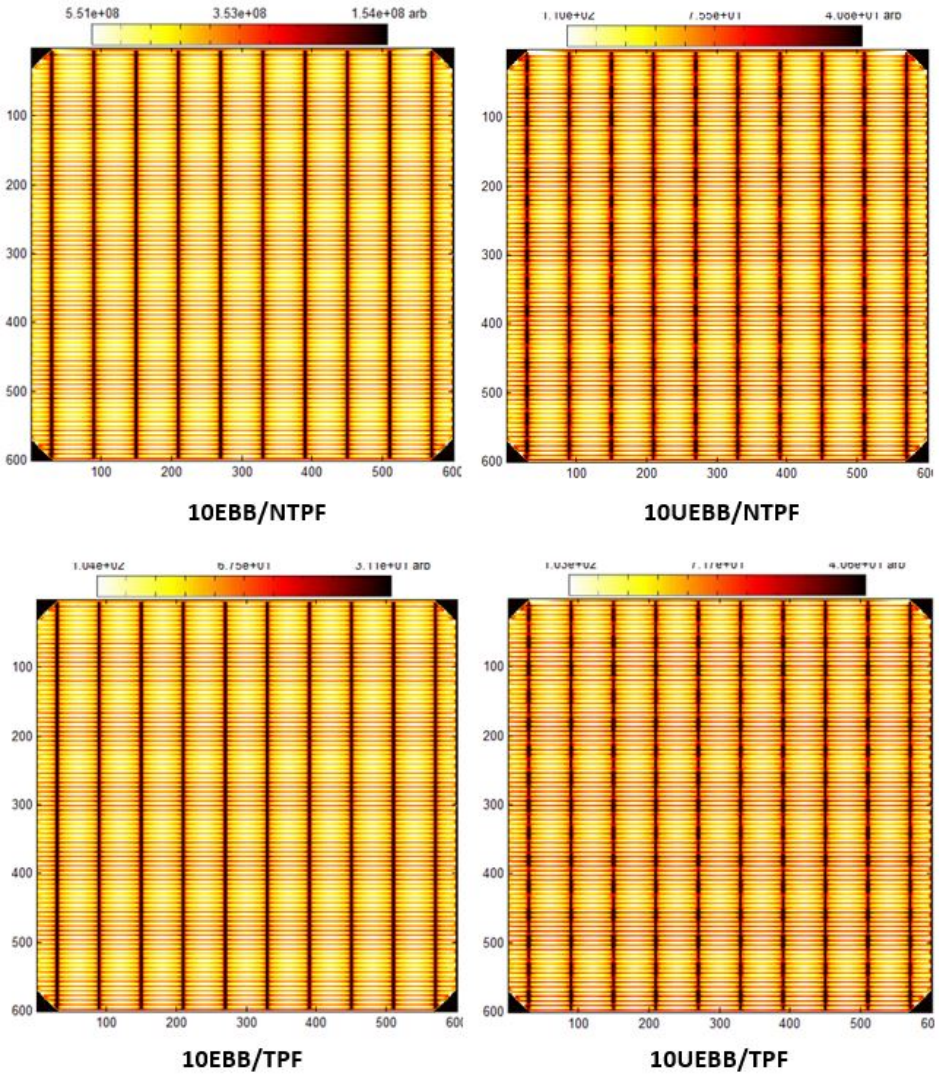



Figure 3.15: 10BB Luminescence Images

Figure 3.15 displays the map of luminescence images created to compare the 10BB designs. The 10BB designs are spread evenly across the same size solar cell that the 5BB designs were on, dramatically cutting back the lateral distance the current has to flow. This helped decrease the series resistance, as these luminescence images display a much lighter solar cell overall.

## 3.3 Electrical output parameters for 5-10BB

This section expands upon the results that were previously only discussed for the 5BB and 10BB design. The finger width is compared to efficiency, FF, and $J_{SC}$ for all variations from 5-10BB designs in one graph. The initial assumption in designing the solar cells was that the more bus bars the design has, the higher the efficiency it would give because of the reduced overall series resistance as the current path length is decreased. This initial assumption proofed to be wrong by the following data.

### 3.3.1 EBB/NTPF

The data shows that although the FF improves with the addition of bus bars, the efficiency is slightly inferior by 0.12% absolute for the NTPF and EBB. However, in between for the 6 and 7BB, the trend follows the prediction after NTPF width of 15 um and 10 um respectively for the 6BB and 7BB as depicted in Fig. 3.16. FF on the other hand followed the trend of increased number of bus bars with the 10BB topping the list as shown in Fig. 3.17. $J_{SC}$ clearly shows the opposite of the prediction, for the EBB and NTPF design as shown in Fig. 3.18.

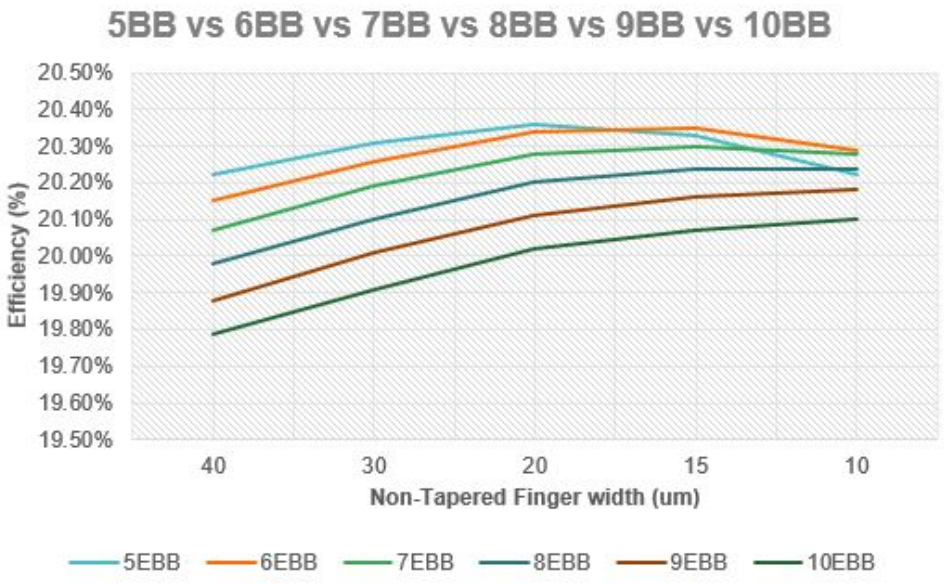



Figure 3.16: 5-10BB - Efficiency as a function of the NTPF width with EBB

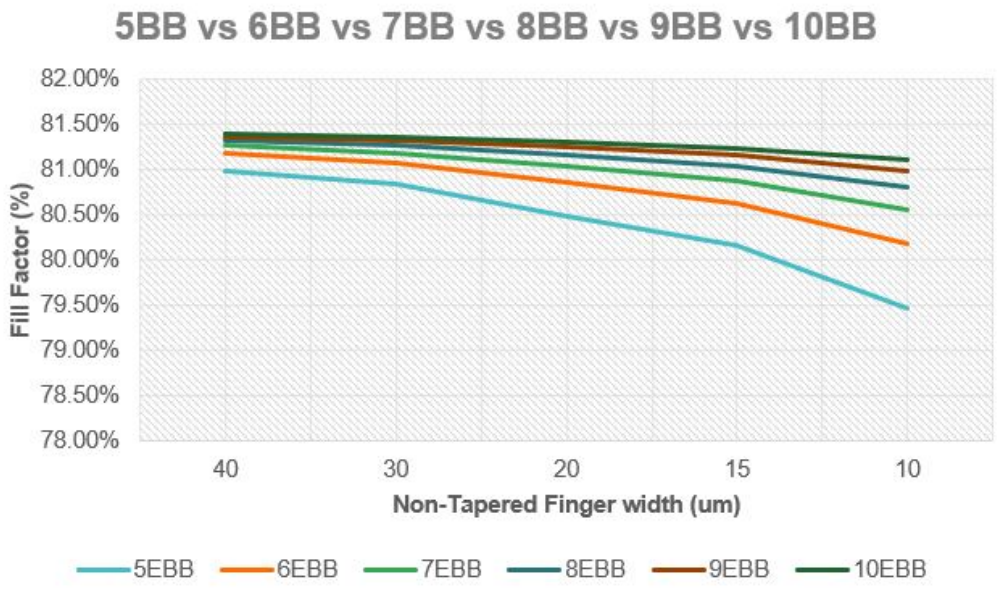



Figure 3.17: 5-10BB - Fill Factor as a function of the NTPF width with EBB

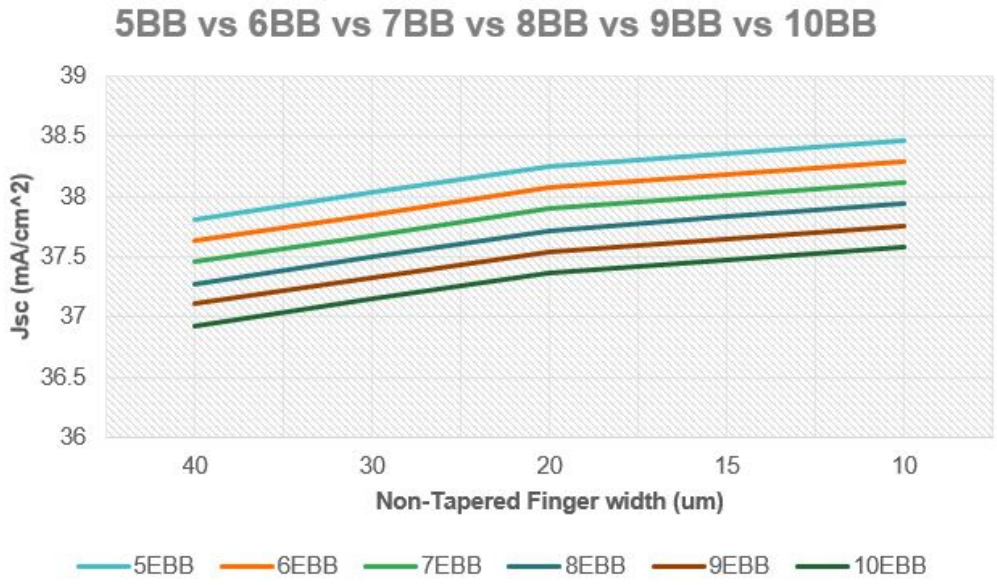



Figure 3.18: 5-10BB - Short Circuit Current as a function of the NTPF width with EBB

### 3.3.2 UEBB/NTPF

Figure 3.19 compared efficiencies of the UEBB/NTPF design for the 5-10BB. It confirms that the 5BB design has a higher efficiency than the designs with more bus bars with the NTPF width from 40-20 um range and then drops after that. This drop in efficiency after the 20um width is evident in the decrease FF as depicted in Fig. 3.20. However, $J_{SC}$ (Fig. 3.21) is best for the 5BB, which is why the FF decreases as high current exacerbates increase series resistance.

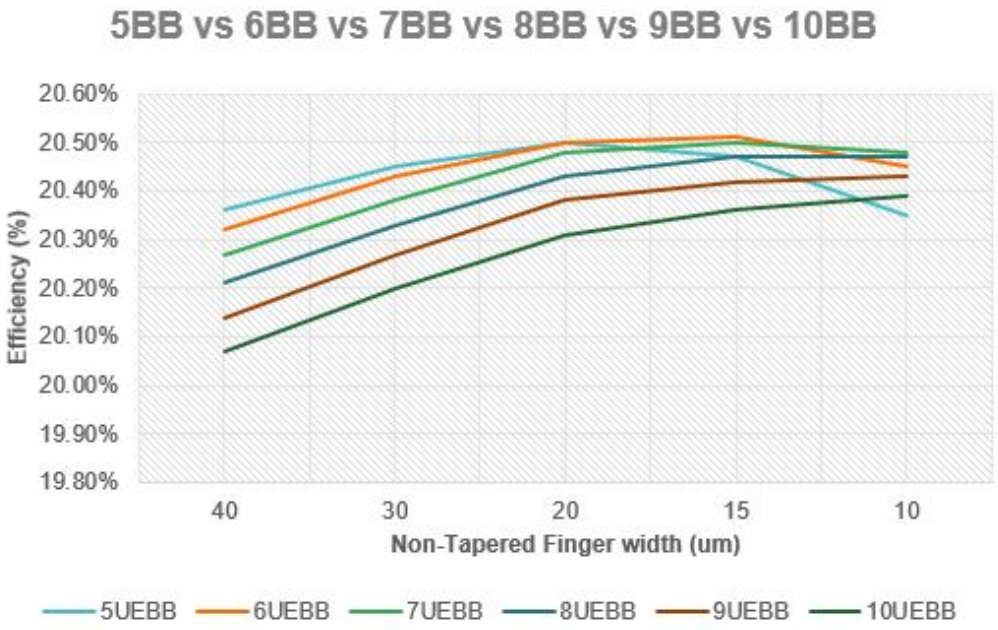



Figure 3.19: 5-10BB - Efficiency as a function of the NTPF width with UEBB

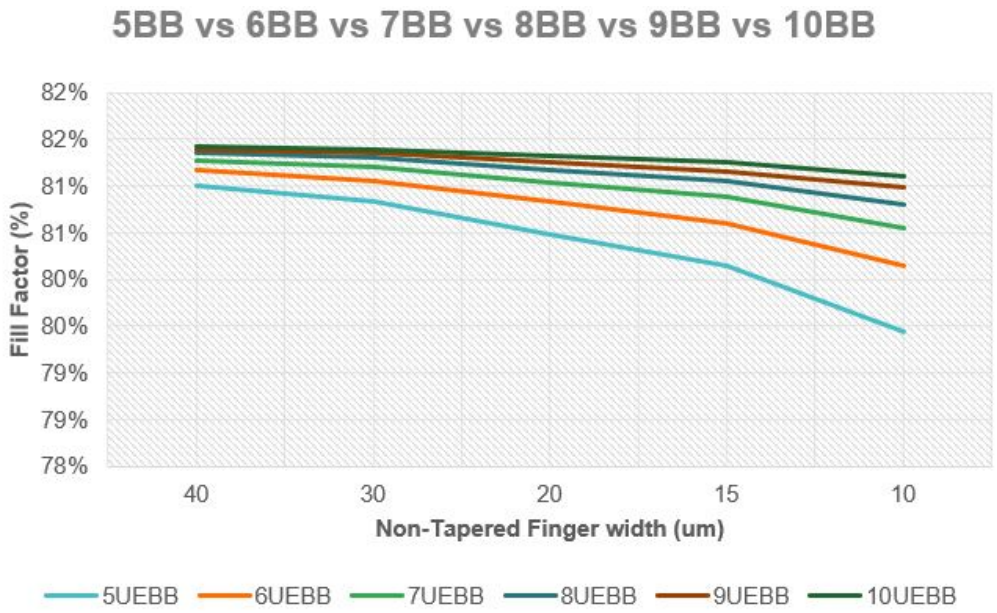



Figure 3.20: 5-10BB - Fill Factor as a function of the NTPF width with UEBB

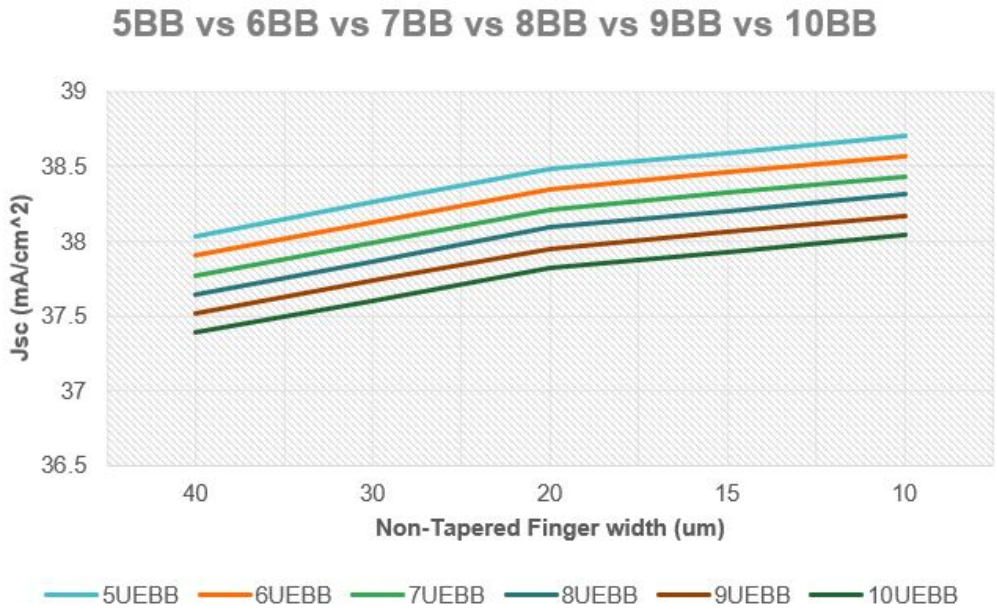



Figure 3.21: 5-10BB - Short Circuit Current as a function of the NTPF width with UEBB

### 3.3.3 EBB/TPF

Fig. 3.22 compares efficiencies of the UEBB/TPF design for the 5-10BB. It shows that the 5BB design has a higher efficiency than the designs with more bus bars with the TPF. This efficiency superiority is dominated by $J_{SC}$ (Fig. 3.24) which is maintained through the range of the TPF width range. The FF as depicted in Fig. 3.23 shows inferior FF as a function of the width range. However, FF follows the prediction.

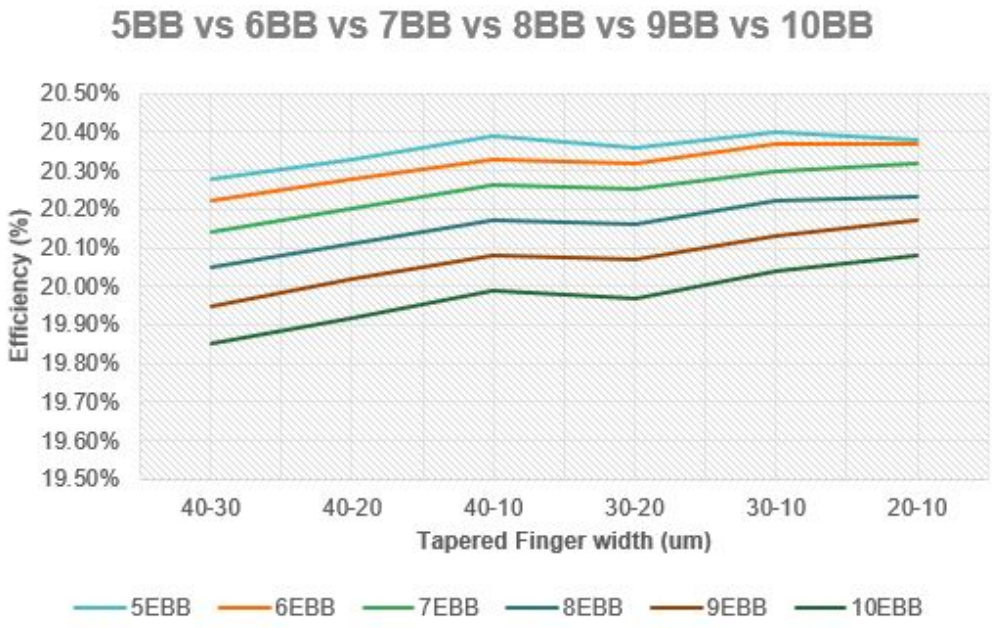



Figure 3.22: 5-10BB - Efficiency as a function of the TPF width with EBB

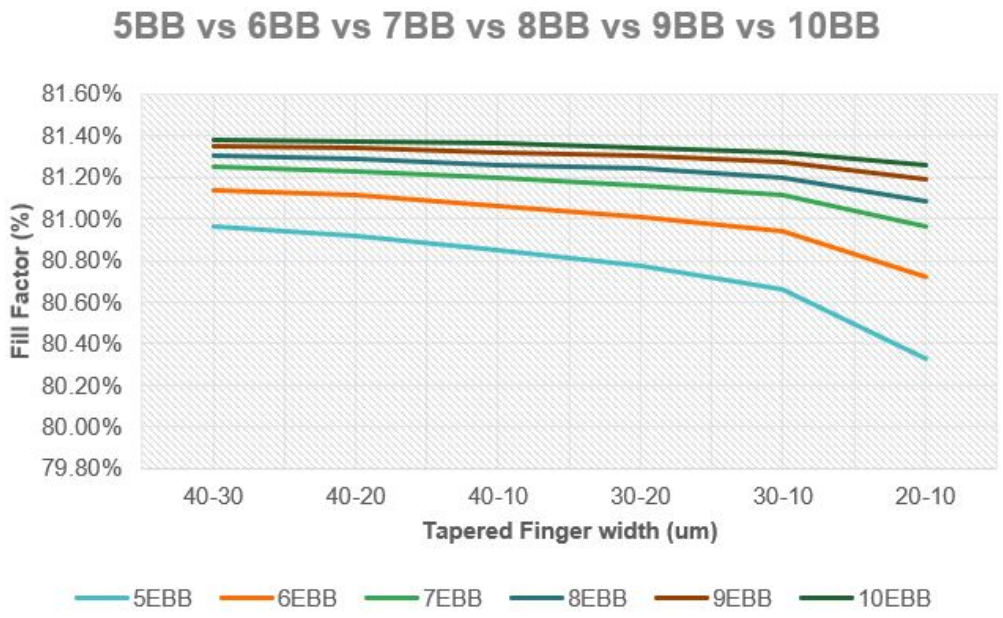



Figure 3.23: 5-10BB - Fill Factor as a function of the TPF width with EBB

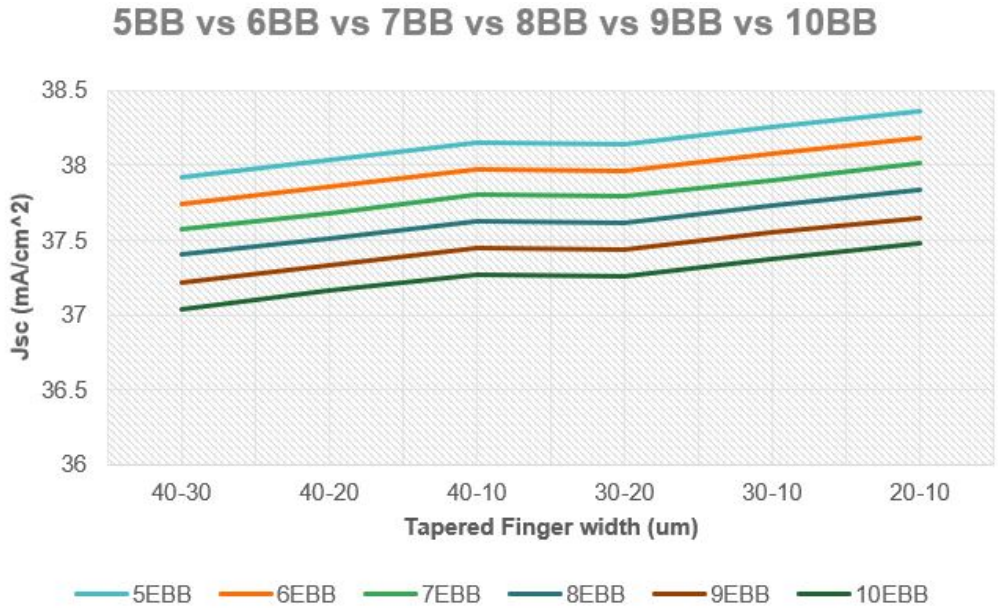



Figure 3.24: 5-10BB - Short Circuit Current as a function of the TPF width with EBB

### 3.3.4 UEBB/TPF

Figure 3.25 compares efficiencies the UEBB/TPF design for the 5-10BB. It confirms that the 5BB design has a higher efficiency than the designs with more bus bars with the TPF width range of 30-10 um and then drops after that. This drop in efficiency after the 30-10um width range is evident in the decrease FF as depicted in Fig. 3.26. However, $J_{SC}$ (Fig. 3.27) is best for the 5BB, which is why the FF decreases as high current exacerbates increase series resistance.

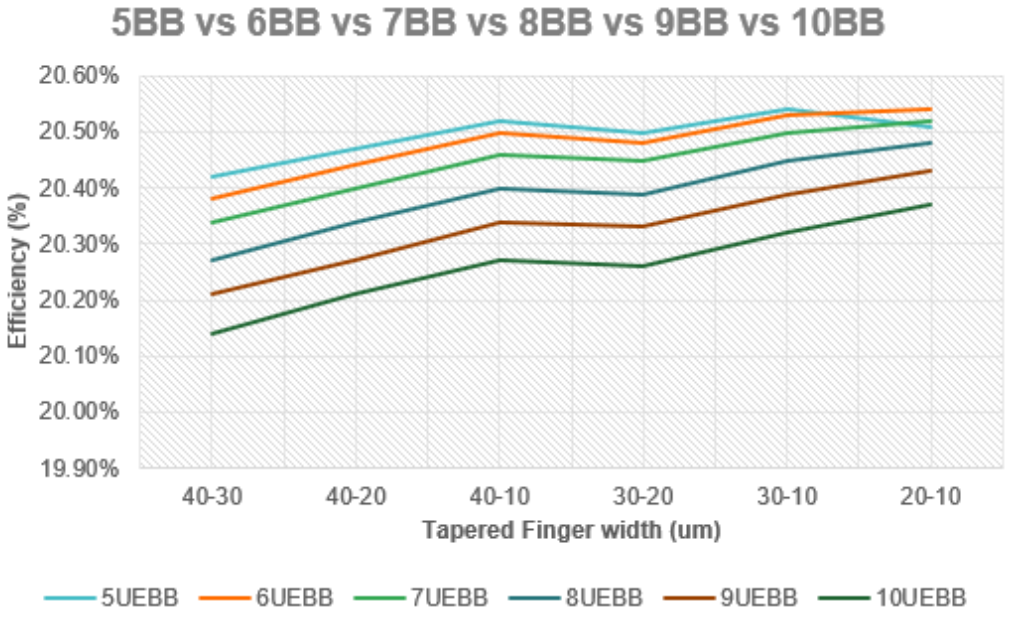



Figure 3.25: 5-10BB - Efficiency as a function of the TPF width with UEBB

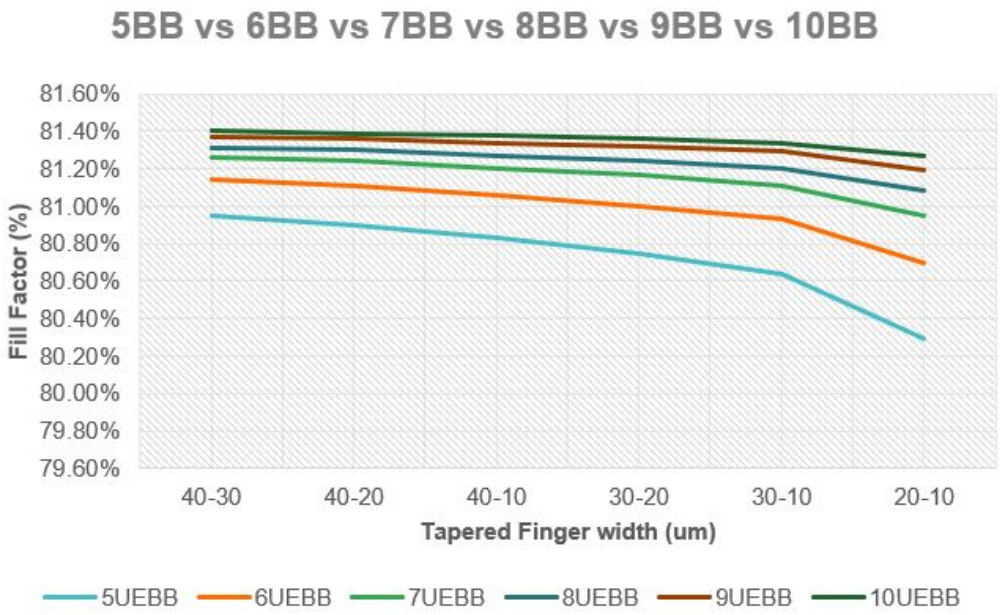



Figure 3.26: 5-10BB - Fill Factor as a function of the TPF width with UEBB

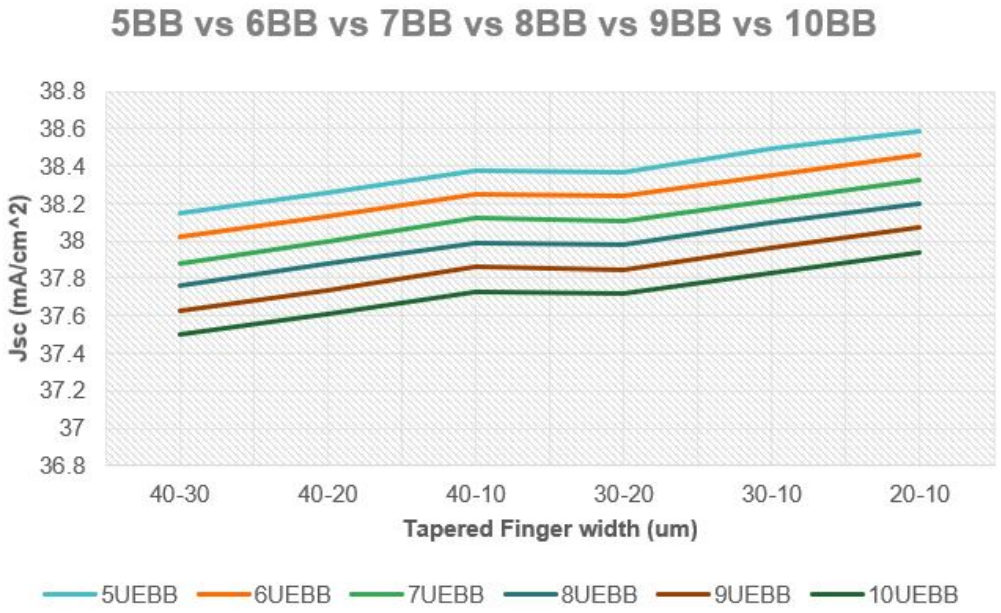



Figure 3.27: 5-10BB - Short Circuit Current as a function of the TPF width with UEBB

# CHAPTER 4: COPPER FRONT METALLIZATION OF SOLAR CELLS

In this chapter, the replacement of a silver paste with a copper paste is analysed. To create improvements in the solar cell industry, one has to either increase the efficiency of solar cells or lower the production cost of solar cells.

## 4.1 Experimental Data of Screen-printing Atmospheric Copper paste

When taking costs into consideration of the fabrication of solar cells, the front grids metallization usage of Ag is the second most expensive part of the solar cell, right after the cost of the Si wafer [37]. The screen-printable silver paste is composed of glass frits, metal powder and organic binder and during high temperature sintering, Ag's reaction forms reliable contacts with the cell through the dielectric. Due to the extensive research that has been done on silver, it is the solar cell industry's choice of metal [18]. Since the cost of silver is relatively high, there is a focus on reducing the amount of silver used in solar cells. A few ways to reduce the amount of silver per wafer are to make design changes to the front grid design of the solar cell. These changes include: (i) decreasing the bus bar width to approximately 0.72mm through even and uneven structures, (ii) switching to tapered fingers of sizes 60um-30um, from the bus bar to the center, (iii) decreasing the number of gridlines, (iv) and the addition of streets to the design [38]. Even though these design changes decrease the amount of silver used, the amount is minuscule and therefore does not largely reduce the cost since the price of silver changes daily. Consequently, a substitute for silver is needed. The goal is to find a replacement, meaning no additional cost of equipment or change in process. The element closest to silver is copper, the conductivity of copper ($1.6\mu\Omega$-cm) is slightly shy of silver's ($1.7\mu\Omega$-cm), but the cost of copper is 50 times

cheaper than the cost of silver [20].

The same fabrication systems that have been used for Ag metallization are also being used to develop front Cu metallization. There have been suggested applications of plating, thick films and alloys, with the inclination to move towards screen printing with pure Cu paste metallization. Moving towards screen-printing Solar Cells with an atmospheric Cu paste would be ideal. Being able to simply exchange the current Ag paste with the Cu paste, would not only save money in material cost, but would also save money in the manufacturing standpoint. Since a simple replacement of pastes does not require any changes to the process of manufacturing solar cells, nor does it require any new equipment, the change is easy to implement.

Preliminary success of utilizing copper for front metallization was achieved in the study *Rapid Thermal Annealing of Screen-printable Atmospheric Cu pastes for PERC Solar Cell* [18]. This study took advantage of fast belt speed and reducing the cost of the second most expensive part of the solar cell, the silver metallization, by using copper. The copper paste utilized in this study was similar to the mixture of the silver paste, without the silver powder. The main challenges to overcome with using copper are its (i) rapid diffusion into the silicon bulk at high temperatures sintering, (ii) oxidation in atmospheric ambient, and (iii) solar cell degradation due to the possible penetration of the pn junction by copper precipitates. These preliminary results overcame all of these obstacles.

Rapid thermal annealing is the conventional approach for making screen printable contact for silicon solar cells. At room temperature the sintering of the metal pastes begin, it then gets ramped up into higher temperatures causing the glass frits in the metal paste to melt and etch through the anti-reflective coating to make contact with the emitter of the solar cell [39]. The focus on rapid thermal annealing in this study was to utilize a faster belt speed than what is common in the industry right now. This process in the industry is limited to 180-200 inches per minute (IPM), hence there is

room to grow. The study shows that the faster the belt speeds, the more uniform and deeper the back surface field. Uniformity and depth make a difference in the open circuit voltage of the solar cell, because the back surface recombination velocity is reduced, therefore Voc is high. Figure 4.1 displays the furnace profiles, showing that the faster the belt speed, the shorter the dwell time. Dwell time is the amount of time the solar cell stays at the peak temperature. The end goal was to have the same single peak temperature for different belt speed. The peak temperatures, dependent on the belt speed, for this experiment were 590°C for 300 IPM, 588°C for 325 IPM, and 584°C for 350 IPM. Due to unreliability of the thermocouple maintaining constant contact on the test wafer, the temperatures vary slightly.

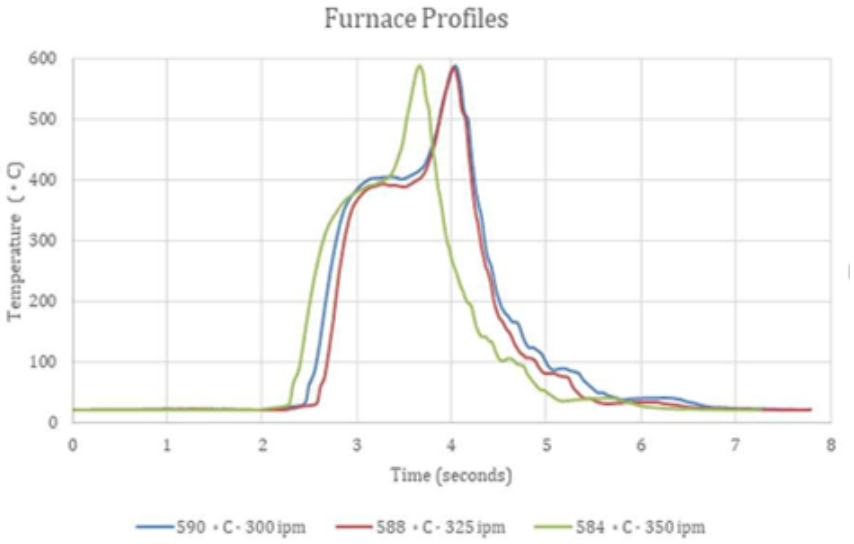



Figure 4.1: Furnace Profiles [18]

Copper functions not only with lower temperatures but also with shorter annealing times. Copper favors lower temperatures, so when it is alloyed with other materials its melting point will decrease, therefore having a lower peak time will not give copper the chance to diffuse. Having a faster belt speed will also lead to a faster ramp down. A fast ramp down reduces the chances of fast oxide growth below the metal contact, preventing the formation of excessive oxide.

The experimental method compared the process sequence of silver and copper pastes. This process is laid out in Fig. 4.2, one can observe that the process of developing these solar cells is identical, besides the exchange of using copper instead of silver. The process starts out with using the same base of the cell, in this case a blue wafer with PERC structures. Then the different pastes were applied, some used the Ag screen-printable paste, while the others used the Cu screen-printable paste. They were then dried for 2 minutes at 200°C and then went through a high temperature anneal to ensure peak temperature after profiling. Afterwards Sun's VOC measurements of the solar cells were taken. These measurements provided the following parameters: n-factor, $J_{02}$, shunt resistance and pseudo efficiency. The final step was taking electroluminescent images to evaluate the series resistance throughout the solar cells [18].

Since copper has a fast diffusion velocity, it cannot be deposited directly on top of the emitter or else it will act as a deep level impurity in the silicon bulk [40]. If copper and the silicon bulk make contact, the precipitation of copper occurs which will drastically reduce the minority carrier diffusion length due to the formation of state bands within the band gap. These state bands create recombination centers, destroying the lifetime of the cell and effectively rendering it useless [19]. When electrons jump straight from valence to conduction band without any state bands in between, then the short circuit current is high. The precipitation of copper in low concentrations constructs self interstitial centers on the perfectly structured n-type Silicon by causing intense strain to the lattice. This point defect in the lattice structure renders undesirable results. [19] [41] Due to the high diffusion velocity of copper, the cell would have to be fired without copper etching through the anti-reflection coating to avoid creating impurities in the silicon bulk. But direct contact to the silicon bulk is needed to reduce the total series resistance of the cell.

Further research showed that there is a difference of copper contamination up to a

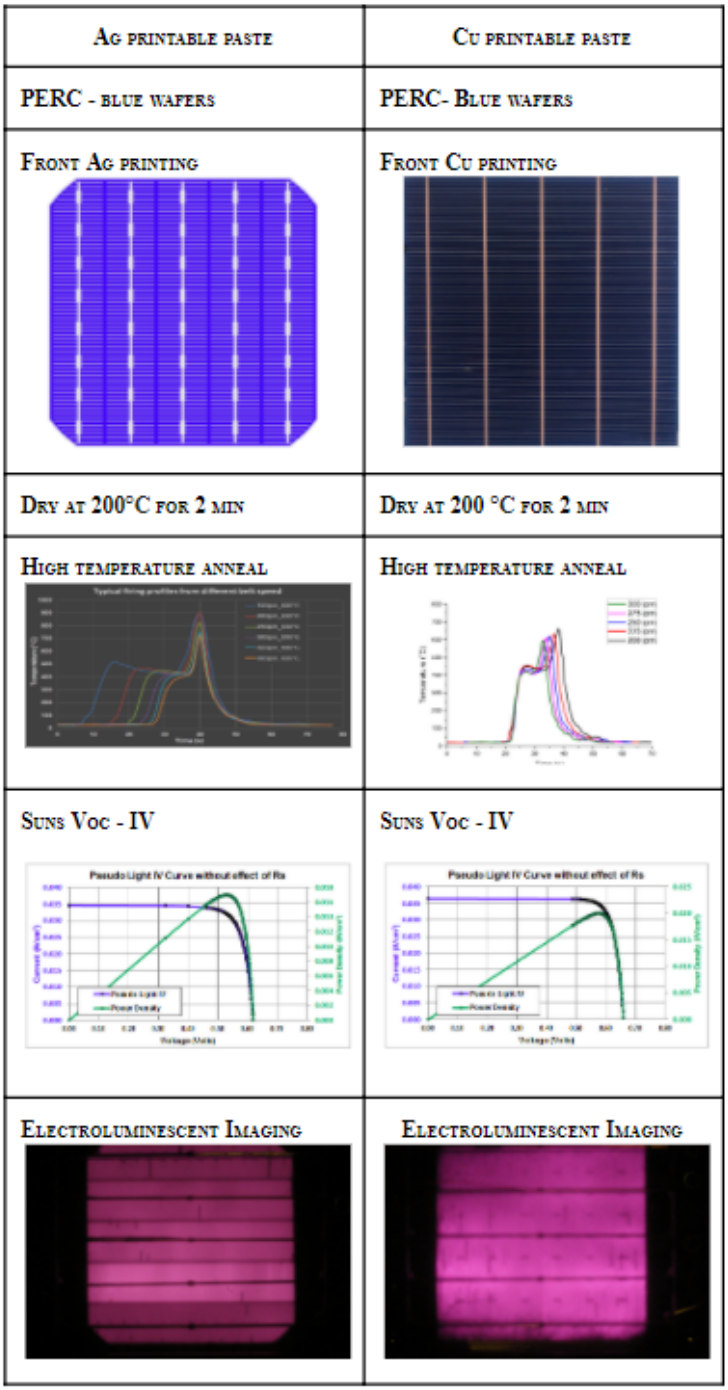



Figure 4.2: Process Sequence for Ag and Cu Pastes, respectively, screen-printed contacts PERC cells [18]

critical level between p-type and n-type Silicon [40]. In p-type Si, contamination levels up to $10^{11}$-$10^{13}$ $cm^{-3}$ had little to no effect on the minority carrier lifetime; further

results even showed an improvement in it. Higher levels of copper contamination in p-type Si leads to the degradation of the minority carrier lifetime. On the other hand, low concentrations of copper is detrimental to minority carrier lifetime on n-type Si [19]. Figure 4.3 shows that copper is able to make contact with the p-type Si bulk, in low concentrations, to create that contact and reduce the series resistance.

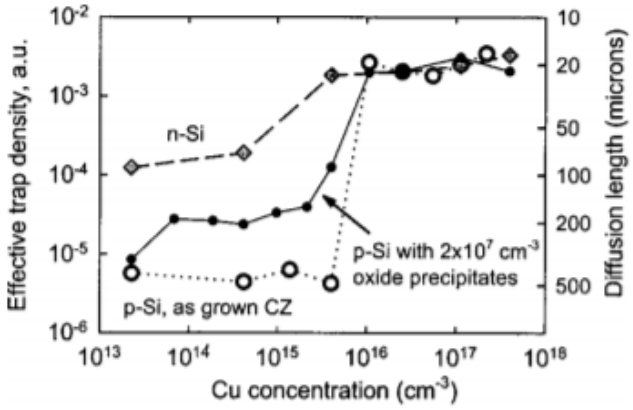



Figure 4.3: "shows 10 Ωcm CZ grown n-type Si samples (diamonds) effective trap density and minority carrier diffusion length as a function of Cu concentration, CZ grown p-type Si (open circles) at 10Ωcm, and internal gettering sites of the order of $2x10^7 cm^{-3}$" [19]

The first set of preliminary results to evaluate from using the atmospheric Cu-paste were the Sun's $V_{oc}$ measurements in Fig. 4.4. As previously stated, low concentrations of copper in n-type Silicon destroys the minority carrier lifetime, rendering the cell to be useless. The ideality factor reflects this concept, as it is an indicator of the junction quality. These results show that no diffusion of copper into the silicon bulk occurred since the Jo2 values are low and the ideality (n) factor is close to 1. For Sun's $V_{oc}$ not taking series resistance into account, the open circuit Voltage is high at around 660 mV with a reputable pseudo efficiency of approximately 20% [18].

The next set of preliminary results to review were the I-V Electrical Output parameters shown in Fig. 4.5. These results display successful annealing of the copper contacts without the copper diffusing into the silicon nor the copper oxidizing. One

| Cell ID | VOC (mV) | n-factor @ 1SUN | JO2 (A/cm$^2$) | Pseudo FF (%) | Pseudo Eff. (%) |
|---|---|---|---|---|---|
| V6-47 | 658 | 1.01 | 6.2E-9 | 83.0 | 20.0 |
| V6-10 | 660 | 0.95 | 1.2E-8 | 82.3 | 19.8 |
| V6-115 | 662 | 1.02 | 4.4E-9 | 83.3 | 20.1 |

Figure 4.4: Sun's VOC Measured Results [18]

parameter to compare between Fig. 4.4 and Fig. 4.5 is the efficiency. While the first figure showed the efficiency to be around 20%, the efficiency in the second figure is much lower at around 16.5%. This is due to series resistance (RS) being taken into account for. The results show higher series resistance values than one would want. The first step was to make good contact with the screen-printable atmospheric Cu paste, the next step will be tackling the high series resistance [18]. The series resistance in Fig. 4.5 suggests a thicker barrier between the Cu precipitates and the emitter. Future work on series resistance should focus on creating a thinner barrier for carriers to tunnel through it.

| Cell ID | VOC (mV) | JSC (mA/cm$^2$) | FF (%) | n-fa. | RS (Ω-cm$^2$) | Eff. (%) |
|---|---|---|---|---|---|---|
| V6-47 | 640 | 36.6 | 72.8 | 1.06 | 1.81 | 17.0 |
| V6-10 | 653 | 36.5 | 69.1 | 1.06 | 2.56 | 16.5 |
| V6-115 | 632 | 34.4 | 71.0 | 0.83 | 2.24 | 15.5 |

Figure 4.5: I-V Electrical Output Parameters Measured Results [18]

Another set of data that proves there was no deterioration on the effective minority carrier lifetime is Fig. 4.6, which also confirms that an effective barrier was formed. Figure 4.7 and 4.8 display the belt speed vs the series resistance and the fill factor,

respectively. Taking into consideration that more tests and data should be collected; the preliminary results show that at a peak temperature of 590°C and a belt speed of 300 IPM, the series resistance is at its lowest, the fill factor is at its highest.

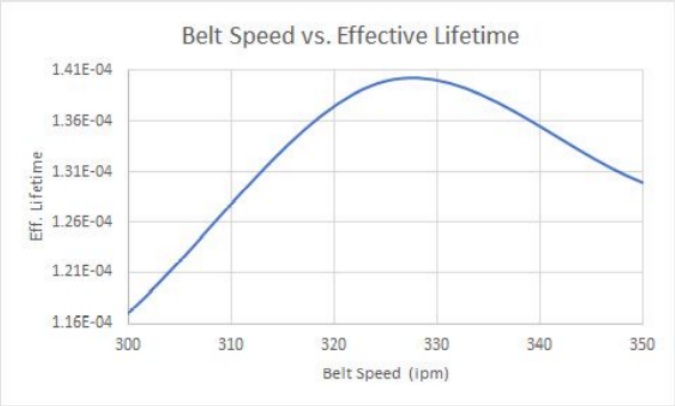



Figure 4.6: Belt Speed vs Minority Carrier Lifetime [18]

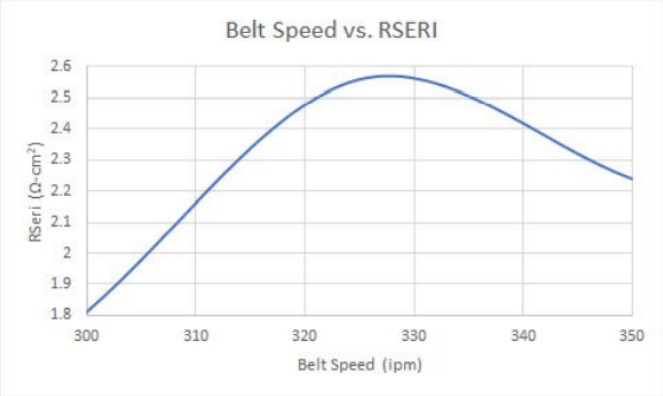



Figure 4.7: Belt Speed vs Series Resistance [18]

The last set of data analysed was the Electroluminescence (EL) imaging. Electroluminescence imaging works by exposing the solar cell to a voltage, which induces a current in the cell causing it to act as an LED. The cell then emits infrared light, which is captured by a camera. The areas which work exceptionally emit more infrared light causing the brighter areas of the cell. The darker areas of the cell are due to a higher series resistance in that area. Higher series resistance, means lower

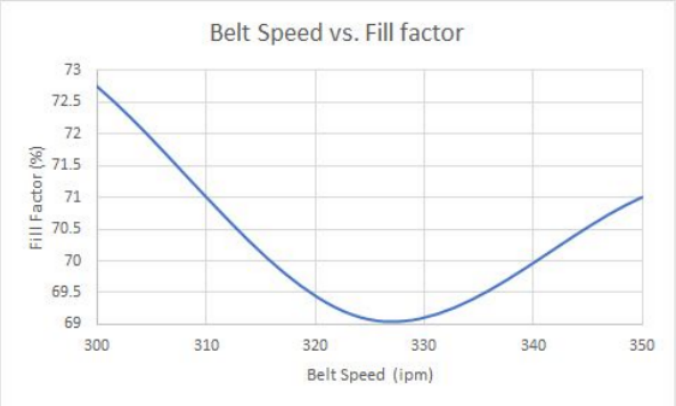



Figure 4.8: Belt Speed vs Fill Factor [18]

current, leading to less infrared light given off. Once the EL images were captured, they were then analysed using a software called ImageJ. This software calculates the ratio of light to dark of an image. Both of these parameters are displayed in Fig.4.9 below. The results suggest that the cell with the highest brightness should have the best series resistance, which in turn confirms that the copper paste PERC cells prefer higher temperature annealing with faster belt speeds. [18]

## 4.2 Copper Impact on Solar Cell

Creating a good contact where metal and semiconductor meet is an important factor in creating highly efficient solar cells. The quality of the contact between the metal and semiconductor is dependent on the potential barrier height. A high potential barrier blocks electrons from passing through. The difference between the work functions of the metal and the electron affinity of the semiconductor are the two factors of the potential barrier. To create good contact between these materials with low contact resistance, the values of these two factors should be very close to each other. If possible the work function of the metal should be smaller than the electron affinity of the semiconductor.

Contact is an important factor when developing a Cu paste. The challenges of creating good contact with Cu are due to oxidation, diffusion and degradation. The

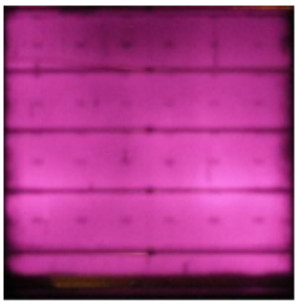
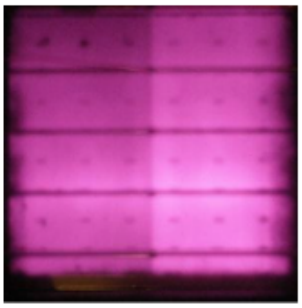
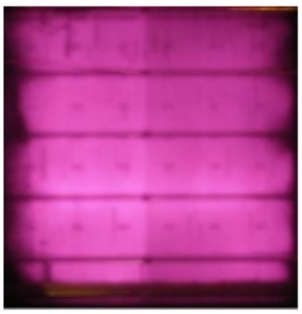
| Cell (Low Voltage) | EL Image | % area (ImageJ) |
|---|---|---|
| V6-47<br>590 Peak Temp.<br>300ipm |  | 30.18 |
| V6-10<br>588 Peak Temp.<br>325 ipm |  | 35.96 |
| V6-115<br>584 Peak Temp.<br>350 ipm |  | 29.03 |

Figure 4.9: Electroluminescence Imaging and ImageJ Calculations [18]

experimental results in the previous section have proven that these challenges have been overcome with the current Cu paste. One of the elements in the Cu paste that aids in creating a barrier to stop oxidation and diffusion is Antimony (Sb). Sb is a semi-metal and has a melting point of 630°C. It is often used in the electronics industry to fabricate semiconductor devices. Sb can be alloyed with other metals to improve their hardness and strength. [42]

# CHAPTER 5: CONCLUSION

Through the research proposed in this thesis a fundamental understanding of solar cells was established. It's characterization through open circuit voltage, short circuit current, and fill factor were discussed. Secondly, 130 different front metallization designs were simulated to fully understand the impact uneven bus bars and tapered fingers have on the efficiency of the solar cell. It was concluded that the design with 5UEBB/TPF was the most efficient design. Therefore increasing the amount of bus bars does not increase the efficiency, it in fact decreases its potential. Finally, replacing the traditional silver paste with copper paste is discussed. The initial experimental data acquired in the UNC Charlotte Photovoltaic Lab proved to have achieved good contact between the copper paste and the semiconductor. Copper's challenges of oxidation, diffusion and degradation were overcome.

For future work, it is recommended to design a front screen with uneven bus bars and tapered fingers as it not only decreases the amount of silver used, lowering costs, but it also increases the efficiency and lowers series resistance. This design should be printed on solar cells utilizing both an Ag paste and an Cu paste. Sun's Voc and IL images should be measured for these cells, and the results should be further analyzed to confirm that the front metallization design increases efficiency irrespective of the metal used for printing. For continued work on the atmospheric Copper paste, once good contact is consistent, there should be further analysis into reducing the series resistance.

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