MODEL PREDICTIVE CONTROL ON THERMAL STRESS REDUCTION FOR GRID-CONNECTED INVERTERS RELIABILITY ENHANCEMENT

by

Luocheng Wang

A dissertation submitted to the faculty of
The University of North Carolina at Charlotte
in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in
Electrical Engineering

Charlotte

2021

Approved by:

_____
Dr. Tiefu Zhao

_____
Dr. Madhav Manjrekar

_____
Dr. Babak Parkhideh

_____
Dr. Shen-En Chen

©2021
Luocheng Wang
ALL RIGHTS RESERVED

ABSTRACT

LUOCHENG WANG. Model Predictive Control on Thermal Stress Reduction for Grid-Connected Inverters Reliability Enhancement.
(Under the direction of DR. TIEFU ZHAO)

Thermal stress has been identified as one of the major failure causes in the power module. It is generated from the mechanical strain by severely varying temperatures at different loci in the power module and the different coefficients of the thermal expansion of materials, where the varying temperatures result from the real-time power loss across the power converter. This thermal stress accelerates the degradation of semiconductor devices, downgrades the system quality and efficiency, and eventually causes catastrophic system breakdowns and extensive economic losses. Therefore, this research is dedicated to investigating both local control level methods and system level strategies to ameliorate the real-time power loss in order to reduce the thermal stress in the power module, thereby extend the component lifetime and enhance the system reliability.

Prior work for local control level methods including the modulation method, and the control target method shows an effective progress on the power loss and thermal stress reductions. However, the increased control loops and complicated modulation schemes in the modulation method affect the system stability. The onefold feature of temperature rising and scalability issue in the control target method restrict the degree on the thermal stress reduction. Besides, prior work for system level strategies is still in its infancy, where a few of strategies are developed preliminarily to reduce the thermal stress and coordinate the power sharing method for the multiple inverters microgrid. However, these strategies

are all power sharing oriented instead of being thermal stress oriented. They may present a limited adjustment on the thermal profile.

In this research, novel local control level method and system level strategy are developed. First, a finite-control-set model predictive control (FCS-MPC) is introduced and deductively investigated from the local control level. Its variable switching frequency property is derived through the geometry analysis on the voltage vector space. It realizes the switching frequency variation autonomously by the loading power. By taking advantage of this property, the power loss is leveled in the real-time operation by FCS-MPC and a more mitigated thermal profile is acquired compared with the one by the conventional controller. Furthermore, an energy-loss-minimization secondary problem formulation in FCS-MPC is proposed to reduce the power loss in order to achieve the junction temperature mean value decreasing in the power module. This secondary problem formulation is integrated with the basic problem formulation by different weightings to achieve the power flow control and the power loss reduction simultaneously. Second, a centralized thermal stress oriented dispatch (TSOD) system level strategy is proposed for multiple paralleled distributed energy resource systems, which help to reduce the thermal stress in the power module of paralleled converters. It is thermal stress oriented and takes effect according to the real-time junction temperature variation, the health condition of the individual converter and the system operation. Two local control level methods, the switching frequency variation and the reactive power injection, are imported separately as the dispatch algorithm to generate the expected power loss. Dealing with the varying mission profile, the more mitigated thermal profiles are achieved for all converters with the assistance of the proposed TSOD strategy.

The effectiveness of all methodologies from both local control level and system level is validated in the simulations, experiments, and Model-in-the-Loop testing. A long-time-scale analysis from the reliability assessment is also conducted to quantify the impacts of the relieved thermal stress on the damage and lifetime of the power module. Results justify the significant thermal stress reduction in the power module of the converter, which is the main contribution of this research.

ACKNOWLEDGEMENTS

I would like to express my greatest and sincere gratitude to my advisor, Professor Tiefu Zhao, for his patience, guidance and supervision throughout these years. The scientific methods and work ethic he taught me made where I am now. I could not have imagined having a better advisor and mentor for my Ph.D. study.

I would also like to thank Dr. Jiangbiao He, Dr. Jiayi Guo and Dr. Tao Han for their technical supports on the converter control, the optimization algorithm, and the communication system setup, respectively, to my research.

Besides, my sincere thanks also go to my committee members: Dr. Madhav Manjrekar and Dr. Babak Parkhideh, my graduate faculty representative: Dr. Shen-En Chen for their innovative comments and advice, all group members from Renewable Energy and Power Electronics Advanced Research Lab (RE-PEARL) for their kindly help.

I appreciate the GASP grant from UNC-Charlotte and the financial support from North Carolina Renewable Ocean Energy Program, administered by the Coastal Studies Institute.

In the end, I would like to thank my family and my friends for supporting me spiritually throughout my research and my life in general.

I dedicate this dissertation to my family,

and all medical staff devoting their lives to fighting Coronavirus Disease.

Thank you all.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AC	alternating current
AD	accumulative damage
ADCP	acoustic doppler current profile
AFE	active front end
Al	aluminum
ATC	active thermal control
BJT	bipolar junction transistor
Cap	capacitor
CCS-MPC	continuous-control-set model predictive control
CPWM	continuous pulse width modulaton
CTE	coefficient of thermal expansion
DBC	direct bond copper
DC	direct current
DER	distributed energy resources
DPWM	discontinuous pulse-width modulation
EOD	electrostatic discharge
EOS	electrical overstress
FCS-MPC	finite-control-set model predictive control
FOP	feasible operation region on power vector space
FOV	feasible operation region on voltage vector space
GCI	grid-connected inverter
HIL	hardware-in-the-loop

IGBT	insulated-gate bipolar transistor
IPM	intelligent power module
LR	line reactor
MHK	marine hydrokinetic device
MIL	model-in-the-loop testing
MOSFET	metal–oxide–semiconductor field-effect transistor
MP	mission profile
MPC	model predictive control
OCEC	ocean current energy conversion
PCC	point of common coupling
PI	proportional integral linear control
PO	physical object
PoF	physics-of-failure
PWM	pulse-width modulation
RPI	reactive power injection
SEM	scanning electron microscope
SFV	switching frequency variation
Si	silicon
SM	submodule
SVM	space vector modulation
THD	total harmonics distortion
TSOD	thermal stress oriented dispatch
TSOD-RPI -FCSMPC	FCS-MPC-controlled GCI with TSOD strategy and reactive power dispatch action

TSOD-RPI-PI	PI-controlled GCI with TSOD strategy and reactive power dispatch action
TSOD-SFV-PI	PI-controlled GCI with TSOD strategy and switching frequency dispatch action
UPFC	unity power factor control
VO	virtual object
WPT	wireless power transfer

CHAPTER 1: INTRODUCTION

1.1 Background on Thermal Stress of Power Modules

Recent estimates indicate that the maximum theoretical annual energy that could be produced from ocean waves and tidal currents is approximately 1,846 TWh per year in North America, approximately 45% of annual U.S. energy demand [1]. With the development of the ocean current energy converter (OCEC) which is a marine hydrokinetic (MHK) device converting fluid kinetic energy into mechanical energy, OCEC system can be planned as the distributed energy resource (DER) system similar to the wind power and solar energy [2]. With advanced power electronics technologies adopted in these DER systems [3]-[5], such as grid-connected inverters (GCI) [6], [7], and solid-state transformers [8], power converters are playing significant roles to transmit and synchronize the power from the front-end renewable energy mechanisms to the main grid.

The most common layout in these DER systems is designed as the multi-stage inline configuration, including the machine side converter unit and the grid side converter unit which are interconnected through a DC bus [3]. The machine side converter, as the name implies, is connected to the front-end renewable energy mechanism and oriented to regulate the real power generated in the DER systems, which normally could be the active front end (AFE) in the wind power and OCEC systems or the DC/DC converter in the solar energy. The grid side converter, on the contrary, is connected to the main AC grid and oriented to synchronize the real power to the grid, which are grid-connected inverters or inverter supply units. Meanwhile, these grid-connected inverters in the industry are equipped with services of the DC bus voltage regulation and the reactive power control, which provides this inline configuration with more flexibilities in the practical applications.

However, the lifetime of power converters in this configuration extremely suffers from the intermittent renewable energy generation which is highly affected by instantaneous environmental conditions. The generated power or the mission profile usually has a large variation in a short duration [9]-[12]. Because of the inline structure, power converters will bear such variation of the real power from hundreds of kilowatts to several megawatts. This variation not only induces the surge and the slump of the power flow on the converter, which increases control requirements in both transient and steady states, but also arises a fast-varying power loss across the power converter. This varying power loss is rapidly aggregated inside of the power module in the form of heat which produces a severe thermal cycling in the power converter over the mission profile [13]. From several military handbook and data surveys [2], [14], [15], it is this thermal cycling that dominates the failure causes of the power converter. It accelerates the degradation of components in the power converter, especially to power modules, and eventually makes the power converter malfunctional and failed.

1.2 Physics-of-Failure of Power Modules

The power module which is fabricated with single or multiple semiconductor devices has been justified as one of the most vulnerable components in the power converter. Failure mechanisms of one typical power module include the chip-related and package-related mechanisms [16]-[18]. Chip-related failure mechanisms are those that destroy a device thoroughly and make the power module malfunctional. The following stated are some the most frequent chip-related failure mechanisms.

1) *Electrical Overstress*: Electrical overstress (EOS) is associated with overvoltage and overcurrent operating conditions.

2) *Electrostatic Discharge*: Electrostatic discharge (ESD) can partially puncture the gate oxide, allowing the device to work sufficiently well for the device to pass inspection, and finally, causing device failure.
3) *Latch-Up and Triggering of Parasitic*: A large value of *dv/dt* during turn-off may cause triggering of the parasitic thryristor in insulated-gate bipolar transistors (IGBTs) or bipolar junction transistor (BJT) in power metal–oxide–semiconductor field-effect transistors (MOSFETs).
4) *Ionic Contamination or Hot Carrier Injection*: Ionic contamination causes the electric field distortion in the passivation of the high-field region and hot carrier injection comes from the growth of defects in the gate oxide.
5) *Electromigration, Contact, and Stress-Induced Migration*: These mechanisms are related to the metallization of the semiconductor devises and influence long-term reliability.
6) *Thermal Activation*: Thermally activated processes are enhanced by an increase in temperature.
7) *External Radiation*: Ionization and displacement damage in power semiconductor devices was observed due to the protons and electrons confined in the earth's magnetic field.
8) *Other Mechanisms for MOS-Gated Devices*: These include the developing of slow trapping levels, microcracking of aluminum metallization, and electromigration of metallization.

Failures on chips can be caused by one or several above failure mechanisms. Most of time, they can be interlinked with package-related failure mechanisms which are

regarded to be more significant in power modules [16]. IGBT modules are typically classified into two types of the packaging: the wire-bonded IGBT module and the press-pack IGBT module. They have different characteristics which is a tradeoff between cost and performance [17]-[18]. By direct press-pack contact for soldering and bond-wire connection, press-pack packaging has the improved reliability, higher power density and better cooling capability than the wire-bonded packaging. However, due to the low cost, wire-bonded packaging IGBT modules are still widely used and absorb the most focuses to address the reliability problem.

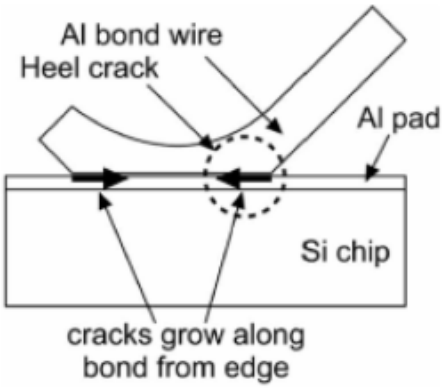


Figure 1.1: Bond wire crack diagram

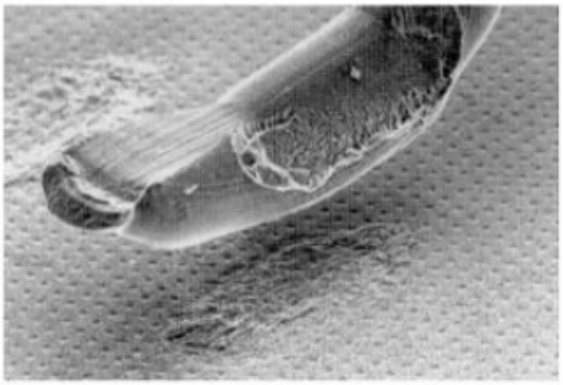


Figure 1.2: SEM image of bond-wire liftoff

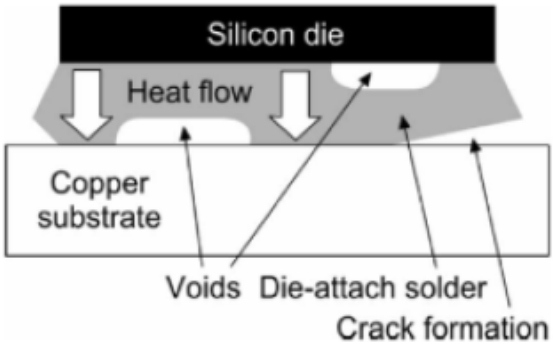


Figure 1.3: Solder joint fatigue diagram

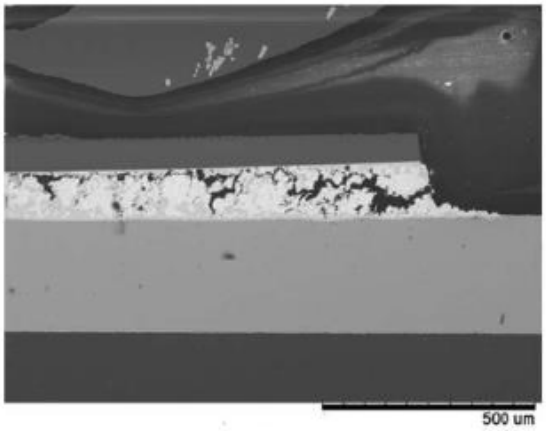


Figure 1.4: SEM image of solder joint fatigue

Two major failure mechanisms in the wire-bonded packaging of IGBT modules are bond-wire liftoff and solder joint fatigue [16]-[18], shown in Figures 1.1, 1.2, 1.3, and 1.4.

1) *Bond-Wire Liftoff*: This failure is mainly caused by thermal mechanic strain of coefficients of the thermal expansion (CTE) mismatch between different material interfaces. The crack appears between aluminum (Al) bond wire and silicon (Si) chip and grows along the interface from both ends to the center due to different CTEs of Al and Si. Eventually, the bond-wire is liftoff. After several testing, it is noted that the huge junction temperature swing value ΔT_j dominates this failure.

2) *Solder Joint Fatigue*: This failure is mainly caused by a shear stress in the solder layer and eventually cracks. The shear stress also comes from the CTEs mismatch between two solder joints, Si chip and direct-bond copper (DBC), DBC and baseplate. This failure results in the increased thermal resistance of IGBT modules, which further increases the junction temperature T_j.

There are some other failure mechanisms found in the wire-bonded packaging IGBT modules, like electrical stress or wire burnout. All these failure mechanisms are related to the thermal cycling in the power module. Two indicators reflecting this thermal cycling are the swing value ΔT_j and the mean value $\overline{T}_j$. When this thermal cycling exceeds the tolerance strength of the power module, it becomes the thermal stress. Thus, **the thermal stress reduction including the temperature swing value reduction, the temperature mean value reduction, and the diminished power-on time** is always desired [19]. It may benefit power modules with not only slowing down the degradation of semiconductor devices, but also monitoring the temperature information and quantifying the cumulative damage. Eventually, it extends the lifetime of the power converter and improves the reliability of the power electronics system.

1.3 Model Predictive Control on Power Converters and Motor Drives

Recently, with advances in microprocessors, a nonlinear control algorithm, model predictive control (MPC), has been gradually employed in the power electronics system for power converters and motor drives [20]-[39]. According to the specific working principle, MPC in the power electronics system can be categorized into two main parts, as shown in Figure 1.5, depending on whether they need an additional modulator to determine the switching state. For those of which needs an additional modulator, this group is called

indirect MPC, where an additional modulator is required to translate the linear voltage vector into the nonlinear switching vector. Hence, the control input in these MPC problem formulations is just a set of the real-valued vector. In addition to the indirect MPC, for those of which does not need an additional modulator, this group is called direct MPC, where the discrete switching vector will be derived directly from these MPC problem formulations. Hence, the control input in these MPC problem formulations is a set of integer vectors or integer and real number vectors. Due to the easily online implementation, the effective performance, and the acceptable computation stress, direct MPC becomes the most popular research hotspot in the power electronics system, not only in the MPC, but also in all different power electronics control methods.

There are three subcategories in the direct MPC as shown in Figure 1.5. Direct MPC include controllers with the hysteresis bound, finite control set and continuous control set. Direct MPC with the hysteresis bound is the first format that MPC is used in the power electronics system. This algorithm uses the hysteresis bound to constrain the state variable in the problem formulation, such as the electromagnetic torque or the magnitude of the stator flux for the motor drive applications. The flexibility of different types of hysteresis bounds is made fully use of to enhance the system performance in other factors such as the harmonic distortions and switching losses [30]. Later, direct MPC with finite control set (FCS-MPC) and continuous control set (CCS-MPC) are introduced in the past decade to the power electronics system and already become the most favored research interests in academia. The distinction between these two comes from the number of the feasible inputs. Since FCS-MPC outputs only one switching state over each control time interval, the duration is the whole control time interval and the time factor is not manipulated in this

control algorithm. Hence, the number of the feasible inputs are finite and known as the discrete switching vectors. For example, for a conventional two-level three-phase converter, the number of feasible inputs is eight, which are eight switching vectors on the voltage vector space. This number is only determined by the topology of the converter, or simply the number of the active switch. However, the time factor is manipulated in the CCS-MPC, where as many as switching states can be output as long as the total duration equals to each control time interval. The number of feasible inputs is infinity in this case, and any combinations of the switching states and their durations could be possible. This distinction completely gives the different advantages between FCS-MPC and CCS-MPC. Due to the intuitive design procedure, the single switching state output, and straightforward implementation [35], FCS-MPC achieves the features of the fast dynamic response and multiple objectives and constrains integration. It also generates the least online computation stress to the microprocessor and a potential to predict the system in an extended receding horizon, which are important for the most of industry applications. On the other hand, due to the infinite feasible inputs, CCS-MPC can certainly expect a better optimal value and a more global solution in the problem formulation and an enhanced steady state performance in the power electronics system could be achieved, which is good for some subtle applications like the aerospace. Moreover, because the switching state can be manipulated within each control iteration in CCS-MPC, some switching related objectives could be designed and controlled as well, such as the fixed switching frequency and a deterministic switching loss [36], which is also a huge concern for FCS-MPC. The variable switching frequency feature of FCS-MPC induces severe concerns on the power

loss estimation, the thermal management, and the filter design in the power electronics system, which is investigated in this dissertation.

In this dissertation, FCS-MPC is fully investigated, not only on its basic working principle, like the variable switching frequency property, but also on its feature on the multiple objectives integration. Besides, its superior performance on the thermal stress reduction of the power converter compared with the conventional PI controller is also demonstrated, which is dedicated to comprehend FCS-MPC thoroughly, explore more opportunities for future industry applications, and provide engineers with more insights to fully leverage the FCS-MPC.

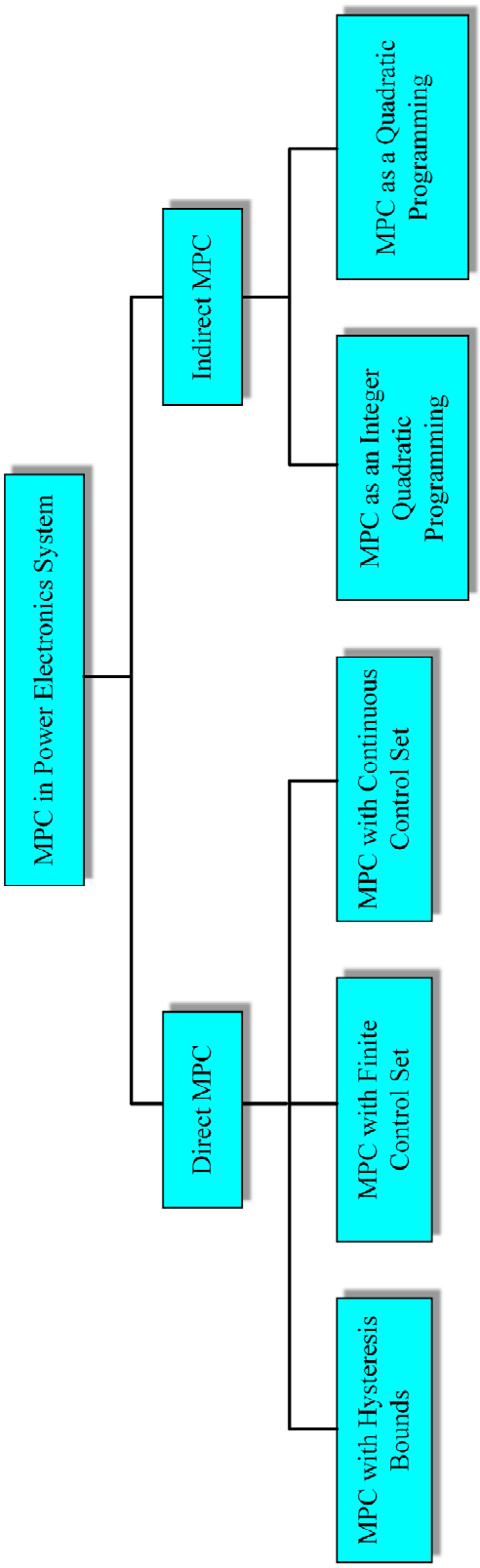


Figure 1.5: Classification of MPC methods in power electronics systems

1.4 Overview of the Proposed Research

In the purpose of reducing the thermal stress in the power module, the novel local control level method and system level strategy are developed in this dissertation. The roadmap on the research trend of the thermal stress reduction methods is summarized in Figure 1.6. It is noted that the thermal stress reduction method for power modules is initiated after 21st century. In the past decade, thermal stress reduction methods surge and gradually spread from the local control level to the hardware level, and further at this moment, to the system level. More and more researchers, universities, and industries participated into this field and were dedicated to the reliability of the power electronics system. The work in this dissertation honorably made a few contributions to the thermal stress reduction methods from the local control level and the system level and was expected to supplement the holistic development of the power electronics research.

First, a finite-control-set model predictive control is introduced and deductively investigated from the local control level. In this part, the variable switching frequency property of the finite control set model predictive control has been investigated. The intuitive relationship between the switching frequency and the magnitude of the converter output voltage reference is proposed through the geometry analysis, by the switching state selection and the switching sequence formulation. The switching frequency is derived to be maximized when the magnitude of the converter output voltage reference is around one third of the DC-bus voltage value. Then, the switching frequency decreases in both directions that the magnitude moves away from this value. Multiple operating points from the contoured feasible operation range are tested. The impacts of this property on the power loss and current harmonics are also analyzed, which provides engineers and researchers

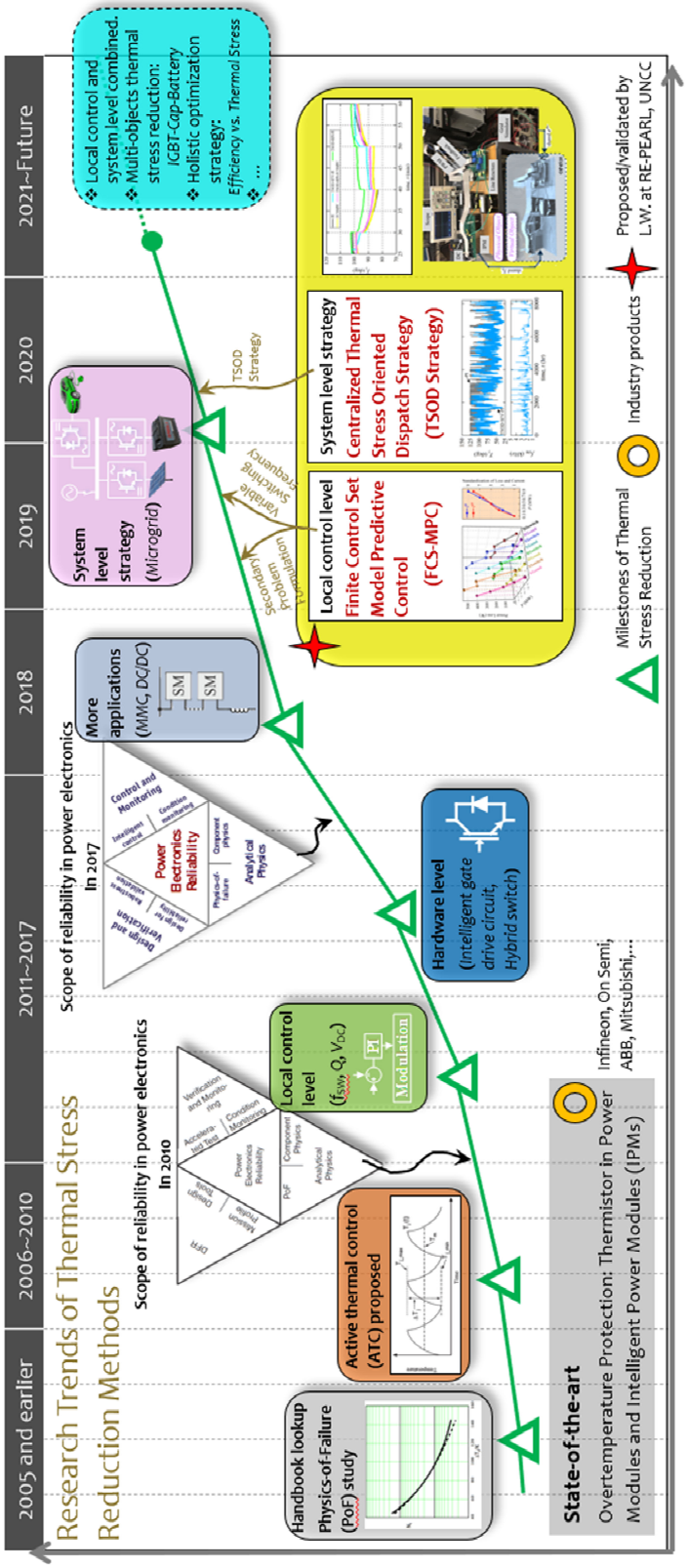


Figure 1.6: Roadmap of thermal stress reduction methods and proposed research contributions from this dissertation

with more insights to fully leverage the finite-control-set model predictive control. One application of this proposed variable switching frequency property is presented to demonstrate the lower thermal stress of power modules by finite-control-set model predictive control compared with the conventional PI controller, where a less-varying temperature profile is achieved over the same mission profile. This contribution can significantly benefit the distributed energy resource systems in the industry application.

Second, a finite-control-set model predictive control with secondary problem formulation is proposed in this part to reduce the power loss of semiconductor devices and then relieve the thermal stress in power modules. By introducing the integrated objective function, it heuristically selects the optimal switching state to achieve a lower power loss while maintaining the normal power flow control. This power loss minimization is estimated from an energy-based loss model as the secondary problem formulation. Compared with other strategies, it eliminates the complicated control loops and modulation schemes. The impact of the problem formulation weightings on the system performance is investigated. A power loss reduction rate variation is observed against different secondary weightings. Based on this, a most efficient weighting curve for different power loadings and a weighting-zones strategy for the grid code compliance are presented, which provide engineers with guidelines to design the proposed finite-control-set model predictive control.

Last but not least, in this part, a centralized thermal stress oriented dispatch system level strategy is proposed to reduce the thermal stress for paralleled grid-connected inverters. In the proposed strategy, the instantaneous thermal stress is identified first, followed by the expected junction temperature and power loss calculations. Then, the proposed strategy takes full advantages of the local control level methods, including the

switching frequency variation and the reactive power injection, to generate the expected power loss and achieve a desired thermal profile with a reduced thermal stress for all paralleled inverters. It turns out that with the proposed centralized thermal stress oriented dispatch strategy, the thermal stress is significantly reduced for both PI and finite-control-set model predictive control controlled inverters. Considering the tradeoff from the system efficiency, the proposed centralized thermal stress oriented dispatch strategy with the switching frequency dispatch algorithm will be chosen to achieve the least thermal stress, the longest lifetime, and the highest system efficiency for paralleled inverters.

1.5 Dissertation Organization

The rest of the dissertation is organized as follows. In Chapter 2, literature review on the power loss and thermal stress reduction methods from the peer work is introduced and categorized. In Chapter 3, the variable switching frequency property of finite-control-set model predictive control is investigated and its impacts and applications on the local control level thermal stress reduction method are presented compared with the conventional linear PI controller. In Chapter 4, a finite-control-set model predictive control with the energy-loss-minimization secondary problem formulation is proposed to further reduce the thermal stress by heuristically reducing the power loss from the local control level. In Chapter 5, a centralized thermal stress oriented dispatch system level strategy is developed for the thermal stress reductions on multiple paralleled grid-connected inverters. Following that, the conclusion, publications and the future work are listed in Chapter 6.

CHAPTER 2 RELATED WORK

In the purpose of relieving such thermal stress and enhancing the reliability of the power electronics system, some researches have been carried out from the following categories: the local control level, the hardware level and the system level to achieve this goal. Several survey and review papers in the past few years have studied and summarized some of these contributions [40]-[43].

2.1 Local Control Level Method

The local control level methods are first introduced, and they are also the first domain that the thermal stress reduction methods have been developed [44]-[87]. Based on the different concentrations in this category, most of them can be divided into the modulation method and the control target method. In the modulation method, the main approach is to manipulate the modulation scheme in order to change the power loss and thereby reduce the thermal stress in the real-time operation. One main solution is to change the switching frequency for those continuous pulse width modulation (CPWM) [44]-[54]. This is because the switching frequency is linear proportional to the switching loss in the CPWM, where the switching loss takes up a significant portion of the power loss in high power applications. The change of the switching frequency would explicitly level the power loss over the varying mission profile and further reduce the thermal stress. Initial concept is presented in [44], where the range of the junction temperature is partitioned into different zones and the switching frequency is adjusted to confine the junction temperature in the moderate zone. An improved method is proposed in [47] and [49] by using the state machine to identify operating states of semiconductor devices and adjust the switching frequency, where its control block diagram is shown in Figure 2.1. Similar idea is also

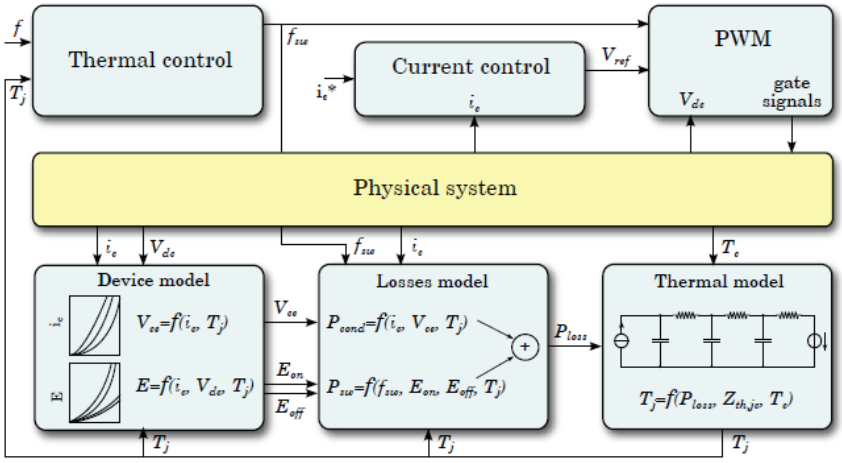


Figure 2.1: Control block diagram of ATC [47]

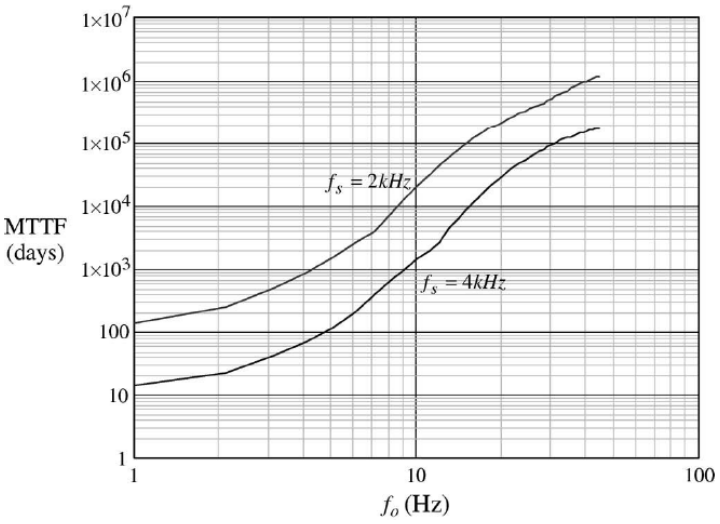


Figure 2.2: Mean-time-to-failure of the motor drive under rated output current by varying switching frequency [45]

implemented in [45], [46], [48], and [50]. [45] investigates the switching frequency variation in the motor drive application as shown in Figure 2.2, where the switching frequency is reduced with the increase of the speed range. [48] investigates the switching frequency variation in the DC/DC converter with the high operating frequency. Another solution is to change the PWM mode in order to change the power loss in the real-time

operation [53]-[61]. In this case, the whole PWM mode is changed instead of just varying the switching frequency in the CPWM. The generic idea is to reduce the number of the hard switching by different firing angles through different PWM modes in the high power loading period and restore the number of hard switching in the low power loading period. A combined modulation method is presented in [53], [60] and [61], that the discontinuous-PWM and space vector modulation (SVM) are adopted respectively for the high power and the low power loadings, where the number of hard switching events decreases by discontinuous-PWM in the high power period and so does the switching loss. [54] combines the SVM and its overmodulation patterns for different power loadings. Both switching frequency variation and different modulation modes combination present their effective performance on the thermal stress reduction. In general, the modulation method manipulates the hard switching, which helps to level the power loss over the mission profile and reduce the thermal stress. However, the local controller complexity has been much increased and may adversely affect the stability of the system.

The second one is the control target method. The main approach is to change the operating point of the power converter [62]-[78]. This is attributed to the dependency of the power loss on the conduction current, the phase angle, the modulation index and the device voltage. Several control targets are investigated to level the power loss and further reduce the thermal stress, including the real power, the DC link voltage, and the reactive power.

First, the real power is controlled [62]-[64]. This is the most straightforward way to level the power loss and reduce the thermal stress since the real power is directly relate to the mission profile which is critical to the thermal cycling in the power converter. [62]-

[63] develop the power limit control to limit power according to the junction temperature of the power module and integrate this power limit control to the conventional maximum power point tracking.

Second control target is the DC link voltage [65]-[67], where the link voltage is adapted during the low speed operation of the motor drive to reduce the semiconductor device voltage and so does the switching loss. All work in the motor drive application. However, the DC link voltage adaption sacrifices the output voltage limit of all linked converters and may deteriorate the thermal stress on other linked power converters. In DER systems, the DC link voltage is regulated at the nominal value most of the time.

One major control target is the reactive power [68]-[73]. The reactive power directly changes the conduction current flowing through the power converter, which would adjust both the conduction loss and the switching loss of power modules. Superior to the DC link voltage adaption, the reactive power injected to one converter is isolated from others. This method is investigated between paralleled neutral point clamped (NPC) converters in [68] and [69]. In addition to the capability of the low-voltage ride through (LVRT), it has been validated that the reactive power can reduce the thermal stress by injecting either capacitive or inductive reactive power, which is also justified for the shunt configuration in DER systems [70]-[73]. However, this reactive power injection method can only generate more power losses than the one under the unity power factor control, which means it would reduce the temperature swing value, but increase the mean value in return. Hence, the impact of the reactive power injection on the lifetime extension and the reliability becomes ambiguous. Besides, the complexity of the reactive power dispatch in these methods is exponentially increased with the number of paralleled converters, which

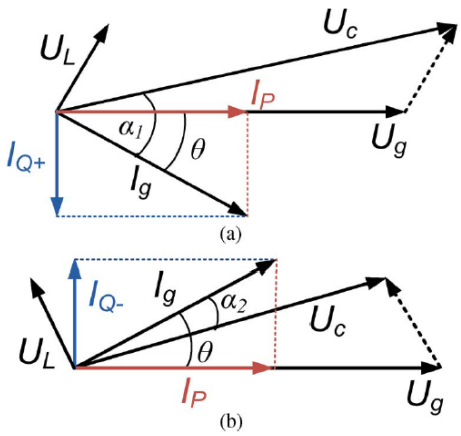


Figure 2.3: Phasor diagram by introducing reactive power to the grid-connected inverter [68]

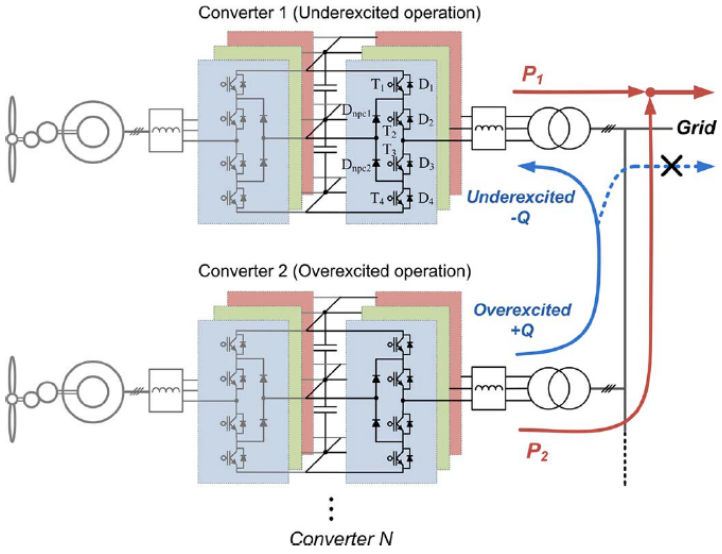


Figure 2.4: Reactive power circulated in paralleled grid-connected inverters [68]

performs a low scalability and suppresses its implementation in DER systems as depicted in Figure 2.4.

Last but not least, there are some other control targets adjustment, such as the output AC voltage in [74] and [75], where the output AC voltage on the LC filter is adjusted in order to change the flowing current at the same power loading and reduce the thermal stress.

Similar idea is also adopted in the motor drive [76], where the trajectory is shifted in order to inject or absorb the current vector and reduce the thermal stress.

All above local control level methods are calibrated with the conventional linear PI controller. Some novel converter controllers are also noticed to have the potential to reduce the thermal stress of inverters, such as the model predictive control [77]-[85]. Most of this novel control method develop a secondary problem formulation on the power loss or the temperature control and integrate it to the primary power flow problem formulation. The rest of them simplify the secondary objective function by reducing the number of the hard switching events instead of directly reducing the power loss or regulating the temperature, which saves lots of online computation efforts as in [77], [83], and [84].

2.2 Hardware Level Method

Apart from the above local control level methods, the hardware level thermal stress reduction methods also have been investigated a lot.

They mainly can be divided into two part. One requires the additional topology or the device, which alters the basic circuit topology or the device fabrication [86]-[92]. [86] embedded a thermoelectric cooling interface between the baseplate of the power module and the heatsink in order to measure the thermal profile by Seebeck effect. Sametime, it enables to control the temperature at that layer and then the junction temperature can be altered. [87] and [89] both change the switching trajectories of the power semiconductor devices. This is because the turn-on and turn-off trajectories directly determine the switching loss in the real-time operation. Several paralleled snubber RC resonant circuits are used in [89] in order to generate different switching trajectories and switching losses as shown in Figure 2.5. [90]-[92] intelligently select different gate resistance for the gate

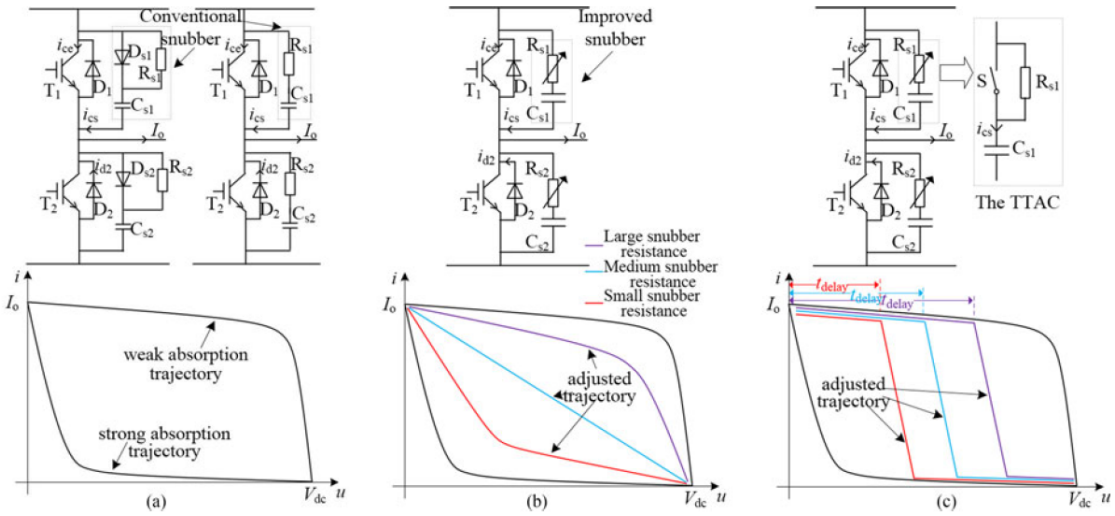


Figure 2.5: The different snubber circuits and turn-off trajectories [87]

signal in order to adjust the switching loss. These two objectives are much closer to the power loss generation than the above local control level methods, which mean they might have better performance than the local control level method. However, the complexity in the gate drive circuit is hugely increased and may adversely affect the system stability and cost.

Another group is related to the gate signal control. This is more inclined to the paralleled power module topology, which becomes a rapid growing topic recently due to the introduction of the wideband gap semiconductor devices. A hybrid or paralleled Si IGBT and SiC MOSFET configuration can achieve a higher system efficiency due to the zero voltage switching on the Si IGBT and a lower system cost due to the low current rated SiC MOSFET. The gate signal control can effectively benefit the temperature balancing between these paralleled devices. [96] and [97] both control the delay time of gate signals to Si IGBT and SiC MOSFET and then the difference on the junction temperatures of Si

IGBT and SiC MOSFET could be minimized and the thermal stress on both switches presents the same level.

Hardware level methods involve the change on the circuit or the device, which brings in the unexpected control and stability issue and may not be the best solution for those high power applications.

2.3 System Level Method

Recently, the system level thermal stress reduction methods start to absorb more and more attentions. The research interests on the thermal stress reduction shift from the local side individual converter to the multiple modular converters and even broader level, like the microgrid.

The first subarea of the system level thermal stress reduction methods focuses on the modular converter units [98]-[109]. All these modular converter units share the responsibility of the one total mission profile and the mission profile on each module is related and not independent. In this case, the real power can be coordinated between these modular units. [98] first propose this concept, named by power routing as shown in Figure 2.6, and level the power loss and reduce the thermal stress by coordinating the real power flow between these modular units. Power sharing between these units are not evenly anymore. The unit suffered from more severe health condition can achieve a less-thermal-stressed power flow and other units would take care of the rest power loading. This goes friendly with applications using the modular multilevel converter or the cascaded converter configuration since multiple units are employed in the local topology and they are sharing the same total mission profile from the upstream. However, this result of this power routing highly depends on the solution of the problem formulation and the solver, where [105]

solves the amount of the power routed in each unit by graph theory and more advanced optimization solution is desired for this method. This strategy also benefits the harmonics distribution [103] and [104], where the harmonics are redistributed by this thermal control and the total harmonic distortion is reduced. For those multiple units sharing different mission profiles or overloading periods, the power routing capability on the thermal stress reduction is highly limited due to the low adjustment degree. And the following method is introduced to deal with that situation.

The second subarea of the system level thermal stress reduction methods focuses on the different functional converters in the microgrid [106]-[109]. Normally, there are two kinds of roles converters are playing of in the microgrid, grid-forming/supporting inverters and grid-feeding inverters. In order to maintain the stable operation for the microgrid in both grid-connected and islanded modes, grid-forming/supporting inverters have to participate into the primary level control for the power sharing. The mission profiles of these inverters are independent and autonomous. In this case, the thermal stress reduction is realized by adjusting the power sharing slope, or the droop gain, and then adjusting the real power and reactive power injecting into the microgrid. Due to the droop control used in the power sharing layer of the microgrid hierarchical control, the communication is not required in these control methods, where the thermal stress reduction methods are also communicationless even though it's system level strategy. [106] implement this idea in the DC microgrid, where multiple grid-supporting inverters and grid feeding inverters are involved in this DC microgrid. The reliability coefficient is defined to adjust the power sharing based on the original droop gain, where if the reliability coefficient is one, the power sharing follows the original slope and if the reliability coefficient is zero, the power

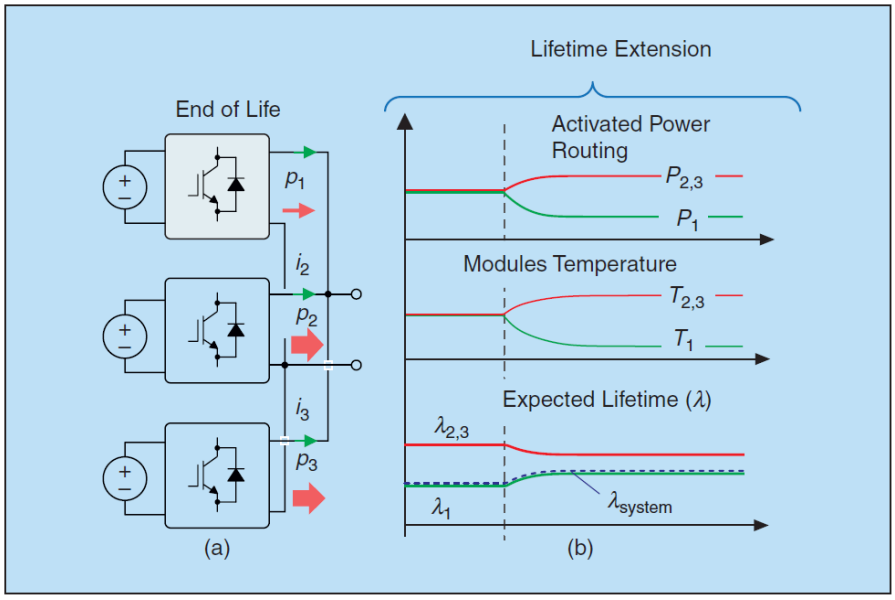


Figure 2.6: An example of power routing's impact on the lifetime of a modular system [98]

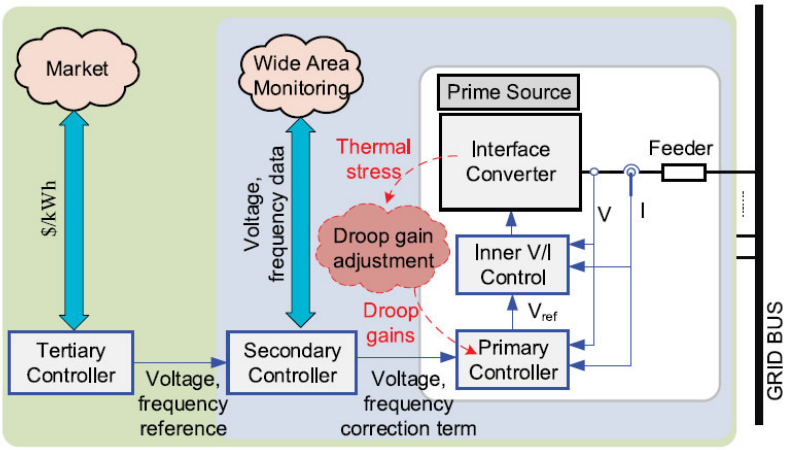


Figure 2.7: Hierarchical control level of an AC microgrid [108]

sharing follow the zero thermal stress. This system level thermal stress method take advantage of the autonomous operation of the droop control and reduce the thermal stress for all paralleled inverters. [107] and [108] verify it effective in the AC microgrid as well as shown in Figure 2.7. Furthermore, [109] summarizes the methodology of this system

level thermal stress reduction method and formulate it into the microgrid hierarchical control for a future framework of the industry application.

CHAPTER 3 INVESTIGATION OF VARIABLE SWITCHING FREQUENCY IN FINITE-CONTROL-SET MODEL PREDICTIVE CONTROL

With only the finite number of switching states from the power converter, finite-control-set model predictive control (FCS-MPC) heuristically selects the optimal switching state among all candidates. The selection of the optimal state is determined by minimizing the objective function from the defined problem formulation. This control algorithm of FCS-MPC brings system with significant features of the fast dynamic response, the nonlinear system formulation and the multiple objectives and constraints integration. However, the basic problem formulation which only contains the current objective function is not fully studied. In this chapter, this basic problem formulation is deeply investigated to reveal the variable switching frequency property of FCS-MPC.

The generic control block diagram of FCS-MPC with the basic problem formulation is presented in Figure 3.1. A two-level three-phase voltage source converter is interconnected between an AC grid and a DC bus as the grid-connected inverter (GCI), where its line current $\boldsymbol{i}^{abc} \in \mathbb{R}^{3x1}$ is regulated to synchronize with the grid voltage $\boldsymbol{e}^{abc} \in \mathbb{R}^{3x1}$ and transmit all the real power to the grid according to the front-end mechanism. The regulation of DC bus voltage V_{dc} is added on the periphery of this block diagram. Since it would not affect the algorithm of the FCS-MPC, only interfere in the current reference $\boldsymbol{i}^{dq*} \in \mathbb{R}^{2x1}$ in the transient state, it is not included in the analysis.

3.1 Variable Switching Frequency Property of Finite-Control-Set Model Predictive Control

3.1.1 System Modeling on Voltage Vector Space

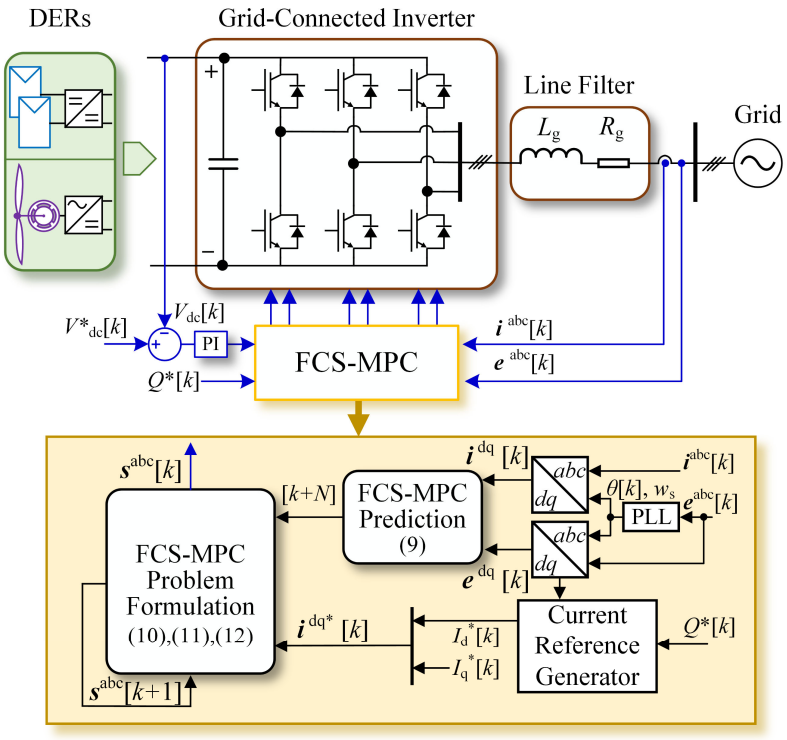


Figure 3.1: System diagram of the GCI regulated by FCS-MPC with the basic problem formulation.

The control algorithm of FCS-MPC contains two sequential sections as emphasized in Figure 3.1, the prediction and the problem formulation. The former predicts the state variables based on the system modeling. In this case, it is developed in the rotating *dq* reference frame and expressed as follows:

$$L_g \begin{bmatrix} \frac{dI_d}{dt} \\ \frac{dI_q}{dt} \end{bmatrix} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} - \begin{bmatrix} E_d \\ E_q \end{bmatrix} - R_g \begin{bmatrix} I_d \\ I_q \end{bmatrix} - w_s L_g \begin{bmatrix} -I_q \\ I_d \end{bmatrix} \tag{3.1}$$

$$\mathbf{T} \triangleq \begin{cases} \boldsymbol{x}^{dq} = \begin{bmatrix} X_d \\ X_q \end{bmatrix} = \begin{bmatrix} \sin(w_s t) & -\cos(w_s t) \\ \cos(w_s t) & \sin(w_s t) \end{bmatrix} \cdot \boldsymbol{x}^{\alpha\beta} \\ \boldsymbol{x}^{\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \boldsymbol{x}^{abc} \end{cases} \tag{3.2}$$

where R_g and L_g are line resistance and inductance respectively, w_s is the synchronous angular speed of the AC grid. $\boldsymbol{e}^{abc}$, $\boldsymbol{i}^{abc}$, and the GCI output voltage $\boldsymbol{v}^{abc} \in \mathbb{R}^{3x1}$ are transformed into the synchronous dq reference variables $\boldsymbol{e}^{dq} \in \mathbb{R}^{2x1}$, $\boldsymbol{i}^{dq} \in \mathbb{R}^{2x1}$, $\boldsymbol{v}^{dq} \in \mathbb{R}^{2x1}$, respectively, by (3.2). The GCI output voltage $\boldsymbol{v}^{abc}$ is given in the voltage vector space as

$$\boldsymbol{v}^{\mathrm{abc}} = V_{\mathrm{dc}} \cdot \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \boldsymbol{s}^{\mathrm{abc}} \tag{3.3}$$

where

$$\begin{aligned} &\boldsymbol{s}^{\mathrm{abc}} \in S := \\ &\{(000),(100),(110),(010),(011),(001),(101),(111)\} \end{aligned} \tag{3.4}$$

$\boldsymbol{s}^{abc}$ represents eight switching states of the two-level GCI. Equations (3.1)-(3.3) can be rewritten as a state-space system

$$\frac{d\boldsymbol{i}^{\mathrm{dq}}}{dt} = A\boldsymbol{i}^{\mathrm{dq}} + B\boldsymbol{u}^{\mathrm{dq}} \tag{3.5}$$

where

$$\boldsymbol{i}^{\mathrm{dq}} = [\, I_{\mathrm{d}} \;\; I_{\mathrm{q}} \,]^T, \; \boldsymbol{u}^{\mathrm{dq}} = [V_{\mathrm{d}} \;\; V_{\mathrm{q}} \;\; E_{\mathrm{d}} \;\; E_{\mathrm{q}}]^T \tag{3.6}$$

$$A = \begin{bmatrix} -\dfrac{R_{\mathrm{g}}}{L_{\mathrm{g}}} & w_{\mathrm{s}} \\ -w_{\mathrm{s}} & -\dfrac{R_{\mathrm{g}}}{L_{\mathrm{g}}} \end{bmatrix} \tag{3.7}$$

$$B = \begin{bmatrix} \dfrac{1}{L_{\mathrm{g}}} & 0 & -\dfrac{1}{L_{\mathrm{g}}} & 0 \\ 0 & \dfrac{1}{L_{\mathrm{g}}} & 0 & -\dfrac{1}{L_{\mathrm{g}}} \end{bmatrix} \tag{3.8}$$

The state variables in (3.5) are predicted by discrete Euler's forward formula in the receding horizon, which is described by the following equation:

$$\boldsymbol{i}^{\mathrm{dq}}[k+H] = \boldsymbol{i}^{\mathrm{dq}}[k] + T_{\mathrm{s}} \sum_{j=0}^{H-1} \frac{d\boldsymbol{i}^{\mathrm{dq}}[k+j]}{dt} \tag{3.9}$$

where H is the prediction receding horizon and T_{s} is the sampling period. In the most grid-connected applications, H is set to be one discrete time instant, because the fundamental frequency of the grid voltage is much smaller than the sampling frequency. One discrete time instant is sufficient to predict the state variables and requires the least online calculation from microprocessors.

The predicted values from (3.9) are transmitted to the second section, the problem formulation of FCS-MPC. The problem formulation consists of objective functions, input variables and constraints. Since the fundamental target of GCIs is to regulate the line current for the power flow control, the basic problem formulation is described as follows:

$$\min_{s^{abc}} \; J = \sum_{j=1}^{H} \| \boldsymbol{i}^{\mathrm{dq}*}[k] - \boldsymbol{i}^{\mathrm{dq}}[k+j] \|_2^2 \tag{3.10}$$

s.t.

$$\mathcal{C}_1 \colon \| \boldsymbol{v}^{\mathrm{dq}}[k+j] \|_2 \leq V_{\mathrm{dc}}/\sqrt{3} \quad \text{for} \;\; j = 1,\ldots, H \tag{3.11}$$

$$\mathcal{C}_2 \colon \| \boldsymbol{i}^{\mathrm{dq}}[k+j] \|_2 \leq I_{\max} \quad \text{for} \;\; j = 1,\ldots, H \tag{3.12}$$

where J and C denote the objective function and the constraint function, respectively, the input variable is $\boldsymbol{s}^{\mathrm{abc}}$ defined in (3.4) and $I_{\max}$ is the maximum continuous current from either the datasheet of the power module or designed power loading. In this chapter, a norm-2 ℓ_2 least square objective function is used in (3.10) due to its differentiability for the later mathematical derivation. Sometimes, the norm-1 ℓ_1 difference objective function can also be adopted. By specifying H at one discrete time instant, (3.10) is expressed as

$$J = \| \boldsymbol{i}^{\mathrm{dq}*}[k] - \boldsymbol{i}^{\mathrm{dq}}[k+1] \|_2^2 \tag{3.13}$$

Eventually, the basic problem formulation is fulfilled by combining (3.10)-(3.13). FCS-MPC selects the optimal switching state by minimizing the objective function (3.13). Since it is the objective function that determines the instantaneous output switching state and later the switching sequence, (3.13) is investigated in more depth. Equation (3.13) is expanded as

$$J = \left(I_{\mathrm{d}}^{*}[k] - I_{\mathrm{d}}[k+1]\right)^{2} + \left(I_{\mathrm{q}}^{*}[k] - I_{\mathrm{q}}[k+1]\right)^{2} \tag{3.14}$$

Then, the predicated state variables in (3.14) are replaced by (3.9) and (3.14) turns into

$$\begin{aligned} J = \quad & \left(I_{\mathrm{d}}^{*}[k] - I_{\mathrm{d}}[k] - T_{\mathrm{s}}\frac{dI_{\mathrm{d}}[k]}{dt}\right)^{2} \\ & + \left(I_{\mathrm{q}}^{*}[k] - I_{\mathrm{q}}[k] - T_{\mathrm{s}}\frac{dI_{\mathrm{q}}[k]}{dt}\right)^{2} \end{aligned} \tag{3.15}$$

Further, the expression of (3.15) can be expanded by using (3.1)

$$\begin{aligned} J = & \\ & \left(I_{\mathrm{d}}^{*}[k] - I_{\mathrm{d}}[k] - \frac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\left(V_{\mathrm{d}} - E_{\mathrm{d}} - R_{\mathrm{g}}I_{\mathrm{d}}[k] + w_{\mathrm{s}}L_{\mathrm{g}}I_{\mathrm{q}}[k]\right)\right)^{2} \\ & + \left(I_{\mathrm{q}}^{*}[k] - I_{\mathrm{q}}[k] - \frac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\left(V_{\mathrm{q}} - E_{\mathrm{q}} - R_{\mathrm{g}}I_{\mathrm{q}}[k] - w_{\mathrm{s}}L_{\mathrm{g}}I_{\mathrm{d}}[k]\right)\right)^{2} \end{aligned} \tag{3.16}$$

It is noted that (3.16) is a multi-variable function and vary with the selection of the switching state due to (3.3). Thus, in order to derive the minimum of (3.16), these equations below need hold,

$$\nabla J = \begin{bmatrix} \dfrac{dJ}{dV_{\mathrm{d}}} \\ \dfrac{dJ}{dV_{\mathrm{q}}} \end{bmatrix} = \vec{0} \tag{3.17}$$

and

$$\begin{cases} D = \dfrac{d^2J}{dV_{\mathrm{d}}^2} \cdot \dfrac{d^2J}{dV_{\mathrm{q}}^2} - \left(\dfrac{d^2J}{dV_{\mathrm{d}}dV_{\mathrm{q}}}\right)^2 > 0 \\ \dfrac{d^2J}{dV_{\mathrm{d}}^2} > 0, \ \dfrac{d^2J}{dV_{\mathrm{q}}^2} > 0 \end{cases} \tag{3.18}$$

Then, (3.17) and (3.18) are calculated and results are shown below,

$$\nabla J = -2\frac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\begin{bmatrix} I_{\mathrm{d}}^*[k] - I_{\mathrm{d}}[k] - \dfrac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\left(V_{\mathrm{d}} - E_{\mathrm{d}} - R_{\mathrm{g}}I_{\mathrm{d}}[k] + w_{\mathrm{s}}L_{\mathrm{g}}I_{\mathrm{q}}[k]\right) \\ I_{\mathrm{q}}^*[k] - I_{\mathrm{q}}[k] - \dfrac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\left(V_{\mathrm{q}} - E_{\mathrm{q}} - R_{\mathrm{g}}I_{\mathrm{q}}[k] - w_{\mathrm{s}}L_{\mathrm{g}}I_{\mathrm{d}}[k]\right) \end{bmatrix} \tag{3.19}$$

and

$$\begin{cases} D = 4\left(\dfrac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\right)^4 \\ \dfrac{d^2J}{dV_{\mathrm{d}}^2} = 2\left(\dfrac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\right)^2, \ \dfrac{d^2J}{dV_{\mathrm{q}}^2} = 2\left(\dfrac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\right)^2 \end{cases} \tag{3.20}$$

Equation (3.20) shows itself permanently greater than zero by positive T_{s} and L_{g}, whereas any $\boldsymbol{v}^{\mathrm{dq}} = [V_{\mathrm{d}},\ V_{\mathrm{q}}]^{\mathrm{T}}$ leading to a zero-vector equality of (3.19) will perform an absolute minimum of (3.16). Its switching state becomes the optimum. However, in FCS-MPC, the feasible inputs $\boldsymbol{v}^{\mathrm{dq}}$ are discrete and finite, shown in (3.3)-(3.4). Equation (3.19) may not receive a zero-vector equality ever. In this case, any input $\boldsymbol{v}^{\mathrm{dq}}$ which drives (3.19) closer to the zero vector will perform a local minimum of this objective function because of the permanently positive results from (3.20). Then, (3.17) can be rewritten into the following for the minimum of the objective function (3.16),

$$\min_{\boldsymbol{v}^{dq}} \left\| \nabla J - \vec{0} \right\|_2 \tag{3.21}$$

In addition, in the system steady state, the instantaneous current $\boldsymbol{i}^{\mathrm{dq}}[k]$ is very close to its reference $\boldsymbol{i}^{\mathrm{dq}*}[k]$, which can be approximated to be identical for the ideal case,

$$\boldsymbol{i}^{\mathrm{dq}}[k] = \boldsymbol{i}^{\mathrm{dq}*}[k] \tag{3.22}$$

Then, (3.19) can be simplified into the following,

$$\nabla J = -2\frac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\begin{bmatrix} -\frac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\left(V_{\mathrm{d}} - E_{\mathrm{d}} - R_{\mathrm{g}} I_{\mathrm{d}}^{*}[k] + w_{\mathrm{s}} L_{\mathrm{g}} I_{\mathrm{q}}^{*}[k]\right) \\ -\frac{T_{\mathrm{s}}}{L_{\mathrm{g}}}\left(V_{\mathrm{q}} - E_{\mathrm{q}} - R_{\mathrm{g}} I_{\mathrm{q}}^{*}[k] - w_{\mathrm{s}} L_{\mathrm{g}} I_{\mathrm{d}}^{*}[k]\right) \end{bmatrix} \tag{3.23}$$

Combining (3.21) and (3.23) together, the optimal solution of the objective function (3.16) can also be derived through solving the following optimization problem. Their optimal solutions are equivalent through (3.17)-(3.23), even though their optimal values are not the same.

$$\min_{\boldsymbol{v}^{\mathrm{dq}}} \left\| 2\left(\frac{T_s}{L_g}\right)^2 \begin{bmatrix} (V_{\mathrm{d}} - V_{\mathrm{d}}^{*}[k]) \\ (V_{\mathrm{q}} - V_{\mathrm{q}}^{*}[k]) \end{bmatrix} - \vec{0} \right\|_2 \tag{3.24}$$

where

$$\begin{cases} V_{\mathrm{d}}^{*}[k] = E_{\mathrm{d}} + R_{\mathrm{g}} I_{\mathrm{d}}^{*}[k] - w_{\mathrm{s}} L_{\mathrm{g}} I_{\mathrm{q}}^{*}[k] \\ V_{\mathrm{q}}^{*}[k] = E_{\mathrm{q}} + R_{\mathrm{g}} I_{\mathrm{q}}^{*}[k] + w_{\mathrm{s}} L_{\mathrm{g}} I_{\mathrm{d}}^{*}[k] \end{cases} \tag{3.25}$$

$\boldsymbol{v}^{\mathrm{dq}*} = [V_{\mathrm{d}}^{*},\ V_{\mathrm{q}}^{*}]^{\mathrm{T}} \in \mathbb{R}^{2\mathrm{x}1}$ represents the converter output voltage reference from the command. At this point, it is observed that finding a local minimum of this objective function is equivalent to seek for an input $\boldsymbol{v}^{\mathrm{dq}}$ that leads to a minimized distance between this input $\boldsymbol{v}^{\mathrm{dq}}$ and the reference $\boldsymbol{v}^{\mathrm{dq}*}$. Then, the switching state of this input becomes the optimum. With multiple iterations of FCS-MPC, the switching sequence will be formed, and the switching frequency will be determined by this algorithm.

3.1.2 Ideal Case of Switching State Selection

Figure 3.2 shows a zoom-in area of the voltage vector space for the two-level power converter. It contains the stationary *abc* reference frame, the rotating *dq* reference frame

and three random output voltage references $\boldsymbol{V}_1^*:=\boldsymbol{v}_1^{dq*}$, $\boldsymbol{V}_2^*:=\boldsymbol{v}_2^{dq*}$, $\boldsymbol{V}_3^*:=\boldsymbol{v}_3^{dq*}$. All three references rotate at the angular speed w_s and are located temporarily in the Sector VI which is the region *OAB* constituted by voltage vectors of non-zero switching states $\boldsymbol{s}_1^{abc}=(1,0,0)$, $\boldsymbol{s}_6^{abc}=(1,0,1)$ and the voltage limit curve $V_{dc}/\sqrt{3}$.

As mentioned above, the optimal switching state is the one of which the voltage vector has the minimized distance to the output voltage reference. Based on this discovery, the region *OAB* is further divided into three quadrilateral subareas, *OXUY*, *AZUX*, *BYUZ*, which are partitioned by any point in this subarea having the shortest distance to the voltage vector of $\boldsymbol{s}_{0/7}^{abc}$, $\boldsymbol{s}_1^{abc}$, and $\boldsymbol{s}_6^{abc}$, respectively. *X* and *Y* are middle points of voltage vectors of $\boldsymbol{s}_1^{abc}$ and $\boldsymbol{s}_6^{abc}$. *Z* is the middle point of curve *AB*. The distance between *O* and *X* or *O* and *Y* is $V_{dc}/3$. *U* is the center of the inscribed circle of Sector VI. The distance between *O* and

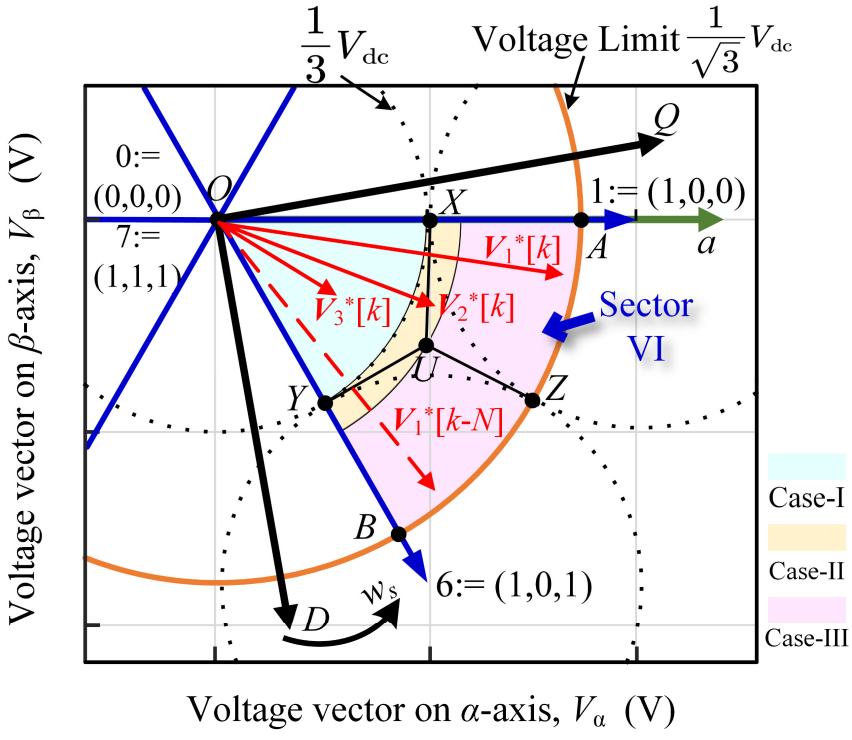


Figure 3.2: Schematic diagram of ideal case switching sequence in Sector VI on the voltage vector space

U is $2V_{dc}/3\sqrt{3}$. It is illustrated graphically that the optimal switching state will be $\boldsymbol{s}_{0/7}^{abc}$, $\boldsymbol{s}_1^{abc}$, and $\boldsymbol{s}_6^{abc}$ for any output voltage reference located at *OXUY*, *AZUX*, and *BYUZ*, respectively. Hence, for references $\boldsymbol{V}_1^*$, $\boldsymbol{V}_2^*$, and $\boldsymbol{V}_3^*$ shown in Figure 3.2, selected optimal switching states by FCS-MPC will be $\boldsymbol{s}_1^{abc}$, $\boldsymbol{s}_1^{abc}$ and $\boldsymbol{s}_{0/7}^{abc}$, respectively.

Furthermore, all these output voltage references are not stationary but rotating at w_s. For example, $\boldsymbol{V}_1^*[k\text{-}N]$ which is $\boldsymbol{V}_1^*$ in N discrete time instants earlier will have an optimal switching state at $\boldsymbol{s}_6^{abc}$ since $\boldsymbol{V}_1^*[k\text{-}N]$ was in *BYUZ* at that time instead of *AZUX* as shown in Figure 3.2. However, for $\boldsymbol{V}_3^*$, its distance to the voltage vector of zero switching state is always the shortest regardless of the angle it rotates. Thus, the optimal switching state of it remains zero switching state $\boldsymbol{s}_{0/7}^{abc}$. It is quite complicated for $\boldsymbol{V}_2^*$ as $\boldsymbol{V}_2^*$ has a magnitude greater than $V_{dc}/3$ and smaller than $2V_{dc}/3\sqrt{3}$. Hence, it locates at *BYUZ*, *OXUY* and *AZUX* in succession, which gives the optimal switching state in a sequence of $\boldsymbol{s}_6^{abc}$, $\boldsymbol{s}_{0/7}^{abc}$, and $\boldsymbol{s}_1^{abc}$.

3.1.3 Ideal Case of Switching Sequence Formulation

Therefore, with the output voltage reference rotating, ideally the sequence of the optimal switching state will be below,

For Case-I, $||\boldsymbol{V}^*||_2 <= V_{dc}/3$,

$$\rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow\ldots\rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow\ldots\rightarrow$$

For Case-II, $||\boldsymbol{V}^*||_2 > V_{dc}/3$ and $||\boldsymbol{V}^*||_2 < 2V_{dc}/3\sqrt{3}$,

$$\rightarrow \boldsymbol{s}_6^{abc} \rightarrow\ldots\rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow\ldots\rightarrow \boldsymbol{s}_1^{abc} \rightarrow\ldots\rightarrow$$

For Case-III, $||\boldsymbol{V}^*||_2 >= 2V_{dc}/3\sqrt{3}$,

$$\rightarrow \boldsymbol{s}_6^{abc} \rightarrow\ldots\rightarrow\boldsymbol{s}_1^{abc} \rightarrow\ldots\rightarrow$$

where … represents repeating the previous switching state. According to above different switching sequences, it is noted that Case-II would have the largest switching frequency since it contains the most transitions between switching states. Case-I would have the smallest switching frequency since it can be controlled to have a sequence with either all $\boldsymbol{s}_0^{abc}$ or all $\boldsymbol{s}_7^{abc}$. Case-III would have a sequence with only non-zero switching states.

3.1.4 Nonideal Case of Switching State Selection

Then, the nonideal case is expected to be analyzed, where the assumption made for (3.22) does not always hold. In the real system, there is an instantaneous current error between the current $\boldsymbol{i}^{dq}[k]$ and its reference value $\boldsymbol{i}^{dq^*}[k]$. This is simple to understand because the selected optimal switching state from (3.24), even if it has the minimized distance to the output voltage reference, does not lead to a zero-vector equality in (3.17) and would result in a voltage vector error and thereby the instantaneous current error. A more sophisticated equation of (3.24) can be written by involving this error,

$$\min_{\boldsymbol{v}^{dq}} \left\| 2\left(\frac{T_s}{L_g}\right)^2 \begin{bmatrix} \left(V_d - \left(V_d^*[k] + \sum_{j=0}^{N} V_d^C[k-j]\right)\right) \\ \left(V_q - \left(V_q^*[k] + \sum_{j=0}^{N} V_q^C[k-j]\right)\right) \end{bmatrix} - \vec{0} \right\|_2 \tag{3.26}$$

where $\boldsymbol{V}^C := \boldsymbol{v}^{dqC} = [V_d^C,\ V_q^C]^T \in \mathbb{R}^{2x1}$ is the output voltage compensation in order to compensate the instantaneous current error from previous time instants. With the error aggregates, $\boldsymbol{V}^C$ would take up more weightings in the vector addition of $\boldsymbol{V}^C$ and $\boldsymbol{V}^{dq^*}$, and eventually lead the vector sum to another quadrilateral subarea. For example, as shown in Figure 3.3, $\boldsymbol{V}_1^C$ and $\boldsymbol{V}_3^C$ are indicated and determined by the vector subtraction between the voltage reference $\boldsymbol{V}^*$ and the output voltage $\boldsymbol{V}$ of previous optimal switching state $\boldsymbol{s}_1^{abc}$ and $\boldsymbol{s}_{0/7}^{abc}$, respectively. At this point, the optimal switching state of $\boldsymbol{V}_1$ is still $\boldsymbol{s}_1^{abc}$ since the

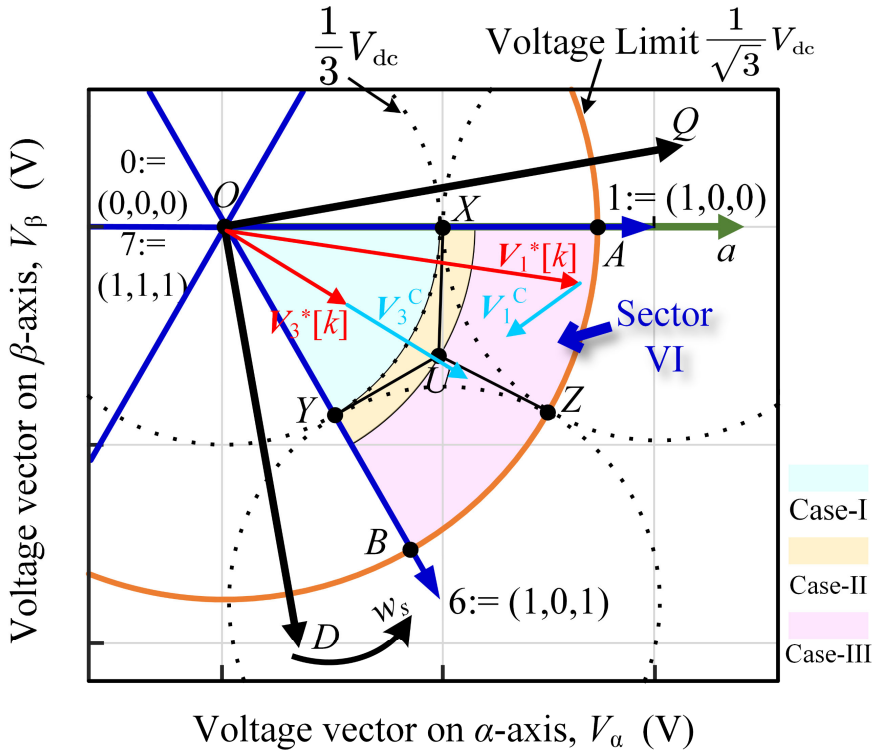


Figure 3.3: Schematic diagram of the nonideal case switching sequence in Sector VI on the voltage vector space.

vector sum of $\boldsymbol{V}_1^*$ and $\boldsymbol{V}_1^C$ is still in *AZUX*. However, this vector sum is inclined to slide into the different subarea. For $\boldsymbol{V}_3$, the optimal switching state changes to $\boldsymbol{s}_6^{abc}$ as the new location of the vector sum is in *BYUZ* instead of *OXUY*.

3.1.5 Nonideal Case of Switching Sequence Formulation

Extending this nonideal analysis into all three cases, the switching sequence will be updated into the following,

For Case-I, $||\boldsymbol{V}^*||_2 <= V_{dc}/3$,

$$\rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow \ldots \rightarrow \boldsymbol{s}_{1/6}^{abc} \rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow \ldots \rightarrow \boldsymbol{s}_{1/6}^{abc} \rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow \ldots \rightarrow$$

For Case-II, $||\boldsymbol{V}^*||_2 > V_{dc}/3$ and $||\boldsymbol{V}^*||_2 < 2V_{dc}/3\sqrt{3}$,

$$\rightarrow \boldsymbol{s}_6^{abc} \rightarrow \ldots \rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow \boldsymbol{s}_6^{abc} \rightarrow \ldots \rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow \ldots \rightarrow \boldsymbol{s}_{1/6}^{abc} \rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow \ldots \rightarrow \boldsymbol{s}_1^{abc} \rightarrow \ldots \rightarrow$$

$$\boldsymbol{s}_{0/7}^{abc} \rightarrow \boldsymbol{s}_1^{abc} \rightarrow \ldots \rightarrow$$

For Case-III, $\|\boldsymbol{V}^*\|_2 >= 2V_{dc}/3\sqrt{3}$,

$$\rightarrow \boldsymbol{s}_6^{abc} \rightarrow \ldots \rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow \boldsymbol{s}_6^{abc} \rightarrow \ldots \rightarrow \boldsymbol{s}_{0/7}^{abc} \rightarrow \boldsymbol{s}_1^{abc} \rightarrow \ldots \rightarrow$$

It is noted that switching frequencies for all cases increase due to more transitions existing in the updated switching sequences. For instance, Case-I has a positive switching frequency this time because of the error compensation from non-zero switching states, which accords with the real system. At this moment, it is difficult to explicitly find that which case has the largest switching frequency. Fortunately, the switching frequency variation within each case is observed and elaborated below.

In Case-I, an output voltage reference $\boldsymbol{V}^*$ with a smaller magnitude would contribute to a smaller voltage vector error and need more aggregations to drive the vector sum of $\boldsymbol{V}^*$ and $\boldsymbol{V}^C$ slide into the different subarea. This results in fewer transitions from non-zero switching states for the compensation. Then, its switching frequency will be less than the one with a larger magnitude of $\boldsymbol{V}^*$. The maximum switching frequency happens when $\boldsymbol{V}^*$ is located at the boundary of Case I which is $V_{dc}/3$. On the contrary, in Case-III, the switching frequency will gradually increase while the magnitude of $\boldsymbol{V}^*$ decreases. The similar analysis can be applied here. The maximum switching frequency happens when $\boldsymbol{V}^*$ is located at the boundary of Case-III which is $2V_{dc}/3\sqrt{3}$.

In Case-II, even though transitions are more complicated than other two cases, it still can be inferred that the switching frequency will gradually increase while the magnitude of the output voltage reference $\boldsymbol{V}^*$ decreases, similar with the Case-III. This is because $\boldsymbol{V}^*$ with a smaller magnitude in Case-II would contain a longer curve located in

OXUY. A longer curve in *OXUY* could trigger more compensations from non-zero switching states like what happens in Case-I. Compensations from non-zero switching states may result in two switching events for one compensation, such as two events for $\boldsymbol{s}_0^{abc} := [0,0,0]^T \rightarrow \boldsymbol{s}_6^{abc} := [1,0,1]^T$. However, conversely compensations from zero switching states like what happens in Case-III can guarantee that at most one switching event exists in one transition, such as only one event for $\boldsymbol{s}_6^{abc} := [1,0,1]^T \rightarrow \boldsymbol{s}_7^{abc} := [1,1,1]^T$. Hence, $\boldsymbol{V}^*$ which occupies a longer curve in *OXUY* will generate more switching events due to compensations from non-zero switching states, eventually have a larger switching frequency. The maximum switching frequency happens when $\boldsymbol{V}^*$ is located at the boundary of Case-II which is $V_{dc}/3$.

Combining the switching frequency variation in all three cases, it is illustrated that the maximum switching frequency of this basic problem formulation happens when $\boldsymbol{V}^*$ has a magnitude around $V_{dc}/3$ and the switching frequency decreases in both directions that the magnitude of $\boldsymbol{V}^*$ increases or decreases away from $V_{dc}/3$. On the other hand, the phase of $\boldsymbol{V}^*$ would not affect the switching frequency variation since $\boldsymbol{V}^*$ is a rotating vector at the constant speed w_s and it will sweep full degrees in the *abc* reference frame, which is always true in regardless of the phase. Hence, the phase of $\boldsymbol{V}^*$ would not affect the proposed switching sequence by geometry analysis and further the switching frequency.

3.1.6 Summary of Variable Switching Frequency Property

To put everything in a nutshell, principles of the variable switching frequency property of FCS-MPC can be summarized in the following,

1) The optimal switching state can be decided by selecting the switching state of which the voltage vector has the minimized distance to the output voltage reference, if the instantaneous current is assumed to be the same as its reference.
2) In the real situation, where there is an instantaneous current error, the optimal switching state can be decided by selecting the switching state of which the voltage vector has the minimized distance to the vector addition of the voltage reference and the voltage compensation.
3) The maximum switching frequency happens when the output voltage reference $\boldsymbol{V}^*$ has a magnitude around $V_{dc}/3$.
4) The switching frequency decreases in both directions that the magnitude of $\boldsymbol{V}^*$ increases or decreases away from $V_{dc}/3$.
5) The phase of $\boldsymbol{V}^*$ would not affect the switching frequency variation due to the voltage vector rotation.

The quantization of the switching frequency in FCS-MPC is complex and out of scope of this chapter. The above proposed principles are significant enough to comprehend the control algorithms of FCS-MPC and provide engineers with more insights to take full advantages of FCS-MPC in the power electronics applications.

3.2 Feasible Operation Region of Power Converters

In this section, the relationship between the switching frequency variation and the steady state of the GCI is analyzed. As inferred in Chapter 3.1, the switching frequency is the largest when the converter output voltage reference $\boldsymbol{V}^*$ has a magnitude around $V_{dc}/3$ and decreases in both directions that the magnitude of $\boldsymbol{V}^*$ increases or decreases away from $V_{dc}/3$. The $\boldsymbol{V}^*$ is generated by $\boldsymbol{i}^{dq*}$ in (3.25), which is actually determined by steady states

of the power converter under the power flow control as shown in Figure 3.1. In this case, if all feasible steady states of the power converter are collected, the converter output voltage reference $\boldsymbol{V}^*$ can be estimated by (3.25) and then the switching frequency variation can be illustrated for the FCS-MPC regulated power converter. Then, the first task is to identify all feasible steady states of the power converter. This is exactly the feasible operation range of the power converter in either the voltage vector space or the power vector space. Each operating point in this range is one potential steady state of the power converter.

In this section, a one-mega-volt-ampere (1-MVA) grid-connected inverter is introduced from the reference model of the ocean current energy converter (OCEC) system as a description example [40]. The system parameters of this GCI are listed in Table 3.1. Six ABB HiPak 5SND 0800M170100 IGBT modules are used for this two-level three-

TABLE 3.1

PARAMETERS OF THE GCI IN THE REFERENCE OCEC SYSTEM

Rated power S	1 MVA/ 1 p.u.
Rated DC bus voltage V_{dc}	1200 V
Grid frequency f	60 Hz
Rated AC grid voltage $\boldsymbol{e}^{abc}$	277/480 V
Line inductance L_g	1 mH
Line resistance R_g	10 mΩ
IGBT module	ABB HiPak 5SND0800M170100 [41]
Junction temperature T_j	-40~125 ºC, Max 150 ºC
Air temperature T_{air}	25 ºC
50% current loading	565.5 A
100% current loading	1131.4 A
Rated (106%) current loading	1203.4 A

phase topology as shown in Figure 3.1 and each module has two paralleled same-polarity IGBT devices with diodes to increase current loadings.

3.2.1 Feasible Operation Region on Voltage Vector Space

First, the feasible operation region in the voltage vector space (FOV) of this GCI is identified. Figure 3.4 presents the complete voltage vector space for the two-level power converter. Both *abc* stationary and *dq* rotating reference frames are shown in Figure 3.4. Voltage vectors of eight switching states from (3.3) and (3.4) are displayed in blue. The voltage limit curve is calculated by (3.11) and specified in the following,

$$\sqrt{V_{\mathrm{d}}^2 + V_{\mathrm{q}}^2} \leqslant V_{\mathrm{dc}}/\sqrt{3} \tag{3.27}$$

The current limit curve is derived by mapping (3.12) into the voltage vector space,

$$\sqrt{I_{\mathrm{d}}^2 + I_{\mathrm{q}}^2} \leqslant I_{\mathrm{limit}} \tag{3.28}$$

Then,

$$\frac{(V_{\mathrm{d}} - E_{\mathrm{d}})^2}{(w_{\mathrm{s}} L_{\mathrm{g}} I_{\mathrm{limit}})^2} + \frac{(V_{\mathrm{q}} - E_{\mathrm{q}})^2}{(w_{\mathrm{s}} L_{\mathrm{g}} I_{\mathrm{limit}})^2} \leqslant 1 \tag{3.29}$$

Details of derivation are in Appendix A. I_{limit} could be either the maximum continuous conduction current of the semiconductor device or the power derating limit. In the example, since it is a 1-MVA system, I_{limit} is 106% current loading of the maximum continuous conduction current of the IGBT module. This value is defined case by case.

The intersection of interior areas of voltage and current limits (3.27) and (3.29) is the feasible operation region of this GCI in the voltage vector space, which is indicated in shadow in Figure 3.4. Conventionally, the DC bus voltage is regulated at a constant value for the enough voltage utilization, where the voltage limit curve is usually stable. By different current loading limits, the intersection varies. 50% derating, 100% full loading

and 106% overloading current limits are all shown in Figure 3.4 in green, which illustrates different feasible operation ranges. The $V_{dc}/3$ curve is shown in the dash line in Figure 3.4

$$\sqrt{V_d^2 + V_q^2} \leqslant V_{dc}/3 \tag{3.30}$$

Any operating point in the shadow is one potential steady state of this GCI. Any operating point located around the $V_{dc}/3$ curve (3.30) will have a larger switching frequency by FCS-MPC and the switching frequency decreases with the operating point moving away from this curve.

3.2.2 Feasible Operation Region on Power Vector Space

Figure 3.4 straightforward shows the relationship between the steady state of the power converter and the switching frequency variation of FCS-MPC in FOV. However, it is not convenient to clarify the relationship from the power perspective which is mostly used to describe a power electronics system. Then, FOV is mapped into the power vector space (FOP) in Figure 3.5.

The voltage limit, the current limit, and the $V_{dc}/3$ curve are all derived in the power vector space respectively as follows,

$$\frac{\left(P^* - \frac{3E_d E_q}{2w_s L_g}\right)^2}{\left(\frac{\sqrt{3}V_{dc}E_q}{2w_s L_g}\right)^2} + \frac{\left(Q^* + \frac{3E_q E_q}{2w_s L_g}\right)^2}{\left(\frac{\sqrt{3}V_{dc}E_q}{2w_s L_g}\right)^2} \leqslant 1 \tag{3.31}$$

$$\frac{(P^*)^2}{\left(\frac{3}{2}E_q I_{max}\right)^2} + \frac{(Q^*)^2}{\left(\frac{3}{2}E_q I_{max}\right)^2} \leqslant 1 \tag{3.32}$$

$$\frac{\left(P^* - \frac{3E_d E_q}{2w_s L_g}\right)^2}{\left(\frac{V_{dc}E_q}{2w_s L_g}\right)^2} + \frac{\left(Q^* + \frac{3E_q E_q}{2w_s L_g}\right)^2}{\left(\frac{V_{dc}E_q}{2w_s L_g}\right)^2} \leqslant 1 \tag{3.33}$$

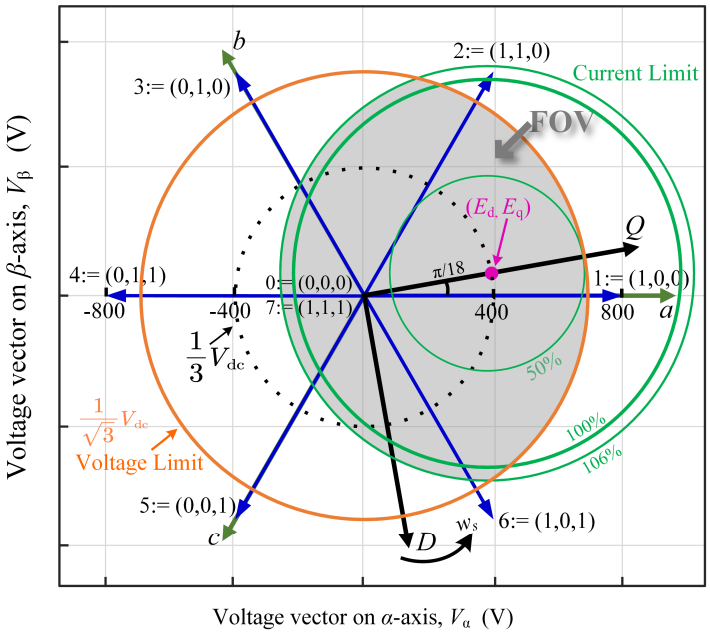


Figure 3.4: Feasible operation region of GCI on the voltage vector space.

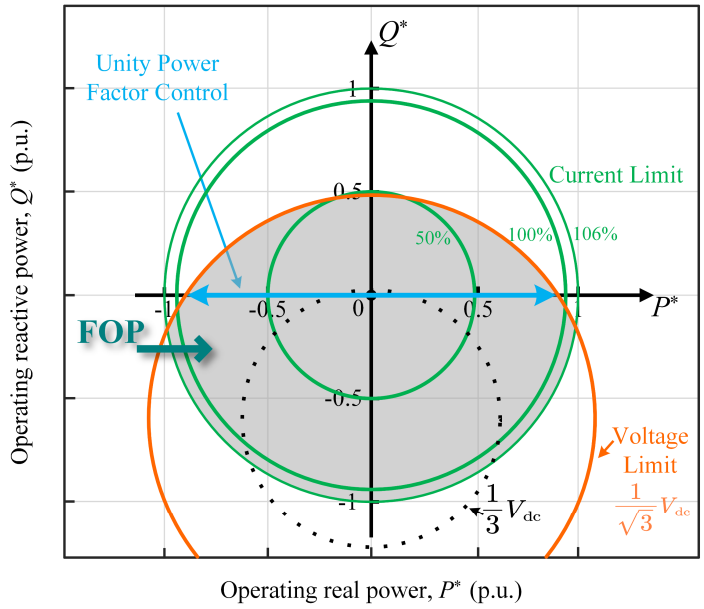


Figure 3.5: Feasible operation region of GCI on the power vector space.

where P^* and Q^* stand for the references of the real and reactive power respectively. Detail of derivation is in Appendix B. Figure 3.5 shows the power vector space. The intersection of interior areas of voltage and current limits is FOP of this GCI, which is also indicated in shadow in Figure 3.5. Any operating point in the shadow is one potential steady state. By commanding different P^* and Q^* to this GCI, the steady state will be different. Similar with FOV, any operating point located around the $V_{dc}/3$ curve (3.30) will have a larger switching frequency by FCS-MPC and the switching frequency decreases with the operating point away from this curve.

The most conventional power flow control is the unity power factor control (UPFC) shown in blue in Figure 3.5. The FCS-MPC controlled GCI will receive different switching frequencies along this control trajectory because of different distances from the operating point to the $V_{dc}/3$ curve. It is also observed that by injecting an amount of the reactive power, the switching frequency will be autonomously adjusted since the operating point is moving closer to or further away from the $V_{dc}/3$ curve. The following sections will verify this variable switching frequency property of FCS-MPC and its relationships with steady states in FOV and FOP. The impact of this property on the GCI will also be investigated.

3.3 Results Validations

3.3.1 Simulation Results

To verify the variable switching frequency property of FCS-MPC and other discoveries discussed above, PLECS and MATLAB/Simulink are used to simulate the sample 1-MVA GCI, considering the system diagram in Figure 3.1. FCS-MPC with only the basic problem formulation (3.10)-(3.13) is calibrated on the local controller. The

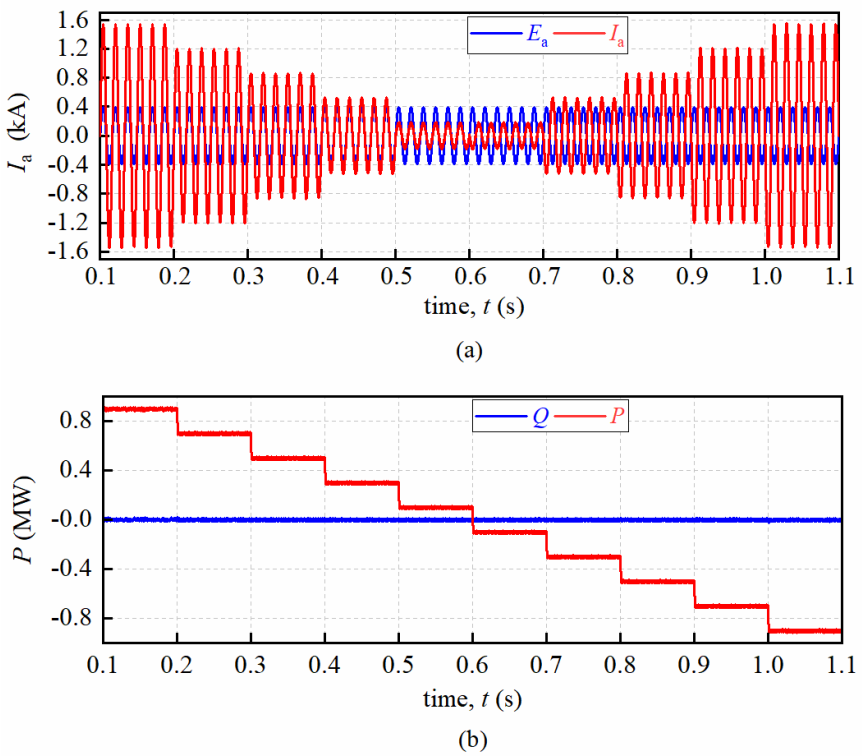


Figure 3.6: Simulation results of the unity power factor control by FCS-MPC including (a) the phase current and (b) the instantaneous power.

TABLE 3.2

PARAMETERS OF THE FCS-MPC WITH BASIC PROBLEM FORMULATION

Prediction receding horizon H	1
Sampling period T_s	50 μs

parameters are set and listed in Table 3.2. FOV and FOP of this simulated GCI are strictly stick with Figure 3.4 and 3.5.

Figure 3.6 presents results under UPFC, where grid voltage and current are shown in Figure 3.6(a) and corresponding real and reactive power are shown in Figure 3.6(b). The reactive power is regulated to be zero and the real power is controlled ranging from 0.9 p.u. to -0.9 p.u., which is following the UPFC trajectory in Figure 3.5. When the real power is positive, the GCI is in the inverter mode and injects power into the grid. When the real

power is negative, the GCI is in the rectifier mode and absorbs power from the grid. The latter is likely to happen when DER systems contain the local energy storage systems or loads. The grid voltage and current are presented in phase and 180° out of phase in the inverter and rectifier mode, respectively, as shown in Figure 3.6(a).

Figure 3.7 shows the output switching states by FCS-MPC from UPFC results in Figure 3.6. Some of steady states in Case-I (0.1, -0.1 MW), -II (0.3, -0.3 MW), and -III (0.9, -0.9 MW) are presents. It is noted that with the operating point moving towards the $V_{dc}/3$ curve as shown in Figure 3.5, switching transitions become more frequently, including transitions between the non-zero switching state and the non-zero switching state or the non-zero switching state and the zero switching state. Since operating points in Case-I are slightly closer to the $V_{dc}/3$ curve than ones in Case-II, switching transitions appear a little bit more from Figure 3.7(b)-(e). Besides, switching sequences of the symmetric operating points in FOP show similar, such as 0.9 MW and -0.9 MW, even though they have different phases of $\boldsymbol{V}^*$ in FOV.

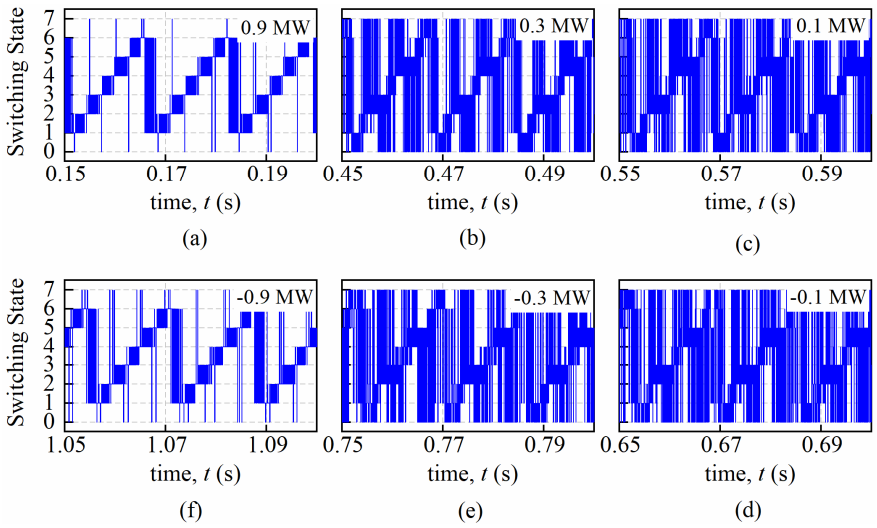


Figure 3.7: Output switching states selected by FCS-MPC along the UPFC

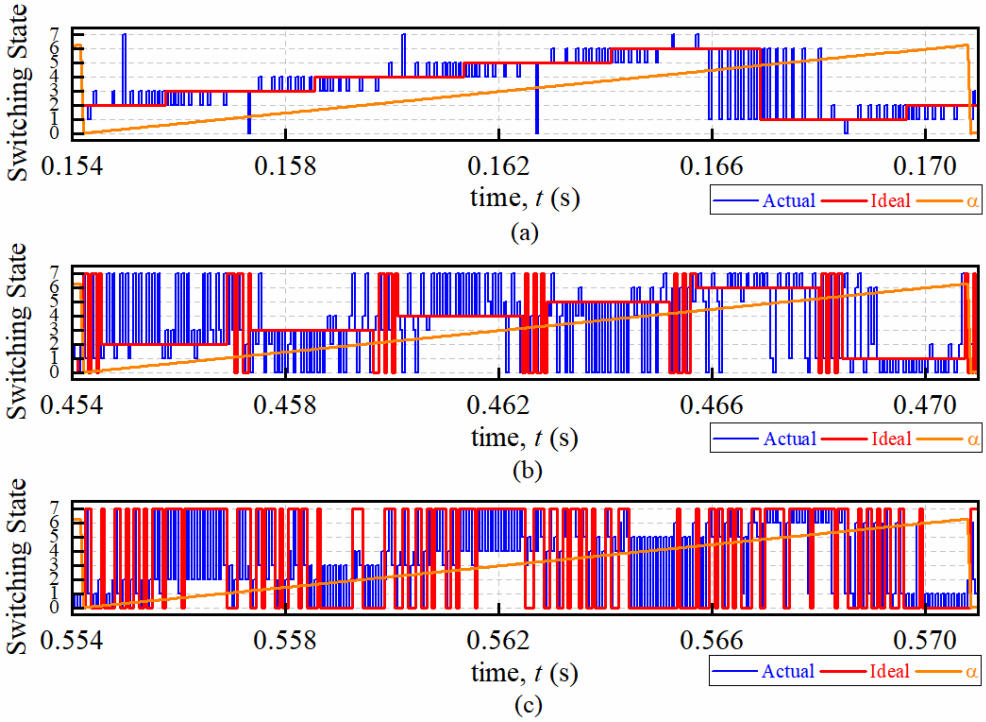


Figure 3.8: One fundamental period window of the output switching state by FCS-MPC (blue), the ideal switching sequence by geometry analysis (red), and the rotating angle α of *dq* reference frame (yellow) including (a) 0.9 MW, (b) 0.3 MW, and (c) 0.1 MW

Figure 3.8 shows the zoom-in observations of Figure 3.7 over one fundamental period. α is defined as the rotating angle between *dq* and *abc* reference frames. α is π/18 rad in Figure 3.4 for instance. Ideal output switching states selected through (3.24) and (3.25) are presented in addition to the actual output switching states by FCS-MPC. It is found that results of ideal cases strictly obey proposed switching sequences in Chapter 3.1 that Case-I only contains zero switching states $\boldsymbol{s}_{0/7}^{abc}$, Case-II contains non-zero switching states $\boldsymbol{s}_{0\text{-}6}^{abc}$ and zero switching states $\boldsymbol{s}_{0/7}^{abc}$, and Case-III only contains non-zero switching states $\boldsymbol{s}_{0\text{-}6}^{abc}$. Then, nonideal cases which are actual results in Figure 3.8 follow outlines of ideal cases, but with more transitions due to the aggregated current error and the output voltage compensation as discussed in Chapter 3.1. In Figure 3.8(a), transitions happen least, and most are between non-zero switching states $\boldsymbol{s}_{0\text{-}6}^{abc}$ because this operating point is

located in Case-III near the boundary of the feasible operation region. In Figure 3.8(b), where the operating point is located in Case-II, the baseline of the switching sequence follows the outline of the ideal case and transitions happen more from the zero switching states $\boldsymbol{s}_{0/7}^{abc}$ due to the voltage compensation from the zero voltage vector. On the contrary, in Figure 3.8(c), transitions happen more from the non-zero switching states $\boldsymbol{s}_{0\text{-}6}^{abc}$ based on the outline of the zero switching states in Case-I. These results in Figure 3.8 effectively justify the proposed switching sequences by geometry analysis for both ideal and nonideal cases in Chapter 3.1.

Then, the switching frequency f_{SW} is calculated by counting the average number of switching events over one second. Switching frequencies of this GCI under UPFC by FCM-MPC are presented in Figure 3.9, which gives an explicit vision on the variable switching frequency property of FCS-MPC. The switching frequency ranges from 2 kHz to 4 kHz, where the minimum value happens when this GCI operates at the boundary of

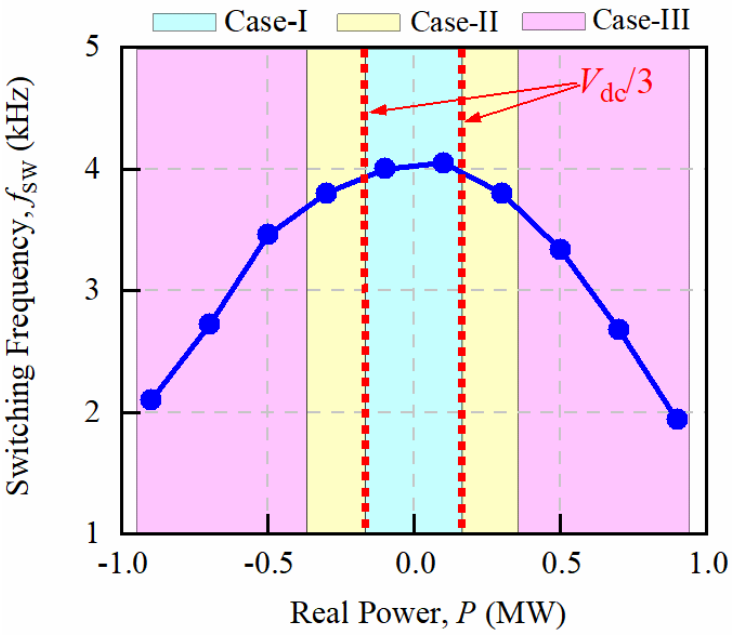
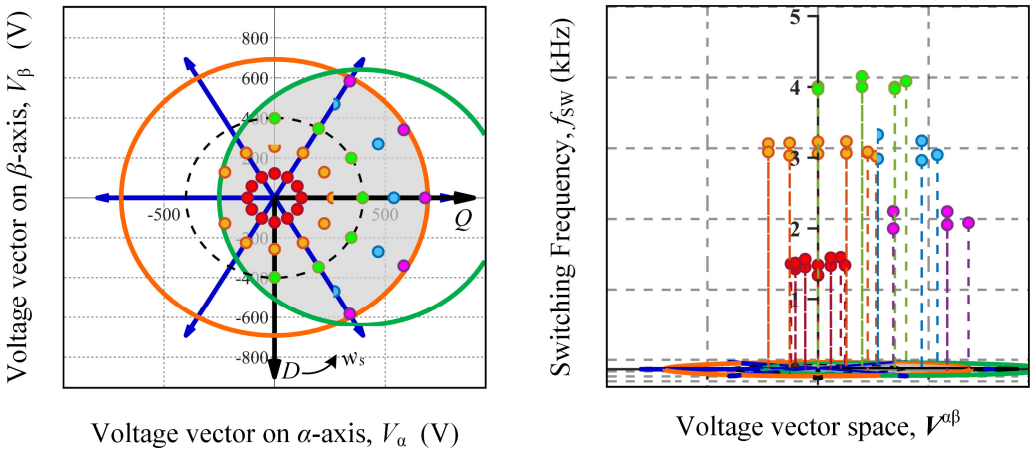


Figure 3.9: Switching frequency by FCS-MPC on the UPFC trajectory

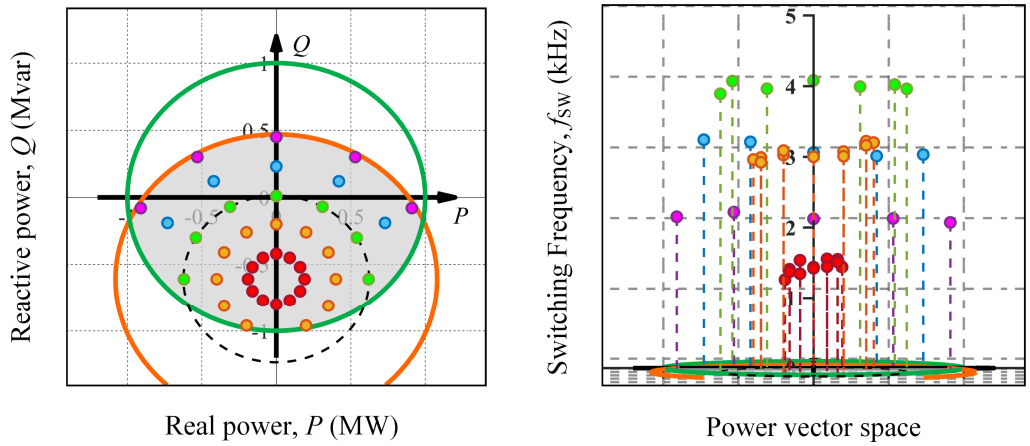
the feasible operation region at +/-0.9 MW, and the maximum value happens around the at $V_{dc}/3$ curve +/- 0.1 MW. It is illustrated that the switching frequency increases with the decrease of the real power since, from FOP in Figure 3.5, a smaller loading on the UPFC trajectory results in a smaller output voltage refence magnitude and a closer distance to the $V_{dc}/3$ curve. The switching frequency variation in Case-I is not clear in Figure 3.9 due to a very tiny overlap between the UPFC trajectory and the Case-I region in Figure 3.5, which will be presented later in results off the UPFC trajectory. It is also observed that the symmetric operating points from FOP have almost the same switching frequency in Figure 3.9 because of the same output voltage magnitude, which also indicates that the switching frequency is independent of the output voltage phase.

More results of the switching frequency for steady states off the UPFC trajectory are presented and mapped on FOV and FOP in Figure 3.10 and 3.11, respectively. Several output voltage references $\boldsymbol{V}^*$ with different magnitudes are tested, including $0.577V_{dc}$, $0.455V_{dc}$, $0.333V_{dc}$, $0.211V_{dc}$, and $0.089V_{dc}$. Figure 3.10(a) shows loci of operating points on the FOV, which are grouped by same output voltage magnitude. Due to the limited feasible operation region of this GCI, the output voltage reference with a larger magnitude results in a narrower phase range, which gives fewer testing samples. However, it is still clear to find in Figure 3.10(b) that with the same magnitude of the output voltage reference, switching frequencies of different steady states are in the same level and are independent of the output voltage phase. In addition, the switching frequency is verified to be maximum at 4 kHz around the $V_{dc}/3$ curve, which is the group of the $0.333V_{dc}$ and decreases with the magnitude increasing in Case-II and -III, which are groups of $0.455V_{dc}$, and $0.577V_{dc}$, with the magnitude decreasing in Case-I, which are groups of $0.211V_{dc}$, and $0.089V_{dc}$. Figure 3.



(a) (b)

Figure 3.10: Operating points on the FOV and corresponding switching frequencies by FCS-MPC.



(a) (b)

Figure 3.11: Operating points on the FOP and corresponding switching frequencies by FCS-MPC.

11 reflects the results in FOP and illustrates the relationship between the variable switching frequency of FCS-MPC and the steady state of the GCI.

Then, the impact of the variable switching frequency on the power loss of semiconductor devices of this GCI is illustrated in Figure 3.12 and 3.13. The temperature dissipation is simulated to guarantee the junction temperature would not exceed 150°C at 1-MVA and f_{SW} = 4 kHz. Figure 3.12 displays the loss distribution of one-phase

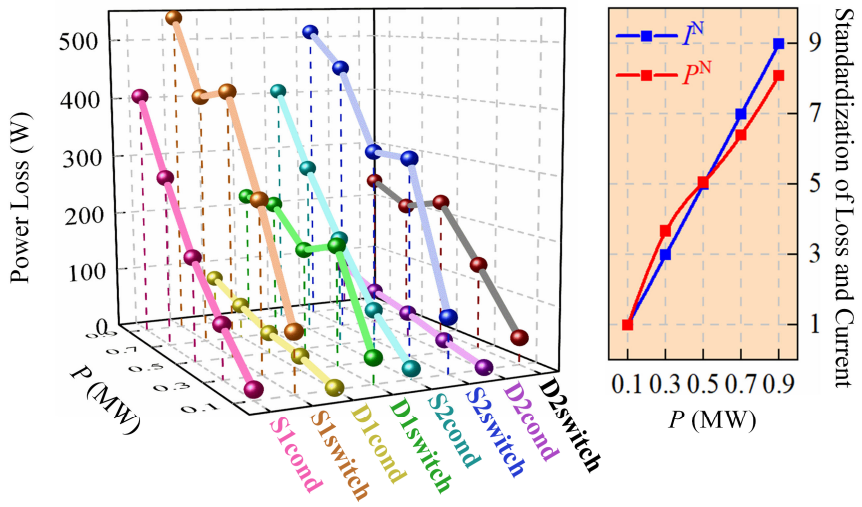


Figure 3.12: Loss distribution of one-phase semiconductor devices (S1, D1, S2, and D2) under UPFC.

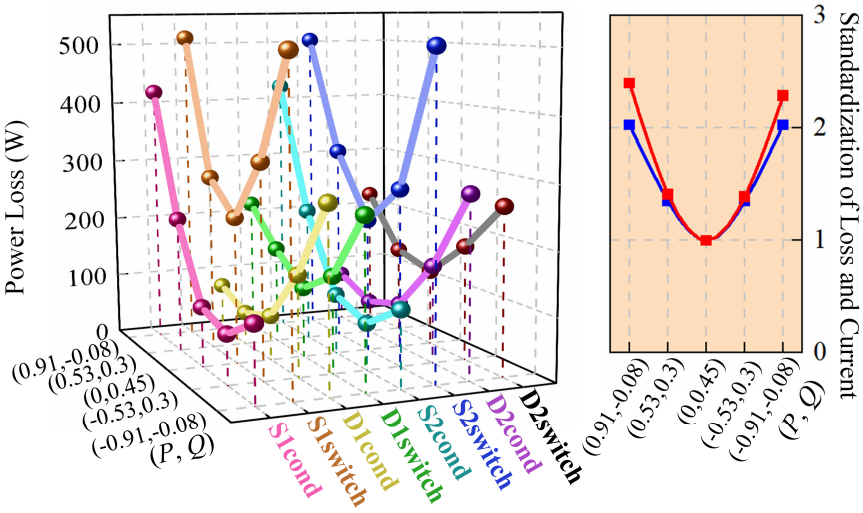


Figure 3.13: Loss distribution of one-phase semiconductor devices (S1, D1, S2, and D2) under $0.577V_{dc}$ output voltage magnitude curve.

semiconductor devices (S1, D1, S2, and D2) under UPFC. All conduction losses vary linearly with the power loading due to the volt-second balance by power flow control. However, the switching loss is noticed to be affected by variable switching frequency property significantly. For S1, at 0.5 MW loading, its switching loss is even larger than the one at 0.7 MW loading. This is because a much higher switching frequency is found at 0.5

MW loading in Figure 3.9. Similar impact is also discovered for D2 since S1 and D2 are in the complementary conduction path. For 0.3 and 0.1 MW loadings, even though switching frequencies keep increasing, due to much lower conduction currents, switching losses decrease. Standardized scales on the one-phase total loss and the conduction current are also indicated. All total losses are divided by total loss at 0.1 MW and all conduction current are divided by current vector magnitude at 0.1 MW. It is observed that the total loss variation is not proportional to the current variation. In the low power loading, the total loss variation increases with a decreasing slope, resulting from a great reduction on the switching loss. In the high power loading, the total loss variation increases with an increasing slope, which is attributed to a similar switching frequency range, but a much higher current conduction.

Compared with Figure 3.12, Figure 3.13 displays the loss distribution of one-phase semiconductor devices under the $0.577V_{\mathrm{dc}}$ output voltage magnitude curve. As shown in Figure 3.11, the switching frequencies for all steady states on this curve are the same around 2 kHz, which almost eliminates the switching frequency variation. It is noted that all losses vary with the power loading and the standardized total loss variation is proportional to the standardized current variation. These findings provide engineers with an intuitive insight on the loss distribution by FCS-MPC regulated GCI and benefit the loss estimation and thermal management design.

3.3.2 Experimental Results

A small-scale GCI prototype is developed to validate the variable switching frequency property of FCS-MPC as shown in Figure 3.15. The experimental parameters are shown in Table 3.3. The corresponding operating points or steady states of this GCI on

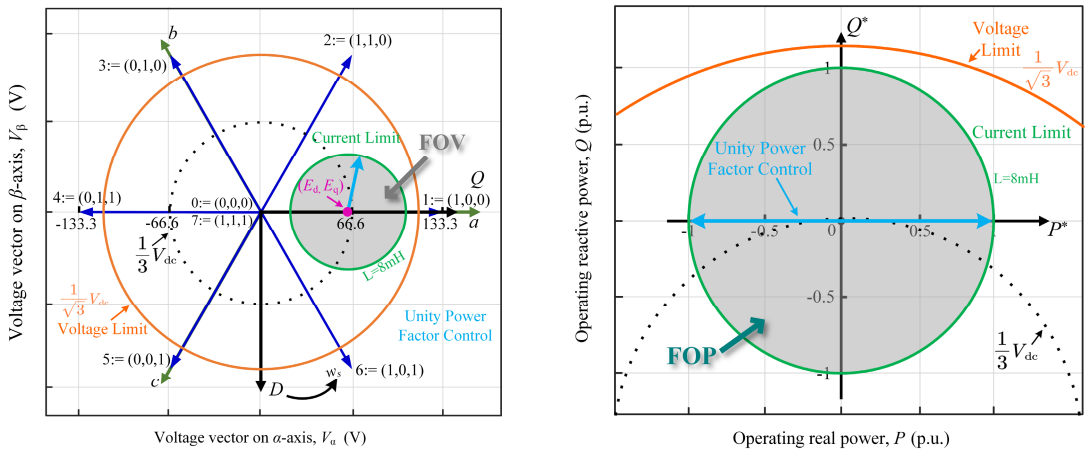
TABLE 3.3

PARAMETERS OF THE GCI IN THE EXPERIMENTS

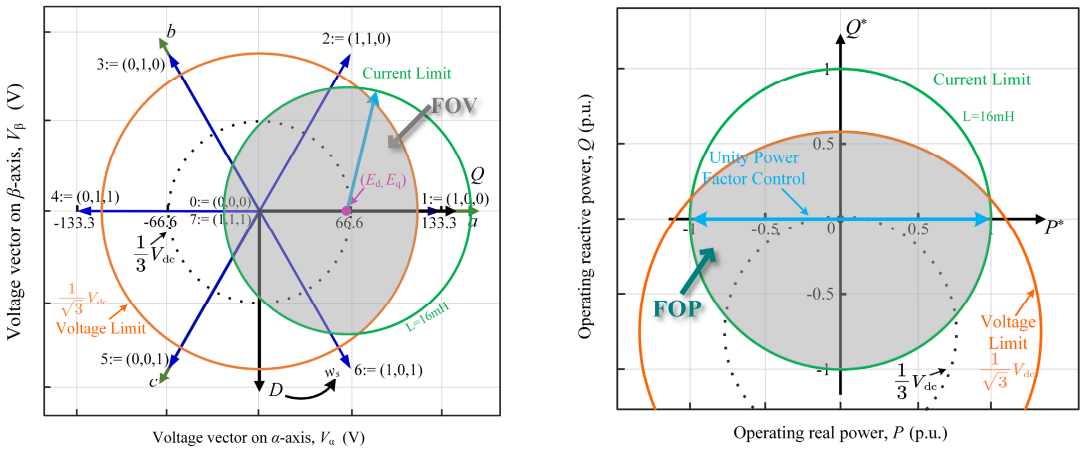
Rated power S	1.4 kVA/ 1 p.u.
Rated DC bus voltage V_{dc}	200 V
Grid frequency f	60 Hz
Rated AC grid voltage $\boldsymbol{e}^{abc}$	46.2/80 V
Line Reactors 1 L_{g1} R_{g1}	8 mH, 0.3 Ω
Line Reactors 2 L_{g2} R_{g2}	16 mH, 0.5 Ω
IGBT module	Infineon IKCM15L60GD [42]
Junction temperature T_j	-40~150 ℃
Air temperature T_{air}	25 ℃
Sampling period T_s	25 μs

FOV and FOP for two types of line reactors (LR) are shown in Figure 3.14, respectively, which are depicted by (3.31)-(3.33). It is noted that with a higher value of the LR 2, the feasible operation region on the voltage vector space has a broader area than the one with a lower value. But it may reduce the maximum power loading since the GCI output voltage would drop more on the line reactor instead of increasing the line current.

Figure 3.16 shows the measured GCI phase voltage V_{an}, line current I_a, and grid voltage E_a of the phase A by FCS-MPC. Figure 3.16(a)-(d) present waveforms under UPFC with LR 2 and the real power P at 0.4 p.u., 0.5 p.u., 0.6 p.u., and 0.7 p.u, where E_a and I_a are in phase. The GCI phase voltage V_{an} reflects the switching states of the phase A by FCS-MPC. The V_{dc} value represents the switching state $s^a = 1$ and the zero value represents the switching state $s^a = 0$. It is observed that with the power loading increasing, the phase voltage V_{an} has the less voltage transitions between V_{dc} and zero, which illustrates that the less switching transitions between 1 and 0 are used under this operating point by FCS-MPC and obviously the switching frequency over one fundamental period will be a lower value. This validates the geometry analysis proposed in Chapter 3.1 since from Figure 3.14(b), the operating points



(a)



(b)

Figure 3.14: Feasible operation ranges for (a) LR 1 and (b) LR 2.

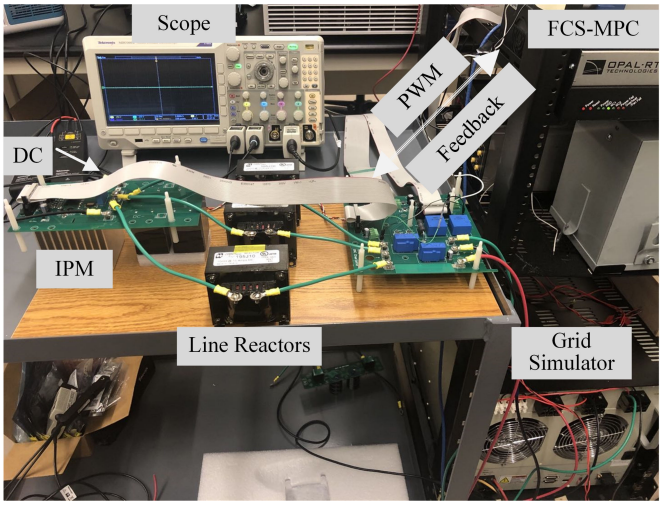
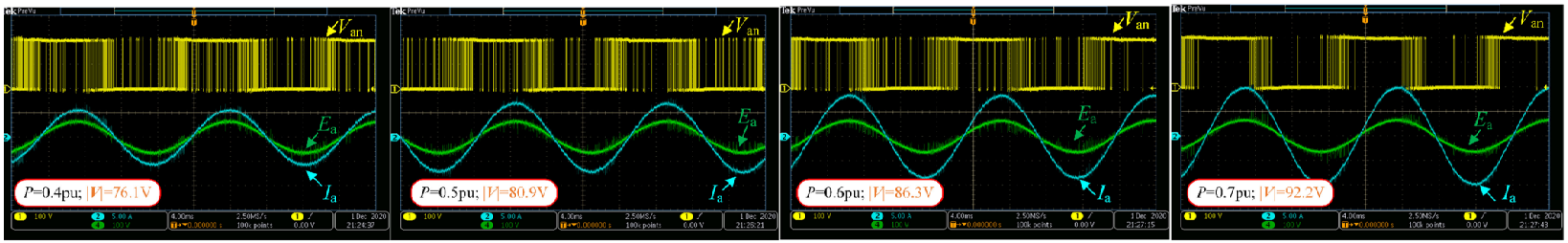
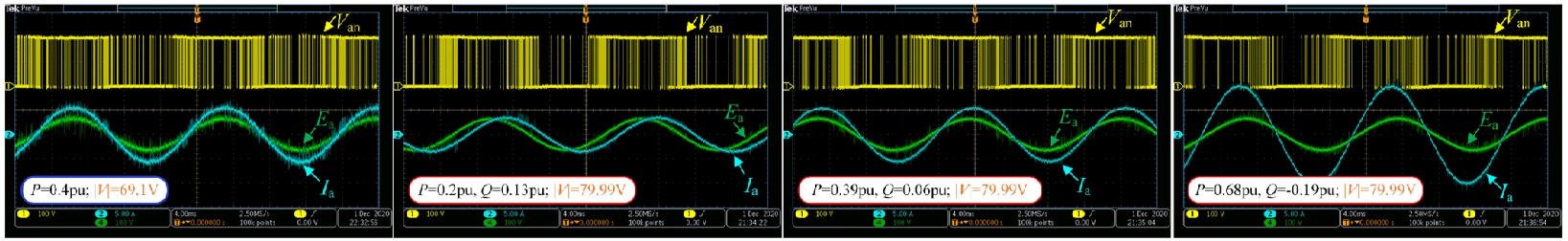


Figure 3.15: Experiment prototype of the grid-connected inverter.



(a) (b) (c) (d)



(e) (f) (g) (h)

Figure 3.16: Experimental results of GCI phase voltage V_{an} (yellow), line current I_a (blue), and grid voltage E_a (green) of the phase A by FCS-MPC including (a) P = 0.4 p.u. with LR 2, (b) P = 0.5 p.u. with LR 2, (c) P = 0.6 p.u. with LR 2, (d) P = 0.7 p.u. with LR 2, (e) P = 0.4 p.u. with LR 1, (f) P = 0.2 p.u. Q = 0.13 p.u. with LR 2, (g) P = 0.39 p.u. Q = 0.06 p.u. with LR 2, (h) P = 0.68 p.u. Q = -0.19 p.u. with LR 2.

from 0.4 to 0.7 p.u. are moving away from the $V_{dc}/3$ curve, and the switching frequency is expected to decrease.

Figure 3.16(e) presents the waveform under UPFC with LR 1 and the real power P at 0.4 p.u. Figure 3.16(a) and (e) give the same current value since they are both controlled at 0.4 p.u. However, the phase voltage V_{an} displays more voltage transitions for LR 1 than the one for LR 2, which reflects more switching transitions for LR 1. This is also can be explained by variable switching frequency property of FCS-MPC in Chapter 3.1, that even though they are under the same power loading, the location of the operating point is changed by different LRs. LR 1 results in the magnitude of the converter output voltage closer to the $V_{dc}/3$ curve compared to the LR 2 as shown in FOV in Figure 3.14, where the switching frequency is expected to increase.

Figure 3.16(b) and (f)-(h) presents waveforms with LR 2 and the magnitude of the GCI output voltage around $0.4V_{dc}$, which is 80V. The phases between E_a and I_a on these four operating points are significantly different. However, the phase voltages V_{an} display about the same amount of the voltage transitions between V_{dc} and zero value, which give about the same amount of the switching transitions. This verifies that the phase angle of the converter output voltage would not affect the switching state selection and further the switching frequency. The specific switching frequency values are compared in the following.

The instantaneous switching frequencies for steady states under UPFC are shown in Figure 3.17. Figure 3.17(a) and (b) present results for LR 1 and LR 2, respectively. The instantaneous switching frequency is calculated by counting the switching events over one fundamental period and then multiplied by fundamental frequency. The maximum

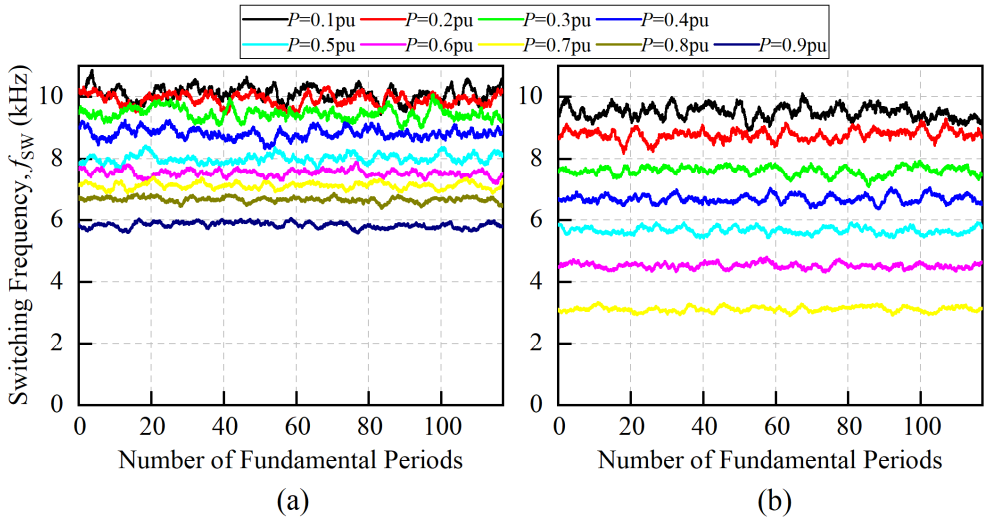


Figure 3.17: Instantaneous switching frequency by FCS-MPC under UPFC trajectory including (a) LR 1 case and (b) LR 2 case.

switching frequency happens at low power loadings for both LR 1 and LR 2 around 10 kHz, which is attributed to the operating points of low power loadings close to the $V_{dc}/3$ curve from FOVs. It is noted that the collection of the switching frequency in LR 1 case is higher than the one in LR 2 case. This is because of the smaller feasible operation region in FOV and all operating points in that FOV are much closer to the $V_{dc}/3$ curve in the LR 1 case, where it provides the GCI with a higher switching frequency at the same power loading. In addition, since in the LR 2 case, the feasible operation region is broader as shown in Figure 3.14, where it provides the GCI with a output voltage magnitude further away from the $V_{dc}/3$ curve and eventually a larger switching frequency range, from 10 kHz to 3 kHz.

Another instantaneous switching frequency result is depicted in Figure 3.18, where the instantaneous switching frequencies are calculated for experiments from Figure 3.16(b) and (f)-(h) and P = 0.9 p.u. in LR 1 case. All of these testing have GCI output voltage magnitudes around $0.4V_{dc}$. It is explicitly illustrated that the switching frequencies are all

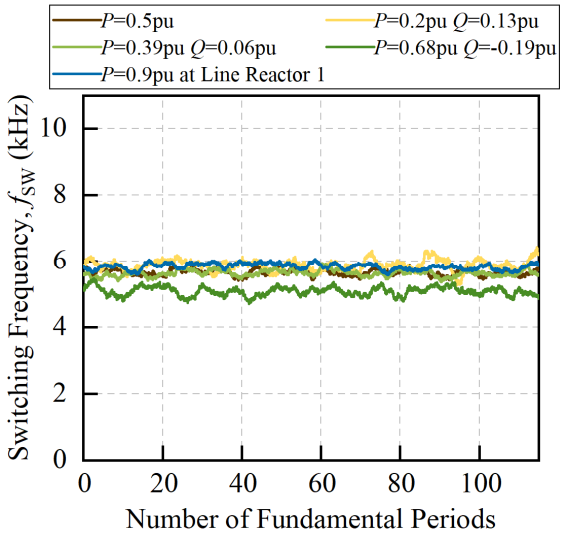


Figure 3.18: Instantaneous switching frequency by FCS-MPC under $0.4V_{dc}$ output voltage magnitude curve.

about the same level, and most are from 6 kHz to 5.5 kHz. This justifies the variable switching frequency property of FCS-MPC that the same converter output voltage magnitude ideally contributes to the same switching frequency and the switching frequency is independent of the phase angle of the output voltage.

By collecting all experiment results and calculating the mean value of the instantaneous switching frequency, the switching frequency distribution over the converter output voltage magnitude is presented in Figure 3.19. Three case regions used in the geometry analysis of Chapter 3.1 and the $V_{dc}/3$ curve are identified in Figure 3.19. It is observed that for the same output voltage magnitude, the switching frequencies for both LR 1 and LR 2 cases turn to be highly consistent. In LR 2 case, more output voltage magnitudes are covered because of the broader FOV. Figure 3.19 effectively justifies the conclusions about the variable switching frequency property of FCS-MPC in Chapter 3.1, that the switching frequency of FCS-MPC regulated GCI depends on the converter output voltage magnitude. The maximum switching frequency happens around the $V_{dc}/3$ curve,

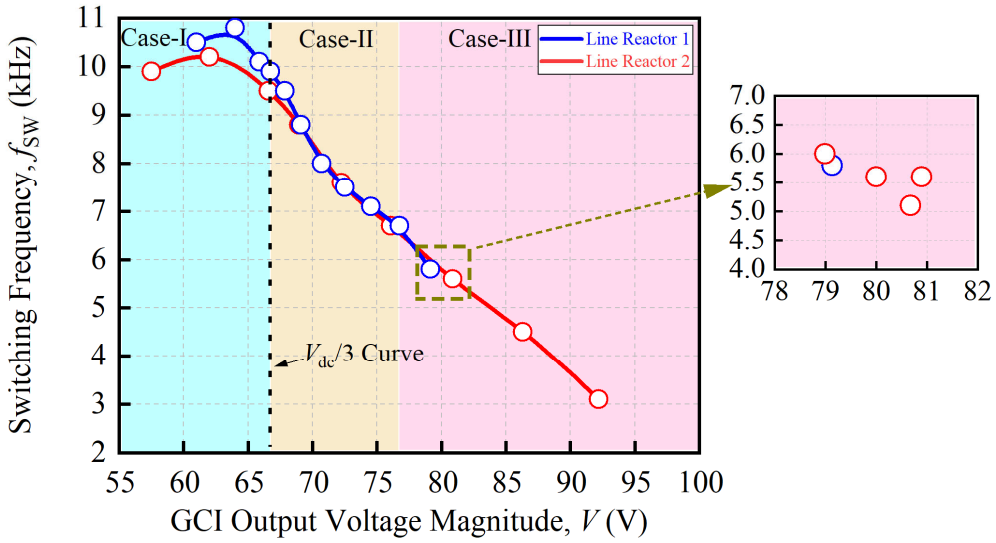


Figure 3.19: Switching frequency over the output voltage magnitude.

which is about 10 kHz to 11 kHz for both LR 1 and LR 2 cases. And the switching frequency decreases in both directions that the output voltage magnitude increases or decreases away from $V_{dc}/3$. Some differences exist because of the disturbance on the grid voltage $\boldsymbol{e}^{abc}$, the mismatch of the model parameters and the switching effect of the power semiconductor devices.

3.3.3 Impacts of Variable Switching Frequency

A significant impact of the variable switching frequency is analyzed on the switching loss, of which results are shown in Figure 3.20. Figure 3.20(a) displays the switching loss distribution of phase A semiconductor devices under the UPFC trajectory with LR 1. It is noted that with the current magnitude increasing, the switching losses for all IGBTs and diodes are not proportionally increasing as the current magnitude. Maximum switching loss happens around $\boldsymbol{I} = 11$ A since the switching frequency decreases more and more according to the Figure 3.17(a). Figure 3.20(b) displays the switching loss distribution under the $0.4V_{dc}$ curve with LR 2. It is noted that the switching loss has a more

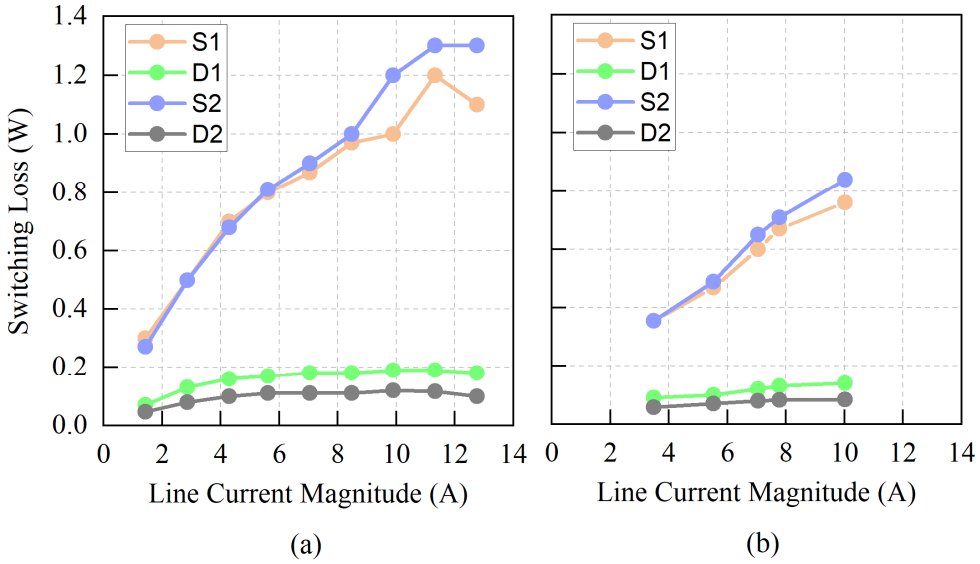


Figure 3.20: Switching loss distribution of one-phase semiconductor devices (S1, D1, S2, and D2) under (a) UPFC trajectory with LR 1 and (b) $0.4V_{dc}$ curve with LR 2.

linear relationship to the current magnitude, which is because switching frequencies for these operating points are about the same range as shown in Figure 3.18. When $\boldsymbol{I}$ = 10 A, which is the steady state at (P = 0.68 p.u. Q = -0.19 p.u), the switching loss does not increase that much as the current magnitude since the switching frequency at this steady state is only 5.1 kHz which is lower than others.

Another impact of this variable switching frequency is preliminarily investigated on the current harmonics. Figure 3.21 reveals the total harmonic distortion of the phase A current under the UPFC in both LR 1 and LR 2 cases. Dash lines represent the THD of the phase A current through the fixed 10-kHz switching frequency modulation. THD values by FCS-MPC are higher than the one under the fixed 10-kHz modulation, especially for the high power loadings, This is because the switching frequency decreases by FCS-MPC with the power loading increasing from FOPs. Then, low order harmonics components on the frequency spectrum would increase and take more weightings in the THD. A more

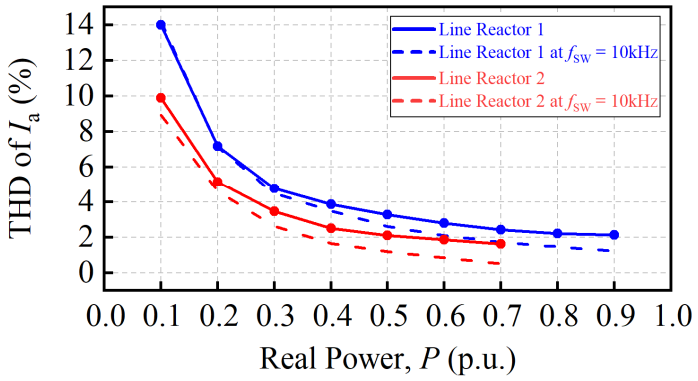


Figure 3.21: THD of phase A current under UPFC by FCS-MPC (solid) and fixed 10-kHz switching frequency modulation (dash).

sophisticated study on the harmonics and the filter design for the FCS-MPC regulated converter will be conducted in the future work.

3.3.4 Application of Variable Switching Frequency on Thermal Stress of Power Converters

Applying this variable switching frequency property of FCS-MPC to the industry application, its advantage would be prominent from the perspective of the thermal stress of power modules on the grid-connected inverter. During the high power loadings, FCS-MPC would autonomously decrease the switching frequency and further the power loss. During the low power loadings, FCS-MPC would increase the switching frequency and further the power loss. A more balanced thermal profile is achieved according to the proposed variable switching frequency property, which eventually contributes to a mitigated thermal stress on the inverter.

Figure 3.22-3.24 demonstrate this advantage by loading a varying mission profile, Figure 3.22(a), on the inverter with LR 1 from Figure 3.13. FCS-MPC and PI linear controllers are calibrated separately to regulate the power flow from the DC-bus to the grid. PI linear controller uses the fixed switching frequency at 8 kHz which is designed to be the

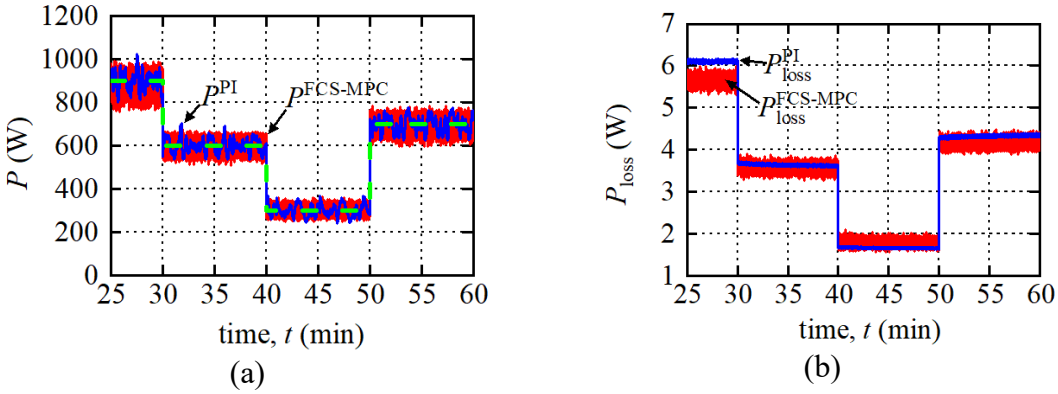


Figure 3.22: Experimental results of the application over the mission profile, (a) the instantaneous real power by PI (blue) and FCS-MPC (red), (b) the averaged single IGBT loss by PI (blue) and FCS-MPC (red).

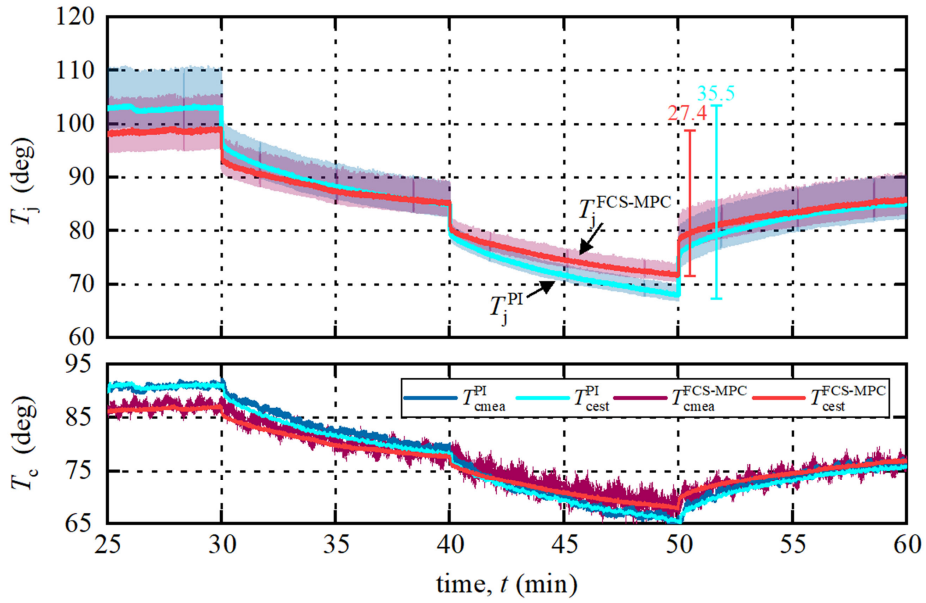


Figure 3.23: Thermal profiles over the mission profile, the estimated junction temperatures, the estimated case temperatures and the measured case temperatures by PI and FCS-MPC, respectively.

mean value as well as the median value of the variable switching frequency results in Figure 3.15(a).

Figure 3.22, 3.23, and 3.24 show the comparisons between FCS-MPC and PI controllers on the averaged single IGBT loss, the thermal profiles, and the system

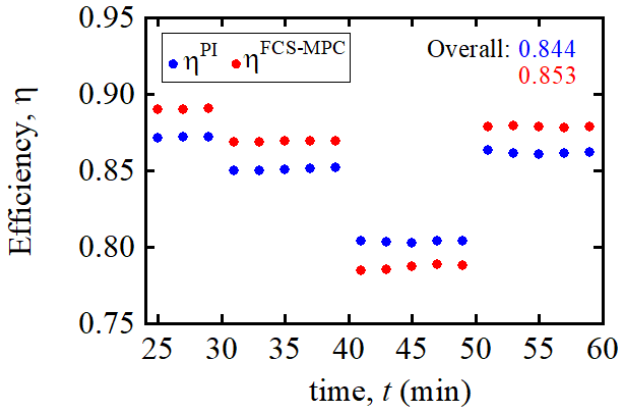


Figure 3.24: System efficiencies over the mission profile by PI (blue) and FCS-MPC (red).

efficiency. Figure 3.22(a) illustrates that both controllers achieve the stable power transmission according to the mission profile. The single IGBT loss in Figure 3.22(b) reflects the distinction by FCS-MPC, that the switching frequency is higher than 8 kHz in the low power loading, and conversely lower than 8 kHz in the high power loading due to its variable switching frequency property. This result directly contributes to a lower thermal stress of power modules by FCS-MPC as shown in Figure 3.23. The junction temperature T_j in Figure 3.23 is estimated through the RC thermal model and the heatsink temperature feedback. It is noted that the junction temperature variation is reduced to 27.4°C by FCS-MPC instead of 35.5°C by PI at around the same mean value. The high consistence of the estimated and measured case temperatures T_c strengthens the accuracy and the authenticity of the conclusions from the junction temperature. The close system efficiencies, 84.4% for PI and 85.3% for FCS-MPC, are noticed in Figure 3.24 over the whole mission profile, where the system efficiency is not sacrificed by variable switching frequency property of FCS-MPC.

Thus, for those mission critical applications, like the solar energy with highly varying mission profiles, FCS-MPC could achieve a superior performance on the thermal stress of power modules and about the same efficiency in the long-term operation compared with the conventional PI controller.

3.4 Conclusion

In this chapter, the variable switching frequency property of the finite control set model predictive control has been investigated. The intuitive relationship between the switching frequency and the magnitude of the converter output voltage reference is proposed through the geometry analysis, by the switching state selection and the switching sequence formulation. The switching frequency is derived to be maximized when the magnitude of the converter output voltage reference is around one third of the DC-bus voltage value. Then, the switching frequency decreases in both directions that the magnitude moves away from this value. Multiple operating points from the contoured feasible operation range are tested in both simulations and experiments. All results verify the proposed variable switching frequency property of FCS-MPC.

The impacts of this property on the power loss and current harmonics are also analyzed, which provides engineers and researchers with more insights to fully leverage the FCS-MPC. One application of this proposed variable switching frequency property is presented to demonstrate the lower thermal stress of power modules by FCS-MPC compared with the conventional PI controller, where a less-varying temperature profile is achieved over the same mission profile. This contribution can significantly benefit the DER systems in the industry application.

CHAPTER 4 FINITE-CONTROL-SET MPC WITH SECONDARY PROBLEM FORMULATION

One significant advantage of FCS-MPC is its flexibility to control multiple objectives simultaneously [38], [39]. In the most power electronics systems, current loop control is the primary control objective to determine the converter duty ratios or the switching state, which is similarly defined as the primary problem formulation in FCS-MPC as investigated in Chapter 3. Compared to the conventional PI control, FCS-MPC provides the system with more freedom to control other objectives at the same time in addition to the current control as shown in Figure 4.1. This is because that there always exists a deterministic switching state that will derive a minimum value of the integrated multiple objective functions. These other objectives are defined as the secondary problem formulations in FCS-MPC, of which objective functions only need a simple addition to the primary objective function. This consolidated control structure in FCS-MPC eliminates the complex cascaded control loops, the mixed PI tunings, and the variable decoupling issues,

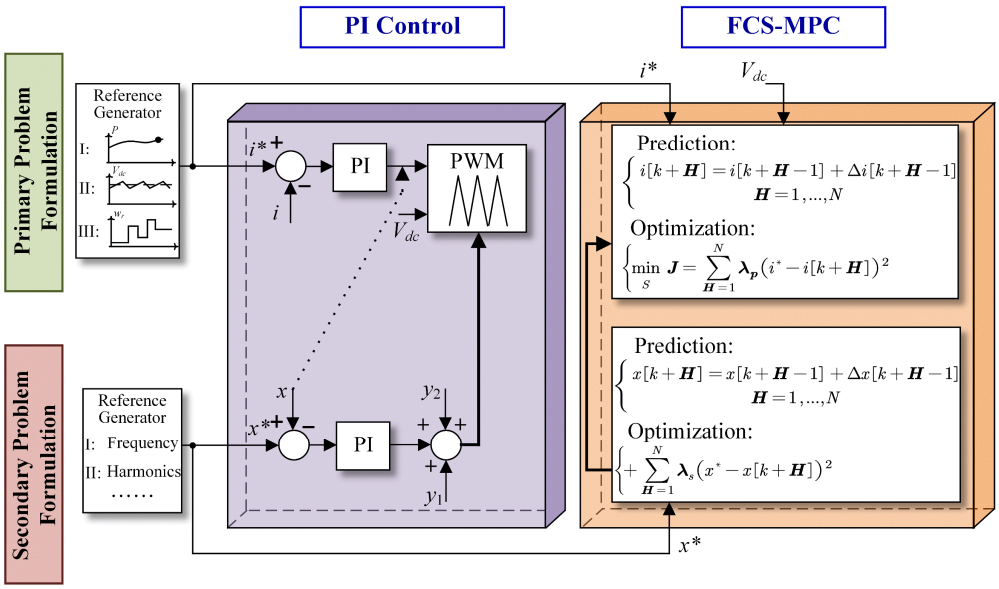


Figure 4.1: Control algorithms of PI control and FCS-MPC with primary and secondary control objectives.

which are inevitable in the PI control. According to this feature, FCS-MPC is believed to have more active effects in the power loss and thermal stress reduction.

As discussed in Chapter 1.2, the thermal stress causes the most failures in power modules, where the junction temperature heated up and cooled down triggers the physical separation at the interface between various materials. It is noted that the junction temperature mean value $T_{j,m}$ and the junction temperature swing value ΔT_j that exceed the strength limit of semiconductor devices would jeopardize power modules. Hence, these two variables are regarded as signatures of the thermal stress. Besides, the thermal cycling duration $T_{j,on}$ is also justified as another thermal stress factor, but out of the scope in this dissertation. As mentioned, this thermal stress is attributed to the power loss during the operation. If the loss of the power module is actively controlled, then the junction temperature can be effectively affected, even though the junction temperature is not the explicit control objective. In this chapter, the secondary problem formulation is defined in the FCS-MPC to reduce the power loss in power modules and further the thermal stress.

4.1 Loss Model of Power Modules

The proposed control method predicts and minimizes the power loss in each discrete sampling period, where an energy-based loss model of the power module is established. The power loss in power modules consists of two parts, the conduction loss and the switching loss, coming from the active switch (IGBT, MOSFET, etc.,) and the antiparallel diode, respectively. The conduction state and switching events for the half-bridge semiconductor devices against the current and the switching state are shown in Figure 4.2, where it covers both upper and lower level switches. All dynamic actions are summarized

for the hard switching on the half bridge. The soft switching is not considered in this dissertation.

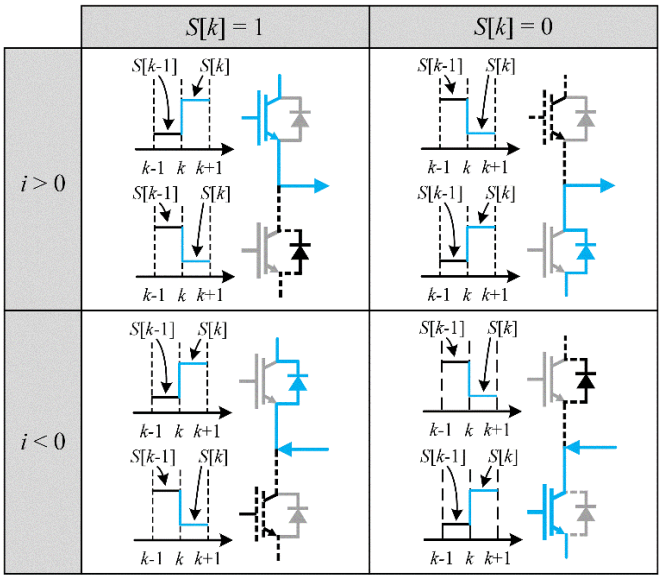


Figure 4.2: Conduction states and switching events of the grid-tied inverter.

Switching loss in terms of the pulse energy happens when the semiconductor device turns on or off for the current commutation. This switching loss can be calculated by using the curve fitting and the behavioral loss model [29]

$$E_{switch} = \begin{cases} E_{on}(\boldsymbol{i}_{abc}, T_j) \cdot V_{CE}/V_{CE,rated}, & \triangle \boldsymbol{s}_{abc} = 1 \\ 0, & \triangle \boldsymbol{s}_{abc} = 0 \\ E_{off}(\boldsymbol{i}_{abc}, T_j) \cdot V_{CE}/V_{CE,rated}, & \triangle \boldsymbol{s}_{abc} = -1 \end{cases} \tag{4.1}$$

where the switching loss depends on the line current $\boldsymbol{i}_{abc}$ for each phase, the blocking voltage V_{CE} that is V_{DC} in the two-level converter, the junction temperature T_j and the successive switching states. Since the current switching state $\boldsymbol{s}_{abc}[k]$ is known in the proposed FCS-MPC, the switching loss in terms of the pulse energy loss is available to be calculated by (4.1).

Conduction loss is the power dissipated on the semiconductor device during the device on-state. In the proposed FCS-MPC, since each output switching state has a fixed duration which is the sampling period, the conduction loss can be estimated in terms of the uniform energy [29]

$$E_{cond} = \begin{cases} T_s \cdot P_{cond} = T_s \cdot v_{CE,ON}(\boldsymbol{i}_{abc}, T_j) \cdot \boldsymbol{i}_{abc}, & \boldsymbol{s}_{abc}[k+1] = 1 \\ 0, & \boldsymbol{s}_{abc}[k+1] = 0 \end{cases} \tag{4.2}$$

where $v_{CE,ON}$ is the voltage drop on the semiconductor device during the on-state which is determined by curve fitting with the current $\boldsymbol{i}_{abc}$ and the junction temperature T_j. In the proposed control method, since the sampling period is much smaller than the fundamental period of the utility grid, the $\boldsymbol{i}_{abc}$ at the sampled time instant is used for the predicted $\boldsymbol{i}_{abc}$ in next few time instants. Thus, the conduction loss in terms of the uniform energy loss is available to be calculated by (4.2).

Then, the total energy-based power loss for all bridges can be calculated in the sum of the switching loss and conduction loss

$$\boldsymbol{E}_{abc}[k] = \sum_{a,b,c} (E_{switch}[k] + E_{cond}[k]) \tag{4.3}$$

It is noted that both switching loss and conduction loss vary with the junction temperature. The amount of power loss would change significantly over a broad range of the junction temperature, even if the converter is operating under the same power loading. Furthermore, the power loss would have a feedback on the junction temperature, which complicates the system dynamic analysis. Therefore, the junction temperature of the power model has to be identified in the proposed control method.

4.2 Thermal Model of Power Modules

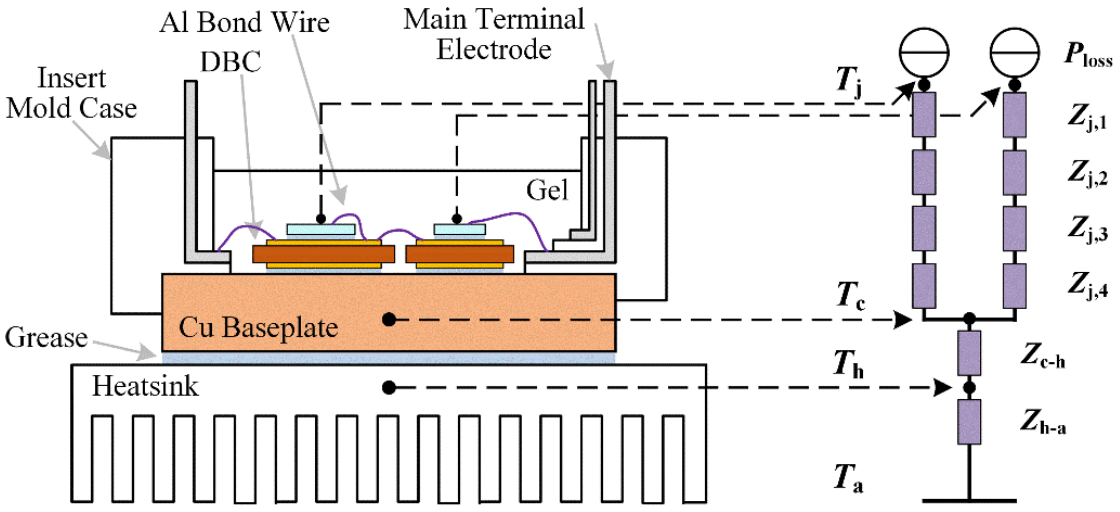


Figure 4.3: Structure of the power module and its Foster-type RC thermal model

Due to the lack of the cost-effective high bandwidth temperature measurement, the junction temperature of the power module is retrieved through the real-time estimation in the most scenarios. The common way to estimate it is through a thermal resistance and capacitance (RC) model and a simple case or heatsink temperature feedback [33]. Figure 4.3 shows a Foster-type RC model of power modules, including four layers of the junction-to-case thermal impedance, one layer of the case-to-heatsink thermal impedance and one layer of the heatsink-to-air thermal impedance. Each thermal impedance consists of one lumped RC which only infers the mathematical fitting of the temperature curve and has no physical meanings. In the proposed control method, since the junction temperature is not the explicit control objective, the use of the Foster-type RC thermal model is sufficient for the junction temperature estimation. Meanwhile, it avoids a large control complexity from other models.

The parameters of the Foster-type RC thermal model are provided based on the transient thermal impedance curve in the datasheet provided by the manufacturer. Thermal

resistance and thermal capacitance are used to obtain the frequency domain representation of the thermal impedance. And the junction temperature of the power module is estimated as

$$T_j = P_{loss} \sum_{i=1}^{n} Z_{j,i} + T_c = P_{loss} \sum_{i=1}^{n} \frac{R_i}{\tau_i s + 1} + T_c \tag{4.4}$$

where P_{loss} is the output from the loss model, R_i and τ_i are the thermal resistance and time constant for the layer i of thermal model, T_c is the case temperature feedback which can be measured through a low-bandwidth thermocouple or a linear thermal sensor.

4.3 Complete Problem Formulation

After implementing the loss model and the thermal model for the power module in the FCS-MPC, the energy-based power loss for future time instants can be formulated in the secondary problem formulation. Similar ℓ_2 norm-2 least square objective function is used to reduce the power loss

$$J_s = \sum_{j=1}^{H} \| \mathbf{0} - \boldsymbol{E}_{abc}[k+j] \|_2^2 \tag{4.5}$$

where $\mathbf{0} \in \mathbb{R}^{3x1}$ is a zero vector formulated as the reference power loss, $\boldsymbol{E}_{abc} \in \mathbb{R}^{3x1}$ is the predicted energy-based power loss from the FCS-MPC secondary problem formulation, $J_s \in \mathbb{R}^{+}$ is the secondary objective value which is calculated for each $\boldsymbol{s}_{abc}$. Then, the integrated objective function including the primary and secondary objective functions is enabled to be defined. A simple addition is used, which maintains the power flow control requested by the mission profile and reduces the power loss and thermal stress simultaneously

$$\min_{\boldsymbol{s}_{abc}} \quad \lambda_p \cdot J_p + \lambda_s \cdot J_s \tag{4.6}$$

where λ_p and λ_s are weightings of primary and secondary objective functions, respectively, which emphasizes the significance of different problem formulations.

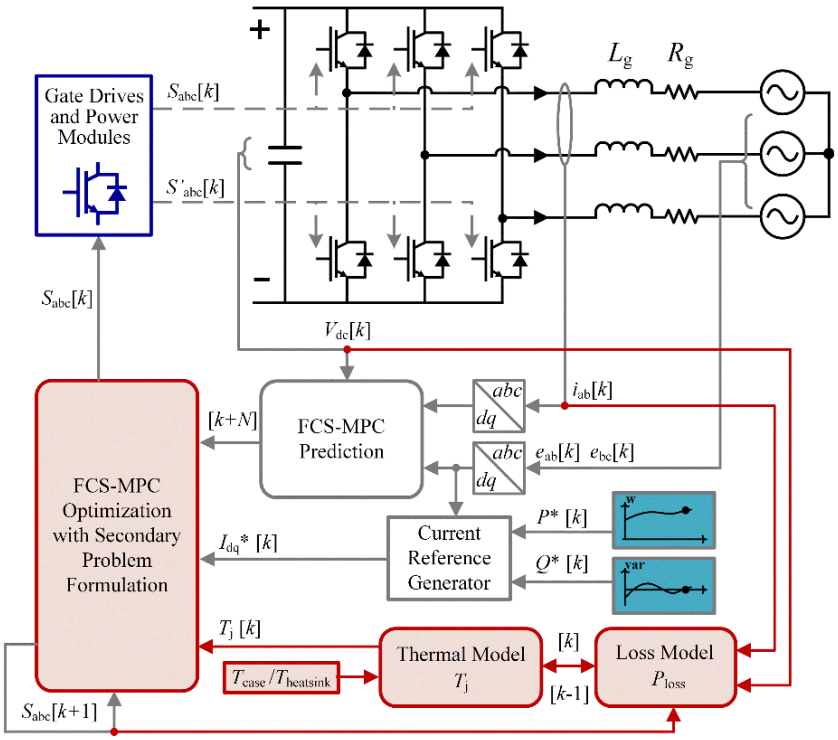


Figure 4.4: System diagram of the grid-tied inverter by the proposed FCS-MPC

The complete control block diagram of the proposed FCS-MPC is shown in Figure 4.4 with red block diagrams for the secondary problem formulation. Since the power flow control by the primary problem formulation is still fundamental in the proposed FCS-MPC, its weighting λ_p is fixed at unity in all operations. However, the weighting of secondary problem formulation λ_s needs be determined based on the magnitude of objective values J_p and J_s, the power converter operation conditions such as the junction temperature level, and the system constraints. System constraints on the line current, the power limit, and the junction temperature are not mentioned in above problem formulations. But they are embedded in the proposed FCS-MPC as well. Hence, the impact of the secondary problem formulation on the system performance extremely depends on the selection of the

secondary weighting λ_s. The investigation of this is presented and analyzed in the Chapter 4.4.1, where a most efficient λ_s curve is proposed to design the proposed FCS-MPC and a weighting-zones strategy is applied for a heavy power loss reduction and a grid code compliance.

4.4 Results Validations

To verify the effectiveness of the proposed FCS-MPC, multiple simulations and experiments have been carried out. All results will be presented and analyzed in this section.

4.4.1 Simulation Results

MATLAB/Simulink and PLECS software are used to simulate a grid-tied inverter rated at 60 kW, considering the system diagram in Figure 4.4. The grid-tied inverter consists of three Infineon FF100R12RT4 half-bridge IGBT modules. The simulation parameters of the grid-tied inverter and the proposed FCS-MPC are shown in Table 4.1 and Table 4.2, respectively. It should be noted that the switching frequency is equal or less than the half of the sampling frequency in this FCS-MPC. Normally, the IGBT switches below than 20 kHz, where the sampling frequency is set at 40 kHz in this case. The prediction receding horizon is set to be only one discrete time instant, because the fundamental frequency of the grid voltage is much smaller than the sampling frequency. One discrete time instant is sufficient to predict the system behaviors and demands the least online calculation. For those high fundamental frequency applications, such as wireless power transfer (WPT), an extended prediction horizon will be employed.

Figure 4.5 shows the comparison results between the proposed FCS-MPC and the conventional FCS-MPC when a rated power is applied at the unity power factor. In the conventional FCS-MPC, the secondary weighting λ_s is always set to be zero in order to

TABLE 4.1

PARAMETERS OF THE GRID-TIED INVERTER SYSTEM IN THE SIMULATION

Rated power P	60 kW/ 1 p.u.
Power factor pf	1.0
Rated DC bus voltage V_{dc}	1000 V
Grid frequency f	60 Hz
Rated AC grid voltage $\boldsymbol{e}_{abc}$	277/480 V
Line current $\boldsymbol{i}_{abc}$	72.2 A
Line inductance L_g	3 mH
Line resistance R_g	10 mΩ
DC bus capacitance C	3300 μF
IGBT module	Infineon FF100R12RT4
Air temperature T_{air}	25 ºC

TABLE 4.2

PARAMETERS OF THE PROPOSED FCS-MPC

Primary weighting λ_p	1
Prediction receding horizon H	1
Sampling period T_s	25 μs

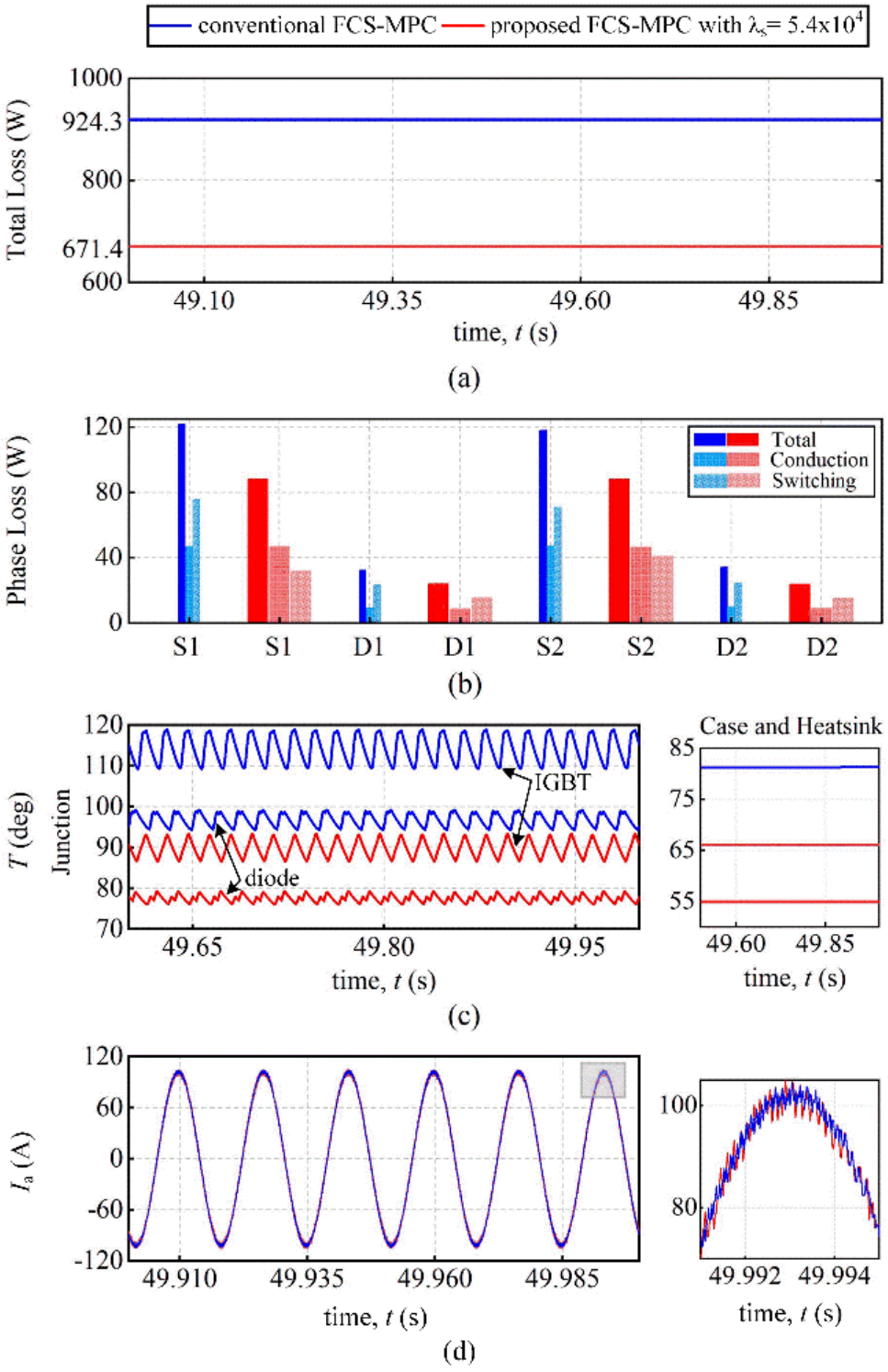


Figure 4.5: Simulation results by the conventional FCS-MPC (blue) and the proposed FCS-MPC at λs = 5.4·104 (red).

eliminate the effect of the secondary problem formulation. It is set to be $5.4 \cdot 10^4$ in the proposed FCS-MPC in this case since the magnitude of the energy-based power loss is found around 10 millijoules, where the secondary objective value J_s is around 10^{-4}. It is noted that the total loss for all switches is reduced from 924.3 W to 671.4 W as shown in Figure 4.5(a). Most of the reduction is attributed to the switching loss, about a half number reduced for both upper and lower switches in Figure 4.5(b). Following this huge power loss reduction, all temperature values including the junction temperature, the case temperature and the heatsink temperature are noticed to be reduced as well. Estimated junction temperatures decrease from a mean value of 114.5 ℃ of the IGBT and 97.5 ℃ of the diode to a mean value of 94 ℃ and 78 ℃, respectively, as shown in Figure 4.5(c). The case temperature and the heatsink temperature also have about 20 ℃ and 10 ℃ cooling down. This improvement clearly validates the effectiveness of the proposed FCS-MPC on the thermal stress reduction.

The tradeoff from this loss reduction is reflected on the current harmonics distortion in Figure 4.5(d), where the total harmonics distortion (THD) is used to evaluate this tradeoff

$$\mathrm{THD} = \frac{\sqrt{I_{2F}^2 + I_{3F}^2 + \cdots + I_{nF}^2}}{I_F} \qquad n = 2, 3, ..., N \tag{4.7}$$

where F is the fundamental frequency, which is 60 Hz in this case, n is the integer multiplication and N is the maximum integer multiplication in this analysis. According to the grid code IEEE Standard 519-2014 [34], the grid-friendly current THD is supposed to be less than 5%. By calculating the THD of the phase current in Figure 4.5(d), it is noted that the THD is increased from 1.63% to 2.23% because of the secondary problem

formulation in the proposed FCS-MPC. However, it is still far below the regulation of the grid code since the sampling frequency is 40 kHz which is high enough in this case. In some low sampling frequency applications, the current THD could be found much higher than these values.

Then, the impact of the secondary weighting is investigated. The system performance and its tradeoff highly depend on the significance of the secondary problem formulation. With the secondary weighting λ_s increasing from zero to $32.4 \cdot 10^4$ at the rated power, the system performance and its tradeoff are shown in Figure 4.6 and Figure 4.7.

In Figure 4.6, the total power loss in power modules keeps decreasing with λ_s increasing. However, comparing the last $5.4 \cdot 10^4$ increment (from $\lambda_s = 27 \cdot 10^4$ to $\lambda_s = 32.4 \cdot 10^4$) to the first $5.4 \cdot 10^4$ increment (from $\lambda_s = 0$ to $\lambda_s = 5.4 \cdot 10^4$), the change on the total power loss is much fewer, only 13.8 W for the last increment. It is also noted that when the secondary problem formulation starts to affect the system, where λ_s is small, the power loss reduction is being accelerated, where the reduction rate increases. Then, a largest reduction rate happens between $2.7 \cdot 10^4$ and $5.4 \cdot 10^4$. Beyond this largest reduction rate, the power loss reduction is being deaccelerated, where the reduction rate decreases. More analysis on this will be discussed later in this section.

The current harmonics are noticed to be further increased as shown in Figure 4.6 and Figure 4.7. In Figure 4.6, an approximate linear relationship between the current THD and the secondary weighting λ_s is noticed. When the secondary weighting is $2.7 \cdot 10^4$, the current THD is around 5%, where any heavier secondary weightings resulting in a higher THD will be prohibited because of the grid code. In Figure 4.7, the current vector in the stationary $\alpha\beta$ reference frame is shown. A much thicker current vector trajectory is

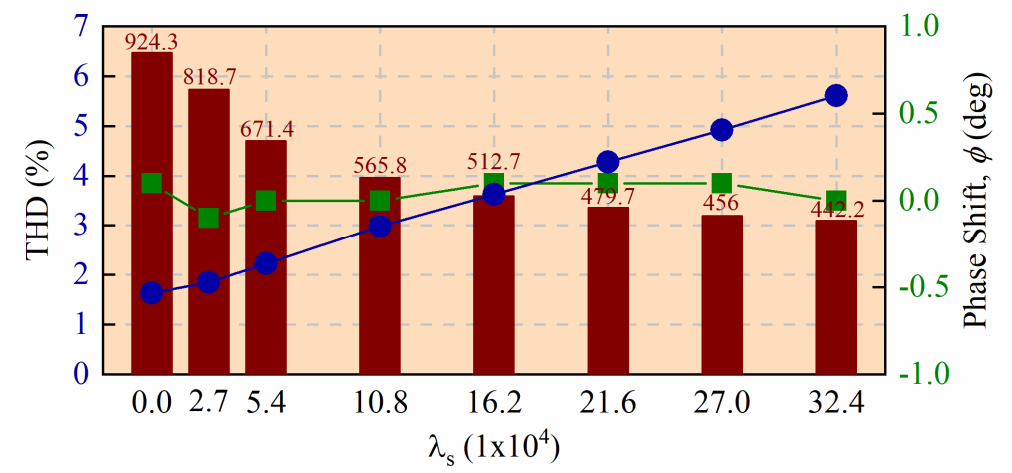


Figure 4.6: Impacts on the system performance by different λ_s at the rated power.

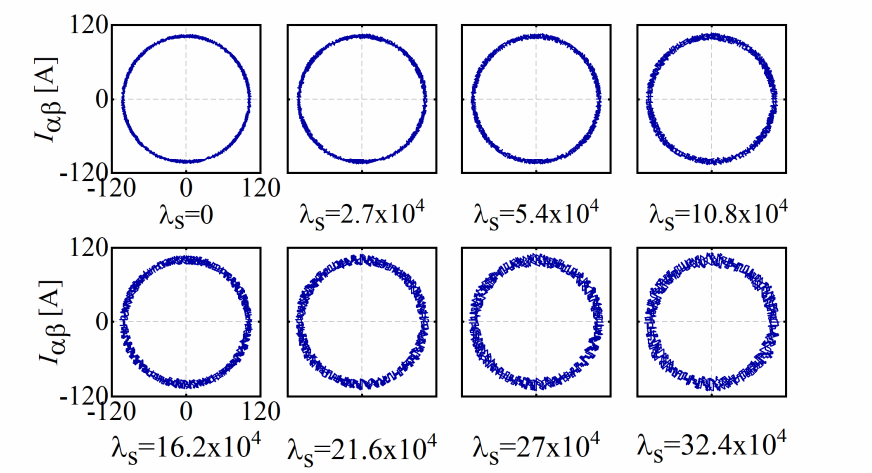


Figure 4.7: Current vectors in the stationary $\alpha\beta$ reference frame by different λ_s.

observed since much more current harmonics are injected with the more weightings on the secondary problem formulation. Impact on the power factor is also noticed in Figure 4.6 by comparing the phase shift between the grid voltage and the current at the fundamental frequency. All phase shifts are close to zero which is the unity power factor as requested by controller.

Based on the findings in Figure 4.6, a most efficient λ_s is defined for the value of λ_s that contributes to a largest power loss reduction rate. Then, it could be formulated as

$$\max_{\lambda_s} \quad c = \left| \frac{dP_{loss}}{d\lambda_s} \right| \tag{4.8}$$

where c is defined as the power loss reduction rate. A most efficient λ_s is found to be $3 \cdot 10^4$ at the rated power. Any other secondary weightings less or greater than this value will have a smaller power loss reduction rate. Multiple power loadings from 1 p.u. to 0.32 p.u. have also been tested for this investigation which is shown in Figure 4.8. A most efficient λ_s curve is highlighted when all most efficient λ_s for different power loadings are connected. The λ_s on this curve will contribute to a largest power loss reduction rate c for the corresponding power loading. The most efficient power loss reduction is achieved by using this most efficient λ_s curve.

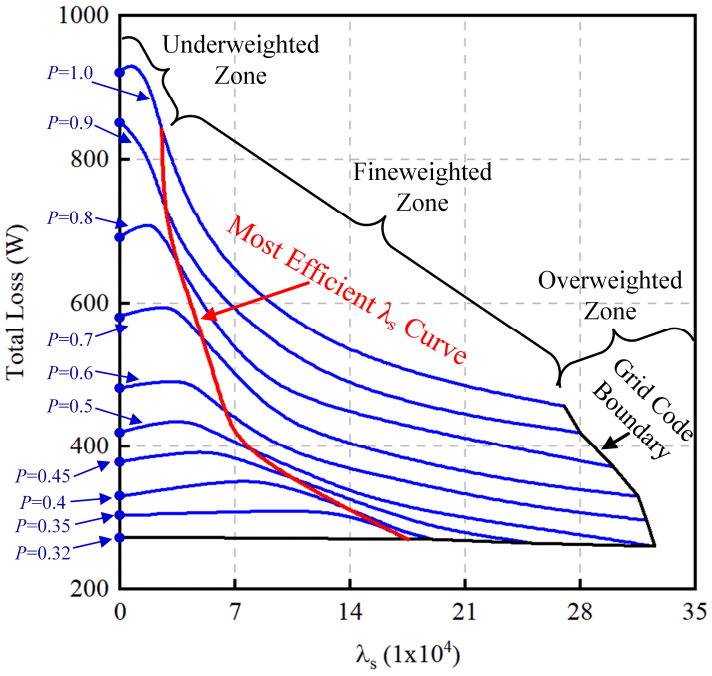


Figure 4.8: Impacts on the system performance by different λ_s for different power loadings including the most efficient λ_s curve and the weighting-zones strategy.

In addition, a weighting-zones strategy is summarized from Figure 4.8. First, with the power loading is reduced, a larger λ_s is required to make the secondary problem formulation effective, because the loading current and the secondary objective value J_s are much smaller than ones in the full loading. For example, the power loss remains the same until the λ_s is larger than $13 \cdot 10^4$ at 0.35 p.u.. Any λ_s located from zero to the most efficient λ_s curve are defined in the underweighted zone, which has a very limited effect on the power loss reduction. Second, the grid code boundary is contoured in Figure 4.8. With the power loading is reduced, the boundary λ_s initially increases because of a lower secondary objective value J_s. However, due to the property of FCS-MPC, the current harmonics varies with power loadings, where an extreme low power loading will generate a current THD close to the grid code boundary even with no secondary problem formulation. The boundary λ_s eventually returns to zero at 0.32 p.u.. Any λ_s located beyond this grid code boundary are defined in the overweighted zone which gives a poor power quality and a small marginal power loss reduction. Last, any λ_s located on the most efficient λ_s curve or between the most efficient λ_s curve and the grid code boundary are defined in the fineweighted zone which contributes to a most efficient power loss reduction or a further reduction if a heavy thermal stress is found in power modules. This weighting-zones strategy provides all engineers and researchers with an intuitive insight and design guidelines to make full use of the proposed FCS-MPC and balance its performance and tradeoff.

4.4.2 Experimental Results

A grid-tied inverter prototype is developed to demonstrate the proposed FCS-MPC as shown in Figure 4.10. The experimental parameters of the grid-tied inverter are shown

in Table 4.3 and the proposed FCS-MPC parameters remain the same as in Table 4.2, where the grid-tied inverter uses the same IGBT modules as that in the simulations. Even though only a low power loading, 2.5 kW (0.042 p.u.), is applied to this grid-tied inverter due to the lab limitation, the effectiveness of the proposed FCS-MPC is still validated from the experimental results.

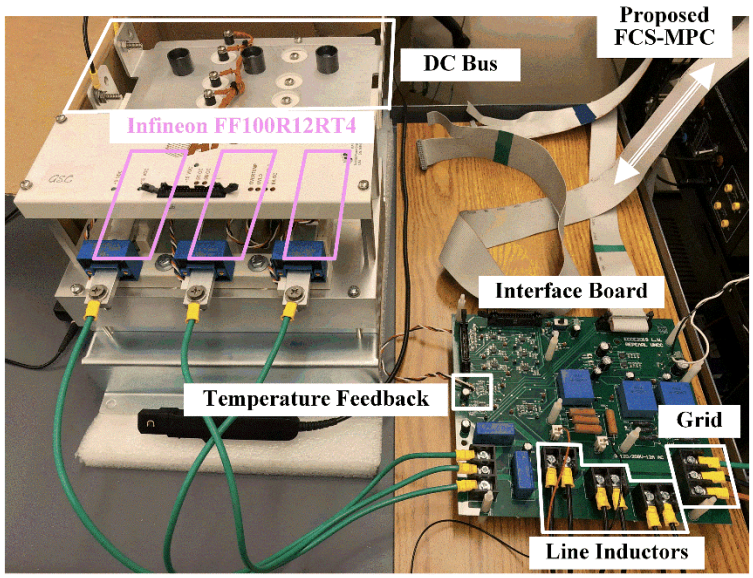


Figure 4.10: The experimental prototype of the grid-tied inverter

TABLE III
PARAMETERS OF THE GRID-TIED INVERTER SYSTEM IN THE EXPERIMENTS

Power P	2.5 kW
Power factor pf	1.0
DC bus voltage V_{dc}	400 V
Grid frequency f	60 Hz
Rated AC grid voltage e_{abc}	80.83/140 V
Line current i_{abc}	11 A
Line inductance L_g	7.8 mH
Line resistance R_g	0.25 Ω
DC bus capacitance C	3300 μF
IGBT module	Infineon FF100R12RT4

Figure 4.9 shows the measured current and voltage waveforms by the conventional FCS-MPC and the proposed FCS-MPC, respectively, where the secondary weighting is fixed at $10 \cdot 10^4$. In Figure 4.9(a) and 4.9(b), the line current i_a and the line voltage e_{ab} are

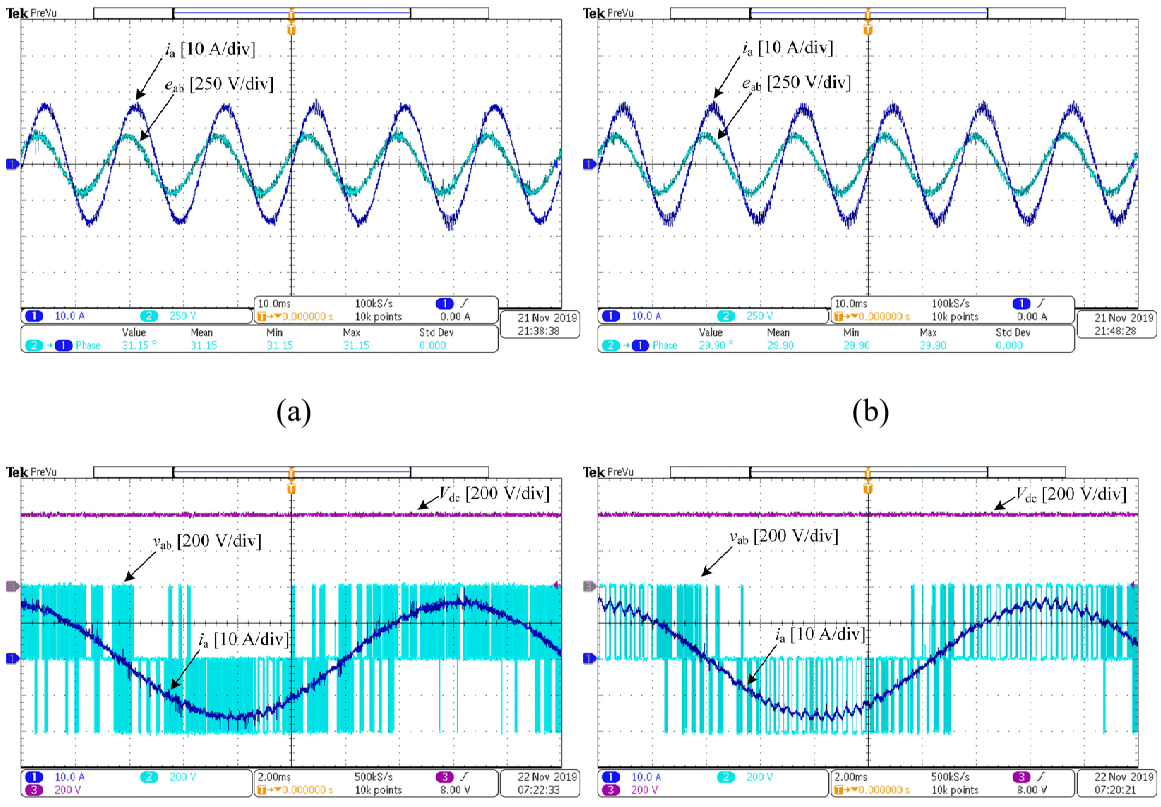


Figure 4.9: Experimental results by the conventional FCS-MPC (left) and the proposed FCS-MPC at $\lambda_s = 10 \cdot 10^4$ (right) including (a) the line current and the line voltage waveforms by the conventional FCS-MPC, (b) the line current and the line voltage waveforms by the proposed FCS-MPC at $\lambda_s = 10 \cdot 10^4$, (c) the DC bus voltage, the line current and the grid-tied inverter output voltage waveforms by the conventional FCS-MPC, and (d) the DC bus voltage, the line current and the grid-tied inverter output voltage waveforms by the proposed FCS-MPC at $\lambda_s = 10 \cdot 10^4$.

presented. It is noted that both the line currents have the same magnitude values around 11 A rms and the similar phase shifts (31.15° by the conventional FCS-MPC and 29.90° by the proposed FCS-MPC) to the line voltage. This verifies that a stable primary problem formulation is maintained in the proposed FCS-MPC, whereas the secondary problem formulation is weighted to $10 \cdot 10^4$.

However, the larger current harmonics are noticed in Figure 4.9(b), which is also seen from Figure 4.9(c) and 4.9(d). In Figure 4.9(c) and 3.8(d), the line current i_a and the grid-tied inverter output voltage v_{ab} are presented. From the output voltage v_{ab}, it is noted that the proposed FCS-MPC contributes to a fewer amount of switching events in the fundamental period and a longer duration time for each switching state, which is dedicated to a reduced power loss by the secondary problem formulation in the proposed FCS-MPC. On the other hand, the line current increases or decreases more in these longer duration times and eventually the current harmonics are increased. A more specific frequency spectrum analysis on the line current is shown in Figure 4.12, where a higher total current harmonics THD is found in the proposed FCS-MPC (5.91%) located at a lower averaged switching frequency around 2.7 kHz, compared with the conventional FCS-MPC (3.64%) at an averaged switching frequency around 3 kHz.

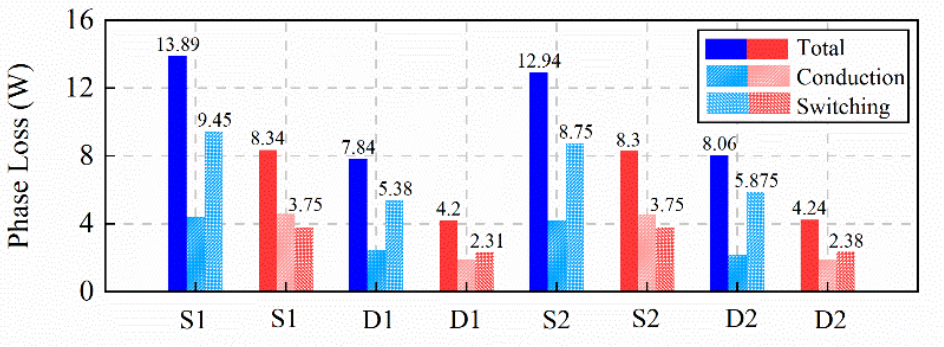


Figure 4.11: The loss breakdown for one phase by the conventional FCS-MPC (blue) and the proposed FCS-MPC at λs = 10·104 (red)

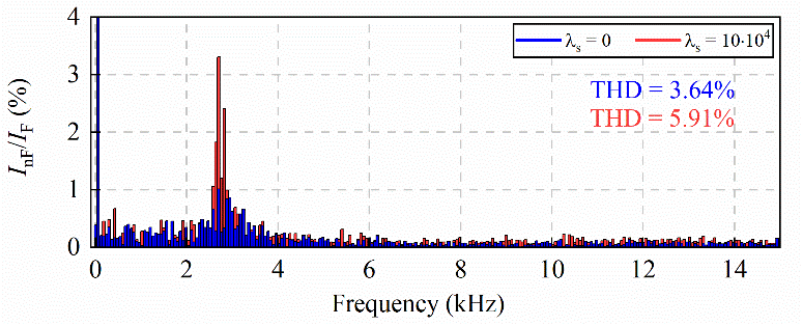


Figure 4.12: Frequency spectrum for the conventional FCS-MPC (blue) and the proposed FCS-MPC at λs = 10·104 (red)

Figure 4.11 shows the loss breakdown for one phase, where the conduction loss is calculated by the periodic average of (4.1) and the switching loss is calculated by the pulse average of (4.2). It is noted that the switching loss is greatly reduced for all semiconductor devices by the proposed FCS-MPC with the secondary weighting $\lambda_s = 10{\cdot}10^4$, whereas the conduction loss is around the similar range. Due to the higher turn-on and turn-off energy loss of the IGBT compared with the ones of the diode, the switching loss of the IGBT is the most reduced (60.3% for S1 and 57.1% for S2). Certainly, the total loss for each semiconductor device is reduced, which verifies the effectiveness of the secondary problem formulation to reduce the power loss in power modules.

The impact of the proposed FCS-MPC on the thermal stress is shown in Figure 4.13, which illustrates the ultimate contribution of the proposed method for the power module thermal stress reduction. Figure 4.13 shows the temperature information including the estimated junction temperatures for one upper switch, and the measured heatsink temperature. A simple heatsink temperature feedback is used as shown in Figure 4.10. Junction temperatures are estimated based on this heatsink temperature and (4.4).

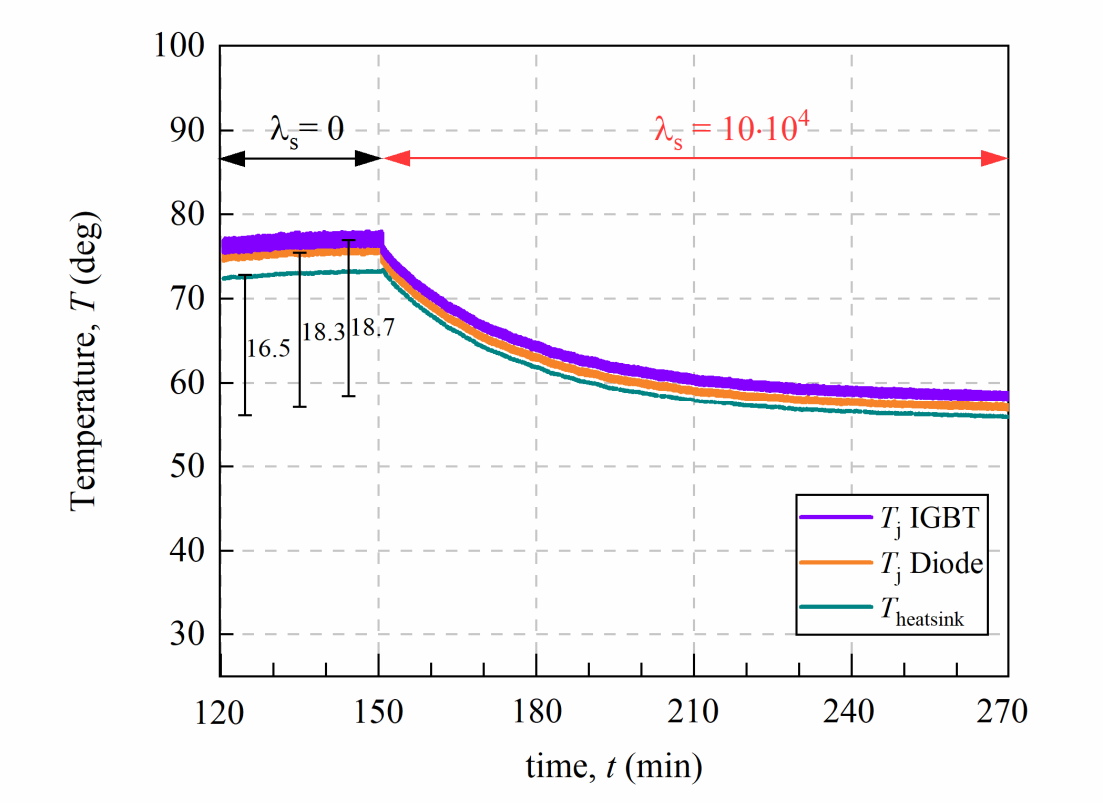


Figure 4.13. The temperature information including the estimated junction temperatures for the IGBT and the diode, respectively, and the measured heatsink temperature.

The proposed FCS-MPC is implemented at 150 mins. Then, immediate temperature drops are noticed in all three values. Due to an extreme low power loading, it takes about two hours for all three values to settle down again. It is noted that estimated junction temperatures for the IGBT and its antiparallel diode are reduced by 18.7 °C (from 77.6 °C to 58.9 °C) and 18.3 °C (from 75.4 °C to 57.1 °C), respectively, whereas the measured heatsink temperature is reduced by 16.5 °C (from 72.5 °C to 56 °C). These temperature reductions are attributed to the power loss reduction shown in Figure 4.11. Then, by applying different power loadings to this grid-tied inverter, multiple temperature reductions will be observed similar to the one shown in Figure 4.12. The long-term temperature mean value and peak-to-peak value will also be reduced effectively, which

contributes to a smoothing thermal cycling in the power module by the proposed FCS-MPC, which significantly relieves the thermal stress to the power module.

4.4.3 Mission Profile Evaluation

A practical mission profile is used to demonstrate the thermal stress reduction by the proposed FCS-MPC. This mission profile is imported from an OCEC reference model which is deployed in Florida, USA [35]. A two-hour time interval is cropped at the most fluctuated period as an example in this mission profile evaluation. Due to the hardware limits, the real-time Hardware-in-the-Loop (HIL) testing is conducted. The OCEC system, the grid-tied inverter and the utility grid are emulated in the real-time simulator. Figure 4.14 shows the imported mission profile according to the acoustic doppler current profile (ADCP). The system parameters are maintained the same as the parameters presented in Table 4.1 and 4.2. The design of the secondary weightings in the proposed FCS-MPC follows the most efficient λ_s curve based on the instantaneous power loading, which is shown in Table 4.4.

TABLE 4.4

SECONDARY WEIGHTINGS BASED ON THE MOST EFFICIENT λ_s CURVE

t (mins)	0-10	10-20	20-30	30-40	40-50	50-60
P (kW)	45.6	55.14	49.2	53.58	54.126	45.42
λ_s (10^4)	4.5	3.1	3.6	3.2	3.1	4.5
t (mins)	60-70	70-80	80-90	90-100	100-110	110-120
P (kW)	8.4	5.13	45.69	46.32	45.87	38.76
λ_s (10^4)	0	0	4.5	4.2	4.4	6.2

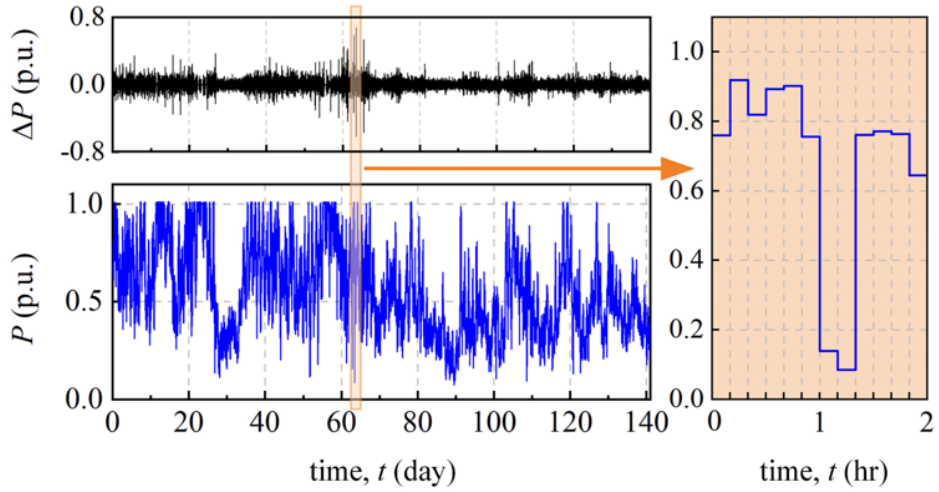


Figure 4.14. The mission profile from an OCEC reference model located in Florida, USA.

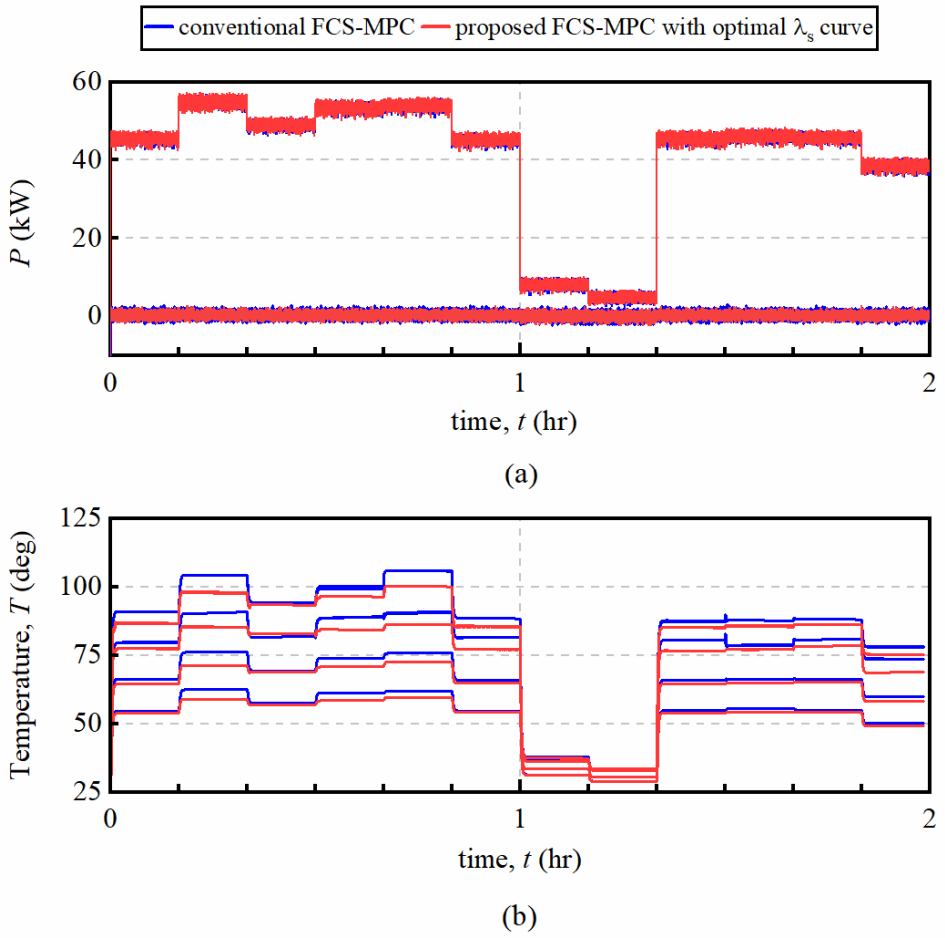


Figure 4.15: Mission profile evaluation by the conventional FCS-MPC (blue) and the proposed FCS-MPC at λs = 10·104 (red)

Figure 4.15(a) shows the instantaneous real and reactive power measured at the grid side, where the proposed FCS-MPC shows a highly identical performance as the conventional FCS-MPC from the overlapped curves. It validates that the proposed FCS-MPC maintains the proper power flow control by using the primary problem formulation. Besides, designing the secondary weighting from the most efficient λ_s curve has a negligible effect on the primary problem performance. It is also noted that the ripple on the instantaneous power from both results shows the similar magnitude level. However, the thermal cycling is significantly optimized in the proposed FCS-MPC. Figure 4.15(b) presents the estimated junction temperatures for one IGBT and its antiparallel diode, the case temperature and the heatsink temperature. First, all temperature values are similar for the power loading less than 0.32 p.u. (60 mins-70 mins, 70 mins-80 mins). This is attributed to the proposed weighting-zones strategy, that the secondary weighting λ_s for the low power loading returns to zero in order to maintain a grid-friendly power quality. Second, for those power loadings greater than 0.32 p.u., the secondary weighting is designed as the most efficient λ_s curve. It is noted that all temperature values are reduced, especially for the full power loading (10 mins-20 mins, 40 mins-50 mins). The proposed FCS-MPC shows a more optimized effect for a higher power loading, observing that a larger temperature reduction happens in those time intervals. With junction temperatures in most time intervals are reduced, the long-term junction temperature mean value and peak-to-peak value over this mission profile are reduced as well. All these results firmly validate the thermal stress reduction by the proposed FCS-MPC.

4.5 Conclusion

A finite control set model predictive control with secondary problem formulation is proposed in this chapter to reduce the power loss of semiconductor devices and then relieve the thermal stress in power modules. By introducing the integrated objective function, it heuristically selects the optimal switching state to achieve a lower power loss while maintaining the normal power flow control. This power loss minimization is estimated from an energy-based loss model as the secondary problem formulation. Compared with other strategies, it eliminates the complicated control loops and modulation schemes. The effectiveness of the proposed FCS-MPC is validated in both simulations and 2.5 kW grid-tied inverter hardware experiments.

The impact of the problem formulation weightings on the system performance is investigated. A power loss reduction rate variation is observed against different secondary weightings. Based on this, a most efficient weighting curve for different power loadings and a weighting-zones strategy for the grid code compliance are presented, which provide engineers with guidelines to design the proposed FCS-MPC. Eventually, the proposed FCS-MPC is evaluated by a practical mission profile from an ocean current energy converter system. The thermal cycling is found to be optimized by achieving junction temperature profiles with a lower mean value and a lower peak-to-peak value, which validates that the thermal stress is relieved in power modules by the proposed FCS-MPC.

CHAPTER 5 CENTRALIZED THERMAL STRESS ORIENTED DISPATCH STRATEGY

In this chapter, a system-level centralized thermal stress oriented dispatch strategy is proposed for multiple DER systems, which reduces the thermal stresses of paralleled grid-connected inverters through the real-time junction temperature variation, the operating and the health conditions of the individual inverter. The switching frequency variation and the reactive power injection are imported separately to this strategy, combining with either conventional PI or FCS-MPC local controller, in order to compare their performance on the thermal stress reduction. Eventually, their impacts on the thermal cycles and the lifetime of power modules will be investigated.

5.1 Introduction of Multiple Paralleled Inverter System

Figure 5.1 shows a typical system diagram of multiple inverters based DER system which consists of paralleled two-level three phases grid-connected inverters (GCIs). These GCIs experience different mission profiles and suffer from different severities of the thermal stress. The thermal profile, including the junction T_j, the case T_c, and the heatsink T_h temperatures of the power module, is normally determined by the power loss of the power converter, the designed thermal management system and the ambient temperature T_a. Conventionally, the power loss is the only degree of freedom to shape the thermal profile during the real-time operation. Hence, in order to reduce the thermal stresses for paralleled GCIs, the power loss of each GCI is changed to shape the real-time thermal profile, where the T_j swing and mean values are expected to be reduced. In the following chapter, the proposed thermal stress oriented dispatch (TSOD) strategy is described step by step to achieve the thermal stress reductions on all GCIs.

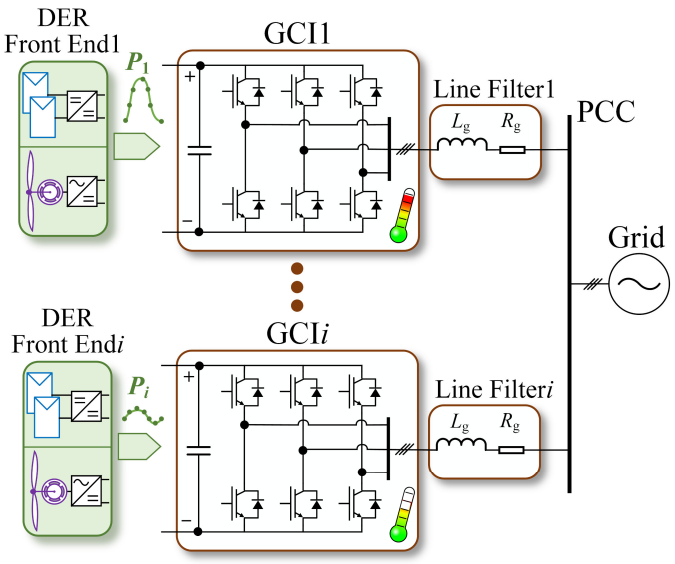


Figure 5.1: System diagram of multiple inverters based DER system.

5.2 Centralized Thermal Stress Oriented Dispatch Strategy

5.2.1 Instantaneous Thermal Stress Identification

First, the instantaneous thermal stress of each GCI is identified. In some of periods of the mission profile (MP), the generated power presents a mild variation, or even no variations. For those periods, GCI may remain its original condition. However, for other periods, where the GCI suffers from a severe thermal stress, the proposed dispatch strategy is enabled to level the power loss and reduce the thermal stress. Hence, several criteria have been defined in following to identify the instantaneous thermal stress of each GCI first,

$$\overline{T_{\mathrm{j,i}}}[k] > UB_{\mathrm{i}} \tag{5.1}$$

$$\left|\Delta\overline{T_{\mathrm{j,i}}}[k]\right| = \left|\overline{T_{\mathrm{j,i}}}[k] - \overline{T_{\mathrm{j,i}}}[k-1]\right| > D_{\mathrm{i}} \tag{5.2}$$

where

$$UB_{\mathrm{i}} = \mathfrak{R} \cdot UB_{\mathrm{i},\ \mathfrak{R}=1} \tag{5.3}$$

$$D_{\mathrm{i}} = \mathfrak{R} \cdot D_{\mathrm{i},\ \mathfrak{R}=1} \tag{5.4}$$

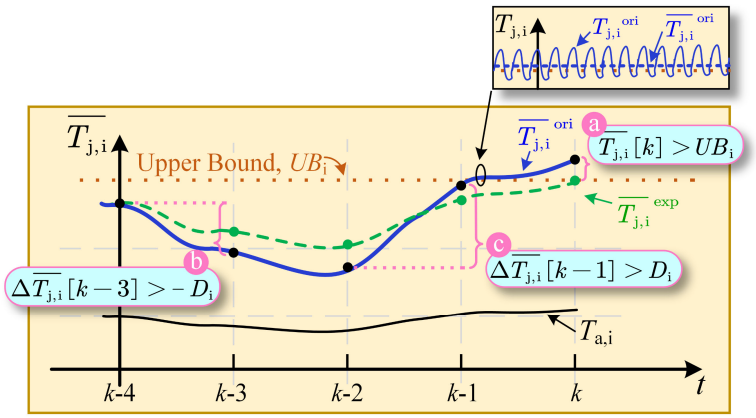


Figure 5.2: Design principles of the proposed centralized TSOD strategy.

i denotes as the *i*th GCI, $\overline{T}_j$ is the mean value of the junction temperature over the fundamental period, which is estimated through the thermal model or indirectly measured through temperature-sensitive electrical parameters [35]. *UB* and *D* are defined as the upper bound and variation borders, respectively. In the proposed strategy, the lower bound border is not defined since it may increase the junction temperature mean value and adversely affect the thermal profile. *UB* and *D* are designed empirically and related to the reliability $\Re$ of the *i*th GCI, where a more degraded GCI is expected to acquire lower *UB* and *D* in order to achieve a milder thermal profile.

Hence, the instantaneous thermal stress is regarded to be severe if (5.1) or (5.2) holds. Figure 5.2 presents the design philosophy of the proposed TSOD strategy. $\overline{T}_{j,i}$, blue in Figure 5.2, is used as the indicator to reflect the real-time thermal profile of the *i*th GCI. At each sampled instant *k*, the instantaneous thermal stress is identified. It turns out that at instants *k*, *k*-1 and *k*-3, the severe thermal stress occurs due to either (5.1) or (5.2) and corresponding situations are labeled by *a*, *b* and *c* in Figure 5.2. In these cases, *i*th GCI will participate into the proposed TSOD strategy for the thermal stress reduction.

5.2.2 Expected Junction Temperature Estimation

For those GCIs participating into the dispatch strategy, their expected junction temperatures $\overline{T_{\mathrm{j,i}}}^{\mathrm{exp}}$ are then estimated. At any instant GCI exceeding either *UB* or *D* border, the proposed strategy would command the GCI to adjust the real-time junction temperature to the expected value in order to eliminate out-of-border periods. Then, the thermal stress will be ideally identified to be non-severe after this adjustment. Obviously, this expected value at least has to comply with criterions (5.1) and (5.2) to keep the GCI away from the severe thermal stress, which is adopted in the proposed strategy as follows,

$$\overline{T_{\mathrm{j,i}}}^{\mathrm{exp}}[k]=\begin{cases} UB_{\mathrm{i}}, & \overline{T_{\mathrm{j,i}}}[k]>UB_{\mathrm{i}} \\ \overline{T_{\mathrm{j,i}}}[k-1]-D_{\mathrm{i}}, & \Delta\overline{T_{\mathrm{j,i}}}[k]<-D_{\mathrm{i}} \\ \overline{T_{\mathrm{j,i}}}[k-1]+D_{\mathrm{i}}, & \Delta\overline{T_{\mathrm{j,i}}}[k]>+D_{\mathrm{i}} \end{cases} \tag{5.5}$$

$\overline{T_{\mathrm{j,i}}}^{\mathrm{exp}}$ is the expected value of the junction temperature profile by proposed TSOD strategy for *i*th GCI in Figure 5.2 in green. It is related to the *UB* and *D* borders from (5.5) because it depends on the way identifying the thermal stress. The expected junction temperature profile in Figure 5.2 clearly presents a milder thermal profile than the one without the proposed TSOD strategy.

5.2.3 Instantaneous Power Loss Identification

Once $\overline{T_{\mathrm{j,i}}}^{\mathrm{exp}}$ is derived, the expected power loss $P_{\mathrm{loss}}{}^{\mathrm{exp}}$ which is the required power loss to generate $\overline{T_{\mathrm{j,i}}}^{\mathrm{exp}}$ needs to be determined. This can be estimated according to the *RC* thermal network of the power module in the designed thermal management system. Usually, a simple heatsink temperature feedback, measured by a low-bandwidth thermocouple or a linear thermal sensor, is calibrated in industrial drives for the temperature monitoring and

overtemperature protection. In the proposed strategy, the real-time heatsink temperature is used to calculate the expected power loss, which is expressed as,

$$P_{\mathrm{loss,i}}^{\mathrm{exp}}[k] = \left(\overline{T_{\mathrm{j,i}}}^{\mathrm{exp}}[k] - T_{\mathrm{h,i}}[k]\right) \Big/ \left(\sum_{\mathrm{l}=1}^{\mathrm{n}} \frac{R_{\mathrm{th,l}}}{\tau_{\mathrm{l}} s + 1}\right) \tag{5.6}$$

where $R_{\mathrm{th,l}}$ and τ_{l} are the thermal resistance and time constant for lth layer of the thermal network. The structure of the thermal network could be different depending on the specific thermal management system. In addition, in the daily or yearly reliability assessment, the thermal capacitance could be ignored since only the steady state of the temperature takes an effect in these time scales, which is discussed in Chapter 5.4.

5.2.4 Dispatch Algorithms

Then, the proposed TSOD strategy derives a new action to force the GCI generating a power loss P_{loss} close to $P_{\mathrm{loss}}^{\mathrm{exp}}$ in order to achieve the expected junction temperature. This is where the local control level thermal stress reduction methods are imported. The power loss of power semiconductor devices, including the conduction loss $P_{\mathrm{loss}}^{\mathrm{cond}}$ and the switching loss $P_{\mathrm{loss}}^{\mathrm{swit}}$, is normally determined by (a) the mission profile, like the real power P and reactive power Q, (b) the operating state of the converter, like the device voltage V_{device} and the conduction current I_{c}, (c) the switching characteristics, like the switching frequency f_{SW} and the gate resistance R_{G}, and (d) the junction temperature T_{j}. However, not all of them can be adjusted from the control level. R_{G} is fixed in most of the industrial drives with no intelligent gate drive circuit. T_{j} is the goal in the proposed strategy and cannot be considered as the input action. P is the generated power from the front-end mechanism and has to be transmitted stably all the time. V_{device} is related to the DC link voltage which is expected to be the nominal value as discussed in Chapter 2. Hence, in the

proposed TSOD strategy, f_{SW} and Q are chosen to be two separate input actions to generate the expected power loss. The specific dispatch algorithms are described below.

1) Switching frequency variation

Adjusting the switching frequency f_{SW} can feasibly control the switching loss during the normal operation and level the power loss over the mission profile. This switching frequency variation (SFV) method is employed as one approach to force the GCI to generate P_{loss}^{exp}.

In order to implement this method, the actual power loss has to be calculated first. Since the mean value of the junction temperature is used as the indictor to reflect the real-time thermal profile, the average power loss over the fundamental period is calculated. The conduction loss of the two-level three phases inverter as shown in Figure 5.1 is calculated below,

$$P_{\mathrm{I}}^{\mathrm{cond}} = \left(\frac{1}{2\pi} + \frac{M\cos\theta}{8}\right) V_{\mathrm{I}} I_{\mathrm{pk}} + \left(\frac{1}{8} + \frac{M\cos\theta}{3\pi}\right) R_{\mathrm{I}} I_{\mathrm{pk}}^2 \tag{5.7}$$

$$P_{\mathrm{D}}^{\mathrm{cond}} = \left(\frac{1}{2\pi} - \frac{M\cos\theta}{8}\right) V_{\mathrm{D}} I_{\mathrm{pk}} + \left(\frac{1}{8} - \frac{M\cos\theta}{3\pi}\right) R_{\mathrm{D}} I_{\mathrm{pk}}^2 \tag{5.8}$$

where $P_{\mathrm{I}}^{\mathrm{cond}}$ and $P_{\mathrm{D}}^{\mathrm{cond}}$ represent the average conduction losses of the IGBT and the antiparallel diode, respectively, M is the modulation index, θ is the phase shift of the grid voltage and the line current, I_{pk} is the magnitude of the current vector. V_{I}, R_{I}, V_{D}, R_{D} are coefficients of the linear relationship of the I-V curve. Then, the switching loss is calculated through the behavioral loss model below,

$$P_{\mathrm{I}}^{\mathrm{swit}} = f_{\mathrm{SW}} \cdot \frac{1}{\pi} \left(E_{\mathrm{on}}(I_{\mathrm{pk}}) + E_{\mathrm{off}}(I_{\mathrm{pk}})\right) \frac{V_{\mathrm{device}}}{V_{\mathrm{rated}}} \tag{5.9}$$

$$P_{\mathrm{D}}^{\mathrm{swit}} = f_{\mathrm{SW}} \cdot \frac{1}{\pi} \left(E_{\mathrm{rec}}(I_{\mathrm{pk}})\right) \frac{V_{\mathrm{device}}}{V_{\mathrm{rated}}} \tag{5.10}$$

where $P_{\mathrm{I}}^{\mathrm{swit}}$ and $P_{\mathrm{D}}^{\mathrm{cond}}$ represent the average switching losses of the IGBT and the antiparallel diode, respectively, E_{on} and E_{off} are turn-on and -off switching energies of the IGBT at the rated voltage V_{rated}. E_{rec} is the reverse recovery energy of the diode. More derivations of (5.7)-(5.10) can refer to [10]. Results of (5.7)-(5.10) are slightly modified according to the junction temperature due to the temperature dependent feature of the power loss.

It is observed that the switching frequency is linearly proportional to the average switching loss from (5.9) and (5.10) and as the input action in the proposed TSOD strategy, it is feasible to generate the expected power loss by only changing the switching frequency, which is a deterministic calculation below,

$$f_{\mathrm{SW,i}}[k] = \begin{cases} f_{\mathrm{SW,i}}[k-1] \cdot F_{\mathrm{i}}, & i \in B \\ f_{\mathrm{SW,i}}[k-1], & i \in G \end{cases} \tag{5.11}$$

$$f_{\mathrm{SW.i}}^{\mathrm{L}} \leqslant f_{\mathrm{SW,i}} \leqslant f_{\mathrm{SW,i}}^{\mathrm{H}} \tag{5.12}$$

where

$$F_{\mathrm{i}} = \frac{P_{\mathrm{I,i}}^{\mathrm{exp}}[k] + P_{\mathrm{D,i}}^{\mathrm{exp}}[k] - P_{\mathrm{I,i}}^{\mathrm{cond}}[k] - P_{\mathrm{D,i}}^{\mathrm{cond}}[k]}{P_{\mathrm{I,i}}^{\mathrm{swit}}[k] + P_{\mathrm{D,i}}^{\mathrm{swit}}[k]} \tag{5.13}$$

$P_{\mathrm{I}}^{\mathrm{exp}}$ and $P_{\mathrm{D}}^{\mathrm{exp}}$ are the expected power losses for the IGBT and the antiparallel diode, respectively. F is the variation ratio of the switching frequency between the expected switching loss and the current switching loss since the conduction loss remains the same. Then, the input action f_{SW} is update by this ratio. B is the set of GCIs participating into the TSOD strategy and G is its complementary set. $f_{\mathrm{SW,i}}^{\mathrm{L}}$ and $f_{\mathrm{SW,i}}^{\mathrm{H}}$ are the lower and higher limits of the switching frequency for ith GCI, which are preset based on the switching speed of the power semiconductor device, the harmonics, and the junction temperature. The result

of (5.11) will be transmitted from the centralized TSOD strategy to the local controller in each dispatch iteration and the modulation scheme in the local controller will adjust the switching frequency as commanded.

2) Reactive power injection

The reactive power Q has validated its influence on the thermal profile in the literature [15], [16]. However, there is not a specific strategy applying the reactive power injection (RPI) method to paralleled grid-connected inverters. This is attributed to the stability and scalability issues of this method. In the proposed centralized TSOD strategy, an optimization problem is formulated to make full use of RPI for paralleled GCIs and maintain the stable operation for the DER system.

Adjusting the reactive power would simultaneously change M, θ, and I_{pk}, which affects both the conduction and switching losses. From (5.7)-(5.10), it is noticed that it is not a simple linear relationship between the reactive power and the power loss. In other words, it can hardly calculate the deterministic reactive power through the expected power loss. In order to eliminate this issue and reduce the online calculation burden, a lookup table is established for each GCI to give a Q-P_{loss} mapping. Then, an optimization problem is defined to calculate the input action Q_{i}, which is shown below,

$$\min_{Q_{\mathrm{i}}} \quad \sum_{i\in B} \frac{\left(P_{\mathrm{loss,i}}(Q_{\mathrm{i}}) - P_{\mathrm{loss,i}}^{\mathrm{exp}}[k]\right)^2}{\left(P_{\mathrm{loss,i}}^{\mathrm{exp}}[k]\right)^2} \tag{5.14}$$

s.t.

$$\sum_{i\in B} Q_{\mathrm{i}} + \sum_{i\in G} Q_{\mathrm{i}} = Q_{\mathrm{g}} \tag{5.15}$$

$$Q_{\mathrm{i}}^{-}[k] \leqslant Q_{\mathrm{i}} \leqslant Q_{\mathrm{i}}^{+}[k] \qquad \text{for } i \in B \tag{5.16}$$

where $P_{loss,i}$ is derived through the lookup table for a certain Q_i. Q_g is the total grid command on the reactive power which has to be maintained all the time. Q_i^- and Q_i^+ confine the feasible range of the candidate reactive power, which depend on the instantaneous mission profile, the inverter output voltage and current limits.

The objective function (5.14) can be solved by enumeration for a small number of GCIs or advanced quadratic programming algorithms, which provides a scalable practical implementation. The result of (5.14) will be transmitted from the centralized TSOD strategy to the local controller in each dispatch iteration and the local PI controller will control the Q of the GCI as commanded.

3) FCS-MPC with reactive power injection

With significant features of the fast dynamic response, the nonlinear system formulation, and the multiple objectives and constraints integration, FCS-MPC has been widely investigated in power electronics systems [22]-[27]. Its capability for the thermal stress reduction is also explored in the local control level [19], [20]. With the further investigation on FCS-MPC, it is found that not only M, θ, and I_{pk} vary with the power flow, but also f_{SW} [21]. Hence, aiming at the FCS-MPC controlled GCIs, the proposed TSOD strategy uses the RPI method to alter M, θ, I_{pk}, and f_{SW} simultaneously and generate P_{loss}^{exp}.

Similar to the reactive power injection for the PI controlled GCI, it is even more difficult to calculate the deterministic reactive power through the expected power loss for FCS-MPC. A new lookup table is built to give a Q-$P_{loss}^{FCS\text{-}MPC}$ mapping. The optimization problem formulation is updated as well,

$$\min_{Q_i} \quad \sum_{i \in B} \frac{\left(P_{loss,i}^{FCS-MPC}(Q_i) - P_{loss,i}^{exp}[k]\right)^2}{\left(P_{loss,i}^{exp}[k]\right)^2} \tag{5.17}$$

where $P_{\text{loss,i}}^{\text{FCS-MPC}}$ is derived through the new lookup table for a certain Q_{i}. The objective function is then replaced by (5.17) and the rest of the problem formulation is the same. The result of (5.17) will be transmitted from the centralized TSOD strategy to the local controller in each dispatch iteration and the local FCS-MPC controller will control the Q of GCI as commanded.

The procedure of the proposed centralized thermal stress oriented dispatch strategy ends up with sending the updated dispatch action to each local controller. Then, each local controller controls the GCI as commanded to generate the expected power loss to reduce the thermal stress. The complete block diagram of the proposed TSOD strategy is shown in Figure 5.3. The flow chart of the centralized TSOD strategy is presented for both PI and FCS-MPC controlled GCIs. The loss and thermal models of power modules are used to estimate the real-time junction temperature locally. The converter information, including the mean value of the junction temperature $\overline{T_{\text{j,i}}}$, the heatsink temperature T_{h}, the real and reactive power P and Q, are collected and transmitted to the centralized TSOD strategy.

A holistic time scale is also presented in Figure 5.3 ranging from microseconds to megaseconds. It shows a comprehensive time scaling frame in the centralized-TSOD-strategy-integrated DER systems. The dispatch period T_{dis} of the proposed TSOD strategy is suggested to be smaller than the time constant of the thermal impedance of power modules, which would interfere the rise or fall of the junction temperature timely, and larger than the fundamental period of the electrical system in order to cover the variation of the instantaneous junction temperature. Besides, the smaller T_{dis} requires more data rate from the communication channel, which is a tradeoff and might be a potential limit. The

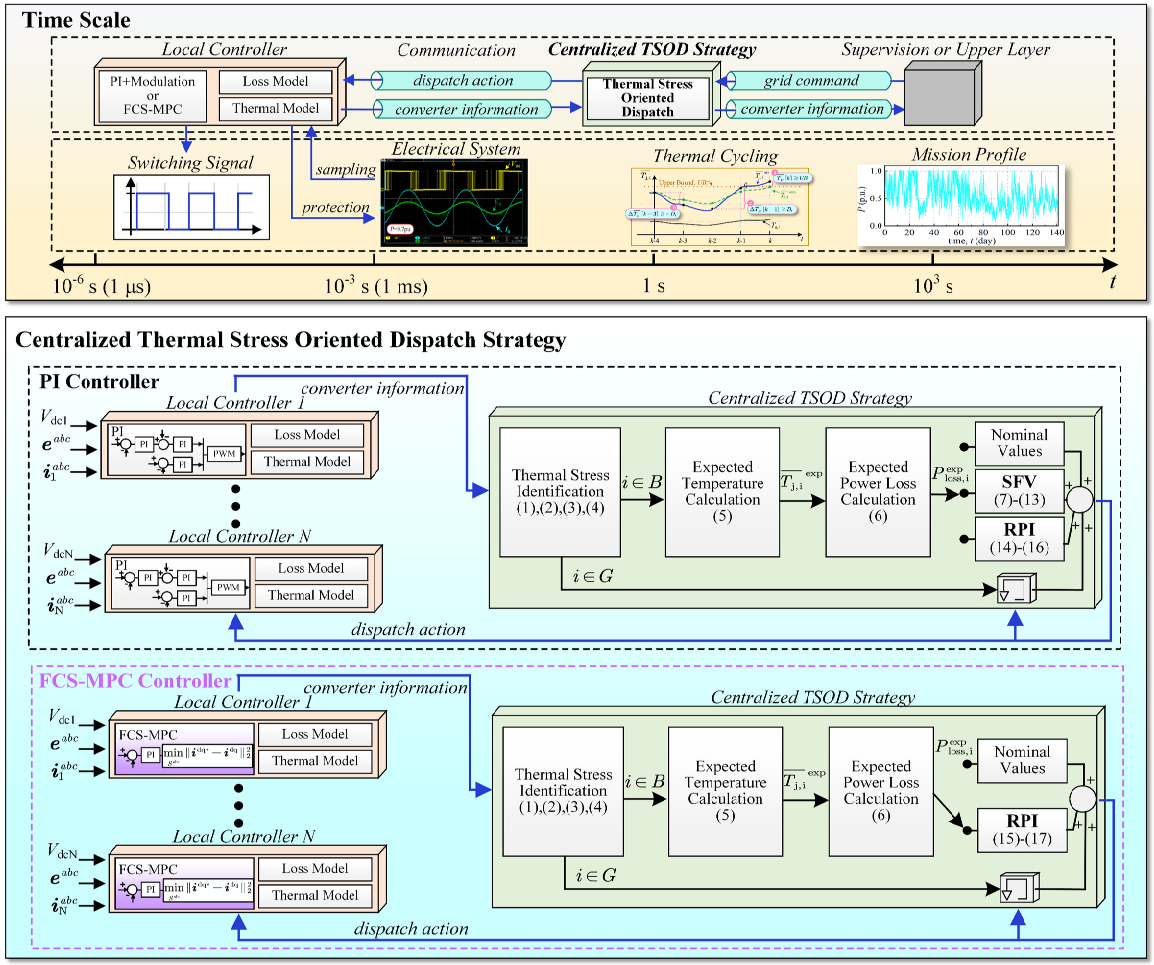


Figure.5.3: System diagram and time frame of the proposed centralized TSOD with different dispatch algorithms for PI and FCS-MPC local controllers.

proposed centralized TSOD strategy is implemented on a four-paralleled-GCIs platform and its performance is evaluated in Chapter 5.3.1 and 5.4.

5.3 Results Validations

5.3.1 Real-Time Simulation Results

To verify the effectiveness of the proposed centralized TSOD strategy, a four-paralleled-GCIs platform is established in the real-time Model-in-the-Loop (MIL) testing. This four-paralleled-GCIs platform is introduced from the reference model of the ocean current energy converter (OCEC) system [28], as shown in Figure 5.4(a). The OCEC system can be planned as the DER system like the wind power. The power electronics systems housing nacelle in Figure 5.4(a) contains four ABB ACS800-17-0790-7 industrial drives in parallel. Each of them is connecting to one electric machine and transmits the power to the point-of-common-coupling (PCC). The circuit diagram on the grid side of the industrial drive is highlighted and displayed in Figure 5.4(b). Six ABB HiPak 5SND 0800M170100 IGBT modules (1700V/800A/125°C) [33] are used for each two-level three-phase GCI. Identical line reactors are connected to all GCIs. The system parameters are listed all in Table 5.1.

Figure 5.5 shows the MIL test platform, which is based on the Opal-RT real-time simulator. PI linear controllers and FCS-MPC controllers are calibrated separately for four GCIs and the same sampling period 50 μs is adopted for both. Other control parameters are listed in Table 5.2. The proposed centralized thermal stress oriented dispatch strategy is built with a one-second dispatch period, where this period is close to 0.7 of the time constant of the thermal impedance. It gives a timely interference before the junction temperature varies beyond the 10°C in the steady state. Other TSOD strategy parameters

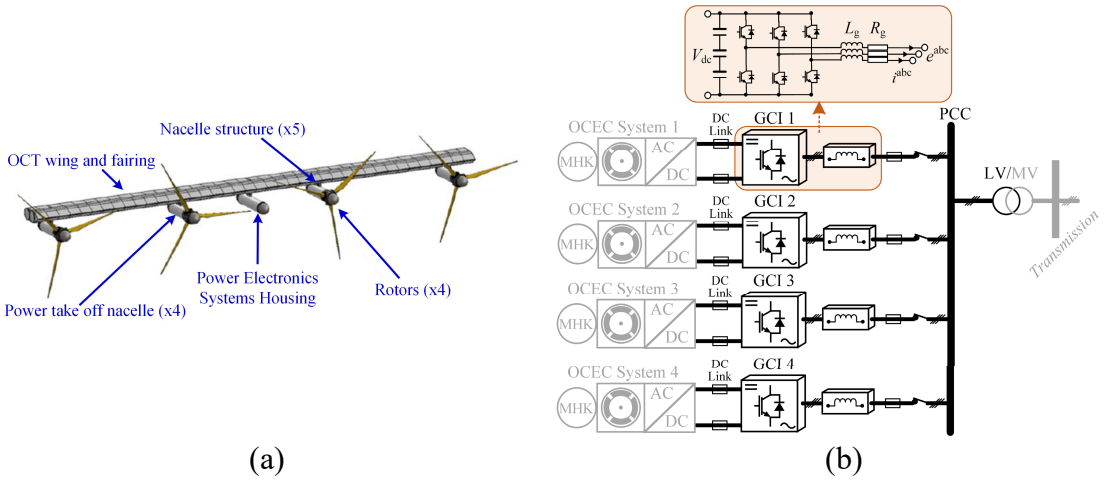


Figure 5.4: Four-paralleled GCIs platform, (a) reference model from [28], (b) circuit diagram.

are listed in Table 5.3. Four yearly mission profiles of the current velocity are imported from moored acoustic doppler current profiles (ADCPs) which are deployed in Gulf Stream, Florida, USA from May 2013 to April 2014 in Figure 5.6 [34]. One-hour data with the 15-minutes interval of these MPs are used to demonstrate the proposed TSOD strategy in the MIL testing. These MPs are translated to the power loadings through the rotor operating characteristics in [28].

Figure 5.7 shows results of the real power and the junction temperatures for four GCIs, where PI linear controllers are used to regulate these GCIs. All dispatch actions calculated from the centralized TSOD strategy are listed in Table 5.4. Dispatch commands are updated twice for both SFV and RPI. When f_{sw} is used as the dispatch command, the reactive power of all GCIs is controlled to be nominal value and vice versa.

Figure 5.7(a), (c), (e), and (g) present the power flow control without and with the TSOD strategy. From the overlapped waveforms, it is noted that the proposed TSOD strategy with either SFV or RPI does not affect the normal real power transmission. DER

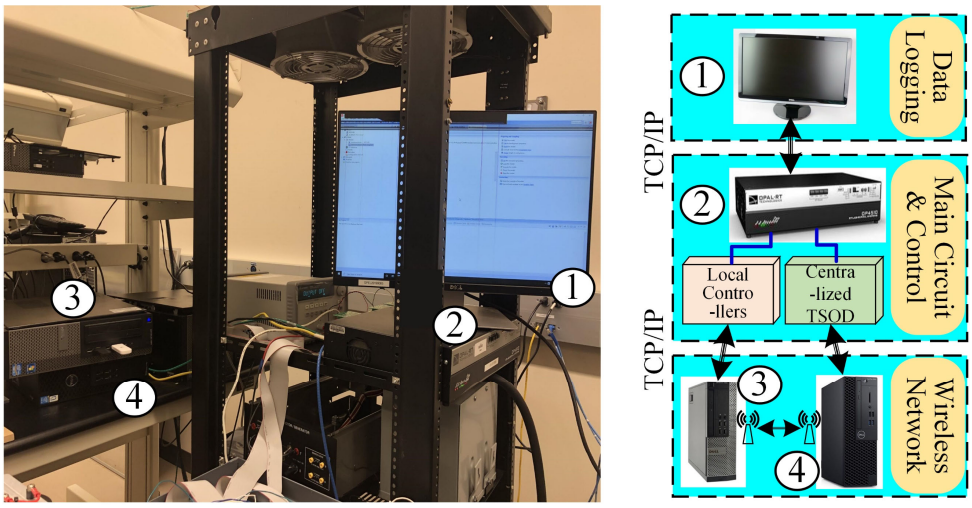


Figure 5.5: Real-time MIL test platform based on RT-Lab.

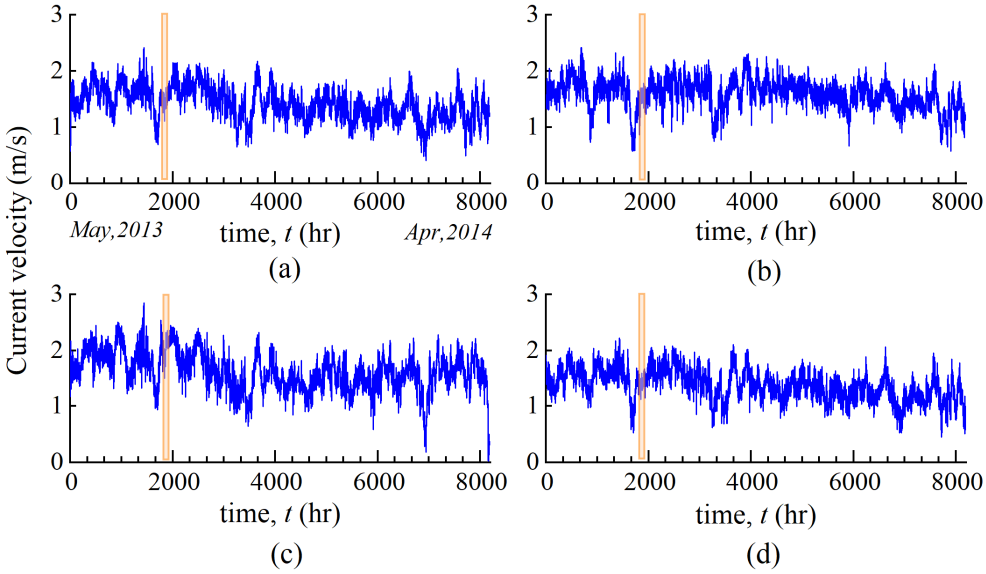


Figure 5.6: Yearly mission profiles of ADCPs in Gulf Stream, Florida, USA.

systems are maintained in the stable condition all the time. Figure 5.7(b), (d), (f), and (h) present the junction temperatures of the IGBTs. From the 15th min, the conventional

TABLE 5.1

PARAMETERS OF ONE POWER CHAIN OF THE OCEC SYSTEM

Rated power P	900 kW/ 1 p.u.
Rated reactive power Q_g	0 kvar
Rated DC bus voltage V_{dc}	1100 V
Grid frequency f	60 Hz
Rated AC grid voltage $\boldsymbol{e}^{abc}$	690 V
Line current $\boldsymbol{i}^{abc}$	753 A
Line inductance L_g	0.4 mH
Line resistance R_g	10 mΩ
Junction temperature T_j	-40~125ºC, 150ºCmax
Air flow	6400 m^3/h
Air temperature T_{air}	25 ºC
IGBT case-heatsink R_{th}	24 K/kW
Diode case-heatsink R_{th}	48 K/kW
Heatsink-ambient R_{th}	20 K/kW

TABLE 5.2

PARAMETERS OF THE LOCAL PI AND FCS-MPC CONTROLLERS

PI Linear Controller	
Sampling period T_s	50 μs
Nominal command Q_i	0 kvar
Nominal f_{SW}	2500 Hz
Switching frequency range	[1000 Hz, 5000 Hz]
FCS-MPC Controller	
Sampling period T_s	50 μs
Prediction receding horizon H	1
Nominal command Q_i	0 kvar

TABLE 5.3

PARAMETERS OF THE PROPOSED CENTRALIZED TSOD STRATEGY

Dispatch period T_{dis}	1 s
Initial reliability $\Re_i$	1
Upper bound border UB_i	125°C
Variation border D_i	5°C

junction temperature experiences a huge fall for all GCIs due to the power dip from MPs. However, with the assistance of the TSOD strategy, the junction temperature is prevented from such huge temperature drop. For TSOD-SFV-PI, the junction temperatures (blue in Figure 5.7) are roughly limited by 10°C-steady-state variation and under 125°C border all the time because of the updated switching loss. For TSOD-RPI-PI, the junction temperatures (green in Figure 5.7) for most GCIs display a smaller drop than the one without the TSOD strategy. However, the temperature profile is not strictly within the 10°C-steady-state variation border as SFV does. This is because that, according to the dispatch algorithm in Chapter 5.2.4, RPI outputs the optimal reactive power by minimizing (5.14), which may not provide the absolute expected power loss from (5.6) and present a compromised performance for most GCIs. The total reactive power is maintained at the grid command Q_g in Figure 5.8.

Figure 5.9 displays the response of the proposed TSOD strategy for GCI1 on the IGBT junction temperature and power loss from 600s to 601.5s, where the real power drops from 450 kW to 270 kW at 600s. At 601s, the TSOD strategy detects the severe thermal stress on GCI1 due to more than 5°C difference from the one at 600s, and then, the updated command (SFV: 3.3-kHz f_{sw} or RPI: 240-kvar Q) is transmitted to GCI1. With the updated command, the new power loss of one IGBT increases from 180 W to 220 W by SFV and to 210 W by RPI and then, the TSOD strategy successfully interferes the junction temperature of GCI1 by preventing from a huge drop.

Figure 5.10(a), (c), (e), and (g) present the power flow control without and with the TSOD strategy. From overlapped waveforms, the real power transmissions in DER systems are also guaranteed all the time for FCS-MPC controlled converters with the

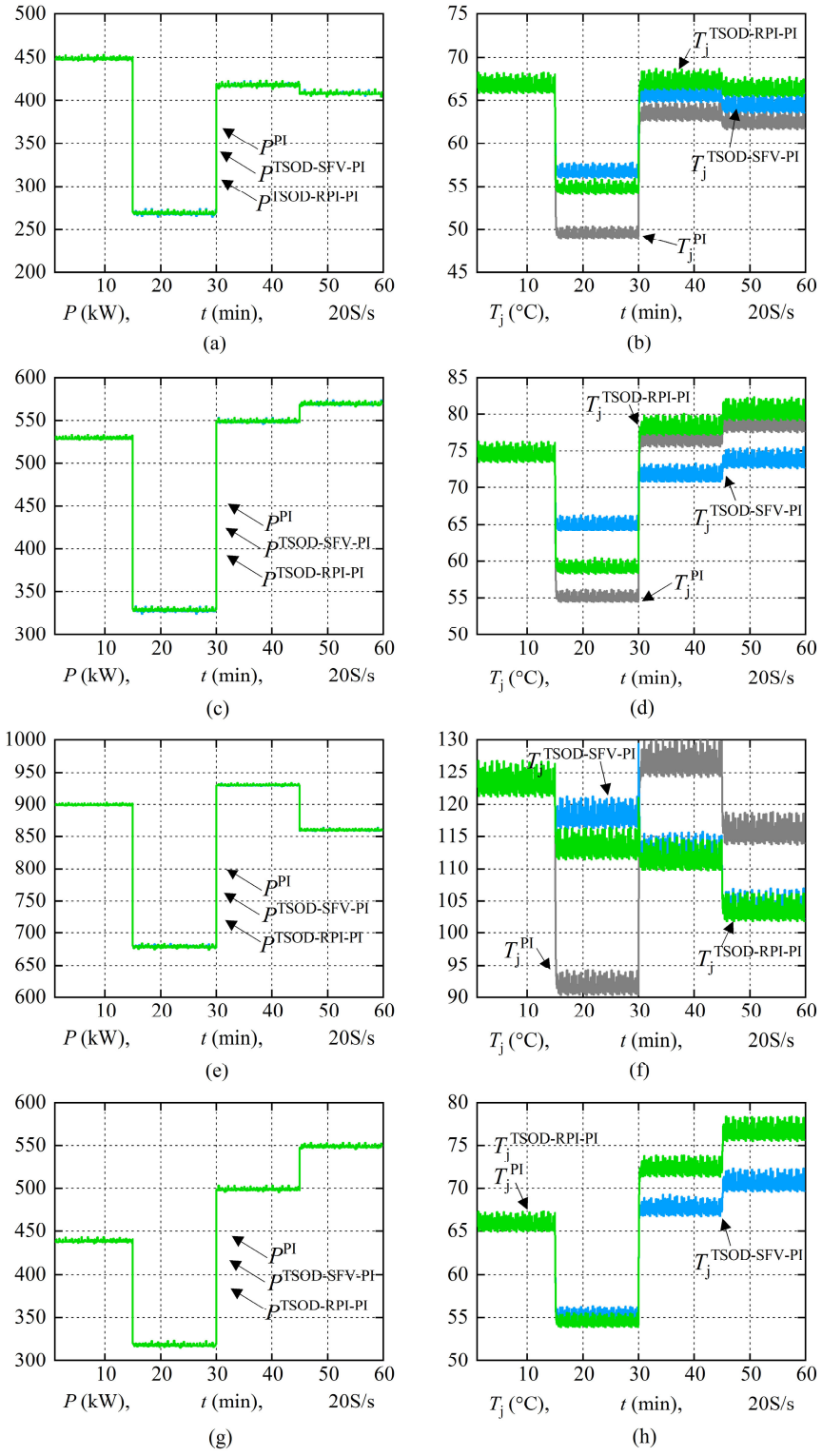


Figure 5.7: MIL results of the power flow (left) and the IGBT junction temperature (right) for PI-controlled (a) and (b) GCI 1, (c) and (d) GCI 2, (e) and (f) GCI 3, (g) and (h) GCI 4.

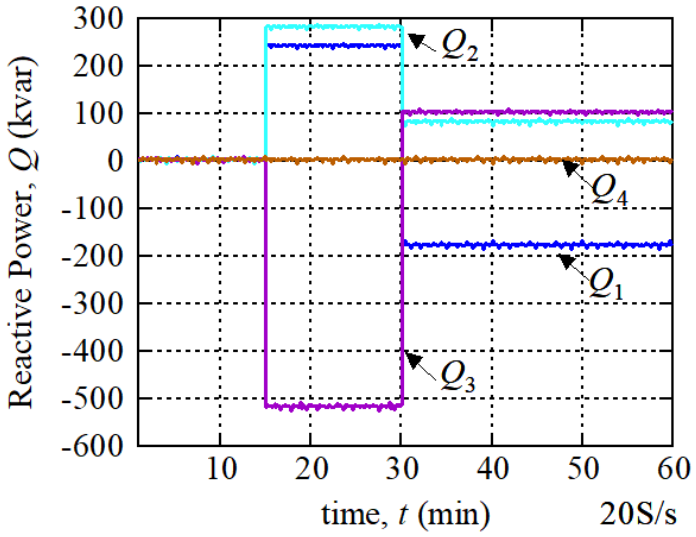
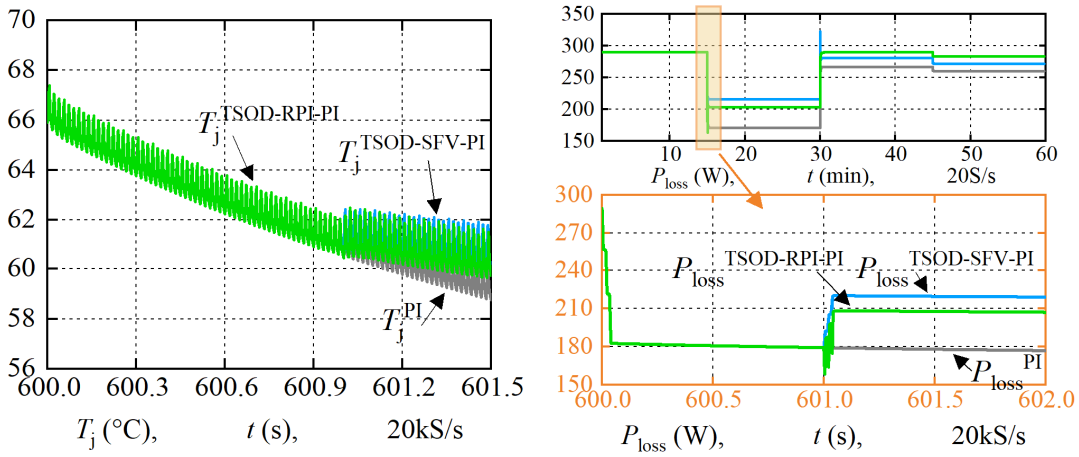


Figure 5.8: Reactive power dispatch commands for PI-controlled GCIs.



(a) (b)

Figure 5.9: Transient response of the proposed centralized TSOD strategy.

TABLE 5.4
DISPATCH COMMANDS FROM THE PROPOSED CENTRALIZED TSOD STRATEGY

	TSOD-SFV-PI, f_{SW} (kHz)		TSOD-RPI-PI, Q (kvar)	
	1st	2nd	1st	2nd
t (s)	601	1201	601	1201
GCI1	3.3	2.6	240	-180
GCI2	3.4	2.2	280	80
GCI3	3.5	2.1	-520	100
GCI4	2.6	2.1	0	0

proposed TSOD strategy. Figure 5.10(b), (d), (f), and (h) present the junction temperatures of the IGBTs. It is observed that with no assistance of the TSOD strategy, the junction temperature results by FCS-MPC controlled GCIs present a slight difference from the ones by PI, which is attributed to the variable switching frequency property of FCS-MPC. Then, with the assistance of the TSOD strategy (purple in Figure 5.10), the junction temperature is further prevented from a huge temperature drop at 15 mins. However, similar with the TSOD-RPI for PI controlled GCIs, the temperature profile is not strictly within the 10°C-steady-state variation border. Besides, the dispatch commands in Table 5.5 are different from the ones in Table 5.4, since in FCS-MPC, the f_{SW} also varies with the operating point of the converter. Hence, the reactive power injection offers more freedoms on the power loss adjustment, whereas the total reactive power is maintained at Q_g as well in Figure. 5.11.

Figure 5.12 displays the response of the proposed TSOD strategy for FCS-MPC controlled GCI1 from 600s to 601.5s. At 601s, the TSOD strategy detects the severe thermal stress of GCI1 again, where both temperature values at 601s and 600s are higher than the ones by PI controlled GCI1, but still beyond the variation border. Then, the updated command (RPI: -150-kvar Q) is transmitted to GCI1. With the updated command, the new power loss of one IGBT increases from 185 W to 215 W and then, the TSOD strategy successfully interferes the junction temperature of GCI1 by preventing from a huge drop.

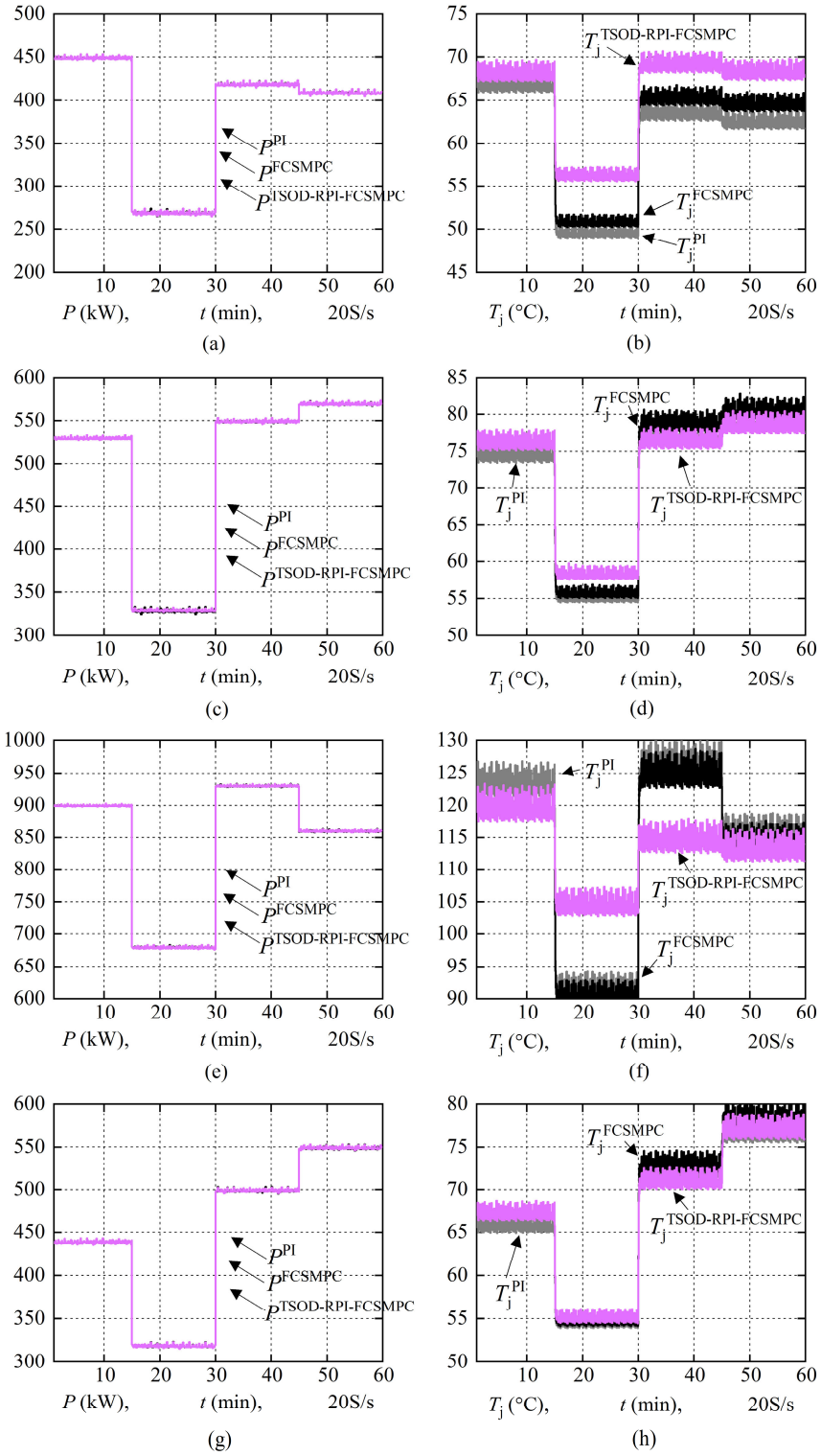


Figure 5.10: MIL results of the power flow (left) and the IGBT junction temperature (right) for FCSMPC-controlled (a) and (b) GCI 1, (c) and (d) GCI 2, (e) and (f) GCI 3, (g) and (h) GCI 4.

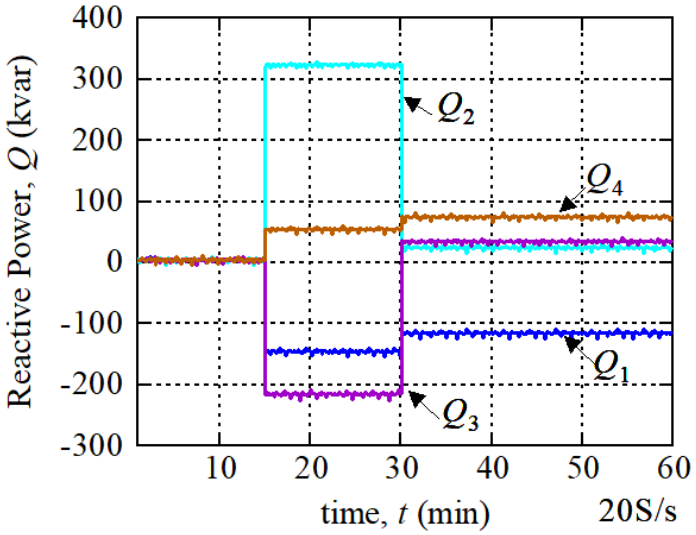
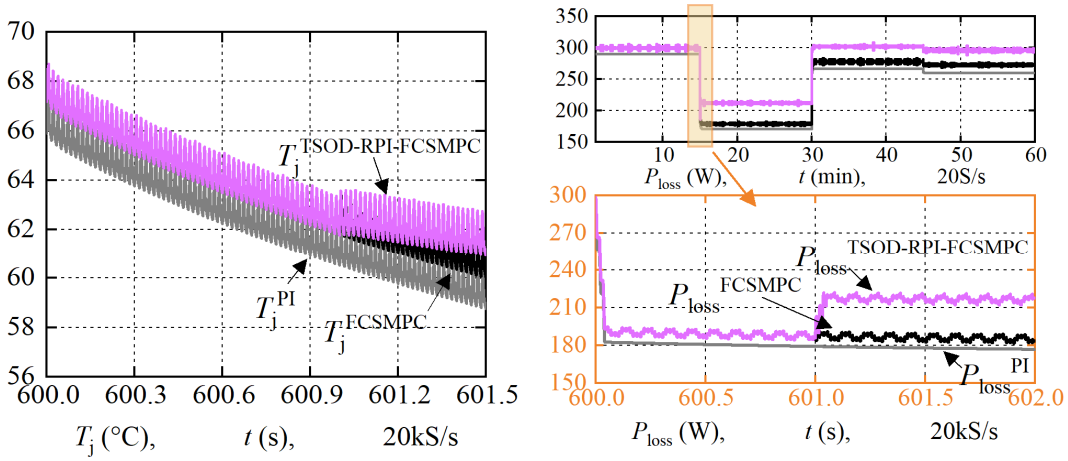


Figure 5.11: Reactive power dispatch commands for FCS-MPC-controlled GCIs.



(a) (b)

Figure 5.12: Transient response of the proposed centralized TSOD strategy.

TABLE 5.5
DISPATCH COMMANDS FROM THE PROPOSED CENTRALIZED TSOD STRATEGY

	TSOD-RPI-FCSMPC, Q (kvar)	
	1st	2nd
t (s)	601	1201
GCI1	-150	-120
GCI2	320	20
GCI3	-220	30
GCI4	50	70

From all MIL results, it is clearly illustrated that the junction temperature is prevented from decreasing to a very low value by proposed centralized TSOD strategy for both PI and FCS-MPC controlled GCIs. A more balanced power loss is achieved for all paralleled inverters by updating the dispatch commands, either f_{SW} or Q. Further verification of the thermal stress reduction will be presented in the next section.

5.3.2 Experimental Results

A digital twin hardware platform is developed in Figure 5.13 to validate the effectiveness of the proposed centralized TSOD strategy as well. It contains a physical object (PO) of a down-scale grid-connected inverter and a virtual object (VO) of the identical inverter in parallel. PO and VO share the grid voltage $\boldsymbol{e}^{abc}$ and the measured heatsink temperature T_h in the real-time operation. Local PI and FCS-MPC controllers are calibrated separately. PI controller uses the fixed switching frequency at 8 kHz which is designed to be the mean value of the variable switching frequency results of FCS-MPC [21]. All experimental parameters are presented in Table 5.6 and 5.7, including the inverter, the local controllers and the designed TSOD strategy. The variation border D_i is set to be 3.5°C at every 1-s dispatch period, which limits a 10°C variation in the temperature steady state. The similar varying mission profiles from Figure 5.14 are loaded on PO and VO simultaneously. The proposed centralized TSOD strategy is applied at 26 min.

Figure 5.15 displays the dispatch action results of TSOD-SFV-PI, TSOD-RPI-PI, and TSOD-RPI-FCSMPC, respectively. It is noted that all dispatch algorithms take effects in experiments. For SFV in Figure 5.15(a), the switching frequency value varies within the range between 5 kHz and 10 kHz. For RPI in Figure 5.15(b) and (c), the proposed TSOD

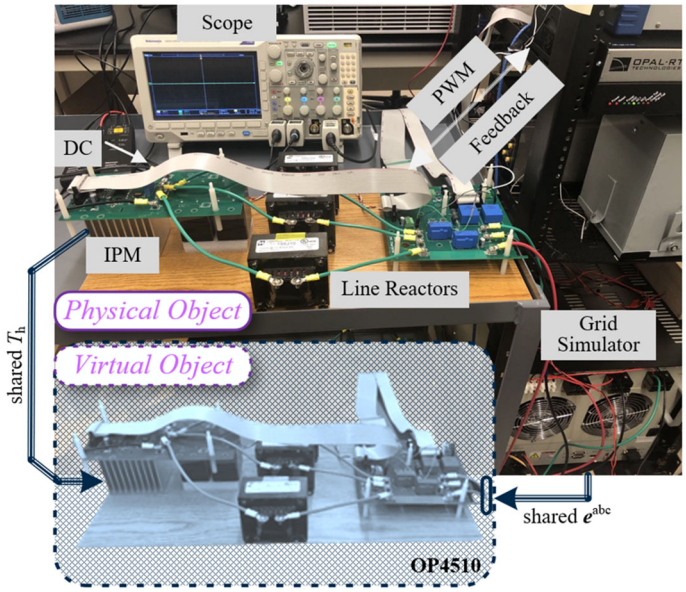


Figure 5.13: Digital twin hardware platform for the experimental testing.

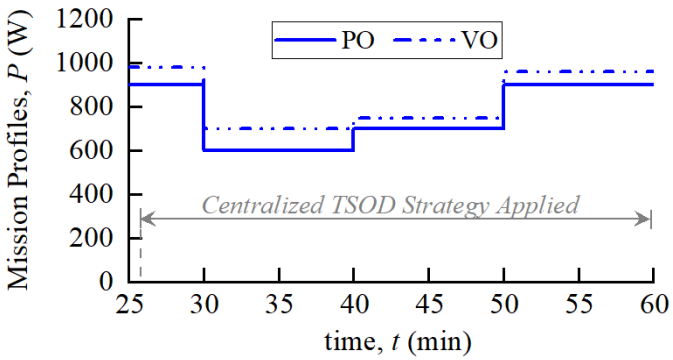


Figure 5.14: The 30-minutes mission profiles for the hardware platform.

TABLE 5.6

PARAMETERS OF THE GCI IN THE EXPERIMENTS FOR BOTH PO AND VO

Rated power S	1.4 kVA/ 1 p.u.
Rated DC bus voltage V_{dc}	200 V
Grid frequency f	60 Hz
Rated AC grid voltage $\boldsymbol{e}^{abc}$	46.2/80 V
Line Reactors L_g R_g	8 mH, 0.3 Ω
IGBT module	Infineon IKCM15L60GD [36]
Sampling period T_s	25 µs

TABLE 5.7

PARAMETERS OF THE LOCAL CONTROLLERS AND TSOD STRATEGY

PI Linear Controller	
Nominal command Q_i	0 var
Nominal f_{SW}	8000 Hz
Switching frequency range	[5000 Hz, 10000 Hz]
FCS-MPC Controller	
Prediction receding horizon H	1
Nominal command Q_i	0 var
Centralized TSOD Strategy	
Dispatch period T_{dis}	1 s
Initial reliability $\Re_i$	1
Upper bound border UB_i	100°C
Variation border D_i	3.5°C

strategy stably maintains the total reactive power at zero all the time for PO and VO and limits their power flow within the rated design 1.4 kVA. Figure 5.16 and 5.17 show the estimated IGBT losses under dispatch actions for PI controlled and FCS-MPC controlled GCIs, respectively. All IGBT losses with the proposed TSOD strategy are more balanced than the one without the TSOD strategy, even though at some time intervals the IGBT losses may be found higher than the highest value or lower than the lowest value of the conventional PI or FCS-MPC results. This is highly acceptable because the temperature

transient response is much slower than the electrical transient response. In other words, it sufficiently validates that the proposed centralized TSOD strategy interferes the rise or fall of the temperature timely.

Eventually, Figure 5.18 and 5.19 present the thermal profile results of PO, where the estimated junction temperatures of the IGBT T_j, the estimated and the measured case temperatures of the power module, T_{cest} and T_{cmea}, are shown. The estimated values come from the thermal model in the local controllers and a heatsink temperature feedback. It is observed that with the TSOD strategy, junction temperatures have less variations compared to the one without the TSOD strategy, and variation limits are around 10°C as designed. The overall junction temperature differences are 13.4°C for TSOD-SFV-PI (blue), 9.7°C for TSOD-RPI-PI (green) compared to 18.0°C for PI (gray) in Figure 5.18, and are 12.5°C for TSOD-RPI-FCSMPC (purple) compared to 14.8°C for FCSMPC (yellow) in Figure 5.19. Besides, TSOD-SFV-PI has a stronger response to the upper bound border from 26 min to 30 min and from 52 min to 60 min, where the switching frequency gradually changes, from 8 kHz to 5 kHz and from 9.6 kHz to 6.9 kHz, respectively, as shown in Figure 5.15(a), in order to prevent the junction temperature from exceeding the border value 100°C. The high consistency of the estimated and measured case temperatures in both Figure 5.18 and 5.19 strengthens the accuracy and the authenticity of the conclusions from the above junction temperatures. Thus, the proposed centralized TSOD strategy has demonstrated its performance on the thermal stress reduction by reducing the swing value of junction temperatures in the experiments.

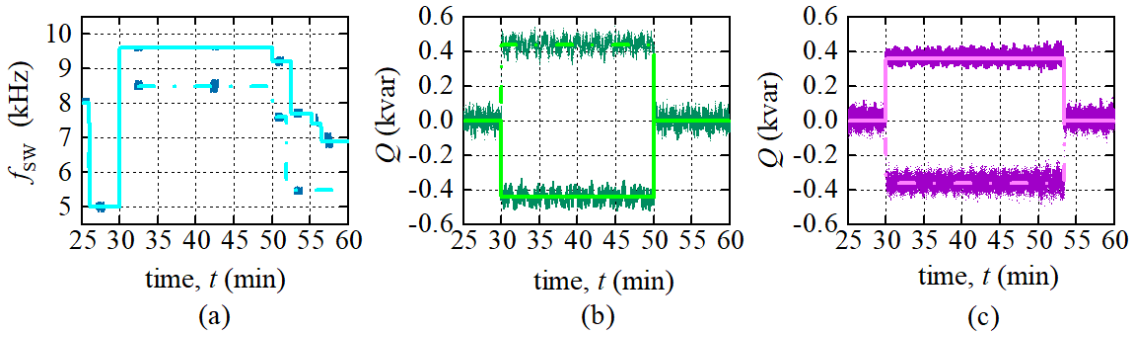


Figure 5.15: Dispatch actions of the centralized TSOD strategy for PO (solid line) and VO (dash line), (a), TSOD-SFV-PI, (b), TSOD-RPI-PI, (c) TSOD-RPI-FCSMPC.

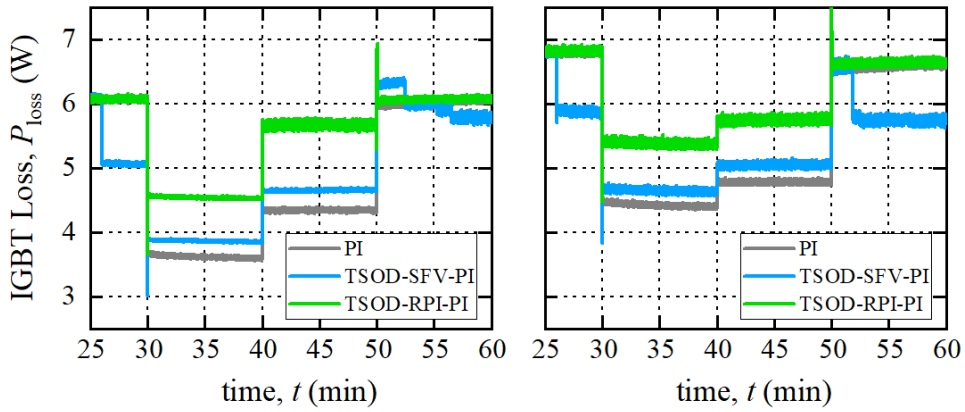


Figure 5.16: IGBT loss for PO (left) and VO (right) with local PI controller.

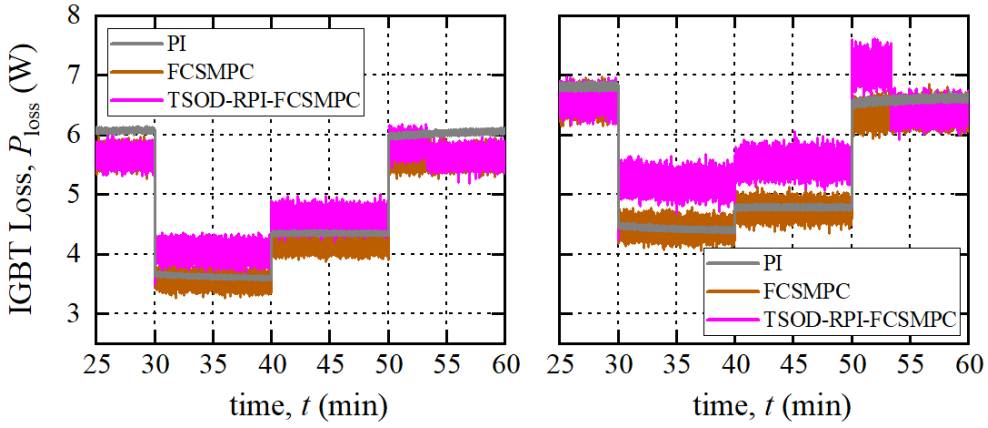


Figure 5.17: IGBT loss for PO (left) and VO (right) with FCS-MPC controller.

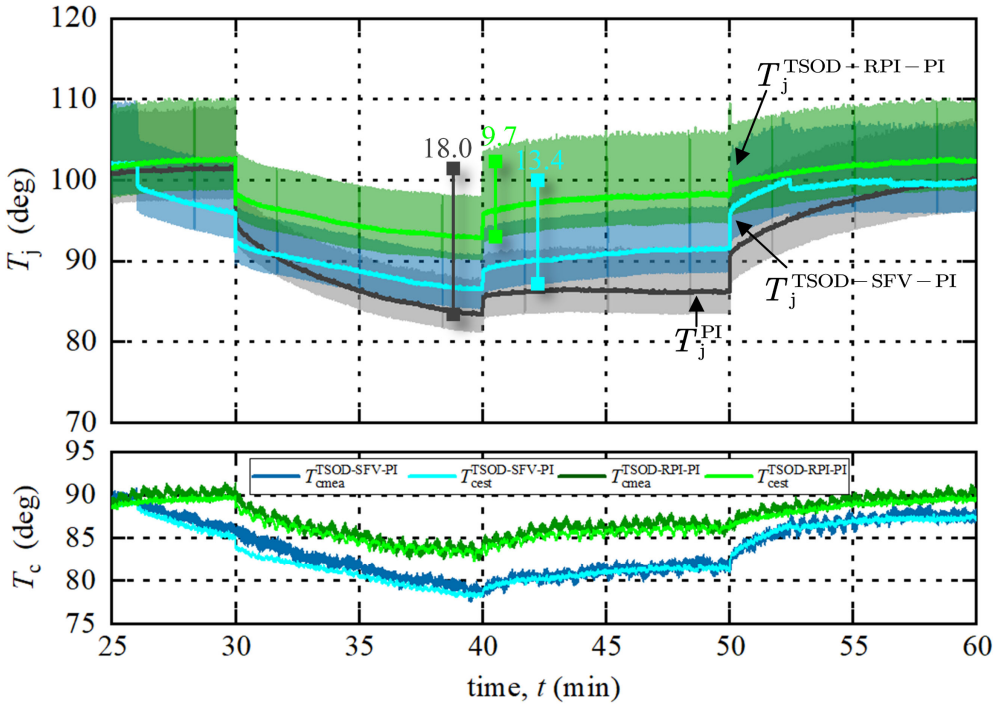


Figure 5.18: Estimated junction, estimated and measured case temperatures of PO with local PI controller for PI (gray), TSOD-SFV-PI (blue), and TSOD-RPI-PI (green).

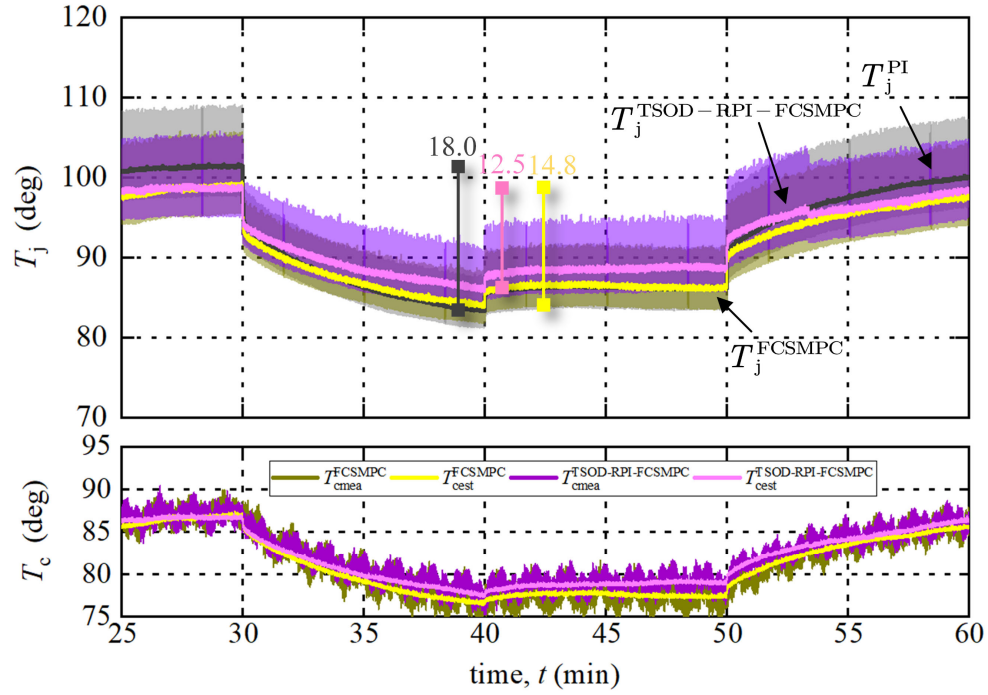


Figure 5.19: Estimated junction, estimated and measured case temperatures of PO with local FCS-MPC controller for FCSMPC (yellow) and TSOD-RPI-FCSMPC (purple).

5.4 Reliability Assessment

In order to further verify the effectiveness of the thermal stress reduction, investigate the impact of the proposed TSOD strategy on the lifetime and reliability of IGBTs, and compare different performance between PI and FCS-MPC local controllers, the reliability assessment and the tradeoff analysis are conducted in this section.

The yearly mission profiles from Figure 5.6 are adopted for the same four-paralleled-GCIs platform. Because the reliability assessment is a long-term profile investigation, the short-term responses including the transient states on the DC link voltage and the line currents, the thermal capacitance, and the small time step are reasonably ignored [2]. The identical parameters of the DER systems, the local controllers, and the proposed centralized TSOD strategy from Table 5.1, 5.2, and 5.3 are used in the reliability assessment. Specific results are presented below in terms of the thermal profile, the thermal cycles, and the accumulative damage and predicted lifetime of IGBTs.

5.4.1 Yearly Thermal Profile

Applying the proposed thermal stress oriented dispatch strategy to the yearly mission profiles derives the yearly thermal profiles. Figure 5.20 presents the yearly junction temperature profiles of IGBT in GCI1, where the results of PI controlled GCI1 are displayed in Figure 5.20(a) and (b) and results of FCS-MPC controlled GCI1 are displayed in Figure 5.20(c). It is observed that with the proposed TSOD strategy, the thermal profiles are all shaped in order to reduce the thermal stress.

Figure 5.20(a) presents the yearly thermal profile by PI and TSOD-SFV-PI. Compared with the conventional profile, the shaped thermal profile achieves a lower junction temperature for most high power loading instants. In some of low power loading

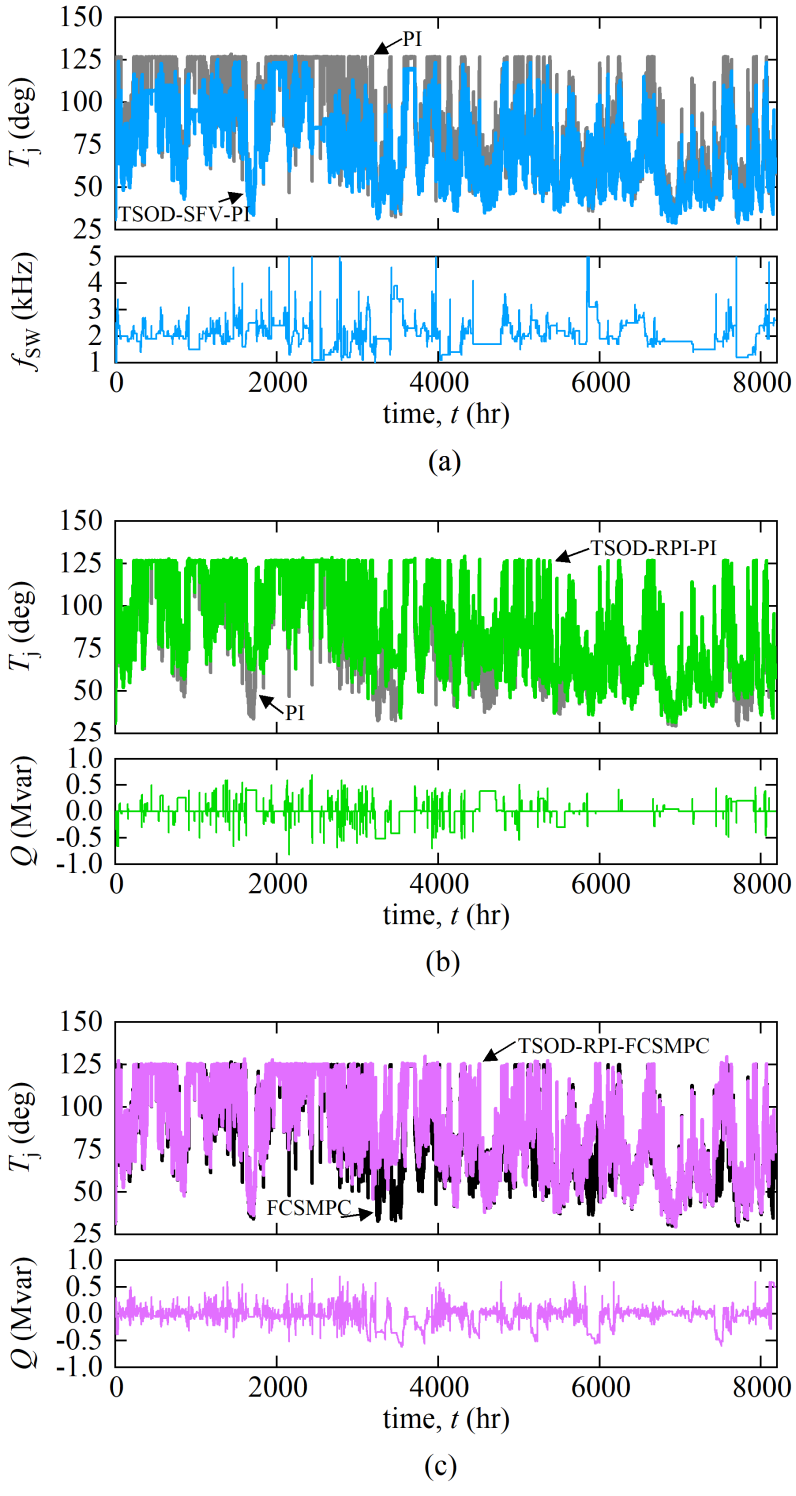


Figure 5.20: Yearly thermal profiles by reliability assessment for (a) PI and TSOD-SFV-PI, (b) PI and TSOD-RPI-PI, and (c) FCSMPC and TSOD-RPI-FCSMPC.

instants, the junction temperature also increases in order to reduce the swing value in the thermal cycling. This is attributed to the switching frequency variation in the PI controller, that the switching loss can be adjusted higher or lower in any direction.

Figure 5.20(b) presents the yearly thermal profile by PI and TSOD-RPI-PI. Compared with the conventional profile, the shaped thermal profile achieves a higher junction temperature for most low power loading instants and the same temperature level for the high power loading instants. This is attributed to the lowest power loss at zero reactive power in the PI controller, that the power loss can only be adjusted to a higher level. Hence, the junction temperature swing value has been reduced by increasing the low level of the thermal profile, and the mean value has been sacrificed in return. Similar case happens to Figure 5.20(c) by TSOD-RPI-FCSMPC. However, since the f_{SW} varies with the reactive power, FCS-MPC provides more flexibilities on the power loss adjustment, where the lowest power loss may not be at zero reactive power operating point. Thus, the thermal profile by TSOD-RPI-FCSMPC is different from the one by TSOD-RPI-PI from Figure 5.20.

5.4.2 Thermal Cycles Counting

Once receiving all thermal profiles for four GCIs, the rainflow counting algorithm, which is a widely used counting method in the fatigue study, is employed to discretize the thermal profile in terms of the junction temperature mean value $\overline{T_{\mathrm{j}}}$, the swing value ΔT_{j}, and the cycling period t_{cycle}, which later are fit into the IGBT lifetime prediction model.

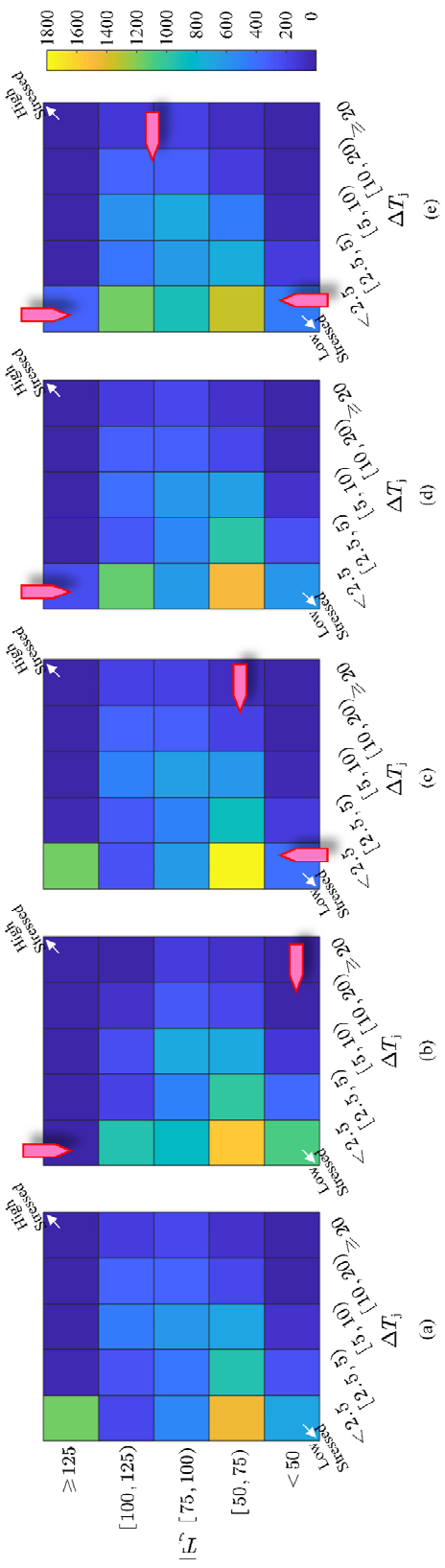


Figure 5.21: Thermal cycles counting results for (a) PI, (b) TSOD-SFV-PI, (c) TSOD-RPI-PI, (d) FCSMPC, and (e) TSOD-RPI-FCSMPC.

Figure 5.21 displays the rainflow counting results from thermal profiles in Figure 5.20 for GCI1. The colormap reflects the number of the thermal cycles based on two variables, the temperature mean value (Y axis) and swing value (X axis). The red arrow reflects the shift direction of thermal cycles compared to the one by PI controlled GCI without the proposed TSOD strategy. Figure 5.21(b) shows the colormap for TSOD-SFV-PI, where more cycles exist in the lower-mean-value and lower-swing-value squares. The number of cycles beyond criterions (1) and (2) is significantly reduced. Figure 5.21(c) shows the colormap for TSOD-RPI-PI, where more cycles exist in the higher-mean-value and lower-swing-value squares. This is compliant with the thermal profile in Figure 5.20(b), that the temperature swing value has been reduced by increasing the low level of the thermal profile, and the mean value has been sacrificed in return. Figure 5.21(d) and (e) display the colormaps for the FCS-MPC and TSOD-RPI-FCSMPC. Without the assistance of TSOD strategy, Figure 5.21(d) illustrates more moderate thermal cycles than Figure 5.21(a), where more cycles are located in the lower-mean-value squares. With TSOD strategy in Figure 5.21(e), more cycles move to the lower-swing-value squares.

From the comparison between these colormaps, more thermal cycles are located in the lower-mean-value and lower-swing-value squares by proposed TSOD strategy, which contributes to a reduced thermal stress on IGBTs. An FCS-MPC controlled GCI performs a more mitigated thermal stress than the one by PI, even if no TSOD strategy is engaged.

5.4.3 Accumulative Damage and Lifetime Prediction

A more straightforward comparison comes from the accumulative damage and predicted lifetime on the IGBTs. Particularly for those TSOD-RPI results, where more thermal cycles exist in the higher-mean-value and lower-swing-value squares, the

quantified results can give an intuitive judgment on whether the thermal stress is indeed reduced by proposed TSOD strategy. Hence, the Bayerer's IGBT lifetime model [29] and Miner's rule [30] are used to calculate the accumulative damage (AD) and the predicted lifetime based on the thermal cycles counting results,

$$N_{\mathrm{f}} = A(\Delta T_{\mathrm{j}}^{-\beta_1}) \cdot \exp\left(\frac{\beta_2}{\overline{T}_{\mathrm{j}} + 273}\right) {t_{\mathrm{cycle}}}^{\beta_3} I^{\beta_4} V^{\beta_5} D^{\beta_6} \tag{5.18}$$

$$\mathrm{AD} = \sum_i \frac{n_i}{N_{\mathrm{f},i}} \tag{5.19}$$

where N_{f} is defined as the number of cycles to failure for the specific thermal stress ($\overline{T}_{\mathrm{j}}$, ΔT_{j}, t_{cycle}), n_{i} is the number of this thermal stress, I is the current per wire bond, V is the voltage class, and D is the diameter of the bond wire. Parameters A and $\beta_{1\text{-}6}$ are device dependent constants according to the aging data provided by manufacturers [31]. The lifetime prediction is calculated by reciprocal of AD. When AD goes to one, the device is regarded to be fully failure out.

Figure 5.22 presents ADs by mission profiles in Figure 5.6 and predicted lifetimes of the IGBT for all four GCIs. The lifetime of the IGBT by PI-controlled GCIs without the proposed TSOD strategy is set to be around 10 years as the benchmark. It is clearly shown that the IGBTs in almost all GCIs achieve the less accumulative damage and the more predicted lifetime with the proposed TSOD strategy. Among all, TSOD-SFV-PI gives the least ADs and the longest lifetime of 13~15 years for all GCIs. Without the TSOD strategy, FCS-MPC controlled GCIs perform slightly longer lifetime of 10~11 years than the ones by PI controlled GCIs. TSOD-RPI-FCSMPC performs even better. It is acknowledged that the accuracy of the IGBT lifetime model has been an open topic, which can be validated

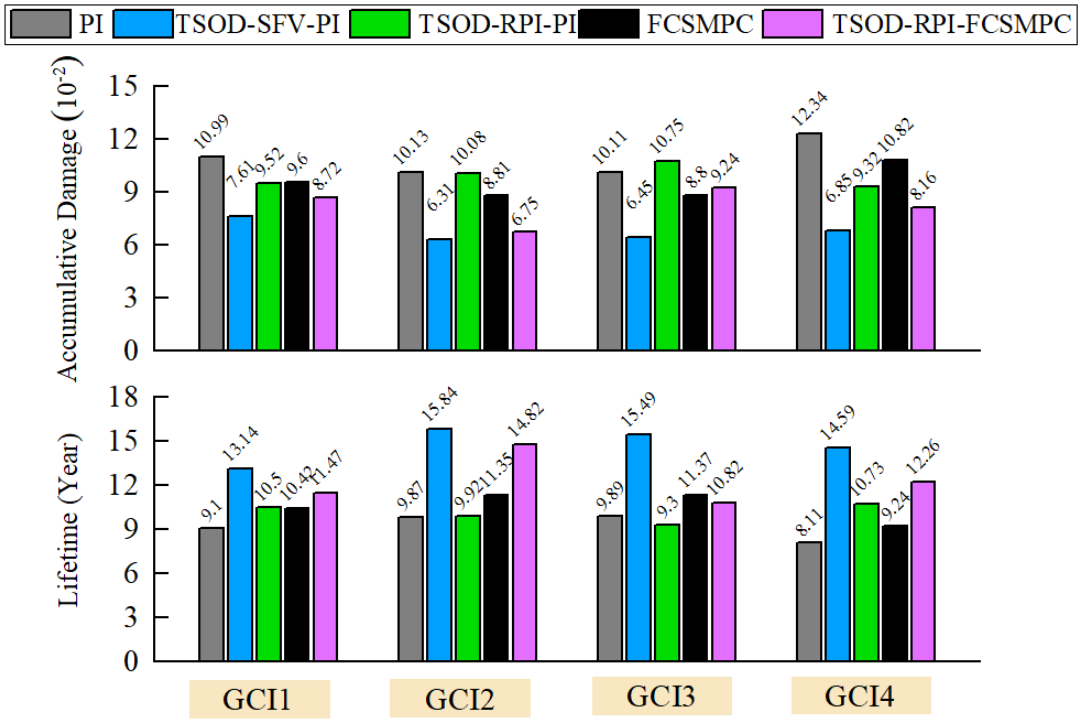


Figure 5.22: Accumulative damages and predicted lifetimes for all GCIs.

through power cycling acceleration tests in the laboratory. However, in this study, the relative changes on the AD and the lifetime are more of the interest and solid to verify the effectiveness of the proposed TSOD strategy and compare different methods.

5.4.4 Tradeoff Analysis

Since the essential idea of the proposed TSOD strategy is to balance the power loss for the thermal stress reduction, the annual energy production and the system efficiency are affected if the TSOD strategy engages. Table 5.8 lists the annual energy productions for all four GCIs and the total platform system efficiency. The benchmark of the system efficiency is set to be 98%-max value at 770 kW with nominal Q and f_{SW} values [32]. It is noted that the TSOD-SFV-PI method contributes to the largest annual energy productions (total in 21,141 MWh) and the highest efficiency (98.10%), which are attributed to the lower power loss by decreasing the switching frequency. Without the proposed TSOD

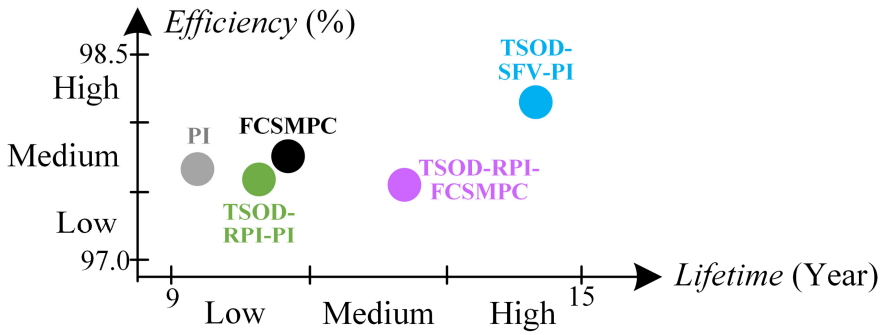


Figure 5.23: Lifetime and efficiency comparison between different methods.

TABLE 5.8

ANNUAL ENERGY PRODUCTIONS AND TOTAL PLATFORM EFFICIENCY

	Annual Energy Productions (MWh)				η(%)
Method	GCI1	GCI2	GCI3	GCI4	Total
PI	4683	6043	5919	4398	97.65
TSOD-SFV-PI	4702	6073	5950	4416	98.10
TSOD-RPI-PI	4677	6043	5918	4393	97.59
FCSMPC	4683	6046	5921	4398	97.67
TSOD-RPI-FCSMPC	4676	6044	5919	4388	97.58

strategy, FCS-MPC controlled GCIs perform higher annual energy productions and the efficiency (total in 21,048 MWh, 97.67%) than ones by PI controlled GCIs (total in 21,043 MWh, 97.65%), which are attributed to the switching frequency variation property of FCS-MPC, where a lower switching frequency is derived at the higher power operating point autonomously. Both TSOD-RPI-PI and -FCSMPC methods downgrade the annual energy productions and the total platform efficiency, since in most of interfered instants, it generates more power losses to reduce the temperature swing value.

Figure 5.23 presents the averaged lifetime and efficiency tradeoff comparisons between different methods. It is observed that for PI controlled GCIs, TSOD-SFV-PI method gives the best performances on both the lifetime and efficiency, which offers the

DER system a strong motivation to implement the proposed strategy. For FCS-MPC controlled GCIs, TSOD-RPI-FCSMPC also has a better performance on the lifetime, where the sacrificed efficiency can certainly be compensated by saved cost on the longer operating lifetime.

5.5 Summary of Local Controllers with Centralized Thermal Stress Oriented Dispatch Strategy

To put everything in a nutshell, the proposed centralized thermal stress oriented dispatch strategy with different dispatch methods, the reliability assessment, and the tradeoff analysis are all summarized in Table 5.9. The proposed TSOD strategy illustrates a significantly effective performance on the thermal stress reduction for paralleled grid-connected inverters.

TABLE 5.9

SUMMARY AND COMPARISON OF PI AND FCSMPC CONTROLLERS WITH CENTRALIZED THERMAL STRESSED ORIENTED DISPATCH STRATEGY

Method	**Centralized TSOD Strategy**			**Local Controller**	**Thermal Stress and Reliability Assessment**				**Other**
Name	Dispatch Action	Dispatch Algorithm	Coordination /Communication demands	Additional control scheme	Controlled Loss	Junction Temperature Mean/Swing	Accumulative Damage	Predicted Lifetime	Energy Production/ Efficiency
PI	NO	NO	NO	NO	NO	Medium/Medium	High	Low	Medium
FCS-MPC	NO	NO	NO	NO	NO	Medium/Medium	Medium	Medium	Medium
TSOD-SFV-PI	f_{sw}	SFV, Deterministic, Linear calculation	NO	Modulation scheme	P_{swit}	Low/Low	Low	High	High
TSOD-RPI-PI	Q	RPI, Non-deterministic, Nonlinear programming	YES	NO	P_{cond}, P_{swit}	High/Low	Medium	Medium	Low
TSOD-RPI-FCSMPC	Q	RPI, Non-deterministic, Nonlinear programming	YES	NO	P_{cond}, P_{swit}	High/Low	Low	High	Low

5.6 Conclusion

In this chapter, a centralized thermal stress oriented dispatch strategy is proposed to reduce the thermal stresses for paralleled grid-connected inverters. In the proposed strategy, the instantaneous thermal stress is identified first. Then, the expected junction temperature and power loss are calculated successively. Following this, the proposed strategy takes full advantages of the local control level methods, including the switching frequency variation and the reactive power injection, to generate the expected power loss and achieve a desired thermal profile with a reduced thermal stress for all paralleled inverters.

The effectiveness of the proposed strategy on the thermal stress reduction is justified on a four-paralleled-inverters system from the real-time simulations and the reliability assessment, and on a digital twin hardware platform from the experiments. It turns out that with the proposed TSOD strategy, the thermal stresses are significantly reduced for both PI and FCS-MPC controlled inverters. Considering the tradeoff from the system efficiency, the proposed TSOD strategy with the switching frequency variation dispatch method will be chosen to achieve the least thermal stress, the longest lifetime, and the highest system efficiency for paralleled inverters.

CHAPTER 6 CONCLUSION AND FUTURE WORK

In this dissertation, the method to reduce the thermal stress of the power module in the power converter has been extensively investigated. The thermal stress, as one of the major failures causes in power modules, is generated from the mechanical strain by severely varying temperatures at different loci in the power module and the different coefficients of the thermal expansion of materials, where the varying temperatures at different loci in the power come result from the real-time power loss across the power converter. This thermal stress accelerates the degradation of semiconductor devices, downgrades the system quality and efficiency, eventually causes catastrophic system breakdowns and expensive economical losses. Therefore, this research is dedicated to ameliorating the real-time power loss and reducing the thermal stress in the power module, thereby extending the component lifetime and improving the system reliability.

In this dissertation, novel local control level method and system level strategy are developed to achieve the thermal stress reduction in the power module. First from the local control level, a finite-control-set model predictive control is introduced and deductively investigated from the local control level. Its variable switching frequency property is derived through the geometry analysis on the voltage vector space. It realizes the switching frequency variation autonomously by different power loadings. By taking advantages of this property, the power loss is leveled in the real-time operation and a more mitigated thermal profile is acquired compared with the one by PI controller. In addition, an energy-loss-minimization secondary problem formulation in FCS-MPC is proposed to reduce the power loss in order to achieve the junction temperature mean value decreasing in the power module. This secondary problem formulation is integrated with the basic problem

formulation by different weightings to achieve the power flow control and the power loss reduction simultaneously. Second from the system level, a centralized thermal stress oriented dispatch system level strategy is proposed for multiple paralleled distributed energy resource systems, which reduces the thermal stress in the power module of all paralleled converters. It benefits the power loss balancing of the power converter through the real-time junction temperature variation, the operating and the health conditions of the individual converter. Two local control level methods, the switching frequency variation and the reactive power injection, are imported separately as the dispatch algorithm. Dealing with the varying mission profile, the expected power loss is generated by updating the dispatch action and more mitigated thermal profiles are desired for all converters.

The effectiveness of all methodologies from both local control level and system level is validated on the simulations, the digital twin hardware platform, and the four-paralleled-grid-connected-inverters system model-in-the-loop testing. A long-time-scale analysis from the reliability assessment is also conducted to quantify the impacts of the relieved thermal stress on the damage and lifetime of the power module. Results not only justify the significantly effective performance by all proposed method on the thermal stress reduction in the power module of the converter, but also provides the finite-control-set model predictive control with a strong support for future industry applications and power electronics engineers with more insights to fully leverage the model predictive control, which are two main contributions in this dissertation.

6.1 Publications

The following list is a summary of my main publications.

1. L. Wang, T. Zhao and J. He, "Centralized Thermal Stress Oriented Dispatch Strategy for Paralleled Grid-Connected Inverters Considering Mission Profiles," submitted to *IEEE Open Journal of Power Electronics*, 2021.

2. L. Wang, T. Zhao and J. He, "Investigation of Variable Switching Frequency in Finite Control Set Model Predictive Control on Grid-Connected Inverters," submitted to *IEEE Open Journal of Industry Applications*, 2021.

3. L. Wang, L. Bai, and T. Zhao, "Thermal Stress Oriented Dispatch Strategy for Paralleled Grid-Connected Converters in Electric Vehicle Charging Stations," *2021 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2021. (accepted)

4. L. Wang, Y. Guan, T. Chen, E. Moges, T. Han and T. Zhao, "Evaluation of Wireless Communication Networks on Secondary Control in Underwater Microgrid," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 3084-3091.

5. L. Wang, J. He, T. Han and T. Zhao, "Finite Control Set Model Predictive Control With Secondary Problem Formulation for Power Loss and Thermal Stress Reductions," in *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 4028-4039, July-Aug. 2020.

6. L. Wang, T. Han, T. Zhao and J. He, "Model Predictive Control with Secondary Objective Functions for Power Module Loss Reduction," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 225-231.

7. L. Wang, T. Han and T. Zhao, "Model Predictive Speed Control with Dynamic Reference for Electric Drive of Permanent Magnet Synchronous Machine," *2019 IEEE*

Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 4085-4090.

8. L. Wang, T. Zhao, S. Chen and D. Cook, "An Inductive Power Transfer System Design for Rail Applications," *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, Long Beach, CA, 2018, pp. 84-89.

6.2 Future Work

The following work will be performed in the future to enhance and strengthen the current contributions.

Based on the work in this dissertation:

- The methodology formulation for the continuous-control-set model predictive control needs to be continued by the optimal switching vector arrangement in order to achieve a global minimum on the power loss.

- The methodology formulation for paralleled grid-forming/supporting inverters needs to be continued in order to achieve the thermal stress reduction for all inverters in the microgrid.

- A holistic optimization, by coordinating the total system efficiency and each inverter thermal stress objectives, needs to be focused based on the proposed centralized thermal stress oriented dispatch system level strategy.

- A more sophisticated testing setup needs to be continued, including the open case power semiconductor module, the temperature controlled hub, and the accurate thermal network.
- More contributions will be summarized and presented in the way of papers and journals.

Based on the research trend of the thermal stress reduction:

- Multiple system targets (capacitors, batteries, motor…) can be considered together to achieve better thermal profiles in the electrical vehicle applications.

- Multi-stage converters investigation, such as the dual active bridge in the wireless power transfer applications, can be considered to explore the thermal stress reduction performance by model predictive control.

REFERENCES

[1] A. Moreno, “Marine Renewable Energy,” 7th Annual North Carolina Renewable Ocean Energy Symposium, Wanchese, NC, USA, April 5-6, 2018.

[2] P. Tavner, “How are we going to make offshore wind farms more reliable?” presented at the SUPERGEN Wind General Assembly, Durham, NC, USA, Mar. 20, 2011.

[3] F. Blaabjerg, R. Teodorescu, M. Liserre and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398-1409, Oct.2006.

[4] J. He, T. Zhao, X. Jing and N. A. O. Demerdash, "Application of wide bandgap devices in renewable energy systems - Benefits and challenges," in *Proc. IEEE Int. Conf. Renew. Energy Res. Appl.*, 2014, pp. 749-754.

[5] W. Chen, A. M. Bazzi, J. Hare and S. Gupta, "Real-time integrated model of a micro-grid with distributed clean energy generators and their power electronics," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, 2016, pp. 2666-2672.

[6] M. Liserre, R. Teodorescu and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 263-272, Jan. 2006.

[7] M. Cespedes and J. Sun, "Impedance Modeling and Analysis of Grid-Connected Voltage-Source Converters," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1254-1261, March 2014.

[8] T. Zhao, G. Wang, S. Bhattacharya and A. Q. Huang, "Voltage and Power Balance Control for a Cascaded H-Bridge Converter-Based Solid-State Transformer," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1523-1532, April 2013.

[9] K. Ma, M. Liserre, F. Blaabjerg and T. Kerekes, "Thermal Loading and Lifetime Estimation for Power Device Considering Mission Profiles in Wind Power Converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 590-602, Feb. 2015.

[10] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo and F. Blaabjerg, "A 3-D-Lumped Thermal Network Model for Long-Term Load Profiles Analysis in High-Power IGBT Modules," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1050-1063, Sept. 2016.

[11] Y. Zhang, H. Wang, Z. Wang, F. Blaabjerg and M. Saeedifard, "Mission Profile-Based System-Level Reliability Prediction Method for Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6916-6930, July 2020, doi: 10.1109/TPEL.2019.2957826.

[12] D. Zhou, H. Wang and F. Blaabjerg, "Mission Profile Based System-Level Reliability Analysis of DC/DC Converters for a Backup Power Application," in *IEEE Transactions*

on Power Electronics, vol. 33, no. 9, pp. 8030-8039, Sept. 2018, doi: 10.1109/TPEL.2017.2769161.

[13] I. Vernica, H. Wang and F. Blaabjerg, "Impact of Long-Term Mission Profile Sampling Rate on the Reliability Evaluation of Power Electronics in Photovoltaic Applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, Portland, OR, 2018, pp. 4078-4085.

[14] L. M. Moore and H. N. Post, "Five years of operating experience at a large, utility-scale photovoltaic generating plant," *Prog. Photovolt.: Res. Applicat.*, vol. 16, no. 3, pp. 249–259, 2008.

[15] E. Wolfgang, "Examples for failures in power electronics systems," presented at the ECPE Tutorial Reliability Power Electronic Systems, Nuremberg, Germany, Apr. 2007.

[16] H. Oh, B. Han, P. McCluskey, C. Han and B. D. Youn, "Physics-of-Failure, Condition Monitoring, and Prognostics of Insulated Gate Bipolar Transistor Modules: A Review," in *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2413-2426, May 2015.

[17] U. M. Choi, F. Blaabjerg and K. B. Lee, "Study and Handling Methods of Power IGBT Module Failures in Power Electronic Converter Systems," in *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2517-2533, May 2015.

[18] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," in *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734-2752, Nov. 2010.

[19] R. Bayerer, T. Herrmann, T. Licht, J. Lutz and M. Feller, "Model for Power Cycling lifetime of IGBT Modules - various factors influencing lifetime," *5th International Conference on Integrated Power Electronics Systems*, Nuremberg, Germany, 2008, pp. 1-6.

[20] J. Rodriguez et al., "Predictive Current Control of a Voltage Source Inverter," in IEEE Transactions on Industrial Electronics, vol. 54, no. 1, pp. 495-503, Feb. 2007.

[21] P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo and J. Rodriguez, "Predictive Control in Power Electronics and Drives," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, pp. 4312-4324, Dec. 2008.

[22] P. CortÉs, J. RodrÍguez, P. Antoniewicz and M. Kazmierkowski, "Direct Power Control of an AFE Using Predictive Control," in *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2516-2523, Sept. 2008.

[23] S. Kouro, P. Cortes, R. Vargas, U. Ammann and J. Rodriguez, "Model Predictive Control—A Simple and Powerful Method to Control Power Converters," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1826-1838, June 2009.

[24] P. Cortes, G. Ortiz, J. I. Yuz, J. Rodriguez, S. Vazquez and L. G. Franquelo, "Model Predictive Control of an Inverter With Output LC Filter for UPS Applications," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1875-1883, June 2009.

[25] M. Pacas and J. Weber, "Predictive direct torque control for the PM synchronous machine," in *IEEE Transactions on Industrial Electronics*, vol. 52, no. 5, pp. 1350-1356, Oct. 2005.

[26] R. Vargas, U. Ammann, B. Hudoffsky, J. Rodriguez and P. Wheeler, "Predictive Torque Control of an Induction Machine Fed by a Matrix Converter With Reactive Input Power Control," in *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1426-1438, June 2010.

[27] O. Sandre-Hernandez, J. Rangel-Magdaleno and R. Morales-Caporal, "A Comparison on Finite-Set Model Predictive Torque Control Schemes for PMSMs," in *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8838-8847, Oct. 2018.

[28] M. Preindl and S. Bolognani, "Model Predictive Direct Speed Control with Finite Control Set of PMSM Drive Systems," in *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 1007-1015, Feb. 2013.

[29] D. E. Quevedo, R. P. Aguilera, M. A. Perez, P. Cortes and R. Lizana, "Model Predictive Control of an AFE Rectifier with Dynamic References," in *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3128-3136, July 2012.

[30] Z. Zhang, F. Wang, T. Sun, J. Rodríguez and R. Kennel, "FPGA-Based Experimental Investigation of a Quasi-Centralized Model Predictive Control for Back-to-Back Converters," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 662-674, Jan. 2016.

[31] J. Z. Zhang, T. Sun, F. Wang, J. Rodríguez and R. Kennel, "A Computationally Efficient Quasi-Centralized DMPC for Back-to-Back Converter PMSG Wind Turbine Systems Without DC-Link Tracking Errors," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 10, pp. 6160-6171, Oct. 2016.

[32] M. Preindl, E. Schaltz and P. Thogersen, "Switching Frequency Reduction Using Model Predictive Direct Current Control for High-Power Voltage Source Inverters," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2826-2835, July 2011.

[33] Y. Zhang, W. Xie, Z. Li and Y. Zhang, "Model Predictive Direct Power Control of a PWM Rectifier with Duty Cycle Optimization," in *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5343-5351, Nov. 2013.

[34] H. Fang, Z. Zhang, X. Feng and R. Kennel, "Ripple-reduced model predictive direct power control for active front-end power converters with extended switching vectors and time-optimised control," in *IET Power Electronics*, vol. 9, no. 9, pp. 1914-1923, 27 7 2016.

[35] Z. Zhang, H. Fang, F. Gao, J. Rodríguez and R. Kennel, "Multiple-Vector Model Predictive Power Control for Grid-Tied Wind Turbine System With Enhanced Steady-State Control Performance," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 8, pp. 6287-6298, Aug. 2017.

[36] P. Cortes *et al*., "Guidelines for weighting factors design in Model Predictive Control of power converters and drives," *2009 IEEE International Conference on Industrial Technology*, Gippsland, VIC, 2009, pp. 1-7.

[37] Y. Zhang and C. Qu, "Model Predictive Direct Power Control of PWM Rectifiers Under Unbalanced Network Conditions," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4011-4022, July 2015.

[38] J. Rodriguez, M. P. Kazmierkowski, J. R. Espinoza, P. Zanchetta, H. Abu-Rub, H. A. Young, and C. A. Rojas, "State of the Art of Finite Control Set Model Predictive Control in Power Electronics," *IEEE Trans. Ind. Inf.*, vol. 9, no. 2, pp. 1003-1016, May 2013.

[39] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo and M. Norambuena, "Model Predictive Control for Power Converters and Drives: Advances and Trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935-947, Feb. 2017.

[40] M. Andresen, M. Liserre and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," 2*014 16th European Conference on Power Electronics and Applications*, Lappeenranta, Finland, 2014, pp. 1-10.

[41] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg and M. Liserre, "Junction Temperature Control for More Reliable Power Electronics," in *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 765-776, Jan. 2018.

[42] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng and D. Cao, "Overview of Real-Time Lifetime Prediction and Extension for SiC Power Converters," in *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7765-7794, Aug. 2020.

[43] J. Kuprat, C. H. Van der Broeck, M. Andresen, S. Kalker, R. W. De Doncker and M. Liserre, "Research on Active Thermal Control: Actual Status and Future Trends Special Issue Commemorating 40 years of WEMPEC, 2021," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

[44] D. A. Murdock, J. E. R. Torres, J. J. Connors and R. D. Lorenz, "Active thermal control of power electronic modules," in *IEEE Transactions on Industry Applications*, vol. 42, no. 2, pp. 552-558, March-April 2006.

[45] L. Wei, J. McGuire and R. A. Lukaszewski, "Analysis of PWM Frequency Control to Improve the Lifetime of PWM Inverter," in *IEEE Transactions on Industry Applications*, vol. 47, no. 2, pp. 922-929, March-April 2011.

[46] G. Lo Calzo, A. Lidozzi, L. Solero, F. Crescimbini and V. Cardi, "Thermal regulation as control reference in electric drives," *2012 15th International Power Electronics and*

Motion Control Conference (EPE/PEMC), Novi Sad, Serbia, 2012, pp. DS2c.18-1-DS2c.18-7.

[47] J. Falck, M. Andresen and M. Liserre, "Active thermal control of IGBT power electronic converters," *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Yokohama, Japan, 2015.

[48] I. Vernica, K. Ma and F. Blaabjerg, "Modelling and improvement of thermal cycling in power electronics for motor drive applications," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, USA, 2016.

[49] I. Vernica, F. Blaabjerg and K. Ma, "Modelling and design of active thermal controls for power electronics of motor drive applications," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, USA, 2017.

[50] T. A. Polom, B. Wang and R. D. Lorenz, "ΔTj control of switching power devices at thermal boundaries via physics-based loss manipulation," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, USA, 2016.

[51] T. A. Polom, B. Wang and R. D. Lorenz, "Control of Junction Temperature and Its Rate of Change at Thermal Boundaries via Precise Loss Manipulation," in *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4796-4806, Sept.-Oct. 2017.

[52] P. Kumar Prasobhu, V. Raveendran, G. Buticchi and M. Liserre, "Active Thermal Control of GaN-Based DC/DC Converter," in *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3529-3540, July-Aug. 2018.

[53] C. H. van der Broeck, L. A. Ruppert, R. D. Lorenz and R. W. De Doncker, "Active thermal cycle reduction of power modules via gate resistance manipulation," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, 2018.

[54] C. H. van der Broeck, L. A. Ruppert, R. D. Lorenz and R. W. De Doncker, "Methodology for Active Thermal Cycle Reduction of Power Electronic Modules," in *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 8213-8229, Aug. 2019.

[55] J. Wölfle, M. Nitzsche, J. Ruthardt and J. Roth-Stielow, "Junction Temperature Control System to Increase the Lifetime of IGBT-Power-Modules in Synchronous Motor Drives Without Affecting Torque and Speed," in *IEEE Open Journal of Power Electronics*, vol. 1, pp. 273-283, 2020.

[56] J. Sheng *et al*., "Active Thermal Control for Hybrid Modular Multilevel Converter Under Overmodulation Operation," in *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4242-4255, April 2020.

[57] K. Ma and F. Blaabjerg, "Modulation Methods for Neutral-Point-Clamped Wind Power Converter Achieving Loss and Thermal Redistribution Under Low-Voltage

Ride-Through," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 835-845, Feb. 2014.

[58] E. Ugur, S. Dusmez and B. Akin, "An Investigation on Diagnosis-Based Power Switch Lifetime Extension Strategies for Three-Phase Inverters," in *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 2064-2075, March-April 2019.

[59] K. Ma and F. Blaabjerg, "Thermal optimised modulation methods of three level neutral-point-clamped inverter for 10 MW wind turbines under low voltage ride through," *IET Power Electron.*, vol. 5, no. 6, pp. 920–927, Jul. 2012.

[60] Y. Ko, M. Andresen, G. Buticchi and M. Liserre, "Thermally Compensated Discontinuous Modulation Strategy for Cascaded H-Bridge Converters," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2704-2713, March 2018

[61] Y. Ko, M. Andresen, G. Buticchi and M. Liserre, "Discontinuous-Modulation-Based Active Thermal Control of Power Electronic Modules in Wind Farms," in *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 301-310, Jan. 2019.

[62] Y. Yang, H. Wang, F. Blaabjerg and T. Kerekes, "A Hybrid Power Control Concept for PV Inverters With Reduced Thermal Loading," in *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6271-6275, Dec. 2014.

[63] A. Sangwongwanich, Y. Yang, D. Sera and F. Blaabjerg, "Mission Profile-Oriented Control for Reliability and Lifetime of Photovoltaic Inverters," in *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 601-610, Jan.-Feb. 2020.

[64] M. Andresen, G. Buticchi and M. Liserre, "Thermal Stress Analysis and MPPT Optimization of Photovoltaic Systems," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4889-4898, Aug. 2016.

[65] J. Lemmens, J. Driesen and P. Vanassche, "Dynamic DC-link voltage adaptation for thermal management of traction drives," *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, USA, 2013.

[66] X. Wang, X. Wang and X. Yuan, "An optimal DC bus voltage control method to improve the junction temperature of IGBTs in low speed operations of traction applications," *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Auckland, New Zealand, 2016.

[67] N. Zhao, N. Schofield, R. Yang and R. Gu, "Investigation of DC-Link Voltage and Temperature Variations on EV Traction System Design," in *IEEE Transactions on Industry Applications*, vol. 53, no. 4, pp. 3707-3718, July-Aug. 2017.

[68] K. Ma, M. Liserre and F. Blaabjerg, "Reactive Power Influence on the Thermal Cycling of Multi-MW Wind Power Inverter," in *IEEE Transactions on Industry Applications*, vol. 49, no. 2, pp. 922-930, March-April 2013.

[69] Y. Yang, H. Wang and F. Blaabjerg, "Reactive Power Injection Strategies for Single-Phase Photovoltaic Systems Considering Grid Requirements," in *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 4065-4076, Nov.-Dec. 2014.

[70] D. Zhou, F. Blaabjerg, M. Lau and M. Tønnes, "Optimized Reactive Power Flow of DFIG Power Converters for Better Reliability Performance Considering Grid Codes," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 3, pp. 1552-1562, March 2015.

[71] J. Zhang, J. Wang and X. Cai, "Active Thermal Control-Based Anticondensation Strategy in Paralleled Wind Power Converters by Adjusting Reactive Circulating Current," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 277-291, March 2018.

[72] D. Zhou and F. Blaabjerg, "Optimized Demagnetizing Control of DFIG Power Converter for Reduced Thermal Stress During Symmetrical Grid Fault," in *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10326-10340, Dec. 2018.

[73] K. Desingu, R. Selvaraj and T. R. Chelliah, "Control of Reactive Power for Stabilized Junction Temperature in Power Electronic Devices Serving to a 250-MW Asynchronous Hydrogenerating Unit," in *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7854-7867, Nov.-Dec. 2019.

[74] Qingmian Chai, Cuo Zhang, Zhao Yang Dong, Yan Xu, Operational reliability assessment of photovoltaic inverters considering voltage/VAR control function, Electric Power Systems Research, Volume 190, 2021.

[75] M. Andresen, G. De Carne and M. Liserre, "Load-Dependent Active Thermal Control of Grid-Forming Converters," in *IEEE Transactions on Industry Applications*, vol. 56, no. 2, pp. 2078-2086, March-April 2020.

[76] J. Lemmens, P. Vanassche and J. Driesen, "Optimal Control of Traction Motor Drives Under Electrothermal Constraints," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 2, pp. 249-263, June 2014.

[77] A. Janabi and B. Wang, "Variable mode model predictive control for minimizing the thermal stress in electric drives," *2017 IEEE International Electric Machines and Drives Conference (IEMDC)*, Miami, FL, USA, 2017.

[78] J. Falck, M. Andresen and M. Liserre, "Thermal-based finite control set model predictive control for IGBT power electronic converters," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, USA, 2016.

[79] J. Falck, G. Buticchi and M. Liserre, "Thermal Stress Based Model Predictive Control of Electric Drives," in *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1513-1522, March-April 2018.

[80] T. Sun, J. Wang, A. Griffo and B. Sen, "Active Thermal Management for Interior Permanent Magnet Synchronous Machine (IPMSM) Drives Based on Model Predictive Control," in *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4506-4514, Sept.-Oct. 2018.

[81] R. Han *et al*., "Thermal Stress Balancing Oriented Model Predictive Control of Modular Multilevel Switching Power Amplifier," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 11, pp. 9028-9038, Nov. 2020.

[82] H. Rong *et al*., "Modulated Model Predictive Control for Reliability Improvement of Extremely Low Frequency Power Amplifier via Junction Temperature Swing Reduction," in *IEEE Transactions on Industrial Electronics.*

[83] M. Novak, T. Dragicevic and F. Blaabjerg, "Finite Set MPC Algorithm for Achieving Thermal Redistribution in a Neutral-Point-Clamped Converter," *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Washington, DC, USA, 2018

[84] M. Novak and F. Blaabjerg, "Model Predictive Active Thermal Control Strategy for Lifetime Extension of a 3L-NPC Converter for UPS Applications," *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, Aalborg, Denmark, 2020.

[85] M. Novak, V. Ferreira, M. Andresen, T. Dragicevic, F. Blaabjerg and M. Liserre, "FS-MPC Based Thermal Stress Balancing and Reliability Analysis for NPC Converters," in *IEEE Open Journal of Power Electronics*, vol. 2, pp. 124-137, 2021.

[86] C. Li, D. Jiao, J. Jia, F. Guo and J. Wang, "Thermoelectric Cooling for Power Electronics Circuits: Modeling and Active Temperature Control," in *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3995-4005, Nov.-Dec. 2014

[87] B. Wang, L. Zhou, Y. Zhang, K. Wang, X. Du and P. Sun, "Active Junction Temperature Control of IGBT Based on Adjusting the Turn-off Trajectory," in *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5811-5823, July 2018.

[88] Y. Yerasimou, V. Pickert, B. Ji and X. Song, "Liquid Metal Magnetohydrodynamic Pump for Junction Temperature Control of Power Modules," in *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10583-10593, Dec. 2018

[89] R. Wang, L. Tan, C. Li, T. Huang, H. Li and X. Huang, "Analysis, Design, and Implementation of Junction Temperature Fluctuation Tracking Suppression Strategy for SiC MOSFETs in Wireless High-Power Transfer," in *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 1193-1204, Jan. 2021

[90] J. Ewanchuk, J. Brandelero and S. Mollov, "Lifetime extension of a multi-die SiC power module using selective gate driving with temperature feedforward compensation," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, 2017.

[91] J. Ewanchuk, J. Brandelero and S. Mollov, "A Gate Driver Based Approach to Improving the Current Density in a Power Module by Equalizing the Individual Die Temperatures," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, 2018.

[92] J. Brandelero, J. Ewanchuk and S. Mollov, "Selective Gate Driving in Intelligent Power Modules," in *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 898-910, Jan. 2021.

[93] X. Wang, Z. Zhao and L. Yuan, "Current sharing of IGBT modules in parallel with thermal imbalance," *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, USA, 2010, pp. 2101-2108.

[94] Brandis, A.; Pelin, D.; Mati´c, T.; Topi´c, D. Temperature Control Concept for Parallel IGBT Operation. Electronics 2021, 10, 429.

[95] V. Ferreira, M. Andresen, B. Cardoso and M. Liserre, "Pulse-Shadowing-Based Thermal Balancing in Multichip Modules," in *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 4081-4088, July-Aug. 2020.

[96] J. Wang, Z. Li, X. Jiang, C. Zeng and Z. J. Shen, "Gate Control Optimization of Si/SiC Hybrid Switch for Junction Temperature Balance and Power Loss Reduction," in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1744-1754, Feb. 2019.

[97] Z. Li *et al*., "Active Gate Delay Time Control of Si/SiC Hybrid Switch for Junction Temperature Balance Over a Wide Power Range," in *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 5354-5365, May 2020.

[98] M. Liserre, M. Andresen, L. Costa and G. Buticchi, "Power Routing in Modular Smart Transformers: Active Thermal Control Through Uneven Loading of Cells," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 43-53, Sept. 2016.

[99] G. Buticchi, M. Andresen, M. Wutti and M. Liserre, "Lifetime-Based Power Routing of a Quadruple Active Bridge DC/DC Converter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8892-8903, Nov. 2017.

[100] F. Hahn, M. Andresen, G. Buticchi and M. Liserre, "Thermal Analysis and Balancing for Modular Multilevel Converters in HVDC Applications," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1985-1996, March 2018.

[101] V. N. Ferreira, R. R. Bastos, T. S. de Souza, M. Liserre and B. J. Cardoso Filho, "Power Routing to Enhance the Lifetime of Multiphase Drives," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019.

[102] V. Raveendran, M. Andresen and M. Liserre, "Improving Onboard Converter Reliability for More Electric Aircraft With Lifetime-Based Control," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5787-5796, July 2019.

[103] V. G. Monopoli, A. Marquez, J. I. Leon, Y. Ko, G. Buticchi and M. Liserre, "Improved Harmonic Performance of Cascaded H-Bridge Converters With Thermal Control," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 4982-4991, July 2019.

[104] A. Marquez *et al*., "Sampling-Time Harmonic Control for Cascaded H-Bridge Converters With Thermal Control," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 4, pp. 2776-2785, April 2020.

[105] M. Liserre, V. Raveendran and M. Andresen, "Graph-Theory-Based Modeling and Control for System-Level Optimization of Smart Transformers," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8910-8920, Oct. 2020.

[106] S. Peyghami, P. Davari and F. Blaabjerg, "System-Level Reliability-Oriented Power Sharing Strategy for DC Power Systems," in *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 4865-4875, Sept.-Oct. 2019.

[107] Y. Wang, D. Liu, P. Liu, F. Deng, D. Zhou and Z. Chen, "Lifetime-Oriented Droop Control Strategy for AC Islanded Microgrids," in *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 3252-3263, May-June 2019.

[108] J. Jiang, S. Peyghami, C. Coates and F. Blaabjerg, "A Decentralized Reliability-Enhanced Power Sharing Strategy for PV-Based Microgrids," in *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 7281-7293, June 2021.

[109] Y. Wang, P. Liu, D. Liu, F. Deng and Z. Chen, "Enhanced Hierarchical Control Framework of Microgrids With Efficiency Improvement and Thermal Management," in *IEEE Transactions on Energy Conversion*, vol. 36, no. 1, pp. 11-22, March 2021.

[110] A. Ammous, S. Ghedira, B. Allard, H. Morel and D. Renault, "Choosing a thermal model for electrothermal simulation of power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 300-307, March 1999.

[111] IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," in *IEEE Std 519-2014 (Revision of IEEE Std519-1992)*, vol., no., pp.1-29, 11 June 2014.

[112] Southeast National Marine Renewable Energy Center, “Resource Measurement & Modeling: Available Data,” ADCP-0001 B2 & B3 (November 2011-April 2012). [Online]. Available: http://coet.fau.edu/resource-measurement-modeling/available-data.html

[113] U. Choi, F. Blaabjerg, S. Jørgensen, S. Munk-Nielsen and B. Rannestad, "Reliability Improvement of Power Converters by Means of Condition Monitoring of IGBT Modules," in *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7990-7997, Oct. 2017.

[114] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters—An Overview," in *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569-3578, Sept.-Oct. 2014.

[115] K. Harada, A. Katsuki and M. Fujiwara, "Use of ESR for deterioration diagnosis of electrolytic capacitor," in *IEEE Transactions on Power Electronics*, vol. 8, no. 4, pp. 355-361, Oct 1993.

[116] A. M. R. Amaral and A. J. M. Cardoso, "A Simple Offline Technique for Evaluating the Condition of Aluminum–Electrolytic–Capacitors," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3230-3237, Aug. 2009.

[117] K. W. Lee, M. Kim, J. Yoon, S. B. Lee and J. Y. Yoo, "Condition Monitoring of DC-Link Electrolytic Capacitors in Adjustable-Speed Drives," in *IEEE Transactions on Industry Applications*, vol. 44, no. 5, pp. 1606-1613, Sept.-Oct. 2008.

[118] X. S. Pu, T. H. Nguyen, D. C. Lee, K. B. Lee and J. M. Kim, "Fault Diagnosis of DC-Link Capacitors in Three-Phase AC/DC PWM Converters by Online Estimation of Equivalent Series Resistance," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 9, pp. 4118-4127, Sept. 2013.

[119] D. C. Lee, K. J. Lee, J. K. Seok and J. W. Choi, "Online capacitance estimation of DC-link electrolytic capacitors for three-phase AC/DC/AC PWM converters using recursive least squares method," in *IEE Proceedings - Electric Power Applications*, vol. 152, no. 6, pp. 1503-1508, 4 Nov. 2005.

[120] M. A. Vogelsberger, T. Wiesinger and H. Ertl, "Life-Cycle Monitoring and Voltage-Managing Unit for DC-Link Electrolytic Capacitors in PWM Converters," in *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 493-503, Feb. 2011.

[121] E. Aeloiza, Jang-Hwan Kim, P. Enjeti and P. Ruminot, "A Real Time Method to Estimate Electrolytic Capacitor Condition in PWM Adjustable Speed Drives and Uninterruptible Power Supplies," *2005 IEEE 36th Power Electronics Specialists Conference*, Recife, 2005, pp. 2867-2872.

[122] H. Wang and H. Wang, "A Two-Terminal Active Capacitor," in *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 5893-5896, Aug. 2017.

[123] H. A. Mantooth and A. R. Hefner, "Electrothermal simulation of an IGBT PWM inverter," in *IEEE Transactions on Power Electronics*, vol. 12, no. 3, pp. 474-484, May 1997.

[124] K. Ma, N. He, M. Liserre and F. Blaabjerg, "Frequency-Domain Thermal Modeling and Characterization of Power Semiconductor Devices," in *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7183-7193, Oct. 2016.

[125] G. C. Konstantopoulos and A. T. Alexandridis, "Full-Scale Modeling, Control, and Analysis of Grid-Connected Wind Turbine Induction Generators With Back-to-Back

AC/DC/AC Converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 739-748, Dec. 2014.

[126] V. Yaramasu, B. Wu, P. C. Sen, S. Kouro and M. Narimani, "High-power wind energy conversion systems: State-of-the-art and emerging technologies," in *Proceedings of the IEEE*, vol. 103, no. 5, pp. 740-788, May 2015.

[127] B. Parkhideh and S. Bhattacharya, "Vector-Controlled Voltage-Source-Converter-Based Transmission Under Grid Disturbances," in *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 661-672, Feb. 2013.

[128] Yue Hong, Rafael Waters, Cecilia Boström, Mikael Eriksson, Jens Engström, Mats Leijon, "Review on electrical control strategies for wave energy converting systems", Renewable and Sustainable Energy Reviews, Volume 31, 2014.

[129] *IEEE Standard Framework for the Reliability Prediction of Hardware*, IEEE Standard 1413, 2009.

[130] Y. Song and B. Wang, "Survey on Reliability of Power Electronic Systems," in *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 591-604, Jan. 2013.

[131] H. Wang, K. Ma and F. Blaabjerg, "Design for reliability of power electronic systems," *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Montreal, QC, 2012, pp. 33-44.

[132] W. Qiao and D. Lu, "A Survey on Wind Turbine Condition Monitoring and Fault Diagnosis—Part I: Components and Subsystems," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 10, pp. 6536-6545, Oct. 2015.

[133] W. Qiao and D. Lu, "A Survey on Wind Turbine Condition Monitoring and Fault Diagnosis—Part II: Signals and Signal Processing Methods," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 10, pp. 6546-6557, Oct. 2015.

[134] A. Marquez Alcaide, J. I. Leon, V. G. Monopoli, S. Vazquez, M. Liserre and L. G. Franquelo, "Generalized Harmonic Control for CHB Converters with Unbalanced Cells Operation," in *IEEE Transactions on Industrial Electronics.*

[135] S. Peyghami, P. Davari, M. F-Firuzabad and F. Blaabjerg, "Failure Mode, Effects and Criticality Analysis (FMECA) in Power Electronic based Power Systems," *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Genova, Italy, 2019, pp. P.1-P.9

[136] S. Peyghami, P. Davari, D. Zhou, M. F-Firuzabad and F. Blaabjerg, "Wear-Out Failure of a Power Electronic Converter Under Inversion and Rectification Modes," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 1598-1604

[137] N. Flourentzou, V. G. Agelidis and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," in *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 592-602, March 2009.

[138] R. Wu, S. B. Dewan and G. R. Slemon, "A PWM AC-to-DC converter with fixed switching frequency," in *IEEE Transactions on Industry Applications*, vol. 26, no. 5, pp. 880-885, Sep/Oct 1990.

[139] R. Wu, S. B. Dewan and G. R. Slemon, "Analysis of an AC-to-DC voltage source converter using PWM with phase and amplitude control," in *IEEE Transactions on Industry Applications*, vol. 27, no. 2, pp. 355-364, Mar/Apr 1991.

[140] V. Blasko and V. Kaura, "A new mathematical model and control of a three-phase AC-DC voltage source converter," in *IEEE Transactions on Power Electronics*, vol. 12, no. 1, pp. 116-123, Jan 1997.

[141] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids—A General Approach Toward Standardization," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 158-172, Jan. 2011.

[142] L. Wang, Y. Guan, T. Chen, E. Moges, T. Han and T. Zhao, "Evaluation of Wireless Communication Networks on Secondary Control in Underwater Microgrid," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 3084-3091.

[143] L. Wang, J. He, T. Han and T. Zhao, "Finite Control Set Model Predictive Control With Secondary Problem Formulation for Power Loss and Thermal Stress Reductions," in *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 4028-4039, July-Aug. 2020.

[144] L. Wang, T. Han and T. Zhao, "Model Predictive Speed Control with Dynamic Reference for Electric Drive of Permanent Magnet Synchronous Machine," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 4085-4090.

[145] L. Wang, T. Han, T. Zhao and J. He, "Model Predictive Control with Secondary Objective Functions for Power Module Loss Reduction," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019.

[146] L. Wang, T. Zhao, S. Chen and D. Cook, "An Inductive Power Transfer System Design for Rail Applications," *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, Long Beach, CA, USA, 2018.

APPENDIX A: FEASIBLE OPERATION REGION ON VOLTAGE VECTOR SPACE (FOV)

The voltage limit curve in FOV is shown in (3.27) and can be rearranged into the following,

$$\frac{(V_{\mathrm{d}})^2}{(V_{\mathrm{dc}}/\sqrt{3})^2}+\frac{(V_{\mathrm{q}})^2}{(V_{dc}/\sqrt{3})^2}\leqslant 1 \tag{A.A.1}$$

which is a circle with the center at the origin (0, 0) and the radius of $V_{\mathrm{dc}}/\sqrt{3}$.

Similar with (A.A.1), the $V_{\mathrm{dc}}/3$ curve can be derived below,

$$\frac{(V_{\mathrm{d}})^2}{(V_{\mathrm{dc}}/3)^2}+\frac{(V_{\mathrm{q}})^2}{(V_{dc}/3)^2}\leqslant 1 \tag{A.A.2}$$

which is a circle with the center at the origin (0, 0) and the radius of $V_{\mathrm{dc}}/3$.

The current limit curve in FOV is shown in (3.28), where I_{d} and I_{q} can be calculated in perspectives of V_{d} and V_{q} in the steady states through the following equations,

$$\begin{aligned} V_{\mathrm{d}} &= E_{\mathrm{d}}+R_{\mathrm{g}}I_{\mathrm{d}}-w_{\mathrm{s}}L_{\mathrm{g}}I_{\mathrm{q}} \\ V_{\mathrm{q}} &= E_{\mathrm{q}}+R_{\mathrm{g}}I_{\mathrm{q}}+w_{\mathrm{s}}L_{\mathrm{g}}I_{\mathrm{d}} \end{aligned} \tag{A.A.3}$$

Then, I_{d} and I_{q} can be represented into the following,

$$\begin{aligned} I_{\mathrm{d}} &= \frac{R_{\mathrm{g}}(V_{\mathrm{d}}-E_{\mathrm{d}})+w_{\mathrm{s}}L_{\mathrm{g}}(V_{\mathrm{q}}-E_{\mathrm{q}})}{R_{\mathrm{g}}^2+(w_{\mathrm{s}}L_{\mathrm{g}})^2} \\ I_{\mathrm{q}} &= \frac{R_{\mathrm{g}}(V_{\mathrm{q}}-E_{\mathrm{q}})-w_{\mathrm{s}}L_{\mathrm{g}}(V_{\mathrm{d}}-E_{\mathrm{d}})}{R_{\mathrm{g}}^2+(w_{\mathrm{s}}L_{\mathrm{g}})^2} \end{aligned} \tag{A.A.4}$$

In the most grid-connected applications, the line reactance is much greater than the line resistance, which is $w_{\mathrm{s}}L_{\mathrm{g}} >> R_{\mathrm{g}}$. Equation (A.A.4) can be further simplified as follows,

$$\begin{aligned} I_{\mathrm{d}} &= \frac{(V_{\mathrm{q}}-E_{\mathrm{q}})}{(w_{\mathrm{s}}L_{\mathrm{g}})} \\ I_{\mathrm{q}} &= \frac{-(V_{\mathrm{d}}-E_{\mathrm{d}})}{(w_{\mathrm{s}}L_{\mathrm{g}})} \end{aligned} \tag{A.A.5}$$

Equation (3.29) can be derived eventually by applying (A.A.5) to (3.28), which is a circle with the center at (E_d, E_q) and the radius of $w_s L_g I_{max}$.

APPENDIX B: FEASIBLE OPERATION REGION ON POWER VECTOR SPACE (FOP)

The steady states of the power converter are mapped from FOV to FOP essentially by the power equations below,

$$\begin{aligned} P &= \frac{3}{2}\left(E_{\mathrm{d}} I_{\mathrm{d}} + E_{\mathrm{q}} I_{\mathrm{q}}\right) \\ Q &= \frac{3}{2}\left(E_{\mathrm{q}} I_{\mathrm{d}} - E_{\mathrm{d}} I_{\mathrm{q}}\right) \end{aligned} \tag{A.B.1}$$

The current limit curve in FOP can be first easily inferred by calculating I_{d} and I_{q} from (A.B.1),

$$\begin{aligned} I_{\mathrm{d}} &= \frac{2}{3}\frac{1}{E_{\mathrm{d}}^2 + E_{\mathrm{q}}^2}\left(E_{\mathrm{d}} P + E_{\mathrm{q}} Q\right) \\ I_{\mathrm{q}} &= \frac{2}{3}\frac{1}{E_{\mathrm{d}}^2 + E_{\mathrm{q}}^2}\left(E_{\mathrm{q}} P - E_{\mathrm{d}} Q\right) \end{aligned} \tag{A.B.2}$$

Due to the Park transformation in the *dq* rotating reference frame, $E_{\mathrm{d}} = 0$ is applied to (A.B.2). Then, (A.B.2) is simplified into,

$$\begin{aligned} I_{\mathrm{d}} &= \frac{2}{3}\frac{Q}{E_{\mathrm{q}}} \\ I_{\mathrm{q}} &= \frac{2}{3}\frac{P}{E_{\mathrm{q}}} \end{aligned} \tag{A.B.3}$$

and the current limit curve in FOP is expressed in (3.32), which is a circle with the center at the origin (0, 0) and the radius of $(3/2)E_{\mathrm{q}}I_{\max}$.

The voltage limit curve in FOP requires the representation of the V_{d} and V_{q} in perspectives of P and Q first. This can be solved by substituting I_{d} and I_{q} in (A.A.3) with (A.B.3) and assuming $w_{\mathrm{s}}L_{\mathrm{g}} >> R_{\mathrm{g}}$,

$$\begin{aligned} V_{\mathrm{d}} &= E_{\mathrm{d}} - w_{\mathrm{s}} L_{\mathrm{g}} \frac{2P}{3E_{\mathrm{q}}} \\ V_{\mathrm{q}} &= E_{\mathrm{q}} + w_{\mathrm{s}} L_{\mathrm{g}} \frac{2Q}{3E_{\mathrm{q}}} \end{aligned} \tag{A.B.4}$$

Then, (A.B.4) is rearranged for a convenient observation,

$$\begin{aligned} V_{\mathrm{d}} &= \frac{2w_{\mathrm{s}} L_{\mathrm{g}}}{3E_{\mathrm{q}}} \left(\frac{3E_{\mathrm{q}}}{2w_{\mathrm{s}} L_{\mathrm{g}}} E_{\mathrm{d}} - P \right) \\ V_{\mathrm{q}} &= \frac{2w_{\mathrm{s}} L_{\mathrm{g}}}{3E_{\mathrm{q}}} \left(\frac{3E_{\mathrm{q}}}{2w_{\mathrm{s}} L_{\mathrm{g}}} E_{\mathrm{q}} + Q \right) \end{aligned} \tag{A.B.5}$$

Equation (A.B.5) is applied to (3.34) and (3.35) for the voltage limit curve and the $V_{\mathrm{dc}}/3$ curve in FOP, respectively, which are displayed in (3.31) and (3.33) and are circles with the center at ($3E_{\mathrm{d}}E_{\mathrm{q}}/(2w_{\mathrm{s}}L_{\mathrm{g}})$, $-3E_{\mathrm{q}}E_{\mathrm{q}}/(2w_{\mathrm{s}}L_{\mathrm{g}})$) and radius of $\sqrt{3}\ V_{\mathrm{dc}}E_{\mathrm{q}}/(2w_{\mathrm{s}}L_{\mathrm{g}})$, $V_{\mathrm{dc}}E_{\mathrm{q}}/(2w_{\mathrm{s}}L_{\mathrm{g}})$, respectively.

VITA

Luocheng Wang was born in Nanjing, China, in 1991. He received his Bachelor of Science degree in electrical engineering from University of Connecticut, Storrs, CT, USA, in 2014 and his Master of Engineering degree in electrical and computer engineering from Cornell University, Ithaca, NY, USA, in 2016. Since 2017, he has been working towards his Ph.D. degree in electrical and computer engineering at the University of North Carolina at Charlotte, Charlotte, NC, USA. His current research interests include advanced control of power converters and electrical drives, model predictive control, reliability in power electronics, grid-integration of renewable energy systems, and inductive power transfer.