ANALYSIS OF FAILURE MECHANISMS THAT IMPACT SAFE OPERATION OF ALGAN/GAN HEMTS

by

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ABSTRACT

MICHAEL DAVID HODGE. Analysis of failure mechanisms that impact safe operation of AlGaN/GaN HEMTs.
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The reliability of AlGaN/GaN high electron mobility transistors (HEMTs) is traditionally determined via thermal lifetime acceleration stress tests. More recently it has been proposed that electric field has a prominent role in limiting lifetimes. Multiple failure mechanisms have been proposed as a result of device degradation observed when stressed under high applied electric fields, as typical when the device is biased into the OFF-state. One potential reason for multiple mechanisms could be due to varying levels of quality and maturity of the GaN processes in the reported literature.

The work presented in this dissertation seeks to provide clarity and understanding into the failure mechanism of AlGaN/GaN HEMT devices under high electric fields. The devices in this study were fabricated in a commercial GaN process, notable for exceptional ruggedness and industry leading $65V$ qualified operational bias for RF power amplifiers. A series of OFF-state, high electric field step-stress experiments, as described in literature, were performed to assess if any were applicable to this process.

It was discovered that device degradation could only be induced when stressed close to the breakdown limits. This lead to the development of a unique stress method that enables the device to be held close to catastrophic breakdown, while avoiding an over stress event that would prevent the device from being studied at the conclusion of the experiment. It was discovered via careful electrical and optical analysis that failure was due to a localized degradation of the Schottky gate diode properties. The physical analysis found the failure inconsistent with the widely reported inverse piezoelectric effect. Instead the failures resemble recently proposed time dependent dielectric breakdown of the AlGaN barrier layer.

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CHAPTER 1: INTRODUCTION

This dissertation details a study on semiconductor devices using modern III-V materials and fabrication processes. The semiconductor material system in these devices was the compound gallium nitride (GaN) and it's ternary alloy aluminum gallium nitride (AlGaN). GaN has several attractive properties that make it ideally suited for a wide variety of applications. These include a wide bandgap, enabling the device to sustain high electric fields, a direct bandgap that enables light emission, high charge density and mobility conducting channel, and high mechanical/thermal stability combined with good thermal conductivity.

This chapter will provide a background on GaN materials and advancements. This will be followed by a review of the primary applications suited for GaN based devices. The chapter will conclude with a motivation of work to be detailed in the remainder of the dissertation.

1.1 Gallium Nitride History and Advancements

The earliest reports of gallium nitride formation was in 1932, in publication by Johnson et. al. [1]. However, it wasn't until 1968, when Radio Corporation of America (RCA) began investigations into the feasibility of flat panel displays, did GaN research truly begin. A researcher at RCA, H. Maruska, reported successful epitaxial growth of GaN on sapphire substrates [2], also that GaN was natively n-type material. Additional work from the RCA group proved that GaN would emit light when excited by a laser, a property of direct bandgap materials [3]. Furthermore, it was possible to make GaN p-type by doping the material with magnesium (Mg) [4] and so it was possible to generate electroluminescence [5]. However, while this work

advanced the status of GaN as a potential semiconductor of interest for electronic devices, the material quality was not sufficient for practical applications.

Up until the early 1990s, research involved improving the crystal quality and finding a shallow p-type dopant to enable the manufacture of GaN light emitting diodes (LEDs). The breakthroughs in crystal quality were initially published by Yoshida et al. [6], describing high quality GaN epitaxy, via molecular beam epitaxy (MBE), on sapphire substrates by first growing an aluminum nitride interlayer between the GaN and non-native substrate. This was due to the fact that AlN had a much better lattice match to GaN than the traditional substrates. These findings were eventually applied to growth of GaN epitaxy via metal organic chemical vapor deposition (MOCVD) by Amano et. al. [8]. In this article the two step growth method, widely used in MOCVD growth, was introduced that consists of first growing the AlN buffer layer at lower temperature and then growing the GaN epitaxy at higher temperatures. This work was extended to growth of p-type GaN by demonstrating successful growth via the use of low energy electron beam irradiation (LEEBI) of Mg [9].

These advancements in the growth quality of GaN greatly accelerated research into the feasibility of a wide range of semiconductor devices in power applications in order to harness the many advantages offered by this material system. These applications ranged from optical, power switching, and RF power applications. The possibility of GaN based transistors was realized by Khan et al. [10] in 1990, when it was demonstrated that a high carrier mobility conducting channel could be formed by growing a thin layer of aluminum gallium nitride (AlGaN) on top of the GaN epitaxy forming a highly conductive channel at the interface. Two years after this result the group was able to successfully report on the first AlGaN/GaN high electron mobility transistor (HEMT)[11].

The demonstration of a GaN HEMT enabled the material system to play a significant role in the semiconductor industry. This was solidified further when Nakamura

et. al. [14] was able to report the first high brightness, double heterostructure blue LED in 1994. This same group extended their work to include multi-quantum well structures in 1996 and was able to demonstrate the first GaN laser diode in the same year [15]. The breakthroughs in discovery of both a transistor and LED for GaN would set in motion a torrent of research and publications in the subsequent years exploring the capabilities of the material.

The adoption of GaN into optical applications has been swift with many commercial items from media players to lighting that now include GaN light emitting devices. Despite the progress reported in GaN power and RF electronic devices in the years since Khan demonstrated the GaN transistor, there still remains a vast amount of potential to be unlocked. Nevertheless, even operating at a fraction of it capability these devices offer enhanced performance when compared to competing semiconductor technologies such as silicon (Si) or other III-V based devices.

1.2 Applications of AlGaN/GaN HEMT Devices

The advancements in AlGaN/GaN HEMTs and LEDs has enabled many applications to utilize the unique properties offered by this technology. As was mentioned in the previous section, GaN LEDs and laser diodes have had tremendous success in penetrating the consumer market for a wide range of applications. The push for green energy will continue to enable adoption in the solid state lighting markets. The work presented in this dissertation will focus on the HEMT side of the technology and as a consequence the LED applications are outside of the scope of this work. In this section the applications for GaN transistors will be presented and discussed.

1.2.1 RF Power Applications

As the world increasingly relies on wireless technology the requirements of microwave systems are more demanding. On the consumer side, system bandwidth requirements have become increasingly taxing with the growing popularity of smart phones, tablets, and other mobile media devices. Furthermore in emerging markets

there is a desire for wireless infrastructure for media connectivity in base station applications that further increase demands for bandwidth and power.

The military industry is also a major driver of RF power devices. Applications include phased array RADARs, electronic warfare such as jamming and surveillance, and communications. More recently mechanized warfare and surveillance through the use of unmanned aerial vehicles (UAV) or drones have placed a high demand on cutting edge RF power devices.

Table 1.1: Comparison of material parameters for competing semiconductor technologies in the RF and power electronic markets. Semiconductor materials shown are gallium nitride (GaN), silicon (Si), gallium arsenide (GaAs), and silicon carbide (SiC) [12] [13]

	GaN	Si	GaAs	SiC
E_g (eV)	3.4	1.1	1.4	3.2
E_c (MV/cm)	3.3	0.4	0.4	3
ϵ_r	9	11.9	12.9	10
n_i (cm^{-3})	$1.9X10^{-10}$	$9.6X10^{9}$	$2.1X10^{6}$	$8.2X10^{-9}$
μ_n (cm^2/Vs)	900	1450	8000	600
v_{sat} $(10^7 cm/s)$	2.5	1	1.2	2
Θ_K (W/cmK)	1.3	1.5	0.4	3.3

A comparison of intrinsic material parameters for competing semiconductor materials in the RF and power electronics application space is shown in Table 1.1. The incumbent materials in the field are Si and GaAs. In lower frequency RF applications, such as L-band and S-band, the primary choice has historically been Si. The dominant RF power device in silicon is the lateral double-diffused-metal-oxide-semiconductor field-effect-transistors (LDMOS FETs). However, LDMOS FETs are limited to operation up to 3.5 GHz [16] due to intrinsic material properties.

Beyond S-band, the choice has typically been GaAs due to superior performance for high frequency operation. This may be attributed to the material high carrier mobility as shown in Table 1.1. One drawback to this choice of material is that high power densities are not possible in conjunction with the frequency performance. From

Table 1.1, GaAs has the lowest critical field of the listed semiconductors, limiting the electric field that can be applied to the device. The maximum power density for GaAs devices when operated in S-band has been reported to be 3.4 W/mm [17].

For next generation applications, RF power devices need to offer a combination of high frequency of operation while providing high power densities. This requires that the intrinsic properties have both high electron velocity and high critical electric fields. Wide bandgap materials offer the possibility of achieving this desired combination. The semiconductors of interest from Table 1.1 are GaN and SiC. The superiority of these materials may be demonstrated by applying the Johnson figure of merit (JM) which was published by Johnson et al. [18] as a means of comparing semiconductor technologies as RF power devices based on intrinsic properties. The figure of merit is given by the following equation.

$$JM = \frac{E_c \cdot v_{sat}}{2\pi} \tag{1.1}$$

A plot of the JM for each of the semiconductors in Table 1.1 is shown in Table 1.2, normalized to the JM of Si. This clearly illustrates the potential of GaN and SiC to displace Si and GaAs as the choice semiconductors for RF power applications.

Table 1.2: Johnson figure of merit (JM), normalized to silicon (Si), for the semiconductor materials shown in Table 1.1. This illustrates that wide bandgap semiconductors SiC and GaN have the potential to displace Si and GaAs and the choice semiconductors for RF power applications.

	Si	GaAs	SiC	GaN
JM	$6.37X10^{11}$	$7.64X10^{11}$	$9.55X10^{12}$	$1.31X10^{13}$
Normalized JM	1	1.2	15	20.6

The intrinsic material properties of GaN and SiC may suggest similar performance. However, in practice this is not the case since GaN HEMTs have been demonstrated while the same cannot be said for SiC. The high mobility channel provided by the HEMT structure yields superior performance under high frequency operation. In fact,

the main advantage of SiC when compared to GaN is the high thermal conductivity by more than a factor of 2. As mentioned in the previous section, GaN is grown on non-native substrates via epitaxial growth processes. Because of this GaN may be epitaxially grown on SiC substrates so that the thermal advantages of SiC may be combined with the frequency and power capabilities of GaN.

The high power density allows GaN to match or exceed GaAs power amplifiers with much smaller transistors and less cooling due to thermal properties. This allows for a reduction in both size and weight of a RF module. The record power density for GaN on SiC substrates was reported as 41.4 W/mm at 4GHz [19] and represents an order of magnitude advantage over other semiconductor technologies. In the realm of mm-wave frequencies, GaN has demonstrated a power density of 10 W/mm at 40 GHz [20].

Recently there has been a push to integrate GaN into an array of RF applications beyond power amplifiers. Commercially available GaN RF switches have been offered in recent years [21] and [22]. The intrinsic properties of GaN make it attractive for switches, such as high carrier mobility resulting in low insertion loss (IL), low dielectric constant that minimizes off capacitance and therefore increases isolation (ISO), and the high critical field enables high power operation. The incumbent semiconductor technologies in this space are Si and GaAs. In terms of providing high linearity and broadband performance, GaAs and silicon-on-insulator (SOI) are the primary choices with the limitation being power handling, limited to power levels $<$10 W. Si PIN diode switches are used in high power applications with the drawback of high bias currents needed to achieve low loss and high isolation. This required bias circuitry adds to system cost, size, and power requirements.

GaN switches have demonstrated marked improvement over the incumbent technologies. Broadband switches have been demonstrated, with frequency of operation as wide as DC-18GHz while maintaining $IL$$<1.5dB$ and $ISO$$>30dB$ [23]. High power

switches have been reported with a 0.1 dB compression in IL up to 100 W at 2 GHz [24] demonstrating an order of magnitude improvement over the existing technologies. The only parasitic power draw of GaN switches is associated with the gate leakage current under OFF-state gate bias that typically is on the order of micro amps, resulting in very little power consumption.

1.2.2 Power Switching Applications

Power switching devices are used in an array of power conversion applications that involves transforming a DC voltage to a lower value (buck converter) or to a higher value (boost converter). This may also be extended to converting a power source from AC to DC and vice versa. The critical feature of power conversion devices is the efficiency at which these transformations take place. Two primary losses impact efficiency, conduction and switching losses. Conduction losses occur when the switch is in the ON state and are due to the parasitic resistance of the device, typically referred to as the on-resistance (R_{ON}). The switching losses manifest when the device is transitioning from OFF to ON state and vice versa. The power losses are the product of the current from source to drain and voltage present across the source and drain terminals. In the ON-state the voltage is low (limited by R_{ON}) and the current is high. In the OFF-state, the voltage is high and current is low (limited by small leakage current in the FET). During the transition there is a short period of time where moderate amounts of voltage and current are present that represents a large loss in power. Switching losses may be minimized by reducing the switching times (t_{ON} and t_{OFF}).

Switching losses play a significant role in normal operation and as a consequence, the frequency at which the converter operates (i.e. ON and OFF cycles) is minimized. The penalty is that the lower the switching frequency, the larger the passive components required in the converter. This in turn leads to increases in size and weight. One of the drawbacks of incumbent silicon technology is due to the low cur-

rent density. This requires large area devices to source high currents. As the chip area increases so does parasitic capacitances that lead to increased switching times, resulting in larger switching losses. Therefore, a technology that minimizes switching losses, via increases in switching speed, could greatly reduce size, weight, and cost of a power system by simply operating at higher switching frequencies.

The other limitation of incumbent silicon technology is that operation temperature is normally limited to around $80°C$. The heat generated in the device due to the losses combined with the high ambient temperatures may require the system to have additional cooling capabilities for the power converter system. An example of this would be hybrid electric vehicles, that has separate cooling systems for both the combustion engine and the power inverter system. Wide bandgap technologies can operate at much higher junction temperatures, $250°C$ is typical for GaN and the higher thermal conductivity means removal of heat from the power device is easier. This has the potential to either greatly reduce or even eliminate the cooling systems from some applications greatly reducing weight and increasing range in the electric vehicle example.

When comparing switch devices, a first order comparison is called the power device figure of merit, which is simply V_{BD}^2/R_{ON}. Where V_{BD} is the breakdown voltage of a device. When designing a power device these parameters have an inverse relation to one another, so this tradeoff must be optimized for a given application. Figure 1.1 is a plot of specific on-resistance versus breakdown voltage, with the data points showing reported achieved performance and the lines represent the theoretical limits. It has been demonstrated by silicon that these theoretical limits may be surpassed via optimization in FET architecture. The super-junction architecture [25] is one such way and as seen in Figure 1.1, the work utilizing this approach is already at the theoretical limit. Also, beyond the SJ-MOS limit is the silicon insulated gate bipolar transistor which has been the incumbent device for high voltage switching applications

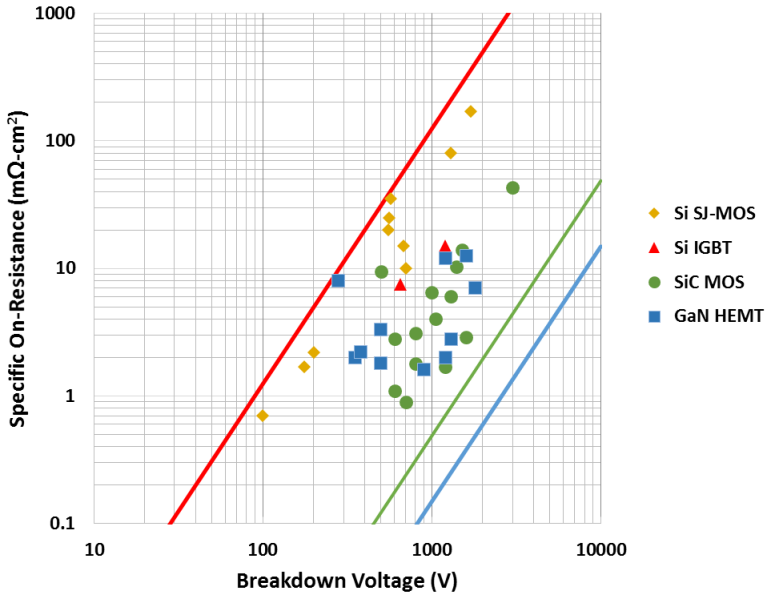

Figure 1.1: Theoretical limits and reported results comparing power switching devices. Resistance is shown as specific on-resistance R_{sp} plotted versus breakdown voltage. Semiconductor technologies compared are silicon (Si), Super-Junction silicon MOSFET (SJ-MOSFET), silicon insulated gate bi-polar transistors (IGBT), silicon carbide (SiC), and gallium nitride (GaN) [26] [28].

in the 600 V and 1200 V range. However, these devices suffer long switching times leading to drops in efficiency due to switching losses.

GaN is a formidable contender to these incumbent Si technologies due to superior critical electric field as was shown in Table 1.1 combined with the low resistance two dimensional electron gas (2DEG) channel, that will be detailed in Chapter 2. This highly conductive, low resistance channel enables for GaN devices to source the same current levels offered by Si technology with much smaller chip area. These small chip sizes not only provide compact solutions but also minimize parasitic capacitances that limit switching speed and, by extension, switching losses. These advantages are represented in Figure 1.1 as the theoretical limit of GaN is well ahead of the competing technologies. The closest semiconductor technology would be SiC. However, it should be noted that this chart does not account for additional performance metrics such as switching losses, power density, frequency capability, and cost. In all of these metrics

GaN has an advantage over SiC except for cost which is on the same order if SiC substrates are used. However, cost can become yet another advantage for GaN by using alternative, cheaper substrates such as Si.

The final challenge that GaN must overcome in power applications to increase adoption and further displace silicon is the development of an enhancement mode (E-mode) (normally off) AlGaN/GaN HEMT without sacrificing performance. Normally OFF devices are preferred and sometimes required in power electronics applications for safety reasons. GaN HEMTs are by nature depletion mode devices (D-mode) (normally on) since the conducting channel is spontaneously created as a consequence of material growth.

There exists a variety of reported methods in literature shown to demonstrate E-mode AlGaN/GaN HEMTs. One common method involves etching a recess in the AlGaN barrier under the gate contact to deplete the underlying channel under the gate contact [29], [30], [31], [32]. Another method involves implantation of negatively charged ions in the gate region, such as fluorine [33]. Also proposed is the growth of additional epitaxial layers above the AlGaN layer, such as InGaN [34], to induce a polarization field to shift the threshold voltage positive. Generally the performance of E-mode AlGaN/HEMTs has been demonstrated as inferior when compared to the D-mode counterparts. This has been attributed to a reduction in the gate voltage swing during operation. To counteract this effect, the use of epitaxial barrier layers, on top of the AlGaN/GaN layers, have been shown to overcome these limitations [34], [35], [36]. Another practical method of achieving normally off operation is by placing a normally OFF FET, such as Si, in cascode with a D-mode GaN HEMT [28]. E-mode GaN power devices have recently been made commercially available, with operation up to 600 V [37].

1.3 Objectives of this Dissertation

AlGaN/GaN devices have made major strides in recent years to displace many incumbent semiconductor technologies in a wide array of power electronics applications. The role of the applied electric field in accelerating device lifetimes and their exact failure mechanisms are not completely understood in literature. As a consequence, this may be seen as limit on GaN technology achieving it's true potential. For example many AlGaN/GaN HEMTs in the market have listed breakdown voltage more than a factor of three higher than the operating bias voltage. The same may also be said of power switching devices, that also show much higher breakdown voltages than specified by the intended application. This suggests that the parts are over designed to meet reliability requirements and that some optimization in the performance vs reliability tradeoff may be better achieved if failure mechanisms due to high applied electric fields are better understood.

Recently there has been discussion in literature about the reliability impacts, especially when switching devices are biased in the OFF-state blocking high RF and DC voltages. These publications have reported a wide variety of results that have led to debate on the actual failure mechanism and their root causes. Because of these varying results there is no clearly understood method of stressing and characterizing devices in the OFF-state.

In this research work the scope was to perform a reliability study on a commercially available and qualified AlGaN/GaN HEMT process that is notable for high breakdown voltage and state of the art power density. The goal was to understand how these devices degrade in the presence of high electric fields. Once degradation is observed it becomes imperative to identify the symptoms of this degradation and how it impacts the device electrically via detailed characterization. From this characterization and analysis a root cause failure mechanism is determined. Any advancement in understanding of device failure could then be used to better assess safe operating

conditions of AlGaN/GaN devices, allowing them to be optimally designed for their intended applications.

CHAPTER 2: ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

This chapter will focus on the details of AlGaN/GaN HEMT fabrication and the physics behind the operation of these devices. It begins with an overview of the intrinsic material properties of Gallium Nitride (GaN). This is followed with a description of the heteroepitaxy of GaN and the alloy, Alumnium Gallium Nitride (AlGaN), and how this leads to the formation of a conductive two-dimensional electron gas (2DEG). Following a discussion on the principles of operations of AlGaN/GaN HEMT devices, the chapter concludes with the fabrication process used to form an AlGaN/GaN high electron mobility transistor (HEMT) as well as an overview of contact formation and properties along with surface passivation.

2.1 Substrates

Ideally, gallium nitride based devices would be grown via homo-epitaxy on native GaN substrates. Recently bulk GaN substrates in 4 to 6 inch diameter wafers have been realized but are still cost prohibitive for large scale manufacturing. As an alternative, cost efficient non-native substrates are used so that GaN HEMTs are grown via hetero-epitaxy. Typical materials for GaN substrates are silicon (Si), sapphire (Al_2O_3), and silicon carbide (SiC).

Table 2.1 shows the mechanical properties of GaN compared to the three most popular materials used as the substrate. The disadvantages of growth on non-native substrates are derived from the inherent lattice mismatch that leads to the formation of threading dislocations in the epitaxial layers. In modern GaN devices, dislocation densities number in the range of $10^{-7} - 10^{-10} cm^{-2}$.

Early in the development of GaN devices, sapphire was the substrate of choice

Table 2.1: Material Parameters of Typical GaN Substrates [41] [42]

Material	Lattice Constant (Å)	Coefficient of Thermal Expansion ($10^{-6}K^{-1}$)	Thermal Conductivity (W/cmK)
GaN	3.19	5.45	1.3
SiC	3.08	4.46	5
Si	5.43	3.59	1.5
Al_2O_3	4.76	7.5	0.5

due to its low cost and mechanically stable properties; sapphire substrates are still popular for GaN optoelectronic applications. However, alternatives to this material are needed for high power devices due to poor thermal conductivity.

Silicon is another low cost substrate option that provides an improvement in thermal conductivity over sapphire. One principle drawback is the large lattice mismatch with GaN that degrades the quality of the GaN epitaxy. Despite this mismatch, additional buffer layers and growth techniques have been developed to improve GaN epitaxy layers grown on silicon. GaN power devices grown on silicon wafers with diameters up to 8 inches hsve been demonstrated [39]. For large scale manufacturing, at low cost, and reasonable device performance, silicon is an attractive option for GaN power devices. The final substrate commonly used for GaN power devices is silicon carbide and is by far the best choice from a performance perspective. SiC has a minimal lattice mismatch with GaN (<5%) which provides for high quality epitaxial GaN films to be achieved during growth without the need of intermediate buffer layers. SiC has an extremely high thermal conductivity that is ten times higher than sapphire and three times higher than silicon or gallium nitride, making it the premier choice for high power devices. SiC wafer sizes lag behind Si as state of the art GaN-on-SiC wafers have been demonstrated up to 6 inches in diameter. Additionally, SiC wafers are substantially more expansive than both Si or sapphire, which currently prevents SiC from becoming the clear substrate choice for GaN devices.

2.2 Bulk Material and Heterojunction Properties

2.2.1 GaN and AlGaN Material Properties

Gallium nitride can be synthesized in two different crystal structures. The first type is a zinc blend structure with a cubic shaped lattice; the second type is a wurtzite structure utilizing a hexagonal shaped lattice. Both crystal types incorporate mechanical strain in the growth process which gives rise to piezoelectric properties that have a large impact on the charge density and electric field distribution within the material[40][43]. In addition to piezoelectric effects, wurtzite materials also possess a very large spontaneous polarization field due lattice charge transfer between the highly electronegative nitrogen atoms and the less electronegative gallium atoms. Depending on the growth method the crystal may be orientated either Ga-face or N-face as shown in Figure 2-1, which determines the polarity of the spontaneous electric field[44]. The devices used in this study were fabricated from Ga-face wurtzite crystal.

GaN crystal growth is achieved via one of two different methods, metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). MBE growth occurs at lower temperatures in the 600-900$°C$ range. The process is highly controlled as the crystal is deposited one atomic layer at a time. However, this means that growth is very slow. The MOCVD method has several advantages over MBE. MOCVD growth is fast, at a rate of a few micrometers per hour, with multi-wafer capability easy to integrate. MOCVD growth temperatures are high, on the range of 1000-1100$°C$, which is thermodynamically favorable. Finally, the overall quality of GaN epitaxy layers is high when compared to MBE. Due to these numerous advantages MOCVD is the dominant growth method for commercial GaN devices.

Both GaN and the alloy AlGaN are wide bandgap materials with high critical electric fields. The bandgap of GaN is 3.4 eV and the bandgap of $Al_xGa_{1-x}N$ depends on the ratio of Al to Ga in the alloy. This can be determined from equation 2.1[44].

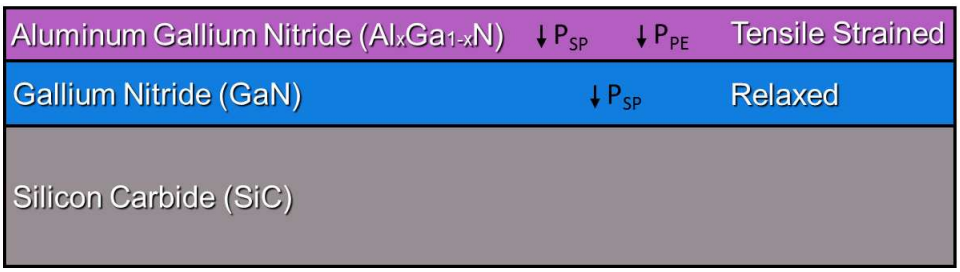

Figure 2.1: Polarization fields in typical AlGaN/GaN heterostructure. P_{SP} represents the spontaneous polarization that is inherently present in all III-N compounds. P_{PZ} denotes the piezoelectric polarization that is present in the strained epitaxial layer.

$$E_g(x) = x6.13eV + (1-x)3.42eV - x(1-x)1.0eV \tag{2.1}$$

Both GaN and AlGaN have very high critical electric fields of 3 MV/cm for GaN and up to 11 MV/cm for AlGaN depending on the ratio of Al and Ga. Both GaN and AlGaN are very stable materials both mechanically and electrically over a wide range of temperatures. Electrical stability with temperature may be illustrated by defining the temperature at which the intrinsic carrier concentration reaches $10^{15}cm^{-3}$ as the threshold which the semiconductor becomes as conductor. Silicon reaches this intrinsic carrier concentration at $315°C$ while GaN retains its semiconducting properties up to $1300°C$. [13] [45].

2.2.2 AlGaN/GaN Spontaneous and Piezoelectric Polarization Fields

AlGaN/GaN HEMT formation starts with the growth of a thin layer of AlGaN ($\sim$ 20 nm) on top of a thick layer of GaN ($\sim$ 1 μm). An example of the epitaxial stack and the polarization fields is shown in Figure 2.1. The spontaneous polarization is present in both layers due to inherent properties described in the previous section. The spontaneous polarization in GaN is $-0.029\ C/m^2$, while the spontaneous polarization in the AlGaN layer can be calculated from equation 2.2.

$$P_{SP}(x) = (-0.052x - 0.029)C/m^2 \tag{2.2}$$

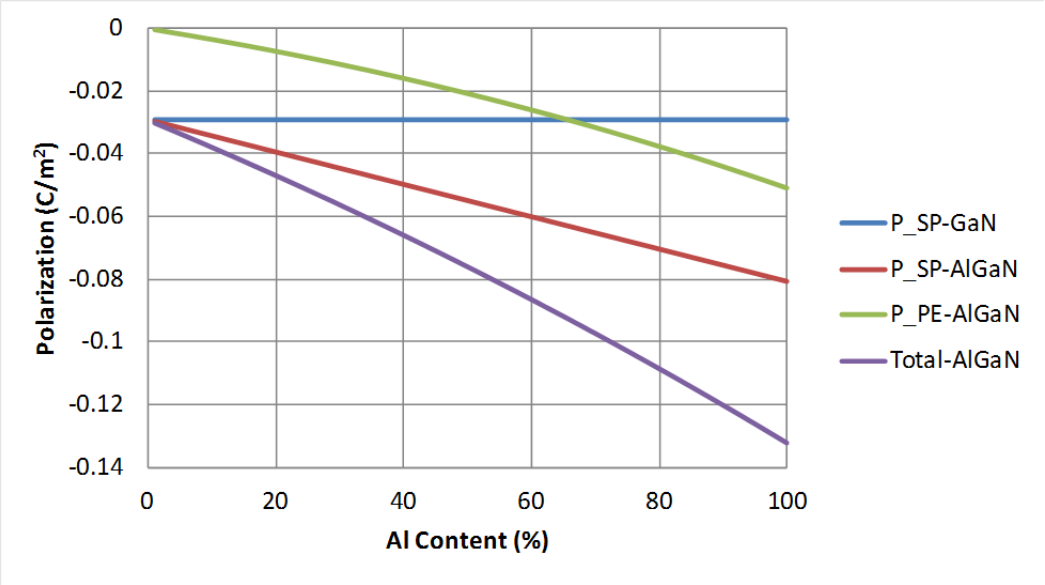

Figure 2.2: Calculated polarization fields in AlGaN and GaN epitaxial layers in a AlGaN/GaN heterostructure as a function of Al content. Since P_{SP} and P_{PZ} in the AlGaN layer have the same polarity, the total magnitude is the sum of both fields.

The second polarization field present in the heterostructure is the piezoelectric polarization due to strain present in the epitaxial layers. The lattice constant of AlGaN is smaller than that of GaN so the epitaxial AlGaN layer is tensile strained when grown on top of GaN. No piezoelectric polarization is present in the GaN layer due to its relaxed state. The piezoelectric polarization field can be calculated by using equation 2.3.

$$P_{PE} = 2\left(\frac{a - a_0}{a_0}\right)\left(e_{31} - \frac{e_{33}C_{13}}{C_{33}}\right) \tag{2.3}$$

In this equation the $2(a - a_0)/a_0$ term represents the in-plane strain, a_0 is the intrinsic lattice constant, and a is the deformation lattice constant due to strain. The terms e_{13} and e_{33} represent the piezoelectric coefficients while C_{13} and C_{33} represent the elastic coefficients. A summary of the these terms for both GaN and AlGaN are given in Table 2.2.

A plot of the calculated polarization fields in both AlGaN and GaN epitaxial

Table 2.2: Lattice Constants and Piezoelectric Coefficients for AlGaN and GaN [44].

	GaN	AlGaN
$a_0(\mathring{A})$	3.19	$-0.077x + 3.189$
$C_{13}(GPa)$	103	$5x + 103$
$C_{33}(GPa)$	405	$-32x + 405$
$e_{13}(C/m^2)$	3.08	$-0.11x - 0.49$
$e_{33}(C/m^2)$	5.43	$0.73x + 0.73$

layers versus Al content is shown in Figure 2.2. Note that as Al content increases so does the spontaneous and piezoelectric fields in the AlGaN layer. Also, since the polarity of both of the spontaneous and piezoelectric fields are the same they combine to increase the magnitude of the total field.

A polarization gradiant gives rise to a sheet charge density given by $\rho_P = \nabla P$. As seen in Figure 2.3 there exists an abrupt change in polarization at the AlGaN/GaN interface. The polarization sheet charge is generally defined as:

$$\sigma = (P_{SP_{top}} + P_{PE_{top}}) - (P_{SP_{top}} + P_{PE_{bottom}}) \tag{2.4}$$

In the typical case of tensile strained AlGaN epitaxially grown on top of relaxed GaN, the equation becomes:

$$\sigma = (P_{SP_{AlGaN}} + P_{PE_{AlGaN}}) - (P_{SP_{GaN}}) \tag{2.5}$$

This indicates that at the AlGaN/GaN heterointerface there exists a permanent fixed polarization sheet charge. As the Al content of AlGaN increases, so does the magnitude of the sheet charge at the interface.

2.2.3 Two Dimensional Electron Gas (2DEG) Formation

As shown earlier in the chapter, both GaN and AlGaN are inherently electrical insulators. Therefore, the material system relies on the polarization fields detailed in the previous section to form a conductive channel at the hetero-interface. The

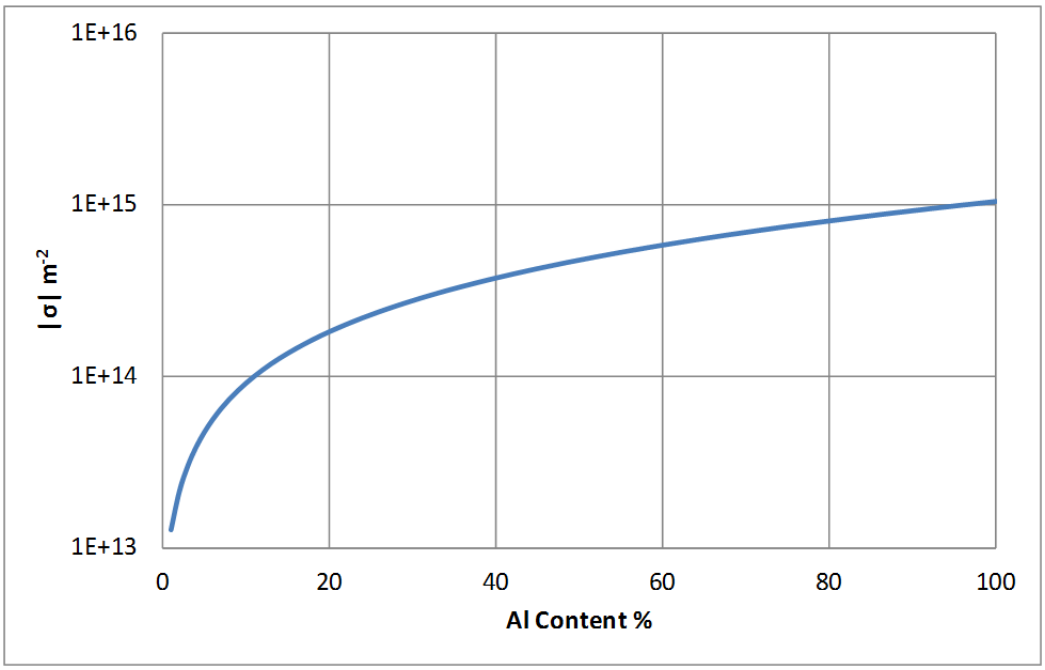

Figure 2.3: Calculated polarization sheet charge density as a function of Al content in the AlGaN barrier layer [44].

polarization fields in both the AlGaN/GaN epitaxy (Ga-face) give rise to a highly positive sheet charge density. Electrons are then attracted by this positive sheet charge so that the electrons become spatially confined at the hetero interface as shown in Figure 2.4. These confined electrons are quantized in two dimensions, leading to the formation of a two dimensional electron gas (2DEG) on the GaN side of the interface.[44]

Electrons in the 2DEG are sourced by the donor-like states at the surface of the AlGaN epitaxy according to the following. First, spatial charge within the structure must sum to zero, meaning the structure is charge neutral. Second, the polarization induced charge constitutes a dipole, meaning that the net contribution to the space charge is zero. Third, the buffer charge must be negative or charge will not remain confined to the hetero interface; the buffer charge is intentionally minimized so that it may considered negligible [46]. If the AlGaN barrier layer is undoped, as is typical in modern GaN heterostructures, the charge in the AlGaN can be considered to be

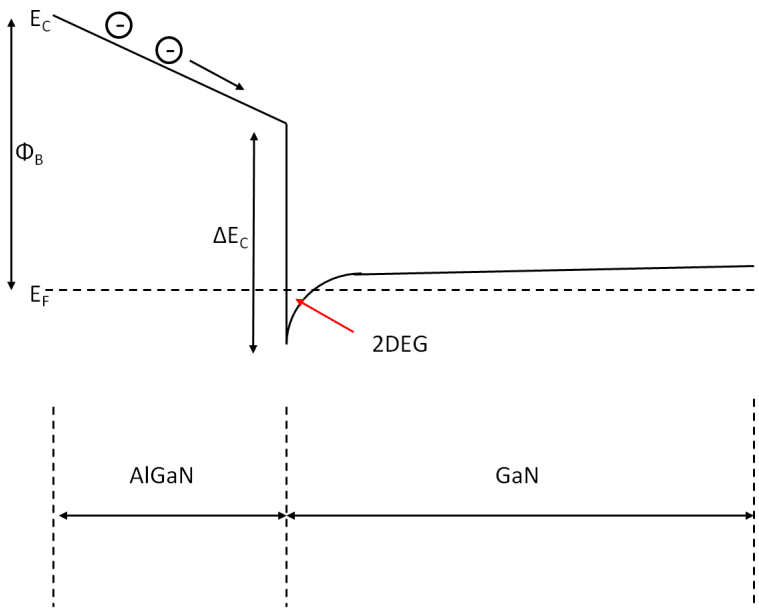

Figure 2.4: Conduction band diagram for the AlGaN/GaN heterointerface.

zero. Therefore the final charge balance equation that must be satisfied is:

$$\sigma_{Surface} - qn_s = \sigma_{Surface} - \sigma_{2DEG} = 0 \tag{2.6}$$

Where qn_s is the charge in the 2DEG. The maximum sheet carrier concentration in the 2DEG in an undoped structure is given by [46]:

$$n_s(x) = \left(\frac{\sigma(x)}{e}\right) - \left(\frac{\epsilon_0\epsilon(x)}{de^2}\right)[e\phi_b(x) + E_F(x) - \Delta E_C(x)] \tag{2.7}$$

In this equation, d is the width of the AlGaN barrier and $e\Phi_b$ is the Schottky-Barrier height of the gate contact. The Fermi level with respect to the GaN conduction band is given by E_F and the conduction band offset between AlGaN/GaN is given by ΔE_C. [44]

Equation 2.7 shows that the number of carriers in the 2DEG must be equal to the number of positive charges on the AlGaN surface in an undoped heterostructure. Therefore, the surface states can be considered donor-like such that they are neutral when occupied by an electron and positively charged when ionized. The donor-like

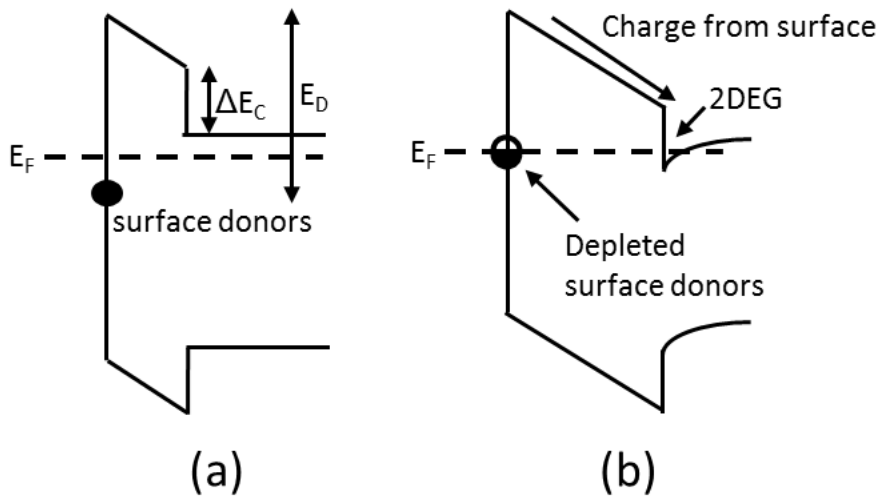

Figure 2.5: Band diagram in an undoped AlGaN/GaN heterostructure. (a) Band diagram when the AlGaN barrier thickness is not sufficient thickness to induce a 2DEG. (b) Band diagram in the case of the AlGaN thickness surpassing the critical thickness necessary to induce a 2DEG. [46].

surface states then have an energy, E_D, below the conduction band when filled as shown in Figure 2.5a. The occupancy of the surface states and by extension the charge, in the 2DEG depends on the E_D relative to the Fermi level E_F. If E_D is sufficiently deep and below the Fermi level, then no 2DEG will form since $\sigma_{Surface} = \sigma_{2DEG} = 0$. At a critical AlGaN barrier thickness the surface donor-like states will reach the Fermi level and begin to ionize by transfer electrons to the empty conduction band states at the AlGaN/GaN interface, thus forming the 2DEG.

The critical thickness, t_{CR}, necessary to induce a 2DEG is given by the following equation.

$$t_{CR} = (E_D - \Delta E_C)\frac{\epsilon}{q\sigma_{PZ}} \tag{2.8}$$

Where ϵ is the AlGaN relative dielectric constant and ΔE_C is the AlGaN/GaN conduction band offset. The 2DEG density as a function of barrier thickness is given by the following equation.

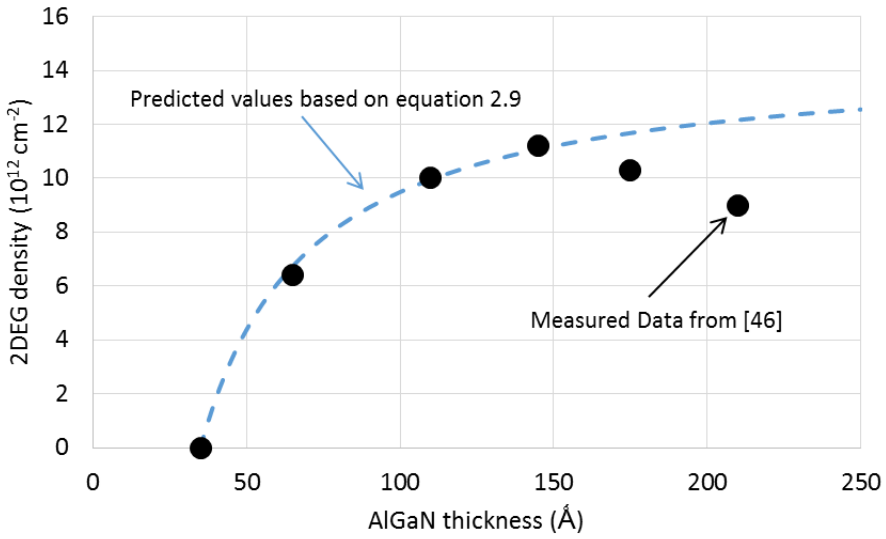

Figure 2.6: Experimentally measured room temperature 2DEG density as a function of $Al_{0.34}Ga_{0.66}N$ barrier thickness. The solid line is calculated from Equation 1.9.[46].

$$qn_s = \sigma_{PZ}\left(1 - \frac{t_{CR}}{t}\right) \tag{2.9}$$

As can be seen in Figure 2.6, n_s rapidly increases once the critical thickness is exceeded as the surface states E_D crosses the Fermi level before finally saturating at σ_{PZ}/q for $t \gg t_{CR}$ once all of the donor-like surface states have been emptied [46].

The formation of the conducting channel in AlGaN/GaN HEMTs is shown to be primarily dependent on two factors. These factors are the Al mole fraction in the AlGaN barrier layer and thickness of the AlGaN barrier layer. An upper limit to AlGaN barrier thickness does exist due to epitaxial strain caused by the lattice mismatch between GaN and AlGaN. Since the lattice mismatch is a function of Al mole fraction, higher Al concentrations come at the expense of a reduced upper limit to the critical thickness. Once this thickness is exceeded, the AlGaN barrier layer will relax via cracking which in turn reduces the piezoelectric component to polarization and thus degrades the 2DEG charge density.

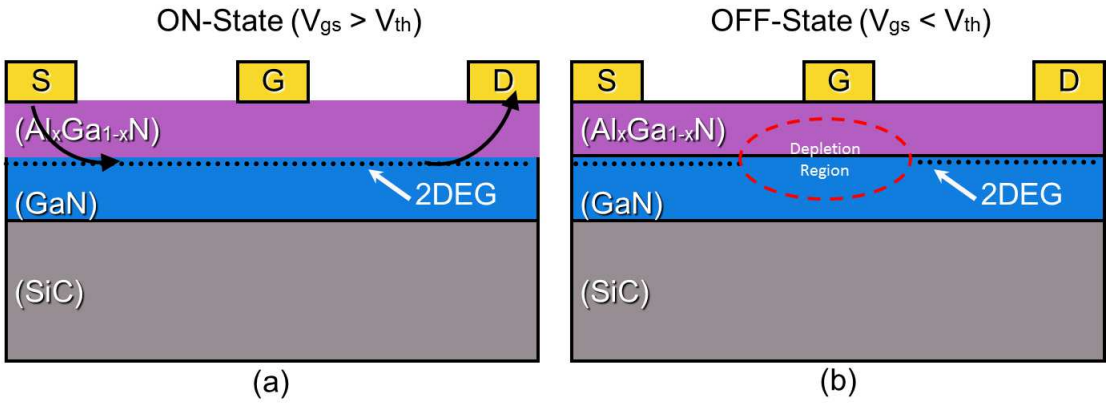

Figure 2.7: Basic operation principles of a AlGaN/GaN HEMT. (a) ON-state condition, when gate bias is more positive than the threshold voltage. (b) OFF-state condition when the gate bias is more negative than the threshold voltage.

2.3 AlGaN/GaN High Electron Mobility HEMT Operation

Previous sections have described how the AlGaN/GaN epitaxy layers generate a sheet of highly mobile electrons that are ideally suited to act as a conducting channel for a three terminal FET device as shown in Figure 2.7. The AlGaN/GaN HEMT has the traditional gate, source, and drain contacts found in the classical metal-oxide-semiconductor field effect transistor (MOSFET). Operation consists of the device operating in the ON-state when gate bias is more positive than the threshold voltage. In this state, the device 2DEG remains continuous allowing the flow of electrons from the source ohmic terminal to the drain ohmic terminal as seen in Figure 2.7a. The device OFF-state is induced when the gate bias is more negative than the threshold voltage. The negative bias in this case is sufficient to deplete the electrons in the 2DEG below the gate terminal leading to an electrical discontinuity between the source and drain terminals, shown in Figure 2.7b.

Since the 2DEG is present as a consequence of the epitaxial growth, the device is in the ON-state when no bias is applied. This makes all AlGaN/GaN HEMTs natively depletion mode devices. This is in contrast to traditional MOSFET devices that are enhancement mode devices, requiring a positive gate bias to be applied to

turn the device ON.

2.3.1 Ohmic Contacts

The source and drain contacts on an AlGaN/GaN HEMT are ohmic, meaning that the metal-semiconductor junction has a linear current-voltage behavior as described by Ohm's law. These contacts provide access to the conductive channel of the device providing a path for electrical current to flow.

Ohmic contacts are formed through the deposition of thin metals on the semiconductor surface that are then rapidly annealed at high temperature to alter the metal semiconductor interface and make the junction ohmic. In AlGaN/GaN semiconductors thin layers of Ti/Al were initially discovered to provide reasonable contact resistances [47]. Subsequent studies introduced additional metal layers to the ohmic stack while demonstrating improved contact resistances. These additional layers on top of the Ti/Al layers consist of a diffusion barrier such as titanium (Ti), nickel (Ni), molybdenum (Mo), or platnium (Pt) before completing the stack with a final gold (Au) layer [48] [49] [50].

Typical AlGaN/GaN semiconductor processes deposit the metals via electron beam evaporation under vacuum to maximize the quality and maintain a high degree of control on the final metal thickness. Contacts are defined via a metal photoresist liftoff process. The deposited contacts are then alloyed in a rapid thermal anneal oven at temperatures that depend on the specific process and can range from $650°C$ to $850°C$. During the anneal an inert gas such as Ar or N is forced into the oven to prevent oxidation of the contact.

The physical mechanism that leads to the formation of low resistance contacts is understood as follows. During the anneal process, the Ti layer in contact with the semiconductor surface diffuses into the semiconductor forming a TiN alloy that is metallic in nature and has a low work function. The formation of TiN at the semiconductor surface directly leads to the generation of nitrogen vacancies. These

vacancies lead to heavy doping of the GaN, effectively thinning the barrier, and provides for a low impedance path to the device 2DEG [51]. The layers at the top of the stack alloy into a stable composite for high temperature applications.

2.3.2 Schottky Contacts

The gate contact on an AlGaN/GaN HEMT acts to modulate the device channel and sets the state of operation. To accomplish this task, the gate contact must have rectifying properties similar to that of a diode. Therefore, unlike the ohmic drain and source contacts, the gate contact is engineered to have a Schottky barrier at the metal-semiconductor junction. An illustration of the band diagram of a metal-semiconductor Schottky junction is shown in Figure 2.8. The gate contact plays a significant role in device performance and reliability as will be discussed in detail in subsequent chapters.

Fabrication of Schottky contacts is similar to the ohmic contact process. A metal stack is deposited on the semiconductor surface, typically via electron beam deposition under high vacuum. Contacts are defined via metal liftoff. Unlike ohmic contacts, no metal annealing is performed after deposition. Several metals have been found to form a Schottky barrier on GaN. The classical metals and their respective metal work functions (ϕ_m) are gold (5.1 eV), palladium (5.12 eV), nickel (5.15 eV), and platinum (5.65 eV) [52]. The contact is then completed with a layer of Au on the top to minimize impedance with an appropriate Au diffusion barrier in the middle to prevent Au from mixing with the Schottky metal.

When the gate is either reverse or forward biased, it is possible for electrons to overcome the Schottky barrier (Φ_B) and transport across the junction. Electron transport is not desired under ideal operating conditions and should be minimized to maximize both performance and reliability. In the presence of low to medium electric fields, transport across the junction is dominated by thermionic emission [12] and is generally the most common emission observed during normal operation

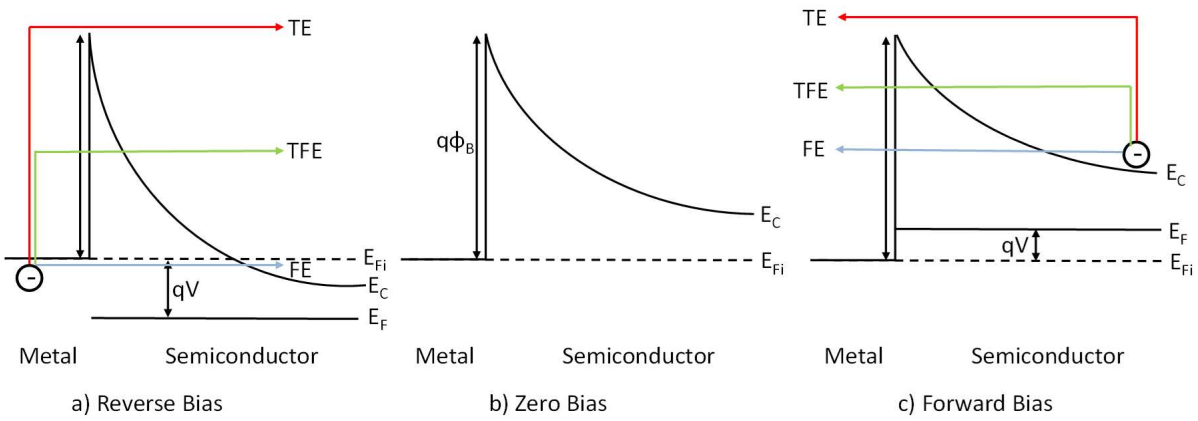

Figure 2.8: Band diagram illustrating the metal-semiconductor junction of Schottky contact. a) Junction is reverse biased. b) Zero bias on the metal-semiconductor junction. c) Forward bias Junction. The colored arrows in the reverse and forward bias show schematically how the electron transport across the barrier could occur. These mechanisms are thermionic emission (TE), thermionic field emission (TFE), and field emission (FE).

of AlGaN/GaN devices. The thermionic emission equation for total current density across the Schottky barrier is given by

$$J_n = \left[A^* T^2 exp\left(\frac{-q\phi_B}{kT}\right)\right]\left[exp\left(\frac{qV}{kT}\right)\right] \tag{2.10}$$

Where A^* is the Richardson constant for thermionic emission and is material specific, T is the ambient temperature of the device, k is the Boltzmann constant, and ϕ_B is the Schottky barrier height [12].

In operation at low temperatures, other transport mechanisms which involve the electron tunneling through the barrier to arrive at the opposite side of the metal-semiconductor junction are dominant. When the electron tunnels directly across the Schottky barrier, aided only by the applied electric field, it is called field emission. Transport across the junction via a combination of both applied electric field and thermal energy is called thermionic field emission[12].

The current density due to field emission transport is given by the following equation.

$$J_{FE} = A^* \left(\frac{E_{00}}{k}\right)^2 \left(\frac{\phi_B + V_R}{\phi_B}\right) exp\left(\frac{2q\phi_B^{3/2}}{3E_{00}\sqrt{\phi_B + V_R}}\right) \tag{2.11}$$

The current density due thermionic field emission is given by the following equation.

$$J_{TFE} = \frac{A^*T}{k}\sqrt{\pi E_{00} q\left[V_R + \frac{\phi_B}{cosh^2\left(E_{00}/kT\right)}\right]}\left(exp\frac{-q\phi_B}{E_0}\right)\left(exp\frac{qV_R}{\epsilon'}\right) \tag{2.12}$$

where

$$\epsilon' = \frac{E_{00}}{(E_{00}/kT) - tanh(E_{00}/kT)} \tag{2.13}$$

$$E_{00} = \frac{h}{2}\sqrt{\frac{N_D}{m^*\epsilon_S\epsilon_0}} \tag{2.14}$$

When fabricated as a lateral device, meaning the gate, source, and drain contacts are all on the same surface of the device, electrical current may flow between the gate and ohmic contacts under bias. When the gate diode is forward biased with respect to the drain and the source, electrons may be thought of as flowing from the ohmic contacts to the gate contact. Under reverse bias conditions the opposite would be true with the electrons flowing from the gate contact to the ohmic contacts. Two paths for conduction are possible and both are illustrated in Figure 2.9. The first path is across the AlGaN barrier to the device 2DEG and from there the electrons may travel to the source or drain contact through a low impedance path. The second path follows the AlGaN surface from the gate contact to the ohmic contact.

In the forward bias case the electrical current fits the thermionic emission model and is understood to be the physical mechanism by which current flows under typical operating conditions and temperatures of an AlGaN/GaN device. The mechanism by which current flows in the device when the gate diode is reverse biased with respect

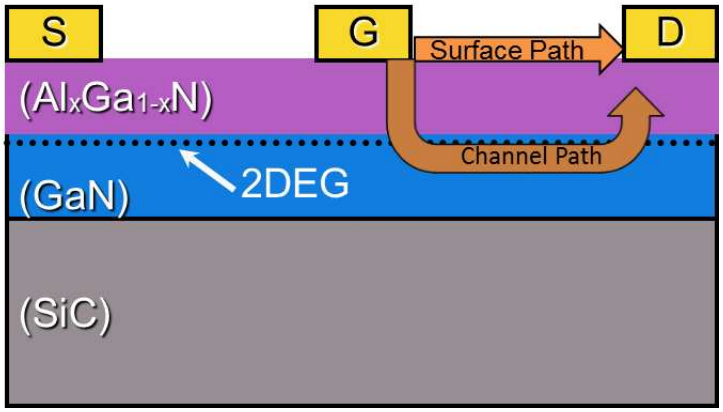

Figure 2.9: Schematic cross section of the device showing the two conduction paths available for electrical current to flow from the gate contact to either ohmic contact. Current flow from gate to drain is pictured.

to the ohmic contacts is still a subject for debate that has not been completely understood in literature.

The field emission (FE) and thermionic field emission (TFE) mechanisms in AlGaN/GaN HEMTs assume that the metal-semiconductor junction is heavily doped ($N_D > 10^{17} cm^{-3}$) [53]. However, this doping concentration typically does not exist as the 2DEG can formed without doping the AlGaN layer. Despite this fact there exist publications that have shown the reverse leakage characteristics can be fitted to the FE/TFE models. In these works the authors fit the model to measured values by assuming the barrier doping as $N_d = 1X10^{17} cm^{-3}$ in [54] and $N_d = 1.4X10^{19} cm^{-3}$ in [55]. The high doping assumptions in the AlGaN barrier are rationalized by the introduction of the "thin surface barrier" model [56]. This thin surface barrier model states that a high density of defect donors are present at the AlGaN surface due to nitrogen vacancies. This acts to reduce the width of the Schottky barrier to enable the probability of electron tunneling to occur under reverse bias conditions. The precise mechanism in this model is dependent on ambient temperature with FE transport said to occur below $250K$ and TFE above this temperature.

Similar to the FE transport is Fowler-Nordheim tunneling which has been shown

to fit reverse Schottky diode leakage at low temperatures [58]. The current density due to Fowler-Nordheim is given by the following equation.

$$J = E_b^2 \left(\frac{q^2(m_e/m_n^*)}{8\pi h \phi_b} \right) exp \left(-\frac{8\pi E_b \sqrt{2m_n^*(q\phi_b)^3}}{3qh} \right) \tag{2.15}$$

Where E_b is the electric field in the AlGaN barrier layer, q is the charge of an electron, m_e is the free electron mass, m_n^* is the conduction band effective mass in the semiconductor, h is Planck's constant , and ϕ_b is the effective barrier height at the Schottky contact [58]. Experimentally, the data in [58] shows that a very weak temperature dependence is present in reverse leakage current measured from $110K$ to $130K$ and was shown to fit the Fowler-Nordheim model.

An alternative model proposed to explain reverse leakage current are the trap-assisted tunneling and thermionic trap assisted tunneling models and have been shown to match the reverse leakage observed in AlGaN/GaN Schottky diodes [57]. In these models the trap-assisted tunneling model suggests that an electron may tunnel through the Schottky barrier by hopping to an intermediate trap state available in the bandgap and then continue traveling to the conduction band of the AlGaN from this trap state. The thermionic trap assisted tunneling model is identical except that it proposes that the electron is thermally excited prior to entering the bandgap trap state and crossing the AlGaN barrier in a region of triangular barrier that is thinner. An illustration of these mechanisms is shown in Figure 2.10.

An extension of trap assisted tunneling methods that has also been utilized to explain gate leakage current is the Poole-Frenkel mechanism [58], [59]. Poole-Frenkel conduction is explained as the emission of trapped electrons, from a continuum of trap states, into the conduction band via thermal excitation and may be enhanced by the applied electric field [60]. Poole-Frenkel has been referenced to explain both vertical [58] and lateral [59] conduction paths, in observed leakage from studies in literature, that are illustrated in Figure 2.9.

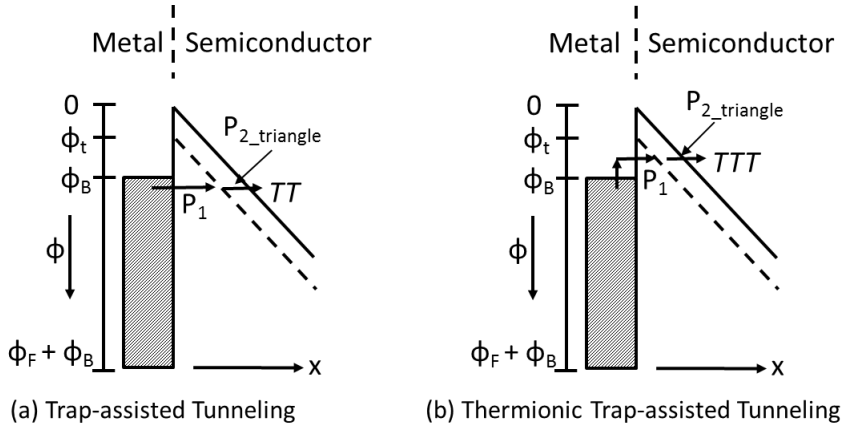

Figure 2.10: (a) Illustration of trap-assisted tunneling mechanism. (b) Thermionic trap-assisted tunneling mechanism. [57]

The total current density due to Poole-Frenkel emission is given by the following equation [58]

$$J = CE_b \left[-\frac{q\left(\phi_t - \sqrt{qE_b/\pi\epsilon_0\epsilon_s}\right)}{kT} \right] \tag{2.16}$$

Where E_b is the electric field in the semiconductor barrier at the metal-semiconductor junction, ϕ_t is the barrier height for electron emission from the traps state, ϵ_0 is the permittivity of free space, ϵ_s is the relative dielectric permittivity of the AlGaN barrier at high frequency, T is the temperature and k is Boltzmann's constant.

The expression for current density as a function of applied bias may be written as:

$$J = Vexp\left(\frac{2a\sqrt{V}}{T} - \frac{q\phi_t}{kT}\right) \tag{2.17}$$

where

$$a = \sqrt{\frac{q}{\pi\epsilon_0 d}} \tag{2.18}$$

In this equation V is the bias that is applied to the gate terminal and d is the thickness

of the AlGaN barrier. Reverse current leakage experimentally measured is then fitted to the above equations. Such fits have been demonstrated in literature and is typically shown on a log scale versus the square of the applied voltage or electric field so that a linear trend may be observed. Examples in literature exist that show a fit to Poole-Frenkel as both a function of applied electric field and temperature [58], and fitting both vertical and lateral gate diode leakage current[59]. By extrapolating the fit data back to the zero bias condition on the gate ($V_{gs} = 0V$) a trap barrier height (ϕ_t) may be extracted from the model. In the cited works, the trap barrier height was estimated to be 0.26 eV for conduction along the AlGaN surface [59] and 0.30 eV for leakage across the AlGaN barrier [58]. Furthermore it was suggested in the latter study that the emission of electrons from the trap state was due to a continuum of electrical states, not in the AlGaN barrier.

If the continuum of trap states were to be located in the AlGaN barrier then it would require that the trap states be located $0.30eV$ below the conduction band in the AlGaN. If this were true, then the trap level would be located $0.8 - 0.9eV$ above the metal Fermi level, in which case the thermal emission of carriers from the metal into the trap state would be the key mechanism allowing the flow of leakage current. This is an unlikely process under reverse bias conditions [58]. Therefore, the authors explain that the reverse leakage current occurs through Poole-Frenkel emission from a state within the AlGaN such as a trap state near the metal-semiconductor interface into a continuum of states associated with conductive dislocation, such as nitrogen vacancies. Another study found the magnitude reverse leakage current to be correlated to the threading dislocation density in the AlGaN barrier layer. In this work it was reported that by reducing the threading dislocation density from $2X10^{10}\ cm^{-2}$ to $5X10^{7}\ cm^{-2}$ led to a decrease in mean reverse leakage by a factor of 45 [62].

In summary, the forward conduction of a Schottky gate contact on an AlGaN/GaN HEMT may be sufficiently described by the thermionic emission theory. The reverse

leakage current is still a subject for debate and not completely understood. Several different works have found that the reverse leakage may be sufficiently described by a variety of mechanisms which may mean that the dominant mechanism is dependent on the specific material that is studied.

2.3.3 AlGaN/GaN HEMT Traps and Surface Passivation

Carrier trapping in AlGaN/GaN HEMTs has been identified in literature as a performance limiting phenomena and leads to a variety of observations which include current dispersion, compression, and power slump. In a power semiconductor device the output power may be estimated by the following equation.

$$P_{out} = \frac{I_{max}(V_{BD} - V_{knee})}{8} \tag{2.19}$$

In this equation I_{max} is the max current output by the device in the saturation region, V_{knee} is the voltage at which the device transitions from the linear region to the saturation region on the I-V curve. The term V_{BD} is defined as the breakdown voltage of the device. When operated under RF or pulsed conditions the DC I-V parameters for a device have been observed to dynamically change and therefore lead to a reduction of output power that is achieved by the device. This observation is wide spread in the literature and is revealed by characterizing the device with a pulsed-IV system. In a pulsed I-V test, the device is DC pulsed from a quiescent bias point, typically chosen for a desired RF power operating condition. The device is then pulsed to various points on the I-V plane. With each pulsed the I-V curve collapses so that max current is continuously reduced along with an increase in knee voltage, and as a result the output power drops. The reduction is due to filling of trap states in the device, so the reduction in drain current is used to quantify the trap state density. This test is used as a proxy for behavior that happens to the device under RF drive.

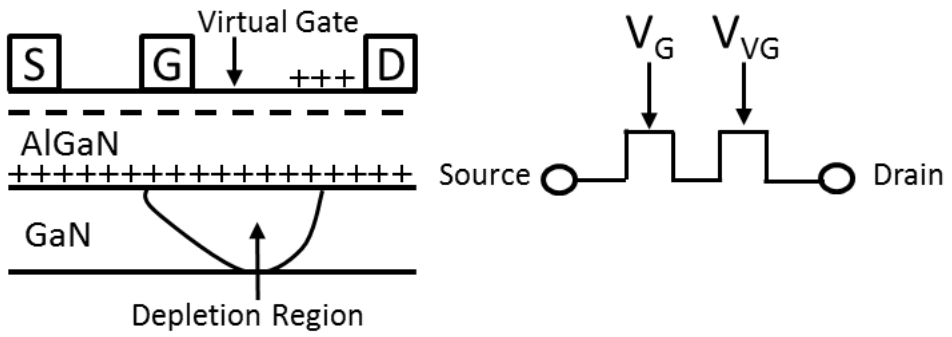

Figure 2.11: Illustration of the virtual gate mechanism described in [63] used to explain the trapping phenomena observed during RF operations and pulsed IV characterization.

The virtual gate phenomena has been used to explain the mechanism by which trapping leads to degradation effects observed during RF operation [63]. As detailed earlier in this chapter, during the growth of the AlGaN/GaN epitaxial layers, the formation of the channel 2DEG gives rise to a sheet of positive surface charge so that charge balance may be achieved in the heterostructure. This positive sheet can arise from ionized donor states at the surface. The virtual gate mechanism states that electrons sourced from the gate metal may be trapped by the ionized donor states that are present on the surface of the semiconductor. These trapped charges on the surface act as a second "virtual gate" and exert a negative potential on the underlying 2DEG and in turn depletes charge from the channel.

The mechanism by which trapping occurs also has been shown to have an opposite de-trapping mechanism by which charge is removed from the virtual gate and restored to the gate metal. Trapping was shown to occur under off-state conditions with high bias applied to the device, while de-trapping occurs when the device was biased into open channel conditions $V_{gs} = 0V$ [63]. This implies that the trapping is heavily dependent on the electric field that is present between the gate and drain contacts. As charge is collected in the virtual gate, it acts to deplete the underlying charge in the 2DEG which leads to a reduction of the electric field at the drain edge of the gate

contact and therefore reducing the rate by which electrons are trapped in the surface states.

The concept of virtual gating may also be extended to the GaN buffer layer below the device 2DEG [64]. These trap states are shown to be deep states and physically far from the AlGaN/GaN interface [65]. The time constants associated with these trap states in the bulk GaN of the semiconductor have been demonstrated to be very long, on the order of minutes to hours. As a consequence they can have similar impacts on performance due to surface trapping [66]. However, advancements in substrate quality and epitaxial growth techniques have greatly mitigated the effects of bulk trap states.

In order to mitigate the effects of surface trapping, surface passivation was introduced and becomes a critical process step in the fabrication of AlGaN/GaN HEMTs. Experimentally, it has been shown that proper passivation with silicon nitride (Si_3N_4), mitigates effects such as dispersion, current degradation, and power droop [63], [64]. Even with surface passivation there still exist states at the AlGaN/SiN interface that may trap charge and therefore lead to virtual gating effects. So high quality passivation with minimal interface states is crucial during device fabrication. This means that surface passivation recipes and materials may vary significantly in different GaN processes, but SiN passivation is by far the most widely used. Deposition of the passivation layer is recommended to occur as early in device processing as possible as the deposition techniques, typically plasma enhanced chemical vapor deposition (PECVD), exposes the surface to ions and other potential contaminants [67].

The exact mechanism by which surface passivation reduces the effect of virtual gating is not clearly understood in literature. Some mechanisms were proposed by Vetury et al. [63] that include the following. The passivant buries the surface donors and makes them inaccessible to the electrons that may leak from the gate metal contact. Another possibility, in the case of silicon based passivants (Si_3N_4 and SiO_2),

is that the deposition process causes Si to incorporate as a shallow donor at the AlGaN surface in large enough quantities to replace the surface donors.

2.4 Summary

In this chapter the fundamental choices and tradeoffs of substrates and basic material growth were discussed. Also detailed was the physics at work during the epitaxial growth of the AlGaN/GaN layers that give rise to the polarization charge and two dimensional electron gas that comprises the conduction channel in a AlGaN/GaN HEMT. A HEMT is fundamentally a three terminal FET device that includes source and drain ohmic contacts with a Schottky gate contact. The Schottky gate contact was highlighted as a critical component that decides device performance and reliability. A detailed review of the conduction mechanism and theories governing forward and reverse leakage currents was discussed. Finally, the chapter concluded with a discussion on trapping by describing the effects and underlying mechanisms proposed in literature and how they may be mitigated through surface passivation.

CHAPTER 3: ALGAN/GAN HEMT RELIABILITY OVERVIEW

This chapter will begin with a review of considerations when determining the reliability of AlGaN/GaN HEMTs. This includes aspects such as operational bias points and their associated applied stresses. Next will be an introduction of AlGaN/GaN reliability motivations and considerations. Then a review of OFF-state reliability literature will be presented which includes the inverse piezoelectric effect and time dependent degradation that has been observed in literature.

3.1 AlGaN/GaN HEMT Operation and Resulting Stresses

The goal of reliability is to predict how long the studied object may be expected to perform it's desired task under a set of defined operating conditions. To achieve this goal, the reliability assessment must begin with a survey of known conditions under which the device will operate. This may include a wide variety of factors for a semiconductor device. Examples include environmental, such as ambient temperature and humidity, along with electrical conditions, such as electric field and current. Equally important is what defines the failure of a device under study, which may be as extreme as complete failure of the device or simply a level of parametric degradation, after which the device becomes marginally useful for it's intended application.

As reviewed in chapter 1, AlGaN/GaN HEMTs are suitable for a wide array of RF and power management applications. Each of these end use applications have different operational requirements that lead to a variety of use conditions and, as such, requires different studies to assess reliability and failure mechanisms under these various operational conditions.

Figure 3.1 illustrates the various bias points mapped to the FET I-V plane from

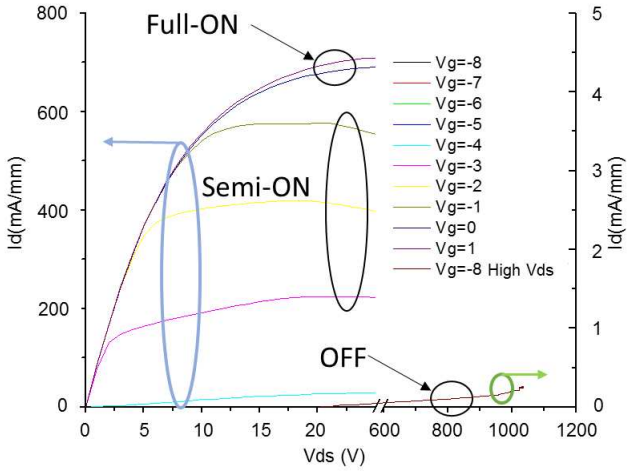

Figure 3.1: Full I-V plot measured on a device fabricated in the studied commercial process that illustrates three possible bias regimes. Full-ON describes the device in open channel conditions, typically with zero or positive bias on the gate. Semi-ON is when the device is not off but the channel is not completely opened, gate bias is between the threshold voltage and zero bias. OFF describes the state when the channel is biased to a state where the channel is depleted under the gate and in a high impedance state.

an example device. Full-ON describes a device biased into open channel conditions, this occurs in AlGaN/GaN depletion mode HEMTs when $V_{GS} \geq 0V$ as is typical of a FET designed into a switching application biased into the ON-State. In the full-ON state the device sources a large output current under a low electric field. The semi-ON condition occurs when the device is biased above threshold but below open channel conditions $V_{TH} < V_{GS} < 0V$ and is typical of AlGaN/GaN HEMTs for power amplifier (PA) applications. In the semi-ON state the device outputs a small to moderate amount of current while under a moderate applied electric field. The last state shown in Figure 3.1 is the OFF-state when the device is biased below the threshold voltage $V_{GS} < V_{TH}$. AlGaN/GaN HEMTs are operated in the OFF-state during RF and power management switching applications and some PA applications (switch-mode). In the OFF-state the device sources a very low amount of current but is under the effects a large applied electric field.

Each of these bias states provide unique challenges and require an array of reliability studies to fully understand degradation signatures and root cause failure mechanisms. This is because each condition exerts a varying combination of stresses on the device. In the ON-state the large amount of current sourced by the device may induce failures in the form of electro migration phenomena in the metals [68]. Forward biasing of the Schottky gate diode may lead to high current through the gate diode and is another potential reliability concern. This could occur for devices biasing into open channel conditions with positive bias on the gate diode ($V_{GS} > 0V$) or on a device operated in the semi-ON state during high RF drive when entering gain compression. Very few authors have reported results of such a reliability test. One such work from Coffie et al. [69] suggests that as long as the gate is not forward biased into an overdrive condition (i.e. electro migration of the gate metal) then no damage is done to the device. Other reviews on GaN reliability have stated that forward bias of the gate diode below overdrive conditions does not lead to device degradation [70], [71], [72]. Lack of interest in a comprehensive study of forward biased conditions may be due to the fact that proper design and biasing of AlGaN/GaN devices avoid gate overdrive conditions under normal operation.

When operated in the semi-ON state the device is conducting an electrical current so that charge is present in the channel while simultaneously biased such that a significant electric field is present across the device active area. This applied electric field acts to accelerate the carriers in the channel that are referred to as "hot electrons". The hot electrons, due to their high energies, may be accelerated out of the device channel and into the adjacent lattice generating defects and trap states that can exacerbate carrier trapping phenomena [70]. The presence of both current and electric field results in high power dissipation which leads to increased junction temperature of the device. High junction temperature is documented as being an accelerator of device lifetimes and therefore has an adverse effect on device reliability

[73].

The OFF-state condition places the device in a state with very low current but extremely high electric fields in the device channel. If the electric field were to be balanced across the device channel from the drain contact to the source it may not present such a reliability concern. However, it has been shown in literature [77] that the electric field concentrates at the edge of the gate contact under typical bias conditions. This leads to reliability concerns at the gate edge footprint as these extreme electric field peaks may lead to defects at the device surface or in the AlGaN barrier layer as will be discussed in detail later in the chapter. The effects of the electric field peak may be mitigated through the use of "field plates" as was described by Karmalker et al. [77]. Field plates act to smooth the electric field across the device channel and as a result reduce the peak field at the gate contact edge, but this is not without penalty. Field plates are typically connected to the source and gate contact and act to increase parasitic capacitance in the device. These increased capacitances lead to increased switching times and reduced bandwidth for broadband amplifiers.

3.2 Motivations of AlGaN/GaN HEMT Reliability Studies

AlGaN/GaN HEMT reliability analysis aims to quantify the lifetime of any population. The field of reliability analysis is applied to a wide range of applications from mechanical systems to chemical processes. Reliability of semiconductors is particularly challenging since no individual failure mechanism can be used to describe device degradation. In fact the failure mechanism is largely dependent on the various stresses that are applied to the device and these can vary under the multitude of conditions ranging from DC, RF, electric field, environmental, and mechanical stresses. Within these applications, the state in which the device is operated may lead to different failure mechanisms.

Reliability analysis is a complex field but generally the failure rate of populations follows the same general trend that is often times referred to as the "bathtub" curve

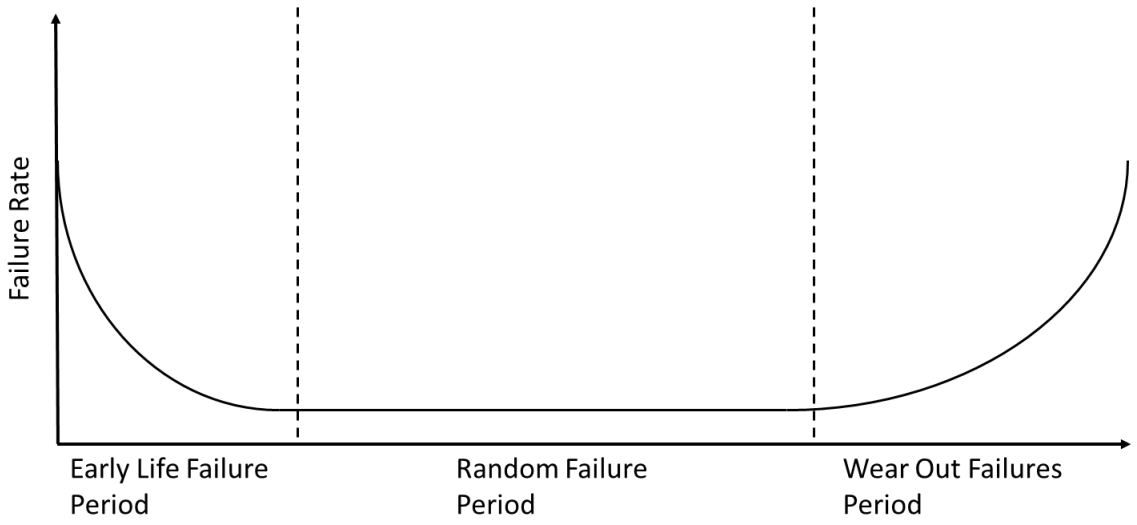

Figure 3.2: General failure rate of a typical population studied for reliability. Called the "bathtub" curve due to the shape. Early in time, population failure rate is high due to infant mortality. Failure rate decreases during the useful life where only random failures occur. Failure rates increase again towards the end of useful life due to wear out mechanisms.

[73], as shown in Figure 3.2. The curve describes the observation that failure rates for a population start out high due to infant mortality. The failure rate drops as the population enters its useful life before eventually failure rates begin to increase again as wear out starts to occur. For semiconductors the failures during the initial part of the bathtub curve are normally due to macroscopic processing defects and is quantified by the process defectivity. If the root causes of defectivity cannot be sufficiently identified and removed from the process then it becomes necessary to screen each product with a thermal and electrical "burn-in" test so that early failures may be screened out before the product is delivered to the end customer.

Reliability studies typically focus on the wear out phase of the bathtub curve. Here failure mechanisms are difficult to measure since it occurs at time intervals much longer than the useful life of the product; to measure wear out in a reasonable amount of time it becomes necessary perform accelerated lifetime tests. Accelerated lifetime tests are only valid when the factors that drive lifetime acceleration are known

for a given population. Temperature is a popular factor for a range of lifetime studies as it has been shown to correlate with wear out. For semiconductors, accelerated lifetime tests utilize elevated temperatures as a means of generating valid population lifetime data in a matter of hours.

The most prevalent accelerated lifetime studies make use of the three temperature tests that are reported in literature [73], [74], [75], [76]. In three temperature lifetime test, the population of parts are divided into three groups, each with a unique stress temperature. Each group is tested under the same bias conditions which may be either the semi-ON or OFF-state. After the testing is completed, typically around 1000 hours of stress time, the cumulative failure rate of each group is recorded and from this a mean time to failure (MTTF) is determined for each of the three temperatures. Failure criteria for AlGaN/GaN HEMT is usually based on the degradation of saturated drain current (I_{dss}) from the initial value recorded prior to stress.

The MTTF data obtained from the three temperature study may then be plotted using the Arrhenius law. The basic Arrhenius equation is given by

$$R(T) = Ae^{\left(\frac{E_A}{kT}\right)} \tag{3.1}$$

Where $R(T)$ is a reaction rate as a function of temperature, T is the temperature, A is a constant, E_A is the activation energy, and k is Boltzmann's constant. The failure rate from a life test may be expressed by the following equation.

$$\lambda \propto \frac{1}{TDH \cdot AF'} \tag{3.2}$$

Where TDH is the total device hours which may be determined by the length of reliability test times the number of devices in the total population. AF is the acceleration factor which may be determined from the following equation.

$$AF = exp\left[\frac{E_A}{k}\left(\frac{1}{T_{op}} - \frac{1}{T_{stress}}\right)\right] \tag{3.3}$$

In this equation T_{op} is the rated operating temperature and T_{stress} is the stress temperature used to accelerate the lifetime of the population. The Arrhenius model activation energy parameter is critical for linking the lifetime of the population under study to the stress. In the case of temperature, when plotted on a semi-log scale, the data will typically produce a linear relationship. From this plot it is possible to extract an activation energy [73].

The Arrhenius equation has limitations when it comes to predicting lifetimes as the activation energy term is restricted to one failure mechanism. If the process under analysis contains multiple failure mechanisms then more advanced techniques must be applied. An example of MTTF data on an Arrhenius plot is shown in Figure 3.3. In the figure, MTTF curves are shown for two commercially available GaN processes from the same vendor. Also included in these plots are the confidence bounds on the extapolated data to "at use" conditions. These confidence bounds represent a 90% confidence interval.

The root cause of failures observed during three temperature studies of AlGaN/GaN HEMT technologies is still under debate. One suggestion in literature is that the AlGaN surface at and just under the Schottky gate is altered during stress so that the threshold voltage of the device is shifted positive, meaning a reduced amount of charge in the channel correlating with the observed drop in I_{dss}. This alteration of the AlGaN surface was shown to saturate over time and electrically to increase the Schottky barrier height [78]. Another report correlated the drop in I_{dss} and subsequent reduction in output power to the formation of crystallographic defects in the AlGaN layer [79]. One final reported mechanism relates to source metal intermixing at the ohmic contact [82].

A summary of three temperature reliability as reported by United States domestic

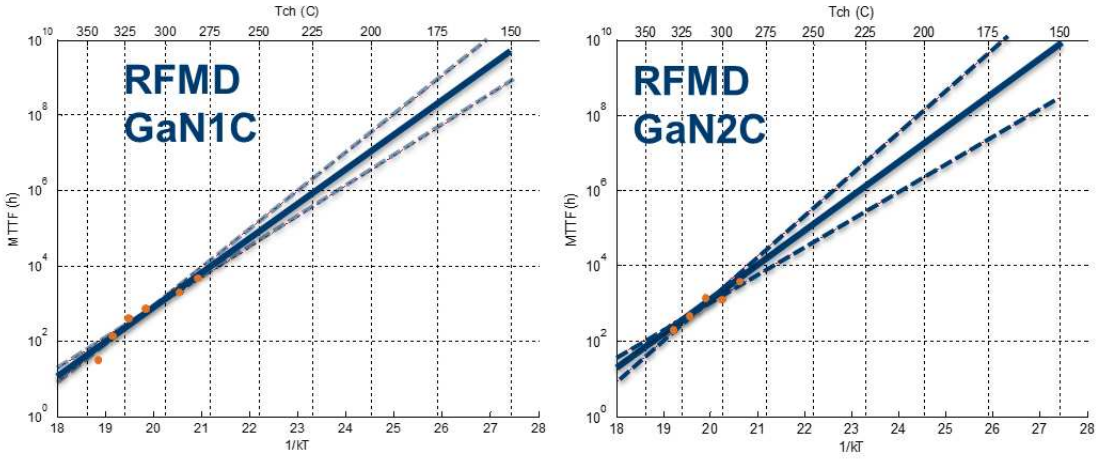

Figure 3.3: Example of typical Arrhenius plot for both RFMD qualified AlGaN/GaN HEMT processes with upper and lower confidence bounds included. (Left) Arrhenius plot of RFMD GaN1C process (Right) Arrhenius plot of RFMD GaN2C process. Reliability of both processes was evaluated in the semi-ON state with a drain bias of $48V$.

GaN foundries is shown in table 3.1. From this table it is possible to gauge typical operating conditions in which state of the art AlGaN/GaN HEMTs are expected to reliably operate. Typical reliability requirements include operating with a junction temperature of $200°C$ for over a million hours which translates to 100 years. Drain biases range from 28 V to 48 V and activation energies for the failure mechanism are around 2 eV.

Table 3.1: Reliability summary of domestic GaN foundries. This is based on published results from three temperature reliability studies. Note the following, TriQuint does not have a published activation energy from their reliability studies. The GCS GaN process is based on a technology transfer agreement with Nitronex.

Foundry	$Ea(eV)$	MTTF (hours)	T_j ($°C$)	V_{DS} (V)	Ref
RFMD	2.4	$>10^7$	200	65	[80]
TriQuint	-	$>10^7$	200	40	[81]
Cree	1.8	$>10^7$	225	28	[82]
GCS	2.2	10^6	200	28	[83], [84]

It is worth noting that all domestic GaN technology MTTFs shown in Table 3.1 are based on the three temperature testing and Arrhenius analysis with the failure criteria set to an arbitrary percent degradation of I_{dss}. Meaning that all reliability data

published by GaN suppliers is based on temperature acceleration. No other acceleration factors have been proposed by commercial GaN suppliers to date. Therefore, the reliability figures quoted could be optimistic if an alternate acceleration factor was to be determined.

It is important to note that gate leakage current is not included as failure criteria in three temperature studies. This is despite the fact that a change in gate leakage has been widely observed in published reports on these studies after stress [72], [73], [74], [85]. While a change in gate current may not drastically affect the end device performance, a large increase in leakage current may impact final device reliability as mentioned in [73]. If gate leakage current was considered, the final MTTF numbers that are reported in Table 3.1 may be impacted. Because such a possibility exists, there have been publications that aim to explain the root causes behind the observed increase in leakage current associated with a degradation of the Schottky gate diode [70], [71] [72], and [73].

The following section will provide a detailed review of AlGaN/GaN gate Schottky diode degradation studies that have been reported in literature.

3.3 Reliability Studies of OFF-state Stressed AlGaN/GaN HEMTs

This chapter began by detailing the various operation states of AlGaN/GaN HEMT and the stresses that are associated with each of those conditions. There exists in literature a multitude of studies that aim to uncover the degradation mechanisms and root causes associated with each of these conditions. This section will detail each of these reported mechanisms.

3.3.1 The Inverse Piezoelectric Effect Degradation Mechanism

To determine gate degradation, various OFF-state studies have been published with a goal of inducing failure by way of applying high electric fields on the device and setting the failure criteria as increased gate leakage current. The analysis of this increase in gate leakage current aims to understand root cause effects and mechanisms.

These studies began by stressing AlGaN/GaN HEMTs using a voltage step-stress method [86], [87], [88], [89], and [90]. This step-stress method may be applied to the device in two different ways. The first involves grounding the source and drain contacts and then applying increasingly high negative bias, in steps, to the gate diode with respect to the source and drain. This is sometimes referred to as a two terminal (2T) stress, which equally stresses both sides of the gate diode (drain and source side). The second method involves biasing the devices into the OFF-state ($V_{GS} < V_{TH}$), with the source contact grounded, and applying increasingly positive bias, in steps, to the drain terminal. This may sometimes be referred to as a three terminal stress (3T), since all three contacts are at different potentials. In this stress method only the drain side of the gate diode is stressed.

In these studies it was shown that by tracking the gate leakage current during the step-stress experiment it was possible to extract a "critical voltage" (V_{crit}) that, once exceeded, lead to an instantaneous increase in gate leakage current. Upon further analysis it was found in these studies that several other parameters suddenly degraded once the V_{crit} was exceeded, for example, max drain current (I_{dmax}) and access resistance of both drain and source (R_D and R_S).

The proposed mechanism, by J. A. del Alamo and J. Joh, leading to the observed degradation in these step-stress studies, was attributed to the "inverse piezoelectric effect" (IPE) [87], [88]. A schematic of the proposed gate leakage path that is generated by IPE is shown in Figure 3.4.

As was detailed in chapter 2, during the growth of the AlGaN/GaN heterostructure, the AlGaN layer has a tensile strain due to the lattice mismatch with the underlying GaN layer. The strain present in the AlGaN layer was shown to have a piezoelectric polarization component. This implies that the AlGaN layer, as grown, has a stored elastic energy. The IPE model proposed by Joh [89] states that stored elastic energy in the AlGaN barrier layer may be increased with the application of

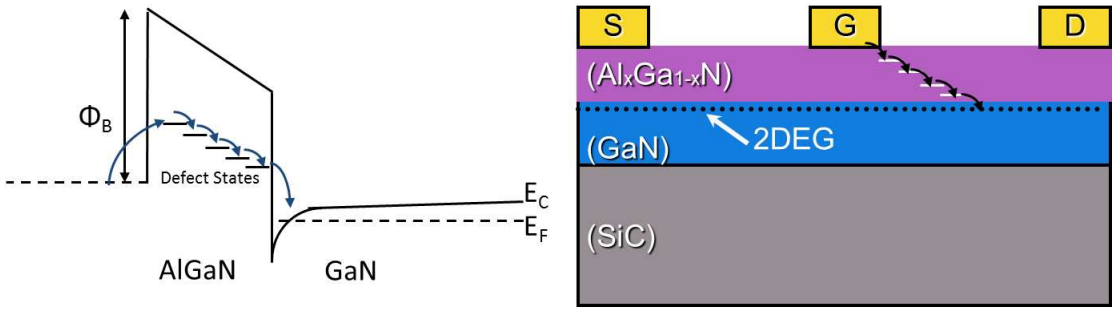

Figure 3.4: Schematic of the proposed gate leakage path induced by degradation from the inverse piezoelectric effect as proposed by Alamo et. al. [88]. The macroscopic defect in the AlGaN barrier (crack or pit) generates trap states which may be used by electrons in the 2DEG and gate Schottky contact to hop across the AlGaN barrier layer.

electric field. During a step-stress experiment, the increasing bias applied to the device increases the tensile strain present in the device. Eventually, a critical elastic energy is surpassed that corresponds to the maximum amount of stored elastic energy in the AlGaN barrier. When this occurs, the excess strain in the AlGaN crystal will be released via relaxation that results in the formation of a crystallographic defect. This defect has been shown to manifest as a crack or pit at the edge of the Schottky gate contact which corresponds to the peak of the electric field present in the channel.

Table 3.2: Material parameters used for calculation of stored elastic energy and tensile strain in the inverse piezoelectric effect model.

	C_{11} (GPa)	C_{12} (GPa)	C_{13} (GPa)	C_{33} (GPa)	C_{44} (GPa)	e_{13} (C/m^2)	e_{33} (C/m^2)	e_{15} (C/m^2)	E_γ (GPa)
GaN	350	110	103	405	105	-0.49	0.73	-0.30	408
AlN	350	110	108	373	105	-0.60	1.46	-0.48	397

The amount of tensile strain in the AlGaN layer and the applied strain due to the electric field may be determined by using the material parameters shown in Table 3.2. The full derivation can be found in the publication by Joh et. al. [89]. During the application of bias to a AlGaN/GaN HEMT, the electric field present in the device may be described as having an x, y, and z component. The x and y components are planar to the surface of the device while the z component is vertical and perpendicular

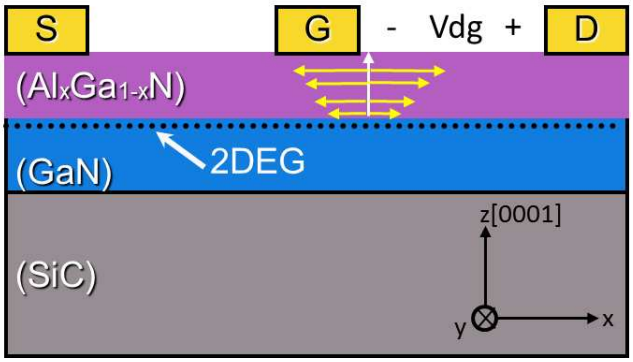

Figure 3.5: Schematic of the tensile strain induced by the applied electric field in the device which is at its peak at the gate contact edge [89]. The derivation of the IPE model in this publications shows that only the vertical component of the applied electric field acts to increase the elastic energy in the AlGaN layer. This applies a lateral stress on the crystal so that once the critical elastic energy is exceeded leads the crystal to relax, resulting in the formation of a surface crack or pit.

to the surface. These components of the electric field may be referred to as E_1, E_2, and E_3, representing the x, y, and z dimensions respectively.

In the derivation presented in [89], it is shown that E_2 (y-dimension), which represents the component of applied electric field parallel to the gate finger, is negligible due to the high aspect ratio of a gate finger to the channel dimensions in the normal construction of a AlGaN/GaN HEMT. Furthermore, E_1 is approximately zero in this derivation since the stress at the surface of the AlGaN is considered to be zero. Therefore, the change in elastic energy in the AlGaN layer is only due to the vertical component of the electric field, shown schematically in Figure 3.5.

The elastic energy density in the AlGaN barrier layer may be calculated with the following equation.

$$W = \left(\frac{C_{33}}{C_{11}C_{33} - 2C_{12}^2 + C_{12}C_{33}} \right) T_1^2 \tag{3.4}$$

Where T_1 is the vertical component of the stress tensor given by the following.

$$T_1 = \left(C_{11} + C_{12} - 2\frac{C_{13}^2}{C_{33}} \right) S_{10} + \left(\frac{C_{13}e_{33}}{C_{33}} - e_{31} \right) E_3 \tag{3.5}$$

In this equation S_{10} is the planar strain at the AlGaN/GaN interface due to the lattice mismatch, which is calculated using the equation.

$$S_{10} = \frac{a_{GaN} - a_{AlGaN}}{a_{AlGaN}} \tag{3.6}$$

Where the lattice constants of both AlGaN and GaN were shown in Table 2.2. The critical elastic energy in the AlGaN barrier is determined by the equation.

$$W_{crit} = E_{\gamma} h_{crit} S_{10}^2 \tag{3.7}$$

Where E_{γ} and h_{crit} are the Young's modulus and critical thickness of the AlGaN barrier layer. Once the stored elastic energy and critical elastic energy of the AlGaN barrier layer are calculated, they may then be compared and from this it is possible to extract the critical voltage for a specific AlGaN layer

The total mechanical stress applied to the AlGaN/GaN heterostructure can be separated into three components. The first is residual stress due to the lattice mismatches between AlGaN and GaN as well as between GaN and non-native substrate. Second is the IPE stress, due to applied electric field. Third, are thermal stresses present when operated in the semi-ON state. The contributions of each of these stresses to the total stress has been largely unknown since these stresses are traditionally difficult to measure.

One method of measuring mechanical stress in the heterostruture is via the use of micro Raman spectroscopy as reported by Choi et al. [91]. The advantage of micro Raman is high spatial resolution provided by the laser source ($\sim 1\mu m$). This provides for accurate measurements at the gate contact edge that corresponds to the peak electric field. Choi et al. [91] studied GaN-on-Si and GaN-on-SiC devices though subtle differences existed in the as processed HEMT structures. For example the GaN-on-Si device had a SCFP that would smooth the channel electric field profile

and the GaN-on-SiC did not have a SCFP. Both sets of devices were biased in the OFF-State and the GaN-on-SiC device in the semi-ON state.

Choi et. al. found that residual stresses played the largest role in the overall mechanical stress present in the device heterostructure. Specifically, the residual stress present in the GaN layer due to the choice of substrate. The conclusion was made that devices were less prone to degradation in the presence of high voltage conditions if the GaN residual stress was more compressive as this translated to the AlGaN barrier layer making it less tensile strained.

Physical analysis of devices from step-stress studies that show the sudden increase in gate leakage, have revealed the presence of crystal defects postulated to occur due to IPE. An example of a crack that extended across the AlGaN barrier layer from a device stressed in a step-stress study is shown by Jimenez et. al [92]. In this work it is not clear how the authors knew exactly what location along the gate periphery to cross section the device to find evidence of the crack. This may imply that the crack was uniformly distributed along the gate periphery.

In another study performed by Makaram et. al. [93] several AlGaN/GaN HEMTs were stressed to varying levels of bias between the gate and drain. After the stress was completed a chemical etch of the gate metal was performed and the surface morphology was mapped with atomic force microscopy (AFM). The progression of crack formation was shown as the unstressed device maintained a smooth surface at the gate edge. However, with increasing stress from 15 V to 57 V a progressively wider and deeper crack formed on the drain side of the gate contact. This trench extends the entire parallel the entire length of the gate finger, corresponding to the region of high electric field. At the extreme bias condition of $V_{DG} = 57V$ an AFM depth profile revealed the crack depth to be as high as $2nm$ on the drain side of the gate. Furthermore it appears as if the pits on the surface with increasing amounts of stress begin to merge together to form a trench in the AlGaN that is parallel with

gate finger.

After the initial discovery of cracking and pitting, additional root cause mechanisms were proposed to explain the genesis of the cracking and pitting. Energy dispersive X-ray (EDX) analysis of regions with and without crystal defects was reported by Park et. al [94] to determine if contaminants were present in the defect regions. It was discovered that oxygen was present at sites where the defects occurred. Further studies have been conducted that conclude that oxygen at the surface of the AlGaN/GaN HEMT may chemically etch the AlGaN barrier, forming Al_2O_3 and Ga_2O_3, during the course of an OFF-state stress test leaving behind pits on the surface via a chemical etching process [95].

Additional experiments on epitaxial growth and processing cleans reported success in mitigating the formation of crystal defects. It was reported that thickening the GaN cap that is typically grown as a final epitaxial layer on top of the AlGaN surface was able to increase the amount of stress time needed to generate a defect. A reduction of the Al% in the AlGaN layer also was able reduce the amount of degradation observed with stress, by lowering the amount of residual strain in the AlGaN layer. [96]. However, both of these approaches adversely affect the device performance as thicker GaN cap can alter Schottky properties of the gate diode and a reduction in Al% reduces the amount of charge in the 2DEG and therefore reduces device power density.

Finally, it was proposed that the pits and cracks generated during OFF-state stress occurred because the device as processed already contained microscopic pits on the surface as a consequence of device fabrication. These microscopic pits which were said to contain residual oxygen from processing which expanded in the presence of an applied electric field to form larger pits and eventually propagate into the AlGaN layer forming a crack. An experiment with surface cleaning was published by [96] that compared the effects of two surface treatments during AlGaN/GaN HEMT

processing. Individually, the process treatments showed a reliability improvement and when utilized together eliminated pitting entirely on the surface. Another article referencing this surface treatment was published showing that the treatment resulted in much lower concentration of oxygen on the surface [97]. The details of the surface treatment was never published, but consistently it has been demonstrated that reduction in surface oxide leads to improved reliability and lower degradation in stressed devices.

3.3.2 Time Dependent OFF-state Degradation

The common theme in the step-stress studies, especially those that assign the root cause to the inverse piezoelectric effect is that damage sustained by the device is instantaneous. The theory assumes a critical voltage exists for a given device so that once exceeded, irreversible damage occurs. This poses the question of what happens to a device continuously stressed below the critical voltage? Initially published by Marcon et al. [98], it was shown that stressing the device below the critical voltage does lead to device degradation. It was shown in this work that with step stress a critical voltage could be found at $70V$. However, with constant stress study on the same devices below $70V$ revealed device degradation, via increased gate leakage, occurs below the critical voltage.

A later publication by Marcon et. al. [99] shows that the critical voltage may be manipulated by the test details. Since the inverse piezoelectric theory postulates damage only occurs once the critical voltage is exceeded then the dwell time at each voltage during a step-stress study was considered arbitrary. However, the authors in [99] show that the exact value of the critical voltage does depend on the dwell time due to accumulated damage that occurs in the device with stress. Therefore devices testing in step-stress experiments with longer dwell times have lower critical voltages. The authors go on to state that step-stress studies still hold value as a tool for quick assessment of a particular technology.

Time dependent dielectric breakdown (TDDB) has been proposed as the degradation mechanism observed in stress below the critical voltage [98]. This failure mechanism has been observed in silicon metal-oxide-semiconductor-field-effect-transistors (MOSFET) as a documented degradation of the gate dielectrics in these devices [101]. In AlGaN/GaN HEMTs it was proposed that the AlGaN barrier layer is analogous to the gate dielectric in a MOSFET device. The theory behind TDDB states that under high electric fields percolation paths form in the gate dielectric. These percolation paths, provide a means for electrons to conduct from the gate contact to the underlying 2DEG. The percolation path density is also said to be a function of stress time, so observed increases in gate leakage is due to the formation of additional paths through the dielectric.

It has been reported in TDDB literature that the percolation model follows Weibull statistics [101]. Marcon et al. was able to show that stress in the OFF-state at three different bias levels also follow a similar Weibull distribution. This provides compelling evidence that the failure mechanism is similar to TDDB. Furthermore, in this same publication the authors did a three temperature study in the OFF-state keeping the bias constant ($V_{GS} = -55V$), the result revealed a weak dependence on temperature. This suggests that when stressed in the OFF-state, applied electric field is the dominant acceleration factor.

It is worth mentioning that electroluminescence has been used extensively in OFF-state stress literature as a means of identifying spatially on the AlGaN/GaN HEMT, a potential failure site location. This method has been utilized in both step-stress and constant stress studies. There are publications aimed to show that correlation exists between EL emission sites and gate leakage locations along the gate, by monitoring EL emission real time during OFF-state stress [100], [102]. Both of these works show that EL intensity increases when step increases in gate leakage occur and that new localized emission sites correlate to the observed increases.

When performing physical analysis, such as TEM, at the observed EL emission sites, the authors report various observations. It has been demonstrated that pits in the AlGaN surface, up to $4nm$ deep were located at these EL sites, which may be linked to some of the root cause findings from the IPE work. Others have reported that no signs of macroscopic crystal deformation may be observed [92], [99], and [115]. Based on these results multiple conclusions may be drawn. The first is that TEM is being performed at the correct location as indicated by EL but the defect due to TDDB is not visually detectable. The second is that, due to the highly localized nature of TEM, the cut is not not being made at the precise location of the increased gate leakage. This could be due to error in translating the EL spot to the TEM cut site or the EL emission is offset from the actual location of the leakage. AlGaN and GaN are transparent materials so it is possible that the EL when observed has shifted from the origin site within the bulk structure. Both of these possibilities have been invoked in literature as a hedge against why a macro defect has not been identified. A third possibility exists in that the EL emission may not actually correspond to the leakage sites at all. While strong arguments have been made in published articles that the insitu monitoring of EL correlates to increases in gate leakage with stress [100], [102], and [104]. There has been no conclusive physical analysis published that proves this to be true.

3.4 Summary

In this chapter the typical operating conditions of AlGaN/GaN HEMTs which includes full-ON, semi-ON, and OFF-state were explained along with the associated stresses exerted on the device. The primary stresses include current, electric field, and temperature. The semi-ON and OFF-state conditions are the operating conditions of the device that are considered the most stressful and as such are the focus of reliability research.

Manufacturers of AlGaN/GaN HEMTs publish reliability results based on three

temperature stress studies at target operating bias points. This data is then plotted according to Arrhenius Law and used to extract MTTF at rated junction temperatures and the activation energy of the thermally accelerated failure mechanism. To date, thermal stress is considered the only lifetime accelerating factor among GaN suppliers. This leads to typical estimated lifetimes greater than 10^6 hours. Reliability publications have suggested that these calculations are optimistic because they do not consider other potential lifetime accelerators such as applied electric field.

In recent years there has been a surge in AlGaN/GaN HEMT reliability studies of devices operating in the OFF-state, a condition that subjects the device to extreme electric field stress. Initially theories stated that GaN devices were limited by the inverse piezoelectric effect when operated in the OFF-state. This theory states there exists a critical voltage that once exceeded leads to irreversible damage to the device in the form of a macroscopic crack or pit in the AlGaN barrier layer. As a consequence it is assumed that if the device operating conditions are below the critical voltage of a given device then degradation will not occur.

Further studies in the OFF-state proved the IPE theory to be flawed as device degradation was shown to occur below the critical voltage. In fact, the critical voltage may be manipulated by the dwell time during a step-stress study. It has been proposed that degradation below the critical voltage is similar to the breakdown of MOSFET gate oxides and capacitor dielectric breakdown, attributed to time dependent dielectric breakdown. Initial reports have shown that the failure data follows the statistical models used in TDDB reliability studies.

CHAPTER 4: RELIABILITY OF COMMERCIAL ALGAN/GAN HEMTS

The objective of this chapter is to introduce the AlGaN/GaN HEMT devices used in this study and the applied stress experiments. The chapter will begin with a detailed description of the devices and their performance as fabricated in this process. Next will be details and observations made during, two stress methods. These methods were the step-stress and constant stress experiments, similar to those detailed in chapter 3. The goal of these experiments were to understand how AlGaN/HEMT devices from a robust commercial process would degrade when subjected to these stress conditions. Then from these observations, an initial assessment will be made on the degradation and failure modes of modern commercial AlGaN/GaN HEMTs.

4.1 Step-Stress Study of Commercial AlGaN/GaN HEMTs

4.1.1 Device Details

The devices used in this study were AlGaN/GaN HEMTs on SiC substrates grown by metal-organic chemical vapor deposition (MOCVD). The devices were fabricated using a process that was qualified for commercial production [105]. However, the devices used an experimental layout that deviated from the qualified layout in three key areas. First, the gate-to-drain and gate-to-source contact spacing was shortened in order to reduce the breakdown voltage. This made it possible to stress the device with a semiconductor parametric analyzer (SPA), capable of accurate measurement of leakage current during stress. Second, the gate was centered in the channel so that the gate-to-drain and gate-to-source spacing was identical. This would effectively make the gate-drain diode and gate-to-source diode identical and allow for a range of analysis options and methods to be applied to understand the nature of device

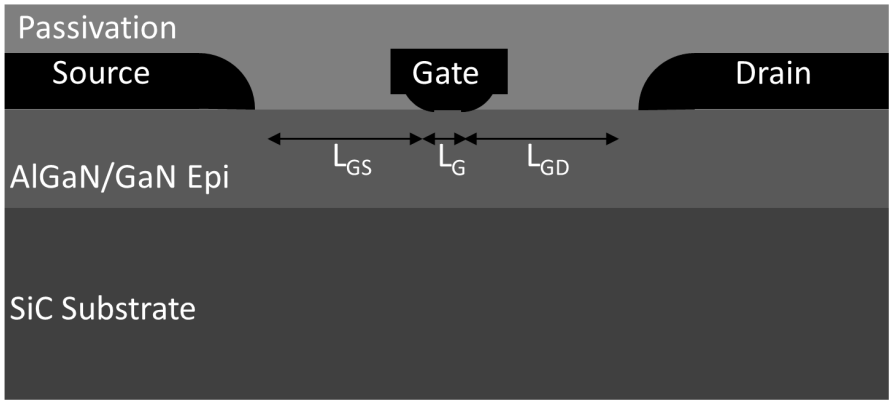

Figure 4.1: AlGaN/GaN HEMT device cross section schematic with key dimensions labeled. Devices in this study were fabricated using a commercially available and qualified AlGaN/GaN fabrication process [105]. The device used in this study used an experimental layout that deviated from the qualified layout from this process in two key areas. First, the gate-to-drain and gate-to-source contact spacing was reduced to allow the device to be stressed by a semiconductor parametric analyzer. Second, the gate was centered in the channel so that the gate-to-drain and gate-to-source spacing was identical. This would effectively make the gate-drain diode and gate-to-source diode the same and allow for analysis options and methods to be applied to understand the nature of device degradation. Third, the source-connected field plate was removed in this layout so that optical analysis may done close to the edge of the gate contact.

degradation. Third, the source-connected field plate was removed in this layout so that optical analysis may done close to the edge of the gate contact.

The devices had two different sets of gate peripheries. Initially, the tested devices had ten gate fingers, each with a unit finger width (UFW) of 100 μm for a total gate periphery (W_g) of $1mm$. Later on the gate periphery was reduced to simplify failure analysis. The later devices had two gate fingers, each with a UFW of 50 μm and a (W_g) of 100 μm. The gate was a typical T-shape with the footprint in contact with the semiconductor, defining the gate length (L_g) as 0.5 μm. A gate field plate was present as a consequence of processing the device T-gate. The gate-to-drain and gate-to-source distance was the only difference between the two variants. Device "A" had the minimal channel spacing allowed by the process ($L_{gs} = L_{gd} = 1.3\mu m$) and device "B" increased these distances to 2 μm. Therefore, the total gap between the

source and drain contact (L_{ds}) for device A was 3.1 μm and device B was 4.5μm. A representation of the channel cross section, with key dimensions labeled, is shown in Figure 4.1. The breakdown voltage of device A was 110 V and device B was 200 V. The next two sections will detail the initial stress studies conducted on these devices, similar to those described in literature as detailed in chapter 3. The goal to determine if similar failure modes exist in this process.

4.1.2 Step-Stress Experimental Details

The step-stress test in this study utilized four different test conditions aimed to uncover the existence of a critical voltage on the devices in this study. These test conditions covered two factors which consisted of bias application and temperature. The chosen bias conditions were similar to the methods shown in [87]. These consisted of both the two terminal (2T) and three terminal (3T) OFF-state stress biasing methods. In the 2T method the source and drain contacts are grounded ($V_d = V_s = 0V$) and increasingly negative bias is applied to the gate. In this method both sides of the gate diode are equally stressed. With the 3T method the device is asymmetrically stressed as the source contact is grounded and the gate is biased so that the device is in the OFF-state ($V_{gs} = -8V$). Then the drain bias (V_{ds}) is stepped positive. In this case, only the drain side of the device is stressed. The second factor considered was temperature, the step-stress was carried out with the device at room temperature (approximately 25°C) and then heated to an ambient of 85°C.

Both device layouts (A and B) were used in the step-stress study, a total of 5 each. Both sets of devices had a total gate periphery of 1 mm. These samples were picked from 5 different wafers, processed in three wafer lots. They were mounted on a copper carrier with silver based epoxy. The FETs were contacted with Kelvin probes on a heated chuck, used to control the ambient temperature. The temperature at the base of the device was measured with a thermocouple on the carrier. The step stress was conducted using an Agilent 4155C SPA.

Ten steps were chosen and the device was held at each step for five minutes. Since the two device variants had different breakdown voltages then the exact bias conditions during the step stress study varied. The maximum voltage applied to the device was one step below the breakdown voltage of the device. In the 2T stress, the gate bias for device A was stepped from $-10\ V$ to $-100\ V$ in $10\ V$ steps while device B was stepped from $-20\ V$ to $-180\ V$ in $20\ V$ steps. Similarly, in the 3T step stress, the gate bias for both devices was set to $V_{gs} = -8V$ and the drain bias was stepped from $10\ V$ to $100\ V$ in $10\ V$ steps on device A and $20\ V$ to $180\ V$ in $20\ V$ steps for device B. A summary of the step stress is shown in table 4.1. All 5 devices from each variant were stressed with conditions 1 and 2. Two of the devices from each population were further stressed under the elevated temperature conditions of 3 and 4.

Table 4.1: Step-stress conditions used in this study for both devices A and B. The max voltage applied to each device was chosen as one step below the breakdown voltage.

Test	Base ($°C$)	$V_g(V)$	$V_d(V)$	Step Size (V)	Time (mins)
1	25	(A) -10 to -100 (B) -20 to -180	0	(A) $10V$ (B) $20V$	Step:5
2	25	-8	(A) -10 to -100 (B) -20 to -180	(A) $10V$ (B) $20V$	Step:5
3	85	(A) -10 to -100 (B) -20 to -180	0	(A) $10V$ (B) $20V$	Step:5
4	85	-8	(A) -10 to -100 (B) -20 to -180	(A) $10V$ (B) $20V$	Step:5

Using Joh et. al. [87] as a guide, these conditions were expected to be sufficient to uncover the critical voltage. In [87] the critical voltage was determined to be 26 V in the 2T stress and 38 V in the 3T stress for a device with $L_{gs} = L_{gd} = 2\mu m$. In that publication, the step size was 1 V with a dwell time at each step of one minute. Therefore, total stress time was 26 minutes in the 2T condition and 38 minutes in the 3T condition.

To quantify degradation due to stress, each device was characterized via a family of I-V curves (I_{ds} vs V_{ds}), transfer curves (I_{ds} vs V_{gs}) at $V_{ds} = 7V$, and a Kelvin measurement of R_{on}. This characterization was performed prior to stress and at the conclusion of each test condition. R_{on} was also measured between each step in voltage. In addition, the gate leakage current was monitored during stress for any sudden increases that may indicate a critical voltage had been surpassed. If a degradation in either R_{on} or I_{dss} >10% was observed then the device would be suspected of degradation via IPE and further failure analysis would be conducted.

4.1.3 Step-Stress Study Results

The parametric shifts as a result of the step-stress experiment are shown in Figures 4.2 and 4.3. Interestingly, the parametric shifts were opposite of what was expected for electrical degradation. Figure 4.2 shows the percent change in R_{on} versus the applied voltage after each step during the step-stress experiment. Both devices A and B across all conditions are plotted, with the general trend being an reduction in R_{on}. The vast majority of the change occurs after the first stress condition afterwards the device settles and stays consistent for the remainder of the stress conditions.

This is further illustrated in Figure 4.3 where the percent change in both R_{on} and I_{dss} before and after each stress condition is plotted. The observed trend was a reduction in R_{on} and an increase in I_{dss}. The degree at which these shifts occurred varied by stressed device from a few percentage points to a couple devices showing >10% parametric shift. However, this shift represented a parametric enhancement and therefore was not considered a failure.

A plot of the device transfer curves is shown in Figure 4.4, from device A1. As shown in Figure 4.3, this device had the largest parametric shift with stress. Therefore, this figure is the extreme case but illustrates the source of the parametric change. It is clear the threshold voltage of the device has shifted negative after the initial stress. This would indicate an enhancement of charge in the channel, as a higher

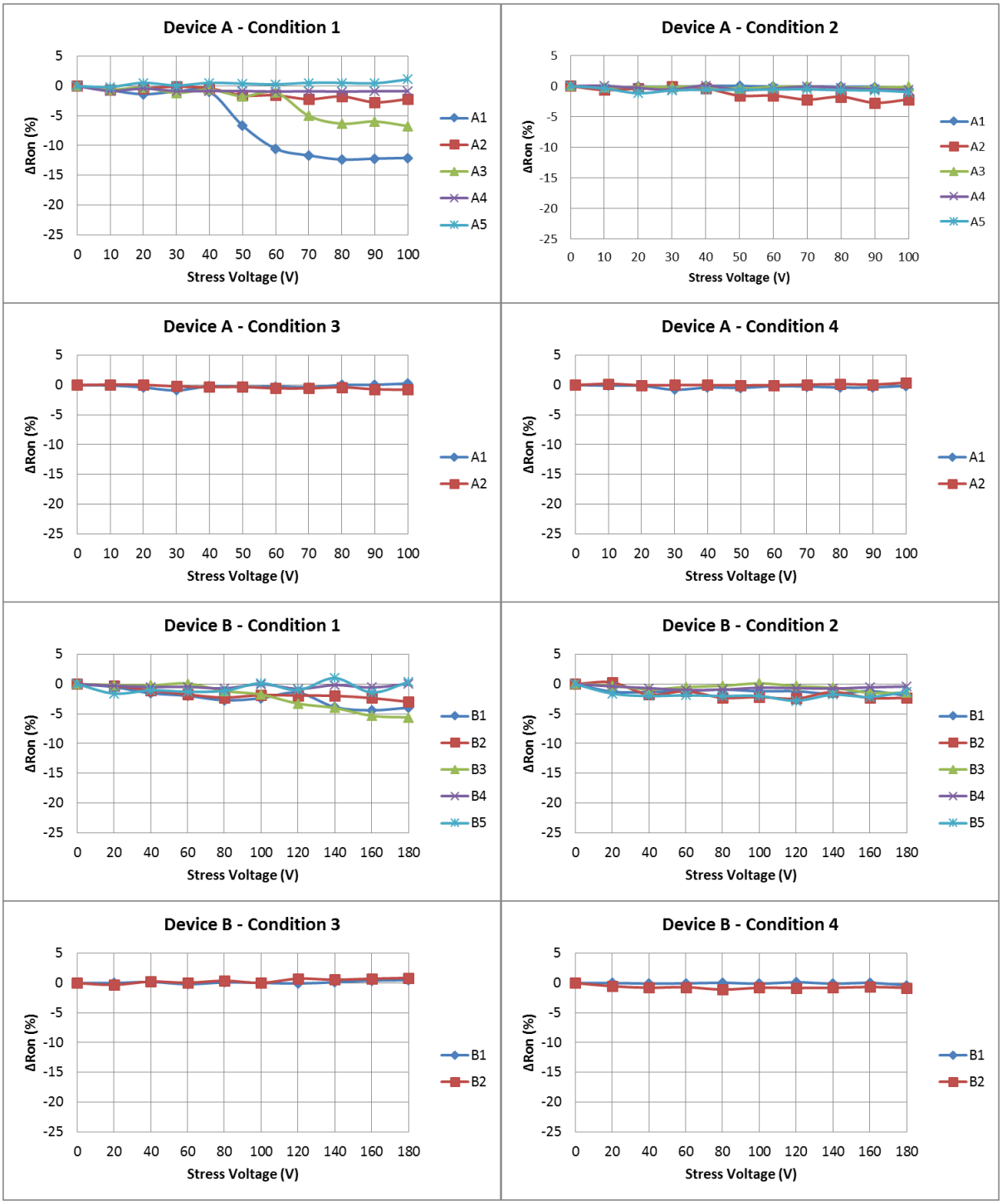

Figure 4.2: Parametric shift of R_{on} versus stress voltage, during the step-stress experiment. Any degradation, increase in R_{on}, that was >10% from the initial values was considered a failure due to IPE based on [87]. The general trend was a reduction in R_{on} indicating a parametric enhancement. This was primarily seen during the initial stress after which the device stabilized.

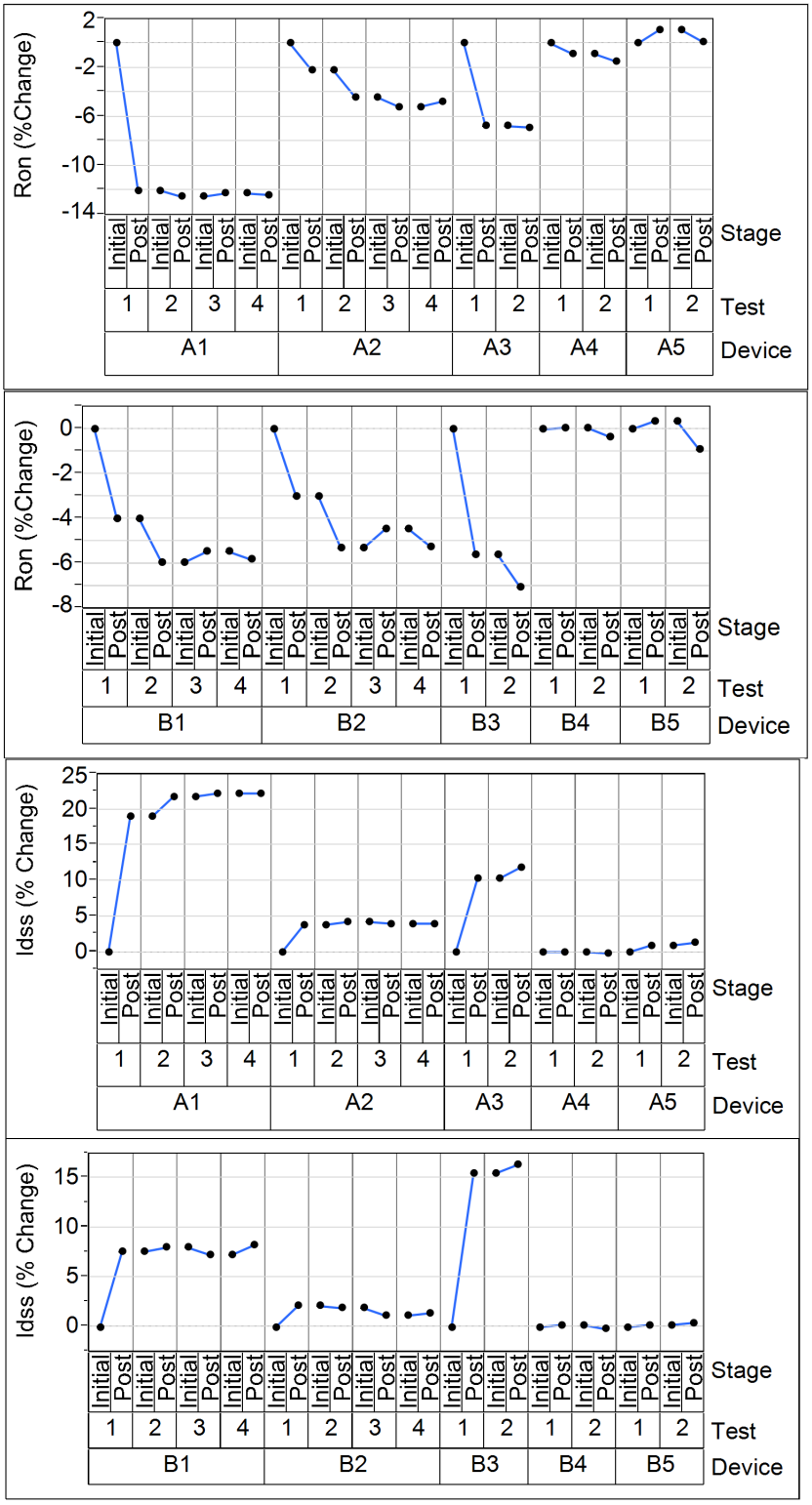

Figure 4.3: Parametric shifts of R_{on} and I_{dss} of each device in the step-stress study. The general trend did not indicate degradation had occurred. This suggests that a critical voltage related to IPE does not exists for devices in this process.

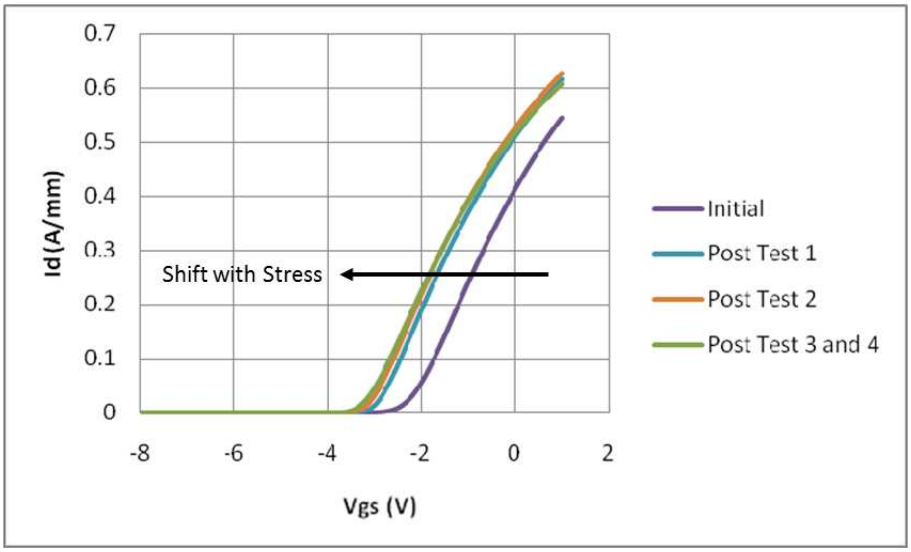

Figure 4.4: Negative shift in threshold voltage observed in the transfer curves (I_{ds} vs V_{gs}) at $V_{ds} = 7V$ for device A1. The curves are from the initial characterization and post test condition 1, 2, and 4. The transfer curve after condition 3 is not shown because the device base was $85°C$ when it was collected and therefore not a fair comparison. The post stress 4 curve was from a second characterization after the device was cooled to room temperature.

negative gate bias is required to deplete the channel. This would also explain the observed decrease in R_{on} and increase in I_{dss}.

The conclusion based on these results was that these devices do not have a critical voltage that was reported in literature. The stress conditions chosen exceeded the step-stress study parameters in previous reports of IPE degradation [87]. No significant parametric degradation was observed that would indicate IPE had occurred.

It is key to note that the general trend was the majority of the parametric shift occurred during the initial application of stress. With additional stress time and conditions, the changes were significantly reduced or not apparent at all. This suggests one of two possibilities, the first being that test condition 1 induces the change as a consequence of its specific stress on the device or simply that the change induced is caused by the application of OFF-state stress and is indifferent to the exact method.

The theory that the change was induced as a consequence of the stress in condition 1 is unlikely since the same bias conditions were applied in condition 3 (at elevated

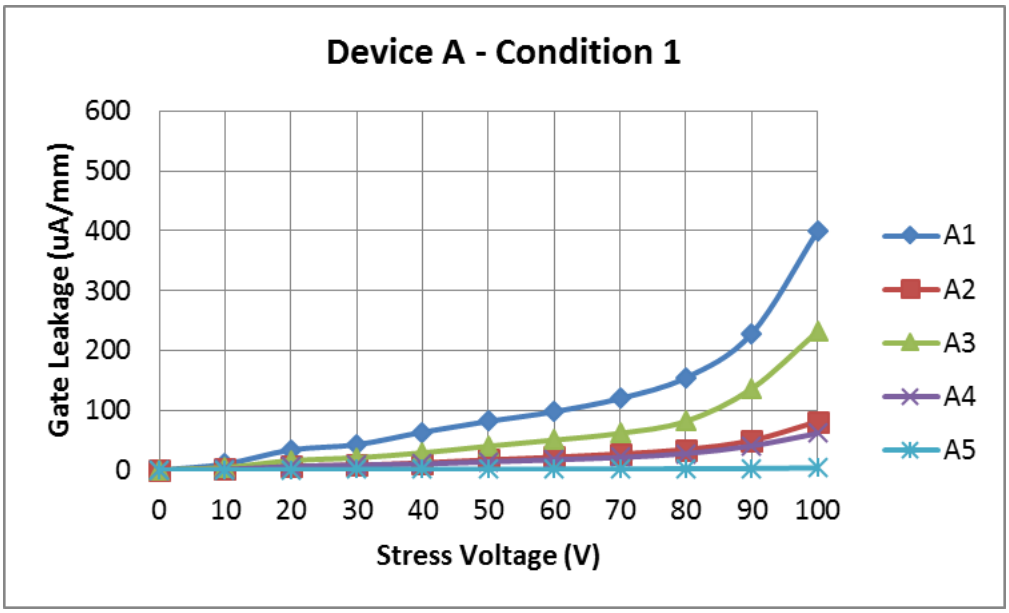

Figure 4.5: Gate leakage current measured during condition 1 of device A. Key take away is that the device with the highest leakage (A1 and A3) also had the most prominent parametric shift with stress. This suggests a link between the observed "burn-in" effect and gate diode leakage.

temperature) and little change was observed in that case. To prove the point, an additional device had the stress order reversed and showed the same large parametric shifts using condition 2 first followed by condition 1.

This suggests that regardless of the stress method, OFF-state stress results in a parametric shift that rapidly changes immediately after the application of stress. After this "burn-in" period the device settles into a steady-state behavior. Also, it is interesting to note that this "burn-in" effect was not thermally induced but instead driven by electric field stress. This effect appears to correlate with the gate leakage current as shown in Figure 4.5. The devices with the highest gate leakage (A1 and A3) also had the highest parametric shift during the step-stress. The initial change in device characteristics will be explored in more detail later in the chapter.

At the conclusion of the step-stress study one final experiment was conducted to understand if a short term constant voltage stress would induce device failure. Device A2 was held at the $V_{gs} = -8V$ $V_{ds} = 100V$, the extreme case of condition 2, for 6

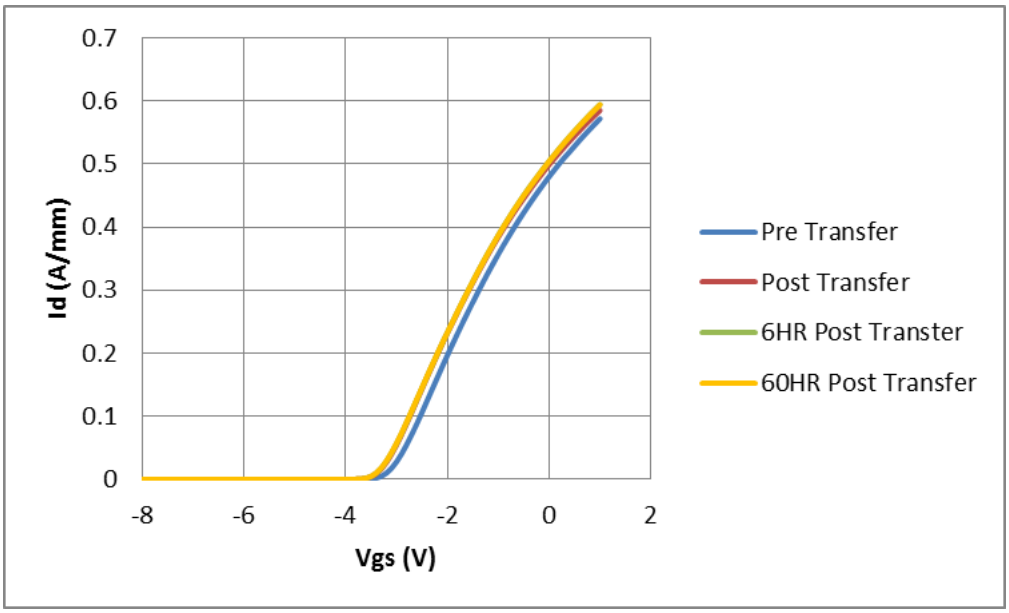

Figure 4.6: Transfer curves from device A2. Pre is from the initial characterization and post is after all 4 step-stress conditions. The device was then held at $V_{gs} = -8V$ $V_{ds} = 100V$ for 6 hours and 60 hours with characterizations in between. The device characteristics did not shift further after the step stress and was stable at the stress condition up to 60 hours.

hours and 60 hours. The results are shown in Figure 4.6. The pre and post curves represent the device before and after the 4 conditions step-stress experiment. The negative shift in V_{th} is observed as in the other devices. However, holding the device at constant stress, close to breakdown, for extended time did not produce additional change or degradation.

This further reinforces the claim that these devices do not have a critical voltage as defined by IPE theory. The next steps were to design and study these devices at the extreme stress conditions, close to breakdown, and understand when they would eventually fail and ultimately what is the failure mechanism.

4.2 Constant OFF-State Stress Experiment Details

The previous section showed that step-stress of AlGaN/GaN HEMTs, up to the breakdown voltage, in this process did not reveal the presence of a critical voltage. This suggests that FETs in this process are not susceptible to the inverse piezoelectric

effect. Therefore, it implies that the FETs in this process may be operated to their breakdown voltage limits without short term reliability effects. In this case it is important to know the consequences associated with long term operation close to the breakdown voltage of the device. This section will detail a constant stress experiment designed to solve this problem.

4.2.1 Device Details

In the initial set of constant voltage stress studies, a FET with the channel dimensions of device B was chosen. A few changes were made to the device and test setup from the step-stress experiment. First, the test FET gate periphery was reduced down to 2 gate fingers, each 50 μm of width, for a total gate periphery of 100 μm. The benefit being that it would allow failure analysis to be easier to conduct, as it leads to less area to search for a failure site. The drawbacks being lower leakage current levels, but these were well within the resolution of the SPA. Second, the SPA used in this part of the study was a Keithley 4200SCS. This instrument allowed for more test automation than the 4155C which was necessary for the long term stresses and characterizations. Third, the FETs were attached via epoxy and wirebonded in a semiconductor device package. It was determined that stressing with needle probes was not feasible as it was possible for the probes to move or vibrate off the pads either stopping the stress or causing immediate failure in the case where the gate probe lost contact (debiasing the gate) while the stress voltage was applied to the drain. The packaged test FET was then placed on a PCB board that was connected to the SPA.

4.2.2 Stress Method

In the stress test, the goal was to hold the device close to catastrophic breakdown until some device degradation was observed. An illustration of the targeted stress is shown in Figure 4.7. In this figure, a breakdown curve shows I_d vs V_{ds} for $V_{gs} = -8V$. As the drain bias approaches the breakdown voltage, the leakage current starts to rapidly increase. In this study we wanted to understand the impacts of holding the

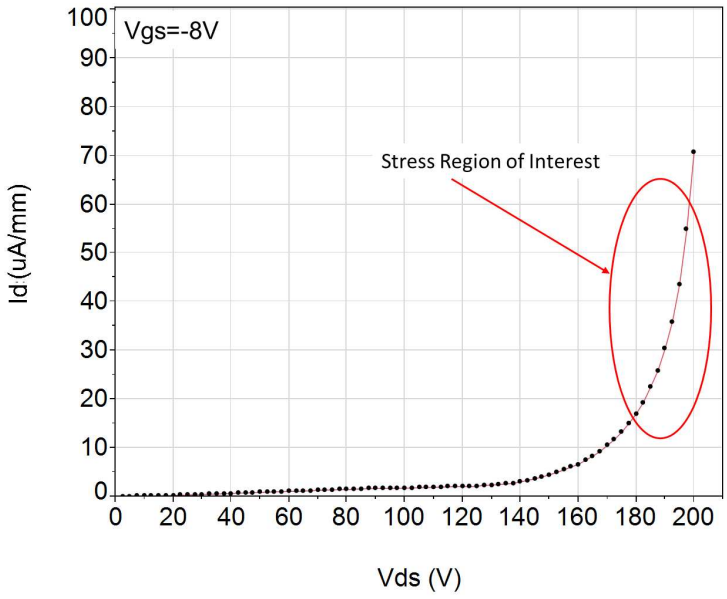

Figure 4.7: Example of a I_{ds} vs V_{ds} breakdown sweep from a device. As the applied bias approaches the breakdown voltage the drain current quickly rises to a runaway condition. Once breakdown is reached the drain current will surge leading to complete failure of the FET. In our breakdown study we wanted to understand the effects associated with stressing the device just before the breakdown condition occurs which meant stressing the device in the region highlighted by the red circle.

FET close to the breakdown voltage which meant stressing in the region depicted by the red circle in Figure 4.7.

At first, stressing the device in this region would seem trivial and accomplished by simply applying a stress voltage and letting the device run until failure. However, in order to preserve the device for failure analysis, protections were put in place to prevent an electrical over stress event (EOS) from shorting the device and leaving nothing useful remaining. Typically is done by setting a compliance current limit, below the defined breakdown current of $<1\ mA/mm$ and is thought to be sufficient in protecting the device. In practice this was found to not be the case.

In order to understand why this method is not sufficient in protecting the device, an understanding SPA operation is required. During the stress, the SPA will fix the voltage applied to a device and monitor the leakage current. Once the value is met or exceeded, the instrument will reduce the voltage to lower the current and bring

it back within compliance. This operation is not instantaneous and there exists the possibility the EOS will occur faster than the SPA is able to react, leading to a destroyed device. At first, an attempt was made by compensating with an external resistor in series with the drain. The reasoning is that a spike in drain current would induce a voltage drop across the resistor that would protect the device long enough to allow for the instrument to reduce the current. Values of the resistors used ranged from 10 $k\Omega$ to 100 $k\Omega$. With a 100 μm FET at a breakdown current of 1 mA/mm this equates to a 1 V to 10 V drop. Values higher than this were not considered as it would greatly impact the stress voltage that was applied to the device.

The drain resistors alone with the SPA in forced voltage mode was not always sufficient in protecting the device from catastrophic failure. As will be shown later in the chapter, once leakage current began to increase with stress time eventually the compliance current level would be reached. In this case, the SPA would continuously apply the stress voltage and need to be limited constantly by the compliance. This creates a situation where the SPA is constantly trying to set a voltage that would destroy the device, eventually leading to an EOS event. The final solution to this problem was to stress the device by operating the SPA in forced current mode.

The detailed mode of stressing the FETs in this study was as follows. The semiconductor parametric analyzer (SPA) was set to forced current mode. The voltage compliance was set at a desired value. In any constant forced current stress mode, the instrument continuously increases the applied drain voltage in an attempt to reach the set value of forced current. If the set value of the forced current is higher than the maximum leakage from a given device, the drain voltage reaches the compliance value before the drain leakage current attains the set value of forced current. Once drain voltage compliance is reached, the drain voltage is held fixed at the compliance limit by the instrument, effectively converting a constant current stress into a constant voltage stress. In this manner, the compliance voltage of the test becomes the

set point of the voltage stress and is hence a key parameter of the test.

The brilliance in this mode of stress is that when the leakage current increases, due to device degradation, the forced current level is reached and the voltage across the FET is dropped to safe level. This means that the SPA is no longer operating in compliance mode once the FET is in a vulnerable state to EOS, such as the onset of degradation. Utilizing this method, the vast majority of devices were still functioning after stress had concluded and allowed for in depth analysis to be conducted. The few devices that were lost were due to the forced current level being set significantly higher than the actual leakage of the device. It was discovered that forcing more than (100 $\mu A/mm$) than the device leakage current placed the FET at risk of an EOS.

In this experiment, ten devices were stressed with the method previously described. Each device was characterized in the ON-state prior to stress, at key points during stress, and finally at the end of stress. Additionally, OFF-state breakdown characterization occurred in between each stress. ON-state characterization consisted of measuring various device parameters including on-resistance (R_{on}), steady state drain current (I_{dss}), and max drain current (I_{dmax}), while OFF-state characterization consisted of measuring breakdown voltage (V_{bd}).

4.3 Constant OFF-state Stress Results and Discussion

4.3.1 Observations

A plot of the in-situ leakage currents for one of the devices in this experiment is shown in Figure 4.3.1. All three terminal currents (gate, drain, and source) are plotted. The general trend for all devices was the same, so this plot is representative of all stressed devices. Two key features that will be explored in detail are observed, these are referred to as breakdown voltage "walk-out" and "walk-in". These terms are linked to the voltage required to be forced to obtain a given leakage current in the OFF-state.

The sequence of applied stress of the device shown in Figure 4.3.1 is listed in Table

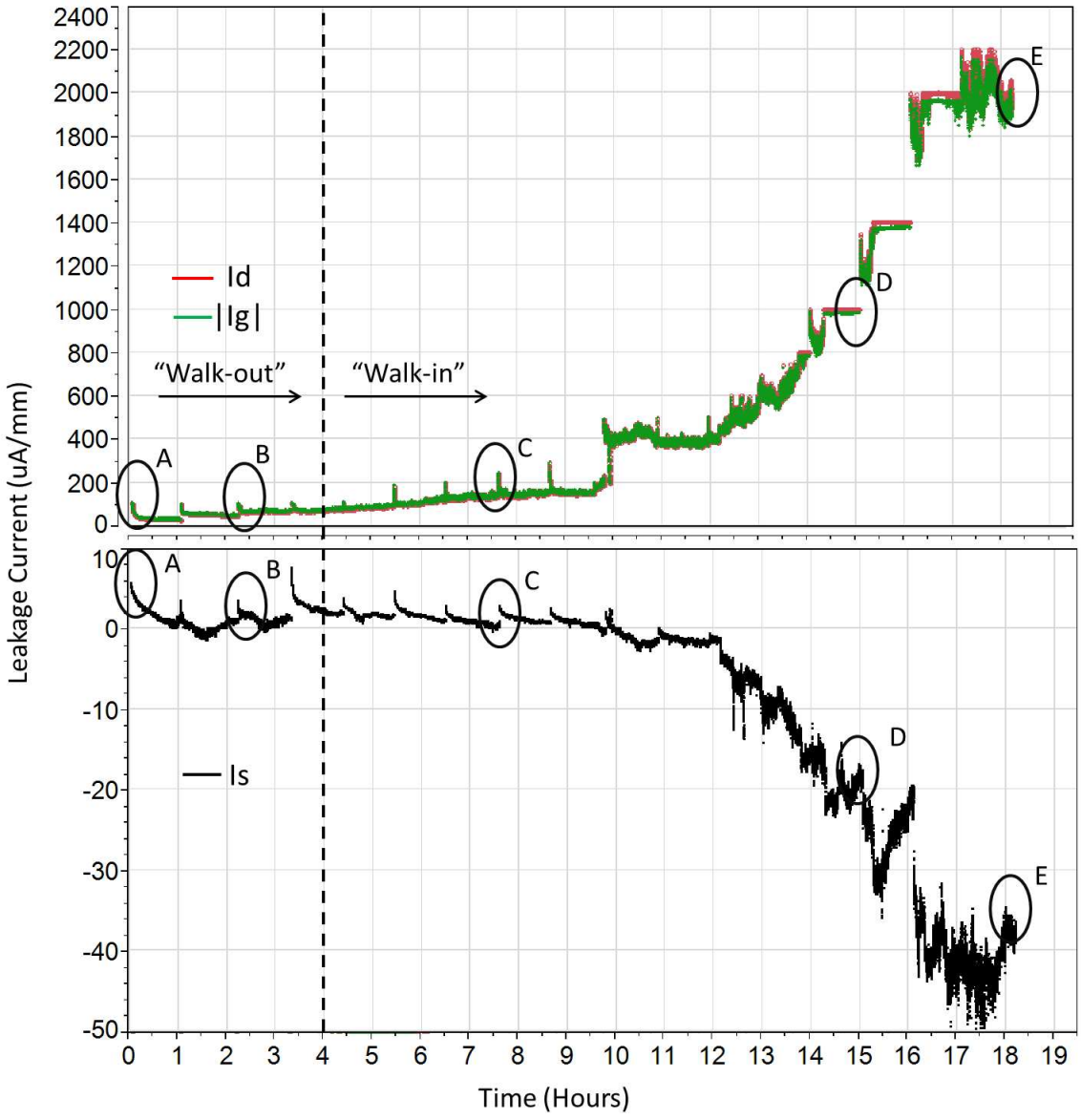

Figure 4.8: In-situ stress leakage data. Circles indicate ON-state characterization points. A) Initial B) Walk-out C) Walk-in D) 1mA/mm E) Final. (Top) In-situ magnitude of gate and drain leakage currents, note that I_d and $|I_g|$ are similar in magnitude, indicating that the majority of the forced drain current exits at the gate terminal. (Bottom) In-situ source leakage current. After the 12 hour point in stress, the leakage becomes increasingly negative, indicating the gate is losing control of the device channel, hence allowing some of the forced drain current to exit the source.

Table 4.2: Table showing the sequence of stress for the device stressed in Figure 4.3.1. Also listed are the points when ON-state and OFF-state characterization occurred.

Stress	Forced Id ($\mu A/mm$)	Drain Compliance (V)	ON-state Test	OFF-State Test
Pre Stress	-	-	A (Initial)	Initial
1	100	190	-	1
2	100	200	-	2
3	100	205	B (Walk-out)	3
4	200	205	-	4
5	200	205	-	5
6	200	205	-	6
7	400	205	C (Walk-in)	7
8	400	205	-	8
9	600	205	-	9
10	800	205	-	10
11	800	205	-	11
12	800	205	-	12
13	800	205	-	13
14	1000	205	D (1mA/mm)	14
15	1400	205	-	15
16	2000	205	-	16
17	2200	205	E (Final)	17

4.2. The five key points during stress (A-E) at which ON-state characterization was performed is listed in the table, and shown in Figure 4.3.1 by the circles, also labeled (A-E).

4.3.2 Walk-out

Breakdown voltage "walk-out" was observed to occur during the first three stresses in Figure 4.3.1 and Figure 4.9b. At these stress conditions the forced current was held constant at 100 $\mu A/mm$ and the compliance voltage was varied from 190 V-205 V. The reason to reduce the voltage early in the stress was to protect the device from EOS as the breakdown voltage for this device was approximately 200 V, prior to stress. Once the device breakdown was increased, to approximately 210 V, via walk-out, it was safe to constantly apply 205 V.

In stress 1, as walk-out occurs, the voltage required to maintain a given value of

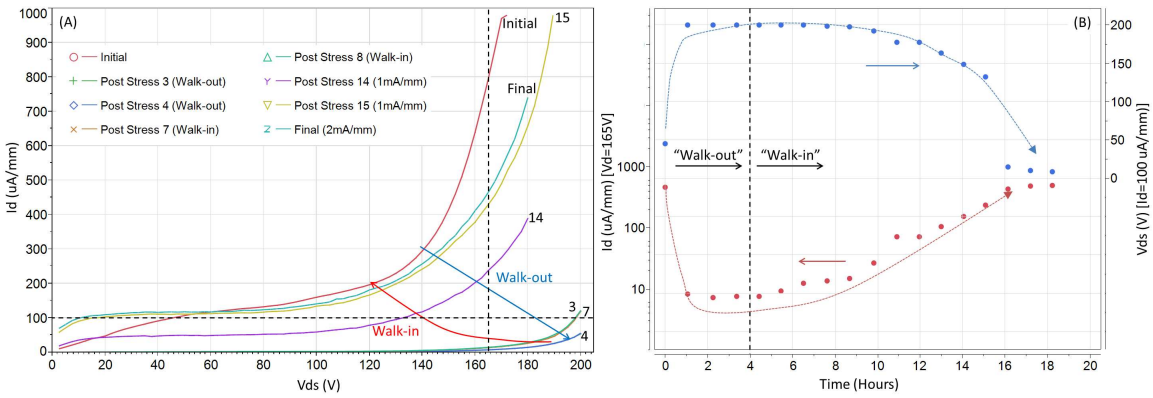

Figure 4.9: (A) Three terminal breakdown curves collected after every hour of stress. Only a subset of the curves are shown to illustrate the general behavior. The breakdown voltage is enhanced up until the 4th characterization point (walk-out). Later in the stress breakdown voltage begins to decrease shown by the 7th characterization and subsequent characterizations (walk-in). (B) To further illustrate walk-out and walk-in, a plot of drain current at $V_{ds} = 165V$ and drain voltage at $I_d = 100\mu A/mm$ from the breakdown characterization is shown versus stress time. The lines on the plots are a visual guide only.

leakage current increases, as shown in Figure 4.9b. In Figure 4.3.1, V_{ds} increases until it reaches the instrument compliance value, at which point the drain current stays at a level consistent with the leakage current in the device at the SPA applied drain voltage. "Walk-out" continues to occur, though at a slower rate, in stresses 2 and 3 as the drain voltage compliance is increased to 200 V and 205 V. The stress compliance was not increased beyond 205 V to provide a 5 V margin and avoid a catastrophic breakdown event.

The phenomenon of breakdown walk-out during stresses 1-3, is evident in three terminal breakdown voltage sweeps shown in Figure 4.9a. The impact of walk-out on drain leakage from the initial state to just after stress 3 are shown between curves "initial" and "post stress 4" in Figure 4.9b. The leakage in the device has been dramatically reduced and the breakdown voltage has been greatly enhanced.

These findings are consistent with the results reported by Ladbrooke et al. [106] in GaAs MESFETs and in greater detail by Menozzi et al. [107] on commercial GaAs pHEMTs. In these studies, the "walk-out" mechanism is attributed to the trapping of

electrons at the semiconductor surface and dielectric passivation interface or within the passivation layer itself. Trapped electrons act to locally deplete the channel, lowering the peak electric field at the drain side of the gate, leading to an increase in V_{bd}. It was found that this mechanism was recoverable as shown in Figure 4.3.1, at each stop/start point for characterization there is an increase and initial drop in leakage current. This further supports the carrier trapping hypothesis.

4.3.3 Walk-in

Continued stress in the OFF-state leads to the observation of breakdown voltage "walk-in". Beyond the 3rd stress progressively less voltage is required for a specific leakage current. To maintain the $205V$ compliance voltage, the SPA forced drain current was stepped up over the course of the test, as shown in Table 4.2. Walk-in may be parametrically observed in Figure 4.9b as decreasing values of drain voltage required to reach the monitored leakage current. In Figure 4.3.1, walk-in is evident after a stress time of 4 hours, as increasing amounts of drain current must be forced to hold the device at 205 V.

The drain leakage increases slowly between 4 and 10 hours of stress time, as seen in Figure 4.3.1. Shortly before the 10 hour point there is an abrupt increase in drain-gate leakage current of 200 $\mu A/mm$ after which the leakage in the device starts to rise more rapidly. Simultaneously, at the 10 hour point, the source terminal leakage begins to trend negative indicating that some of the forced drain current is being sinked to the source terminal. The device leakage starts to accelerate rapidly after the 13 hour point. From this point until the end of the stress, the drain and gate leakage rises from 800 $\mu A/mm$ to 2200 $\mu A/mm$ and the source leakage increases from 5 $\mu A/mm$ to 50 $\mu A/mm$. The increase in gate leakage suggests a degradation of the gate Schottky properties. Due to this degradation in Schottky properties the gate contact is not able to effectively control the channel leading to the observed increase in source current. The increase in gate leakage is much larger in magnitude than the

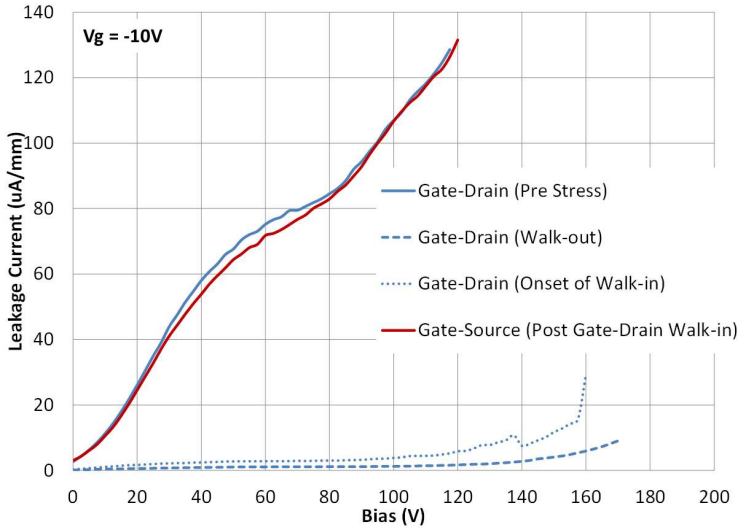

Figure 4.10: Breakdown curves of a device used in this experiment. The blue lines are from three terminal breakdown characterization with the source grounded, $V_{gs} = -10V$, and V_{ds} swept positive in voltage. The blue lines track the device from initial, walk-out, to walk-in. After walk-in had occurred the three terminal breakdown was reversed, shown by the red line, with drain grounded, $V_{gd} = -10V$, and V_{sd} swept positive in voltage. The result was that the source side of the device seemed to be relatively unaffected by the stress on the drain side.

increase in I_{ds} suggesting that the degradation is not buffer related.

The effects of walk-in are clearly shown by the OFF-state breakdown characterization in Figure 4.9a. The first characteristic to note is that during the onset of walk-in between stresses 4 and 9 the leakage curves remain unchanged at low voltages ($<100\ V$) but differ from each other at high voltages. After stress 9 the shape of the breakdown curve starts to change below $100\ V$. From stress 11 to the final stress point two changes occur in OFF-state characterization. First, the voltage necessary to induce a rapid increase in drain current continues to reduce, keeping with the trend observed between stresses 4 and 9. Second, an overall increase in drain leakage at low voltages starts to occur. This further points to a degradation in Schottky gate diode properties as the mechanism for the observed degradation and suggests that the current transport mechanism has less of a field dependence with sustained stress.

A test was performed to determine if the gate-source region of the device was

affected by the stress up to the onset of "walk-in". One device was stressed to the point of "walk-in" and then characterized for 3 terminal breakdown in both typical ($V_{gs} = -10V$, V_{ds} swept from 0 to 200 V) and reverse configuration ($V_{gd} = -10V$, V_{sd} swept from 0 to 200 V). As this is a symmetric device, it was reasonable to expect that the leakage characteristics in either configuration would be similar since there were no differences between the source and drain access regions. Figure 4.10 shows the result of this test. It is clear that leakage in the reverse configuration after "walk-in", is almost identical to the pre-stress leakage in the normal configuration. This suggests that any degradation that occurs in the device is localized to the gate-drain region of the device until "walk-in". The hypothesis being that the degradation is localized to the drain edge of the gate contact.

4.3.4 ON-State Characterization

Device characterization in the ON-state at points A-E reveals minimal degradation in charge transport of the device. A transfer plot of I_d and $|I_g|$ versus V_{gs} is shown in Figure 4.11. The gate leakage during characterization first decreases after walk-out and then begins to rise during the onset of walk-in. The drain current behavior differs in that nearly all of the change is observed in the subthreshold region of the curve $V_{gs} < -4V$.

A summary of the ON-state parametric change is shown in Table 4.3. The ON-state parameters I_{dss} and I_{dmax} show very little change from initial to walk-in. Once gate leakage begins to increase during walk-in these parameters do decrease but still remain within 5% of their original value. The reduction in parameters I_{dss} and I_{dmax} are likely due to the large increase in gate leakage. After an initial increase in R_{on} during walk-out the value remained unchanged after subsequent characterizations. The increase in R_{on} is consistent with the proposed walk-out mechanism of surface trapping of carriers, leading to an extension of the depletion region in the channel. The value of R_{on} varied no more than 7% of it's initial value.

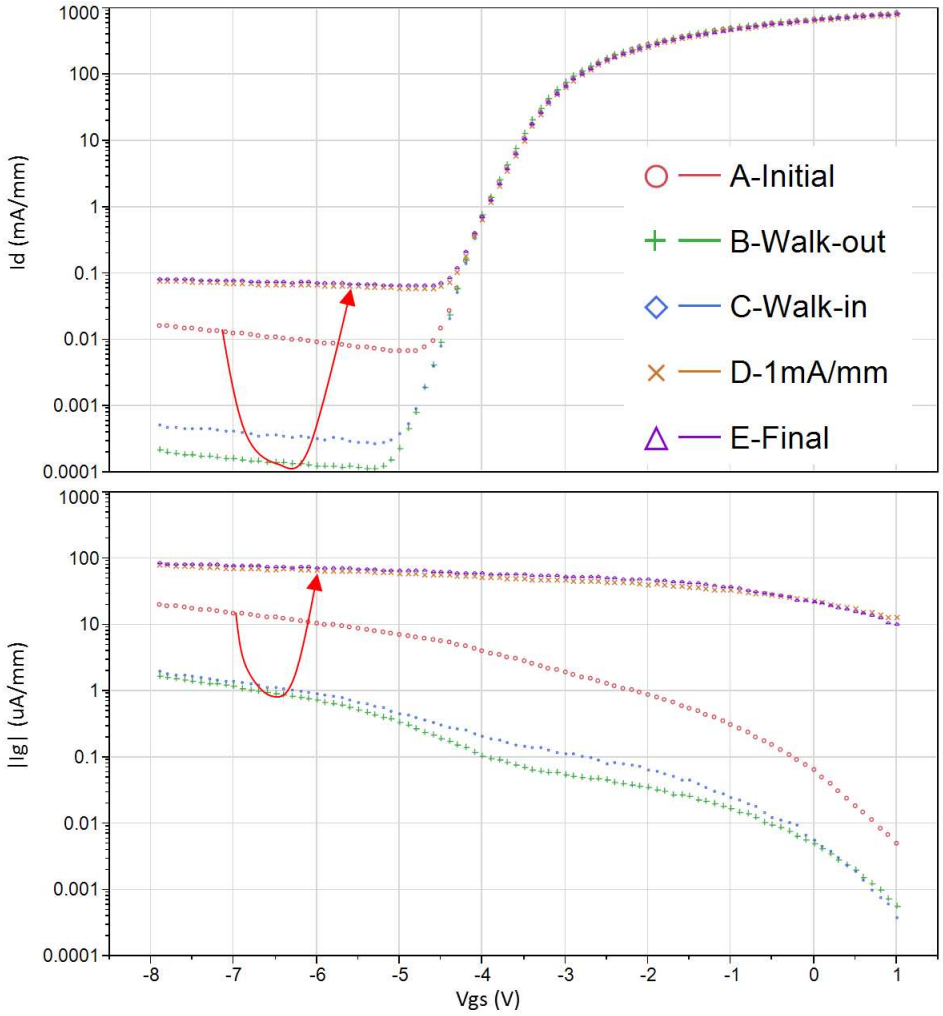

Figure 4.11: Transfer curves from the ON-state characterization that was performed at the 5 points A-E during stress. Large changes in device characteristics are evident in the I_d vs V_{gs} plot, in the subthreshold region of the curve $V_{gs} < -4V$. Once the device turns on the changes in drain current are minimal. However, the degradation is evident throughout the entire sweep in the I_g vs V_{gs} plot.

Table 4.3: Summary of the ON-state parametric shifts observed at the five characterization points (A-E). Shown is the measured value and the percent change from the initial measurement.

Stress Point	Ron (Ωmm)	Idss (mA/mm)	Idmax (mA/mm)
A-Initial	2.61	672.7	824.7
B-Walk-out	2.79 (+6.45%)	676.1 (+0.05%)	827.1 (+0.3%)
C-Walk-in	2.79 (+6.45%)	666.7 (-0.1%)	818.9 (-0.7%)
D-1mA/mm	2.77 (+5.78%)	650.5 (-3.3%)	801.1 (-2.95%)
E-Final	2.76 (+5.43%)	648.3 (-3.6%)	799.8 (-3.11%)

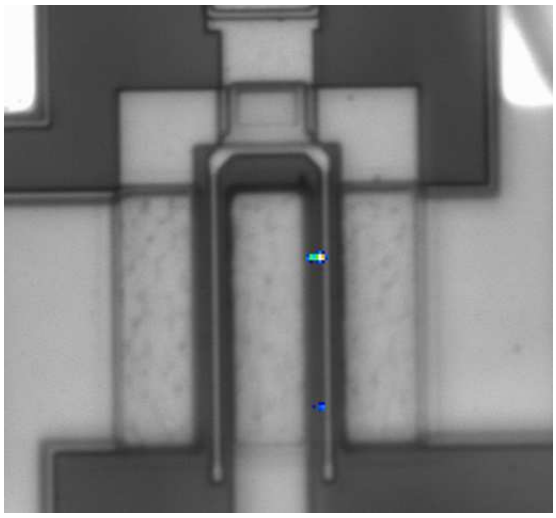

Figure 4.12: Image of device in this study biased with $V_{gs} = -10V$ and $V_{ds} = 10V$ showing localized electroluminescence (EL), similar to that reported in [100] [102]. The localized EL has been hypothesized in literature as being the defect site responsible for the observed degradation.

The magnitude of these results contrast with reported IPE literature [86] [87] [88] [109], that shows significant changes (>10%) to channel charge and transport parameters.

4.3.5 Failure Analysis

At the conclusion of the constant stress experiment, the devices that still functioned after walk-in were then studied to see if a physical mechanism could be identified that would explain the degradation observed during walk-in. The primary method of identifying failure sites is to bias the device in the OFF-state and look for localized electroluminesce (EL) emission within the device channel. The localized

emission sites have been hypothesized to be the area of degradation during the stress test [100] [102].

In this experiment it was discovered that all devices had such localized EL when biased in the OFF-state. An example of one device is shown in Figure 4.12, biased at $V_{gs} = -10V$ and $V_{ds} = 10V$. The EL is present on the right side gate finger. Once the EL was discovered a laser was used to mark the locations on the adjacent source finger to ensure that cross sectional cuts were made at the precise location in the channel that the EL appeared.

Next the device was cut at the EL location, perpendicular to the gate finger, using a focused ion beam (FIB). This section of the device was then removed and imaged using scanning transmission electron microscopy (STEM) in an attempt to identify any macroscopic crystal defects such as a crack or pit that would be consistent with IPE degradation. After imaging seven devices stressed to walk-in and one control, in two different failure analysis labs, no crystal defect could be found.

There was still the possibility that a microscopic defect was present at the EL site that could not be optically observed. Next, three devices and the control were tested to see if the defect could be uncovered via elemental analysis. Using a combination of both energy dispersive spectroscopy (EDS) and TEM electron energy loss spectrum (EELS) it is possible to identify, spatially, the locations of various elements. All metals in the gate contact, along with aluminum (Al), gallium (Ga), nitrogen (N), and oxygen (O) were examined. At the EL sites all elements were present in their as processed locations. No metal from the gate stack was observed to have diffused into the semiconductor. Also, no oxygen was found in the semiconductor, as was observed in the IPE literature. Based on these findings it was considered unlikely that the degradation in this study was due to IPE.

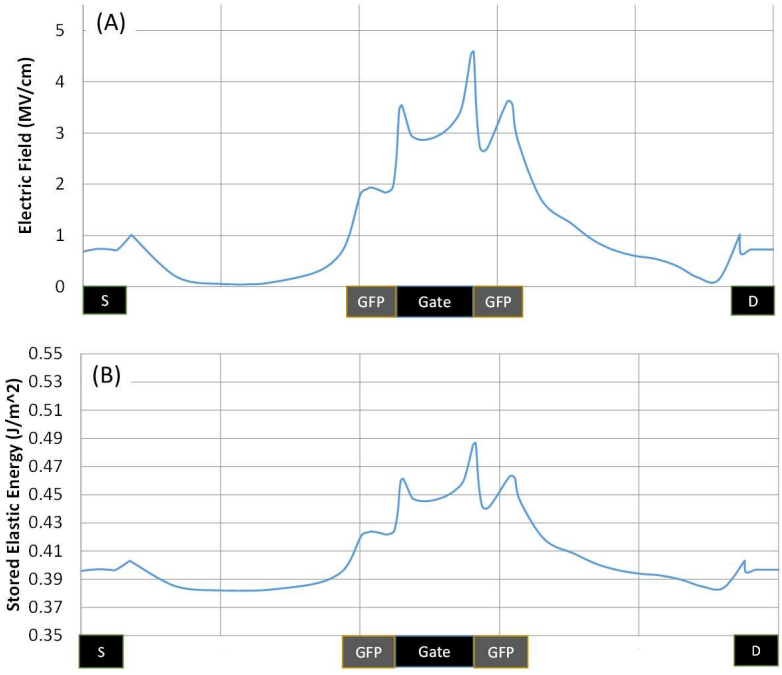

Figure 4.13: (A) Electric field distribution and (B) stored elastic energy profile in the device channel. The bias condition simulated is the same as the constant stress condition ($V_{gs} = -10V$ and $V_{ds} = 205V$). Device simulations results from an AlGaN/GaN HEMT model developed in Sentaurus TCAD.

4.4 Applied Electric Field Simulation

The observations from the step-stress experiment and the failure analysis from the constant stress experiment suggested that the devices in this study did not have a critical voltage and by extension not susceptible to degradation via IPE. If this were true then the IPE model reported in [89] should confirm this result. The IPE model states that crystal defects are generated when the stored elastic energy in the crystal at any point within the channel exceeds the critical stored elastic energy. This requires the electric field profile under stress to be known.

The electric field profile for the devices used in the constant stress experiment was simulated using a device model developed in Synopsys Sentaurus TCAD. The FET in this model was modified to reflect the layout changes made to the qualified layout. The device was then simulated at the constant stress bias condition ($V_{gs} = -10V$

and $V_{ds} = 205V$). The plot of the electric field profile is shown in Figure 4.13a. The x-axis of this figure is cross section of the FET channel from source to drain as pictured in Figure 4.1. The boxes under the x-axis denote the locations of the source, gate, and drain contacts. The "GFP" boxes represent the gate metal field plate as a consequence of the T-gate process. The electric field in the channel spikes at the edge of any metal contact or field plate. The vast majority of the electric field is concentrated around the gate contact and is highest at the gate edge on the drain side as expected.

The stress and strain coefficients may be calculated by using the method detailed in chapter 3 and using the piezoelectric coefficients detailed in Table 3.2. Once the stress and strain coefficients are calculated it is then possible to translate the electric field profile to a distribution of stored elastic energy in the channel, shown in Figure 4.13b. This simulation shows that the peak stored elastic energy in the AlGaN barrier layer to be just under 0.49 J/m^2, for the stress applied in this experiment. To put this number into context a calculation of the critical elastic energy is required for the AlGaN barrier thickness and Al mole fraction used in these HEMTs. This was calculated to be 0.7 J/m^2, which is greater than the simulated peak elastic energy. Therefore, it is reasonable to conclude the degradation observed in this experiment cannot be attributed to IPE.

4.5 Safe Operating Voltage

Earlier in the chapter a problem was raised regarding the voltage limits in the OFF-state, if a device did not have a critical voltage and exhibited degradation due to IPE. It was shown in the subsequent experiment that operating the AlGaN/GaN HEMT 5 V from the breakdown voltage did induce significant device degradation. Then it is of interest to understand how much margin between the operational point and the breakdown voltage is necessary for reliable operation. In doing so it would be possible to define a safe operating point for a given device and application.

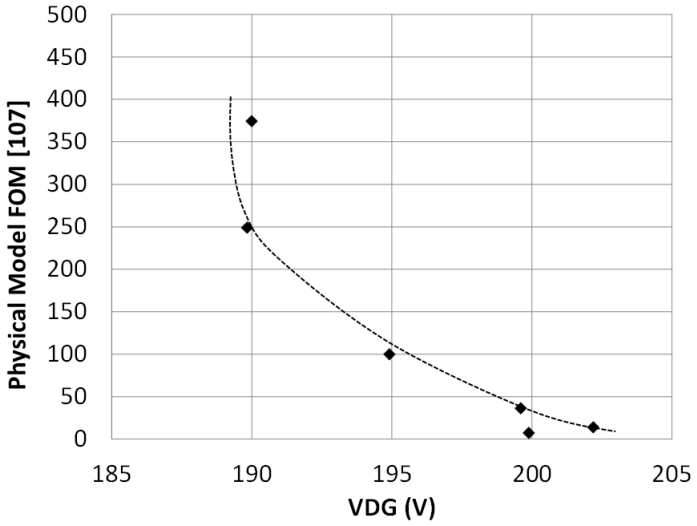

Figure 4.14: Using the field acceleration law reported in [110] on AlGaAs/GaAs HEMTs, an attempt was made to fit the data from devices in this study at different stress voltages. Since the voltage was increased after walk-out, the average voltage applied to the device during the constant stress is plotted. This result shows that the lifetime figure of merit rapidly increases backed off from breakdown. This suggests there exists a voltage after which lifetime rapidly degrades.

A field accelerated lifetime figure of merit was derived for AlGaAs/GaAs HEMTs in [110]. In this publication it was shown that experimentally observing time to failure and gate current versus varying stress voltages, it was possible to determine a safe operating voltage. In an attempt to replicate this study additional devices were stressed at lower voltages, using the time to the first step increase in gate current as the failure criteria. This produced devices with a range of time-to-failures (TTF). A plot of the average stress voltage versus the figure of merit described in [110] is shown in Figure 4.14. This suggests that the lifetime of the AlGaN/GaN HEMTs rapidly degrades beyond a certain voltage. Therefore it is reasonable to expect that with sufficient time and resources the curve may be filled in for lower voltages allowing for the extraction of voltage that would define the safe operating limits of the device (and by extension the technology) for a reasonable lifetime in the end user application.

4.6 Summary

In this chapter, an OFF-state reliability assessment of the AlGaN/GaN technology on devices from this process was presented. First, a step-stress experiment was conducted as recommended in literature to do a quick assessment of process reliability. No significant degradation was observed and neither was a critical voltage found up to 90% of the device breakdown voltage.

To determine the reliability consequences associated with operating the device near the breakdown voltage, a constant OFF-state stress experiment was conducted. Utilizing a novel stress method the AlGaN/GaN HEMTs were able to be stressed within $5V$ of the breakdown voltage, while still protecting the device from an EOS failure. This allowed for the physical analysis of the devices in hopes of uncovering a root cause mechanism. The results from this experiment shows that two different device altering mechanisms occur during stress. The first is breakdown voltage walk-out, identified by a reduction in leakage current and an enhancement of breakdown voltage. This was attributed to surface trapping and the virtual gating effect as described in literature. The second mechanism was breakdown voltage walk-in which consists of an increase in gate leakage current and a reduction in breakdown voltage.

Failure analysis was performed and it was found that localized EL emission in the channel may be identified suggesting the site of the observed degradation. FIB cuts at the EL site and subsequent TEM did not reveal the presence of a crystal defect. Furthermore, elemental analysis on the FIB section did not produce any compelling results. This led to the conclusion that the degradation was not due to IPE. To confirm this conclusion a simulation of the electric field profile during stress and a calculation of the stored elastic energy was performed. It was found that the stored elastic energy did not exceed the calculated critical elastic energy for the AlGaN barrier layer in this heterostructure.

Finally, a short experiment was conducted varying the stress voltage; by defining

the failure criteria as the point at which the first step leakage current increase of walk-in is observed, a range of time-to-failures was extracted. By plotting these failures against a field accelerated FOM proposed by [110] for GaAs devices it was clear that the lifetime of the devices rapidly increases with additional margin between the stress voltage and breakdown voltage. This suggests that for a given technology and device a safe operating voltage may be extracted for a given application.

CHAPTER 5: ANALYSIS OF TIME DEPENDENT E-FIELD DEGRADATION

This chapter will build on the results of the previous chapter and provide additional analysis on the degradation observed during constant, high electric field, OFF-state stress. In chapter four, it was found that stress near the breakdown voltage leads initially to a breakdown voltage walk-out observation where device leakage is reduced and the breakdown increased. With continued stress the device entered breakdown voltage walk-in, during which leakage current increased and breakdown voltage was reduced. The latter was shown to induce permanent degradation of the device but no clear failure mechanism was identified.

This chapter will present a repeat of the OFF-state stress detailed in the last chapter and a careful analysis of the AlGaN/GaN HEMTs at each stage of stress in order to provide insight into the actual source of degradation and to better understand some of the underlying physical mechanisms. The analysis will consist of two parts. The first is an electrical analysis of both the breakdown mechanism of the FET and the gate diode properties are altered with OFF-state stress. The second part will involve a detailed optical analysis to understand how the dominant EL emission that was shown in Figure 4.12 evolves will stress and a method of confirming that this EL site corresponds to the region of the gate finger responsible for the increase in leakage current with stress.

5.1 Time Dependent Degradation Analysis Experiment Details

To gain insight into the changes that occur in the device after breakdown voltage walk-out and walk-in, six devices were characterized in detail using two different methods. First was a detailed electrical analysis that included over temperature

breakdown and gate diode characterization. The second method was a detailed optical analysis using both electroluminescence and infrared thermal imaging.

Six devices were fully analyzed in three stages at varying degrees of stress, as shown in Table 5.1. The ensuing sections provide the details of the experiment.

Table 5.1: Six devices were electrically and optically analyzed in detail to uncover physical effects of constant OFF-state stress. The analysis occurred in three stages with the devices at different levels of degradation.

Device	First Analysis	Second Analysis	Third Analysis
1	Initial	Walk-out	Walk-in
2	Initial	Walk-out	Walk-in
3	Walk-out	Walk-in	-
4	Walk-out	Walk-in	-
5	Walk-in	-	-
6	Walk-in	-	-

5.1.1 Device Details

In this experiment the AlGaN/GaN HEMTs had the same channel dimensions as device A, detailed in the previous chapter. The gate length (L_g) was $0.5\mu m$ and had the same gate-to-drain distance as gate-to-source ($L_{gs} = L_{gd} = 1.3\mu m$). The transistor gate periphery (100 μm) and finger configuration ($2X50\mu m$) was the same as the device used in the constant stress experiment of chapter 4. The device did not have source connected field plate, but a gate field plate was present as a consequence of processing the T-gate. The representation of the channel cross section shown in chapter 4 remains accurate, shown in Figure 4.1.

5.1.2 Breakdown Characterization

In order to better understand the breakdown limitations within the AlGaN/GaN HEMT, breakdown voltage of the device was characterized via the drain current injection method, as reported by Bahl et al [111] in GaAs MESFETs and AlGaAs/GaAs HEMTs. This method consists of forcing a constant current into the drain terminal (with a maximum compliance limit imposed on drain voltage) while sweeping the gate

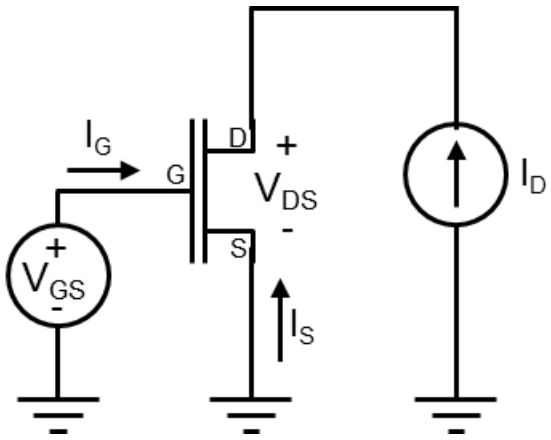

Figure 5.1: Schematic of the drain current injection method used to determine device breakdown [111]. This method of characterization was used in this study to understand the device physics of breakdown.

bias to transition the device from the ON to OFF-state. A schematic of the forced drain current method is shown in Figure 5.1.

Typically breakdown voltage for most FET devices in either GaAs or GaN technologies, is defined as the voltage at which the drain current reaches a value of $1mA/mm$. Based on this definition of breakdown voltage, it may be expected that the drain current injection method would force a drain current of 1 mA/mm. However, in practice, this level of current causes irreversible damage to the FET gate diode. To ensure that the device was not damaged during characterization the forced drain current was reduced to 300 $\mu A/mm$. In order to verify that the characterization did minimal damage to the device, multiple characterizations were conducted and these were found to be identical.

A plot of the characteristics obtained from a representative device using the drain current injection method is shown in Figure 5.2. It is seen that the characteristic can be divided into five distinct regions denoted by the Roman numerals on Figure 5.2. Insight into the device operation and breakdown mechanism is obtained by analyzing these five distinct regions of the V_{dg} vs V_{gs}, V_{ds} vs V_{gs}, and I_g vs V_{gs} curves of which, the first four were extensively described in [111] for AlGaAs/GaAs HEMTs.

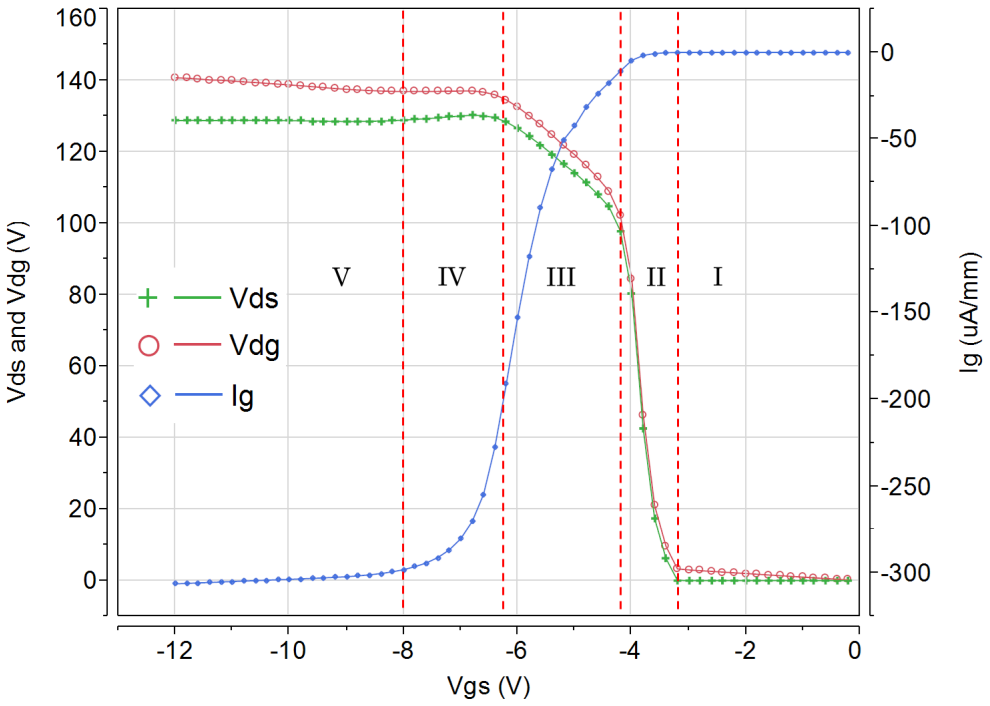

Figure 5.2: Drain current injection measurement used to determine device breakdown. Forced drain current used in this study was $300\mu A/mm$. This method is useful determining device breakdown and the physical mechanism limiting max voltage on the device. Region I and II represents the device transitioning from the linear to saturation regions in the ON-state operation. Region III represents channel breakdown (V_{ds} breakdown) as the device is now in the OFF-state and the gate current is relatively low with respect to the drain current. Region IV is when the device transitions from channel breakdown to drain-gate breakdown (V_{dg} breakdown) as evidenced by the constant value of V_{dg} in this region. A region V was identified in this study that was not previously reported in [111] at which the device is once again limited by drain-source breakdown as V_{ds} is constant in this region. It is not known what mechanism is limited V_{ds} in this region but it could be related to buffer breakdown or channel avalanche breakdown as the electric field in this region is 100 V/um.

Region I of the curve represents the linear (or resistive) region of operation. Region II occurs when the device enters saturation. Region III shows the channel breakdown of the device (V_{ds} breakdown). This is because the device has transitioned to the OFF-state but the gate current is small compared to the drain current, indicating that drain to source leakage is dominant. Region IV represents the breakdown of the gate-drain diode (V_{dg} breakdown). This is evident as the gate current is rapidly increasing to match the forced drain current value indicating all of the leakage current is moving from the drain to gate terminal. The V_{ds} curve confirms this behavior as it is decreasing in III, which indicates I_{ds} is decreasing as more current is traveling through the gate diode. Furthermore, the slope of the V_{dg} vs V_{gs} curve is flat in this region indicating the voltage value is clamped which is an indication of breakdown limiting mechanism. A fifth region (V) was observed in these devices, that was not reported in [111], when the gate was biased below $-8V$ ($V_{gs} < -8V$). In this region devices enters a state where breakdown is limited by V_{ds}, since slope is flat versus V_{gs}, once again indicating the voltage is clamped to a constant value and is a signature of a breakdown limiting mechanism. The limiting mechanism in region V is not clear at this time, possibilities could include avalanche breakdown of the channel or buffer breakdown.

Figure 5.2 shows the maximum V_{ds} is 129 V and the maximum V_{dg} is 140 V at $20°C$ for these devices. These voltages can be referred to as the breakdown voltages at the specific drain current chosen. It is important to note that no catastrophic event has occurred and any irreversible degradation of the device is minimized, as evidenced by the repeatable nature of these characteristics.

5.1.3 Electrical Stress

In this experiment, six devices were stressed in the same method as the constant stress detailed in chapter 4. This included forcing a drain current in the OFF-state that was slightly higher than the leakage current, while setting the compliance volt-

age to the desired stress voltage. This stress technique previously demonstrated the ability to hold the device close to the breakdown voltage and therefore accelerate the degradation mechanism while at the same time providing enough margin to prevent an EOS event.

The gate bias was held at $V_{gs} = -10V$ and the induced drain bias was set to $V_{ds} = 120V$. The device was stressed in four to eight hour intervals with a three terminal sweep of the breakdown voltage between each interval. The stress intervals were set to eight hours initially as minimal change was observed. Once degradation was observed, intervals were shortened to collect more characterization data. During the entire stress the device was held at room temperature.

5.1.4 Electrical Degradation

A plot of the drain (I_d) and gate (I_g) terminal leakage currents during the stress of a representative device are shown in Figure 5.1.4. Both gate and drain current are of similar magnitude, indicating the leakage current is dominated by drain to gate leakage, while drain to source leakage is negligible. This is consistent with the behavior observed in on devices in chapter 4.

After every stress interval the device breakdown voltage was characterized via a three terminal breakdown measurement. During this characterization the bias conditions were, $V_{gs} = -10V$ and V_{ds} was swept from 0 V to 125 V. A plot of the breakdown sweeps is shown in figure 5.4. In this figure only a subset of the breakdown sweeps are shown to illustrate the evolution in the breakdown characteristics with stress. During the walk-out portion, the breakdown voltage is enhanced and the leakage decreased from the initial sweep to the first and eighth characterization points. The breakdown sweeps corresponding to when the device leakage began to increase during walk-in is shown in the remaining sweeps. Once again, these results were consistent with the previous constant stress experimental study.

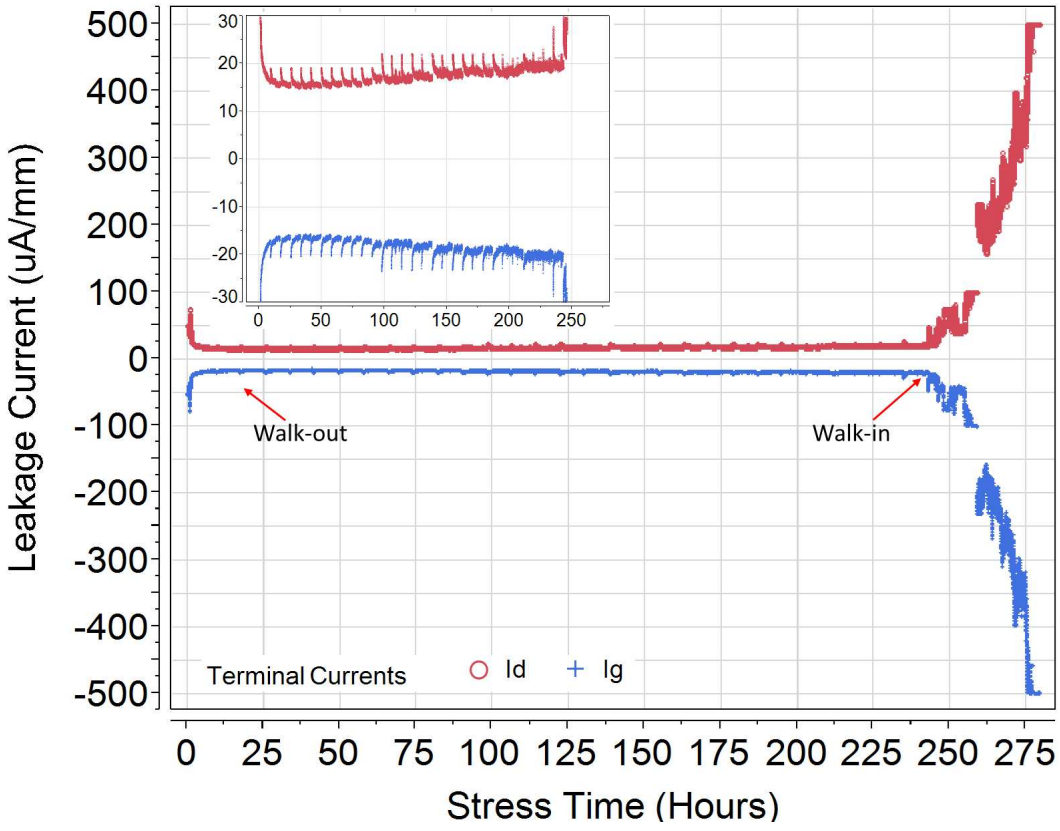

Figure 5.3: Leakage currents measured at both the drain and gate terminals during stress. Both I_d and $|I_g|$ are nearly identical, indicating all leakage in the device is from gate to drain. After initial application of stress a rapid decrease in leakage current is observed corresponding to breakdown voltage walk-out. After 245 hours of stress the device shown starts to enter breakdown voltage walk-in as evidenced by the rapid increase in gate-drain leakage current. Once walk-in begins the leakage current continues to increase with stress time until the test was stopped after device leakage current reached 500 $\mu A/mm$.

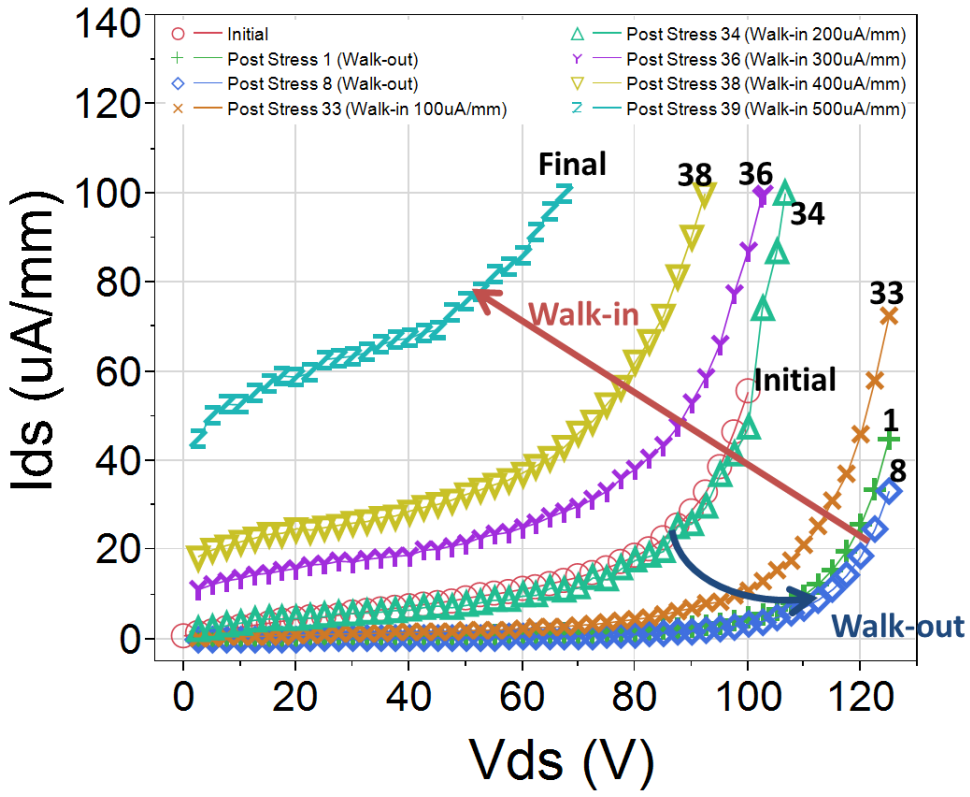

Figure 5.4: A plot of three terminal breakdown characterization that was performed at multiple intervals during the stress test of the device shown in figure 5.1.4. The test condition was $V_{gs} = -8V$ and V_{ds} was swept from 0 V to 125 V. The compliance current was set to 100 $\mu A/mm$ to prevent damage to the device. Breakdown voltage walk-out observed in figure 5.1.4 is apparent from the initial characterization prior to stress to the first and eighth characterization as the breakdown sweep is now able to sweep to the 125 V limit. The breakdown voltage walk-in state is clearly observed after the 33rd characterization point (approximately 245 hours into the stress) as leakage current is increased with each additional sweep until the device hits the compliance limit at 70 V after stress testing was concluded.

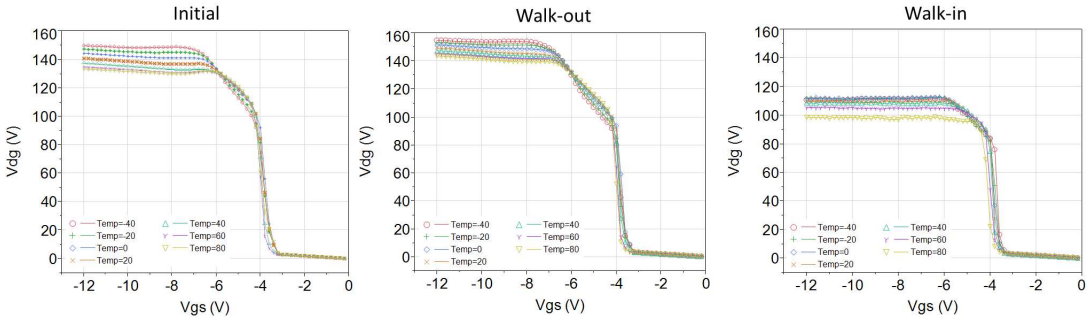

Figure 5.5: Drain current injection characterization with temperature shown at initial, walk-out, and walk-in. Prior to stress the device breakdown has a strong temperature dependence. With increasing stress times the temperature dependence collapses as the gate diode barrier degrades with stress.

5.2 Electrical Analysis

Electrical characterization of the stressed device at each stop point versus temperature was analyzed for insight into the root cause of the observed "walk-in" degradation. To study this phenomenon, characterization of device breakdown via drain current injection and a two terminal voltage sweep of the gate diode was performed over temperature at three different time periods. The "initial" characterization was done prior to application of stress. The "walk-out" characterization was performed immediately after the application of OFF-state stress for one hour. The "walk-in" characterization was performed after the device had reached the targeted leakage current of 500 $\mu A/mm$. The characterization with temperature data was collected from $-40°C$ to $80°C$ in $20°C$ increments.

5.2.1 Drain Current Injection Characterization

A plot of the drain current injection characterization is shown in Figure 5.5. Characterization of device breakdown across all three stages was consistent with behavior that was observed by the 3 terminal breakdown characterization that was performed after each stress interval. From initial to walk-out an increase in breakdown voltage is observed at all of the temperature points. During the initial characterization, the channel breakdown region of the curve, between $V_{gs} = -4V$ to $V_{gs} = -6V$, shows in-

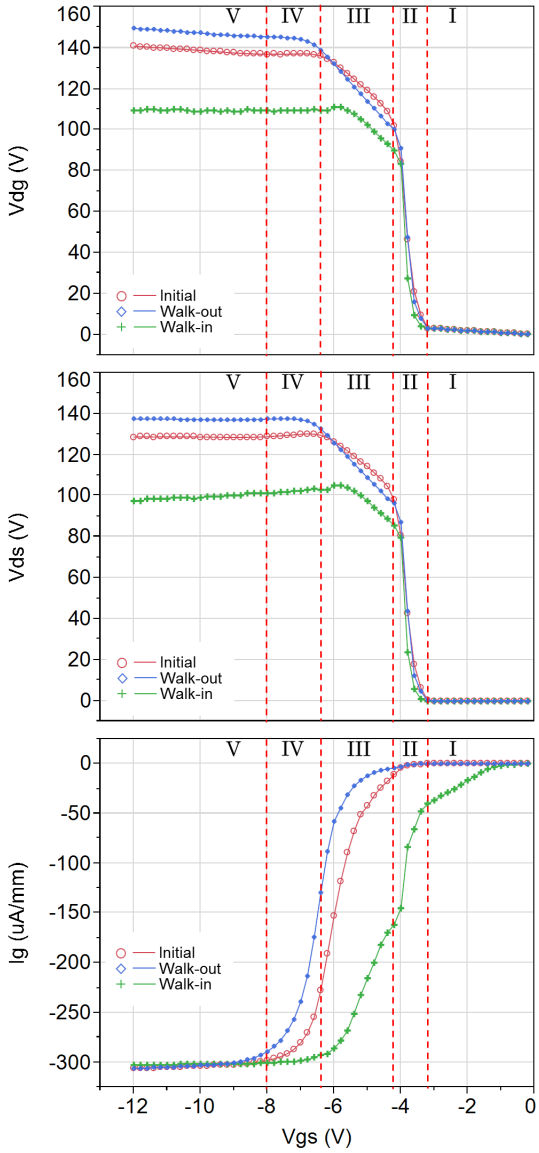

Figure 5.6: Drain current injection characterization of a representative device from initial to walk-out and finally to walk-in at room temperature. After walk-out it appears the region III shown in figure 5.2 has expanded to more negative V_{gs} as gate leakage has been reduced. This is evident in the plot of I_g vs V_{gs} the amount of reverse gate bias needed for conduction to occur from drain to gate has increased. After sufficient stress to push the device into the walk-in state the region V that was shown in figure 5.2 appears is no longer observed. Instead the device remains in a state limited by V_{dg} breakdown as V_{dg} remains constant and V_{ds} is decreasing. This is likely due to the a degradation in Schottky properties that no longer is able to effectively block reverse leakage current. It is worth noting in the I_g vs V_{gs} plot, after walk-in the curve shape is altered in region III and has several inflection points that previously did not exist. This region corresponds to the device transitioning from the ON-state to the OFF-state. These inflection points represents different sections of the gate periphery turning pinching off the device channel at varying levels of bias. This is due to various levels of degradation localized within the gate periphery of the device and provides evidence that degradation is localized within the gate periphery of the device.

creasing breakdown voltage at higher temperatures. Once the device exits the channel breakdown region ($V_{gs} < -6V$) the trend reverses as the breakdown voltage increases with cooler temperatures. After walk-in a reduction in breakdown voltage is shown and the temperature dependence of the breakdown curves is greatly reduced. Virtually no difference in breakdown can be observed in the device shown in Figure 5.5 for ambient temperatures between $-40°C$ to $40°C$.

A direct comparison at each device state from the drain current injection characterization at $25°C$ is shown in Figure 5.6. This figure shows V_{dg}, V_{ds}, and I_g versus V_{gs}. The shift in breakdown is evident in both the V_{dg} and V_{ds} plots. In the V_{dg} vs V_{gs} plot both the initial and walk-out curves are continuously increasing in the sub-threshold region ($V_{gs} < -8V$) until the max gate voltage tested ($V_{gs} = -12V$). This indicates a properly working gate diode and that breakdown is limited by V_{ds} breakdown. Diode degradation is evident by the drop in V_{dg} breakdown voltage from $150V$ after walk-out to $110V$ after walk-in. Also, V_{dg} does not exhibit the same increasing trend as was present in the initial and walk-in curves for $V_{gs} < -8V$. The region V shown in Figure 5.2 has vanished once stressed into walk-in, indicating the device breakdown voltage is now limited by V_{dg} breakdown.

The trends observed in both of the voltage plots are reinforced by the I_g vs V_{gs} plot also shown in Figure 5.5. From initial to walk-out the point at which the onset of gate current conduction begins is shifted more negative in V_{gs}. This correlates to the evidence that leakage current is reduced from drain to gate, and that breakdown voltage has increased as higher bias is needed to induce leakage current. A positive shift in V_{gs} is shown for the onset of gate leakage after walk-in has occurred, indicting lower bias is needed to induce gate conduction, which corresponds to a reduction in breakdown voltage. The value of V_{gs} required to reach the forced drain current during characterization follows the same trend. Another feature to note is the shape of the curves. Both the initial and walk-out curves show the classical "S-shape" as expected

during this type of test. The shape of the walk-in curve has been altered with stress with inflection points in the middle region of the curve ($-6V < V_{gs} < -2V$). One explanation of these inflection points is that damage to the gate diode is localized within the gate periphery with variable amount of degradation at each localized defect site. This would then lead to device behavior where sections of the FET gate finger has locally more negative values of V_{th} leading to soft pinch-off and requiring more negative value of V_{gs} to turn off.

This analysis shows that the breakdown characteristics have been altered when the device was stressed to walk-in. First, the voltage limiting mechanism that was previously observed in region V has shifted from limited by channel breakdown V_{ds} to the gate diode breakdown of V_{dg}. This essentially eliminates the region V and merges it with the observed region IV. Second, it was shown that the gate leakage current shape during the transition from ON-state to OFF-state has been altered. After stress the curve shape suggests that multiple localized threshold voltages now exists within the gate periphery as regions of the FET are turning OFF at varying values of V_{gs}. This indicated that damage to the gate diode with stress is varying along the gate fingers and is localized rather than uniformly distributed.

5.2.2 Gate Diode Characterization

Several key observations may be made from the two terminal diode characterization. A plot of the gate diode sweep with varying temperature is shown in Figure 5.7. While little change occurs to both the forward and reverse diode properties from the initial to the walk-out state, notable changes occur to the diode properties from the walk-out to the walk-in state. First, in the forward direction the general shape of the diode curve has changed indicating a shift in ideality factor and effective barrier height. Second, in the reverse bias section of the curve, initially the leakage current was very low, on the order of nA/mm. After stressed to the walk-in state, leakage current increases orders of magnitude with negative bias to the range of $\mu A/mm$.

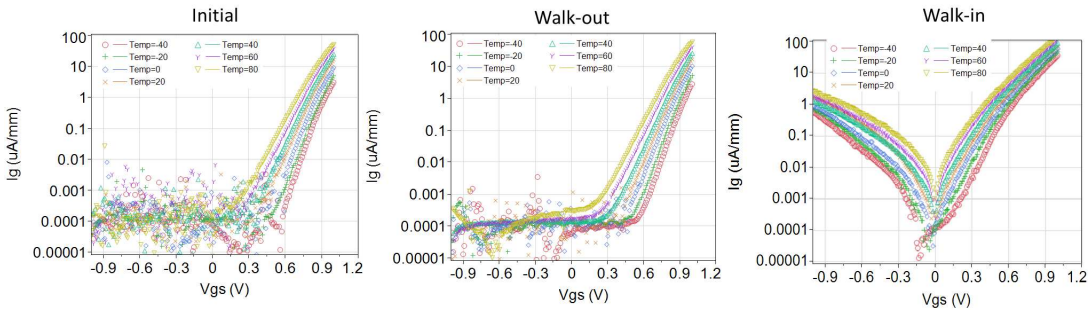

Figure 5.7: Gate diode characterization with temperature shown at initial, walk-out, and walk-in. The plots of diode characterization shows that after walk-in has occurred both the forward and reverse properties of the gate diode are changed. In the forward direction the slope of the I_g vs V_{gs} curve has changed indicating a change in ideality and barrier height. In the reverse bias case leakage current has increased 5 orders of magnitude and has a temperature dependence as the properties more closely resemble a resistor rather than diode.

To quantify the changes observed in the reverse diode characteristics, an attempt was made to fit the reverse leakage to an established reverse Schottky diode leakage model. The work presented by Zhang et. al. was used as a reference [58]. The reverse diode leakage in this study has a temperature dependence which implies the leakage mechanism is not due to a quantum mechanical tunneling mechanism as shown by the Fowler-Nordheim model. Instead the temperature dependence would imply a trap-assisted tunneling mechanism such Poole-Frenkel model given by the following equation.

$$J = CE_bEXP\frac{-q(\phi_t - \sqrt{qE_b/\pi\epsilon_0\epsilon_s})}{kT} \tag{5.1}$$

The reverse diode leakage characteristics shown in Figure 5.7, did not fit the Poole-Frenkel model. This result does not rule out a trap assisted tunneling mechanism as the Poole-Frenkel model assumes uniform leakage along the entire gate diode area. One explanation is that the observed leakage current is confined to localized areas along the gate finger. Therefore the leakage current at the localized defects may still be attributed to trap assisted tunneling mechanisms.

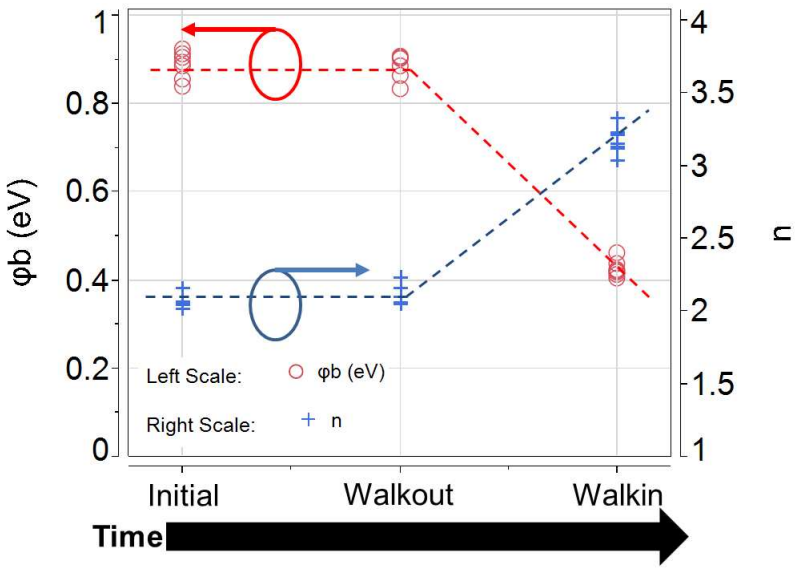

Figure 5.8: Ideality factor and Schottky barrier height from two terminal diode characterization over temperature with respect to device degradation state. The dotted lines are visual guides only. No change is observed from the initial to walk-out state. However, after walk-in diode properties are quantitatively shown to degrade significantly.

To quantify the changes to the diode in the forward direction both the ideality factor and the barrier height, were extracted from the data at each stress and temperature point. The ideality factor of a Schottky diode is given by the following equation.

$$n = \frac{q}{kT}\left(\frac{\partial V_G}{\partial \ln I_G}\right) \tag{5.2}$$

The barrier height of the Schottky diode was calculated using the following equation.

$$\phi_b = \frac{q}{kT} * \ln \frac{AA^*T^2}{I_0} \tag{5.3}$$

A plot of the effective ideality factor and barrier height versus degradation stage is shown in Figure 5.8. Since we propose the post stress gate leakage is not uniform along the gate periphery, this data is meant only to illustrate the average characteristics of

the gate diode at each stage of degradation. In this figure only the data from one device is shown, the multiple points at each stage are from the seven temperature points taken at each step ($-40°C$ to $80°C$ in $20°C$ steps).

The data shows minimal change to the diode properties from initial state to the walk-out state. However, the diode properties are significantly degraded from the walk-out stage to the walk-in stage. At room temperature the ideality of the diode has degraded from 2.07 to 3.21 while the barrier height has lowered from 0.892 eV to 0.424 eV. The variance of the diode properties with temperature show minimal change with degradation. During initial characterization, the ideality of the diode varied by 0.14 and barrier height by 0.07 eV over temperature. At the walk-in stage the range was 0.29 and 0.05 eV for both the ideality and barrier height respectively.

In this section it was shown that the degradation of the Schottky gate diode is responsible for the observed walk-in phenomena. When the gate diode is reversed biased the leakage current increased and had a strong temperature dependence, suggesting a trap assisted tunneling mechanism. The forward bias properties of the diode were quantitatively shown to have degraded when stressed to the walk-in state.

5.3 Optical Analysis

5.3.1 Electroluminescence

Electroluminescence (EL) is one method utilized to identify an area of interest along the periphery of a device. This is done by reverse biasing the device and searching for light emission (near-IR and/or visible) along the gate finger, as shown in Figure 5.9. Several publications have reported localized EL emission detected on devices stressed in the OFF state and report a correlation of real time increases in leakage current during stress with the formation of local EL sites [70] [90] [112] [113] [102]. However, attempts to uncover physical evidence of crystallographic deformation at these emission sites has had limited success [114] [115]. The only crystal defect mentioned is the formation of surface pits described in Bajo et. al. [102]. It has been

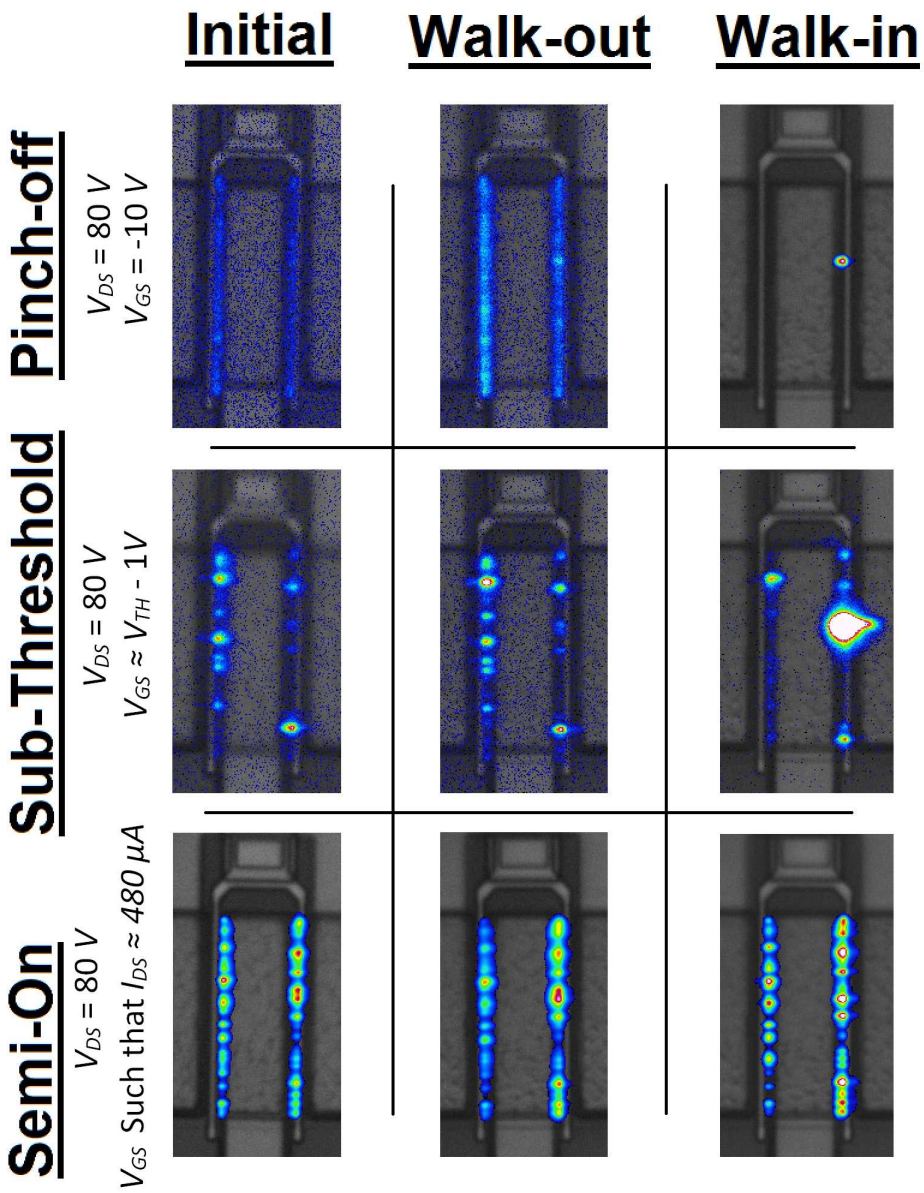

Figure 5.9: (EL) mapping of a representative device in this study with each column corresponding to a stage of stress after which the device was characterized. Each row corresponds to a different bias conditions. (Top) EL map of the device in the full OFF-state, $V_{gs} = -10V$ and $V_{ds} = 80V$ (Middle) Sub-threshold with $V_{gs} = -4.45V$ and $V_{ds} = 80V$ (Bottom) Semi-on with $V_{gs} = -3.7V$ and $V_{ds} = 80V$. Brightness scales are arbitrary. EL is shown to be present at random localized sites in the ON-state but the emission vanishes once biased into the OFF-state. After walk-in a dominant EL emission site with high intensity is apparent and persists in the OFF-state. This behavior has been reported in literature [102] [112] [113] and hypothesized to be the local point along the gate finger that has degraded with stress.

proposed by Marcon et. al. [114] that a leakage path is formed via percolation paths through the AlGaN barrier layer that are not physically observable.

In this study all six devices were characterized by EL in the walk-in state. Four of the devices were characterized at both walk-out and walk-in. Finally two of the devices were characterized at all three stages of initial, walk-out, and walk-in. The general behavior was consistent in all devices. Figure 5.9 shows the evolution of the EL across all three stages from one of the representative devices that had EL mapping collected at each stage.

The bias conditions in Figure 5.9 are full OFF-state ($V_{gs} = -10V$ and $V_{ds} = 80V$), sub-threshold ($V_{gs} = V_{th} - 1V = -4.45V$ and $V_{ds} = 80V$), and semi-ON ($I_{ds} = 480uA$ and $V_{ds} = 80V$). All EL emission appears on the drain side edge of the gate finger. Both the initial and walk-out EL characterizations look similar. In the semi-ON bias conditions EL may be observed, with varying degrees of intensity, along the entire gate finger. In the sub-threshold condition much of the light along the gate finger is extinguished but some EL emission sites persist which may indicate local variations of threshold voltage along the gate finger. After V_{gs} is biased well below V_{th} all localized EL emissions sites are very low in intensity prior to walk-in.

In comparing the EL emission from initial and walk-out to walk-in, some changes are observable in the device. Clear evidence of change is difficult to distinguish in the semi-on state but a very bright EL emission site is visible in the sub-threshold and deep pinch-off towards the center of the right side gate finger in Figure 5.9. In the sub-threshold condition the sparse EL emission is still present as was observed in the previous stages but now a dominant EL site is clearly present. The dominant EL site persists when the device is biased completely off after walk-in was observed.

Study of EL over a range of device states of operation is necessary to evaluate and understand localized emission along the gate finger, because in our study what will eventually become the dominant EL emission site is not observable at all bias

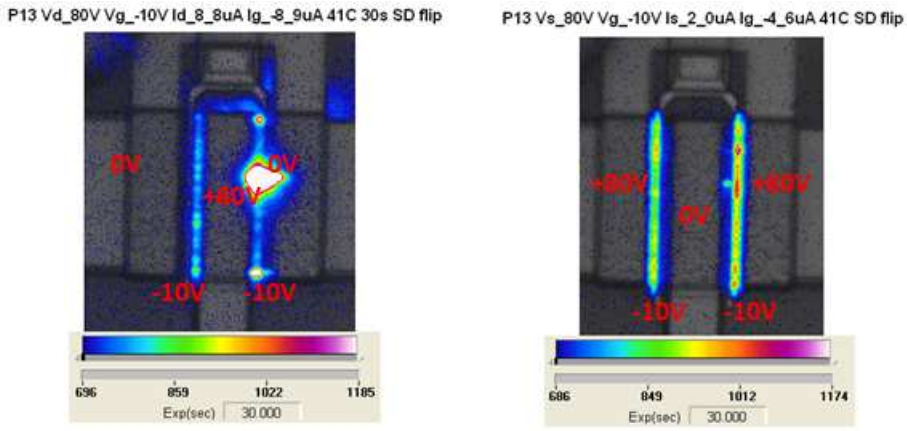

Figure 5.10: (a) EL images of the same device shown in Figure 5.9 in the walk-in state at pinch-off. (Left) Device is biased with $V_{gs} = -10V$ and $V_{ds} = 80V$ showing the same dominant emission site as was observed in Figure 5.9. (Right) Drain and source bias is reversed ($V_{gs} = -10V$ and $V_{sd} = 80V$). Sensitivity is increased in this image so that weak EL emission is observed along the gate finger. Dominant EL emission site is clearly visible in the left image but after reversing the source and drain bias emission is difficult to detect at the dominant EL emission site. This indicates that the damage to the gate diode after walk-in occurs on the drain edge of the contact and is not easily observed when biasing the device from the source side. The same arbitrary brightness scale applies to both images. (b) EL images of the same device shown in Figure 10 in the walk-in state at a semi-on condition before and after reversing source and drain bias (composite image in center). It can be seen that some emission sites correlate indicating that the source of variation is present on both sides of the gate.

conditions prior to walk-in degradation. Instead, other localized emission sites exist that do not evolve into a significant leakage current path with stress. It is not clear at this time the exact relationship between eventual degradation with OFF-state stress and the presence of these sites. It is worthwhile to note that localized emission does not necessarily indicate that site is a damaged section of the gate diode.

As mentioned earlier, all of the EL emission observed was localized to the drain side of the gate finger. This is expected since during EL mapping the drain was biased to $80V$ with respect to the source. Figure 5.10 shows a comparison with the drain-source bias reversed on a device stressed to walk-in. In this study, the device channel is symmetric about the gate so the same fields are present in the channel, but on the

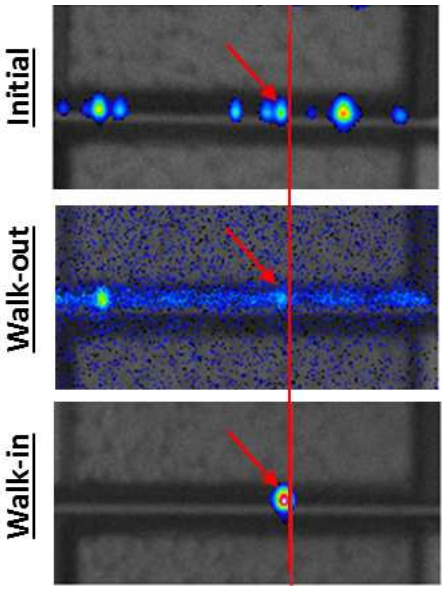

Figure 5.11: Zoom in of the EL images of the same device in Figure 5.9. It is shown that the location that eventually becomes the dominant emission site after walk-in is also present in the initial and walk-out images. However, the dominant emission site in walk-in is not the most intense emission in the initial and walk-out images. This suggests that localized emission sites observed prior to the application of stress may indicate localized areas of the gate finger that are preferential for degradation when stressed in the OFF-state.

opposite side of the gate finger when the source and drain bias is reversed. The image on the left side of Figure 5.10 is the same walk-in image, at pinch off bias in Figure 5.9 when the device was biased $V_{gs} = -10V$ and $V_{ds} = 80V$. The only change is that the sensitivity is increased to reveal lower levels of EL emission. The image on the right side of the figure is a comparison with the bias set to $V_{gs} = -10V$ and $V_{sd} = 80V$. With the drain-source voltage reversed the EL emission along the gate flips from the drain side of the gate finger to the source side as expected. The key observation made from this test is that once the bias is reversed the dominant EL emission location still has the highest intensity emission on the source side. This indicates that the damage to the gate diode may be observed on the source side of the gate finger, which is the opposite side of the gate finger that was stressed. Furthermore, this suggests that the leakage current path is through the AlGaN barrier and not across the semiconductor surface.

An effort is made in Figure 5.11 to understand the evolution of EL emission at the localized site within the gate periphery that transforms into the dominant EL emission site after walk-in. This figure shows that EL emission is present at what will eventually become the dominant EL emission spot at both the initial and walk-out characterization. This suggests that localized EL sites observed prior to stress may indicate areas of the gate finger that are preferential to degradation with OFF-state stress.

Cross sectional TEM images at the localized emission site of a device stressed to walk-in and a control unstressed part produced no clear evidence of a defect. The devices stressed to walk-in did not have surface cracking or pitting at the dominant EL emission site. Furthermore material defects at the emission site such as threading dislocations were not abnormal compared to the control site in both density and location of material defects with respect to the gate contact. No clear processing defects were evident in gate contact formation.

5.3.2 Thermal Infrared (IR)

While it is generally accepted that EL emission may be used to identify regions of high leakage current in the OFF-state there exists some critique in using this approach. The intensity of EL is affected by the following; the localized current, the efficiency of emission of photons of a suitable energy to be detectable of that local current (which can vary by orders of magnitude), and the efficiency with which light can reach the detector (peak emission is likely under the gate field plate). Furthermore, because GaN and SiC are optically transparent and can channel light to other locations, is it not obvious that EL emission implies locally high leakage current.

To confirm the localized EL emission site was the actual site of the increase in leakage current during walk-in, a thermal IR measurement ($\lambda = 2 - 5\mu m$) was made on the same device. IR measurements of devices biased into the OFF-state are challenging since the power dissipation necessary to achieve a measurable signal is difficult

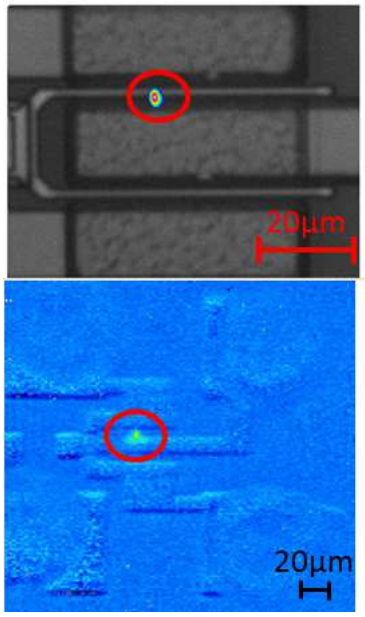

Figure 5.12: (Top) EL image of a device that has been stressed to walk-in with a localized emission site on the drain side of the top gate finger. (Bottom) Same device with a localized IR hotspot at the same location. Previously it has been shown in literature [102] [112] [113] that increased in electrically measured gate current occur simultaneously with appearance of localized EL. The comparison in this figure proves that the EL emission sites appear in the localized area of high gate leakage current.

to obtain. In the OFF-state very little current is conducted in the device, typically on the order of 10s of microamps for a degraded device. Also the max voltage of the device is limited by the breakdown which has degraded during the walk-in process. To generate a measurable IR result on this device, the test conditions were $V_{gs} = -10V$, $V_{ds} = 110V$, $P_{diss} = 3.84mW$, and $T_{base} = 41°C$. The observed thermal IR signature is shown at the bottom of Figure 5.12. Both the EL and IR emission sites are close enough to be considered the same location along the gate finger. This observation was confirmed for two other devices in the study.

5.4 Summary

In this chapter a follow up experiment to the constant OFF-state stress study presented in chapter 3 was detailed. The purpose of this experiment was to conduct a detailed electrical and optical analysis, with stress, to understand physical changes

in the device that occur during the walk-out and walk-in phases of stress. An emphasis was placed on walk-in as it represents the permanent degradation and eventual failure of the AlGaN/GaN HEMT.

In the electrical analysis it was clearly shown via multiple methods that gate diode degradation leads to observed failure. Using the drain current injection method it was demonstrated that prior to walk-in, device breakdown is ultimately limited by V_{ds}. After walk-in occurs, the limiting factor is V_{dg}, indicating the gate diode no longer can sustain high voltages and the channel limiting mechanism is no longer observable. Additionally, it was shown that the gate leakage current when transitioning the device to the OFF-state contains several inflection points that did not previously exist. These points indicate that localized damage along the gate finger has led to localized shifts in the threshold voltage. This implies that damage done via stress is localized within the gate periphery and not uniformly distributed. This result was further supported when analyzing the electrical data versus temperature. Prior to stress, it was shown that reverse diode leakage was very low and did not have a temperature dependence. After walk-in, the reverse bias leakage current increased several orders of magnitude and had a significant temperature dependence. This leads to the conclusion that the reverse leakage in the gate diode is related to trap assisted tunneling, via a trap state that has been generated in the AlGaN barrier layer during stress. Finally, a quantitative analysis of the gate diode properties shows a significant degradation in both ideality and barrier height after walk-in.

Optical analysis was performed on the AlGaN/GaN HEMTs, prior to stress and after the walk-out and walk-in conditions. First, it was discovered that localized emission along the gate finger is present when biased above threshold but this emission nearly vanished when the device was biased well below the threshold voltage prior to degradation. After the observed degradation in the walk-in state a localized EL emission site was revealed in the OFF-state that is consistent with prior literature

[70] [90] [112] [113] [102]. Second, reversing the bias of the drain and the source under OFF-state conditions produced EL emission at the dominant EL emission site. This shows that the leakage path was across the AlGaN barrier and not across the surface between the gate and drain contacts. Third, to the best of the author's knowledge, this is the first time it has been shown a localized EL emission site was present prior to stress, at the area of the gate finger that would eventually evolve into the dominant EL site after permanent degradation. This indicates that localized areas along the gate finger may be preferential to degradation as processed. Fourth, for the first time it was confirmed that the localized EL emission observed in the OFF-state after degradation corresponds to the region of the gate finger that is the source of reverse leakage current via IR imaging.

Cross sectional images of the devices at the dominant EL emission site did not produce any obvious defects when compared to control cross sections on an unstressed device. There was no evidence of surface cracking or pitting as observed in literature attributing failure to the inverse piezoelectric effect. No material or processing defects were obvious in the cross section images when comparing stressed devices to each other and to a control unstressed device. The absence of a physically observable defect suggests that the failure mechanism is related to time dependent dielectric breakdown and formation of percolation paths as was suggested by Marcon et al. [114]. In summary, these observations together with the method of stress testing described in this work, suggests a methodology for identifying and understanding the failure mechanisms that limit the SOA of GaN HEMTs.

CHAPTER 6: REVIEW AND CONCLUSIONS

AlGaN/GaN HEMTs have made major strides in recent years towards achieving widespread adoption in a variety of high power and high frequency applications. A complete understanding of failure mechanisms that limit the safe operating area of GaN devices provides the means of unlocking additional capability of GaN technology needed for many emergent applications of GaN devices in power electronics and RF switches, in addition to the RF power amplifiers. This study sought to answer what are the consequences to device performance and lifetime when operated close the breakdown voltage and what failure modes lead to the observed degradation.

This dissertation began with a review of AlGaN/GaN HEMTs and explained how the technology is optimally suited for future generations of high power and frequency devices via unique material properties. These properties enable semiconductor devices to sustain high electric fields, while providing high current density, and allowing for high speed operation.

A review of AlGaN/GaN HEMT reliability publications and methods was presented. Conventionally, reliability studies are conducted using a three temperature accelerated lifetime test and applying the results to Arrhenius law to extract a mean time to failure. This method assumes that the failure mechanism for AlGaN/GaN HEMTs is driven only by a temperature acceleration factor. In recent years it has been proposed that an electric field driven failure mechanism also exists for this technology. The prevalent theory in literature is based on the inverse piezoelectric effect. This theory states that once the stored elastic energy in the AlGaN barrier layer exceeds a critical value the material will relax, forming a macroscopic defect in the

crystal. Since the AlGaN barrier is piezoelectrically strained, this elastic energy may be increased via an applied electric field. This gives rise to a critical voltage, that when exceeded leads to the material relaxation. More recently alternatives have been proposed that suggest the failure is not instantaneous but instead time dependent, similar to dielectric breakdown observed in silicon MOS devices.

One reason for so many varying reports of failure mechanisms could be related to levels of quality for the various processes from which the devices studied were fabricated. In this work, AlGaN/GaN HEMT devices were fabricated in a commercial GaN process, notable for industry leading qualified 65 V operation of RF power amplifiers. These devices were stressed according to the methods described in the inverse piezoelectric literature. The results found that no critical voltage could be uncovered for these devices up to the breakdown voltage. Furthermore, short term constant voltage stress on similar time scales reported in literature could no produce the observed device degradation.

This observation led to the development of a unique stress method that allowed for the HEMTs in this study to be stressed within 5 V of breakdown to understand the safe operating limits of devices in this technology. By stressing the device in such a manner it was discovered that two distinct electrical observations may be made with stress. First, was that the device undergoes breakdown voltage walk-out, immediately after the application of OFF-state stress, during which the leakage current in the device is reduced and the breakdown voltage is enhanced. This was found to be a recoverable change, as the leakage would return if the device was allowed to idle without stress. This suggested the physical mechanism to be related to carrier trapping and parametric shifts measure were consistent with this hypothesis.

The second and most interesting electrical observation was breakdown voltage walk-in. This occurred after several hours of stress and may be described as in increase in leakage current and reduction in breakdown voltage. This degradation was found to

be permanent and was noted as the electrical failure mode when stressing these devices beyond the safe operating limits. Initial analysis into this phenomena found that it was unrelated to the inverse piezoelectric effect for three reasons. First the electrical degradation in the ON-state was not as extensive (>10%) for ON-state parameters such as R_{on}, I_{dss}, I_{dmax} as was reported in previous IPE literature. Second, FIB cuts at localized electroluminescence emission sites and subsequent STEM did not reveal the presence of macroscopic crystal defects such as cracks or pits in the AlGaN barrier layer. Third, a device simulation of electric field profile in the channel during stress was performed. From this it was possible to calculate the peak stored elastic energy in the AlGaN barrier layer for these devices, along with the critical elastic field. This analysis revealed that the critical elastic energy for this heterostructure was not exceeded during stress and therefore confirms the degradation was not due to IPE.

In order to better understand the observed failure mode of breakdown voltage walk-in a final experiment was performed to electrically and optically characterize the device prior to stress, after walk-out, and finally after walk-in. The electrical analysis shows conclusively that the degradation is related to failure of Schottky gate diode, via four key observations.

First, the device was fully characterized via the drain current injection mechanism, previously shown in literature to be a powerful measurement for providing physical insight into how GaAs based FETs are limited under high electric field conditions. It was shown that prior to degradation the breakdown of the device is limited by V_{ds}, implying a limitation due to the device channel or buffer breakdown. After stressed to walk-in the breakdown voltage was limited by V_{dg}, which suggests a failure of the gate diode to sustain the applied voltage in the OFF-state.

Second, by analyzing the gate current during the drain current injection method, it was shown that during the transition from the ON-state to OFF-state the turn

off characteristics of the diode were significantly impacted. Prior to walk-in the gate leakage curve displayed the classic "S-shape" consistent with reverse leakage of diode with a uniform threshold voltage along the entire gate periphery. After walk-in the curve shape was significantly impacted such that the leakage began to increase at much lower bias along with the presence of several inflection points. These inflection points represent localized shifts in the threshold voltage within the gate periphery of the device. These shifts suggest localized degradation of the gate diode where the Schottky properties were altered such that the gate is no longer behaving as an ideal diode.

Third, over temperature characterization of the gate diode revealed that prior to walk-in the reverse gate diode leakage current did not have a temperature dependence. After walk-in had occurred the reverse leakage current increased three orders of magnitude and had a strong temperature dependence. This was consistent with a trap assisted tunneling mechanism, such as Poole-Frenkel conduction mechanism.

Fourth, an quantitative analysis of the gate diode data revealed that after walk-in, diode characteristics were greatly degraded. Both ideality and barrier height of the diode was extracted from the measured data. This confirmed that both the overall barrier height of the diode and ideality significantly degraded after walk-in.

The optical analysis provided several key insights to the observed device degradation. First, it was shown that localized EL emission was present in the device channel in the semi-ON and subthreshold bias states that could be completely extinguished in the OFF-state prior to stress and after walk-out. After walk-in had occurred, localized EL emission was observed in the OFF-state along the drain side of the gate finger and shows the degradation is consistent with recent literature. EL emission was also collected at alternate bias conditions not previously shown in literature to understand how the EL changes with device operation. It was shown that localized EL emission is also present in the semi-On and ON-states. This localized emission

was also present prior to stress, suggesting that EL does not necessarily represent a damaged region of the gate finger. The localized dominant EL site observed after walk-in supports the electrical evidence that the degradation occurred to the gate diode and was localized within the gate periphery of the FET.

Second, an experiment conducted by reversing the drain and source bias in the OFF-state produced high intensity localized EL emission at the dominant EL site on the source side of the gate finger. This suggests that the leakage current path is across the AlGaN barrier and not the surface of the semiconductor. Third, by analyzing the EL emission observed prior to walk-in it was demonstrated that EL emission could be observed at the site that would eventually produce the dominant EL emission after walk-in. This suggests the possibility that certain areas along the gate finger are preferential for degradation prior to stress.

Fourth, thermal IR measurements were collected on a device biased deep in to pinch off to confirm if the EL emission site was consistent with the region of localized increase in leakage current. It was shown that the IR and dominant EL emission site are close enough to be considered the same spot. Indicating that EL emission is a reasonable proxy for determining the area of the gate diode that has degraded and is responsible for the increased leakage current.

In conclusion, the failure mode of the AlGaN/GaN HEMTs in this study was not due to the inverse piezoelectric effect that has been widely reported in OFF-state reliability literature. The observed Schottky diode degradation and the absence of visible crystal defects are consistant with recent publications [99] [114] that theorize the failure mechanism in GaN devices is similar to time dependent dielectric breakdown, as is well understood in silicon MOSFET technology. The degradation is linked to the formation of percolation paths in high electric fields regions, near the gate edge, generate leakage paths across the AlGaN barrier layer. Further work would need to be conducted to confirm this is in fact the physical failure mechanism of this process.

The work presented in this dissertation provides the means of thoroughly characterizing an AlGaN/GaN process, up to the breakdown voltage, to determine the failure modes. As was discussed in chapter 3, a wide array of failure modes and mechanisms have been reported in literature. Only through the careful experimentation and analysis can the limitations of a particular process be understood.

6.0.1 Future Work

While this study detailed a comprehensive stress and analysis of AlGaN/GaN HEMTs operated to the process breakdown limits there exists additional work that could provide further insight. With a fixed fabrication process, it would be of interest to explore various material and layout permutations to understand the impacts on electric-field degradation. As an example, on the material side it would be useful to confirm if the failure remains constant when varying Al% in the AlGaN barrier layer, as this has been know to affect material strain. Also what is the impact to recently reported interlayers at the AlGaN/GaN interface such as AlN and the impact on the formation of percolation paths. As for layout, the devices in this study did not have a source connected field plate, but understanding the reliability impact would be of interest, as this would distribute the electric field profile more uniformly within the device channel.

It was shown in chapter 5 that local EL emission was discovered to be present prior to walk-in in an unstressed device at what would form into the dominant EL site. Study of the cross sections at these degradation sites did not produce compelling evidence of a material or process defect when compared to control site and devices. A careful study to analyze the material and processing factors that lead to EL when the device is biased just below threshold may produce the factors that lead to this observation. The results suggest that if these factors may be corrected and therefore suppress sub-threshold EL perhaps the damage seen by walk-in may be delayed or greatly reduced and there improve OFF-state reliability.

At the conclusion of chapter 4 an abbreviated study in varying the stress voltage to understand the safe operating voltages was shown in Figure 4.14. With more devices and resources to stress several parts simultaneously, it would be possible to generate lifetime statistics versus operational voltage relative to the device breakdown. From this data it would be possible to see if the failures in this study fit a Weibull distribution, as shown in [99] [114] that would confirm if the failure mechanism follow the time dependent dielectric breakdown model. Perhaps with careful analysis it may be discovered that a unique electric field accelerated lifetime model does exist for GaN devices. Such a model would be very powerful in advancing alternate lifetime acceleration factors and allow a more thorough characterization of device lifetimes.

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