ACTIVE AND REACTIVE POWER COMPENSATOR USING WIDE BAND GAP SEMICONDUCTORS FOR VOLTAGE SUPPORT IN LOW VOLTAGE NETWORKS

by

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ABSTRACT

RAKESH KUMAR BELCHANDAN. Active and reactive power compensator using wide band gap semiconductors for voltage support in low voltage networks. (Under the direction of DR. MADHAV MANJREKAR)

The purpose of this research is to develop and demonstrate a solution for voltage support at the low voltage distribution networks using wide band gap semiconductor devices. The distribution networks need just the active power or reactive power or the combination of both for voltage support depending on the load conditions. Conventional equipments operating at mid-voltage levels such as static VAR compensator (SVC) and static synchronous compensators (STATCOM) are incapable to foresee and respond to the problem aroused at low voltage levels. Moreover, they are only capable of generating reactive power but at the distribution levels, with smaller X/R ratios, active power plays a major role for voltage stability.

To keep the distribution level voltage within limits, voltage regulators are used traditionally to keep the voltage constant at the consumer ends but they have their operational limitations and require maintenance after certain number of operations. So, in this thesis, effort has been made towards an inexpensive and reliable system that can be employed in the house-holds and power exchange can take place at the local point-of-common-coupling. Employment of such micro-system in large numbers at the distribution level will drastically reduce the transmission requirements.

The proposed solution deals with the development of low voltage grid-tied inverters with active and reactive power controls for fine-tuned voltage control. The integrated system developed has the photo-voltaic and battery energy storage system for power generation and storage. The effectiveness of this solution has been demonstrated using simulation and experimental results. The hardware setup has been designed to handle the power level upto 10 kW.

DEDICATION

I would like to take a moment to express the gratitude to the Supreme Lord for giving me the courage, inspiration and wisdom to execute every single thing in my life.

I dedicate this thesis to my parents who encouraged me to pursue higher studies and to my elder sister whose support was a pillar of strength throughout my academic goals.

ACKNOWLEDGEMENTS

I would first like to thank my academic advisor Dr. Madhav Manjrekar of University of North Carolina at Charlotte. His support and encouragement at every step in the thesis were phenomenal. His constant encouragement to make me try new things by explaining their importance and doing things out of my comfort zone were the seeds of my involvement in this work. He was always there to help whenever I ran into trouble spot and gave me valuable suggestions. He increased my curiosity and breadth of knowledge in all aspects of academia. He constantly allowed me to work independently but always steered me in the right direction.

I would also like to thank Dr. Velentina Cecchi and Dr. Tiefu Zhao for their invaluable suggestion during the research and preparation of thesis document.

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LIST OF ABBREVIATIONS

AC Alternating Current.

BESS Battery Energy Storage System.

CMOS Complementary Metal-Oxide Semiconductor

DC Direct Current.

DER Distributed Energy Resources.

ECE An acronym for Electrical and Computer Engineering.

EMI Electro-magnetic Interference

IC Integrated Circuit

MPPT Maximum Power Point Tracking

PCB Printed Circuit Board

PLL Phase Locked Loop

PV Photo-voltaic.

PWM Pulse Width Modulation.

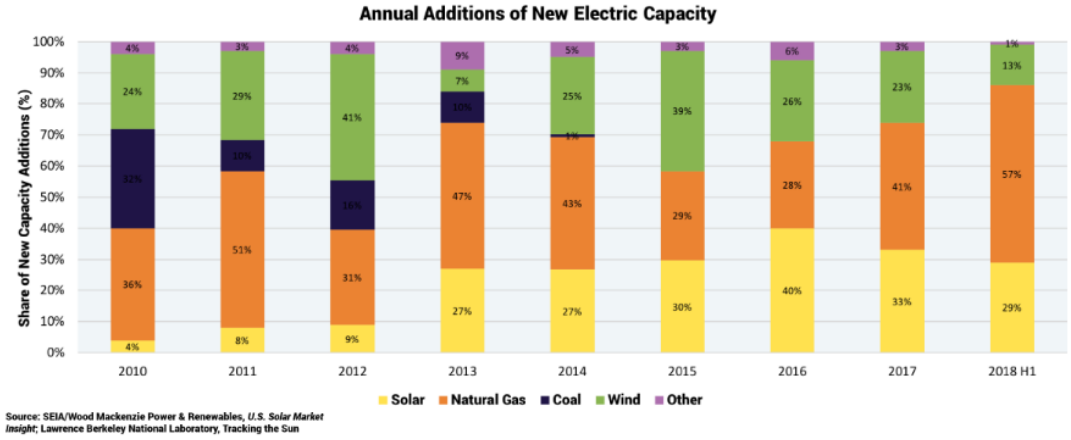
STATCOM Static Synchronous Compensator.

SVC Static VAR Compensators.

CHAPTER 1: INTRODUCTION

1.1 Photovoltaic Growth In Recent Years

The demand for energy is increasing but the rate of growth for the conventional energy sources based power generation is decreasing. Installed capacity is increasing but there is not much interest towards installing the conventional generating stations. There is a paradigm shift in the mode of power generation in the recent past. According to a statistics by Solar Energy Industries Association[1], in the recent capacity additions, solar and natural gas have the highest share. Figure 1.1 shows the individual shares in generation capacity for different modes of generation.

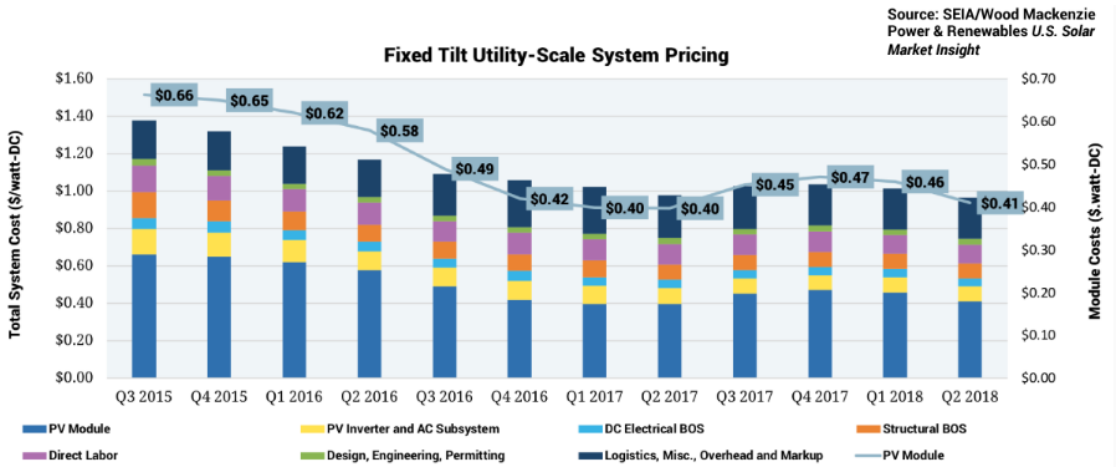


(a) Generation capacity addition in recent past

Figure 1.1: Generation capacity addition in recent past

Solar's increasing competitiveness compared to other technologies has allowed it to quickly increase its share of total U.S. electrical generation from just 0.1% in 2010 to over 2% today. This competitive increment is because there is a decreasing trend in solar installation cost in past decades. Another Figure 1.2 by Solar Energy Industries

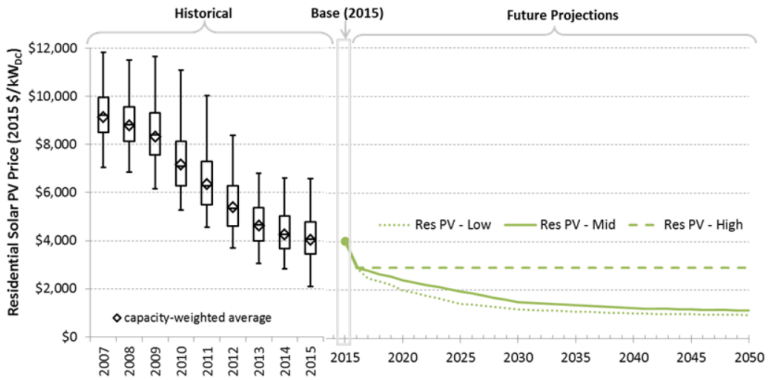
Association shows the trend of per watt pricing of solar installations over the years. The slight increase in few quarters of 2017 is due to import duty imposed by U.S. government on the panels and accessories. In the recent past, there is a fall in price due to steep reductions in Chinese demand. Below figure shows the utility scale price drop over the years.



(a) Solar installation cost per watt over different quarters

Figure 1.2: Solar installation cost per watt over different quarters

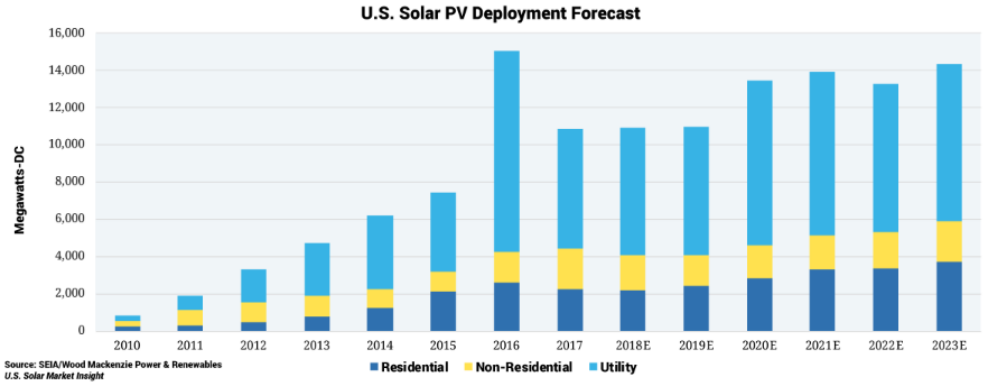
According to National Renewable Energy Laboratory[2], the residential photovoltaic demand is on rise and the prices are going down each passing year. It is estimated that the prices will be going down further in coming years. NREL has estimated price based on capital expenditure and operation and maintenance data. The high, mid and low PV data are based on no change in PV capacity factor over the years and mean and low bound of the capital expenditure and operation and maintenance costs respectively. The figure below shows the estimated variation of price in the future.



(a) Estimated residential photovoltaic cost

Figure 1.3: Estimated residential photovoltaic cost based on capital expenditure and operation and maintenance data

There is an steady pace of growth estimated in 2018 in residential, non-residential and utility photovoltaic installations. Incremental growth is expected to return in 2019. It is estimated that there will be over 100 GW of solar installation by 2021 according to Solar Energy Industries Association.



(a) Residential nonresidential and utility photovoltaic installations

Figure 1.4: Past and estimated residential nonresidential and utility photovoltaic installations

All the aforementioned factors are assisting the growth of photovoltaic installations in the market and the residential installations are at all time high and it is expected to grow further in future.

As the above statistics shows the increasing trend towards the residential photo-

voltaic installments, there are multiple challenges related to DERs in distribution systems which needs to be resolved for stable system operation. These challenges will be discussed later in this chapter.

1.2 Issues Related to Electrical Distribution System With Increasing Distributed Energy Resources

Distribution lines are normally short lines which ranges anywhere below 50 miles. In these lines line resistance are more dominant than the line reactance because of lesser lengths. So, X/R ratio is smaller than medium or high voltage lines. That is why it has significant voltage drop problems. According to NEC code 110-3b, which defines the equipment installation and connection guidelines, the voltage variation can be anywhere between 3 to 5% depending on the systems. There are many challenges related to the electrical distribution system which is discussed below.

- *Voltage variation*: Voltage drop is one of the important issues related to the distribution lines. The voltage drop limits must be maintained in order to keep the current drawn by the electrical equipment within reasonable limits. To keep the voltage within these limits, voltage regulators are used. But these voltage regulators have their operational limits because of arc generation while raising and lowering the taps. These regulators require maintenance from time to time.
- *Voltage swell and voltage sag*: Due to any electrical fault in the distribution system or any large induction motor start and stop can lead to voltage swell and sag. They exist for a shorter period of time most of the time during transients but it can lead to power system instability in cases where voltage is not restored within short period of time. In the medium voltage lines, these situations are handled by SVCs and STATCOMs by feeding or sinking the required reactive power. But in distribution lines the loads may be resistive such as heaters and irons. So, just feeding reactive power is not adequate to maintain the voltage levels.

- *Voltage imbalance*: Voltage imbalance is caused by unbalance load or dissimilar voltage drop in three phases. Voltage imbalance produces negative sequence currents in the system and the electrical system will have more losses. The negative sequence current produces a negative sequence torque in rotating machines which opposes the normal mechanical torque due to positive sequence currents. These negative sequence currents heats the machine windings, hence the losses are increased.
- *Harmonic distortion*: With the increasing penetration of DERs in the distribution system at low voltage levels, harmonic injection into the grid is a prevailing issue. The power electronics based power processing equipments such as inverters are the main source of harmonic distortion. Also, switching power supplies, rectifiers and UPS used in residential building adds to this problem. These harmonic injection causes the line conductors to overheat due to skin effect which becomes significant for harmonics above 7^{th} order. These harmonics also causes overheating of transformers and motors.

These aforementioned challenges are very significant in the distribution systems and the research presented here will be helpful to address these issues. If the above challenges are out of the limits, then can turn into loss of stability and consequently can lead to loss of synchronism.

In the later sections, we will show how the equivalent X/R ratio changes the compensation requirements to maintain the voltage levels.

1.3 Watt-Var Compensation

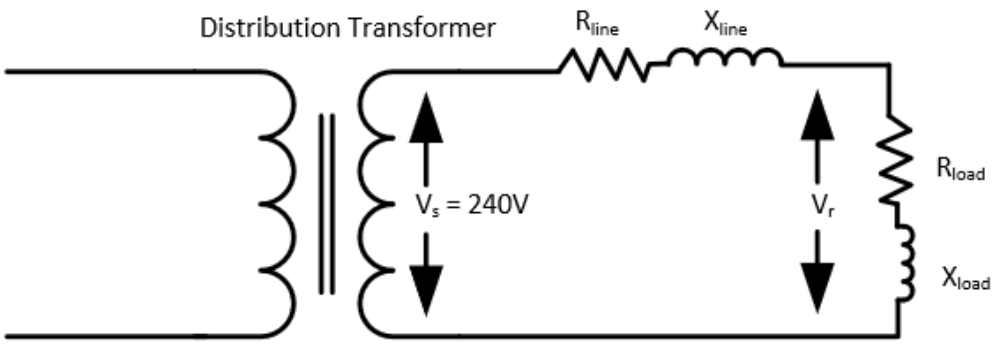
As discussed in previous sections, Voltage instability at the distribution level is one of the major problems at the leaf end of the power system. Conventionally, the voltage drop in the transmission lines is being compensated by the generation of reactive current by using SVCs and STATCOMs. They work very well at the transmission or mid-voltage level since the X/R ratio of the transmission line is dominated by

reactance value. They are built with more focus on reactive current generation capability. Also, they perform fine-tuned voltage regulation and facilitate faster response than the mechanical voltage regulators. At the distribution level the same equipment will not be very useful because the X/R ratio varies largely and mere generation of reactive current is not adequate to maintain the voltage stability. Moreover, with increasing DERs penetration in recent times, there is limited response and capability to foresee the problem which arises at the distribution level from the transmission level by these semiconductor based voltage regulators.

To illustrate, let us suppose we have a system as shown in the figure below. The 240V AC source represents output at the secondary of the distribution transformer and then the power is being transmitted to the loads. The transmission level X/R ratio is fixed whereas the X/R ratio of the load is varying according to the varying load conditions.

In the first case, there is no compensation provided and the voltage at the receiving end is lesser than the sending end due to drop in distribution lines. The maximum allowed disruption at the receiving end voltage is $\pm 5\%$ of rated 240V. There are four cases shown below. First is the receiving end voltage without any compensation, second one with active compensation, third with reactive compensation and last one with active and reactive compensation.

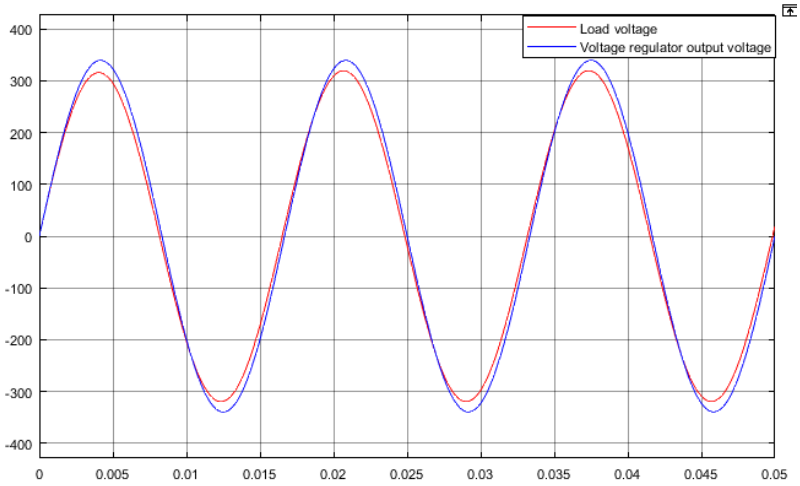
When there is no compensation provided, there is voltage drop in the distribution lines and the receiving end voltage is always less than the sending end voltage. If this variation lies within 5% then it is within limits but with more junctions and branches at the distribution level, it might go below this value.



(a) Uncompensated distribution system

Figure 1.5: Uncompensated distribution system

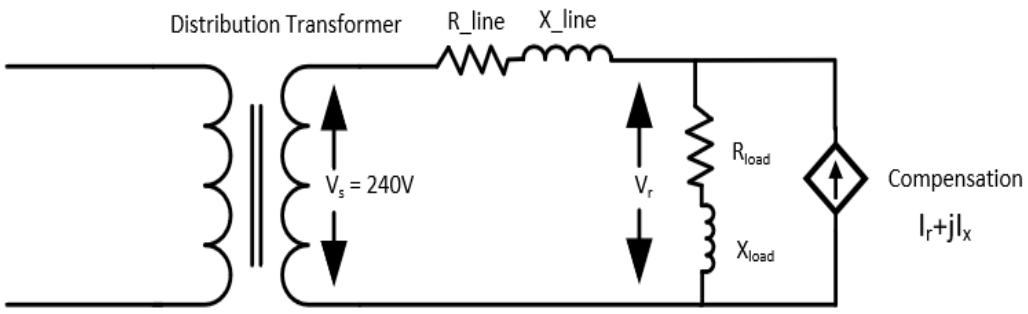
It can be seen here that the receiving end voltage is always lesser than sending end voltage.



(a) Voltage at the sending end and receiving end in the uncompensated distribution system

Figure 1.6: V_s and V_r in uncompensated system

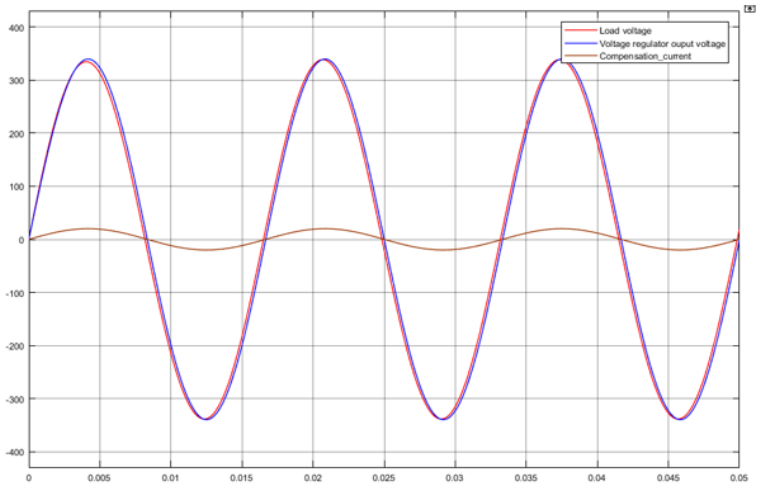
Now, let us see a system, with the capability of active and passive compensation.



(a) Compensated distribution system

Figure 1.7: A distribution system with Watt-VAR compensation

With a system where R_{load} is more dominant than X_{load},

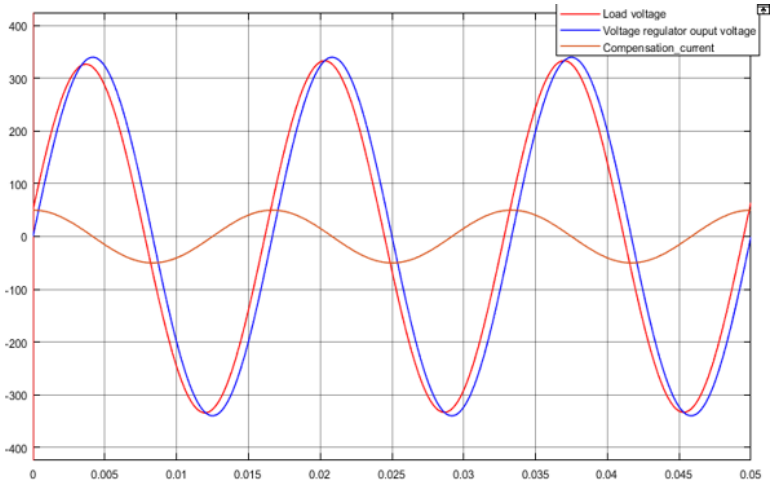


(a) Voltage at the sending end and receiving end with active compensation for dominant R load

Figure 1.8: V_s and V_r in a distribution system with Watt compensation

In this situation, the compensated power is only active power for a resistance dominant load. Active power impacts the voltage level more as compared to the reactive power. After the active compensation the system is able to maintain the voltage level at the load.

With a system where X_{load} is more dominant than R_{load},

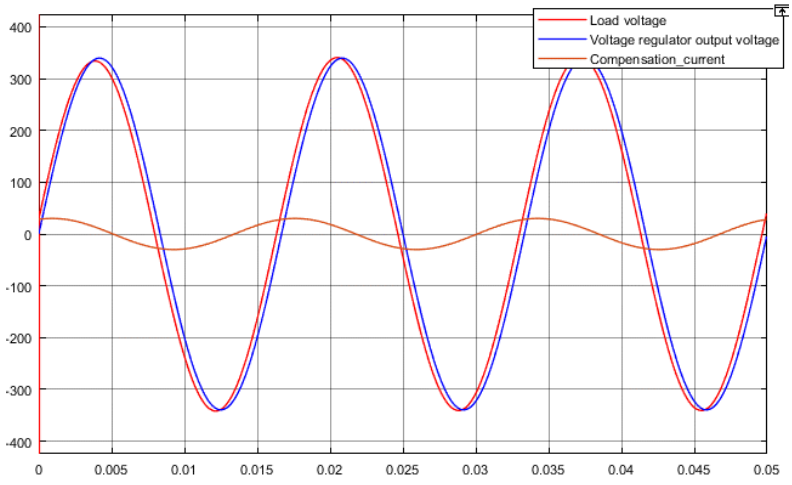


(a) Voltage at the sending end and receiving end with reactive compensation for dominant X load

Figure 1.9: V_s and V_r in a distribution system with VAR compensation

In this scenario, the compensated power is only reactive power for a reactance dominant load. Reactive power impacts the voltage level more as compared to the active power. After the reactive compensation the system is able to maintain the voltage level at the load.

With a system where X_{load} and R_{load} both are dominant



(a) Voltage at the sending end and receiving end with both active and reactive compensation

Figure 1.10: V_s and V_r in a distribution system with Watt-VAR compensation

In this scenario, the compensated power is both active power and reactive power. Both active and reactive power impacts the voltage level to equal effect. After the combined compensation the system is able to maintain the voltage level at the load.

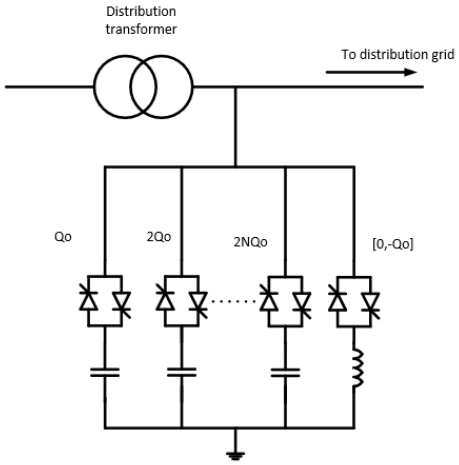
In this way, we can see that for maintaining a fixed voltage at the distribution level requires the compensation of both active and reactive component at times depending on the varying load conditions.

1.4 Literature Review

It is well established practice to use reactive power compensation to increase the transmittable power in AC power systems. Fixed capacitors such as capacitor banks or mechanically-switched capacitors and reactors have long been employed to increase the steady-state power transmission by controlling the voltage profile along the lines. Solutions such as STATCOMs and SVCs exists at the medium voltage levels[3]. These devices are faster than the mechanically switched voltage regulators such as line tap changers[4]. Moreover, they are bulky and active control of grid voltage harmonics is not possible[5]. All of these equipments have a common characteristics in that the necessary reactive power required for the compensation is generated or absorbed by traditional capacitor or reactor banks and the thyristor switches are used only for the control of combined reactive impedance these banks present to the system during successive periods of applied voltage. Consequently, conventional thyristor controlled compensators present a variable admittance to the transmission network and therefore generally change the system impedance[3].

1.4.1 Static VAR Compensators (SVC) and Static Synchronous Compensators (STATCOMs)

Static VAR compensators are traditionally used equipments for reactive power exchange at the point of common coupling. The configuration of Static VAR compensators is shown in the figure below:

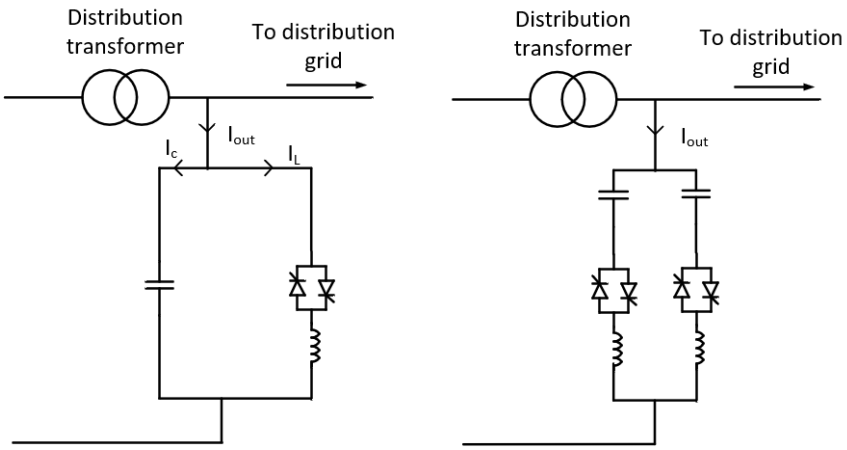


(a) SVC connected at the power line

Figure 1.11: SVC connected at the power line

These SVCs can support voltages of critical loads, improve transient stability and dampens the power oscillations[6]. The STATCOM has the same capabilities, but with a higher control bandwidth and the additional capability of providing higher currents at low voltage levels since the SVC VAR generation is a function of V^2 and in STATCOM it is a function of V [7][8]

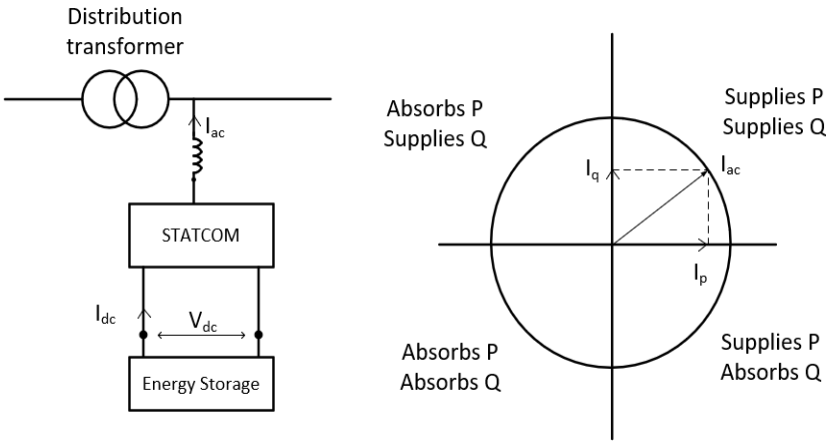
STATCOM is a power electronics device based on the voltage source converter principle [9]. The technology typically, in use is, depending on the voltage level and total rating, two or three level voltage source converter, controlled by digital techniques and connected to the power system in shunt through a filter and possibly a coupling transformer[10]. Whereas, SVCs consists of thyristor controlled reactor, and thyristor or mechanically switched capacitors. It can be considered as a shunt impedance determined by the parallel connection of the capacitor and the effective inductance of the thyristor controlled reactor[9],[11].



(a) STATCOM connected at the power line

Figure 1.12: STATCOM connected at the power line

However, when the STATCOM is used for reactive-power generation, the converter itself can keep the capacitor charged to the required voltage level. This is accomplished by controlling output voltage lag behind ac-system voltage by a small angle. In this way, the converter absorbs a small amount of real power from the ac system to meet its internal losses and keep the capacitor voltage at the desired level. The same mechanism can be used to increase or decrease the capacitor voltage. The reactive and real power exchange between the STATCOM and the ac system can be controlled independently of each other. Any combination of real power generation or absorption with VAR generation or absorption is achievable if the STATCOM is equipped with an energy storage device of suitable capacity as shown in the figure below.



(a) STATCOM with an energy storage and its operating zone

Figure 1.13: STATCOM with an energy storage and its operating zone

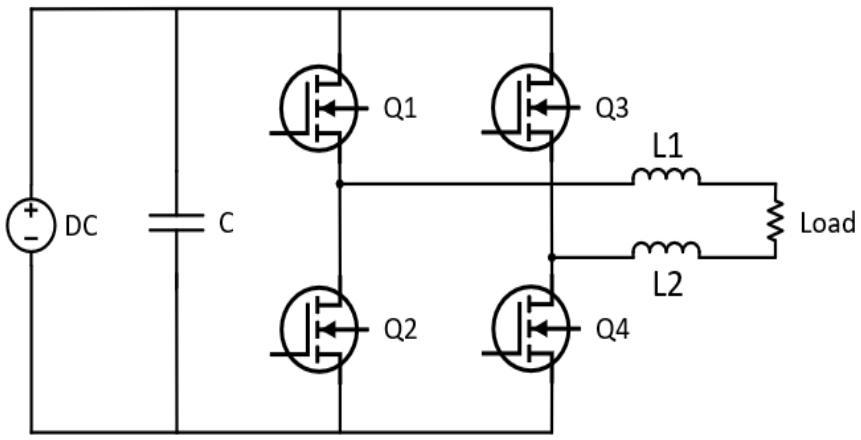
These power electronics devices are very vulnerable in terms of harmonic distortion. They inject harmonic currents in the grid and active control is very difficult for harmonic mitigation[5].

1.4.2 Two-level and Three-level Inverters

Single phase inverters can be designed in various ways namely two-level and multi-level inverters. From the literature review point, I am focusing on 2-level and 3-level inverters which has been discussed below:

1.4.2.1 Two-level inverters

The converters which produce an output voltage or current with level either +ve /-ve are known as two level converters. In high power and high voltage applications this two level inverter however have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating.

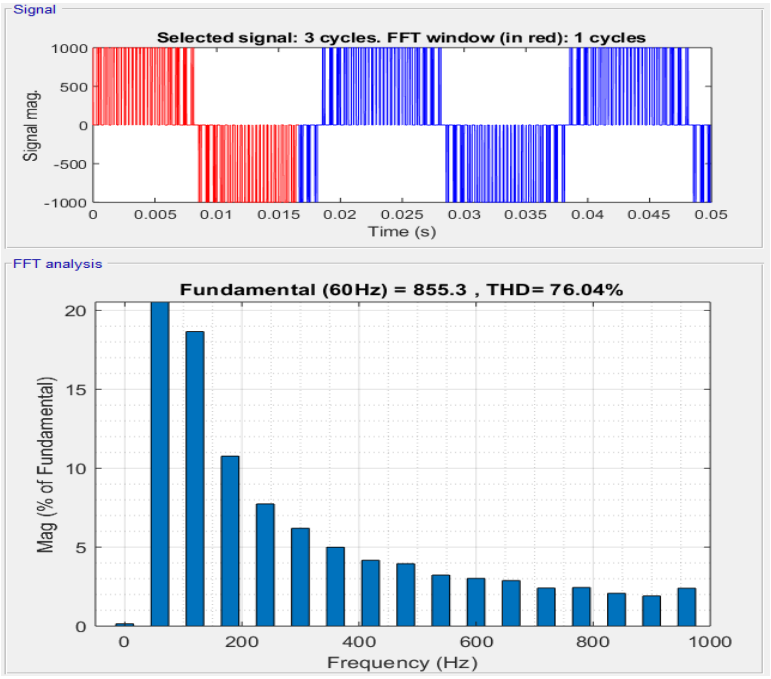


(a) Two-level H-bridge inverter

Figure 1.14: Two-level H-bridge inverter

As the devices switch between +maximum to -maximum of the DC voltage, the stress on the device is more. Also, since we get only two switching levels, the harmonics are more as compared to three-level inverters.

Switching current harmonics in a typical 2-level inverter:

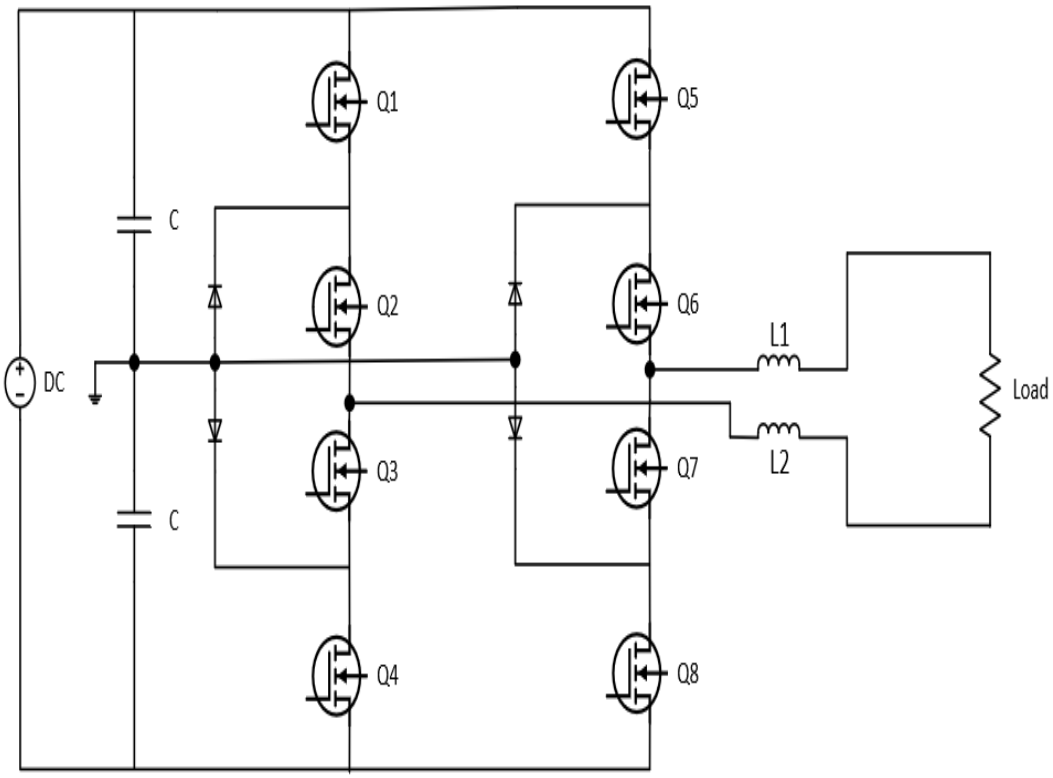


(a) Two-level H-bridge inverter voltage harmonics

Figure 1.15: Two-level H-bridge inverter voltage harmonics

1.4.2.2 Three-level inverters

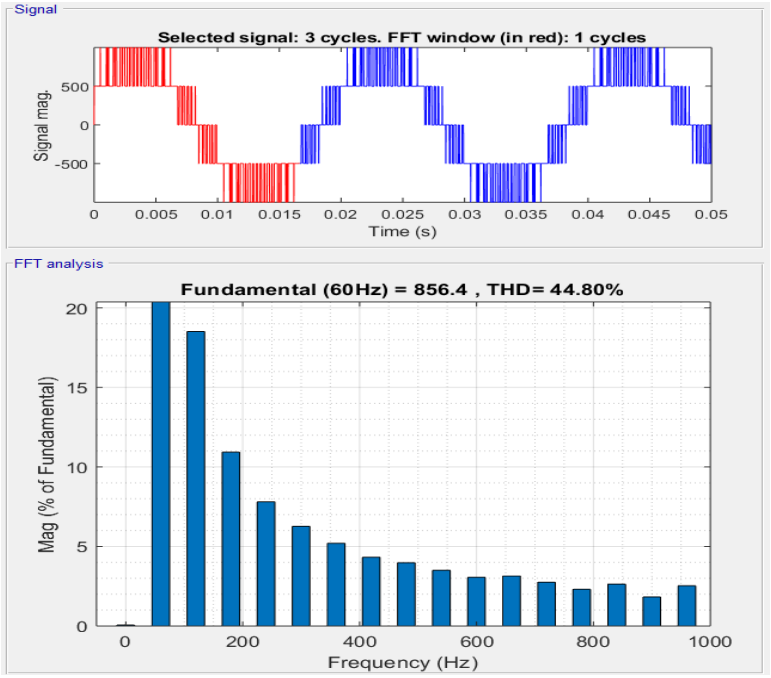
In multilevel inverter we generate more than two voltage levels which exhibits almost pure sinusoidal output voltage waveform. Which has low dv/dt, low harmonic distortions. Because of multiple voltage levels in the output the waveform becomes more smoother but with increasing levels the circuit becomes more complex due to addition of the valves. And complicated control circuit is also required. For understanding purpose the circuit diagram of three level inverter is shown below. This design resembles to the two level inverter having only two additional switches and diodes are used and called as clamping diodes.



(a) Three-level H-bridge inverter

Figure 1.16: Three-level H-bridge inverter

Switching current harmonics in a typical 3-level inverter:

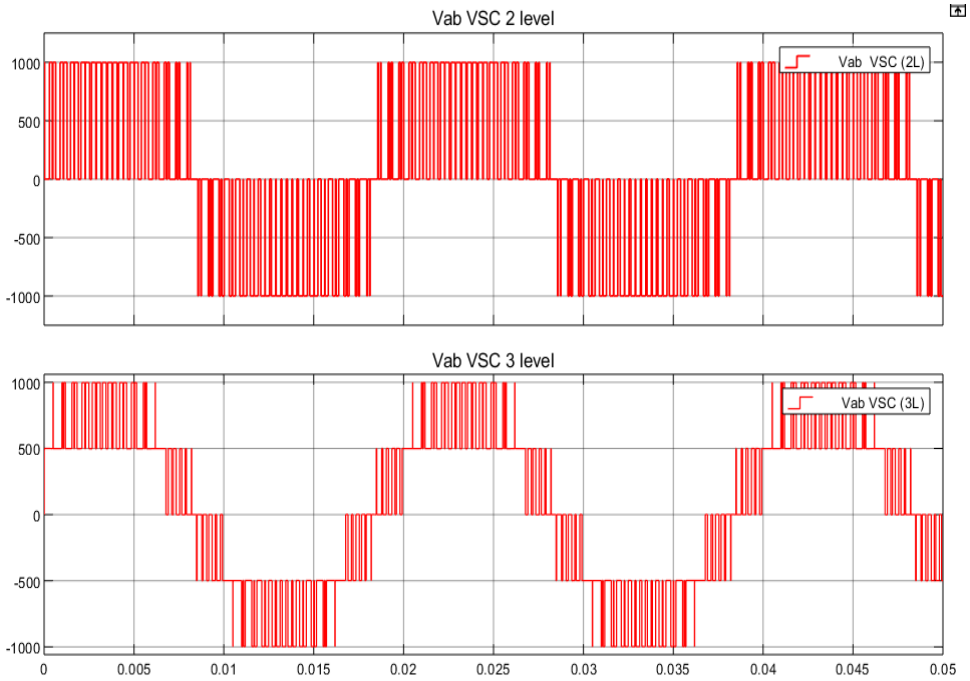


(a) Three-level H-bridge inverter voltage harmonics

Figure 1.17: Three-level H-bridge inverter voltage harmonics

1.4.2.3 Comparison between two-level and three-level inerters

The two-level inverter will need high voltage semiconductor devices for high DC bus applications. Multilevel inverters on the other hand, have better performance than the two-level topology since they produce much better output voltage waveforms and they can operate at a lower switching frequency than two-level inverters but magnetics need to be designed accordingly. They also can utilize low voltage semiconductor devices which are less expensive and faster in operation.



(a) Two-level and three-level H-bridge inverter waveforms

Figure 1.18: Two-level and three-level H-bridge inverter waveforms

Table 1.1: Comaprison of two-level and multi-level invertes on different attributes.

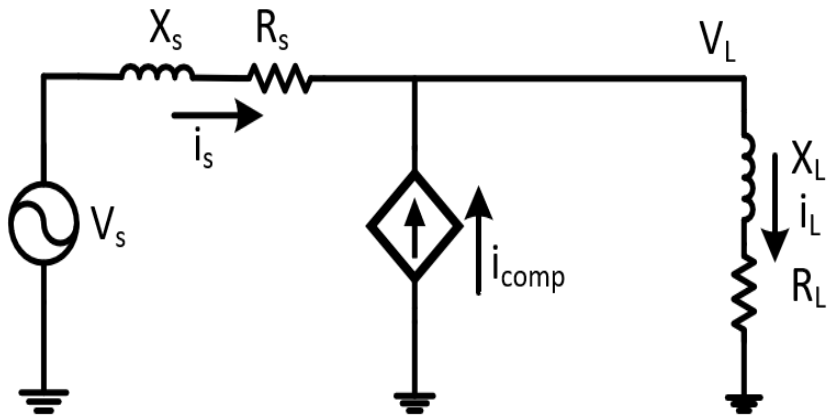
S.No.	Attributes	Two-level inverter	Multilevel inverter
1	Rate of rise of voltage	high	low
2	Switching losses	high	low
3	Application	low voltage	high voltage
4	Voltage stress in switches	more	less
5	Multiple voltage levels	can not be produced	can be produced
6	Harmonics	more	less
7	Complexity	less	more

As we see that the harmonic distortion in 2-level converter is more as compared to 3-level converters for the same switching frequency. But if we increase the switching

frequency the harmonic distortion can be minimized in 2-level inverters significantly.

1.5 Problem Statement

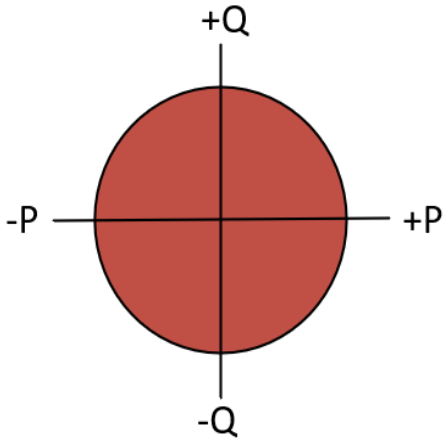
Now since we know from the above discussions, that both active and reactive power needs to be compensated to maintain required voltage depending on the load at the distribution level. It is very important to investigate different permutations and combinations of active and reactive power for voltage stability.



(a) A distribution system with active and reactive compensation

Figure 1.19: A distribution system with active and reactive compensation

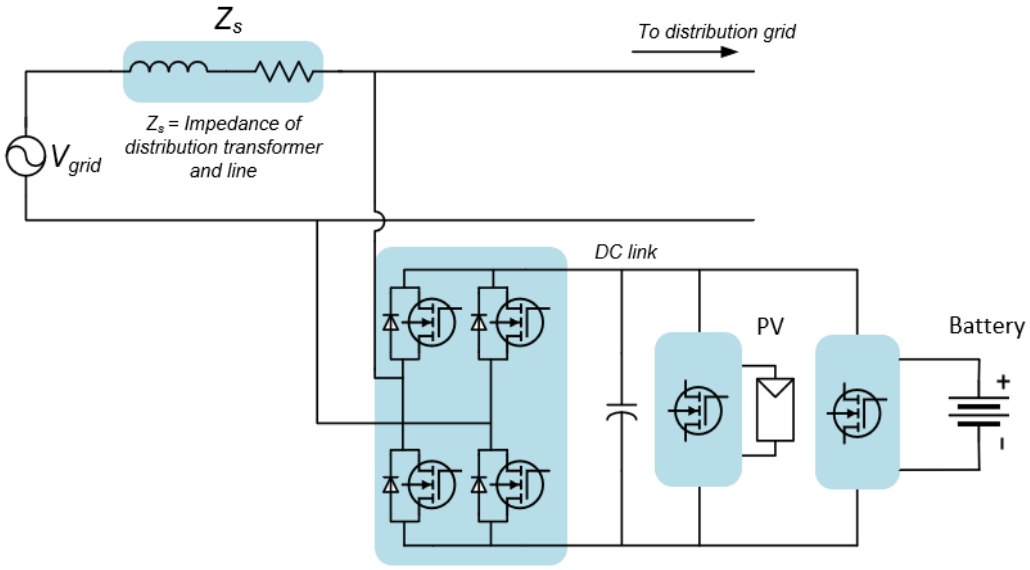
Maintaining the voltage at fixed level is only possible when the power demand is equal to the power input in the particular node. Any imbalance or mismatch between these two, would result as the voltage falling below the required values of standard distribution voltages. There might be case of excess and scarcity of active power and reactive power at any node. So, to resolve this issue, the solution must be able to operate in all kinds of different combinations of active and reactive power. That means the solution must be able to sink or source active or(and) reactive power simultaneously. That means if we think of a four-quadrant system having active and reactive power as its axis, it must be able to operate in all the four quadrants as shown in the figure below.



(a) Four quadrant operation

Figure 1.20: Four quadrant operation

Therefore, a power electronics inverter which can be operated in all four zones of active and reactive combinations needs to be developed. The dynamics of this operation is well discussed in [12].

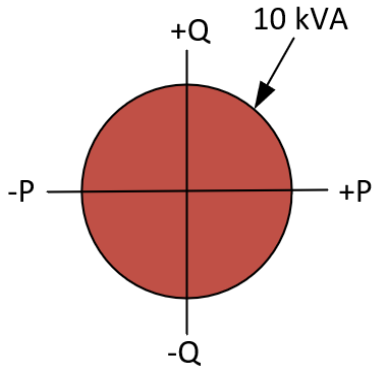


(a) An integrated system with power electronic converters to provide active and reactive compensation

Figure 1.21: An integrated system with power electronic converters to provide active and reactive compensation

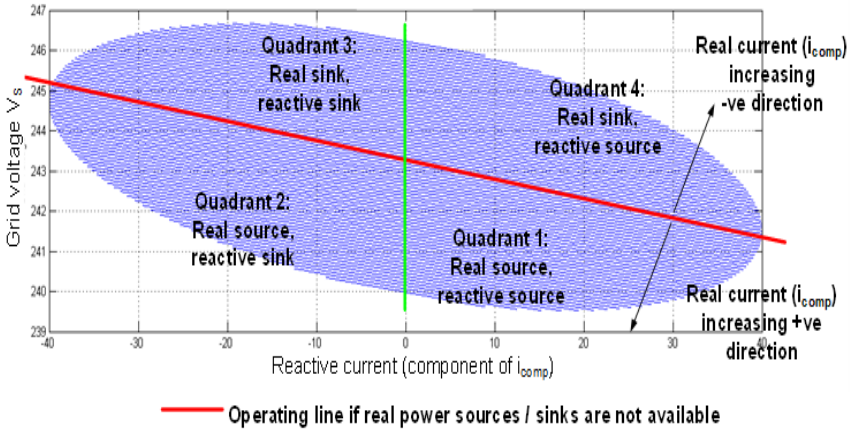
As explained in [12] and [13], the converter should be able to perform the controls operation in all four quadrants within its ratings. According to X/R ratio of the requirements of P and Q changes as shown in the figure according to [12][13].

For a 10 kVA application the four-quadrant operation and voltage support capability is shown in the figure.



(a) 10 kVA compensator four quadrant operation

Figure 1.22: 10 kVA compensator four quadrant operation



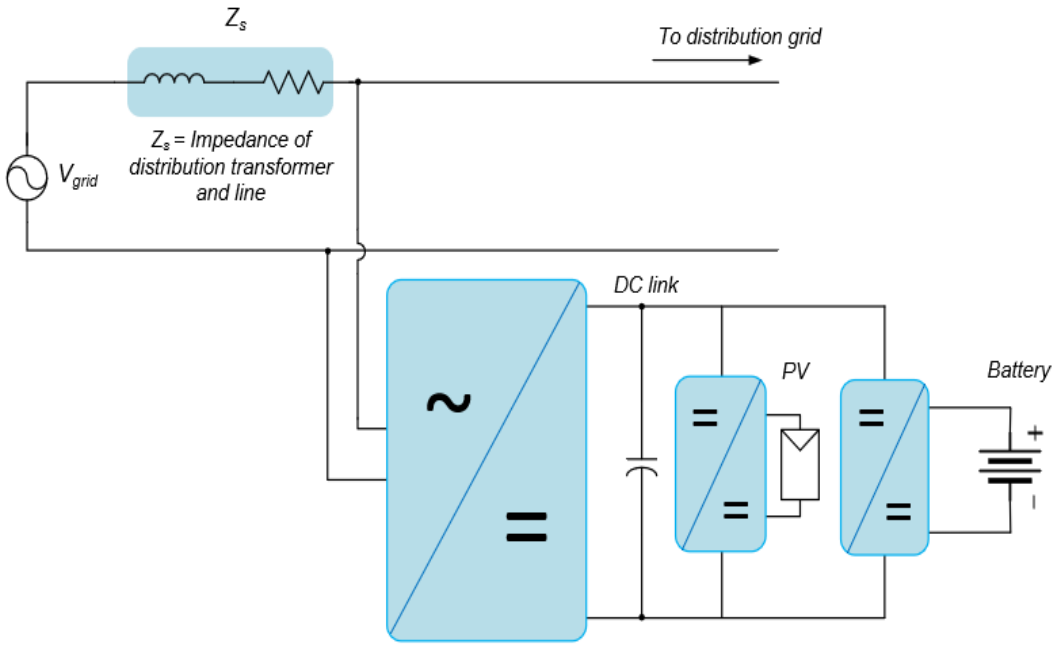
(a) Voltage support capability of a μ-statcom

Figure 1.23: Voltage support capability of a μ-statcom

The goal of the thesis is to develop a power electronics converter for the four quadrant operation.

CHAPTER 2: STABILITY ANALYSIS

The development of power electronics system is a complex task and it requires complete knowledge of a system. The system can be analyzed mathematically by the means of system stability and controls. The open loop and closed loop response of the system characterizes the system and hence it is used to define the control equations. The integrated system which is being proposed is as follows:



(a) Integrated system

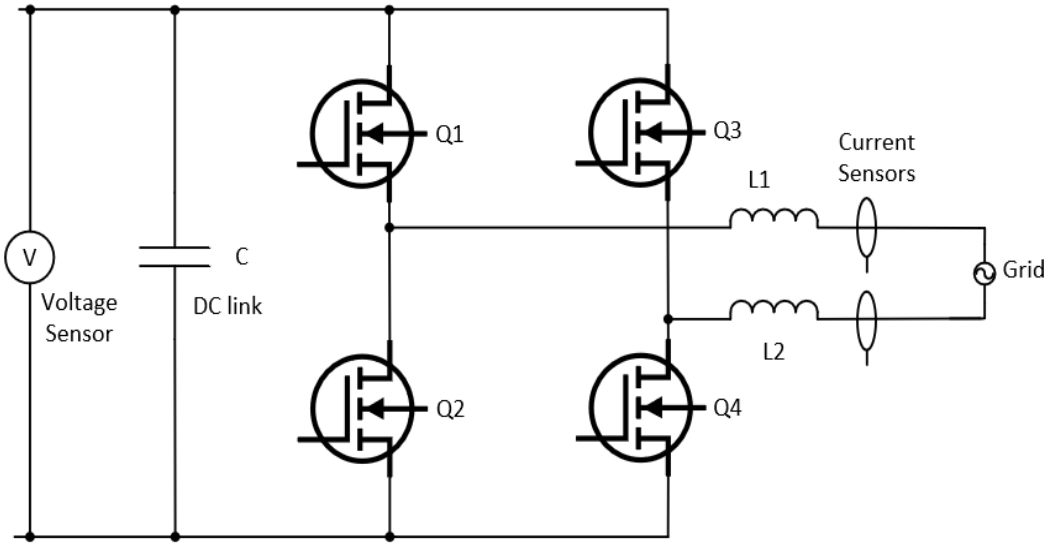
Figure 2.1: Integrated system

The integrated system consists of a Photovoltaic DC-DC converter for boost operation, a battery converter for buck-boost operation and an inverter which regulates the current waveforms through controls for the grid-tied operation.

The central part of the analysis in this chapter will be characterizing inverter

transfer function and analyzing the stabilty for controlling the grid current.

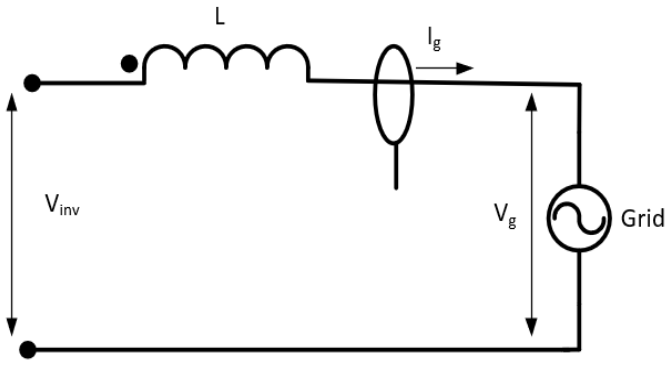
The inverter circuit design consists of two half bridge MOSFETs which makes it full H-bridge, two splitted inductors connected in series and the DC link capacitors. The AC current sensosrs and DC link voltage sensors are used for performing controls. The schematic is shown below.



(a) Inverter

Figure 2.2: Inverter

Suppose switching voltage at the output of the inverter is V_{inv}, grid voltage is V_g and grid current is I_g. These three quantities are related as follows.



(a) Inverter when seeing from the grid

Figure 2.3: Inverter when seeing from the grid

Writing the states of this circuit

$$x = I_{\mathrm{g}} \tag{2.1}$$

Applying the KVL in the circuit,

$$V_{\mathrm{inv}} = L\frac{dI_{\mathrm{g}}}{dt} + V_{\mathrm{g}} \tag{2.2}$$

and output,

$$y = I_{\mathrm{g}} \tag{2.3}$$

$$\dot{x} = [0]\begin{bmatrix} I_{\mathrm{g}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{-1}{L} \end{bmatrix}\begin{bmatrix} V_{\mathrm{inv}} \\ V_{\mathrm{g}} \end{bmatrix} \tag{2.4}$$

$$y = \begin{bmatrix} 1 \end{bmatrix}\begin{bmatrix} I_{\mathrm{g}} \end{bmatrix} + [0]\begin{bmatrix} V_{\mathrm{inv}} \\ V_{\mathrm{g}} \end{bmatrix} \tag{2.5}$$

Comparing the equation with the standard equation:

$$\dot{x}(t) = A(t)x(t) + B(t)u(t) \tag{2.6}$$

$$y(t) = C(t)x(t) + D(t)u(t) \tag{2.7}$$

We get,

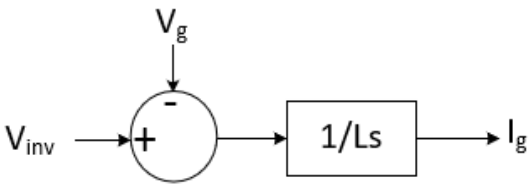
$$A = 0, B = \begin{bmatrix} \frac{1}{L} & \frac{-1}{L} \end{bmatrix} \tag{2.8}$$

$$C = 1, D = 0 \tag{2.9}$$

So, the open loop transfer function will be G(s) = (C)$(SI - A)^{-1}$(B) + D

$$G(s) = \frac{I_{\mathrm{g}}}{V_{\mathrm{inv}}} = \frac{1}{Ls} \tag{2.10}$$

The open loop system of the inverter will be as shown in the below figure:



(a) Open loop transfer function

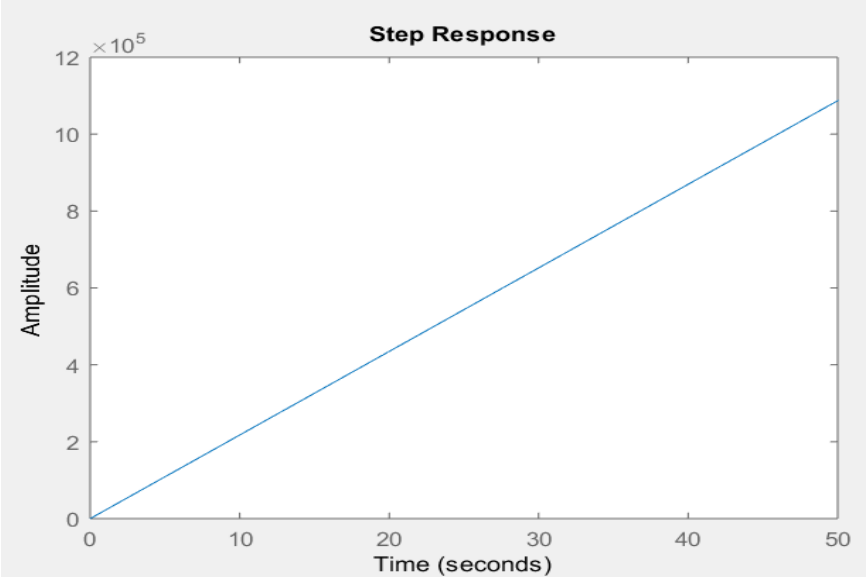
Figure 2.4: Open loop transfer function

with L = 46μH

The transfer function is first order transfer function.

$$G(s) = \frac{1}{46x10^{-}6s}$$

Open loop step response of the system is

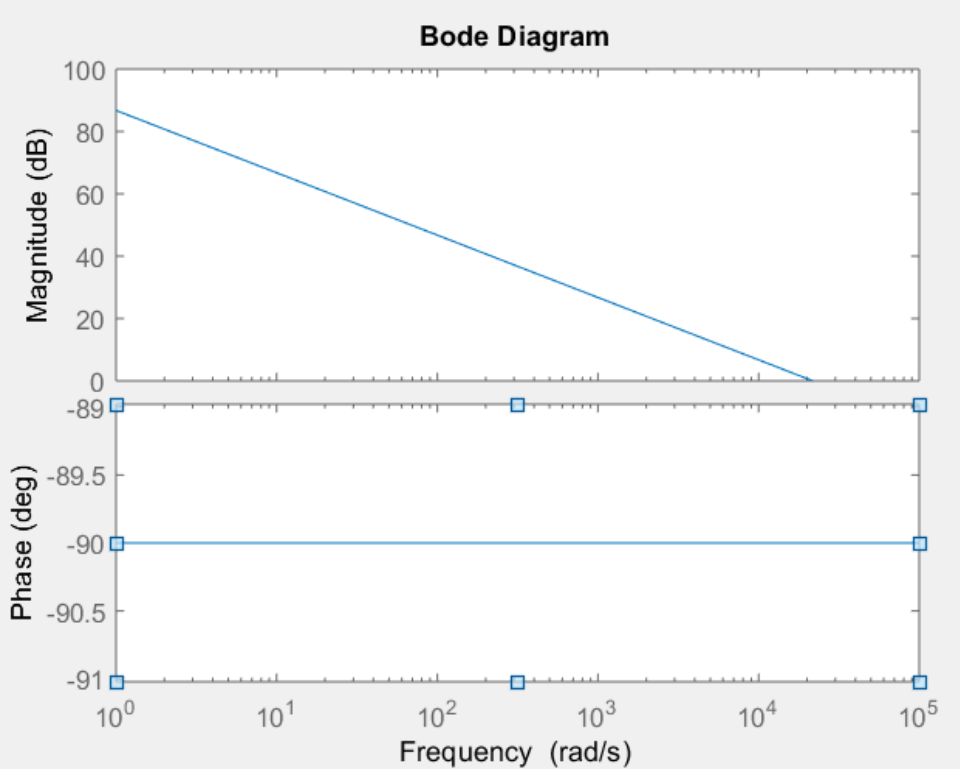


(a) Step response of open loop system

Figure 2.5: Step response of open loop system

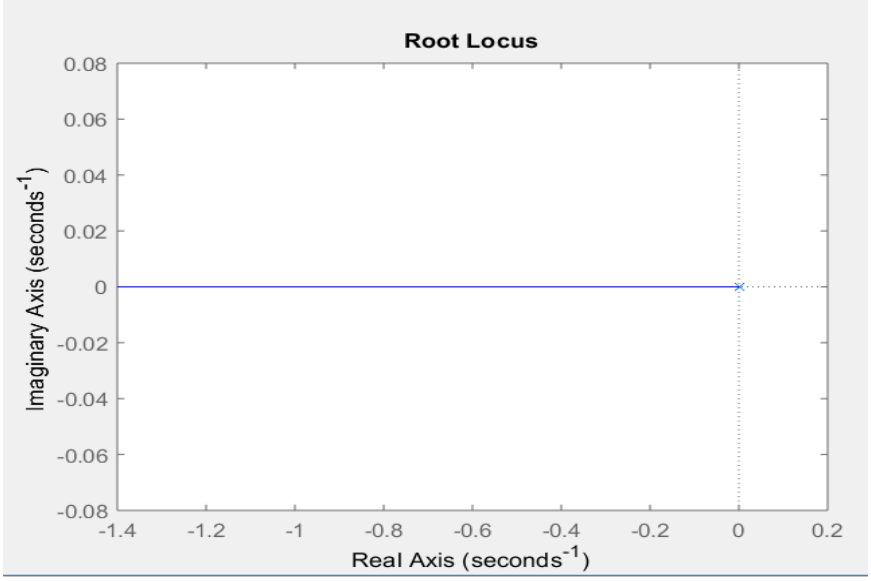
Above picture shows there is unbounded output while feeding the bounded input, which indicates that the system is unstable.

The phase and gain margin are:



(a) Phase margin and gain margin of open loop system

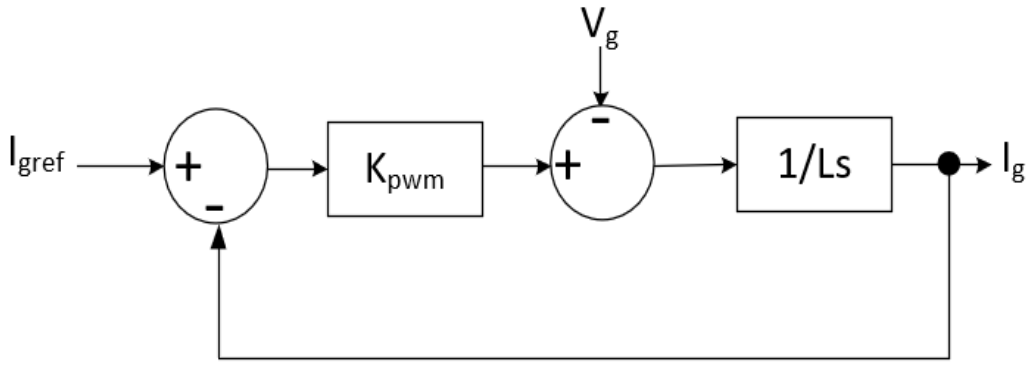
Figure 2.6: Phase margin and gain margin of open loop system



(a) Root locus of open loop system

Figure 2.7: Root locus of open loop system

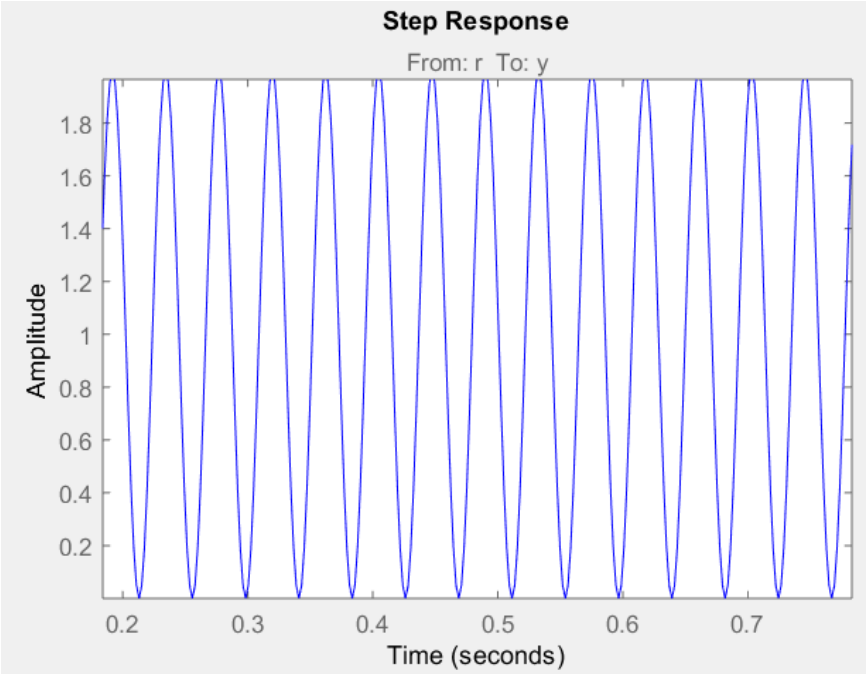
Let us see the unity feedback closed loop response with an additional pole at the origin:



(a) Closed loop unity feedback system

Figure 2.8: Unity feedback closed loop transfer function

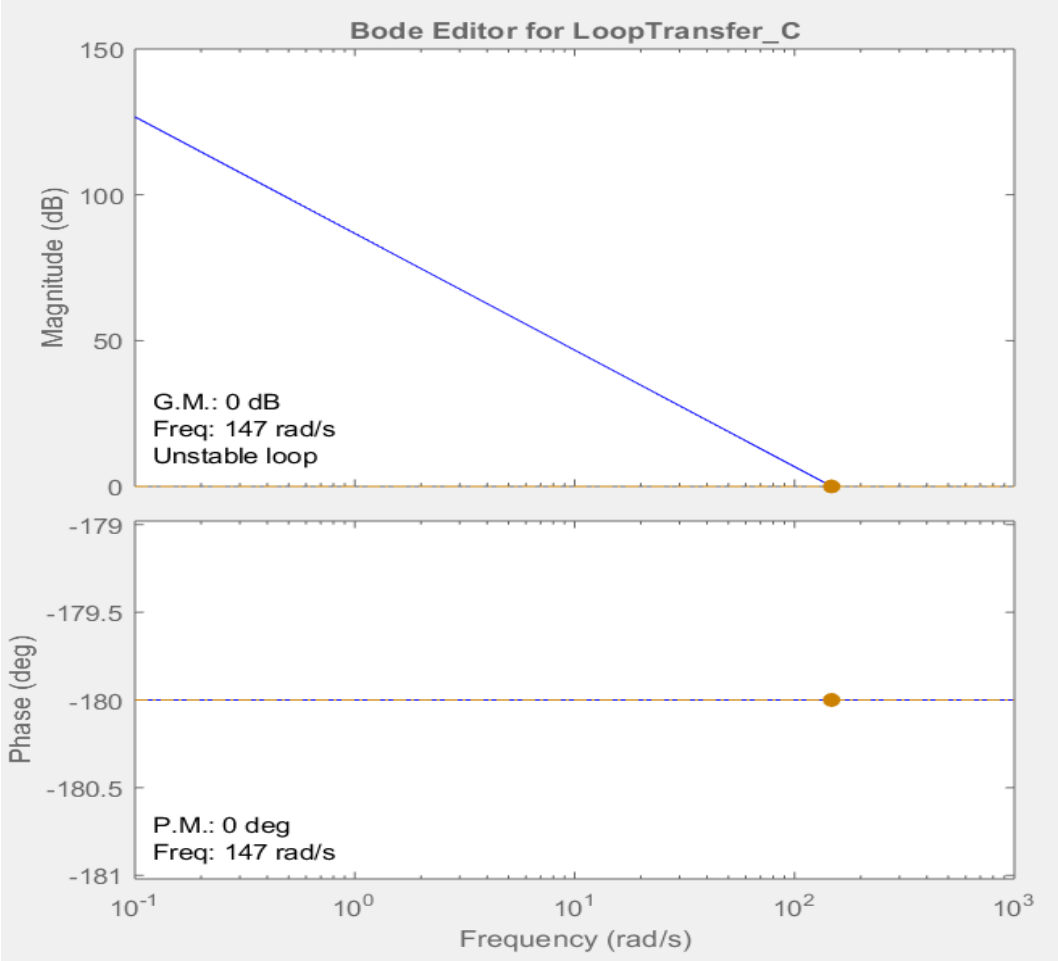
The stability attributes for this system:



(a) Step response of unity feedback closed loop system

Figure 2.9: Step response of unity feedback closed loop system

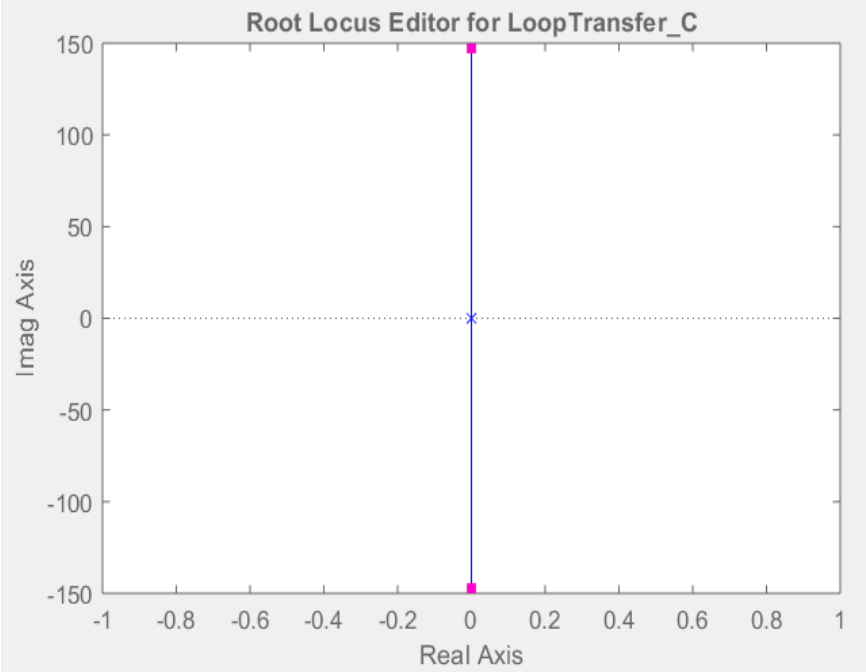
From the above plot of step response we can observe that the system is oscillating at constant frequency which indicates that the system is unstable.



(a) Bode plot of unity feedback closed loop system

Figure 2.10: Bode plot of unity feedback closed loop system

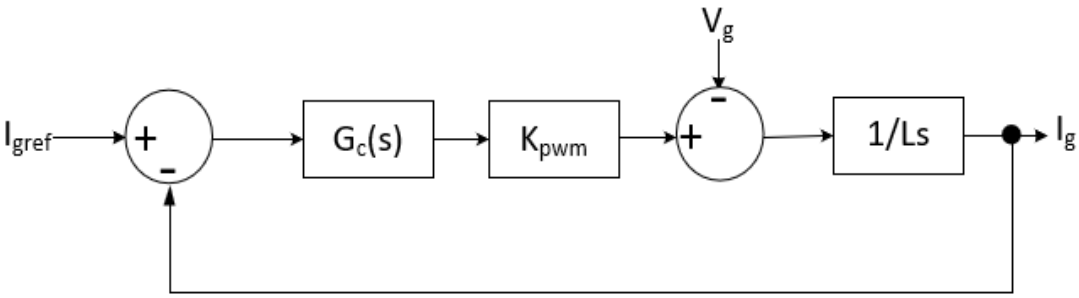
There is no phase and gain margin which further indicates that the system is unstable. This system is unity feedback uncompensated system and since it is unstable we need to add compensators to stabilize the system.



(a) Root locus plot of unity feedback closed loop system

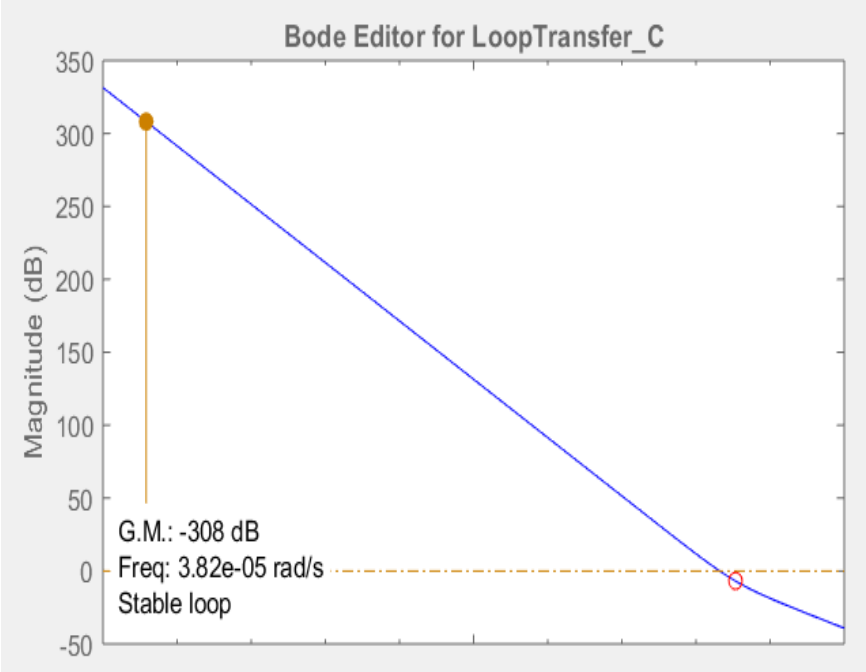
Figure 2.11: Root locus plot of unity feedback closed loop system

Let us analyze the closed loop system for the inverter:



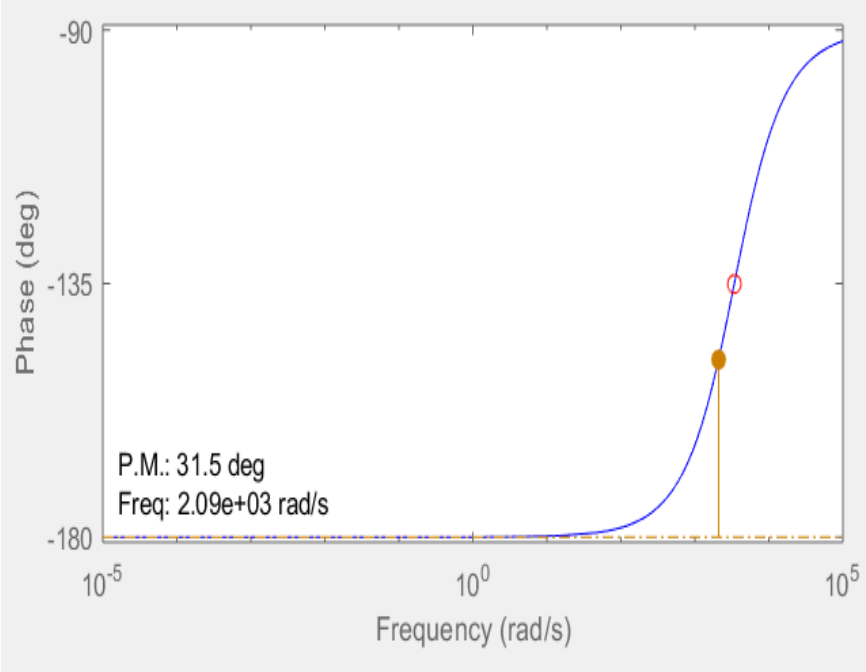
(a) Closed loop transfer function

Figure 2.12: Closed loop transfer function



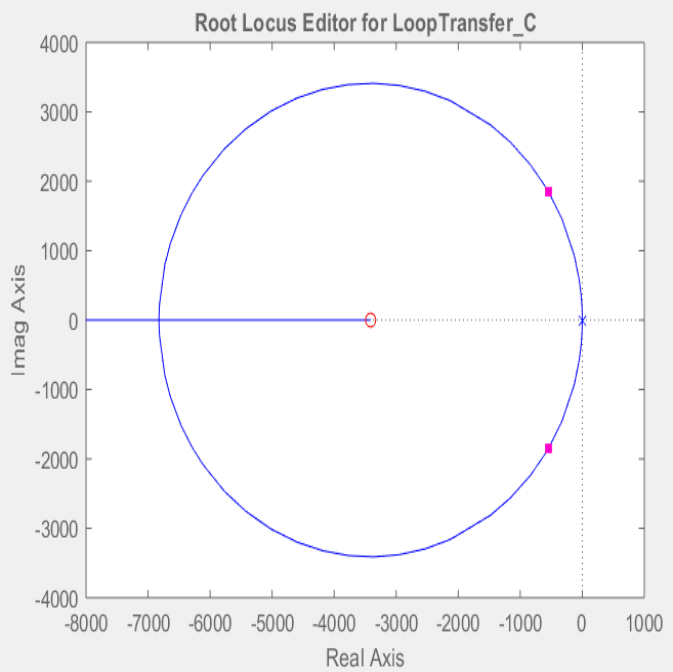
(a) Gain margin of compensated closed loop system

Figure 2.13: Gain margin of compensated closed loop system



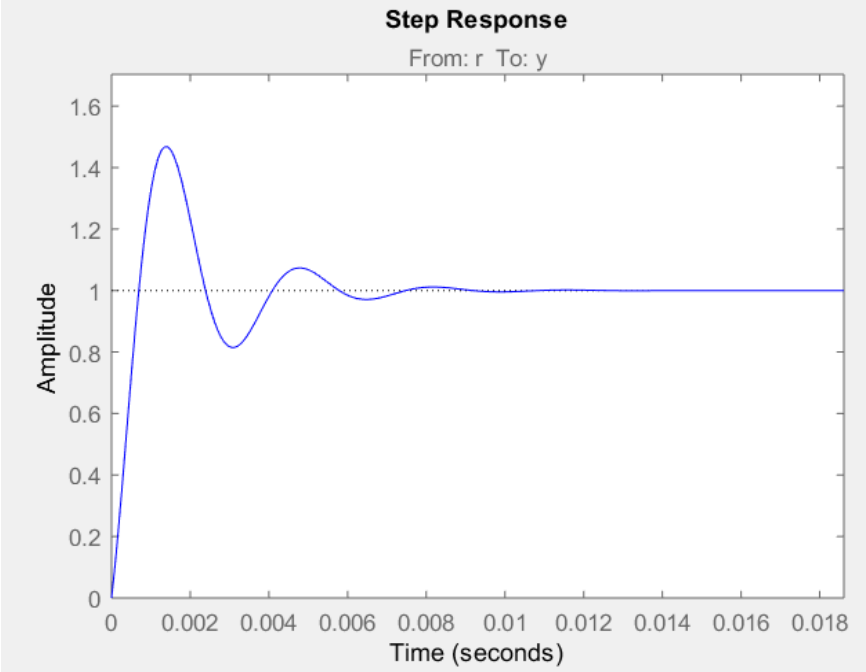
(a) Phase margin of compensated closed loop system

Figure 2.14: Phase margin of compensated closed loop system



(a) Root locus of compensated closed loop system

Figure 2.15: Root locus of compensated closed loop system



(a) Step response of compensated closed loop system

Figure 2.16: Step response of compensated closed loop system

Here we can observe that the compensated closed loop transfer function is stable. The poles at the origin is compensated by a zero at the left hand side of the root locus graph in frequency domain. The overall system is stable and it produces the bounded output for the bounded input and the step response stabilizes after small transients.

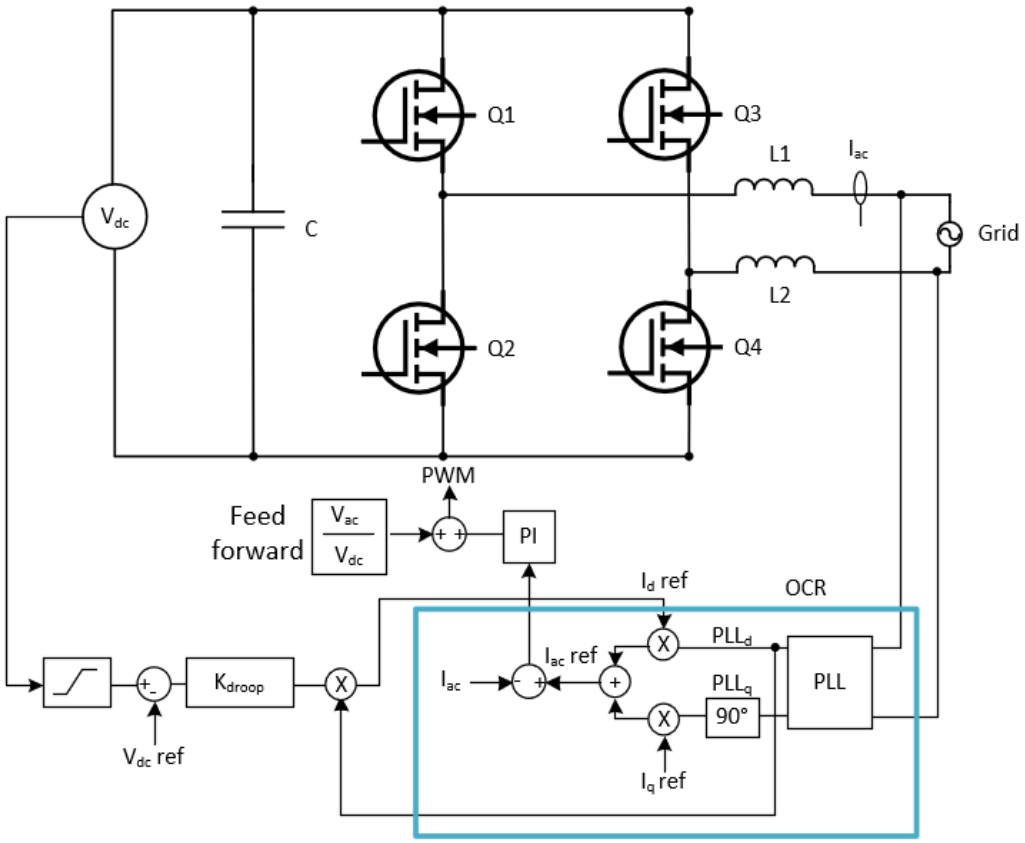
The closed loop response is the characterization of closed loop transfer function which tells the system can remain in stable zone within the controller bandwidth. The concept of compensated stable system will be implemented in later sections for control algorithm implementation.

In the next chapter, the control implementation has been discussed in detail.

CHAPTER 3: CONTROLS AND SIMULATIONS

3.1 Control Philosophy

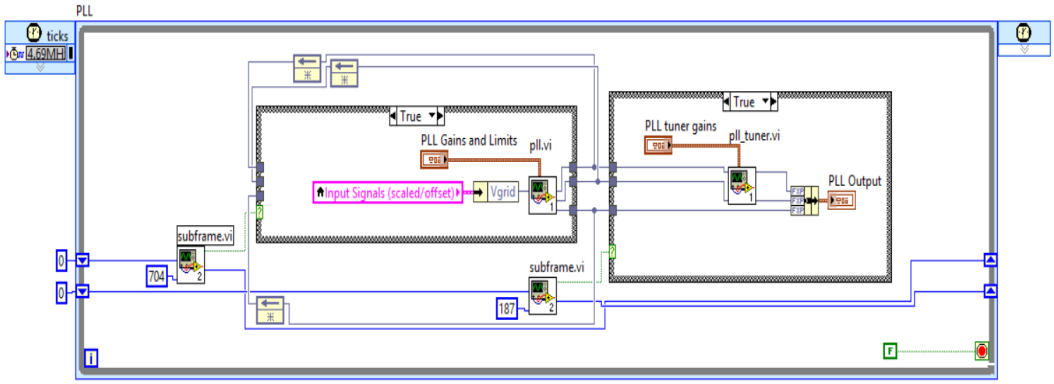
The power electronic controls strategy of the inverter is shown below. The control loop is the fast output current regulator (OCR) which is responsible for generating a output current that matches the current reference. To achieve faster response, and to avoid phase shift due to the grid voltage fundamental component, AC voltage feed-forward is employed.



(a) Control Philosophy

Figure 3.1: Closed loop controls

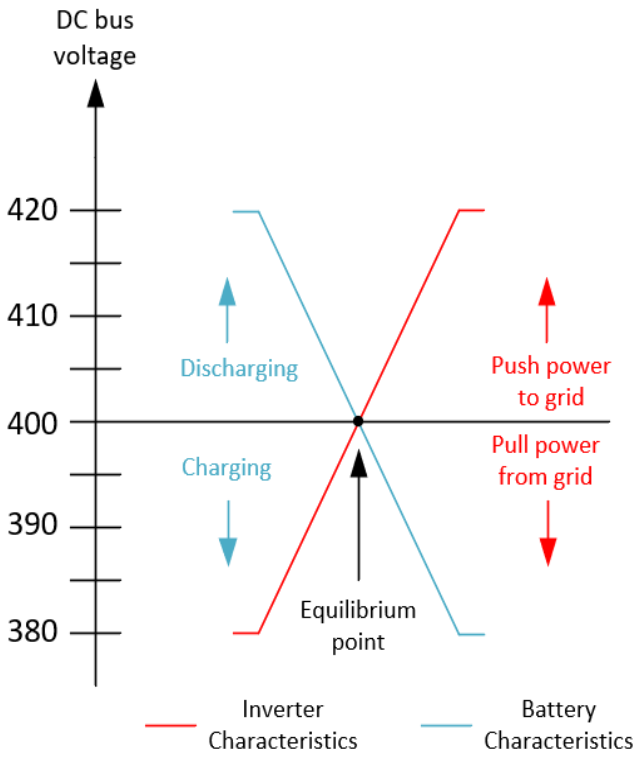
Below picture shows the implementation of PLL in LABVIEW environment.



(a) PLL implementation in labview

Figure 3.2: PLL implementation in labview

The picture below shows the droop control for maintaining the DC bus at 400V. The overall control philosophy is described below:

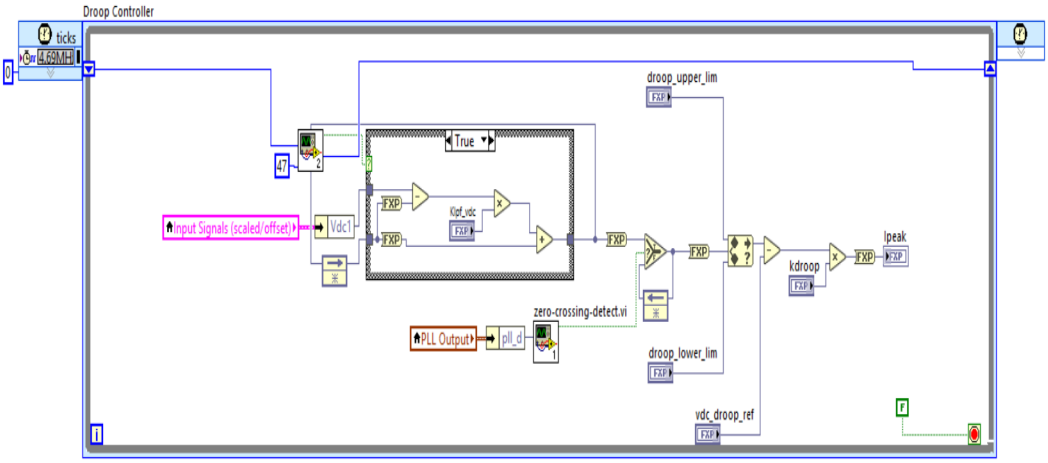


(a) Droop control implementation

Figure 3.3: Droop control implementation

The inverter in closed loop operation changes the direction of the current in such a way that it helps the operating point to move closer to 400V DC bus. If the DC link voltage is above 400V, then the control will try to discharge the capacitor to move closer to equilibrium point and if the DC link voltage is below 400V, it will try to pull power from the grid to maintain the DC bus at 400V.

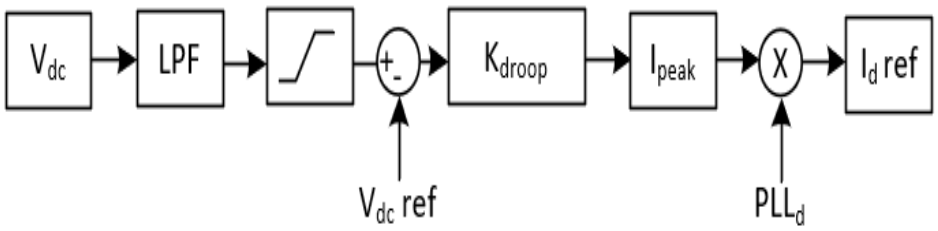
The floating characteristics of the droop is being used to charge and discharge the battery. When the inverter current direction changes, the battery current direction also changes to move closer to the equilibrium point.



(a) Droop control implementation in labview

Figure 3.4: Droop control implementation in labview

The reference current I_d is generated as shown in the figure below.

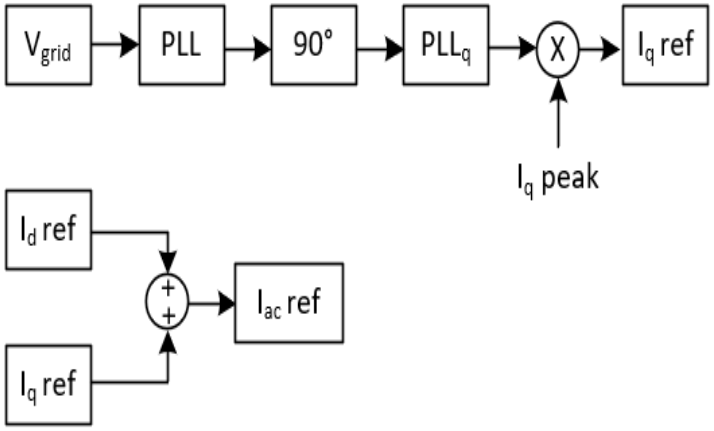


(a) Generating I_d reference

Figure 3.5: Generating I_d reference

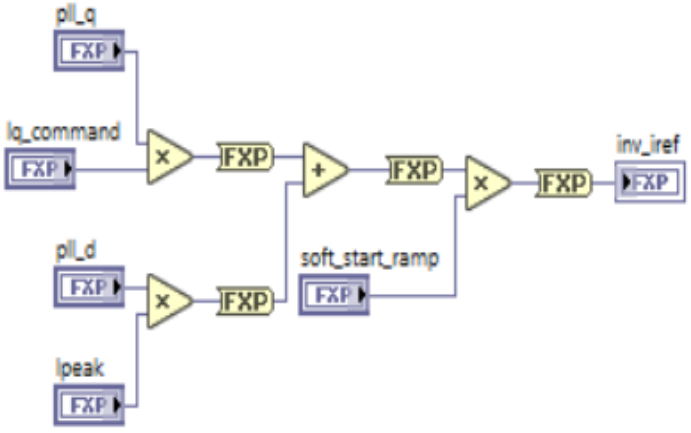
I_d reference is generated by sensing DC link voltage and comparing it to the reference voltage. It is scaled to K_{droop} and the magnitude is multiplied by the in phase component of PLL.

The magnitude of reference current is generated by the addition of two sinusoidal components namely I_d and I_q which are scaled values of in-phase and quadrature component of PLL.



(a) Generating current reference

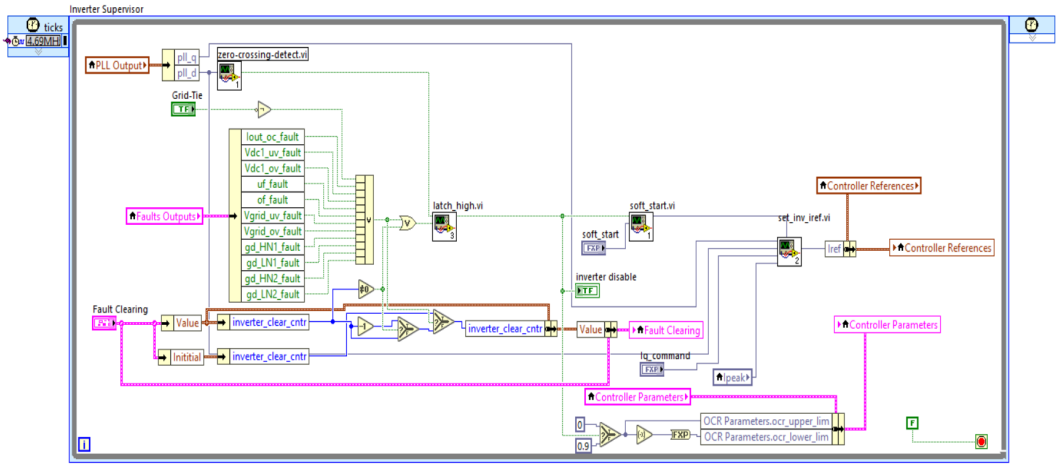
Figure 3.6: Generating current reference



(a) Generating current reference in labview

Figure 3.7: Generating current reference in labview

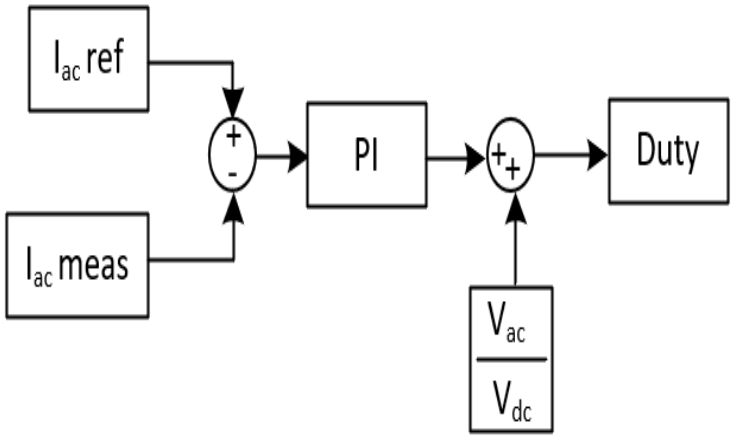
The reference current is fed to a proportional and integrator (PI) controller. To accommodate the effect of grid disturbance and to make the controller faster, a feed-forward gain has been employed.



(a) Generating control references in labview

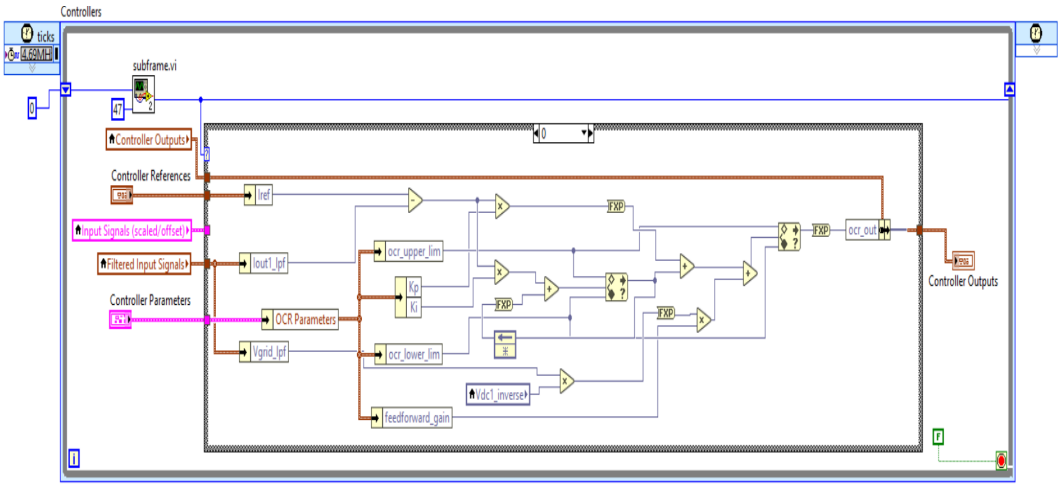
Figure 3.8: Generating control references in labview

Below figure shows the PI control with the feed forward and thereby generating the duty cycle.



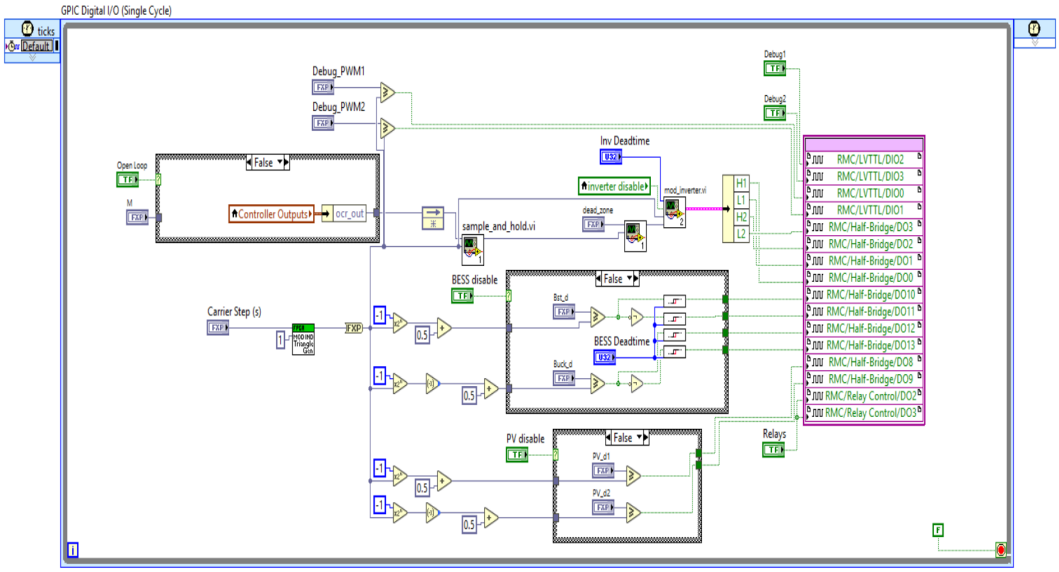
(a) Generating control outputs in labview

Figure 3.9: Generating control outputs in labview



(a) Generating control outputs in labview

Figure 3.10: Generating control outputs in labview



(a) PWM outputs in labview

Figure 3.11: PWM outputs in labview

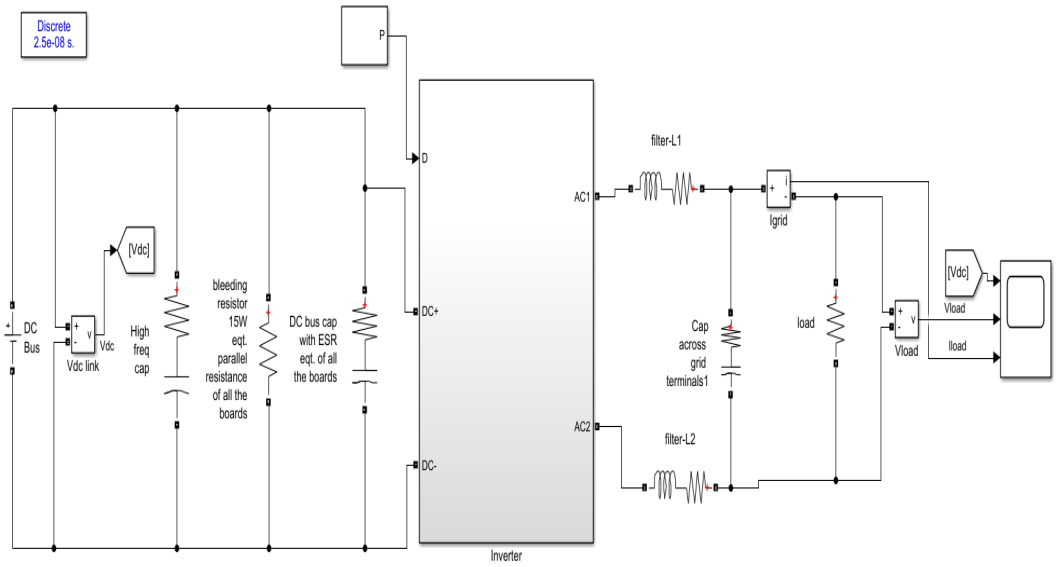
The above method of droop-control for DC voltage regulation and active, reactive control is well established method. The implementation in the LABVIEW requires all the controls to be implemented in discrete domain.

3.2 Simulations

The inverter is being fed from the power supply at the DC bus. DC bus is maintained at 400V and the AC output voltage is 240V RMS. A resistive load is connected across the AC terminals.

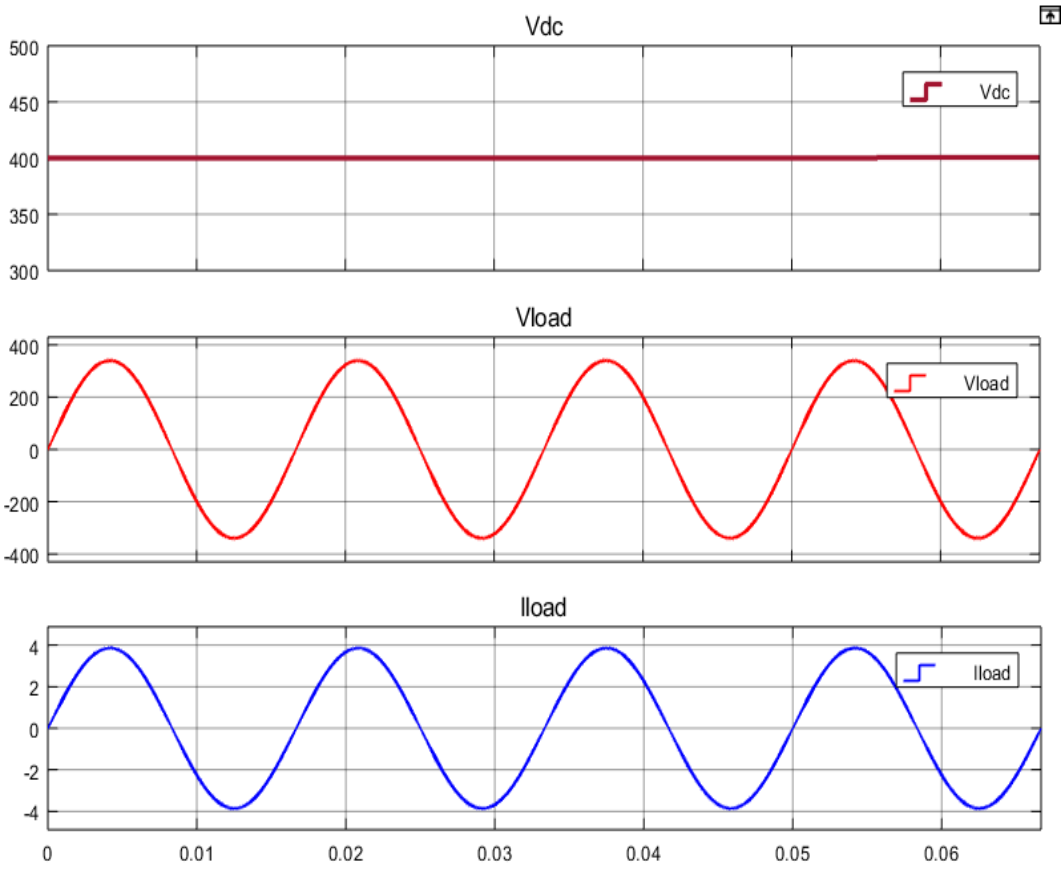
3.2.1 Open Loop Operation

- Open loop with a resistive load of 88 ohms



(a) Open loop with a resistive load of 88 ohms

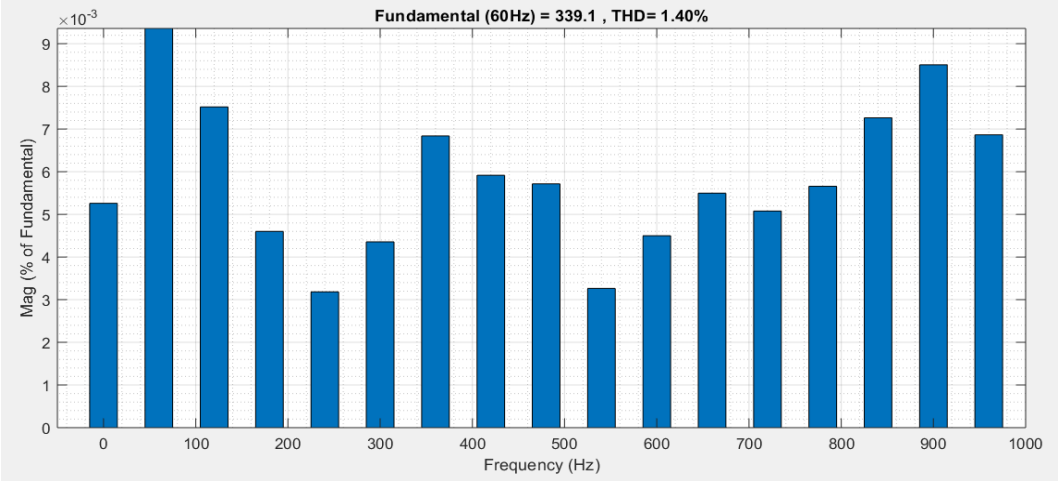
Figure 3.12: Open loop with a resistive load of 88 ohms



(a) Open loop with a resistive load of 88 ohms

Figure 3.13: Open loop with a resistive load of 88 ohms

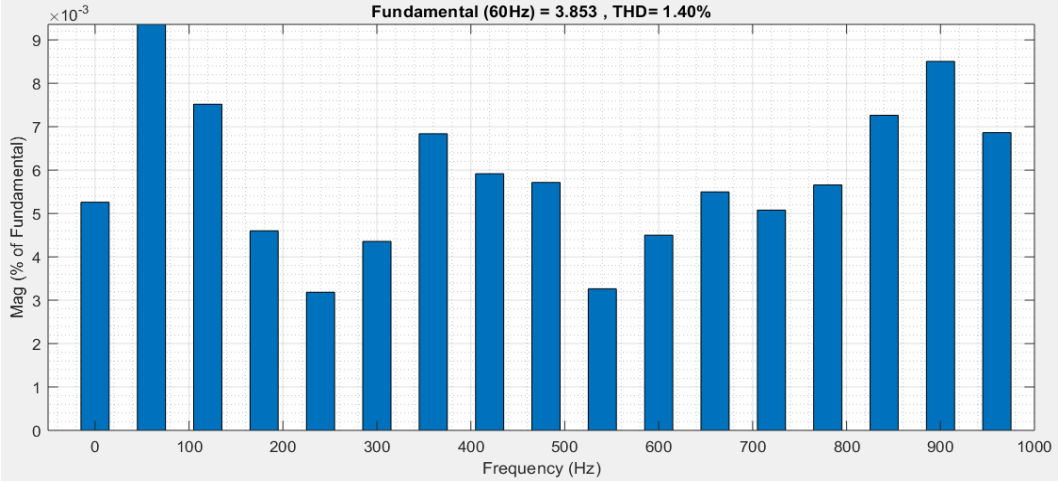
AC output voltage harmonics is shown in the figure below.



(a) Open loop voltage harmonics

Figure 3.14: Open loop voltage harmonics

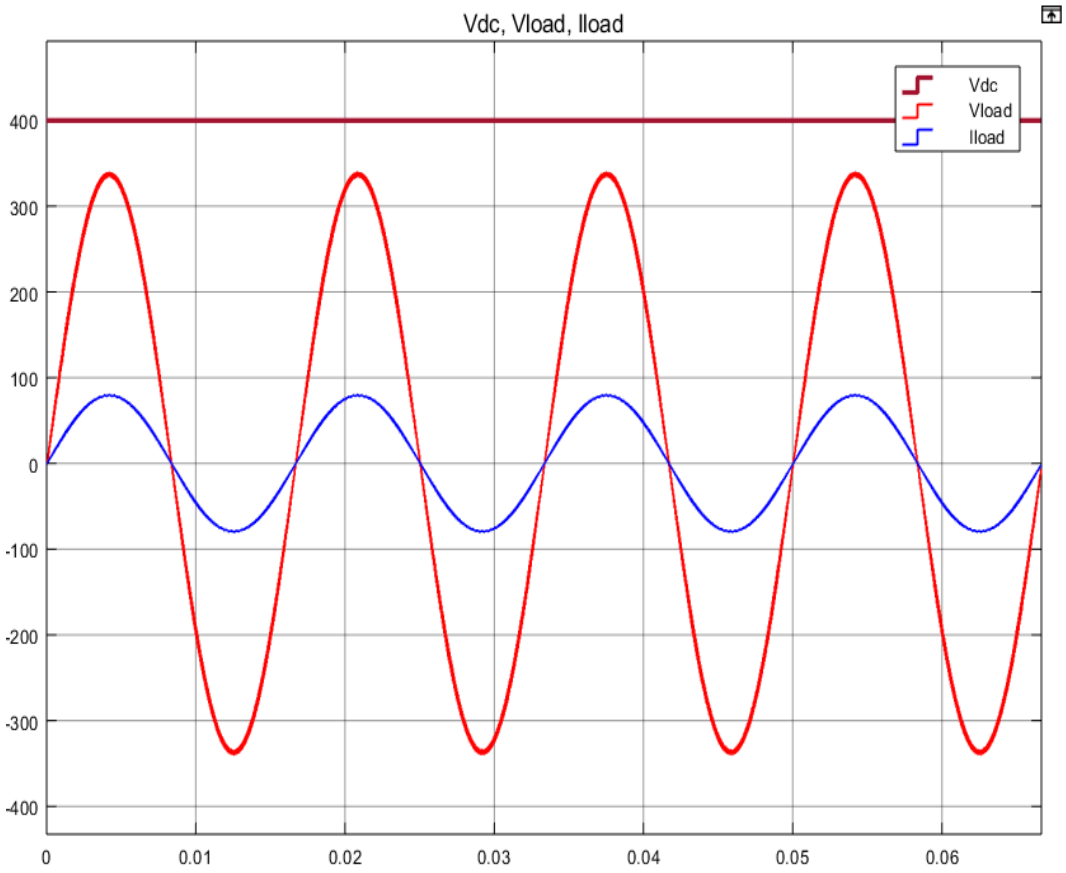
AC output current harmonics is shown in the figure below.



(a) Open loop current harmonics

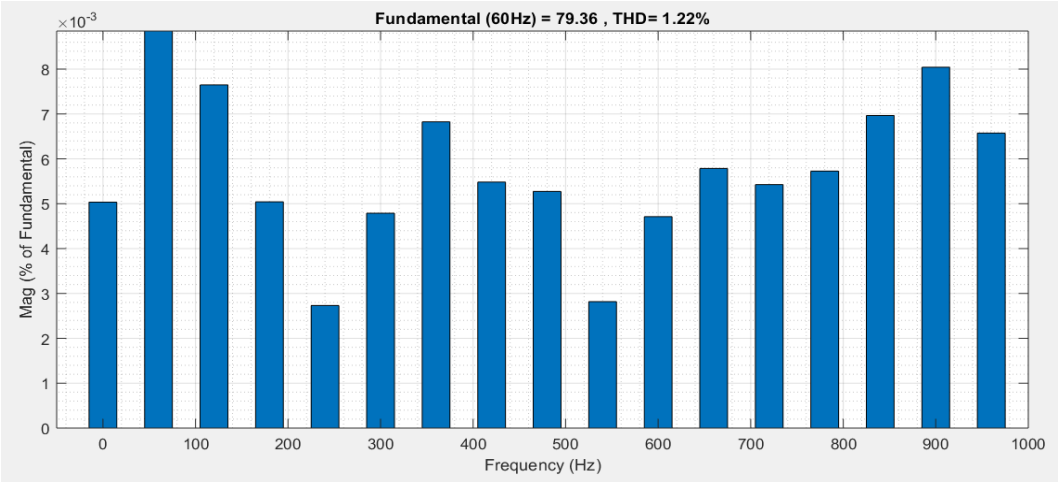
Figure 3.15: Open loop current harmonics

- Open loop with a resistive load of 4.24 ohms



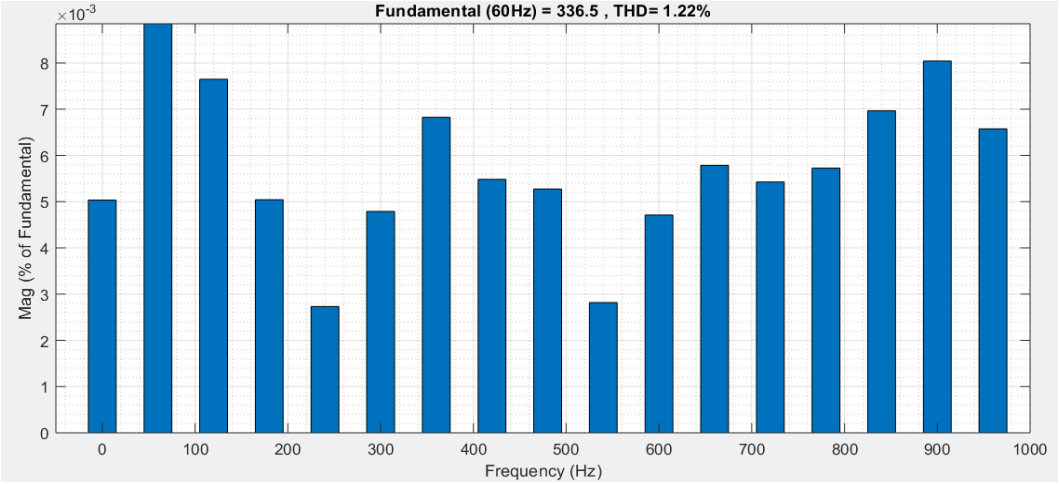
(a) Open loop with a resistive load of 4.24 ohms

Figure 3.16: Open loop with a resistive load of 4.24 ohms



(a) Open loop voltage harmonics

Figure 3.17: Open loop voltage harmonics



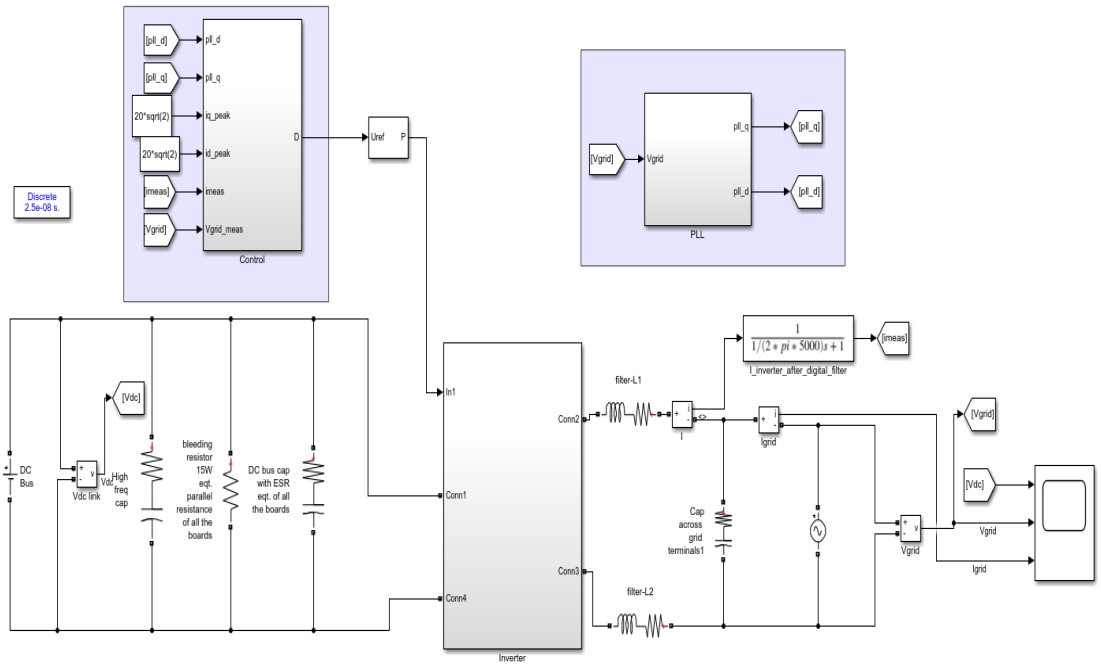
(a) Open loop current harmonics

Figure 3.18: Open loop current harmonics

3.2.2 Closed Loop Operation

3.2.2.1 First quadrant

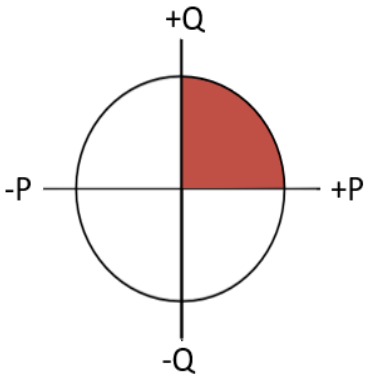
In the closed loop operation of the inverter, AC output is tied to grid and the inverter is being operated in various quadrants.



(a) Closed loop control for four quadrant operation

Figure 3.19: Closed loop control for four quadrant operation

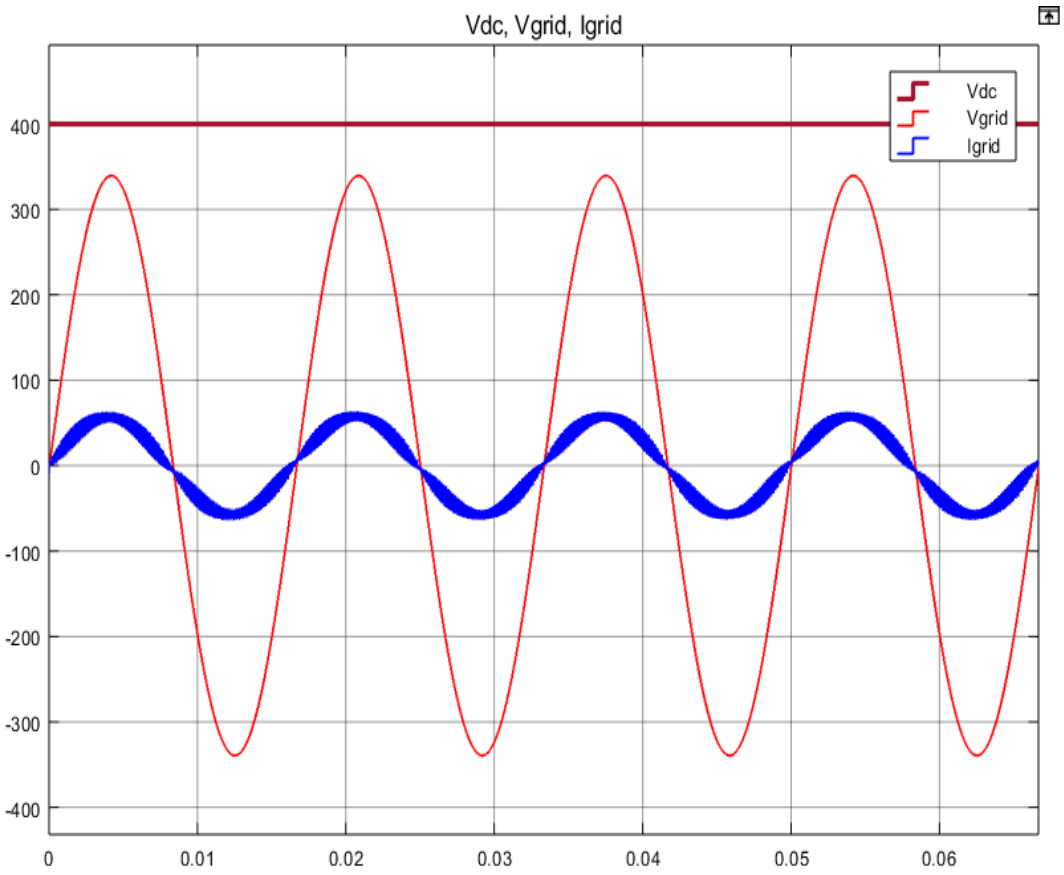
- First quadrant operation (+P, +Q)



(a) First quadrant operation

Figure 3.20: First quadrant operation

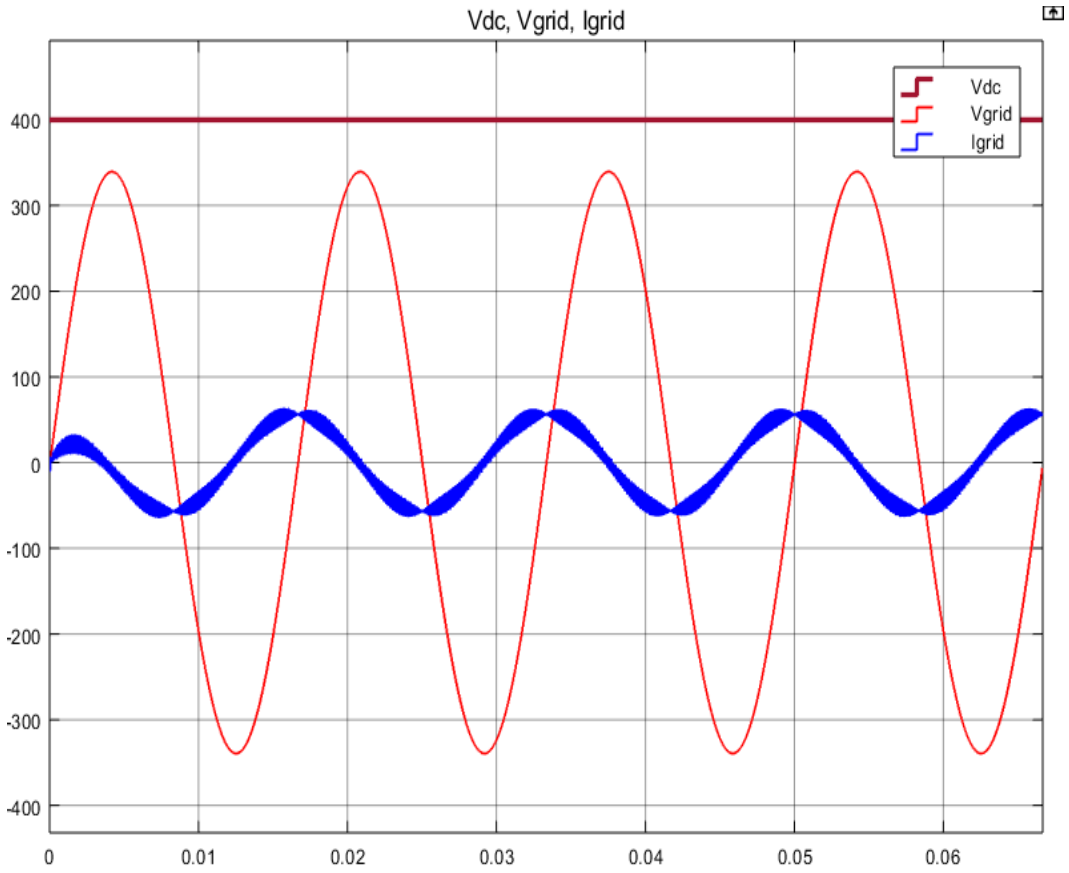
I_d=$40\sqrt{2}$, I_q=0



(a) First quadrant operation with pure active control

Figure 3.21: First quadrant operation with pure active control

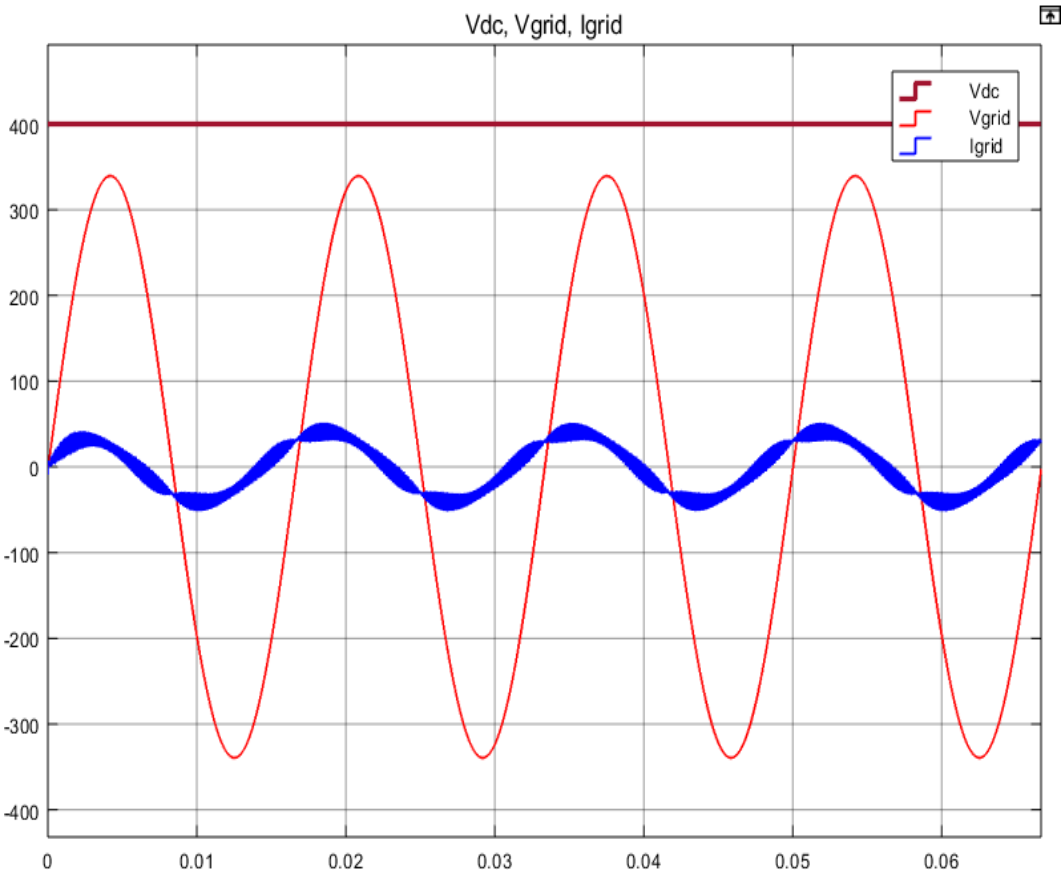
I_d=0, I_q=$40\sqrt{2}$



(a) First quadrant operation with pure reactive control

Figure 3.22: First quadrant operation with pure reactive control

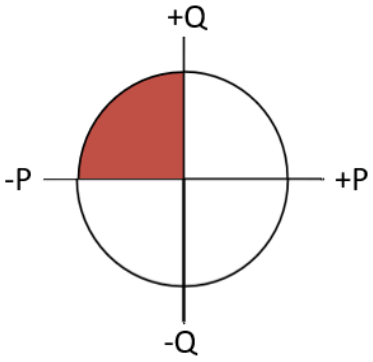
I_d=$20\sqrt{2}$, I_q=$20\sqrt{2}$



(a) First quadrant operation with combined active-reactive control

Figure 3.23: First quadrant operation with combined active-reactive control

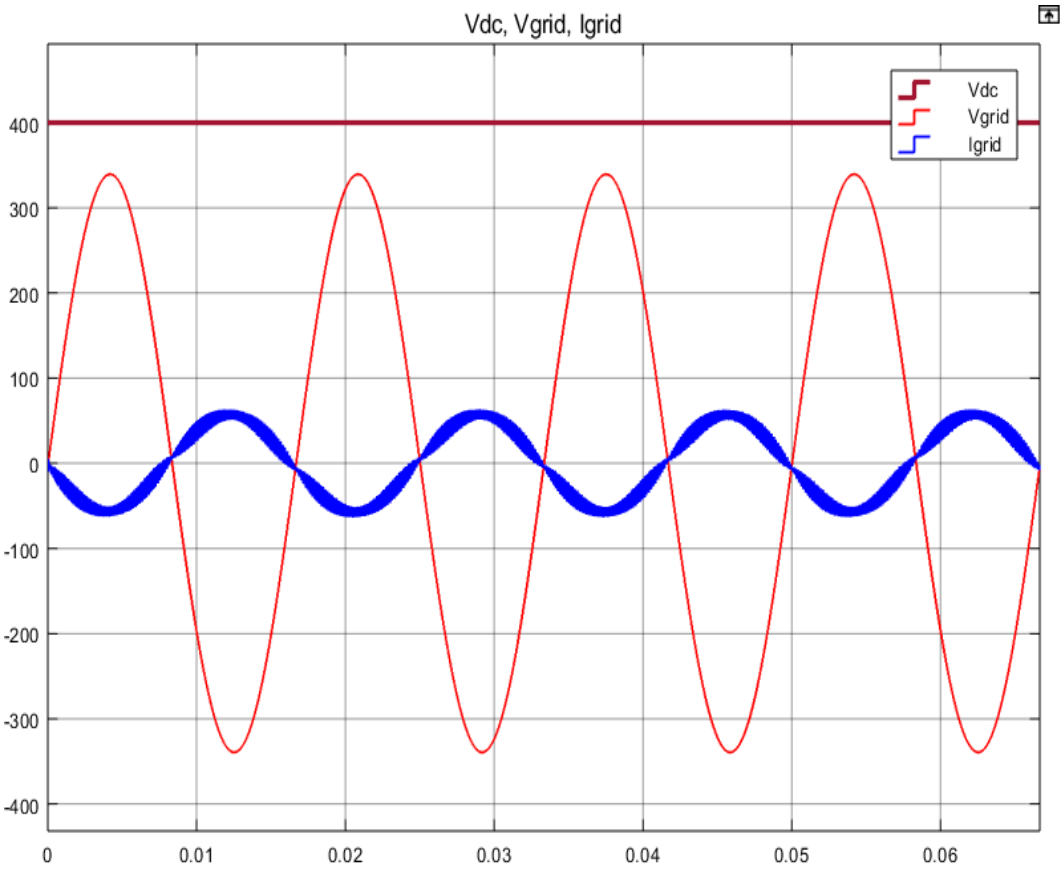
- Second quadrant operation (-P, +Q)



(a) Second quadrant operation

Figure 3.24: Second quadrant operation

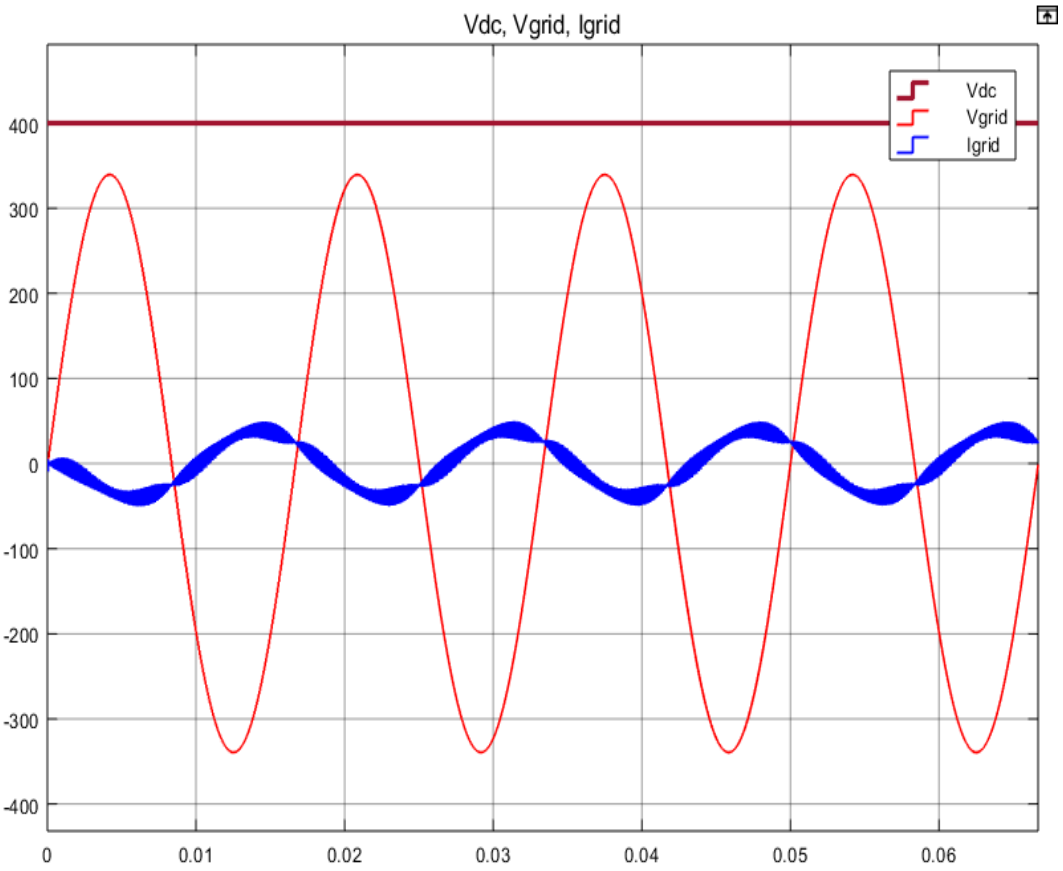
I_d=-40$\sqrt{2}$, I_q=0



(a) Second quadrant operation with active control

Figure 3.25: Second quadrant operation with active control

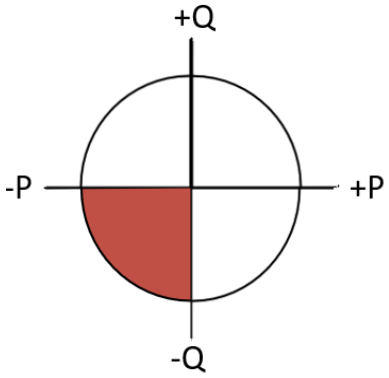
I_d=-20$\sqrt{2}$, I_q=20$\sqrt{2}$



(a) Second quadrant operation with combined active-reactive control

Figure 3.26: Second quadrant operation with combined active-reactive control

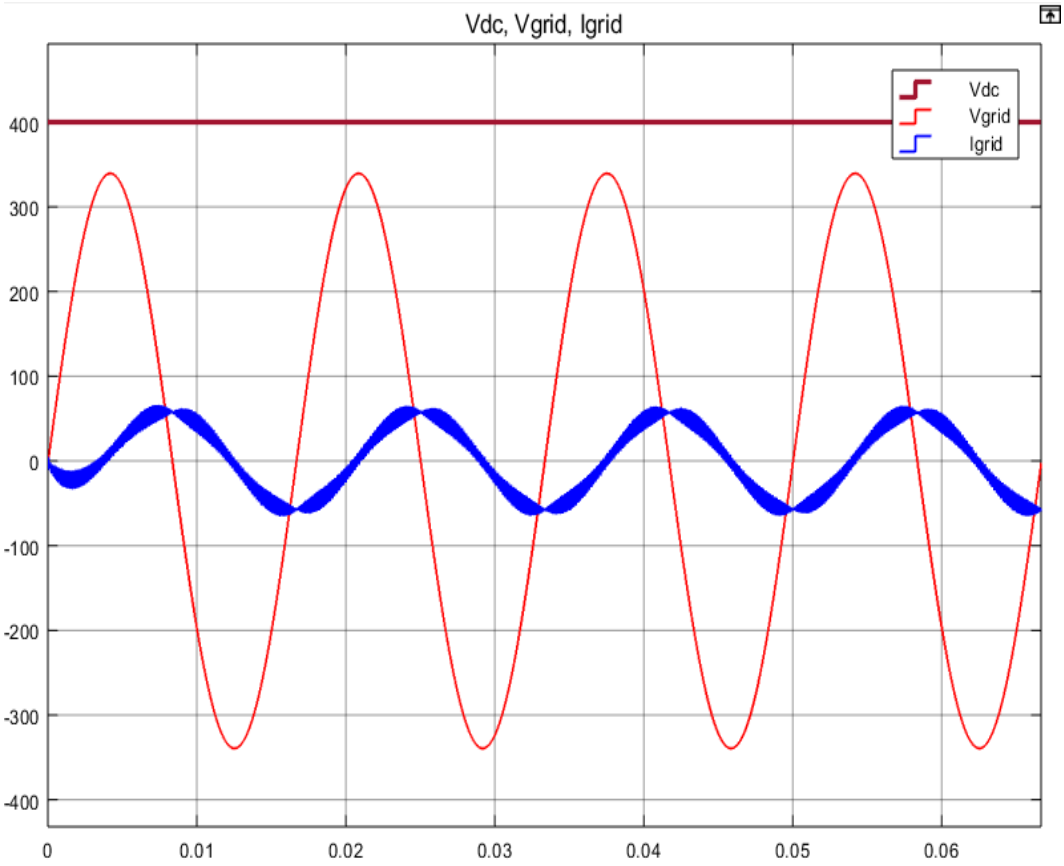
- Third quadrant operation (-P, -Q)



(a) Third quadrant operation

Figure 3.27: Third quadrant operation

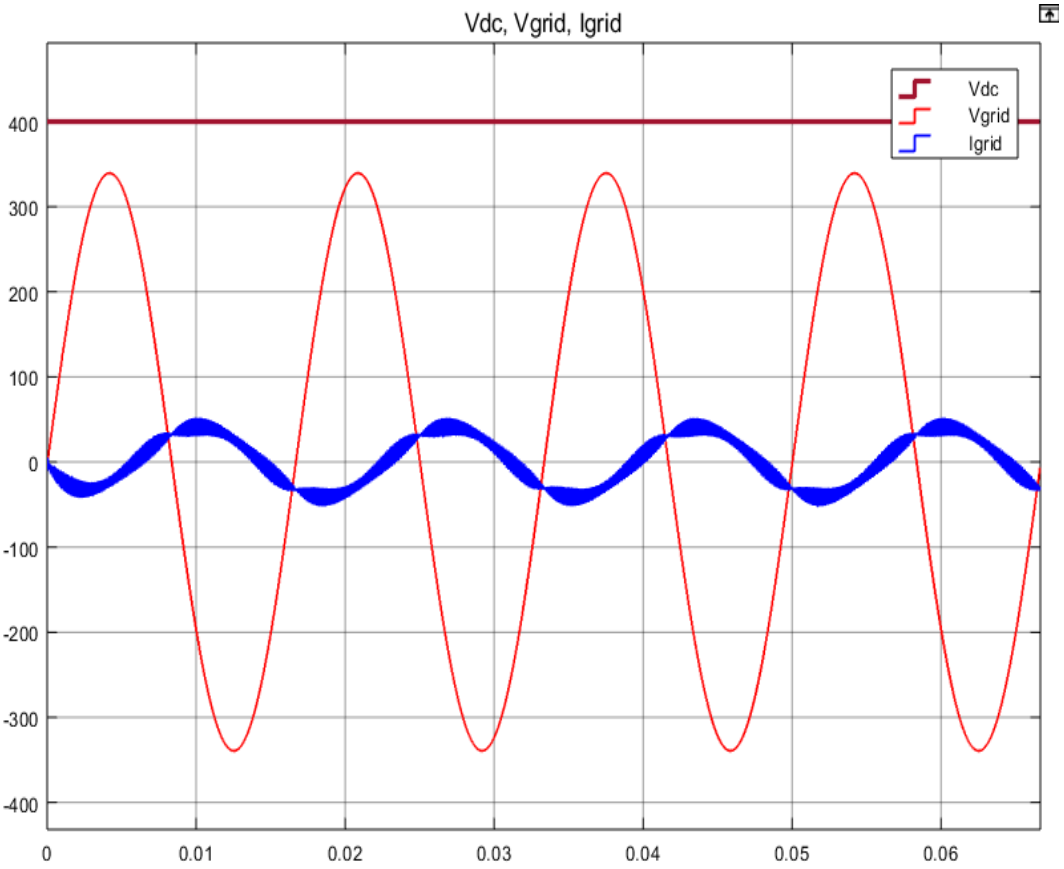
I_d=0, I_q=-40$\sqrt{2}$



(a) Third quadrant operation with reactive control

Figure 3.28: Third quadrant operation with reactive control

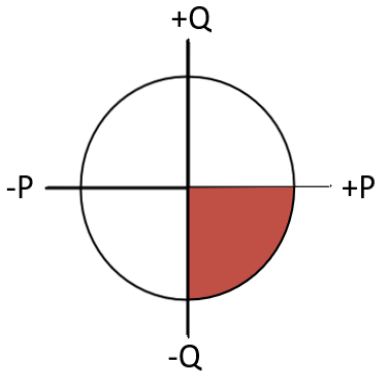
I_d=-20$\sqrt{2}$, I_q=-20$\sqrt{2}$



(a) Third quadrant operation with combined active-reactive control

Figure 3.29: Third quadrant operation with combined active-reactive control

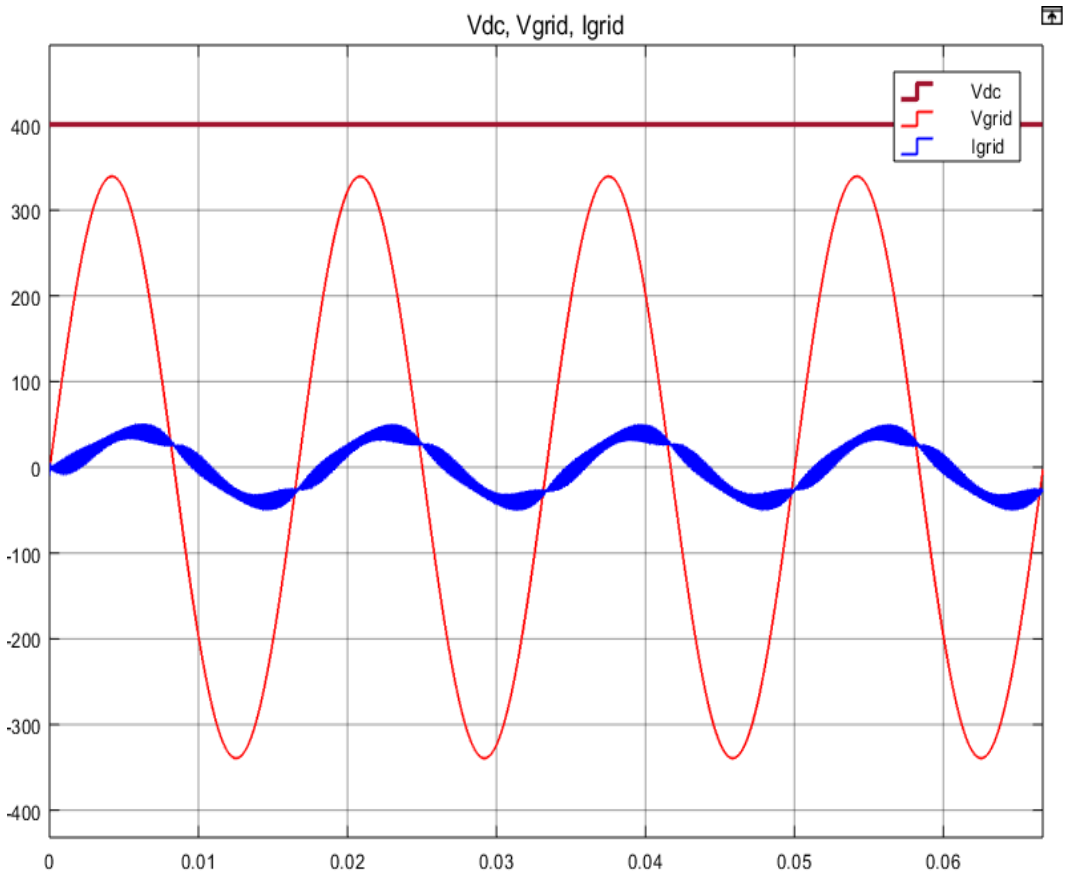
- Fourth quadrant operation (+P, -Q)



(a) Fourth quadrant operation

Figure 3.30: Fourth quadrant operation

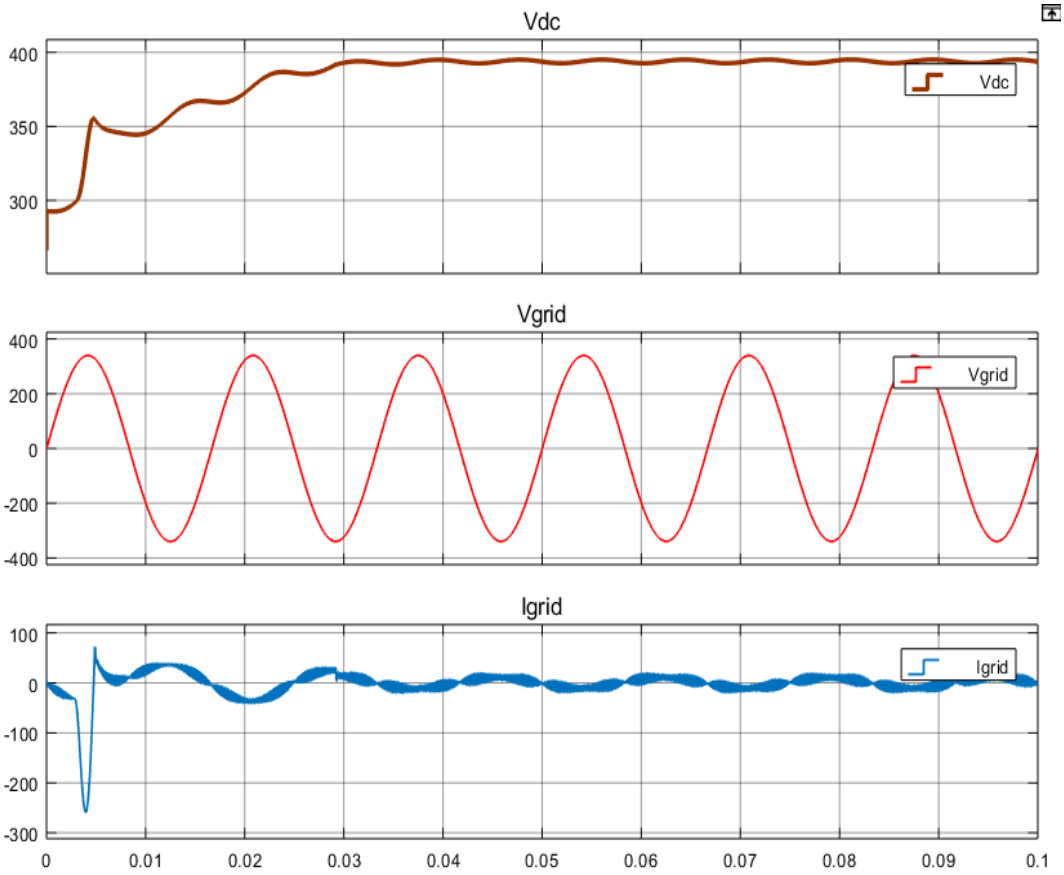
I_d=$20\sqrt{2}$, I_q=-$20\sqrt{2}$



(a) Fourth quadrant operation with combined active-reactive control

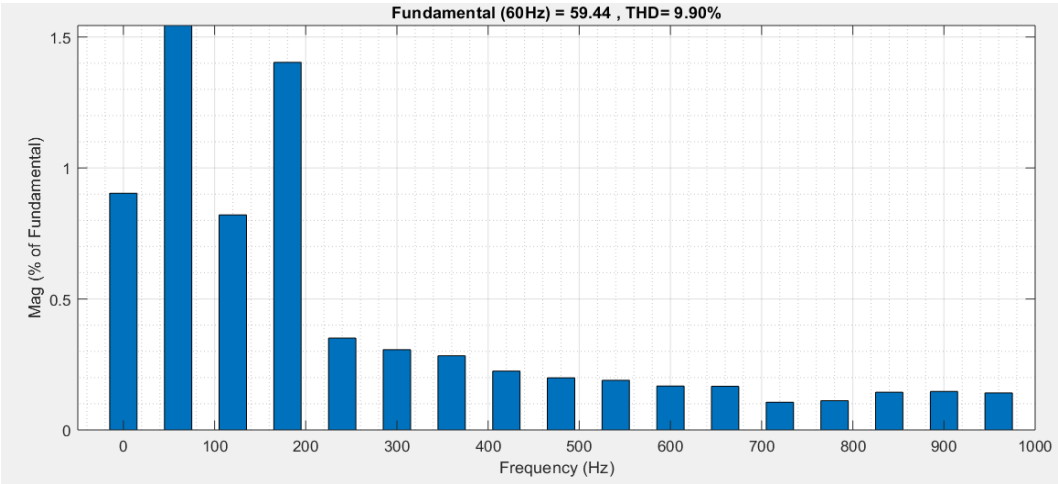
Figure 3.31: Fourth quadrant operation with combined active-reactive control

- V_{dc} regulation in closed loop



(a) V_{dc} regulation in closed loop

Figure 3.32: V_{dc} regulation in closed loop



(a) Close loop current harmonics for V_{dc} regulation in closed loop

Figure 3.33: Close loop current harmonics for V_{dc} regulation in closed loop

CHAPTER 4: HARDWARE DEVELOPMENT AND EXPERIMENTAL RESULTS

4.1 Hardware Development

4.1.1 Introduction

The hardware has been developed keeping the integrated system in mind. All the major power processing boards such as inverter, photovoltaic DC-DC converters board and battery energy storage DC-DC converters board have been developed separately. The inductors have been developed separately by winding the magnetic cores with standard gauge wires. The inductors are not employed on the main power processing board for the same reason as to make the boards less bulky. The gate drive board has been developed such that it fits nearer to the devices in vertical manner to avoid noise interference and minimize the board sizes. The DC bus capacitors have been split across the boards to make the boards lighter and easy to handle. The ratings of the PCB boards are as follows:

- PV: 2.5 KW
- BESS: 2.5 KW
- Inverter: 10 KW

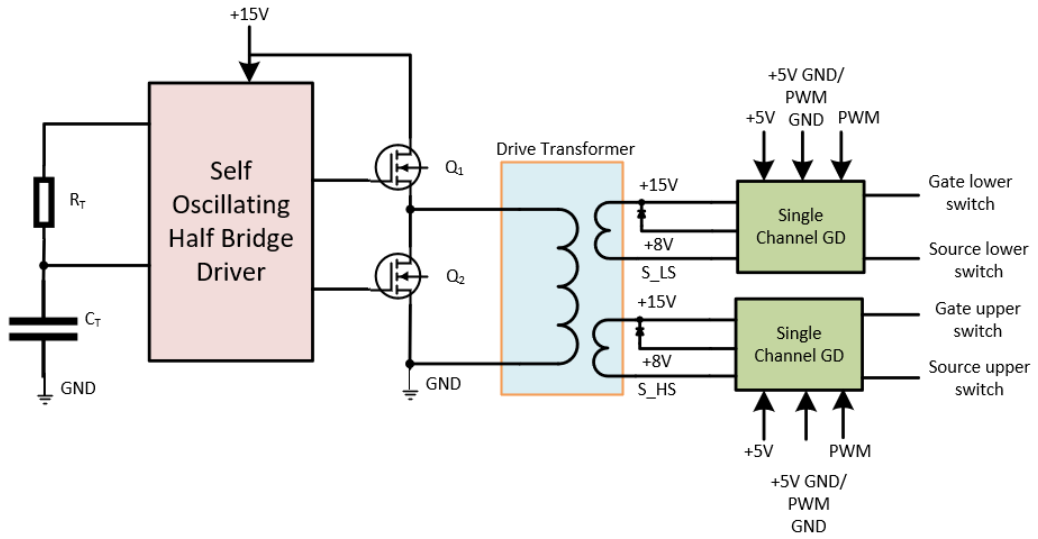
The hardware design has been developed keeping following important points in mind.

- Low harmonics
- Small magnetics
- More power density
- Less complexity
- Low cost
- Modular packaging

Selected two-level topology for the inverter allowed the flexibility to choose the controller and helped to make the board less complex. Also, to minimize several EMI issues several things have been kept in mind such as to avoid routing the housekeeping supplies for gate drive below the switching nodes and using shielded twisted pairs for the control and PWM signals. The development of all the boards have been discussed in separate sections below.

4.1.2 Gate Driver Board

A single gate drive board has been designed to accommodate two switching pulses namely upper and lower pulses as referred to the one leg of a H-bridge. Various components such as common mode chokes and filters have been used wherever necessary to minimize the propagation of noises from the switching power supplies and DC-DC converters. The schematic diagram of the gate drive board is shown below.



(a) Gate drive schematics

Figure 4.1: Gate drive schematics

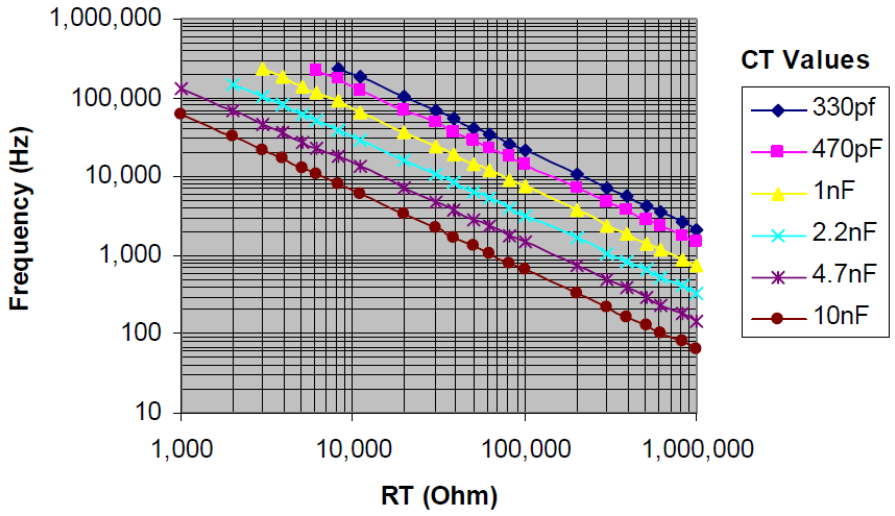
IRS 2153 from international rectifier has been used as self oscillating half bridge gate driver. It incorporates a a high voltage half-bridge gate drive with front end oscillator similar to industry standard CMOS 555 timer. The output driver features

a high pulse current buffer stage designed for minimum driver cross conduction. It has a under voltage lock-out protection mode which activates when the V_{cc} voltage is below the turn-on threshold of the integrated circuit. This mode is designed to draw very small current while in lock-out mode and guarantees the functionality of the integrated circuit before the high and low side gate drivers are activated. Under normal operating mode the frequency of oscillation can be determined from the equation $f = \frac{1}{4.53 R_T C_T}$. It is evident from the equation that the oscillating frequency can be varied to desired frequency by varying the values of R_T and C_T.

Main features of this IC are:

- The chip is designed to withstand and operate with voltages as high as 600V DC.
- Consists of an internal built-in oscillator circuit with a 50% fixed duty cycle, while its frequency can be simply determined through two external R and C components.
- Consists of a built-in high side driver network which allows a fail-proof conduction of the high-side MOSFET (upper MOSFET) with the required essential boot-strapped gate voltage.
- Allows an external shut-down feature to be enforced just by adding an additional transistor stage with the IC (Non-latched shutdown on CT pin ($1/6th V_{CC}$). This feature can be very useful for applications where an automatic current or voltage regulation is crucial.
- The chip also includes a Micro-power start-up feature which assures guaranteed initialization even under relatively minimal voltage and current conditions.
- An internal dead time feature ensures perfect separation between the outputs for fail proof operations.
- All the the pin-outs are electrostatic discharge protected internally for safeguarding the chip against static voltages during packaging and handling.

Based on different R_T and C_T values below diagram shows the frequency variation.



(a) Frequency variation w.r.t. R_T and C_T values

Figure 4.2: Frequency variation with R and C values in a self-oscillating gate driver

The output of the IC is two switching pulses which drives two small MOSFETs. The output pulses are then fed to a drive transformer for galvanic isolation and minimizing noise interference propagation to the single channel gate drivers. Drive transformers are also used here to split one output into two. These two outputs then supplies the required power to drive two single channel gate drivers.

Single channel gate driver IC is a general purpose MOSFET gate driver. The integrated galvanic isolation between control input logic and driving output stage grants additional safety. Its wide input voltage supply range support the direct connection of various signal sources like DSPs and microcontrollers. The separated rail-to-rail driver outputs simplify gate resistor selection, save an external high current bypass diode and enhance dV/dt control. The separated rail-to-rail driver outputs simplify gate resistor selection, save an external high current bypass diode and enhance dV/dt control. With bipolar supply the driver is typically operated with a positive voltage of 12 V at VCC2 and a negative voltage of -8V at GND2 relative to the source of the MOSFET. Negative supply can help to prevent a dynamic turn on of the MOS-

FET. For unipolar supply configuration the driver is typically supplied with a positive voltage of 12 V at VCC2. In this case, careful evaluation for turn off gate resistor selection is recommended to avoid dynamic turn on.

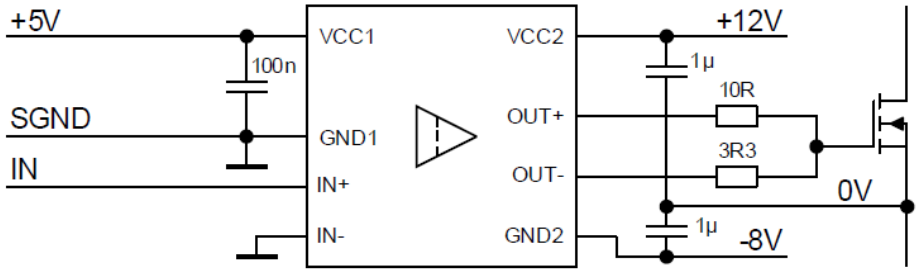


Figure 4.3: Single channel gate driver IC schematic

Following major components have been used for the gate drive[14]:

Table 4.1: List of gate drive board main components.

S.No.	Components	Quantity
1	Self oscillating half-bridge driver	1
4	Small signal transistor	2
2	Drive Transformer	1
3	Single channel gate driver IC	2

- Self oscillating half-bridge driver: It is an integrated 50% duty cycle oscillator and half-bridge driver IC in a single package. Dead-time can be controlled through proper selection of CT and can range from 50ns to 200ns. Internal soft-start increases the pulse width during power up and maintains pulse width matching for the high and low outputs throughout the start up cycle. The IR2085S initiates a soft start at power up and after every overcurrent condition. Undervoltage lockout prevents operation if VCC is less than 7.5V.

Figure 4.4: Self oscillating half bridge driver

- Small signal transistor: It is small signal N-channel MOSFET rated 30V, 7.1A. This MOSFETs has been used for switching purposes to generate pulses at the input of the drive transformer. The above mentioned gate driver is used to drive this device.

Figure 4.5: Small signal MOSFET

- Drive Transformer: To provide galvanic isolation and minimizing noise interference propagation to the single channel gate drivers.

Figure 4.6: Drive transformer

- Single channel gate driver IC: It is a general purpose MOSFET gate driver.The integrated galvanic isolation between control input logic and driving output stage grants additional safety.

Figure 4.7: Single channel gate driver IC

Below picture shows the PCB design of a gate drive board.

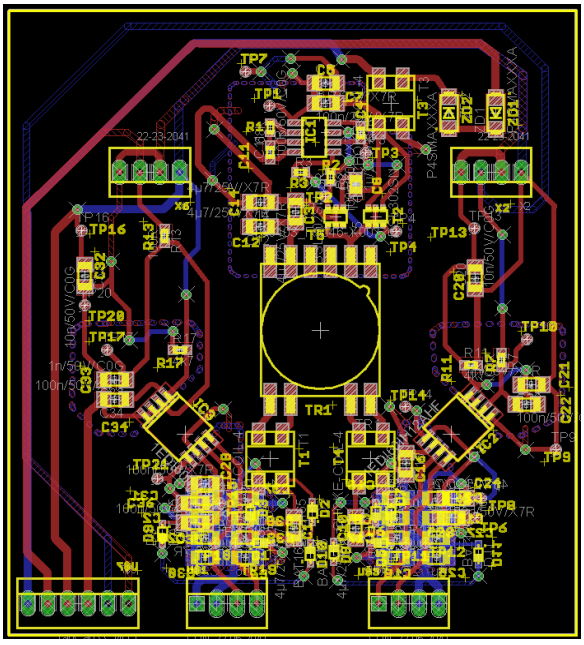


Figure 4.8: Gate drive board PCB layout

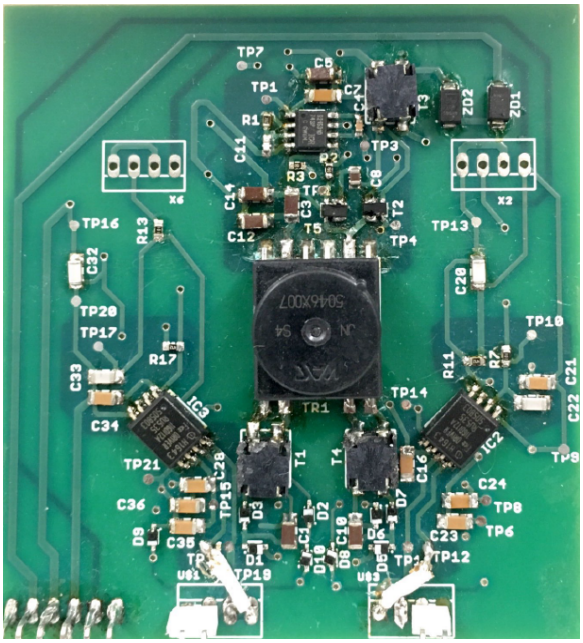


Figure 4.9: Gate drive PCB board

4.1.3 Inverter Board

Inverter is the main component of the hardware system. The rated voltages and power are 400V DC link voltage, 240V AC output with 10kW rating. Schematic diagram for the inverter is as shown in the figure below.

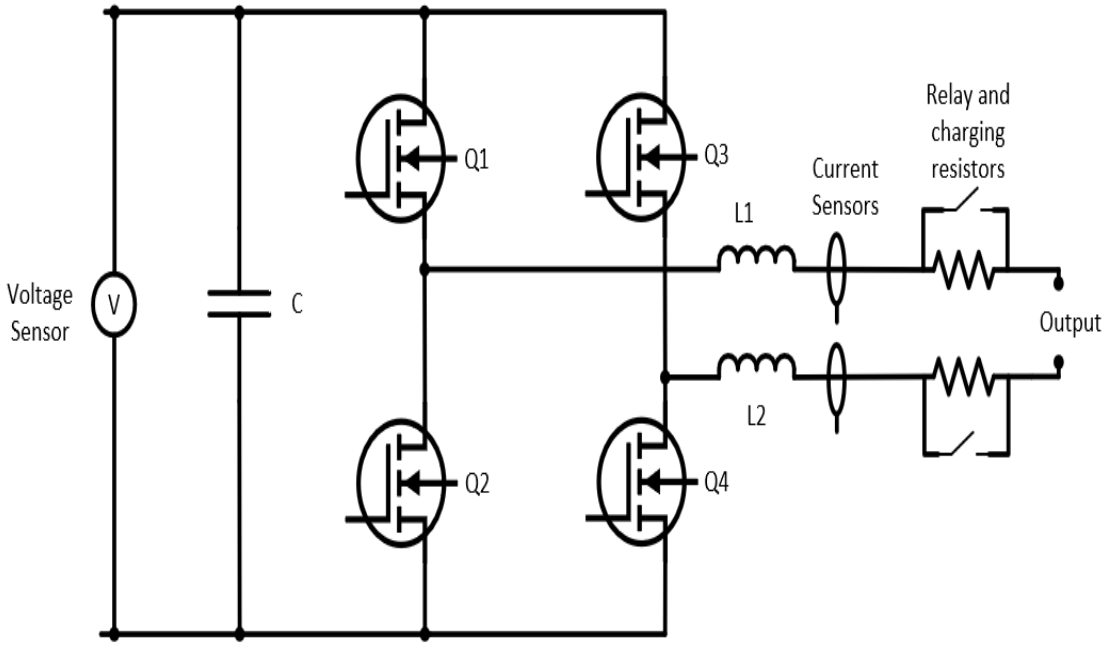


Figure 4.10: Inverter board schematic

The inverter can be broken down in the three parts namely:

- Pre-charging circuit
- Power processing circuit and DC bus
- House-keeping supplies

We will discuss all the above sections one by one.

4.1.3.1 Pre-charging circuit

The pre-charging circuit consists of two charging resistors in parallel with charging relays. The pre-charging resistors limit the charging current drawn to charge the DC bus when it is connected to the grid. The relays are closed when the DC bus is almost charged to the peak of the applied AC voltage at the output terminals. These two charging relays thus remain in line during normal operation to avoid any ohmic losses in the circuit because they have very small contact resistance.

4.1.3.2 Power processing circuit and DC bus

The power processing circuit consists of two silicon carbide MOSFETs which constructs a two-level full H-bridge inverter. Each silicon device is consists of one leg of a H-bridge with two upper and lower MOSFETs with its anti-parallel diode. DC bus consists of three numbers of parallel connected DC capacitors each 1000 μF. These capacitors are screw mounted capacitors rated at 650V. Bleeding resistors have been provided to discharge the DC bus capacitors when the circuit is not in function.

4.1.3.3 House-keeping supplies

The housekeeping supply scheme is shown below in the figure for the inverter board.

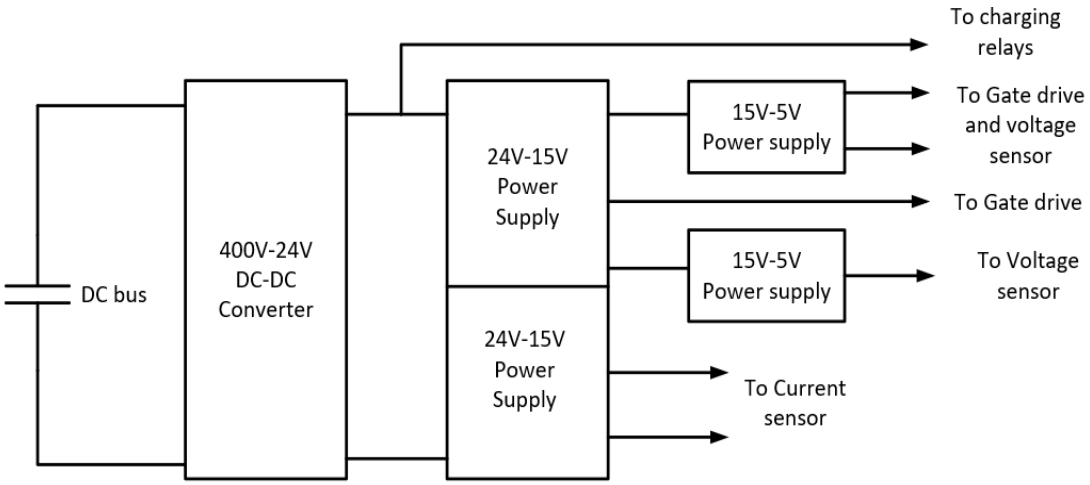


Figure 4.11: House-keeping supply for the inverter

The figure shows the layout for the house-keeping power supplies. Initially the inverter baords needs 24V external house-keeping supplies to power up the gate drives, voltage and current sensors. When the DC bus is charged up to 200V, the 400V-24V converter starts to operate. This converter is sufficiently rated to supply the house-keeping supplies of other power processing boards also such as PV and BESS board. This 400V-24V power supply further powers two numbers of 24V-15V power supply which supplies the gate drive boards and current sensors. One of the 24V-15V power supply powers two different 15V-5V power supplies which gives the required voltage

and power to the gate drives and voltage sensors.

Below table shows the main components of the inverter board[14].

Table 4.2: List of main components of inverter board.

S.No.	Componets	Quantity
1	DC voltage sensor	1
2	AC current sensors	2
3	DC link capacitors	3
4	Pre-charging relays	2
5	400V-24V DC-DC converter	1
6	24V-15V DC-DC converter	2
7	15V-5V DC-DC converter	2
8	SiC MOSFET	2

- DC voltage sensors: Broadcom - C870 series

  The Broadcom ACPL-C87B/C87A/C870 voltage sensors are optical isolation amplifiers designed specifically for voltage sensing. Its 2V input range and high 1-GΩ input impedance, makes it well suited for isolated voltage sensing requirements in electronic power converters applications, including motor drives and renewable energy systems. In a typical voltage sensing implementation, a resistive voltage divider is used to scale the DC-link voltage to suit the input range of the voltage sensor. A differential output voltage that is proportional to the input voltage is created on the other side of the optical isolation barrier.

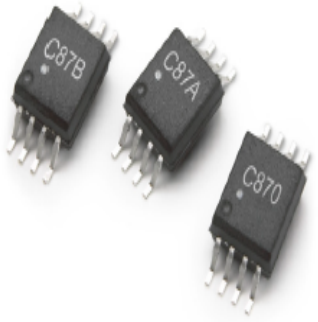


Figure 4.12: DC bus voltage sensor

- AC current sensors: LEM - Current Transducer LAH 50-P

  It is a isolated current sensor which can measure up to 50A of current with high immunity to external interferences.

Figure 4.13: AC current sensor

- DC link capacitors: Nippon - ERHA651LGC102MDA0M

  It is a 1000 μF 650V DC screw mounted capacitor.

Figure 4.14: DC link capacitor

- Pre-charging relays: Panasonic - HE1AN-W-DC24V-Y6

  It is a high capacity, compact size modular relay normally used for solar inverters. It is rated 48A with a contact resistance of the order of mΩ and takes very low power to operate.

Figure 4.15: Charging relays

- 400V-24V DC-DC converter: Vicor - DCM4623xD2H31E0yzz

  This is a 500W high power density, highly efficient isolated and regulated DC-DC voltage converter which can operate at the input voltage range of 200V-420V.

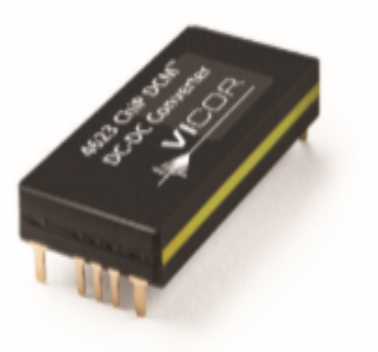


Figure 4.16: 400V-24V DC-DC converter

- 24V-15V DC-DC converter: CUI INC - PRD15-Q24-S15

  It is a 15W highly efficient low ripple, low noise isolated voltage converter with over voltage, over current, short circuit and over temperature protection.

Figure 4.17: 24V-15V DC-DC converter

- 24V-15V DC-DC converter: CUI INC - PDM2-S24-S15-S

  It is a 2W isolated highly efficient DC-DC voltage converter in a small package with short-ciruit protection.

Figure 4.18: 24V-15V DC-DC converter

- 15V-5V DC-DC converter: RECOM - RI-1505S

  It is a highly efficient, isolated 2W converters which occupies minimum board space.

Figure 4.19: 15V-5V DC-DC converter

- SiC MOSFET: Infineon FF11MR12W1M1-B11 It is a half bridge 1200V, 100A SiC MOSFET device.

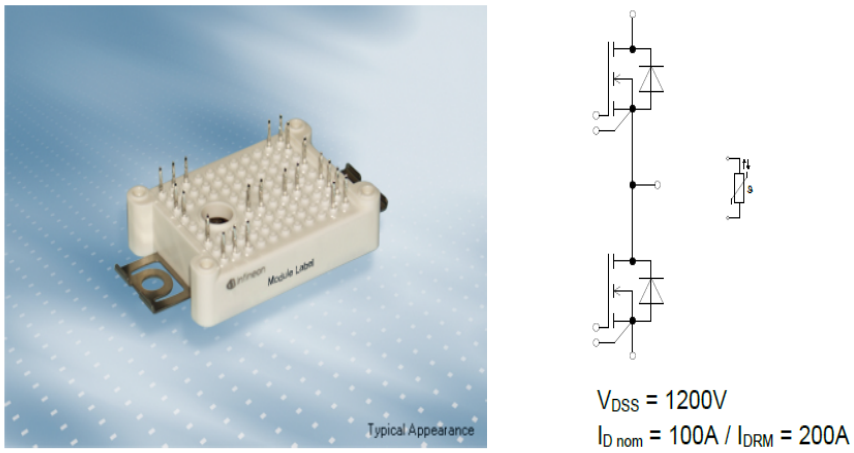


Figure 4.20: SiC MOSFET

Below picture shows the PCB design of the inverter.

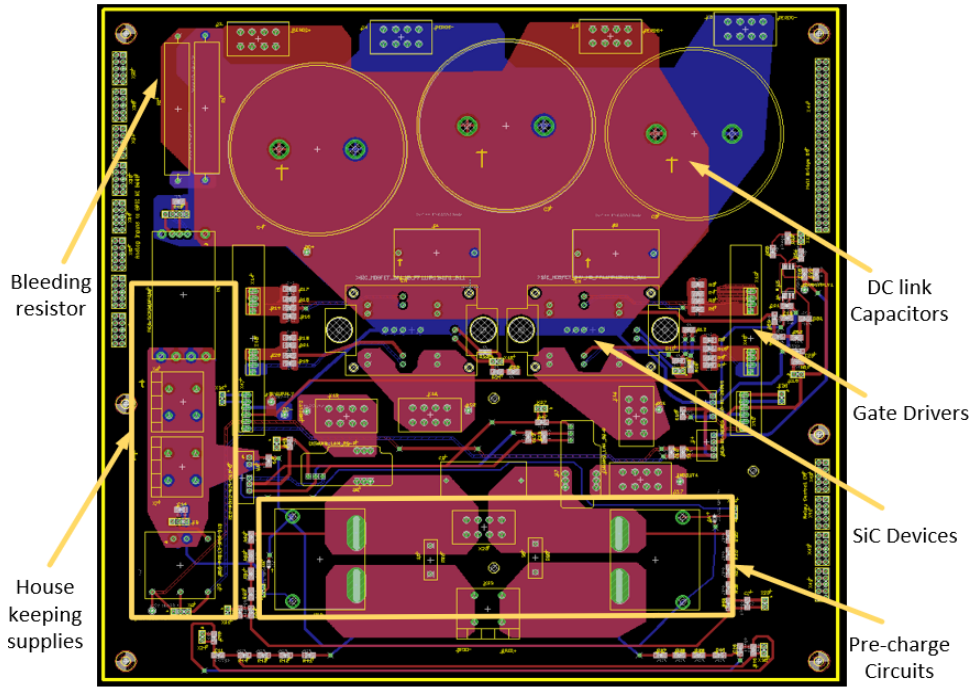


Figure 4.21: Inverter board PCB layout

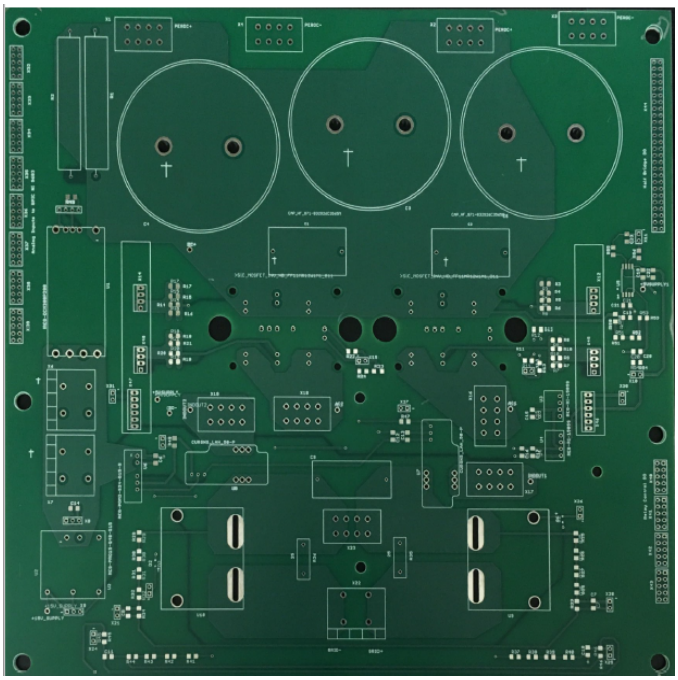


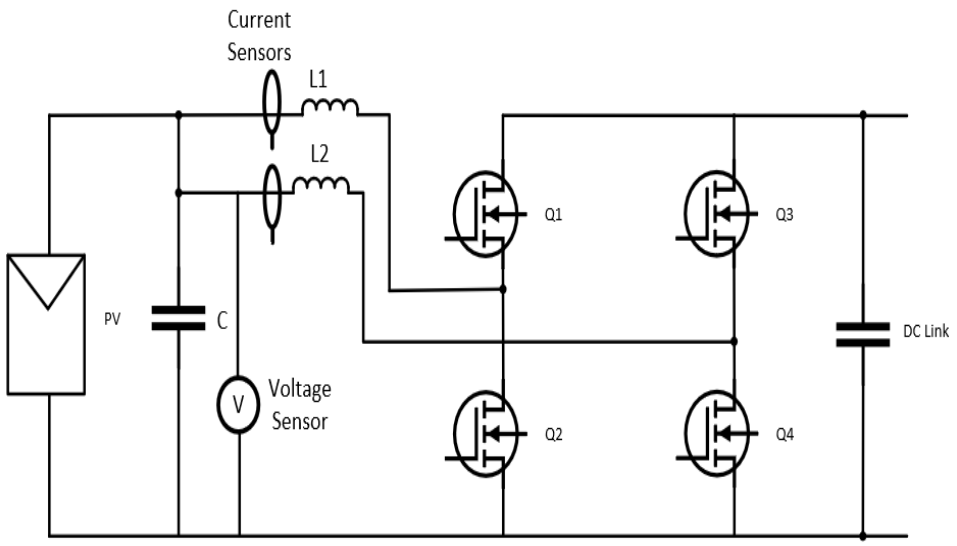
Figure 4.22: Inverter PCB board

4.1.4 PV and BESS Boards

The PV and BESS boards consists of two DC-DC converters. In PV board two parallel DC-DC boost converters share the current. It also acts as a impedance matching circuit for MPPT algorithm for PV board. Two DC current sensor and one DC voltage sensors have been used as shown in the figure.

Two parallel DC-DC converter also helps to split the inductors to make the PV setup light weight. One DC bus capacitor of 1000 μF which is same as inverter DC bus capacitor is used. The DC bus capacitor rating is 650V DC.

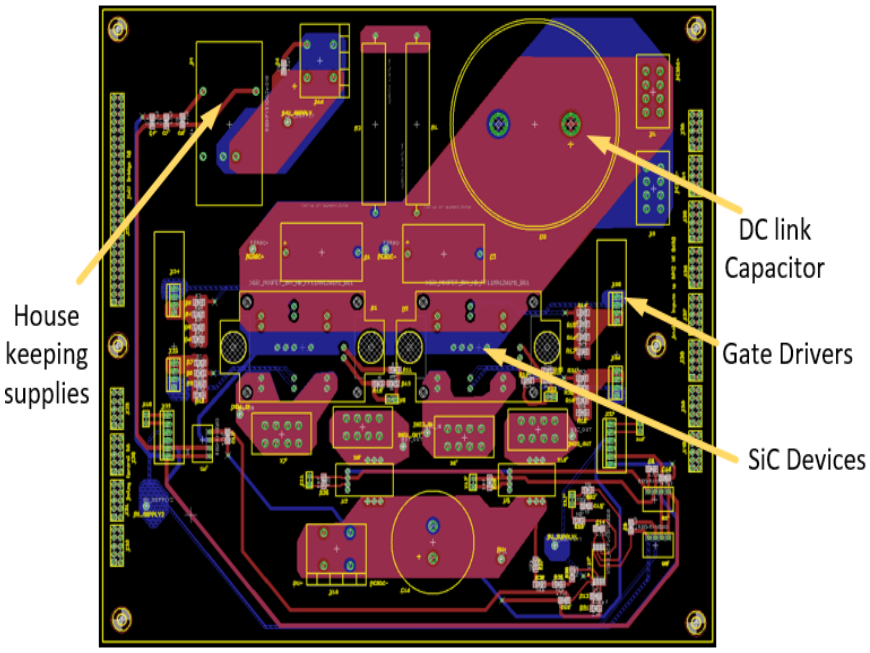
The PV board schematics is shown below:



(a) PV board schematic

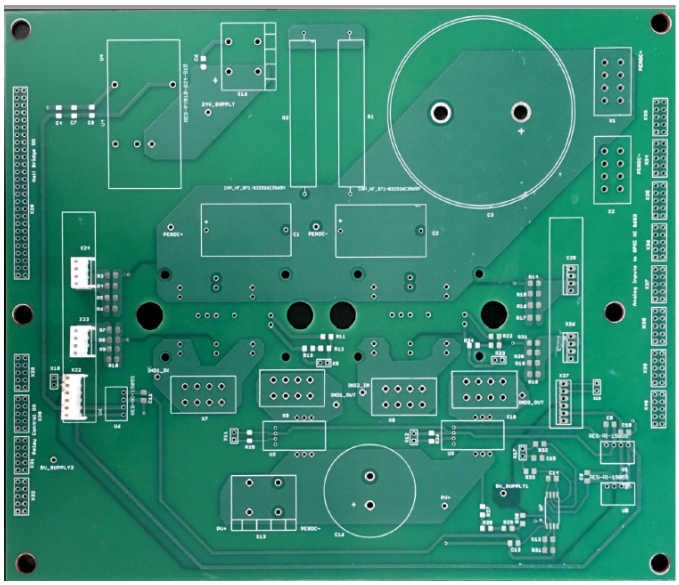
Figure 4.23: PV board schematic

The PCB design for the PV board is shown in the figure below.



(a) PV board PCB layout

Figure 4.24: PV board PCB layout



(a) PV PCB board

Figure 4.25: PV PCB board

Major components of the PV board have been listed below[14].

Table 4.3: List of main components of PV board.

S.No.	Componets	Quantity
1	DC voltage sensor	1
2	DC current sensors	2
3	DC link capacitors	1
4	24V-15V DC-DC converter	1
5	15V-5V DC-DC converter	2
6	SiC MOSFET	2

All the components are same as inverter board except DC current sensors and 24V-15V DC-DC converters.

- DC current sensors: LEM - Current transducer LTSR 15-NP This current sensor

is suitable for upto 15A DC current applications. It is an isolated and compact DC current sensor and requires 5V housekeeping supply.

(a) DC current sensors for PV and BESS board

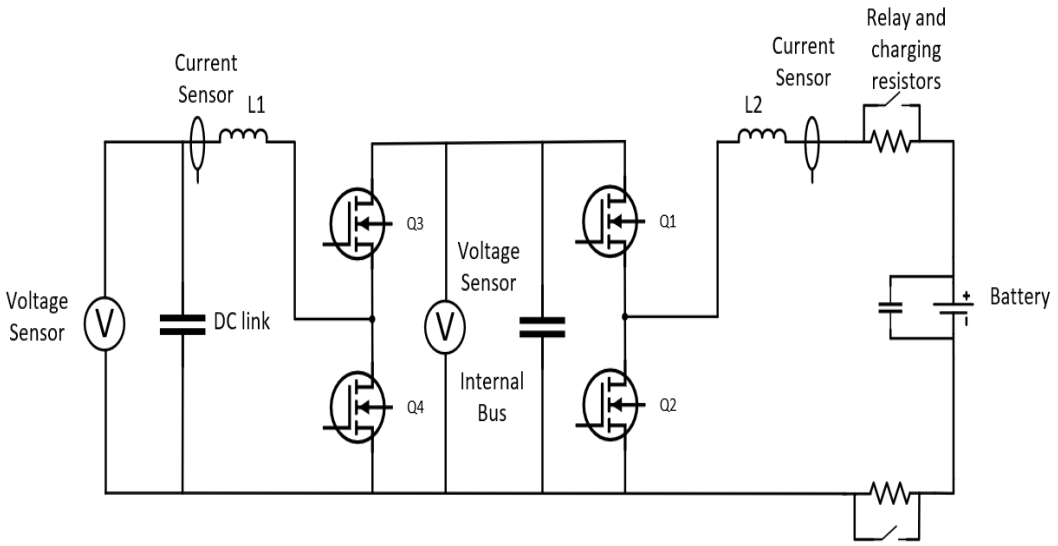
Figure 4.26: DC current sensors for PV and BESS board

- 24V-15V DC-DC converters: CUI INC PYB10-Q24-S15 This is a 10W isolated power supply with short circuit and over-voltage protection.

(a) 24V-15V power supply for PV and BESS board

Figure 4.27: 24V-15V power supply for PV and BESS board

Similarly, BESS board has two DC-DC converters the schematics is shown below.



(a) BESS board schematic

Figure 4.28: BESS board schematic

Two DC-DC converters can work as buck or boost converters depending on the charge or discharge mode of the battery. Two current sensors and two voltage sensors have been used as shown in the figure. All the components used are same as PV board except the charging relays.

The main components of BESS board has been listed in the table below[14].

Table 4.4: List of main components of BESS board.

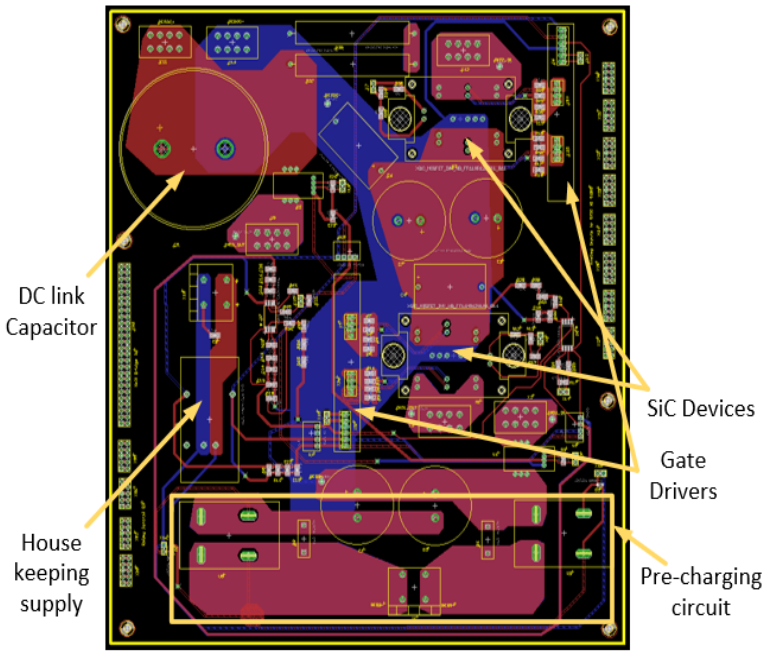
S.No.	Componets	Quantity
1	DC voltage sensor	2
2	DC current sensors	2
3	DC link capacitors	1
4	24V-15V DC-DC converter	1
5	15V-5V DC-DC converter	2
6	Charging relays	2
7	SiC MOSFET	2

- Charging relays: OMRON - Z4382-ND This is a 400V 15A DC relay with low contact resistant and takes very small power to operate. It requires 24V supply to operate.

(a) BESS charging relay

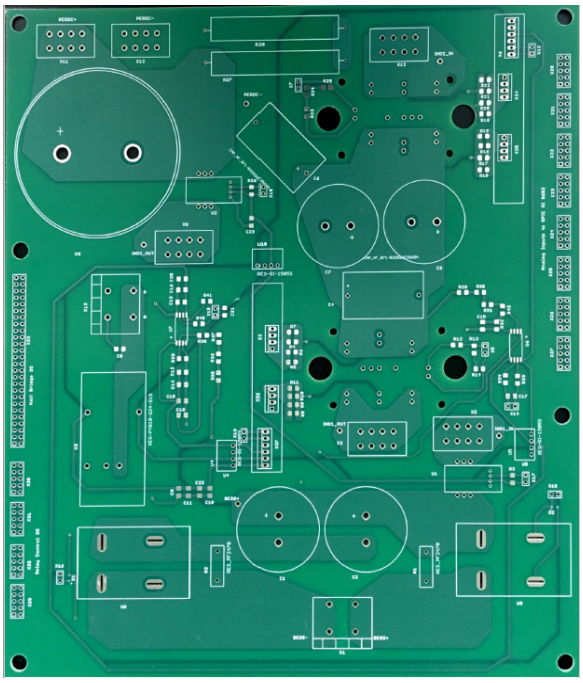
Figure 4.29: BESS charging relay

Below figure shows the PCB design of BESS board.



(a) BESS board PCB layout

Figure 4.30: BESS board PCB layout



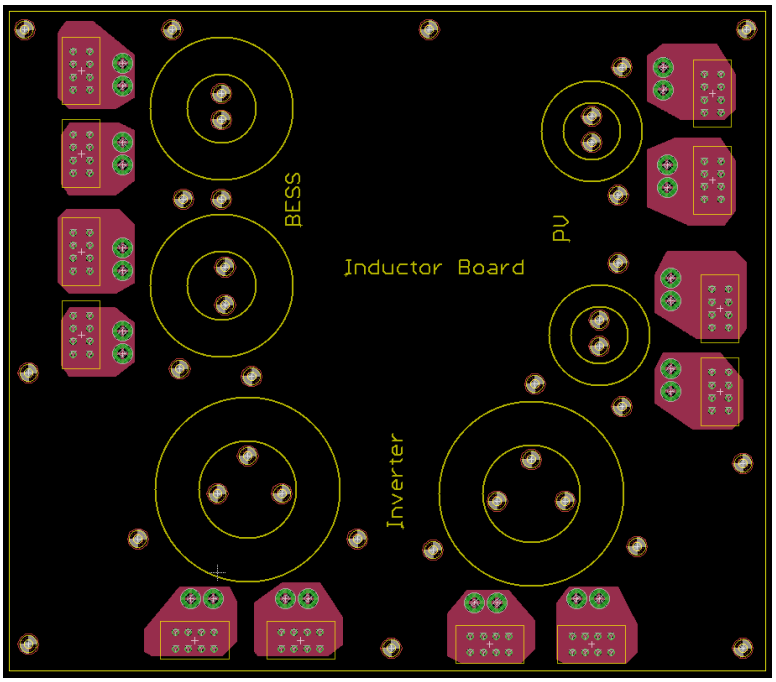
(a) BESS PCB board

Figure 4.31: BESS PCB board

4.1.5 Inductor Board

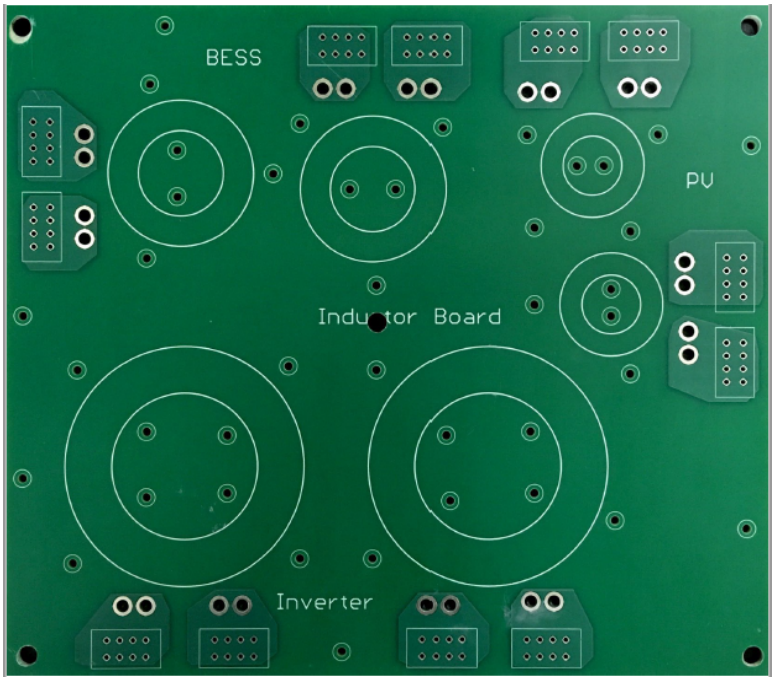
The inductor board has been developed separately to accomodate all the major power processing circuits inductors. Due to higher switching frequency used for SiC devices, the magnetics are light-weight. All the inductors have been manually wound with standard guage wires.

Below figure shows the PCB design of the inductor board.



(a) Inductor board PCB layout

Figure 4.32: Inductor board PCB layout



(a) Inductor PCB board

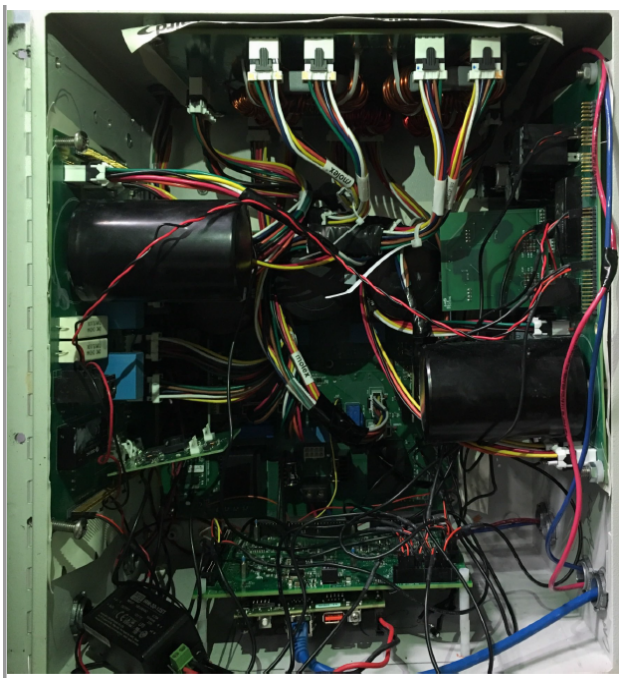
Figure 4.33: Inductor PCB board

The inductors values used for different power processing circuits are as follows:

Table 4.5: List of inductance values of different boards.

S.No.	Power processing system	Values	Quantity
1	Inverter	23 μH	2
2	BESS	423 μH	2
3	PV	309 μH	2

Below picture shows overall development of the hardware setup:



(a) Hardware inside the enclosure

Figure 4.34: Hardware inside the enclosure

(a) Hardware inside the enclosure with heatsinks attached

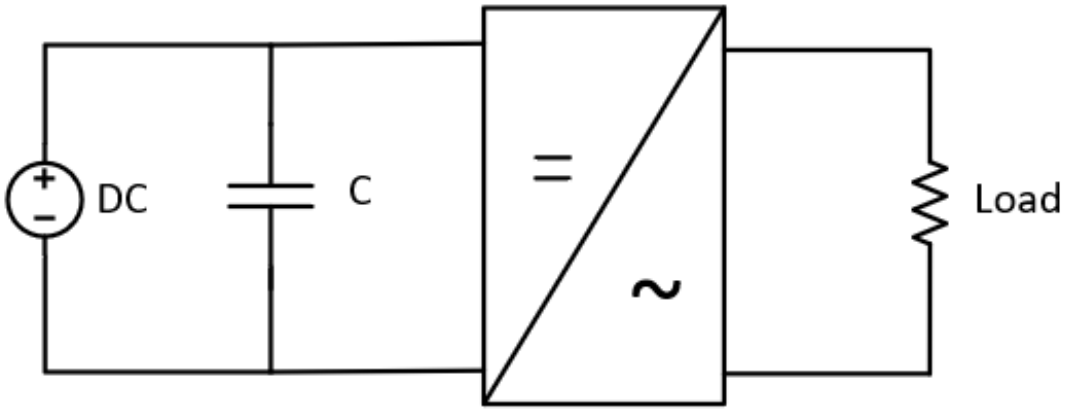
Figure 4.35: Hardware inside the enclosure with heatsink attached

4.2 Experimental Results

The whole setup inverter, BESS and PV board have been integrated and tested at the rated DC bus voltage. The experimental results are as follows:

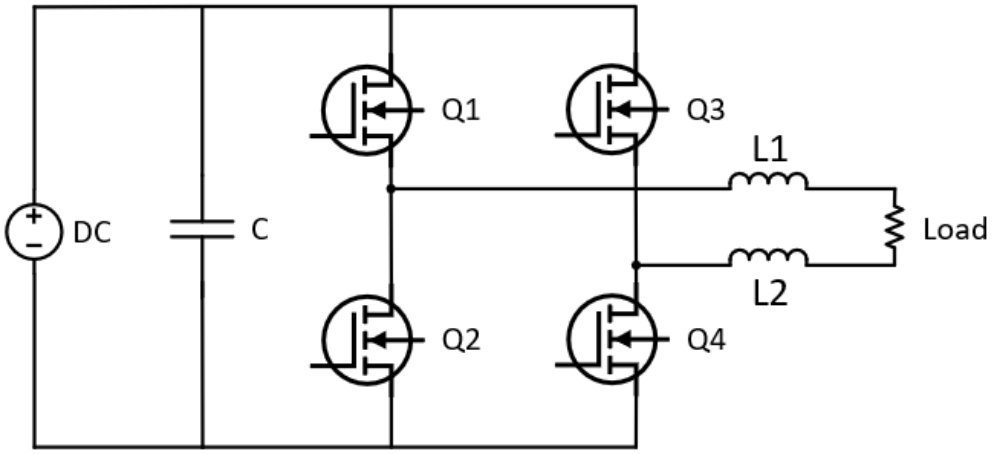
- Open loop test of the inverter

  The open loop test was performed with a 400V power supply. 400V was applied at the DC link and unipolar PWM modulation is used in open loop. A 88Ω is applied at the AC output terminals.



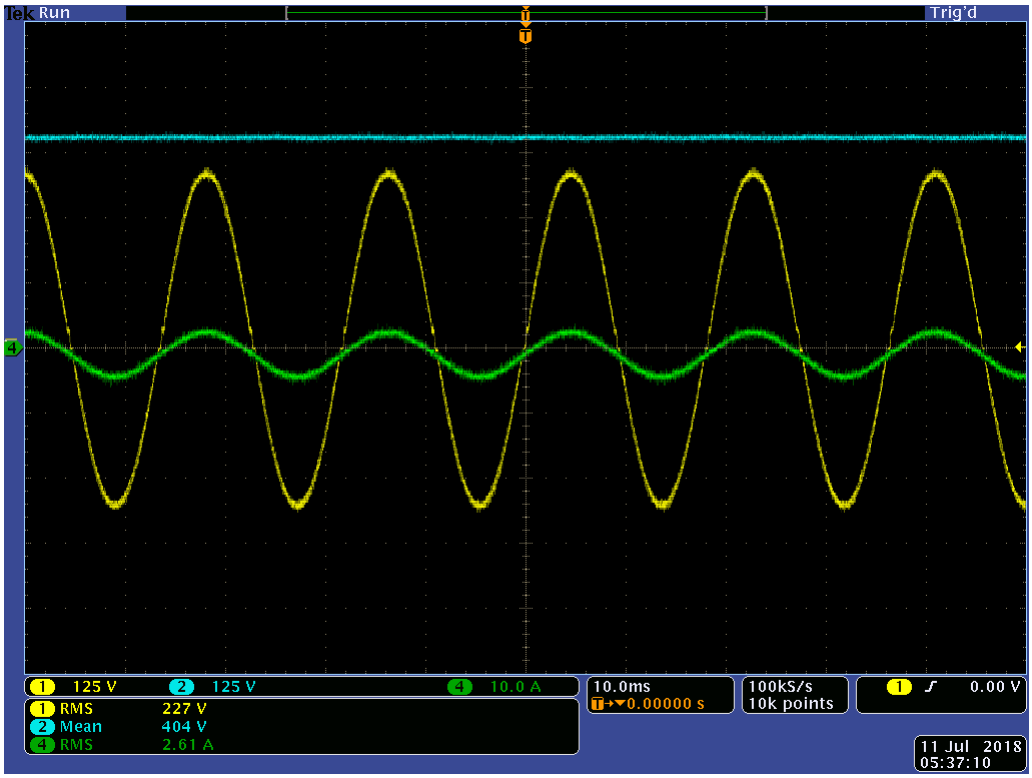
(a) Open loop inverter test general schematic

Figure 4.36: Open loop inverter operation general schematic



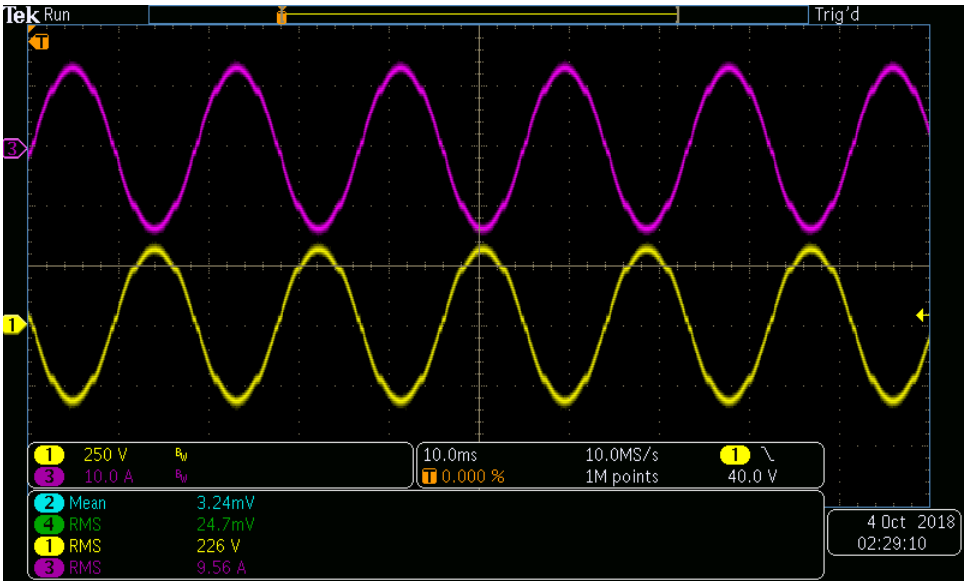
(a) Open loop inverter test schematic

Figure 4.37: Open loop inverter test schematic



(a) Yellow: Inverter output voltage, Green: load current, Blue: DC bus voltage

Figure 4.38: Open loop inverter operation at 500W

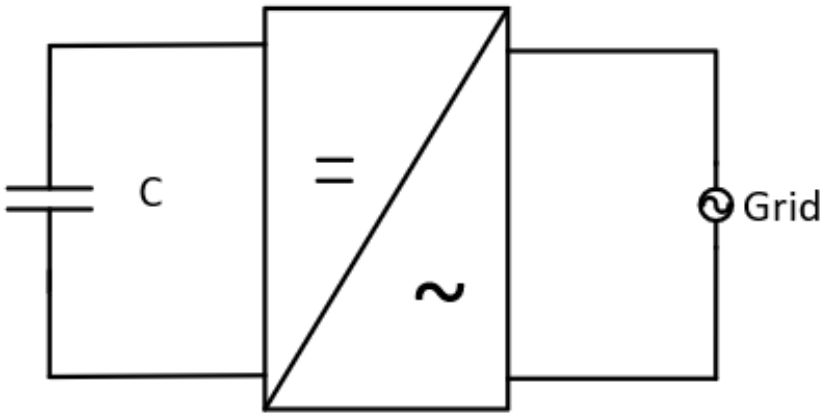


(a) Yellow: Output voltage, Pink: load current

Figure 4.39: Open loop inverter operation at 2.2kW

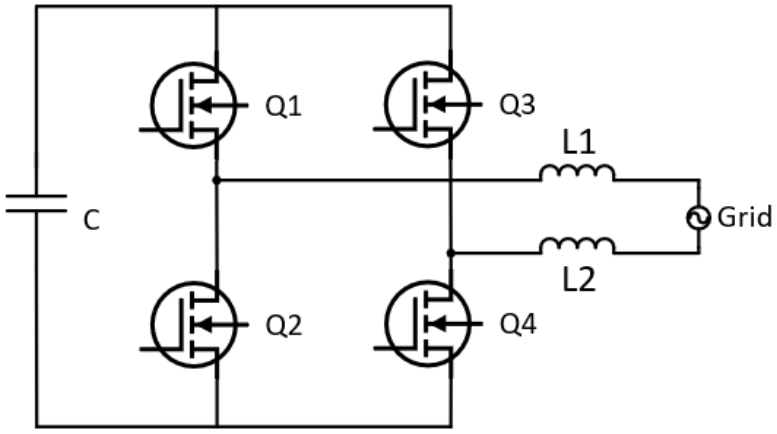
- DC voltage regulation without any load at the DC bus

  The test has been performed by connecting a 240V AC supply at the AC terminals of the inverter. The controls are applied in such a way that the DC voltage is being maintained at 400V.



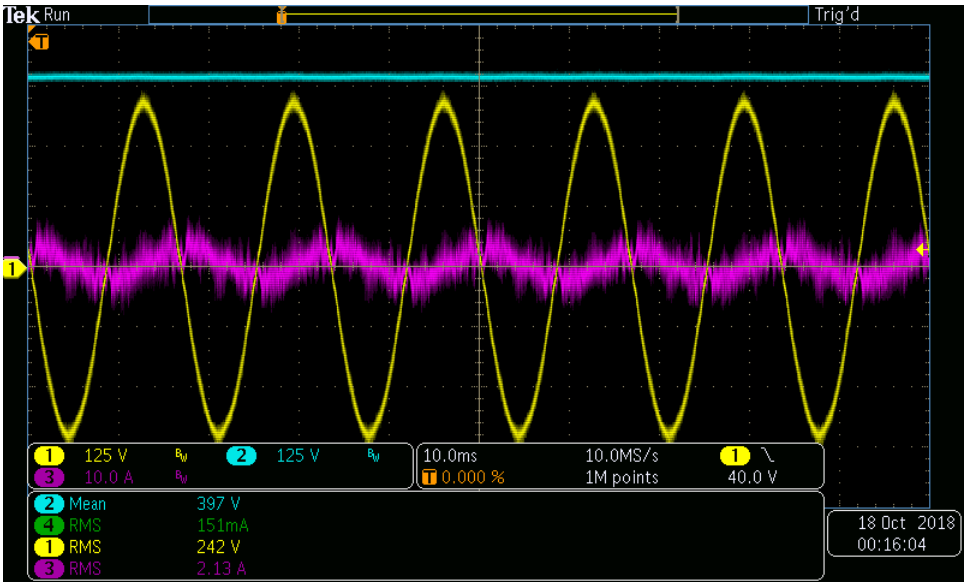
(a) V_{dc} regulation from grid general schematic

Figure 4.40: V_{dc} regulation from grid without any load at DC bus



(a) V_{dc} regulation from grid general schematic

Figure 4.41: V_{dc} regulation from grid without any load at DC bus

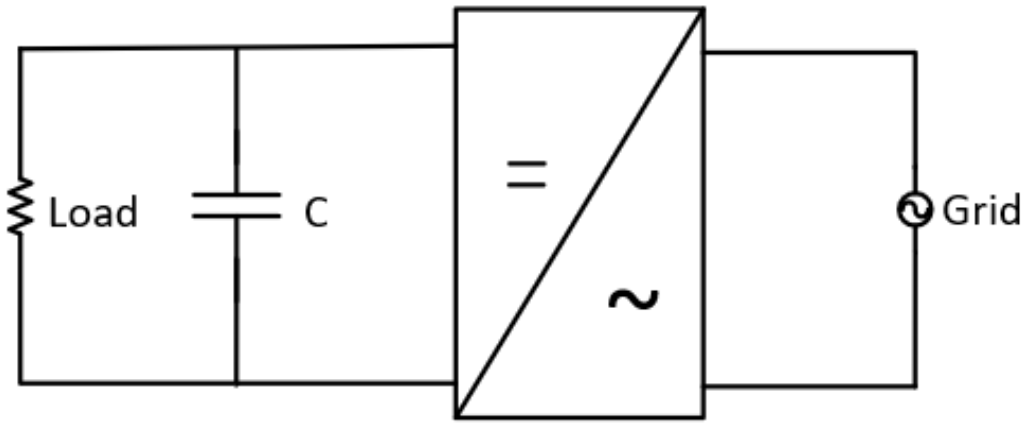


(a) Yellow: Grid voltage, Pink: Grid current, Blue: DC bus voltage

Figure 4.42: V_{dc} regulation from grid without any load at DC bus

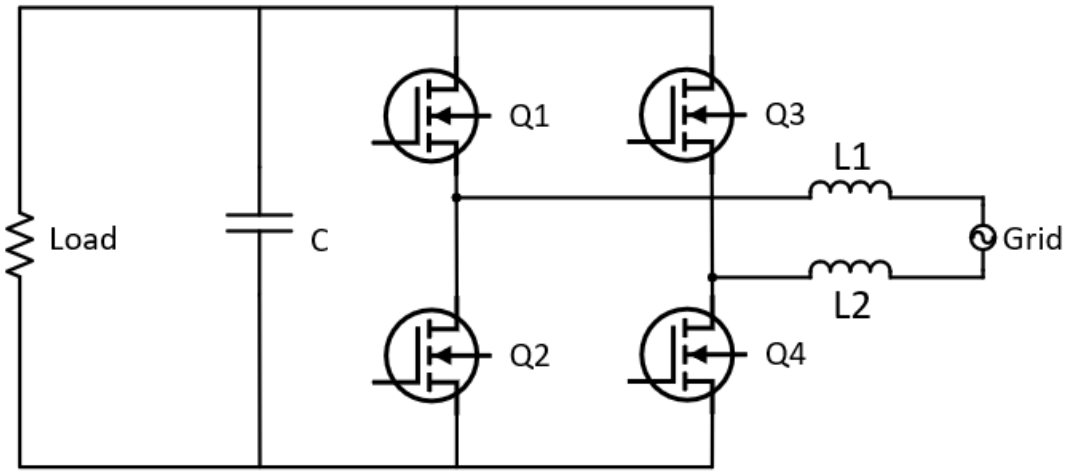
- DC voltage regulation with load at the DC bus

  To simulate the battery charging from the grid, the DC bus terminals were loaded with 88Ω load and the controls were applied to maintain the DC link at 400V.



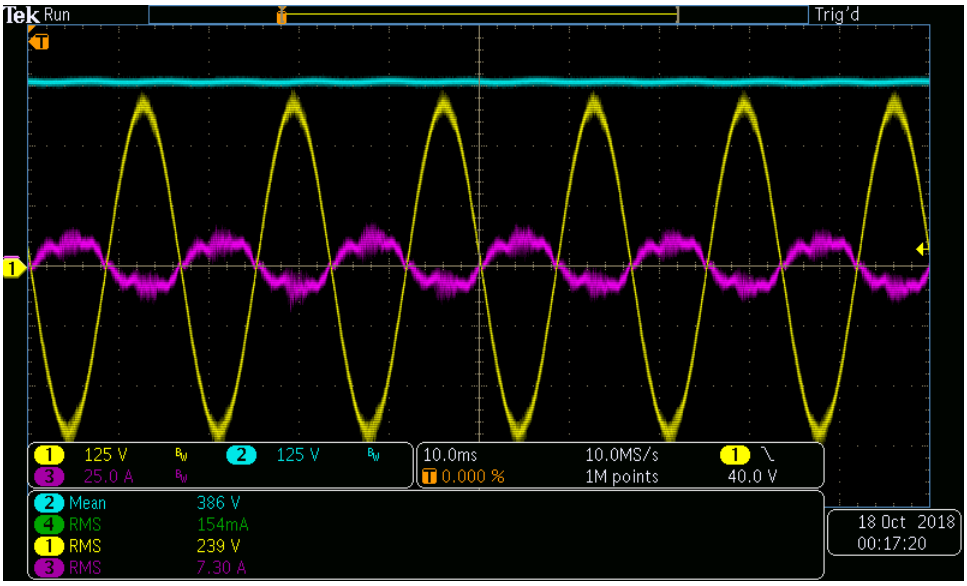
(a) V_{dc} regulation from grid general schematic

Figure 4.43: V_{dc} regulation from grid with load at DC bus



(a) V_{dc} regulation from grid general schematic

Figure 4.44: V_{dc} regulation from grid with load at DC bus

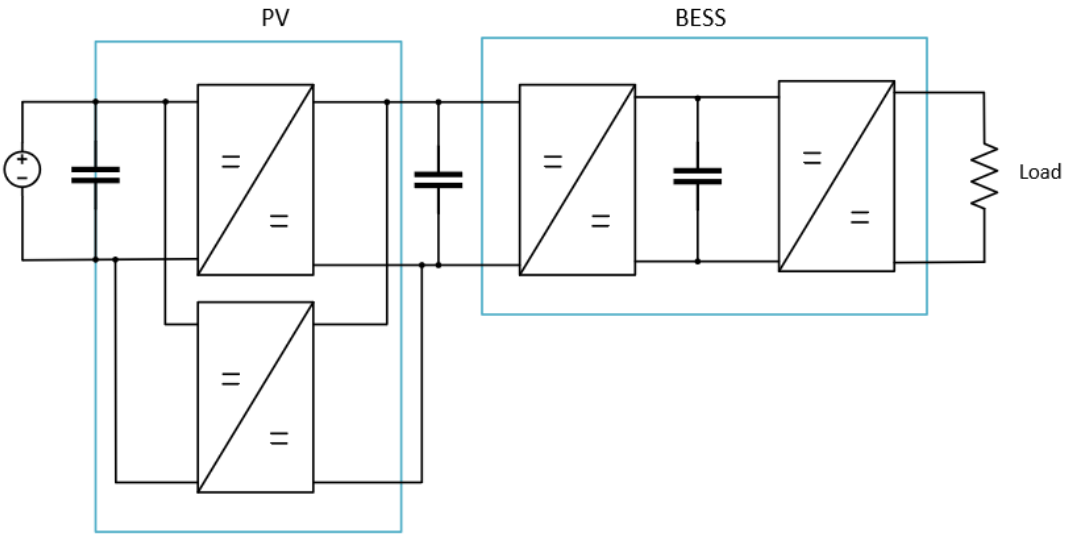


(a) Yellow: Grid voltage, Pink: Grid current Blue: DC bus voltage

Figure 4.45: V_{dc} regulation from grid with 88 ohms load at DC bus

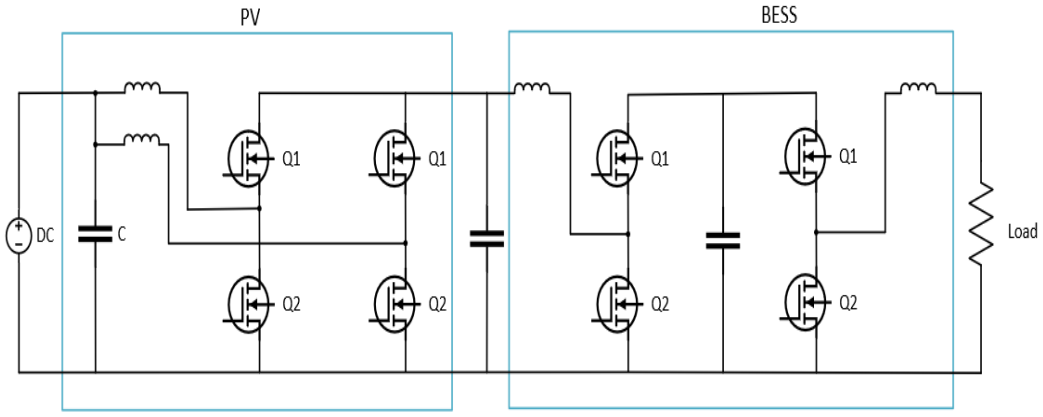
- Battery charging from PV

  The battery in open loop is being charged by the PV. Charging action is being simulated by the load at battery terminals. PV board is fed from the DC power supply.



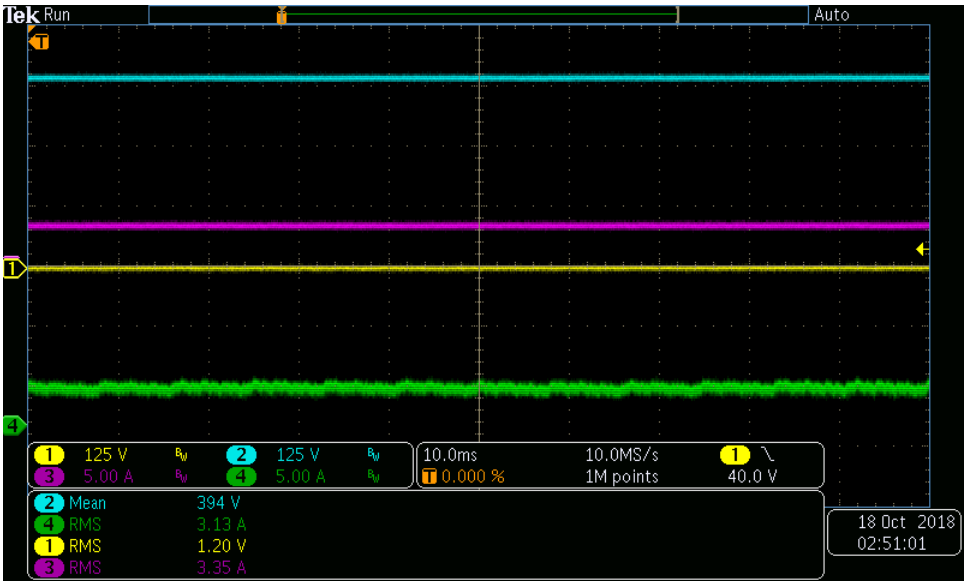
(a) Battery charging from Photovoltaic module

Figure 4.46: Battery charging from Photovoltaic module



(a) Battery charging from Photovoltaic module

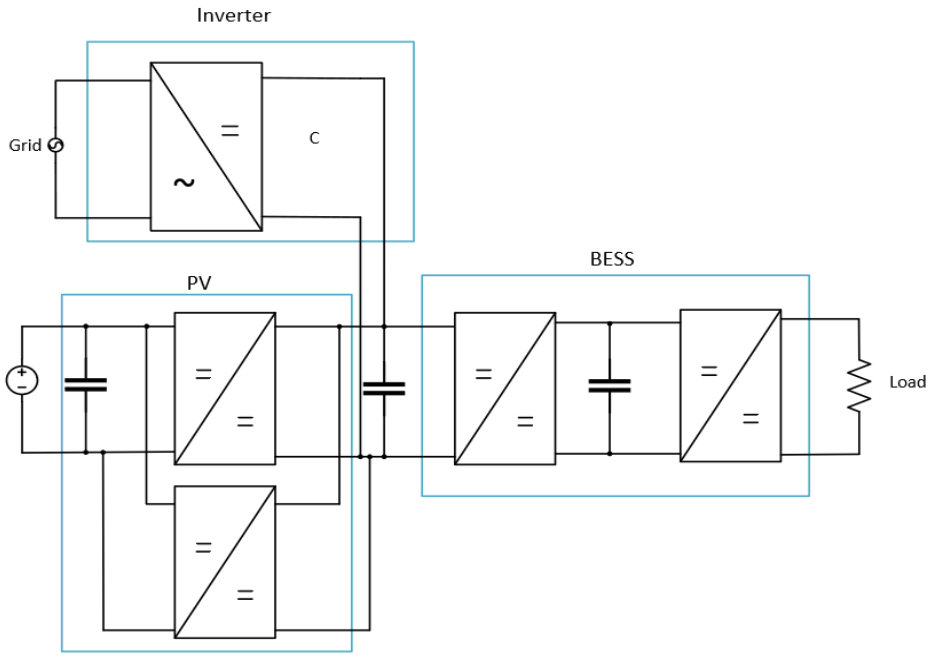
Figure 4.47: Battery charging from Photovoltaic module



(a) Green: DC Power supply current at input terminals, Pink: Battery charging current, Blue: DC bus voltage

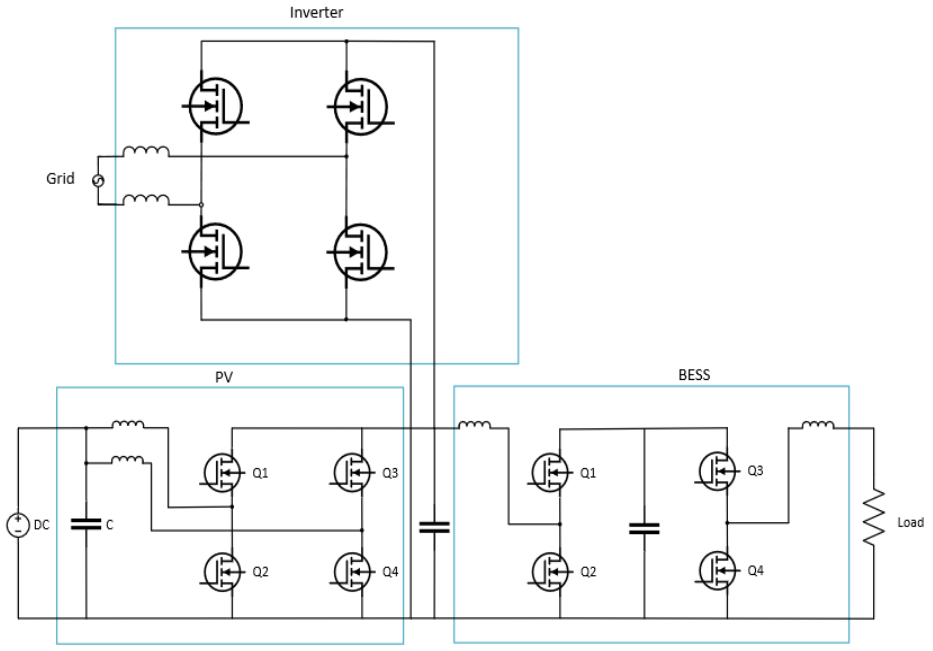
Figure 4.48: Battery charging from Photovoltaic module

- Battery charging from photovoltaic module with grid-tie The battery is being fed from the PV board with the DC link voltage being maintained at 342V. Since the peak of AC voltage is more than the DC voltage, the anti-parallel diodes of the MOSFETs are conducting.



(a) Battery charging from Photovoltaic module with AC grid-tie

Figure 4.49: Battery charging from Photovoltaic module with AC grid-tie



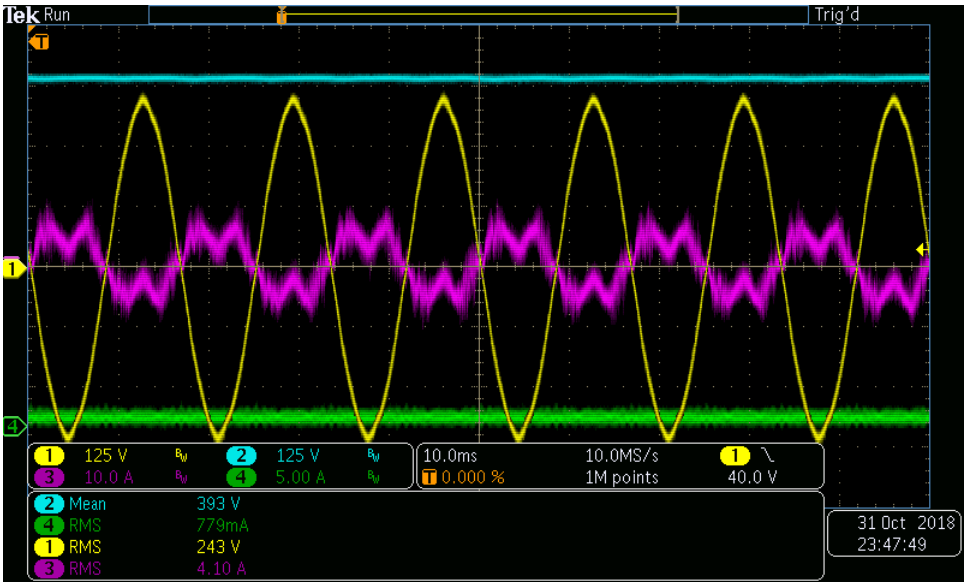
(a) Battery charging from Photovoltaic module with AC grid-tie

Figure 4.50: Battery charging from Photovoltaic module with AC grid-tie

(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

Figure 4.51: Battery charging from Photovoltaic module with AC grid

The grid is feeding the required amount of active current to maintain the DC bus at nearly 400V.

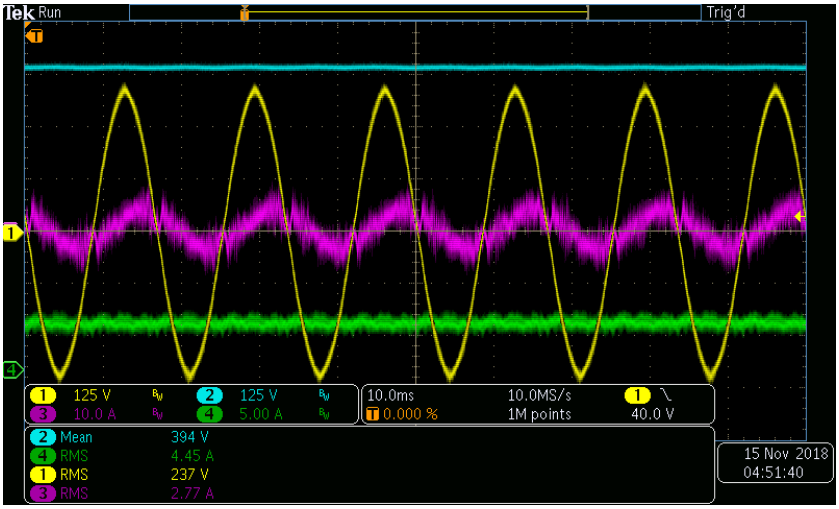


(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

Figure 4.52: Battery charging from Photovoltaic module with AC grid-tie

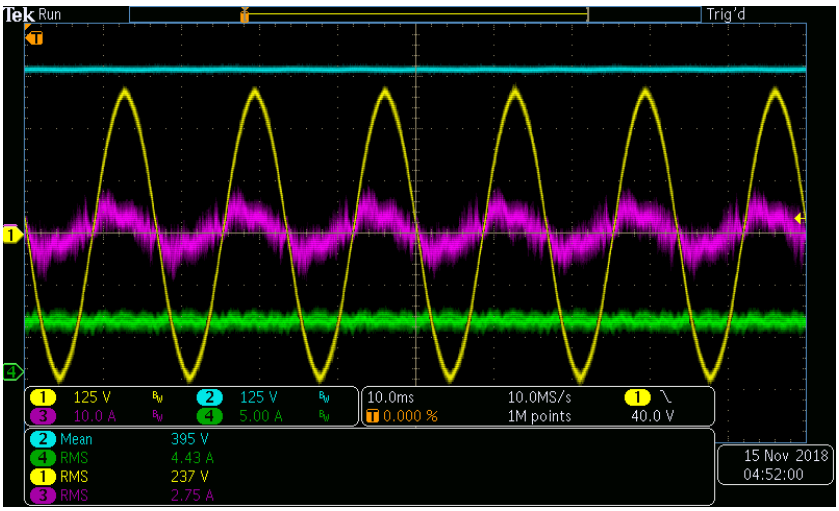
- P-Q control

  First quadrant operation



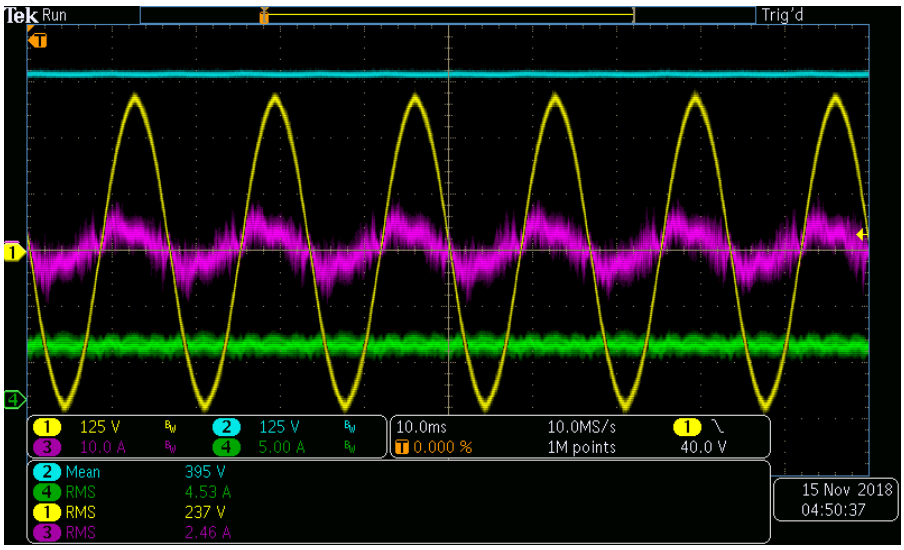
(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

Figure 4.53: Battery charging from Photovoltaic module with grid-tie inverter operating in first quadrant



(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

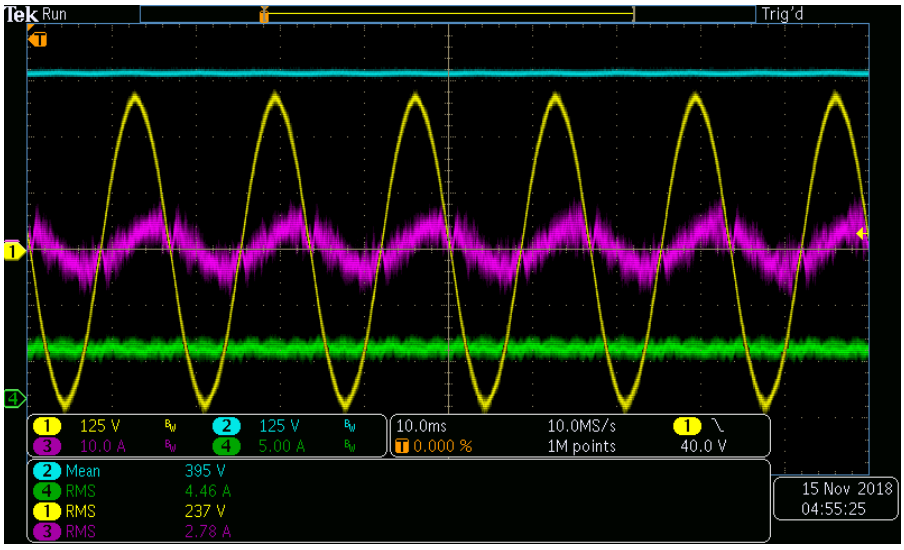
Figure 4.54: Battery charging from Photovoltaic module with grid-tie inverter operating in first quadrant



(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

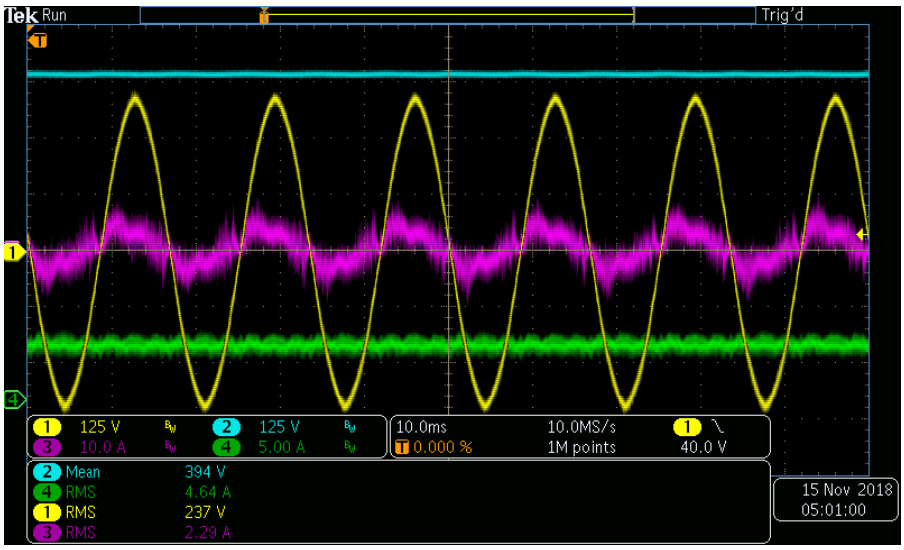
Figure 4.55: Battery charging from Photovoltaic module with grid-tie inverter operating in first quadrant

Second quadrant operation



(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

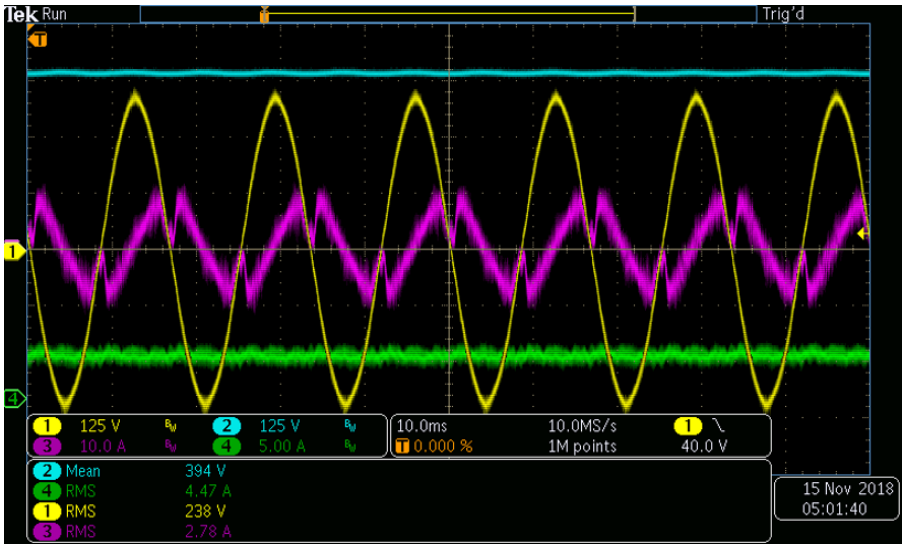
Figure 4.56: Battery charging from Photovoltaic module with AC grid-tie inveretr operating in fourth quadrant



(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

Figure 4.57: Battery charging from Photovoltaic module with grid-tie inverter operating in second quadrant

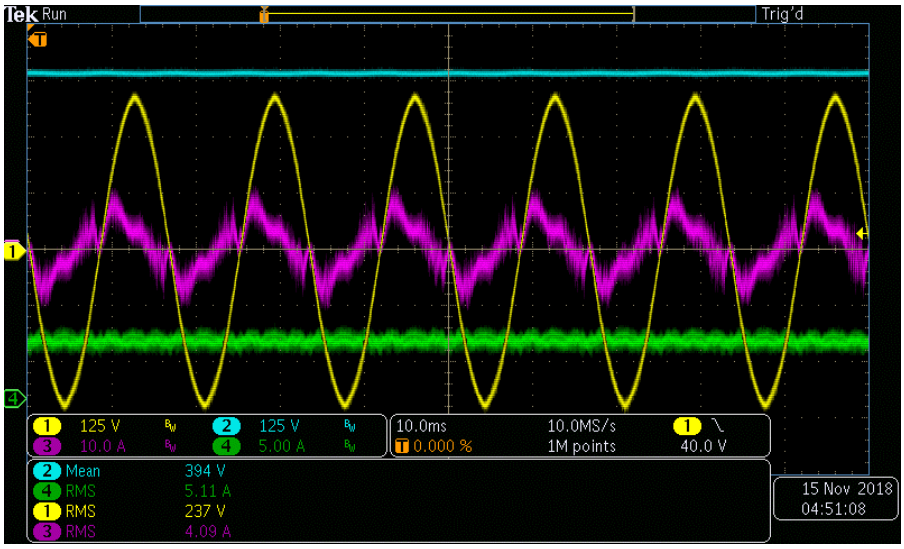
Third quadrant operation



(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

Figure 4.58: Battery charging from Photovoltaic module with grid-tie inverter operating in third quadrant

Fourth quadrant operation



(a) Yellow: Grid voltage Pink: Grid current Blue: DC bus voltage Green: DC power supply current

Figure 4.59: Battery charging from Photovoltaic module with AC grid-tie inverter operating in fourth quadrant

CHAPTER 5: CONCLUSIONS AND FUTURE SCOPE

5.1 Conclusions

All four quadrants of operation have been demonstrated in hardware setup within laboratory constraints. All three power processing units integrated operation has been demonstrated for various functions such as battery charging, Vdc regulation and P-Q controls. The controls are working well for the experimental test for all the functionalities.

The grid-tied operation of a high switching frequency inverter using silicon carbide device has been demonstrated. All the permutations and combinations of active power and reactive power have been shown. Depending on the varying loading condition at the distribution level.

This converter resolves high power quality problem with low inductance and high switching frequency. The harmonics can be further minimized with suitable active control mechanisms.

Because of the inverter capability to operate at different parameters, it is capable to perform voltage support in the low voltage distribution networks upto 10 KVA.

5.2 Future scopes

A suitable active control can be implemented for the mitigation of harmonic currents.

Increasing the inverter inductance little bit can provide good current waveforms.

LC filter has been used while developing the inverter. A small inductance has been used because of the high switching frequency of the silicon carbide MOSFET device. Instead of LC filter a LCL filter can be used. LCL filters in grid connected inverters

allow the use of smaller inductance values and attenuates the high frequency harmonics better than the LC filters. Active damping of LCL filter can be implemented for better stability.

Automation of reference signals can be done by sensing the grid conditions. This will allow to avoid manual change of reference signal. A suitable algorithm can be programmed to change the reference signals fro P-Q control depending on the grid voltages.

Number of current sensors can be reduced by developing an algorithm to predict or estimate the current.

GaN devices can be used in the power processing units for high power density.

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