HIGH FREQUENCY GAN POWER CONVERTERS DIGITAL TWIN

by

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A dissertation submitted to the faculty of
The University of North Carolina at Charlotte
in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in
Electrical Engineering

Charlotte

2018

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ABSTRACT

MEHRDAD BIGLARBEGIAN. High Frequency GaN Power Converters Digital Twin. (Under the direction of DR. BABAK PARKHIDEH)

There is a need for a foundation of a research study aimed at investigations on near real-time reliability awareness of Gallium Nitride devices in high-frequency power converters for which we need advanced hardware and algorithms. This dissertation is moving beyond traditional reliability analysis and looking to more applicable and accurate analytical tools by introducing deep learning techniques and advanced sensing solutions. The computational structures will be applied at the edge of the power converter through online sensing and data processing units as well as on a remote server. They will provide an iterative ability to predict the time until the device may fail or reach a pre-defined degradation threshold.

With the availability of the most granular information deduced from advanced devices, a new data-driven scheme is proposed for system monitoring and possible lifetime extension Gallium Nitride power converters. The approach relies on the real-time $R_{ds(on)}$ data extraction from the power converter, and calibration of an adaptive model using multi-physics co-simulations under power cycling. More specifically, the focus is on deploying machine learning algorithms to exploit for the parameter estimation in power electronics engineering reliability. The proposed techniques in this work are quite new and have not yet been developed and analyzed for high-frequency power converters specifically with Gallium Nitride power semiconductor devices.

ACKNOWLEDGEMENTS

I would like to thank my adviser Dr. Babak Parkhideh for his continuous support on my work, which helped me to complete this dissertation. His positive attitude toward research is unique and made me believe that I can aim for the highest goals. Thanks also go to my dissertation committees Drs. Badrul Chowdhury, Robert Cox, and Maciej Noras. I was fortunate to learn a lot from all of them in both teaching and research.

I would like to thank EPIC and ECE at UNC-Charlotte, and NSF for providing me with scholarships, and Dr. Mohammad Biglarbegian at University of Guelph, which further facilitated conducting my Ph.D. research.

Many thanks to my fellow students and friends at UNC-Charlotte who have supported my work. In my daily life, I have been blessed with so many wonderful friends that I am afraid I can not mention them one by one here. I would like to sincerely thank my colleagues Hamidreza Jafarian, Iman Mazhari, Namwon Kim, Shahriar Nibir, Neel Shah, Mohammadreza Baharani, Saman Mostafavi, Daniel Evans, John Troxler, Michael Ajazi, Sven Hauer, Andreas Lauer, Daniel Fregosi, Deepak Somayajula, and many others in the PV Integration Lab for unforgettable memories.

I wish there was a chance to present this work to my father who left me alone in the middle of my Ph.D. His spirit will always be with me, and he was always encouraged me to continue my studies. I want to express my greatest thankfulness to my mother and my brothers Drs. Mohammad and Behzad for their endless support in my whole life. All these years, I got a lot of encouraging words from my best family members all around the world that I will remember these fruitful moments and the emotional supports.

Finally, I would like to thank my great teachers and professors in my whole life for their dedication and excellence in teaching and education.

DEDICATION

To my beautiful wife Fatemeh!

It wouldn't have been possible this without your supreme patience!

Your boundless love was always inspiring me to continue all days and nights!

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LIST OF ABBREVIATIONS

2DEG Two-Dimensional Election Gas

ADC Analogue to Digital Converter

ALT Accelerated Life Test

BCM Boundary Conduction Mode

BPTT Back Propagation Through Time

CCM Continuous Conduction Mode

CHIL Controller Hardware-In-the-Loop

CMPR Counter Compare Register

CTE Coefficient of Thermal Expansion

DAS Data Acquisition System

DCM Discontinuous Conduction Mode

DUT Device Under Test

EMI Electromagnetic Interfaces

FEA Finite Element Analysis

FET Field Effective Transistors

GaAs Gallium Arsenide

GaN Gallium Nitride

HEMT High Electron Mobility Transistors

IGBT Insulated Gate Bipolar Transistor

IoT Internet of Things

LSTM Long Short-Term Memory

MCMC Monte Carlo Markov Chain

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MPPT Maximum Power Point Tracking

MR Magnetoresistance

MSE Mean Square Error

PF Power Factor

PoF Physics of Failure

PV Photovoltaic

RLHS Random Latin Hypercube Sampling

RNN Recurrent Neural Network

Si Silicon

SiC Silicon Carbide

SIRI Smart Inverter Robustness Index

SMPS Switch Mode Power Supply

TBCTR Time-based Counter Register

TBPRD Time Based Period Register

THD Total Harmonic Distortion

WBG Wide Bandgap

XINT External Interrupt

ZCD Zero Current Detection

CHAPTER 1: INTRODUCTION

1.1 Motivation

Over the years, many solutions have been proposed to convert the primary source of energy to the electricity. Despite all the novel techniques to improve the quality and the conversion efficiency, more than 40% of the primary energy got lost [1]. Power electronics systems can provide effective solutions due their reliable, efficient, smaller footprint and weight in the wide range of applications as high voltage direct current, motor drives, distributed energy sources, solid-state transformers, transportation systems, data centers, and etc. Due to significant progress of consumer electronics in recent years, it is expected by 2030, the power electronics will be used in 80% of applications somewhere from generation to end-users [2].

Having advanced Wide Band-gap (WBG) technologies such as Silicon Carbide (SiC), Gallium Arsenide (GaAs), Aluminum Nitride (AlN), Boron Nitride (BN), and Gallium Nitride (GaN) are crucial to meet the progressive trends in future. For the power applications ($< 650V$), GaN semiconductor is a promising solution for many due to their superior performance regarding conduction loss, switching loss, thermal resistance. Although GaN devices theoretically are more reliable compared to the existing Si-based technologies, however, lack of available data sets do not exist to guarantee their reliable service over the time. Lack of this information will significantly impact maintenance scheduling for large companies and utilities.

This dissertation focuses on the challenges on the reliability of GaN power devices, and explicitly proposes a new cost-effective framework online reliability assessment of high-frequency GaN power converters.

1.2 Literature review

In today's world, for practical implementation and proper functionality of switching power supplies, several main performance factors are considered: efficiency, size, cost, and the reliability. The advancement material, digital processors, and power semiconductors provide new opportunity to reach beyond the former limits quickly. Depending on the usage, some of these factors could be highlighted more than the others; however, due to the dependability of many applications to switching power converters, these days we need to improve all these factors (Fig. 1.1) at the same time. The dependability in power electronics converters makes the reliability very critical from component level manufacturing to system level engineering.

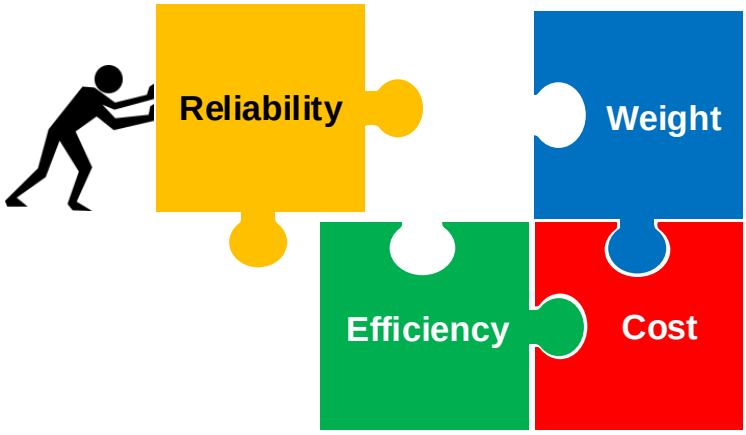


Figure 1.1: **Conceptual matrix**: The four major parameters for advanced power electronics converter designs.

Many studies have been dedicated to analyzing the reliability of power electronics systems under electrical loading, environmental conditions, and mechanical stresses over the years. In one of the most comprehensive survey-based studies over 200 products of 80 companies, solder and semiconductors are responsible for 34% of the failure, capacitors 30%, Printed Circuit Board (PCB) for 26%, and the rest goes to connectors and different facts [3, 4]. Therefore, many reliability analysis dedicated to power semiconductors and capacitors. Many researchers spend significant time to

study capacitor failures. The outcome is that a capacitor is among the weakest link, which degrades quite fast over thermal and electrical stresses. In digitally controlled-power converters, the failure diagnostic in capacitors are relatively straightforward. The ripple current/voltage variations, changes of equivalent series resistance, and capacitance are the most common techniques for diagnostics of failure in capacitors [5, 6].

In power semiconductor modules duo to significant higher stress on power semiconductor modules and continuous progress of devices, vast studies carried out and still the research is continuing. For instance, in Si-based power modules such as Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Insulated Gate Bipolar Transistor (IGBT), the failure mechanisms are categorized into two groups as extrinsic and intrinsic failures. The extrinsic failures include the transistor packaging issues that are mainly summarized as a bond-wire lift, die solder detachment, and contact migration [7, 8]. The intrinsic refers to failure damages coming from the semiconductor itself. Most common failures of intrinsic types are the dielectric breakdown, time-dependent dielectric breakdown, electromigration [9, 10, 11, 12].

In recent years, thanks to the development and growth of WBG devices, efficient, lighter, and reliable power converter will be promised to the industry. The WBG materials have much higher energy band-gap compared to Si, which enables a new path for operating at higher temperature and power.

Although technically the WBG-based power converter should be more reliable due to their higher activation of energy, practically due to continuous improvement of cost-effective device packaging, the reliable operation of these compound semiconductors is unknown. There are some research papers and industrial reports dealing with the reliability analysis of Si devices and recently SiC devices, whereas there are few reports on GaN power devices. Recent studies focus on single device performance in DC operation for power and thermal cycling like most reliability study. The

Weibull distribution has historically been the best tool for describing the reliability engineers in probability prediction of failures over time. While this technique is very accurate at describing failure distributions for large populations of components, it works very poorly at predicting the time until failure of an individual component Fig. 1.2. Moreover, the proposed techniques are very expensive (time, and cost), and their adaptability for the new technologies should be examined fundamentally. Therefore, there is a need to rethink about the reliability platform establishing for failure pattern recognition.

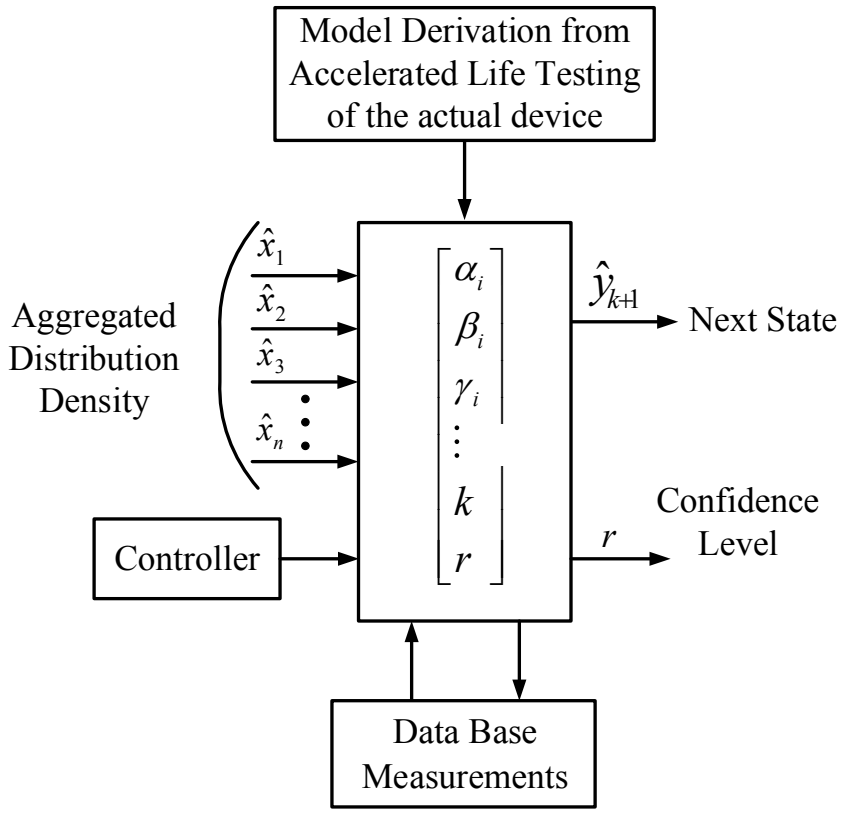


Figure 1.2: **Conventional reliability modeling**: Accelerated life tests of hundreds of hours are developed for extracting the mathematical modeling of device failure.

1.3 Proposed solution

In this dissertation, the goal is to characterize and recognize the component-wise pattern variations through the actual measurement of the GaN power devices in a power converter. Therefore, a new concept of reliability analysis is proposed, and the

main contributions are presented as follows:

a) Data collection for fault diagnostic and risk analysis through the state of the high-frequency current solutions. This part mainly focuses on gathering data related to the failure mechanism of the devices to run advanced learning methods.

b) From the available data, the advanced learning methods should be processed to be able to extract the proper information to be able to analyze the power converter reliable, safe and healthy operation shown in Fig. 1.3. In this framework, the machine learning technique will be used to be able to find the correlations between unknown physical and mathematical equations.

c) Proposing mathematical modeling from the existing technologies of GaN devices used in power converter, and calibrating them for advanced learning.

The behavior of the device during normal operation and the degradation region will be analyzed. The features associated with the failure will be extracted using Recurrent Neural Network (RNN) method, and the faulty device will be recognized. Once the healthy pattern versus defective device got identified as the base of training the data, the new data sets will be predicted with the actual measurement of the device. In general, the process could be analyzed either through edge computation in the microprocessor as cloud computations where the cloud servers are located for the captured data. In this thesis the cloud server computation was used for easier implementation; however, the possibility of edge computation was also examined.

As it mentioned above, most of the commonly applied techniques relied on the Accelerated Life Test (ALT) of the actual device as Device Under Test (DUT) to apply harsh testing and be able to find the suitable regions of the devices through the Physics of Failure (PoF). In our proposed method, the Finite Element Analysis (FEA) will be used, and the ALT will be implemented in the simulation platform. As we expect the simulation modeling might not be accurate in the beginning state due to lack of the previous model of a device or converter, the active calibration

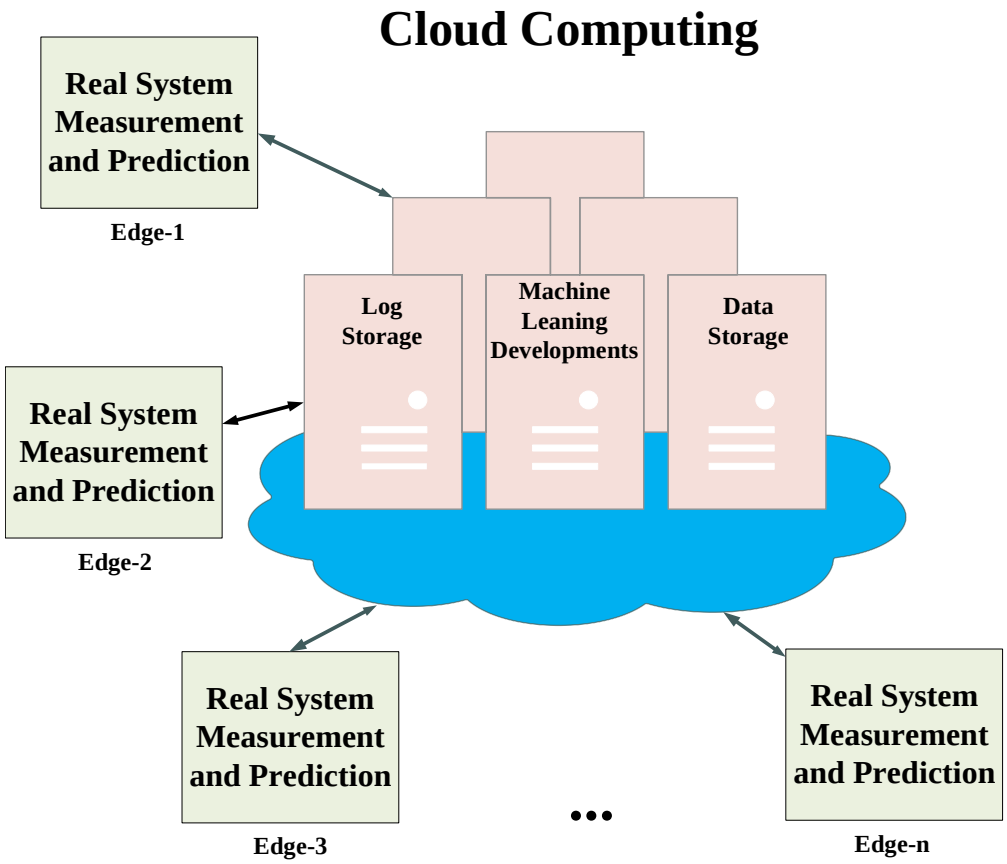


Figure 1.3: **General proposed reliability solution**: The proposed framework of Internet of Things reliability analysis using edge/cloud computations for an advanced power electronics converter.

method will be used to reduce the computation error over the time through the actual measurements. This eventually leads to finding cheaper, and adaptable solution as more data will be collected, and the simulation could be calibrated over the time.

1.4 Thesis contributions

The thesis chapters are described as follows: Chapter 2 describes the failure mechanism affecting enhancement mode GaN power devices. Chapter 3 focuses on the fault diagnostic and the proposed solution for the active prognostics including the test benches. This chapter presents the architecture of the system as power electronics point of view. In Chapter 4, the concept of Deep Learning Reliability Awareness of Converters at the Edge (Deep RACE) is developed. Chapter 5 focuses on the

system integration through edge computation following with the experimental results in Chapter 6. Chapter 7 discusses a new current measurement technique for active $R_{ds(on)}$ measurements followed with the experimental results along with the conclusion and future work in Chapter 8. The thesis organization is also shown in Fig. 1.4.

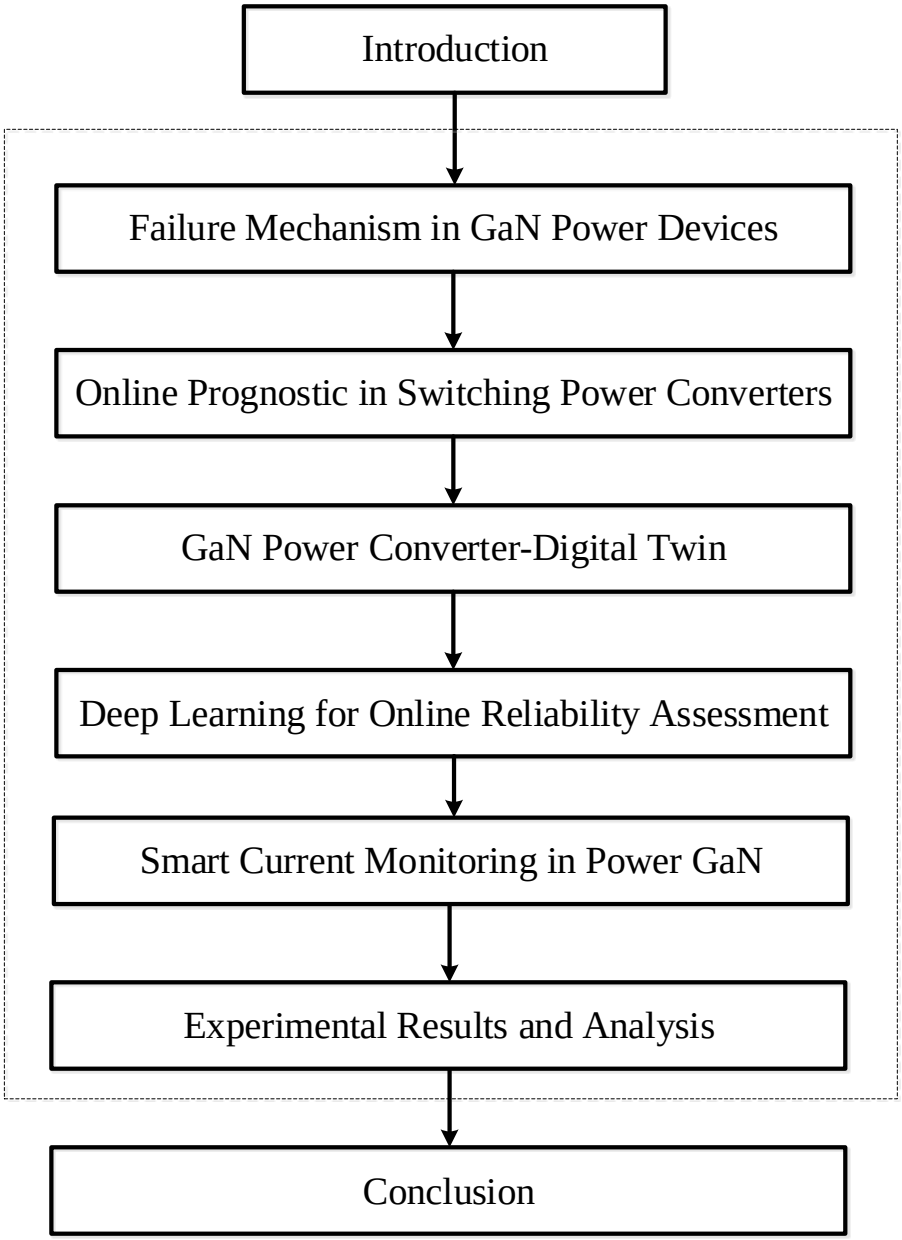


Figure 1.4: **Thesis framework**: The main contributions of this work are provided in eight chapters.

CHAPTER 2: FAILURE MECHANISM OF GaN TRANSISTORS IN POWER APPLICATIONS

2.1 Characteristics and structure of GaN transistors

The invention of the High-electron-mobility transistor (HEMT) and using a channel instead of a doped region, which results in the generation of GaN transistors goes to back to 1970s. However, they have not been widely used due to technology maturation, and significantly lower cost of Si-based transistors. After 2000, using depletion mode GaN devices in RF application got more popular, where fabrication of different crystals such as SiC and AlGaN have been implemented [13, 14]. Nowadays, the general road map of using GaN will be categorized as: GaN on Si (for high power low cost applications) [15, 16], GaN on SiC (high performance, high cost for RF applications) [17], GaN on Diamond (for higher thermal conductivity applications) [18], GaN on GaN (Integrated IC, vertical GaN for future applications) [19]. It is expected by 2024 the GaN power market has annual growth more than 28% [20].

The common structure of GaN power devices is built in lateral architecture, which results in lower parasitic capacitance. Moreover, this architecture makes the main conduction path shorter, which results in lower $R_{ds(on)}$. In today's technology, the Si wafer is considered for the substrate to reduce the cost of manufacturing. GaN crystals are grown on the buffer layer (typically AlN) on the top of the substrate, followed by AlGaN to form an ohmic contact. The piezoelectric effect as a main source of GaN conductivity, the high concentration of electrons will be accumulated between AlGaN and GaN layer, and typically referred to as Two-Dimensional Electron Gas (2DEG). In enhancement mode GaN devices, a dielectric layer is considered underneath of the gate metal to make the normally-off transistors shown in Fig. 2.1.

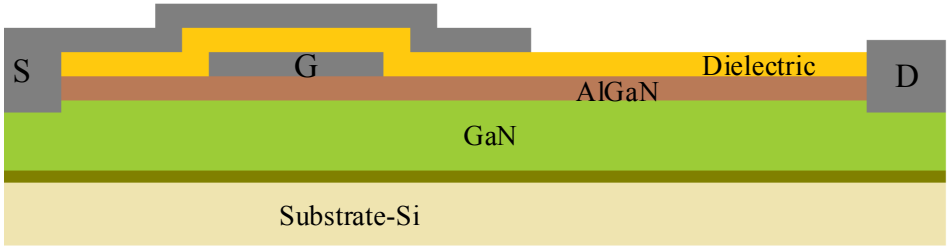


Figure 2.1: **Lateral GaN structure**: The cross section of an enhancement GaN.

The lateral GaN structure has some benefits like relatively easy fabrication, lower conduction loss, and inexpensive solution. However, relatively low breakdown voltage, and the current collapse issue (due to high current flow near the surface) are the main drawbacks of this architecture [21]. After processing the waver, in order to make electrical connection to the outside, unlike many conventional methods for bond wire attachment, direct soldering of contacts to the wavers are used in state-of-the-art solutions of lead manufacturers [13, 16].

In general, higher energy band gap results in higher voltage breakdown, and lower ohmic resistance, which GaN shows promising performance on this side. Theoretically, GaN transistors should have a longer lifetime than Si devices because of their significantly higher activation energy (>2.0 e.V compared to 0.7 e.V for Si). However, engineers based on their requirements might come up with an individual converter design. These design might also have significant differences concerning topology, power rating, efficiency, performance, and implementation.

Today's manufacturers focused on two types of GaN power modules as enhancement and Cascode GaN devices. The enhancement mode GaN was known as normally OFF devices, and Cascode built as the combination of depletion mode GaN in series with Si-MOSFET. The Cascode architecture was proposed by different manufacturers (Transphorm, Sharp and TI), where in addition to depletion mode GaN a normally OFF Si-MOSFET is offered to make it feasible in many common designs. The gate circuit design of the MOSFET can control the ON/OFF state of the GaN since the

MOSFET with higher absolute voltage compared to GaN threshold voltage. This topology has two side effects: As the gate circuit of the MOSFETs operates at a higher voltage level compared to the GaN, and consequently has a higher loss in the circuit. Moreover, the series MOSFETs will add additional resistance on the conduction path and reverse recovery charge of the body diode. On the other side, enhancement mode GaN give an opportunity to make the device normally OFF when the applied gate voltage compared to the source is zero. However, the effect of reverse conduction due to its inherent physics of the GaN semiconductors, they can fully turn on in the third quadrant. Lack of Si-body diode in the GaN devices might result in a higher loss during transients in Switch Mode Power Supplies (SMPS), which needs careful adjustment of dead-times. Moreover, a lower threshold of the voltage in the enhancement mode GaN offers lower loss in the gate driver circuits, but it makes the design very challenging because of overshoot and cross-talk considerations in the layout. All in all, simple packaging and no reverse recovery charge issue coming from the body diode, potentially much lower on-resistance gives a lot of interest for the manufacturer and designers to invest in this technology.

Due to relatively new evolved technology in the last years, and different manufacturing processes for GaN modules, a need for comprehensive reliability analysis would be crucial. This will be very helpful for designers who need transitions to this technology. Even for Si-based devices where their reliability have been examined, and standards test setup have been verified for several decades, there is no specific methodology to show the performance and characterization of power devices under converter operation, which might be varied from one to another design.

2.2 Failure mechanism in power semiconductors

2.2.1 Challenges for reliability evaluation in GaN power devices

Theoretically, GaN power transistors should have a longer lifetime than Si-devices because of their higher activation energy. However, due to some manufacturing lim-

itation, this might not have been shown in any product yet. For instance, to reduce the cost of the GaN devices, many of lead manufacturers fabricate GaN on the Si-substrate, where GaN and Si inherently have crystal mismatching. High-temperature methods have characterized most common ALT analysis for Si-based semiconductors and the failure mechanisms. For instance, Arrhenius exponential law as one of the most common techniques for the reliability assessment in Si-based semiconductors, the variation of activation energy results in the higher error for extrapolation to the real test conditions. Therefore, there are some severe constraints to comment on the accuracy of the conventional methodologies for failure mechanism extraction and remaining useful life estimation [22, 23].

Table 2.1: Summary of main failure mechanisms in GaN power

Failure Potential	$R_{ds(on)}$	V_{th}	I_g
Scottkey contact	Increase	Increase	-
Contact degradation	-	-	Increase
Ohmic thermal degradation	Increase	Abnormal changes	-
Charge trapping*	Increase	Decrease	-
Hot carrier trap generation*	Increase	Decrease	Increase
Piezoelectric*	Increase	Decrease	Abnormal changes

2.2.2 A review of failure mechanism in previous studies

Power cycling tests on the discrete 650V GaN devices have been performed thoroughly in [24, 25] under several ALT. These studies showed the variations of I_{dss}, $R_{ds(on)}$, V_{th}, and T_j are more dominant after the ALT, and also verified that the solder layer is crucial in the device early degradation. Using $R_{ds(on)}$ as a precursor for earlier failure of GaN devices was considered under ALT, and Extended Kalman Filter estimator was developed for device failure propagation and threshold identification in [26]. However, all of these methods have been analyzed under DC input supplies, where the results might vary under real switching converter operation, and need further evaluations.

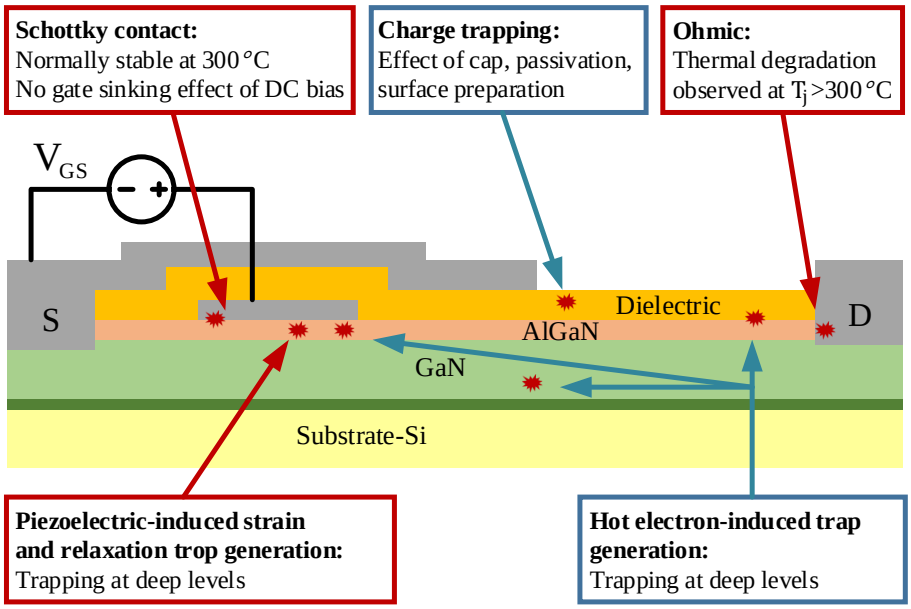


Figure 2.2: **Lateral GaN structure**: The most susceptible regions in GaN device.

Furthermore, the focus is on finding the root of failure in GaN devices, by using similar semiconductors as Si-power semiconductors and GaAs in RF applications. The failure mechanism in Si-modules is categorized into two main groups as intrinsic and extrinsic. Intrinsic refers to failure damages coming from the semiconductors failures; however, the latter one includes the transistor packaging issues. Most common failures of intrinsic types are the dielectric breakdown, time-dependent dielectric breakdown, electromigration. For extrinsic, bond-wire lift failure, die solder degradation are reported in the previous literature [7, 8, 27, 28, 29, 30]. These studies verified the bond-wire lift has the severe effect on the device failure over time. However, because of the significant progress of developing new packages, such as LGA or GaN-PX, the conventional bond-wire issues cannot be easily found as the common failure in the modern GaN devices [31, 32]. Some studies by focusing on the similarity of the crystal structure of GaAs, and considering the similar substrate characteristics of Si-based semiconductors derived the potential failure in GaN modules [33, 34, 35, 36]. The most common potential failure of lateral GaN power devices is shown in Fig. 2.2 and precursor identifications are summarized in Table 2.1.

CHAPTER 3: ONLINE PROGNOSTIC IN SWITCHING POWER CONVERTERS

3.1 Introduction

Controllable power semiconductor devices play the most dominant role in the switching power converters. Operating at high current and voltage create extreme stress on the power devices, which meanwhile make them the most susceptible components in the converters. Therefore, reliable operation of the power converters will be more highlighted in emerging technologies and future applications.

To address the reliability issues of a complex system in the design, fabrication, and maintenance process, different diagnostic and prognostics techniques are proposed. The evaluation of these processes is beneficiary to enable health management systems for useful life estimation and reducing the risk of failures [37, 38, 39]. However, the applied techniques (i.e., such as Kalman filter and Bayesian calibration) used classical first-order models; therefore their accuracies are limited and cannot be adaptive to long-term changes. Moreover, in advanced power electronics, it is hard to understand the degradation physics due to the system's sophistication, which makes then model them accurately in mathematical formats [40, 41, 42].

Recent advances in machine learning open a new horizon toward smart and autonomous systems. Applying machine learning at the earliest stage of design procedure has the most significant effect on the reliability pattern modeling. With the new wave of the Internet of Things (IoT), there is a big chance to be connected to any devices [43, 44]. In particular, the much higher impact could be in the power electronics as many factors are unknown, or it is tough to model in classical fashion. A real-time, low latency decision making and scalable systems require to move the computation of prediction from the cloud to the network nodes.

This section presents a transformative approach for power semiconductor devices reliability to streamline the integration of devices into the smart power electronics systems. Therefore, an integrated framework is proposed based on cloud-edge platform, where training happens in the cloud and inference at the edge next to the power devices. In this regard, the recent advances of Recurrent Neural Networks (RNN) in deep learning is used to capture the behavior over time in complex systems. While training can be done off-line, interference will be operated at the edge (on-line) providing real-time feedback of the reliability modeling as well as active control and decision making for device proliferate.

3.2 Online reliability analysis GaN devices

The GaN power semiconductor is a promising solution to improve the efficiency and the performance of future power converters [45, 46]. Despite the superior characteristics of GaN devices, they are often turned down due to limited information on reliability in many applications. Diagnostics/prognostics approaches enable a possibility of solving reliability issues in complex systems from design to operation for remaining useful life estimation, and mitigation of failure risks. The studies on reliability assessment and system monitoring have focused on component level reliability, damage accumulation, data analytic and condition-based predictions [12, 40]. Component failure approaches rely on the statistical model derived from obtained data in a laboratory environment and/or historical component usage [11]. These methods are not considered prognostics since they do not take into account the unit-to-unit difference and their specific usage history. The damage accumulation methods offer more accurate tendency, but they need empirical verification and experimental observations. Data analytic and condition-based monitoring focus on big-data extraction, and estimation with the past usage history data provided by ALT. Several methods are proposed for mean-life estimates like six sigma, fault tree analysis, state space, and filtering estimations [41, 47].

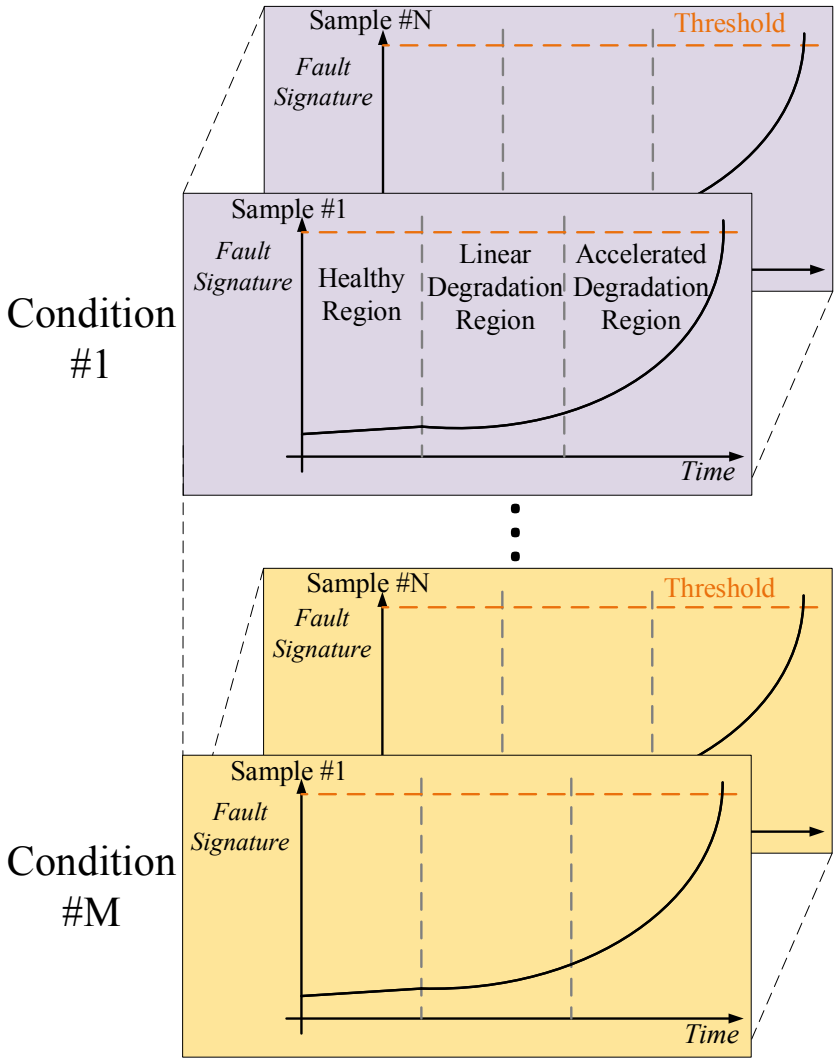


Figure 3.1: **Conventional reliability solution**: #N samples of devices with #M conditions have been analyzed experimentally under accelerated life tests to find the reliability model. Adaptability with the new technologies and the experimental costs are their main drawbacks.

Furthermore, a newly developed PoF analysis is presented to identify the failure root mechanism and drive the reliability models quantitatively. Theoretically speaking, it is possible to make life predictions based on these methods; however, the performance is likely going to be poor when compared to the actual failure time observed. This occurs because no knowledge of the actual component is used, and all the applied techniques considered the constant failure rates in components and system levels [11, 48]. Most of the developed approaches relied on stress on the de-

vices under power/thermal cycling with the experimental observations shown in Fig. 3.1. In the active monitoring technique, based on the available data from the system, a predictive online model for the converter operation can be derived. Having the limited knowledge of the existing state or the system status, the adaptive model can predict the system characteristics within the next time horizons shown in Fig. 3.2. The combination of failure diagnostics (model derivation) and self-verification techniques (deep learning analysis) can be evolved as a new generation of physics-based diagnostic/prognostic scheme to develop an adaptive model for a system level reliability.

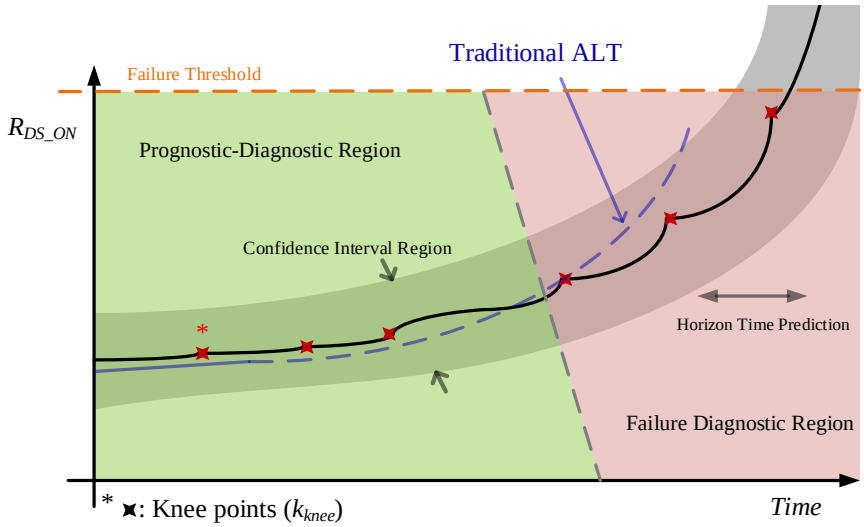


Figure 3.2: **Proposed solution**: Adaptive prognostics concept using multi-physics co-simulations and machine learning algorithm with advanced monitoring.

This work presents a hybrid condition-based prediction where the ALT will be run in multi-physics simulations. Based on the simulated reliability model, a new RNN machine learning scheme is proposed for the system prognostics. Here, the component selection for the reliability analysis and modeling of solder fatigue in the power converter is described. This section also proposes the methodology for health conditioning system, which focuses on machine learning method for parameter estimations of the system calibration.

3.3 GaN Power Converter-Digital Twin

3.3.1 Thermomechanical susceptibility

In the existing lateral enhancement mode GaN products, GaN is grown on the Si-substrate. Due to inherent mismatching of stacked materials, the different Coefficient of Thermal Expansion (CTE) of the mounted GaN onto the PCB causes generation of cracks. The GaN power device is subject to the high power, which makes the thermo-mechanical stress in the solder joints among the most susceptible sections. Therefore, the crack could propagate along the solder joints and eventually it will result in permanent failure in the devices. The solder joint fatigue existed in Si-based devices, but the fatigue in the compound semiconductors will be worse. Although there is no direct correlation between crack propagation and physical parameter extraction, the previous study showed this mechanism could have an impact on the gradual increase of the electrical resistance [49, 50, 51].

3.3.2 Reliability framework of power converter

To comment on the reliability assessment of power converters, it is essential to have a robust converter. Therefore, the summarized all the possible candidate of GaN devices are provided that could be used for this study. The loss index of $R_{ds(on)} \times Q_g$ is defined to compare the efficiency power conversion in different devices, the thermal resistance and the reverse recovery charge also considered as shown in Table 3.2.

The various CTE of stacked layers inject stress concentrations, and they cause deformation of materials. The deformation mainly is observed as a crack on the solder joints, and eventually results in permanent failure of the compound semiconductors. The characterization of the crack propagation is very hard because of the complexity of the device and assembling of stacked layers. Moreover, challenging on the measurements of the operation of high-frequency converter makes the system modeling very difficult. Therefore, a new framework is proposed to be able to characterize the un-

known parameters that physically are not possible to measure them on the operating power converter. The main contribution is to correlate the mathematical formulations of the direct measurement of $R_{ds(on)}$ the corresponding mechanical parameters responsible for the fatigue. The proposed framework consists of three main sections as simulation-based ALT, online system monitoring, and the machine learning unit.

In the simulation-ALT, the energy-based fatigue of the power semiconductor under stress-strain hysteresis is modeled. The Gerber files of the converter layout will be imported, and the semiconductor device is shaped accordingly. Knowing the device conduction loss, the ALT is carried out under temperature cycling with the FEA. The simulation output provides a degradation model of the actual system. The model calibration is needed due to lack of detailed information of mounted device onto the PCB in the real order. The calibration will be done with the online measurements and update the unknown parameters through machine learning units. The online monitoring system focuses on system measurement of the main physical parameters (e.g., voltage, current, and the temperature). The resistance of the semiconductor, total loss, and the converter power range can be calculated based on the captured data. The machine learning unit based on the proposed model calibrates the simulation model according to the actual measurements shown in Fig. 3.5.

3.3.3 Energy-based fatigue failure modeling

Thermal fatigue failure due to the CTE of materials is the main failure mechanism of the solder joint connections, especially in the compound semiconductors. The increase in the electrical resistance during fatigue has been studied and verified in [49, 50]. The energy-based fatigue is used by focusing on the energy accumulated in the susceptible regions shown in Fig. 3.3. The dissipated energy occurs within the strain-stress diagram, and the variations of resistance-strain are depicted in (3.1):

$$\Delta R_{ds(on)} = R_{ds(on)}(1 + 2v + a)\epsilon \tag{3.1}$$

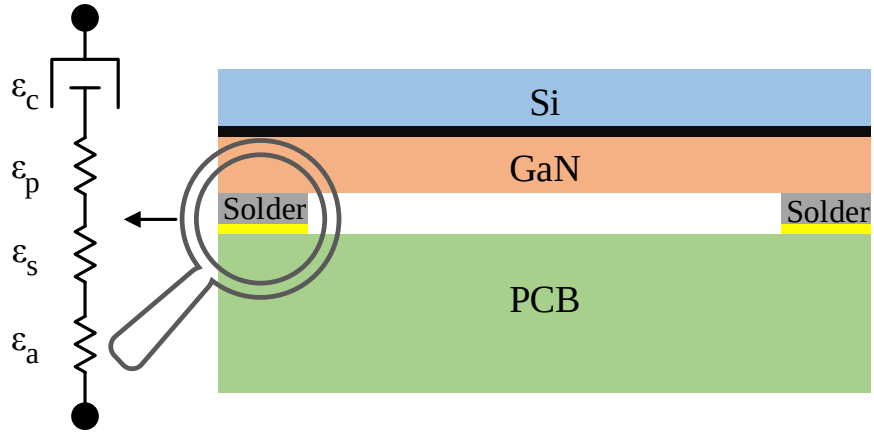


Figure 3.3: **Mounted GaN on the PCB**: Simplified model of a lateral GaN mounted on the PCB. GaN and Silicon (substrates) are isolated with thin layer of AlGaN, and packaging is not considered in the model.

where v is Poisson ratio, a is the resistivity of the material, and ϵ is the material strain [51]. These parameters depend on the material and the operational temperature can be considered as constant values. The total mechanical strain of the solder deformation can be given as (3.2):

$$\epsilon_t = \epsilon_e + \epsilon_c + \epsilon_p \tag{3.2}$$

where the ϵ_e, ϵ_c, ϵ_p are elastic, creep and plastic strains respectively, and can be calculated in (3.3):

$$\frac{d\epsilon_s}{dt} = C_{ss}[sinh(\alpha\sigma)]^n exp(\frac{-E_a}{kT}) \tag{3.3}$$

$$\epsilon_e = \sigma/E \tag{3.4}$$

$$\frac{d\epsilon_c}{dt} = \frac{d\epsilon_s}{dt}(1 + \epsilon_t B)exp(-B\frac{d\epsilon_c}{dt}t) \tag{3.5}$$

The summary of the parameters and the associated values are in Table 3.1.

Table 3.1: Stress-strain parameters for the simulation analysis

Parameter	Description	Value	Unit
C_{ss}	Constant	$8 \times e^{4}$	$1/s$
α	Stress level	$4.6 \times e^{-4}$	$1/psi$
k	Boltzmann coefficient	1.38×10^{-23}	m^2Kg/s^2K
n	Stress component	4	-
E_a	Activation of energy	0.7	$e.V$
ϵ_t	Transient creep strain	0.025	-
B	Transient creep coefficient	260	-
C_p	Constant	$1.2 \times e^{-23}$	-
m	Constant	5.5	-
T	Ambient Temperature	300	K

During solder fatigue, the plastic strain plays a major role, where the rests of the strain changes remain almost constant [41, 52]. Knowing the material properties and the junction temperature of the device, the parameters associated with the elastic and creep strains will be constant:

$$\Delta W_{hys} = \oint_{Hystloop} \sigma d\epsilon \tag{3.6}$$

wherein (3.6) σ is the stress, ϵ is strain, and W_{hys} is the cyclic dissipated energy loss shown in Fig. 3.4. Knowing the changes of strain (ϵ) could result in changes of on-resistance $R_{ds(on)}$, while the ALT runs for each iteration, a series test resistor will be added to the model to calculate the resistance variations. It can be presumed that the energy loss calculated in ΔW_{hys} will potentially affect the tiny variations on the physical measurement of the on-resistance. Since finding all the unknown parameters associated with the loss model could be very difficult and time-consuming, the simplified model of this is used. Since the strain changes have a linear impact in the initial stages, the simplified model is developed as:

$$\epsilon_t = A \times (\sigma_{load}/\sigma_{ref})^B \tag{3.7}$$

where A and B are the unknown parametric constants coming from the machine learning algorithm, ϵ_t is the total strain and σ_{load} is the load stress depending on the GaN loss generation and material properties defined in the simulation platform, and σ_{ref} is the reference stress expected from the manufacturer test plans shown in Fig. 3.6. Here, the fundamental material properties are used that has been used in the lateral GaN devices.

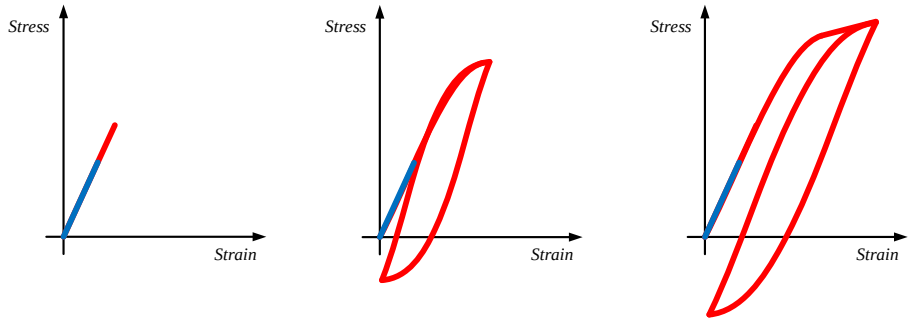


Figure 3.4: **The hysteresis loss**: Once the nominal mean stress is less than border mean stress (left) vs. the mean stress is higher than the border mean stress (right).

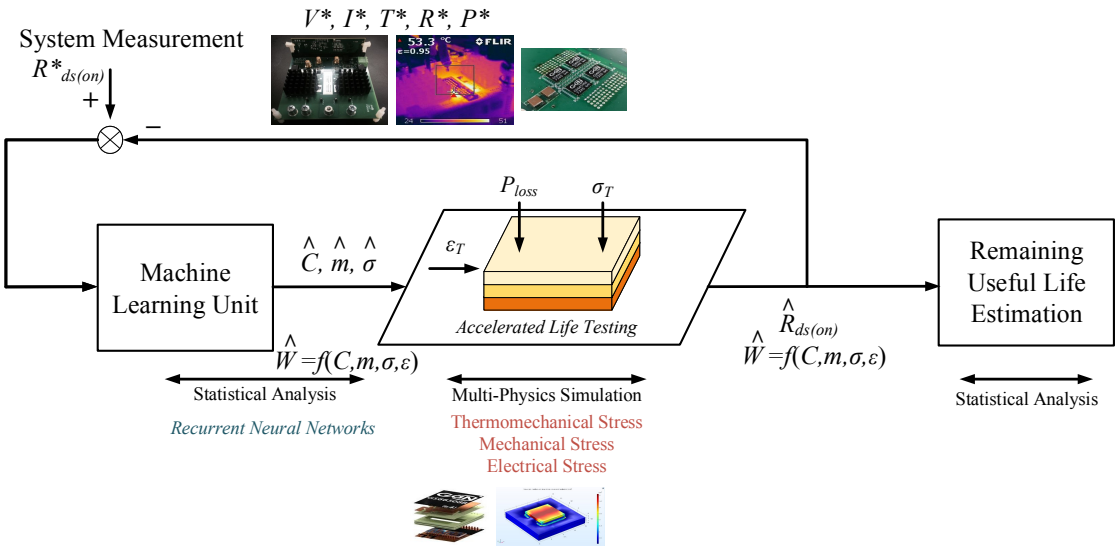


Figure 3.5: **Proposed framework for GaN power converter-Digital Twin**: The online device monitoring, and simulation-based ALT for reliability analysis. A machine learning system is developed for system calibrations and parameter estimations.

The major contribution here is to estimate the infinitesimal loss generation resulted

from the solder fatigue of the stress and strain diagram through the simulations. In practical application, it is tough to measure the stress-strain variations, but with physical loss generation of the device, the loss could be speculated through the mathematical analysis. Knowing the properties of the material in the stacked layer of the GaN devices, a test resistor will be placed to characterize the device resistance variations. In this system, Darveaux fatigue modeling is used to evaluate the crack propagation and life prediction of the solder material [52]. Based on this model, the solder fatigue under the thermal cycle conditions tests can be simplified as (7.6):

$$N = k_1(\frac{\Delta W_{ave}}{W_{ref}})^{k_2} + a/k_3(\frac{\Delta W_{ave}}{W_{ref}})^{-k_4} \tag{3.8}$$

where, ΔW_{ave} is the average dissipated energy calculated in the infinitesimal the area of stress-strain of the solder joint under the fatigue cycles, k_1 and k_3 are energy coefficients of crack initiation and propagation, and k_2, k_4, are energy exponents of crack initiation and propagation respectively. The a parameter reflects the distance of the crack, and it could potentially start from one side of solder joint [53].

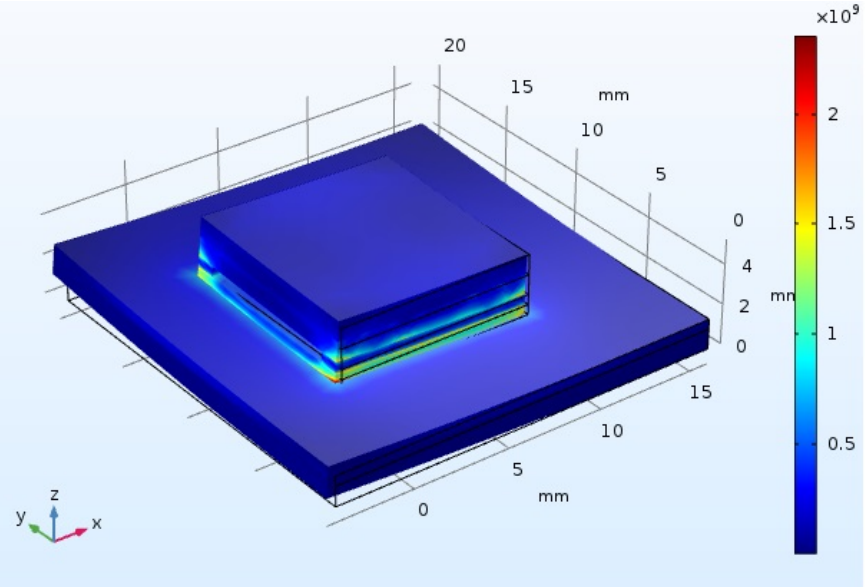


Figure 3.6: **Simulation of the accelerated life test**: The fatigue failure mode of the lateral GaN device is simulated through the finite element analysis.

The variations of the electrical resistance results in the changes of the strain productively, where the simulated results for filtered 10000 cycles are shown in Fig. 3.7.

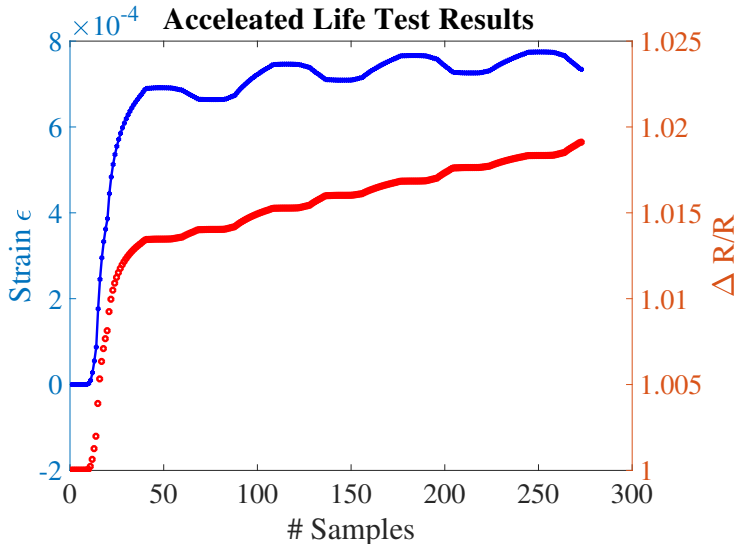


Figure 3.7: **Simulation of strain-resistance**: The resistance variations and the strain changes are simulation based on the proposed geometry.

The strain variations resulted from Fig. 3.7 could potentially change the variation in energy loss generated through the solder fatigue. Therefore, in each run, the stress changes in equation 3.7 is calculated and the power loss generation in each cycle is simulated accordingly shown in Fig. 3.8.

Finally, the simulated results for on-resistance for more than 10000 iterations under four different scenarios with various coefficients in equation 3.7 shown in Fig. 3.9. Since the simulation gives pure resistance changes, a normal distribution process noise is added to the simulated results for easier training and make it more realistic to the actual device measurement.

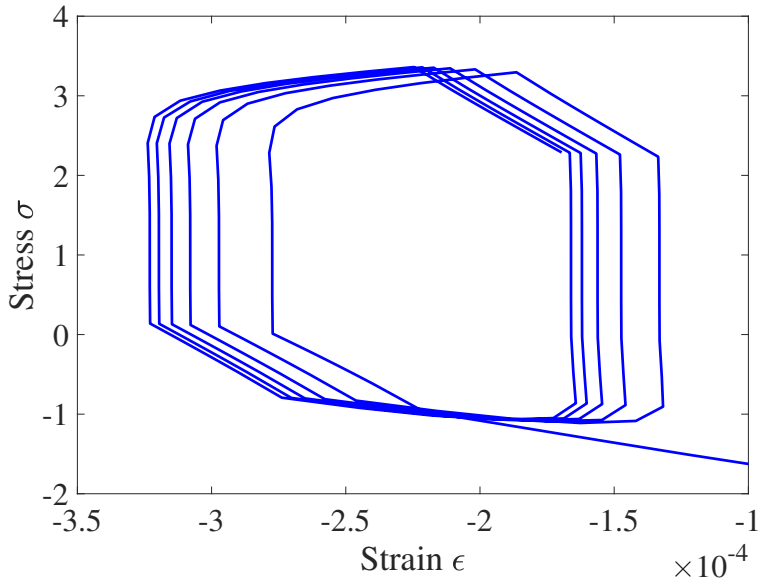


Figure 3.8: **Simulation of strain-resistance**: The simulated energy loss generated from the stress and strain variation of the joints in the accelerated life analysis.

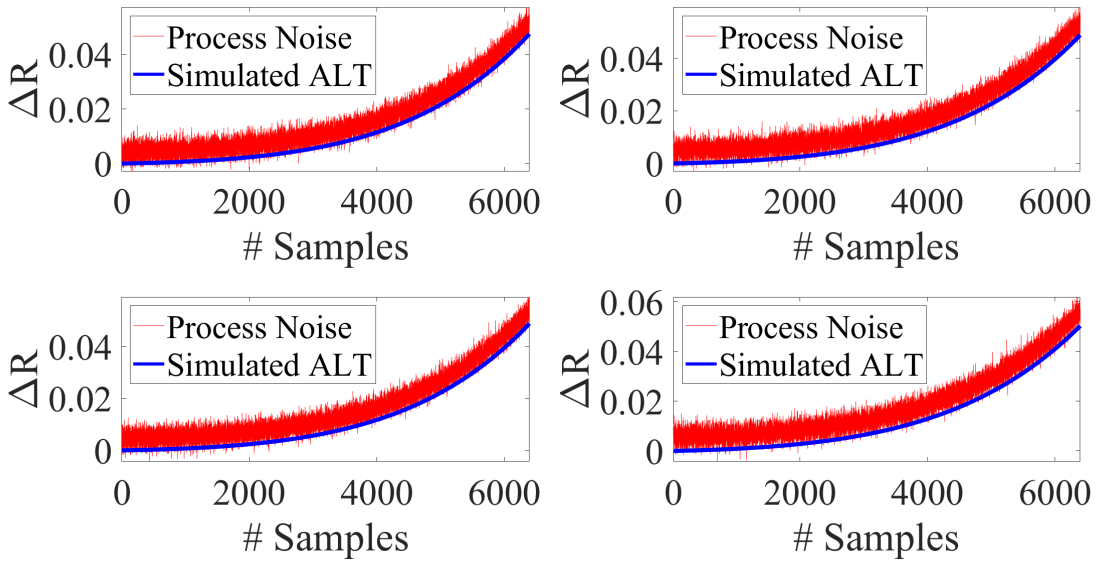


Figure 3.9: **Simulation result of the accelerated life test**: The variations $R_{ds(on)}$ under temperature cycling due to solder fatigue of GaN on Silicon.

Table 3.2: Selected device characteristics comparisons for converter design

Type	Part Number	Voltage	Current	Resistance	Gate Charge	Loss Index	Thermal Resistance	Reverse Recovery Charge	Package
		V	A	$m\Omega$	nC	$R_{ds(on)} \times Q_g$	C/W	nC	
E-mode	GS66516T	650	60	25	12.1	302.5	0.3	0	GaN_{PX}
E-mode	GS66516B	650	60	25	12.1	302.5	0.55	0	GaN_{PX}
E-mode	GS66504B	650	15	100	3	300	1	0	GaN_{PX}
C-mode	TPH3208L	650	20	130	10	1300	1.3	54	PQFN
C-mode	TPH3206LD	600	17	180	6	1080	1.55	54	PQFN
C-mode	TPH3205WS	600	36	52	28	1456	1.0	136	TO247
E-mode	PGA26E07BA	600	26	56	5	280	1.3	0	DFN
E-mode	PGA26E19BA	600	10	140	4	560	1.9	0	DFN
C-mode	NTP8G206N	600	17	150	6.2	930	1.55	53	TO220
D-mode	MGG1T0617D	600	30	170	4	680	-	0	Die

* E-mode: Enhancement, C-mode: Cascode, D-mode: Depletion

*In this table, RF GaN products, GaN power devices with voltage rating <600V, and devices with integrated gate driver circuits are not included.

CHAPTER 4: DEEP LEARNING FOR ONLINE RELIABILITY ASSESSMENT

4.1 Introduction

With the significant growth of advanced high-frequency power converters, on-line monitoring and ongoing reliability assessment of power electronic devices are incredibly crucial. Existing reliability modeling approaches for power electronic devices often use classical first-order models which limit the reliability assessment. Furthermore, they often look at the individual devices in isolation and do not take into account the collected data across many devices with similar underlying physic. Mathematically formulating and precise understanding of the physical degradation in high-frequency power converters is notoriously tricky, due to systemâs sophistication and many unknown non-deterministic variables. To solve this problem, a wide range of stochastic diagnostic and prognostics techniques have been proposed to address the reliability issues of a complex system in the design, fabrication, and maintenance process. Examples are classical time series modeling and prediction techniques such as Kalman filter and Bayesian calibration. However, these approaches are often bounded to first-order models in isolation and are not able to bring the collective behavior of many devices with the same underlying physic to create an accurate algorithmic construct. Therefore, their prediction accuracy is minimal. One example of associated issues using existing machine learning technique in the next subsection. Recent advances in deep learning open a new horizon toward smart and autonomous systems. Deep learning offers a data-driven paradigm to understand, model and predict the behavior of complex systems by extracting the in-depth collective knowledge.

4.1.1 Challenges of using machine learning algorithm (Bayesian model)

The growth pattern of $R_{ds(on)}$, can be modeled using an exponential fit as the device goes through aging. The goal is to fit a model with the best set of parameters whose behavior resemble the $R_{ds(on)}$ variations. In the proposed approach, unlike the reliability-based models, a single system (subsystem) is considered. The principle of the proposed algorithm follows Bayes theorem. The parameters are considered as unknown random variables and express our knowledge about the parameters in the form of probability distributions. Based on this prior knowledge and available observations (measurements), a posterior probability of parameters can be derived. The prior knowledge about parameters is expressed independently from observation, and the posterior probability of parameters given a series of observations is derived using Bayes theorem. Since it is virtually impossible to obtain the posterior in a closed form manner, this is done through a Monte Carlo Markov Chain (MCMC) process. Metropolis-Hastings algorithm is one form of these methods, which have been recently used in the model calibration applications [54].

The behavior of On-resistance change has different patterns of growth that are distinguishable by abrupt changes shown in Fig. 4.3. One specific implication of this statement is a sharp knee shape variation in the observed data due to loading conditions, ambient temperature or substantial device/system characteristic changes. This can be seen as a critical point in which the device degradation pattern starts growing at a faster rate. To find the knee, a line is regressed from the first to the last measurement. The knee lies in the region that has the largest amount of deviation from the regressed line. $R_{ds(on)}$ behavior is modeled in (4.1):

$$log(R_{ds}) = \begin{cases} a_1 \times t + b_1, & t < t_0 \\ a_2 \times (t - t_0) + b_2, & t \geq t_0 \end{cases} \tag{4.1}$$

where t_0 is a point in the neighborhood of the knee and a_1, b_1, a_2 and b_2 are regression parameters. In this framework, each parameter has a prior probability density function that expresses the prior beliefs in the true parameter values. The proposed priors are Normal (Gaussian) distributions $N(\mu, \sigma)$ where the means (μ) are reasonable guesses for the parameter values based on some initial test results. The algorithm estimates the posterior $P(\theta|D)$ distribution using a limited number of sampled parameters. It starts by generating a candidate sample θ^c of parameters from the parameter space with a probability $p(\theta^c)$ and likelihood $P(D|\theta^c)$. The next candidate $\theta^{c'}$ is selected using a random jump from θ^c. The new candidate is always accepted if it improves the ratio $r = \frac{P(\theta^{c'}|D)}{P(\theta^c|D)} \times \frac{P(\theta^{c'})}{P(\theta^c)}$, otherwise the candidate has a second chance of acceptance through comparing r with a randomly generated number, $0 < \alpha < 1$. If $r > \alpha$ the new candidate is accepted. Meanwhile, the old candidate is chosen as the new candidate for the next iteration. After enough iterations (greater than 20000 as suggested by [54]) the algorithm stops, and convergence for posteriors is reached as shown in Fig. 4.1 and Fig. 4.2, respectively.

As of the main advantages of using this method, Uncertainty is a natural outcome of the process during the parameter extraction estimation, and learning algorithm development, which highlighted are in Fig. 4.3.

It should be noted this method avoids the high number of damage accumulation in comparison with conventional reliability-based prediction methods where a large number of units are âtestedâ under same conditions, and consequently, the confidence interval of the model is derived. Therefore, initially, a single device is considered in both the accelerated test set up and nominal (practical) operating points of the converter. Also, the importance of the proposed method becomes apparent when either there are negligible changes in the fault cursor for a significant time or there is a substantial change in the operating conditions.

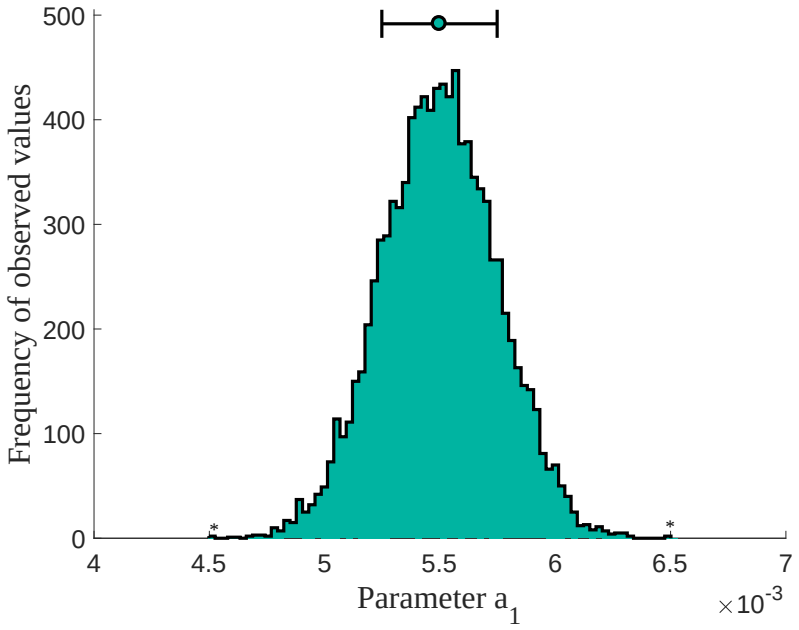


Figure 4.1: **Parameter estimation**: The probability density function of the posterior as the unknown parameters, and verification MCMC algorithm.

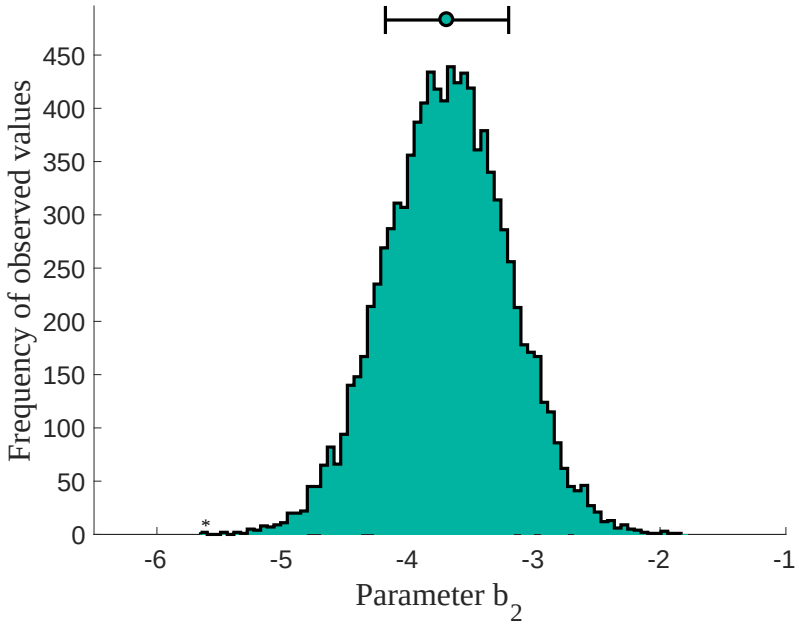


Figure 4.2: **Parameter estimation**: The probability density function of the posterior as the unknown parameters, and verification MCMC algorithm.

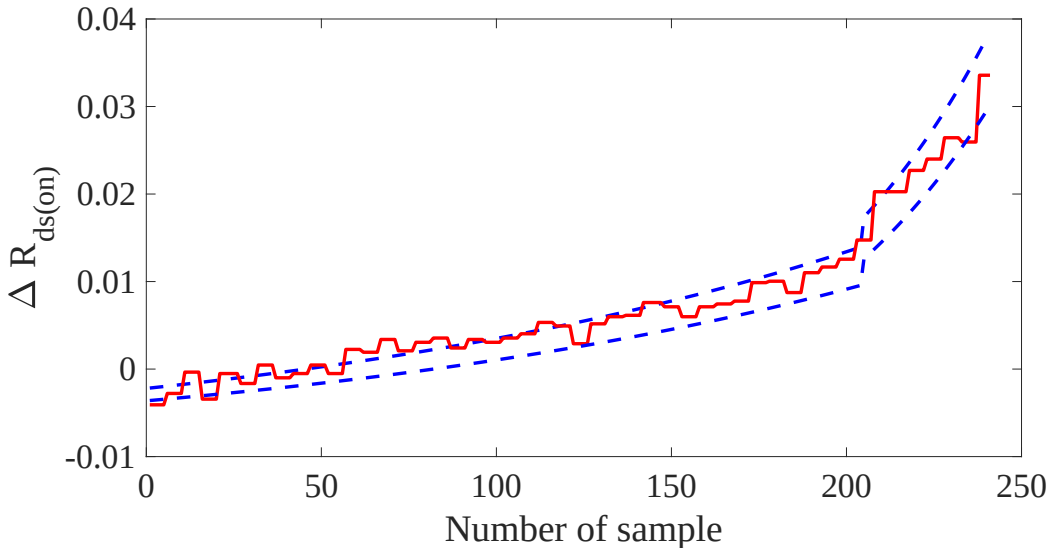


Figure 4.3: **Bayesian calibration**: The output results of the algorithm for pattern recognition within the confidence interval. Red: drain-source resistance changes, blue: the estimated resistance variation within the specific confidence level after the data filtering and highlighted near the knee point.

4.2 Recurrent neural networks

The RNN is a branch of neural networks specialized for analyzing a sequence of data notated by $X = [x_1 \quad x_2 \quad ... \quad x_\tau]$ where τ is the number of input sequences. Fig. 4.4 depicts an RNN computation node, i.e. neuron, and its unrolling version where $\tau = 4$. A neuron passes the information from the past to the current time by sharing the information and updating the cell state, c; therefore, the sharing process enables RNN to model a behavior of a time sequence. In a standard RNN cell, and the given input X, the cell output $Z = [z_1 \quad z_2 \quad ... \quad z_\tau]$ is computed as:

$$i_t = W_i x_t + W_c c_{t-1} + b_i \tag{4.2}$$

$$c_t = \zeta(i_t) \tag{4.3}$$

$$o_t = W_o c_t + b_o \tag{4.4}$$

$$z_t = \xi(o_t) \tag{4.5}$$

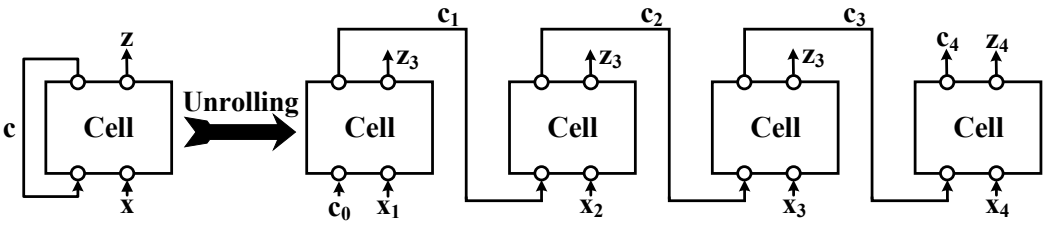


Figure 4.4: **Recurrent Neural Networks**: The schematic of standard RNN cell and its unrolling version for four input time sequence

where $\zeta(\cdot)$ and $\xi(\cdot)$ are nonlinear activation functions, W_i is input weight, W_c is the state cell weight, W_o is the output weight, and b_i, b_o are biases for input and output values, respectively. Knowing $Y = [y_1 \quad y_2 \quad ... \quad y_\tau]$ as the referenced output, the loss function can be defined in:

$$L(Z, Y) = \sum_{t=1}^{\tau} L(z_t, y_t) \tag{4.6}$$

In (4.6), $L(z_t, y_t)$ can be mean squared error of a regression function or cross-entropy for classification purposes.

$$\underset{\theta}{\text{argmin}}\ L(z(\theta), Y) \tag{4.7}$$

where θ is a network vector model described as: $\theta = [W_i \quad W_c \quad W_o \quad b_i \quad b_o \quad c_0]$. To extract the proper weight factors of the proposed model, Back Propagation Through Time (BPTT) algorithm can be applied to train the RNN network [55, 56]. In the standard RNN, one of the major issues of using BPTT is losing the sensitivity of cells to the earliest inputs due to the chain of partial derivation. This phenomena is known as vanishing gradient problem and eventually prevents the network reaches to the earliest states in deep RNN [57].

4.3 Deep Learning Reliability Awareness of Converters at the Edge (Deep RACE)

This section presents a framework of online reliability awareness system for power device diagnostics model and system integration for prognostic development. The extended version of RNN is applied, called LSTM for data training, and edge computations. Then, a new architecture is proposed that leverages the benefits of advanced power electronics converter, communication, control structure, and the cloud-edge platform for real-time prediction. First, the work focused on how the power MOSFET degradation behavior was modeled using deep LSTM network. Then, the new architecture is presented for the online system integration through the edge-cloud computation platform.

4.3.1 Long short-term memory

To prevent the vanishing gradient, LSTM is introduced, which proposes a subset of the cyclical node inside its cell known as "memory" [58]. An LSTM cell has three vectorized sigmoid (σ) functions, which each individual function operates as a gate and controls the flow of information passing through the cell — the input, output, and forget gates. Each gate maps its input to $S = \{s_i | s_i \in [0, 1]\}$, where zero is a closed gate and one means the gate is open. Moreover, the cell state (memory) is preserved by C as a new candidate. The information of new candidates should be stored in cell state, and introduced by $\tilde{c}$ shown in Fig. 4.5. Therefore, the output of each LSTM cell is:

$$i_t = \sigma(W_i v_t + b_i) \tag{4.8}$$

$$f_t = \sigma(W_f v_t + b_f) \tag{4.9}$$

$$o_t = \sigma(W_o v_t + b_o) \tag{4.10}$$

$$\tilde{c}_t = tanh(W_c v_t + b_c) \tag{4.11}$$

$$c_t = f_t \odot c_{t-1} + i_t \odot \tilde{c}_t \tag{4.12}$$

$$h_t = o_t \odot tanh(c_t) \odot \tilde{c}_t \tag{4.13}$$

where $\theta = [W_i \quad W_o \quad W_f \quad W_c \quad b_i \quad b_o \quad b_f \quad b_c \quad c_0]$ is a network model that should be trained, and $v_t = [x_t \quad h_{t-1}]$, $\odot$ is Hadamard product. The input gates (4.8) decide what portion of current input will be stored in cell memory and forget gate (4.9) chooses which portion of memory should be erased. Therefore, new information (candidate) will be mined by (4.11), and the cell memory will be updated in (4.12). Moreover, the output gate (4.10) decides which part of cell memory should affect the LSTM output at time t, and finally the LSTM output value is calculated in (4.13).

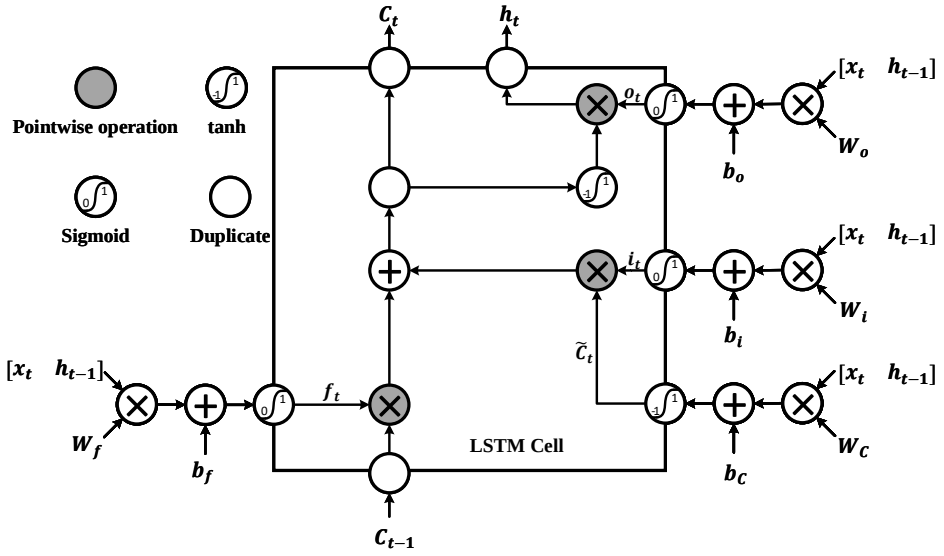


Figure 4.5: **A single LSTM cell**: Inside of an LSTM cell consisting of three gates and the state of the cell is preserved by variable c_t.

To model the complexity of $\Delta R_{ds(on)}$ propagation, using an individual cell is not sufficient. Therefore, there is a need to design a deep LSTM architecture to increase the network depth, and build up the progressive pattern recognition of sequential data in both coarse and fine grain directions. In this real-time system, a stacked LSTM is developed to generalize the existing pattern in power MOSFET degradation.

4.3.2 Device model training

For the precursor of device failure degradation, we consider the trajectory resistance of drain-source of power MOSFET during ON time (i.e., $\Delta R_{ds(on)}$). As $\Delta R_{ds(on)}$ is intrinsically a time series, we design the model using deep LSTM network, where the training is developed by aggregating data from different devices with the same technologies. For each network training iteration of power devices, a batch should be created. Therefore, for predicting the next n samples of $\Delta R_{ds(on)}$ based on provided last input sequence (τ), batch should consist of $\Delta R_{ds(on)}$ with the size of $(\tau + n)$. In each batch, increasing of device vectors help to expand the network and model the complex degradation properly that results in higher accuracy of the predicted trajectory. The 3D-batch tensor configuration for training iteration is shown in Fig. 4.6. The dimension of vector R^k_{mt} is characterized based on the *input size* shown by k, where m is the available devices for training, and t is the sequence.

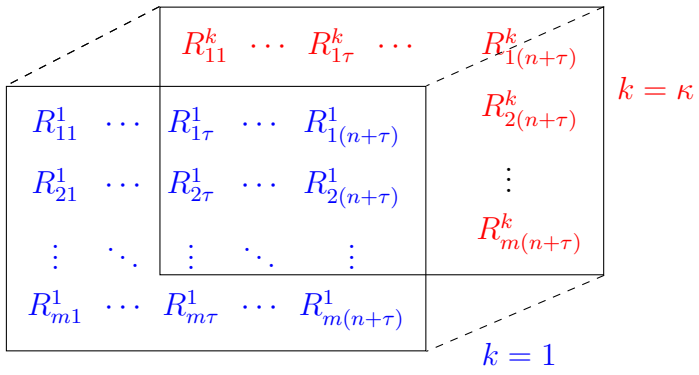


Figure 4.6: **Batch tensor configuration**: Three dimensional batch tensor with a characterized vector R^k_{mt}.

For designing of deep LSTM network, we also need to consider two major parameters known as *number of hidden layers*, and the *number of stacked layers*. The number of hidden layer is the dimension of vectors generated in equations (4.8)-(4.13). The vector size can be changed by altering the weight tensor shape and bias tensor shape defined in equations (4.8)-(4.11). Increasing the hidden layer is interpreted as in-

creasing the "memory" size of the LSTM and its capacity to learn existing complex pattern in a signal. The stacked layer is the other parameter to increase the depth of the LSTM network. Here, by stacking the cell up together in a way the h_t of one cell is used as an input to its adjacent top cells. Acquiring proper values for these parameters can be done by exploring the space-based design constraints (e.g., system accuracy, processing time, and power consumption) [59]. The architecture of stacked LSTM with the input sequence of τ and the stacked layer size of ℓ is depicted in Fig. 4.7.

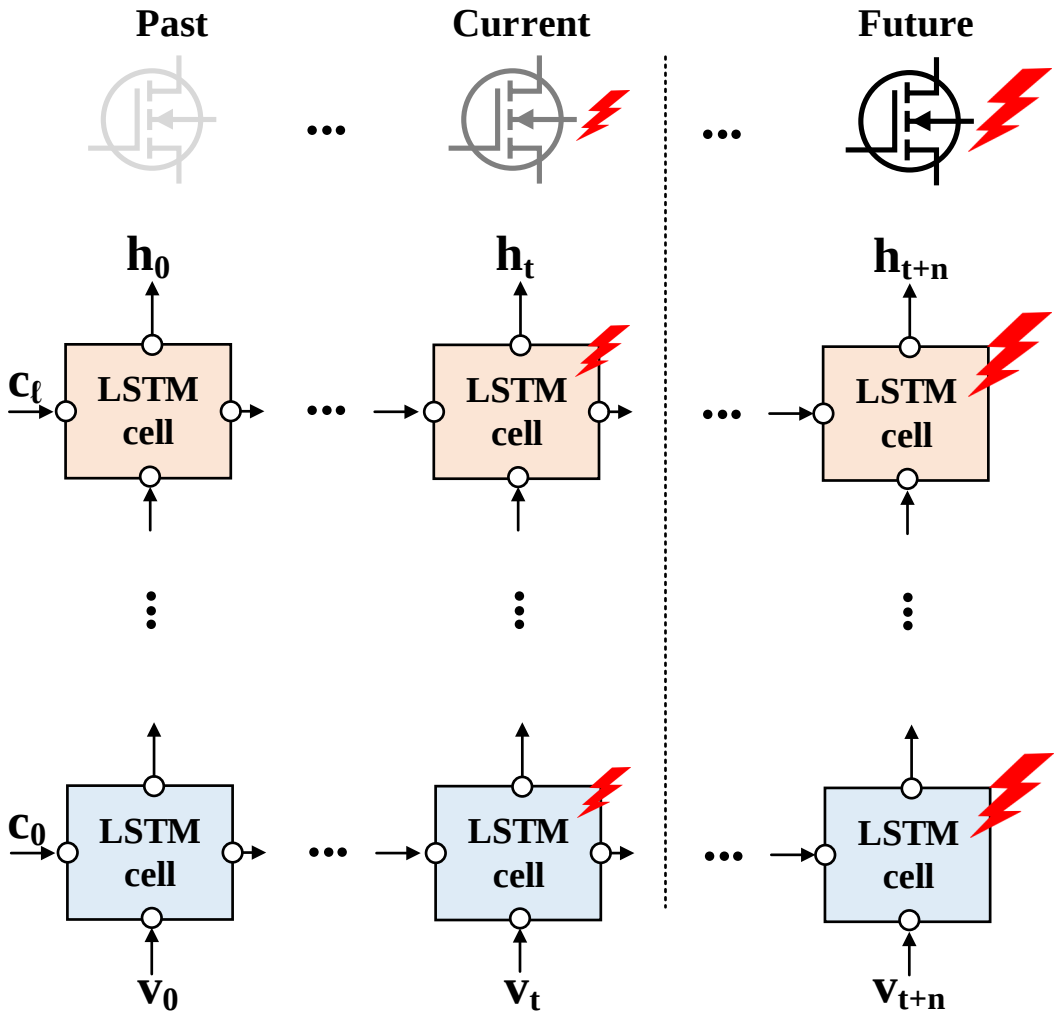


Figure 4.7: **The stacked LSTM**: An unrolled LSTM cell predicts the next n samples of $\Delta R_{ds(on)}$ based on last sensed data.

Algorithm 1 Training the deep LSTM network

Input: $X_{training}, Y_{training}, X_{test}, Y_{test}, \tau, m, n, \ell, k, \epsilon, e_{th}, it_{max}$
Output: $\theta_\lambda; 1 \leq \lambda \leq \ell, \theta_d$ ▷ Network models

```
computation_graph ← LSTM(hidden_layer, ℓ)
error ← ∞                                              ▷ Initialize the test error
ȷ ← 0
init_rand(θ_λ for λ in [1...ℓ])   ▷ Initialize LSTM network models from truncated normal distributions
init_rand(θ_d)
while (ȷ ≤ it_max) or (error ≥ e_th) do
    X_batch, Y_batch ← generate_data(X_training, Y_training, m, n, τ, k)
    ΔR_ds(on) ← inference(computation_graph, X_batch, [θ_λ for λ in [1...ℓ]], θ_d)   ▷ Predicted ΔR_ds(on) for training
    error_training ← L(ΔR_ds(on), Y_batch)
    [θ_λ for λ in [1...ℓ]], θ_d ← optimizer(computation_graph, error_training, [θ_λ for λ in [1...ℓ]], θ_d)
    x_test, y_test ← generate_data(X_test, Y_test, m, n, τ, k)
    ΔR_ds(on) ← inference(computation_graph, x_test, y_test, [θ_k for k in [1...ℓ]], θ_d) ▷ Predicted ΔR_ds(on) for test
    error ← L(ΔR_ds(on), y_test)
    ȷ ← ȷ + 1
end while
```

Since the output vector $h_t \in [-1, 1]$, it is required to denormalize the deep LSTM network output to actual system measurement. Therefore, a fully connected layer is added to the output of stacked LSTM to map h_t to the predicted $\Delta R_{ds(on)}$ at time t as shown in Fig. 4.8.

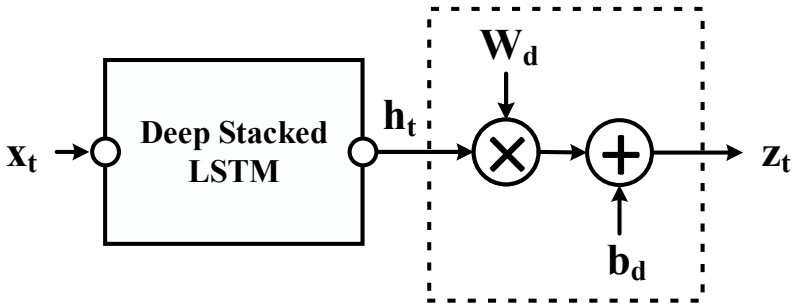


Figure 4.8: **The proposed deep LSTM network model**: A linear layer is added to the deep stacked LSTM to map h_t to on-line measured ΔR at time t.

Based on modified deep LSTM structure, the network models are described as:

$\theta_\lambda = [W_{\lambda_i} \quad W_{\lambda_o} \quad W_{\lambda_f} \quad W_{\lambda_c} \quad b_{\lambda_i} \quad b_{\lambda_o} \quad b_{\lambda_f} \quad b_{\lambda_c} \quad c_{\lambda_0}], 1 \leq \lambda \leq \boldsymbol{\ell}$. In our model, k is the index of stacked layer, and $\boldsymbol{\ell}$ is the stacked layer number. In each LSTM cell, $\theta_d = [W_d \quad b_d]$ will be trained by the cloud, and it will be used at edge for real-time prediction.

CHAPTER 5: SYSTEM INTEGRATION

5.1 Introduction

This section presents the framework of the online reliability awareness system for diagnostic modeling and prognostic development. The proposed architecture uses advanced communication, control and power structure for reliability analysis. The four major sections are a) power stage development, b) sensing unit, c) control system and d) cloud computation networks.

5.1.1 Real-time edge analysis

The edge converter has its local controller equipped with an embedded SoC to predict the power transistor degradation. The μ-controller unit is responsible for modulating the gate signals for the power converter control, and continuous monitoring the voltage, current, and temperature of power converters. The captured data also will be transferred to the cloud to perform the reliability analysis for each edge node. The SoC runs inference section of deep LSTM and estimates the trajectory device resistance $\Delta R_{ds(on)}$ based on the trained network models from the cloud. The real-time edge node computation of switching converter through Deep RACE is shown in Fig. 5.1.

5.1.2 Data training and batch aggregation on the cloud

Despite conventional methodologies, where the reliability models were extracted from costly accelerated life tests, we added the cloud server for real-time system operation. The cloud stores the actual data from the switching converter and trains them for reliability model exploration. In this context, the cloud side update edge Deep LSTM models to increase the confidence interval of the prediction, and estimate

the remaining useful life the devices. While the edge nodes use local computing power to perform the prediction, it relies on the cloud for training the network and updating the aggregated device models. To increase the confidence interval of the power devices and the system operation, we defined ΔR_t as the predefined threshold. Once the error of predicted device resistance $\Delta R_{ds(on)}$ is greater than the preset threshold ΔR_t, the network models will be automatically updated through training the network on the cloud server.

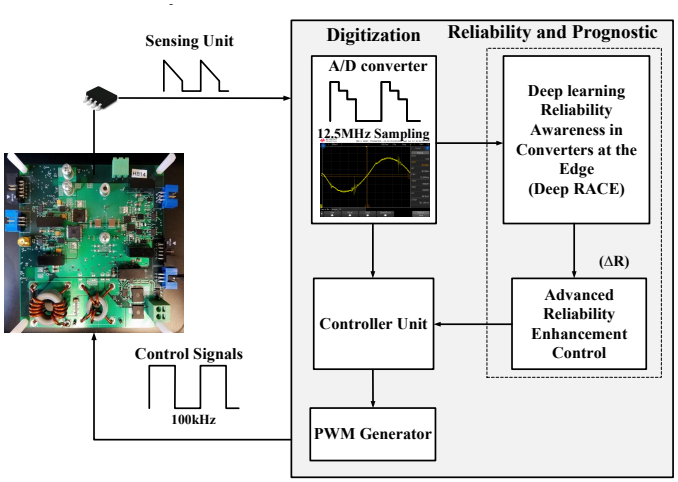


Figure 5.1: **The edge node diagram**: It consists of a μ-controller and AI SoC to generate gate signals and predict the trajectory resistance of power transistor.

5.2 Architecture for real-time system monitoring

5.2.1 Proposed physics of failure-statistics model using cloud computations

To enable an active diagnostic/prognostic reliability awareness system, a new baseline architecture for investigation and predictive model development is proposed as shown in Fig. 5.2. This architecture utilizes the most advanced communication, control, and power structures to address the system robust operation with IoT approach. The overall system is categorized into four major sections as a) power stage, b) sensing elements, c) control units, d) cloud networks. In the power stage, the most advanced power electronics converter without any compromising on the system performance will be designed and operated under nominal conditions. The power converter can be

tested under different ambient temperature or humidity for robustness evaluations. The second stage consists of accurate high current and voltage sensors to capture characterization and enable a proper Data Acquisition System (DAS) for converter monitoring under switching. In the controller unit, all the digitization process of the measurement signals and transferring the signal to the cloud, as well as an advanced analogue/digital controller will be performed. This section is a local controller of the converter, which can effectively implement the predictive models defined in the other layers. Lastly, the cloud network, which consists of multi-processors to run the complex parallel computations for model derivation with the multi-physics co-simulations, as well as the deep learning algorithm for parameter calibrations. This section potentially is a data storage area, which is available for data processing, and advanced algorithm development.

5.2.2 Hardware system setup

To verify the analysis, a buck converter consists of four GaN modules (GS66516B) is designed in a parallel configuration. The power stage schematic of the synchronous buck converter is shown in Fig. 5.3. Considering all the precautions for optimized gate loop path, reducing magnetic interface, and thermal management, the prototype was built on a four-layer PCB. The inner layers board were utilized to conduct the switching node current, which also increases the surface to dissipate the heat generation. The input signals for the gate driver generated from the micro-controller. The +9V isolated power supplies for the gate drivers were clamped with a Zener diode at +5.6V to make sure the devices are fully ON in the saturated region, but still lower than the absolute borderline for gate signals (+7V) recommended by the manufacturer. The more detailed analysis of this design can be found in [60], and the main components used for the prototype design are provided in Table 5.1.

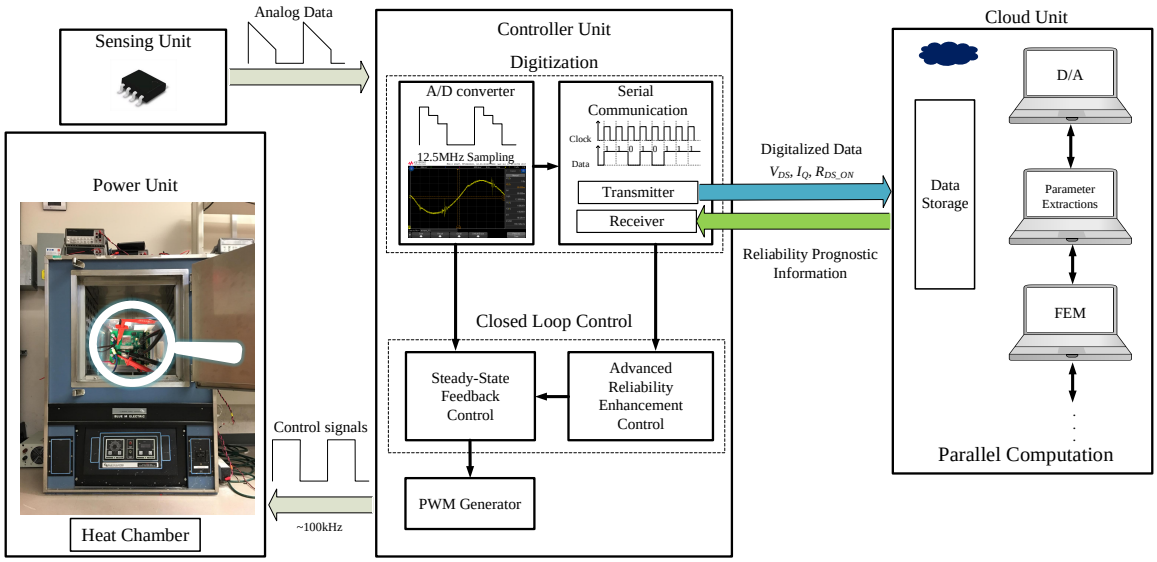


Figure 5.2: **New IoT approach for reliability assessment**: DAS for characterization of power converters, and multi-process computation on cloud networks. The proposed infrastructure architecture provides feasibility of data-processing techniques for adaptive prognostics in power electronics converters.

5.2.3 Prototype robustness verification

For precise assembling and soldering of the GaN modules on the PCB, the re-flow oven (LPKF ProtoFlow S) for surface mount devices is used. To verify the performance robustness of the converter operation, for the first two weeks, the converter was running with no heat-sink, but with Fluorinert (FC-40), as a non-electrical conductive liquid. The Fluorinert is elected because of the advantage of having a wide range of boiling temperature, and very high-volume electrical resistivity. These capabilities provide a symmetric temperature distribution and isotherms behavior. Then, DC input bus voltage was set at 60V and the switching frequency of the gate drivers fixed at 100kHz and 50% duty cycle. This forces 14A current passes through the RL load with an impedance of 2Ω. The converter was successfully tested for two weeks at the 400W nominal power.

Afterward, the heat-sink was attached to the board to make the junction temperature of the GaN devices at the nominal current operation less than 80 in the standard

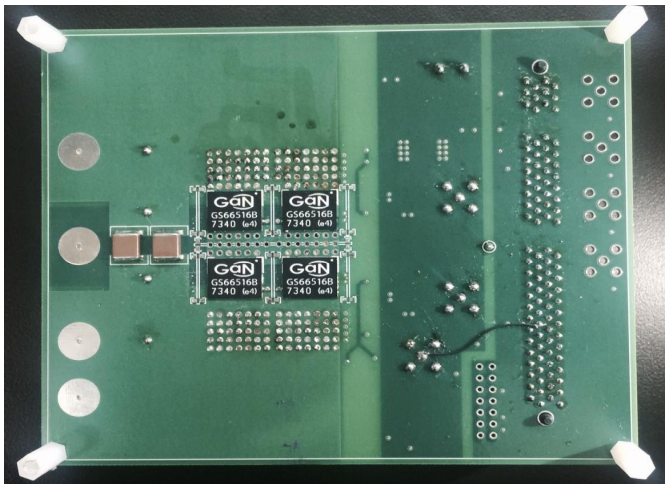


Figure 5.3: **Hardware prototype**: The buck converter designed in four layers.

room temperature. For this test, the automatic software-based protection system was built-up to provide the feasibility of continuous setup operation. The prototype was tested for more than 30 billion cycles with an active cooling system.

Table 5.1: Components in Converter Circuit Design

Item	Manufacture Part No.	Description
1	GS66516B	GaN transistors
2	SI8271GB-IS	Isolated gate driver
3	PES1-S5-S9-M-TR	Isolated power supply
4	ACM4520-142-2P-T000	Common mode choke filter
5	CD0603-Z3V9	Zener diode
6	C1608X7R1H104K080AA	0.1uF Bypass capacitor
7	C5750X7R2E105K230KA	1uF Bypass capacitor
8	ERJ-3BQF1R0V	1Ω Resistor
9	ERJ-3EKF20R0V	20Ω Resistor
10	ERJ-FC0603E50R0BST1	10Ω Resistor
11	ERJ-PA3F4701V	4.7kΩ Resistor

To enable continuous operation of the switching converter, a supervisory system control was designed. This system is implemented in Python, where power supply units and all measurement are controlled remotely and operated continuously as shown in Fig. 5.4. Two threads, one for measurement, and one for safety concerns are considered. The measurement thread will capture the scope data, and stores in

the cloud networks. If the load current is within the safety range, the $R_{ds(on)}$ will be calculated based on the captured raw data.

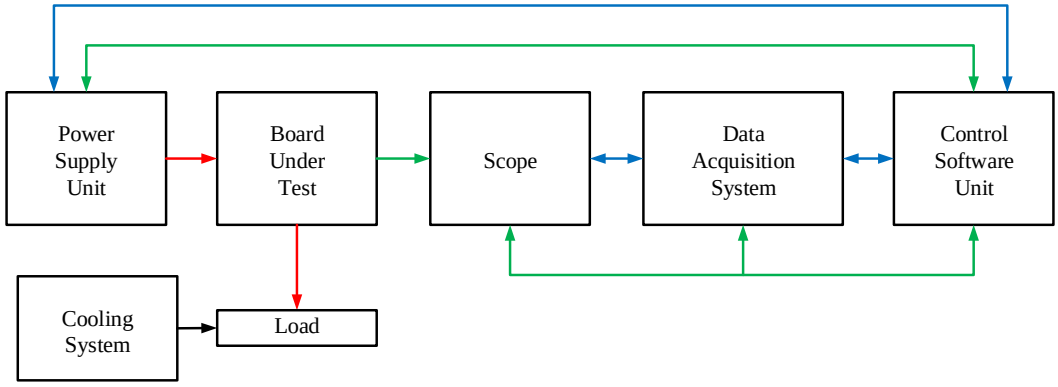


Figure 5.4: **Data acquisition system**: Supervisory system control was designed for data collection and converter protection. red: power path, blue: control signals, and green: sensing signals.

The calculation is relying on the voltage measurement of the bottom switches (N2890A), and the differential voltage measurement (N2791A) for top devices, as the inductor current, will be captured by the high bandwidth current probe (TCP303). To avoid the effect of noise during transients and improve the measurement accuracy, $R_{ds(on)}$ will be calculated only during 40% to 60% dury cyles in both rising and falling of inductor current.

The second thread for the safety requirement will repeatedly acquire the power supply status. Depending on the status or the output power, a shutdown will be initiated. This is mainly based on the deviation between actual power and the desired power (400W). If the deviation of the load current exceeds 3%, an emergency shutdown will be initiated, where the detailed thread is shown in Fig. 5.5.

Moreover, automated data acquisition system for the switching converters is designed. This system is implemented in Python, and all the units were operated continuously over 30 billion electrical cycles and data also stored on the cloud shown in Fig. 5.6 whereas the second system operates over 100 billion electrical cycles in Fig. 5.7.

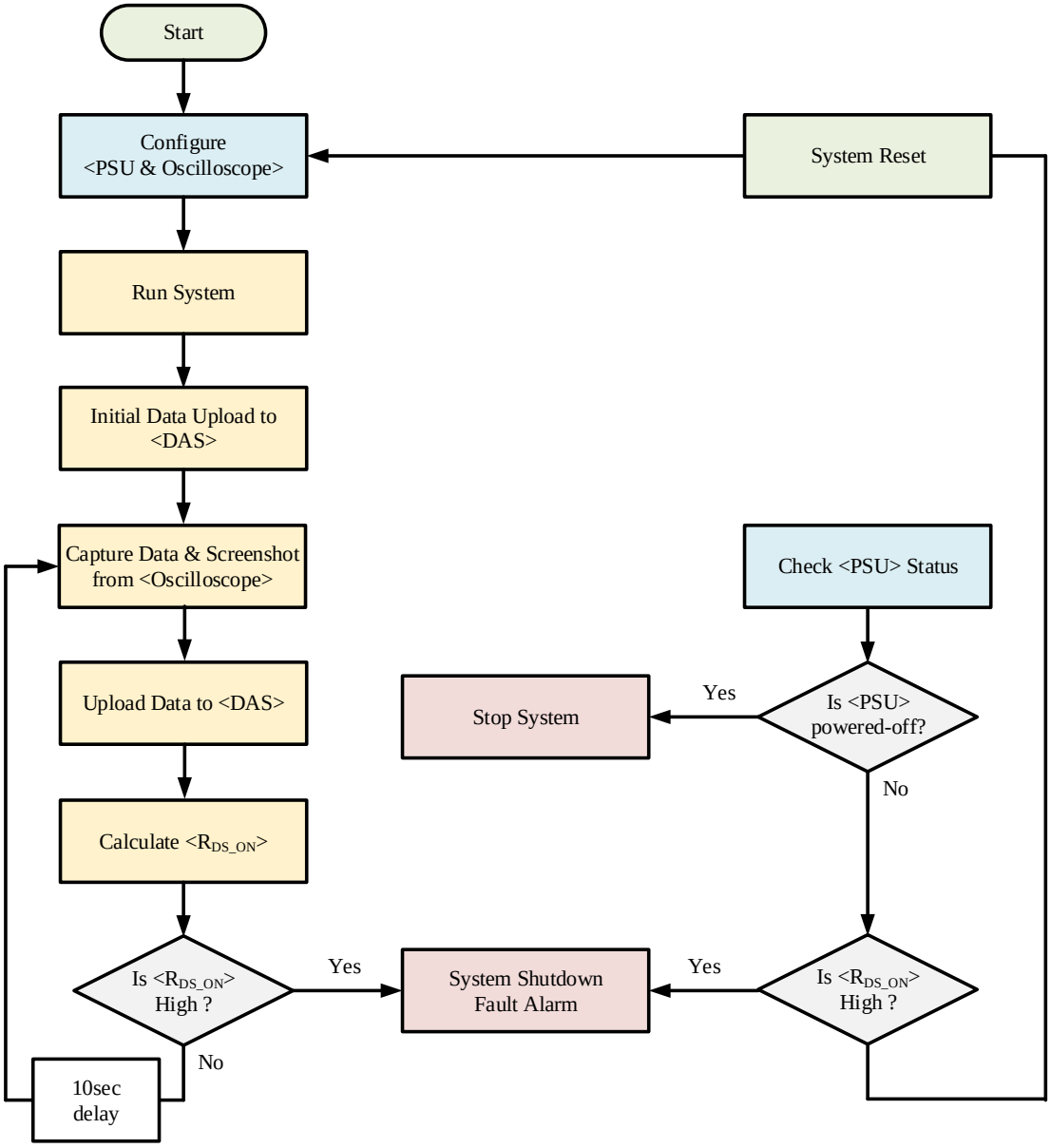


Figure 5.5: **Data acquisition system**: The thread is provided for device characterization and resistance measurement.

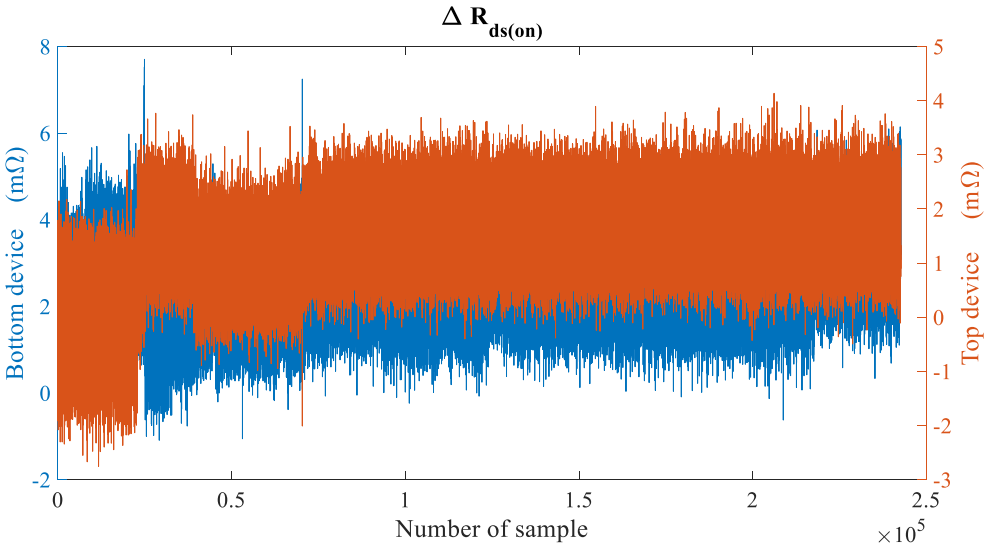


Figure 5.6: **The filtered on-resistance variations**: The 400W buck prototype was tested over 30G cycles with continuous operation at 100kHz switching frequency, and drain-source resistance variations was captured automatically.

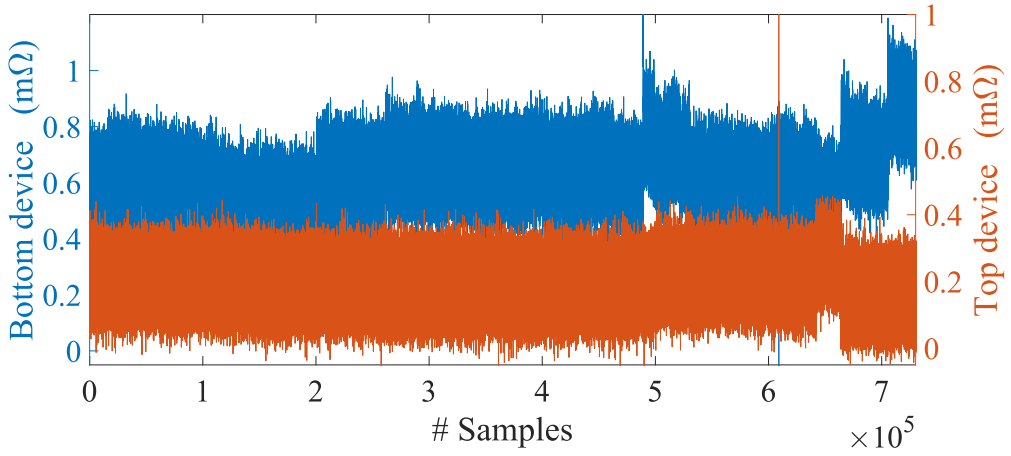


Figure 5.7: **The filtered on-resistance variations**: The buck converter was tested over 100 billion electrical cycles $400W$ and $100kHz$. The drain-source on-resistance variations was captured automatically, and stored on the cloud networks.

CHAPTER 6: EXPERIMENTAL RESULTS

6.1 Introduction

The performance of the proposed real-time reliability analysis was examined for training the data and applying the Deep RACE. This section describes the testing scenarios, the hardware setup, and the experimental results. First, the proposed method is verified using the experimental setup results from the available data in [30], and the simulated package in the FEA. The details of the concept are shown in Fig. 6.1

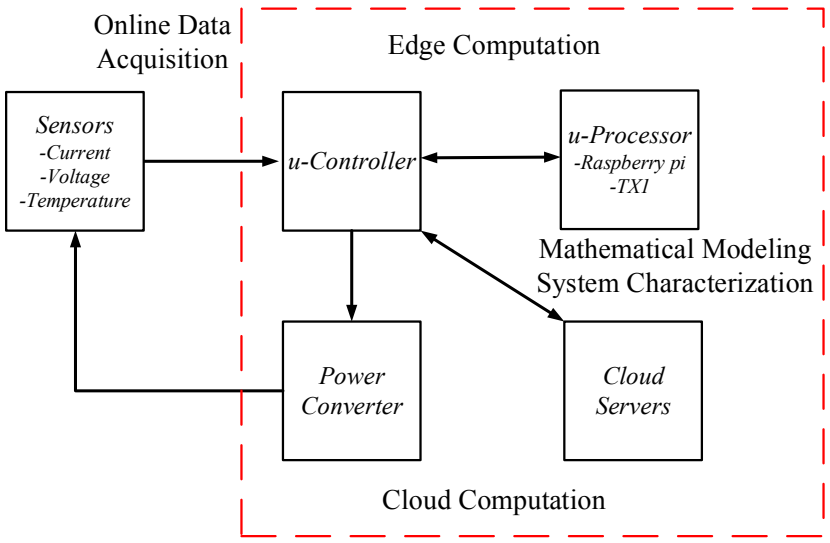


Figure 6.1: **The proposed reliability solution**: The advanced solution leverages the benefits of Internet of Things for reliability analysis using edge/cloud.

6.1.1 Experimental training of power transistors

On the cloud server, we used Intel Xeon CPU E5-2640 to train the deep LSTM network, where we initially modeled Si-power MOSFETs. The experimental data sets

for the training of the power MOSFET (IRF520NPbf) are provided in [30]. Then, a new set of data is predicted based on the trained system at the edge with no prior knowledge. For the application with higher window resolutions (i.e., higher output sequence), the network input sequence should also be increased to minimize the prediction error. The experiments verified for the prediction of $\Delta R_{ds(on)}$ degradation behavior, even limited data sets were enough for training the system characteristics. Therefore, the Deep RACE is trained to estimate the next 104 samples (equals to one minute ALT). Table 6.1 summarizes the deep LSTM network parameters.

Table 6.1: The parameters for LSTM network training

Item	Parameter	Description	Value
1	k	Input size	1
2	τ	Input sequence	21
3	e_{th}	Error threshold	10^{-5}
4	n	Output sequence	104
5	it_{max}	Maximum iterations	1000
6	ϵ	Number of hidden layer	64
7	ℓ	Number of stacked layer	4
8	m	Number of device for training	4

The Google TensorFlow framework is used to implement our stacked LSTM network model. Each LSTM cell is instantiated by calling $tensorflow.contrib.rnn.LSTMCell$ function where the number of "hidden layer" is passed as an argument to this function. In the next step, an array consists of $LSTMCell$ with the size of "stacked layer" is generated. Then, the array will be passed to the $tensorflow.contrib.rnn.MultiRNNCell$ function to create the stacked LSTM network. The network unrolling is accomplished through $tensorflow.nn.dynamic\_rnn$ function. We defined Mean Square Error (MSE) (6.1) as an objective loss function, and used $tf.train.AdamOptimizer$ method to minimize the function:

$$MSE = \frac{1}{n}\sum_{i=1}^{n}(y_i - z_i(\theta))^2 \tag{6.1}$$

where $z_i(\theta)$ is the predicted output trajectory from the Deep RACE, and y_i is the actual measurement of the device resistance.

6.1.2 Hardware setup design and verification

To evaluate the prediction system on edge, a hardware setup is developed. In this system, μ-controller controls the power converter, and also captures the voltage, and current of the power semiconductor and then transfers them to TX2 board for edge analysis. For the safety purpose, the automated supervisory control is designed for analogue data collection of the switching converter and also protects the system operation if the power conversion deviates more than 5%.

While the training process is performed in the cloud, we evaluated the prediction of the device resistance variation at the edge. Fig. 6.2, Fig. 6.3 Fig. 6.4, Fig. 6.5, and Fig. 6.6 illustrate five examples of predicted results of power devices and clarifies the effectiveness of the proposed algorithm. Although the apparatus behavior of each power device degradation looks similar, the microscopic observation of the transistors is different within the same time horizon. For instance, the trained network is expecting an exponential increment in a region of $\Delta R_{ds(on)} > 0.02\Omega$ for Dev#4. Then, the MSE was compensated through a learning phase at cloud-side, and the predicted resistance was increased linearly at the edge.

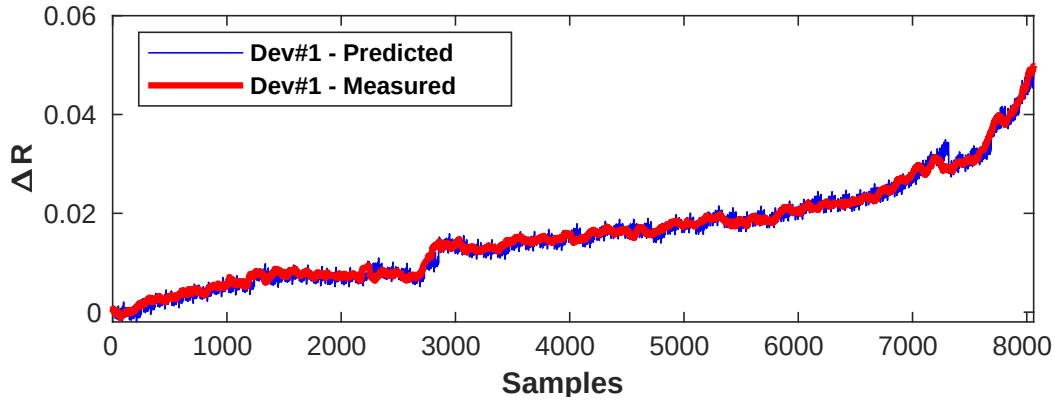


Figure 6.2: **Experimental results:** The prediction of $\Delta R_{ds(on)}$ variations of device-1 through Deep RACE method.

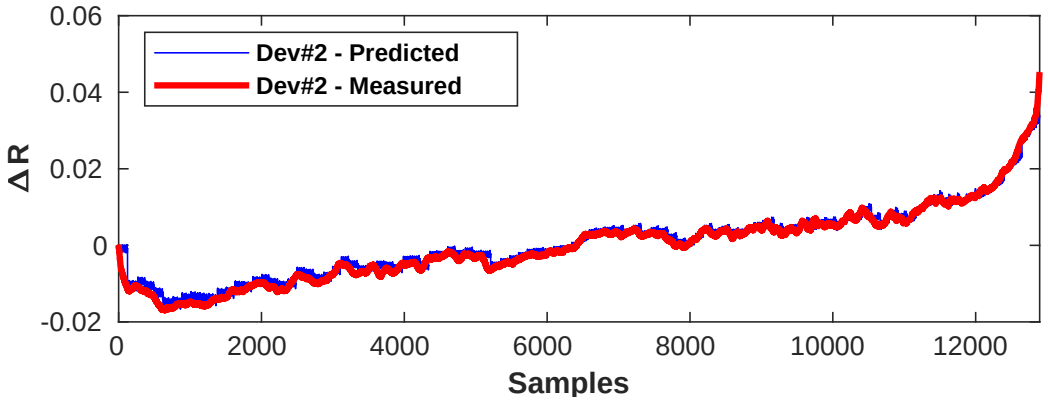


Figure 6.3: **Experimental results:** The prediction of $\Delta R_{ds(on)}$ variations of device-2 through Deep RACE method.

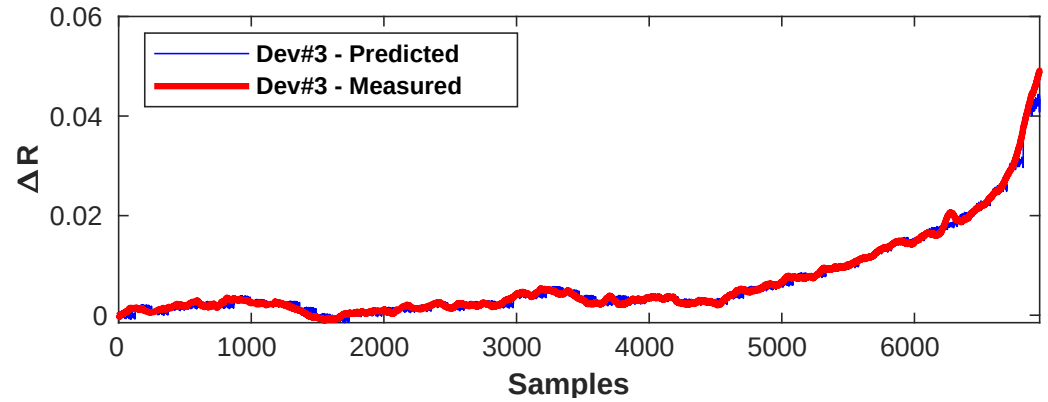


Figure 6.4: **Experimental results:** The prediction of $\Delta R_{ds(on)}$ variations of device-3 through Deep RACE method.

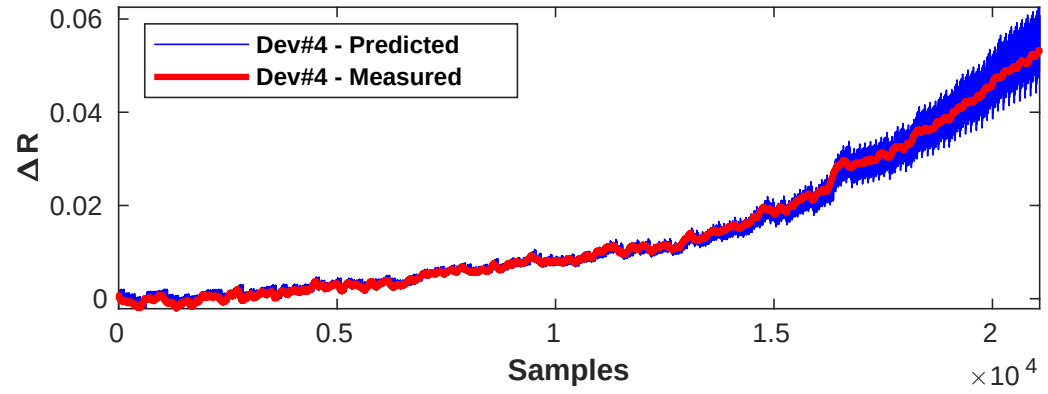


Figure 6.5: **Experimental results:** The prediction of $\Delta R_{ds(on)}$ variations of device-4 through Deep RACE method.

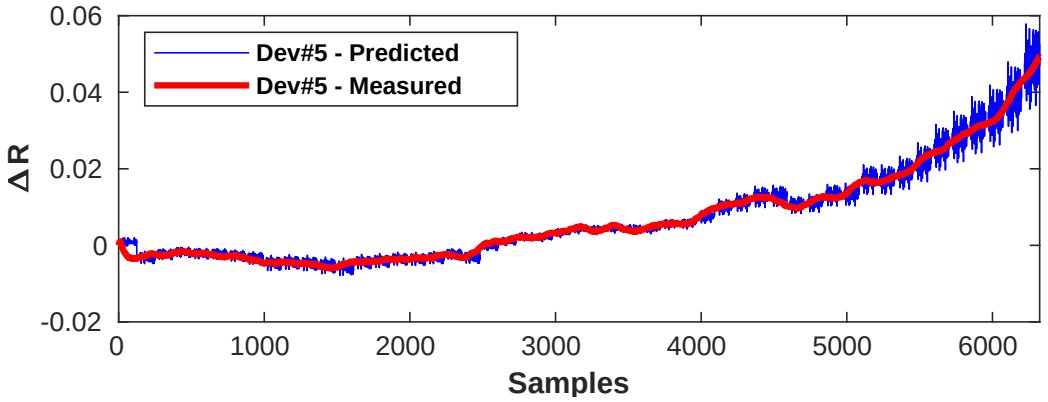


Figure 6.6: **Experimental results:** The prediction of $\Delta R_{ds(on)}$ variations of device-5 through Deep RACE method.

In the various scenarios of the system training, the trajectory resistance for Dev#5 is predicted based on learning from Dev#1 to Dev#4. Then, recursively we substitute the other devices to predict an unknown transistor resistance variations. We also verified the system characteristics from achieved the experimental results in two scenarios as MSE and error distribution in Table 6.2.

Table 6.2: Prediction error for the power MOSFET transistors

Devices	#1	#2	#3	#4	#5
log(MSE)	-13.61	-13.05	-13.95	-13.36	-12.94

The error distribution for system overall convergence error is defined as follows:

$$Error_{dist} = (y_i - z_i(\theta)) \tag{6.2}$$

where $z_i(\theta)$ is the predicted output trajectory from the Deep RACE, and y_i is the actual measurement of the device resistance ($\Delta R_{ds(on)}$ in our model). Fig. 6.7 depicts that the error distribution caused by Deep RACE method is less than 1% percent on average. Moreover, we compared our method with two well-known classical approaches (Kalman Filter, and Particle Filter) for power MOSFETs. Since it is very

crucial to detect the MOSFET resistance variation $\Delta R_{ds(on)} < 0.05\Omega$, we compared the average of absolute error at the detection point($=\Delta R_{5\%}$) in these methods by using (6.3), and the results are summarized in Table 6.3.

$$Error_{abs} = \frac{|\Delta R_{ds(on)} - \Delta R_{5\%}|}{\Delta R_{5\%}} \tag{6.3}$$

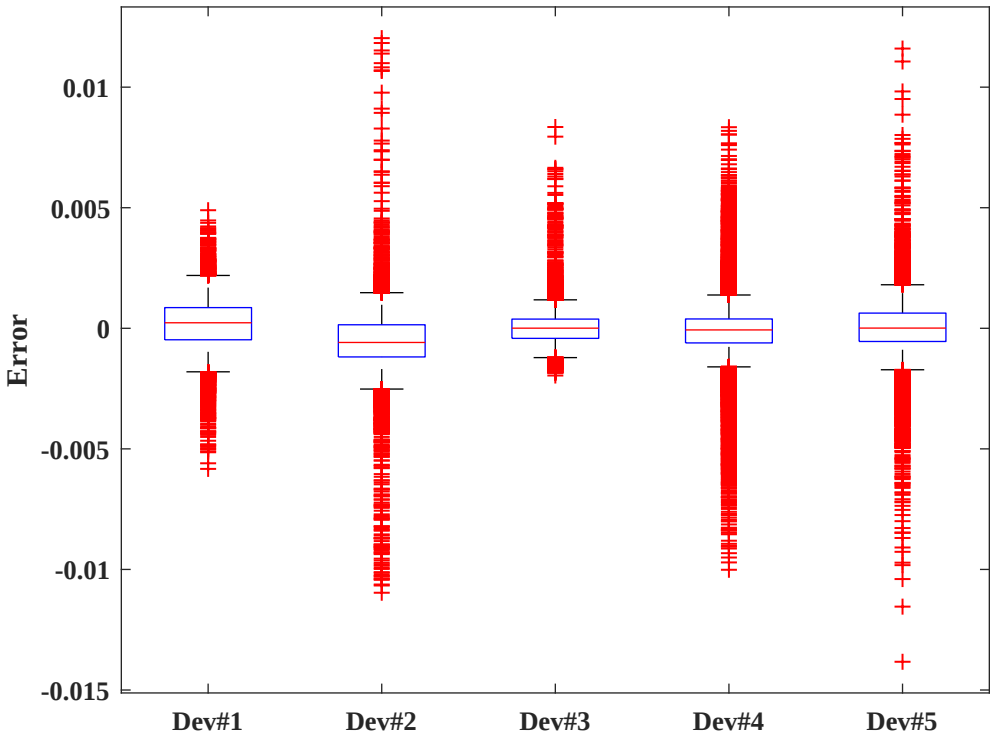


Figure 6.7: **Error distribution**: The box plot of errors for five power modules.

Table 6.3: The comparison of absolute average error of Deep RACE with the others

Method	Kalman Filter [61]	Particle Filter [30]	Bayesian Calibration [62]	Deep RACE
Average Absolute Error	17.75%	15.85%	15.00%	11.01%

We extended our exploration to consider the effect of power device data aggregation on prediction accuracy and risk analysis. For each data point, we ran 1000 Monte-Carlo test, and then the average of the whole sets of the test is picked. The results

show that by increasing the number of devices, the MSE decreases with an exponential rate depicted in Fig. 6.8.

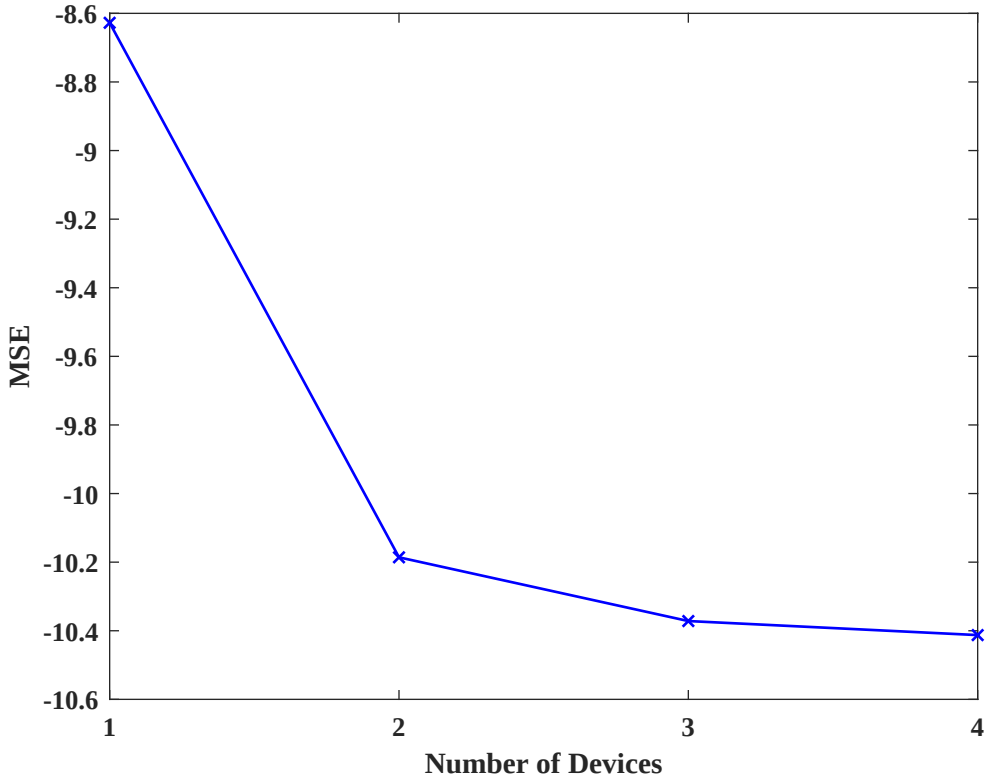


Figure 6.8: **The egde node diagram**: It consists of a μ-controller and AI SoC to generate gate signals and predict the trajectory resistance of power transistor.

6.1.3 Power consumption and processing time analysis

Furthermore, we evaluated the power consumption for the inference part of the network on an embedded TX2 board. The nVidia Jetson TX2 embedded SoC is used to evaluate the performance of Deep RACE approach at the edge. Table 6.4 summarizes the specification of embedded SoC.

We set the tensorflow configuration to `device_count = {'GPU': 0}`, where no computation carried out at the embedded GPU, and in the second approach we made it ON. For the matrix size of 125 (input sequence + output sequence), it was observed that the CPU processed 3.2x faster than GPU for one device prediction. This

Table 6.4: nVidia TX2 embedded module specification

CPU	Quad Cortex-A57 @ 2GHz + Dual Denver2 @ 2GHz
GPU	256-core Pascal @ 1300MHz
DDR	8GB LPDDR4 @ 1866MHz

performance degradation is because of data copying between CPU and GPU memory region – Note the DDR power consumption is higher for `'GPU': 1` scenario. In the other word, the amount of data is not enough for GPU to overlap the delay between data computation and movement. Increasing the number of devices that should be predicted per each edge node or increasing the prediction window resolution (*output sequence*) improves the performance for GPU since it performs more computation than CPU per each data movement. Table 6.5 summarizes the delay and power dissipation for two different cases.

Table 6.5: TX2 embedded board power consumption

	GPU: OFF			GPU: ON		
Module	CPU	DDR	CPU+DDR	GPU	DDR	GPU+DDR
Power (W)	1.07	0.80	1.87	0.166	0.90	1.06
Delay (ms)	26			85		

Now the work is extended the work to analyze a single unit of GaN power converter (Fig. 6.9 and Fig. 6.10) with the proposed hybrid condition-based prognostic. The simulation platform is designed for GaN on Si for ALT analysis based on the rated power of the semiconductor total loss discussed in Section 3.3. Four simulation results are provided for the training, and then the machine learning technique is applied. The results are provided in Fig. 6.11. Using the simulation analysis for the training of the system, the predicted results showed consistency within the time interval frame.

In summary, a novel framework for reliability assessment of power converters. The approach can be used for new technologies where limited information on their reliability is available. In this work, the focus was on the monitoring of the on-resistance

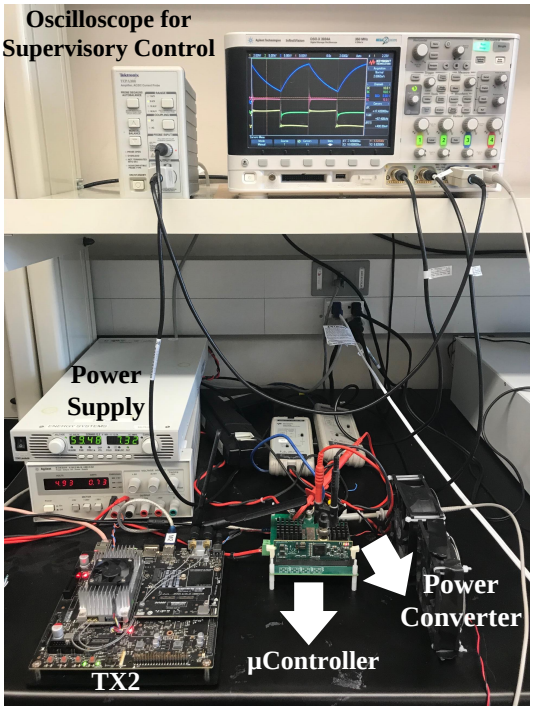


Figure 6.9: **Experimental verification**: The hardware setup was implemented including the high-frequency power converter controller by μ-controller, the SoC-TX2 for edge computation. The supervisory control is designed for the safety protection.

Figure 6.10: **Experimental verification**: Temperature rise control of the converter through thermal image.

variations over the time as a precursor for failure diagnostics of the synchronous $400W$ GaN buck converter at $100kHz$. The failure mechanism of solder fatigue with the energy-based modeling was discussed using FEA simulations. The RNN method is applied for data analysis and model calibration. The proposed network model verified with Si-MOSFET using the simulation analysis and available experimental. The work

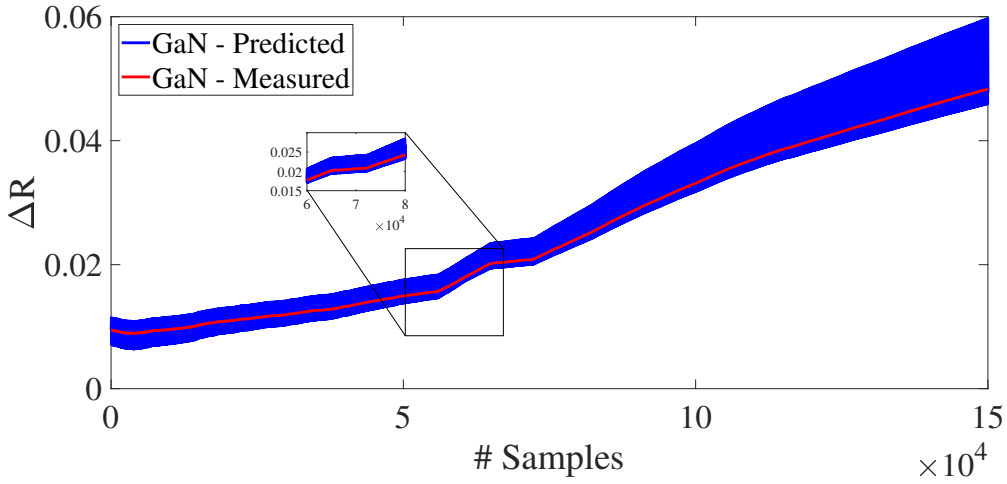


Figure 6.11: **Prognostic results**: The $R_{ds(on)}$ variations for GaN with Si-substrate using the FEA simulations, and only one set of data for training.

is also extended our network model to predict the GaN converter trajectory resistance using the simulation analysis. The more detailed analysis also carried out to observe the failure mechanism on the GaN power devices as proof of concept shown in Fig. 6.12 and Fig. 6.13.

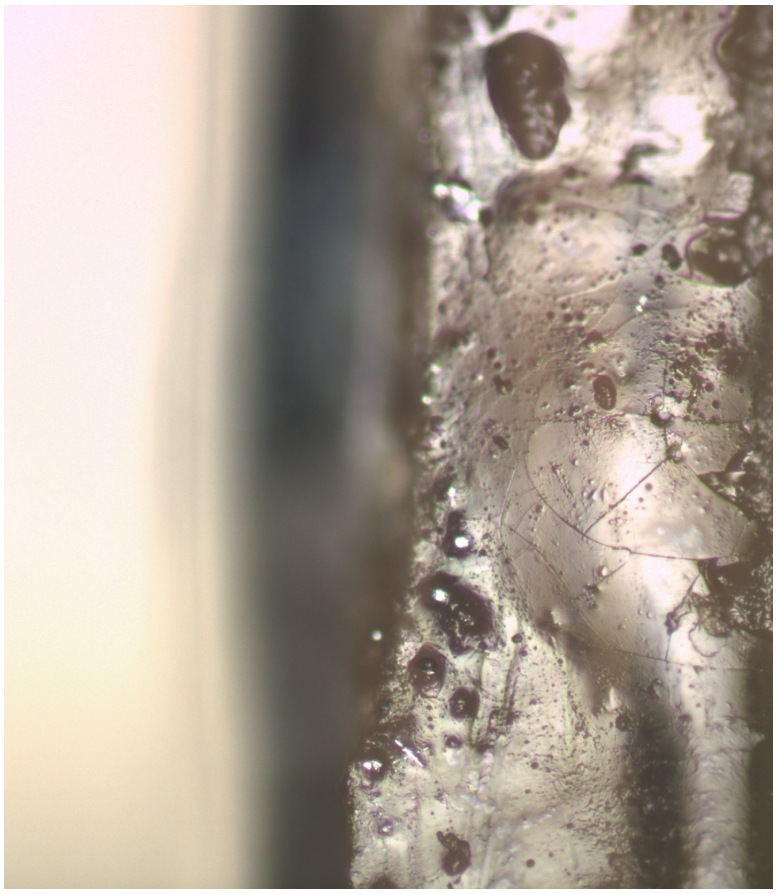


Figure 6.12: **Experimental results**: The solder degradation is observed on the source of GaN power devices in the defected device of the buck converter.

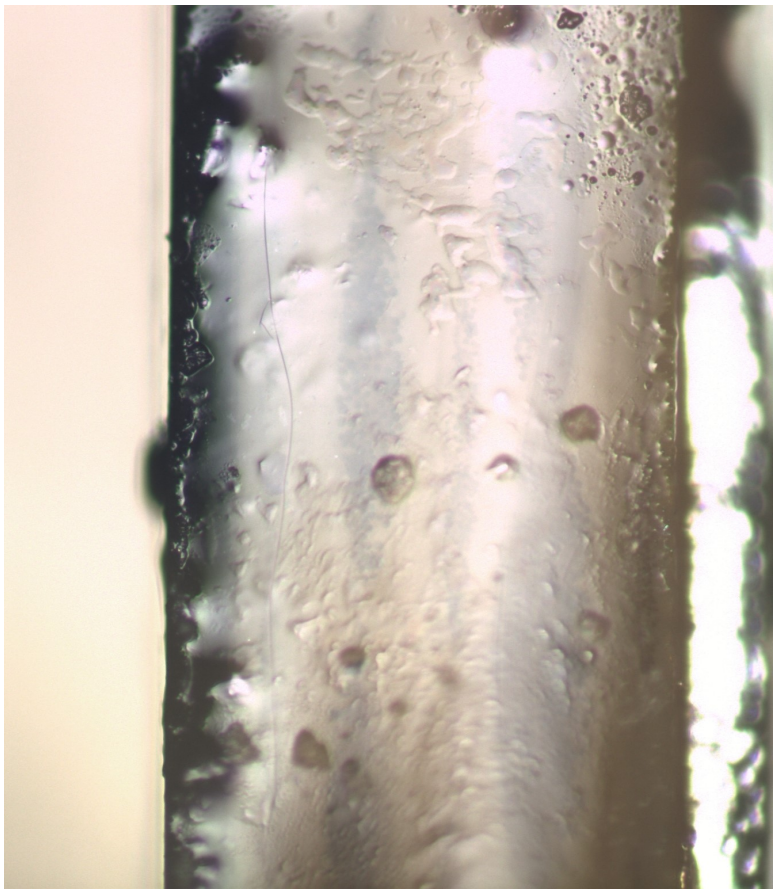


Figure 6.13: **Experimental results**: The solder degradation is not observed on the source and drain of GaN power devices in the healthy device of the buck converter.

CHAPTER 7: SMART CURRENT MONITORING IN GaN POWER DEVICES-SENSEGaN

7.1 Introduction

To enhance the performance of switching converters along with improving their efficiency in power electronics applications, a need for higher switching frequency is inevitable. Thanks to the development of WBG semiconductors like SiC and GaN, by knowing hardware difficulties for implementation of high switching frequency/high-current converters to overcome layout issues, electromagnetic interfaces, thermal dissipation management, and passive component challenges, finding alternative solutions for current information is important [63, 64]. Accurate current sensing methods are among the major steps toward the WBG power converters, bringing multiple opportunities such as effective protection, control, loss calculation, and prognostics techniques [65]. Traditional resistive based methods such as Shunt resistor and $R_{ds(on)}$ (drain-source resistance during ON time) monitoring, due to their high losses, and temperature variation dependency, have some fundamental challenges, especially in high-frequency converters [66].

In modern research of current measuring using advanced methods, (Hall Effect, Induction-based transducers, Rogowski coil, and Magnetoresistance (MR) sensors are now more focused on the investigation of alternative isolated approaches [67]. Although significant progress has been made in recent years in the development of these sensors, they are limited to the effective bandwidth of less than 1MHz. High current MR-based sensors have superior performance at the higher frequencies, but due to their relatively high costs, they have not been fully developed in most of the commercial products [68]. Therefore, with significant efforts in pushing the frequency

and power in WBG semiconductors (especially GaN), novel sampling techniques can still provide useful current information. The target is to develope a discrete design of current mirroring method to monitor the current of an active switch in boost converter at 150kHz with GaN.

The current mirroring technique can be used for monitoring power device currents practically in a loss-less manner compared to the Shunt resistor method. In power electronics, the current mirroring is commercialized and often known as the SenseFET approach [69, 70, 71, 72]. In this approach, two Silicon-Metal Oxide Semiconductor Field Effect Transistors (Si-MOSFET) with different resistances are connected in parallel. The one with higher resistance carries much smaller current, yet can represent the current in the main branch [73, 74, 75, 76]. Recently, this approach has been demonstrated for SiC and GaN devices integrated with Si MOSFET [77, 78]. However, this technique is typically non-isolated and hence, applicable for grounded devices where the common mode voltage is higher than 30V.

7.2 Current mirroring in GaN-SenseGaN

Current sensing with SenseGaN originally comes from current mirroring in integrated MOSFET at electronic circuits. In most of the transistor fabrication both in Field Effective Transistors (FET) and High Electron Mobility Transistors (HEMT), either in lateral or vertical, thousands of individual cells are interconnected in parallel configurations[79, 16, 31, 80]. Since these cell arrays are all identical, by isolating the source connection of one or several cells, a new pin can be considered for sensing purpose. The new configuration can monitor the active switch current proportionally.

As the Power and Sense transistors have the common drains and gates, by neglecting the small fraction of a voltage drop across the Sensing resistor, the gate-source signal can be assumed the same for both modules. Furthermore, the amplifier circuits force the same drain-source voltage drop across the Power transistor. Therefore, it is expected that the voltage drop across the sensing resistor proportionally shows the

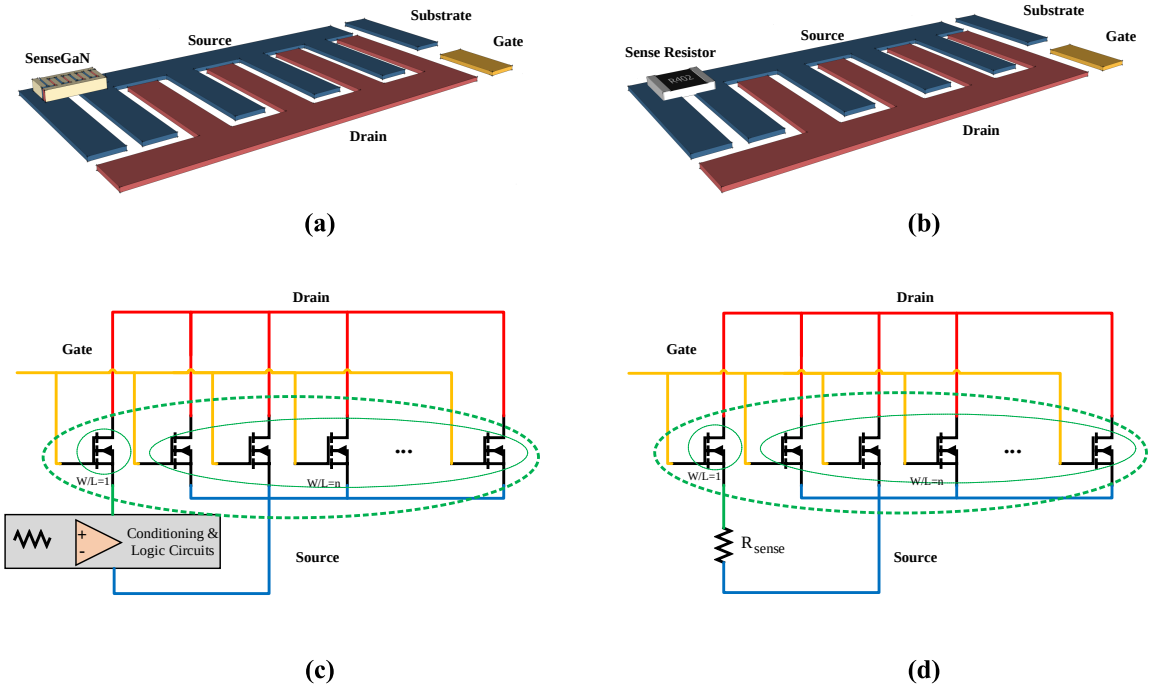


Figure 7.1: **SenseGaN configuration**: Proposing a scheme of SenseGaN for lateral dies based on available commercial products. (a): shows the geometry of SenseGaN die with virtual grounding to compensate thermal coupling and impedance matching. (b): represents the geometry of SenseGaN dies with Sense resistor without virtual ground compensation. (c): shows the equivalent electrical circuit model of SenseGaN with virtual grounding. This section will include all the logic circuits in a die interconnected into the power transistor. (d): shows the equivalent electrical circuit model of Sense resistor for a single switch.

drain-source current of the main Power device. This configuration also provides an opportunity to change the width-length ratio (W/L) of the channel in FETs, which directly reflects on the transistor turn-on resistance. The scaled-down version of the main current stream of the drain can pass through the transistor with smaller W/L ratio and would dramatically improve the loss compared to other resistive techniques like the Shunt resistor measurement [81]. In the integrated switch, the combination of parallel cells can be arranged by Power and Sense modules as shown in Fig. 7.1.

Theoretically, this technique does not suffer from bandwidth limitations and can be perceived as very high accurate measurement method; however, in practice, the voltage sampling and current measurement accuracy might be varied due to the tem-

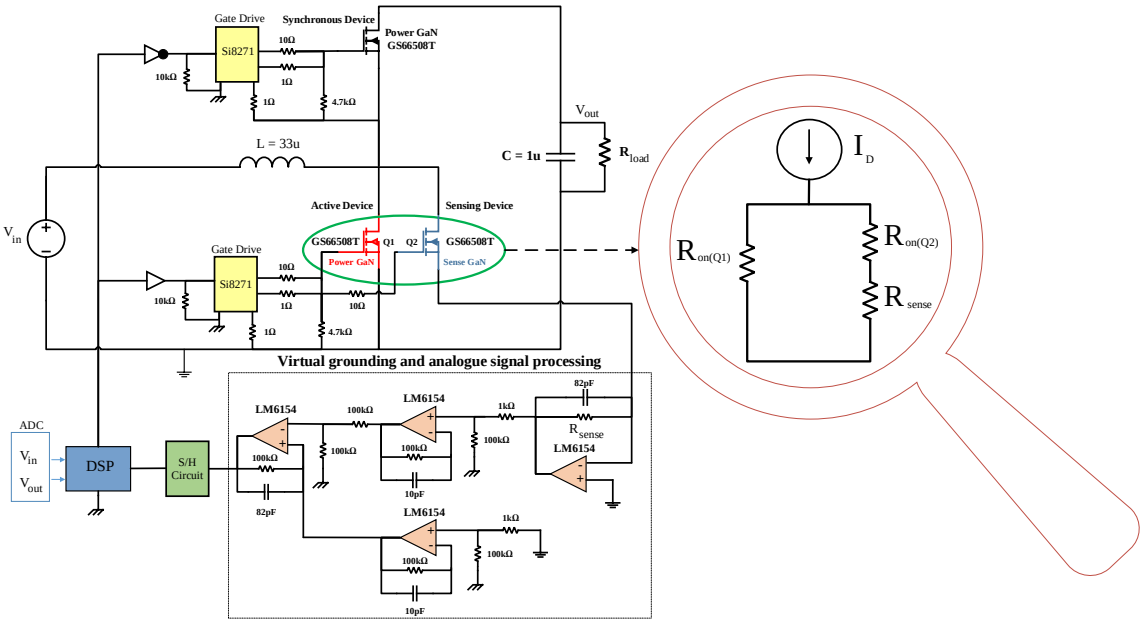


Figure 7.2: **Schematic capture**: Schematic of implemented virtual grounding for SenseGaN technique in a GaN boost converter. The virtual grounding circuit guarantee the tight connection of GaN power (Q1) and Sensing GaN (Q2) and consequently more accurate monitoring of the main current. The zoomed-in of the circuit shows the main current stream for temperature variation characterization.

perature dependency of $R_{ds(on)}$, sensing resistor, and gate-source mismatching. Moreover, in GaN transistors, $R_{ds(on)}$ increases at higher voltage like MOSFETs, which also needs to be considered. To mitigate the effect of temperature dependency and current ratio mismatching of SenseGaN, it is required to optimize sensing resistor. Therefore, based on the proposed technology for compensation of impedance matching, and virtual grounding for both transistors (Power and SenseGaN), additional circuits should be carefully designed shown in Fig. 7.2.

7.3 SenseGaN characterization

To analyze the temperature dependency and selecting proper Sense resistance for the proposed method, thermal coupling between Power and Sensing modules should be considered carefully. Since both devices are coming with the same fabrication technology, the thermal coupling between the transistors will be assumed the simi-

larly [82]. Therefore, drain-source resistance of the GaN device running at various temperature can be varied and simplified as (7.4):

$$R_{DS(on)} = R_{DS_{(ON)}}^{25^\circ C} e^{(T-25^\circ C)/k} \tag{7.1}$$

In which, T represents the device temperature in Celsius, and k is the thermal coefficient of the transistor. Equation (7.4) shows drain-source resistance while the switch is running, and the equivalent electrical circuit of SenseGaN topology can be modeled as Fig. 7.2(b). Assuming ideal current sharing in both Power and Sense Modules, the current ratio based on the voltage drop across the sensing resistor can be simplified as (7.5):

$$\frac{I_{Q1}}{I_{Q2}} = \frac{R_{DS(on)Q2} + R_{sense}}{R_{DS(on)Q1}} = \frac{R_{DS_{(ON)Q2}}^{25^\circ C} e^{(T-25^\circ C)/k_{Q2}}}{R_{DS_{(ON)Q1}}^{25^\circ C} e^{(T-25^\circ C)/k_{Q1}}} + \frac{R_{sense}}{R_{DS_{(ON)Q1}}^{25^\circ C} e^{(T-25^\circ C)/k_{Q1}}} \tag{7.2}$$

where R_{sense} is the sensing resistor, $R_{ds(on)Q1}$ and $R_{ds(on)Q2}$ show the drain-source resistance of Power and SenseGaN, respectively. To mitigate the temperature dependency of the current ratio in the switches, multiple parameters can be adjusted. The simplified equation is in (7.6):

$$\frac{I_{Q1}}{I_{Q2}} = \frac{R_{DS_{(ON)Q2}}^{25^\circ C}}{R_{DS_{(ON)Q1}}^{25^\circ C}} + \frac{R_{sense}}{R_{DS_{(ON)Q1}}^{25^\circ C} e^{(T-25^\circ C)/k_{Q1}}} \tag{7.3}$$

In (7.6), similar device fabrication technology provides a close thermal coupling which enforces the first term as a constant parameter, and the temperature dependency of the second term can be optimized by minimizing R_{sense}. Therefore, choosing low values for sensing resistor will help to reduce temperature dependency effects and increase the enhanced performance at a higher switching frequency.

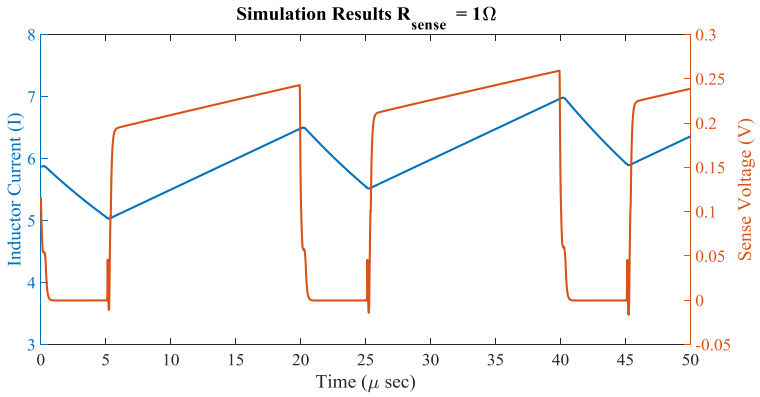
7.4 Converter design-simulation analysis

As a proof of concept for implementation of SenseGaN, a boost converter was initially modeled accurately in the Spice using manufacturer model (GS66508T). At the power stage level of this design, the isolated gate drivers are considered to run both Power and SenseGaN. As all the devices are selected similarly, they all have adequate breakdown voltage across the drain-source. Since the input capacitance of the both devices is the same, a bigger resistor also added on gate path of SenseGaN to bring a small delay and avoiding high voltage transient. This modification is essential to make sure GaN power (Q1), fully operates in a saturated mode and can be reflected in sensing transistor (Q2).

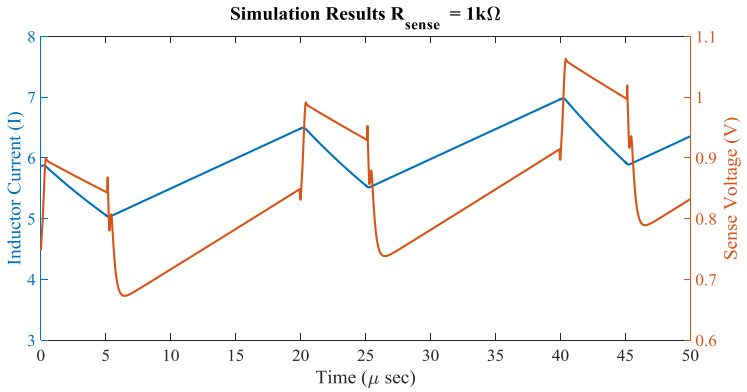
7.5 Converter design-simulation analysis

There are three different methods to provide proper isolation to avoid the voltage common mode issue: a) optical, b) capacitive, and c) electromagnetic isolations. The first method relies on the light intensity proportional to the measured signal coming through the photoconductive element (typically a diode). However, this technique requires at least 0.7V to guarantee the diode is ON. The second method is a proper solution for many systems, but the capacitance characteristics make a longer delay on especially during fast transients. In the electromagnetic method, a pair of conductive coils provides a physical barrier between circuits. The proposed method is the combination of the second and third approaches, where the two small air-core inductors as well as the capacitor resonance circuits, and virtual grounding.

As shown in (7.6), to reduce the effect of temperature dependency, the sensing resistor should be selected as small as possible; however, choosing small resistor has a drawback, which enforces the higher drain current pass through SenseGaN (Q2) and consequently increases the loss. On the other hand, Fig. 7.3 shows higher resistance holds the voltage across the sensing transistor while it is off and thus creating some



(a)



(b)

Figure 7.3: **Spice simulation results**: SenseGaN in two different scenarios. blue: inductor current, orange: measurement with SenseGaN circuit a) sensing resistor is 1Ω, b) sensing resistor is 1kΩ. As it shown choosing higher resistance would impact the sensing significantly. For these devices, it is recommended to use sensing resistor <20Ω to compromise between higher efficiency and system robustness performance.

issues. For instance, while the sensing resistor is very large (assuming open circuit), no current will circulate from the sensing path, and the sensing transistor shows the scaled down of the drain-source voltage across the switch. This can also be observed in Fig. 7.3 for two different scenarios. In the hardware setup, it is recommended to use a resistor less than 20Ω to make sure the system operation at higher switching frequency is still robust. The resistor itself could be more robust to decouple the variations, which also can be used for $R_{ds(on)}$ capturing.

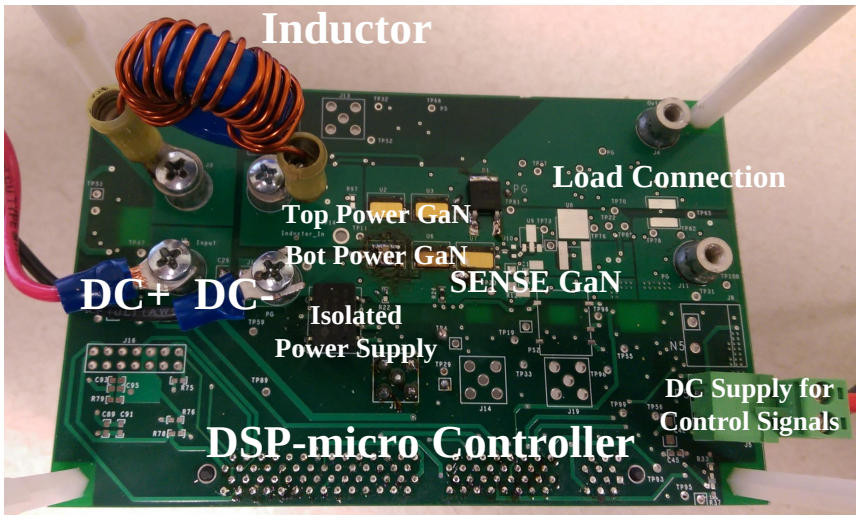
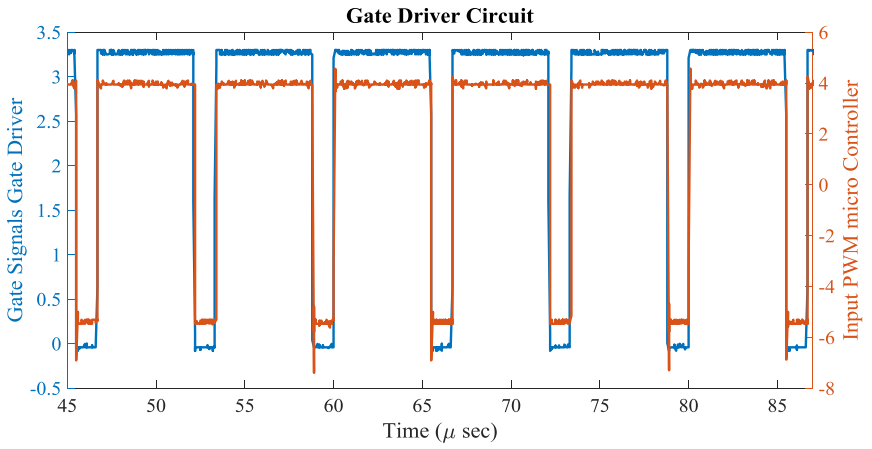


Figure 7.4: **Hardware setup**: The prototype was designed in four layers: Top layer: Power stage, Inner layer-1: Power ground, Inner layer-2: Shield layer, Bottom layer: Control signals and conditioning circuits.

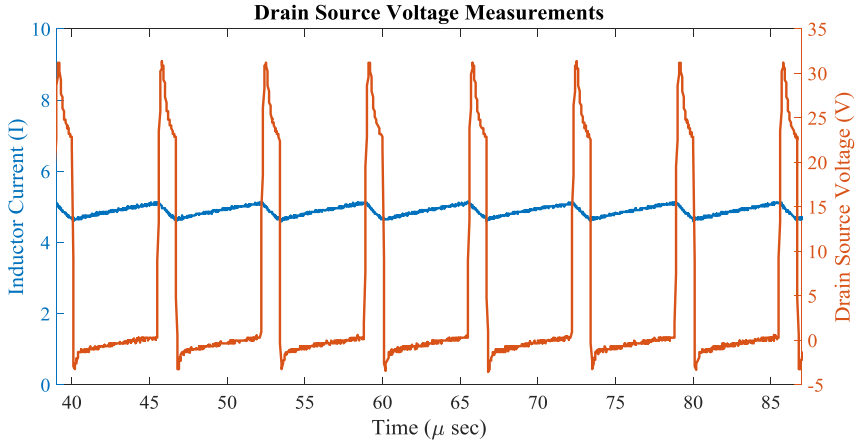
7.6 Converter design-hardware prototype and experimental results

To verify the analysis and simulation results, a prototype board was built with four layers as it shown in Fig. 7.4. The converter was tested under different loads as well as switching frequencies (up to 150kHz). The input signals for the gate driver generated from the microcontroller. The +9V isolated power supplies for the gate drivers were clamped with a Zener diode at +3.9V to make sure the devices are fully ON in the saturated region, but still lower than the absolute borderline for gate signals (+7V) recommended by the manufacturer.

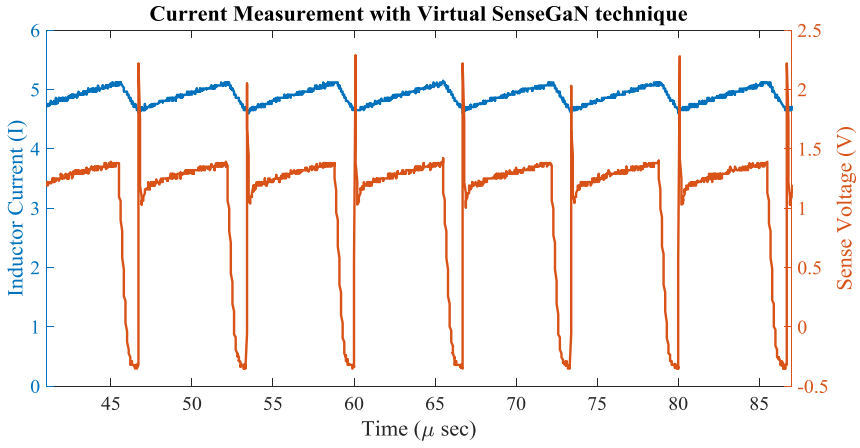
Furthermore, very fast precision rail-rail Op-Amp (LM6154) was also used to generate virtual grounding. Since spikes can also be observed during turn on of the sensing device, selecting a capacitor in the range of ($<1nF$) in parallel with sensing resistor, and having multiple filter stages is recommended to reduce the effect of common noise. Finally, the prototype converter was tested successfully, and the results are provided in Fig. 7.5. Although in the figure some, spikes are observed during turn-on time, they are not harmful and can be ignored with blind analogue circuits.



(a)



(b)



(c)

Figure 7.5: **Experimental results**: a) blue: input gate signal from micro controller, and orange: output gate signals of the isolated gate driver. b) blue: inductor current measured with amplifier current gun, orange: drain-source voltage of the converter c) blue: inductor current measured with amplifier current gun, orange: current measurement with SenseGaN 150kHz, 5A boost power converter.

7.7 SenseGaN in the BCM control of a DC-DC boost converter

In (quasi) soft-switching circuits, most attentions have been paid to zero-voltage switching due to the ease of voltage measurement and availability of passive components [83]. In power MOSFETs, turn-on losses are more dominant than turn-off losses [84]. Therefore, Boundary Conduction Mode (BCM) operation is desirable in many power electronics converters [85]. To operate the converter at BCM, it is required to have a proper control scheme to change the switching frequency as well as an accurate method to detect the zero current.

Different Zero Current Detection (ZCD) methods and associated control schemes for BCM operation have been proposed in recent literature. The current monitoring with isolated secondary winding of an inductor for unidirectional application is used in [86], dynamic current mirroring by memorization capability of charging capacitor is presented in [87], reverse current detection of inductor current by freewheeling switch is implemented in [88], and online digital predictive BCM using equivalent series resistance of an inductor is provided in [89]. In a cost conscious yet efficient converters with voltage mode or duty cycle control, series-connected RC filters are used to detect the zero-current crossing point in [90], [91]. For bidirectional converters, using a secondary winding only for zero current crossing detection has been proposed in [92]. Cost, bandwidth, and sensitivity at low currents are the reasons that isolated current sensors such as Hall-effect current sensors may not be the solution for many and emerging high-frequency power converters.

The current mirroring technique can be used for monitoring the power device current practically in a loss-less manner compared to shunt resistor method. In power electronics, current mirroring is commercialized and often known as SenseFET approach. In this approach, two Si MOSFETs with different resistances are connected in parallel. The one with higher resistance carries much smaller current, yet can represent the current in the main branch with proportion. Recently, this approach

has been demonstrated for SiC and GaN devices integrated with Si MOSFET in [77], [78]. This approach can be cost effective if all integrated into the device die [72], [71]. However, the SenseFET is typically non-isolated and hence, applicable for grounded devices where the common mode voltage is higher than 30V. For instance, the SenseFET in synchronous boost converters as power factor correction circuit can be used in the active switch for controlling the converter in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM).

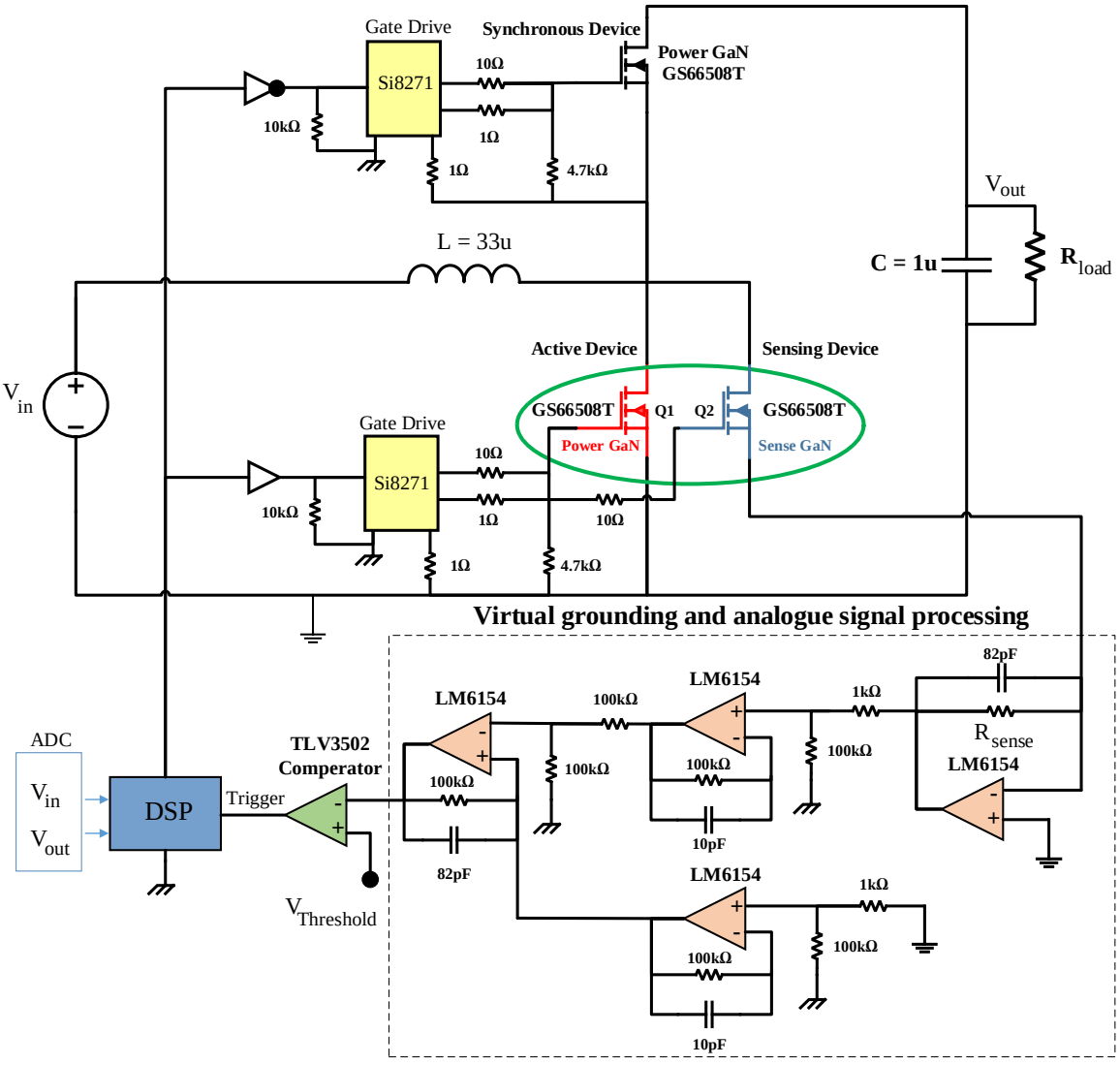


Figure 7.6: **Schematic capture**: The boost operation system with SenseGaN and control units.

In this section, a control scheme is proposed for a synchronous boost converter to operate in BCM. The active switch current is only sensed using the current mirroring technique. The challenge is the zero current for BCM operation obtained at the synchronous mode is not available for direct measurement. The converter operation mode cursor, i.e. CCM/BCM is identified through an adaptive comparison. The cursor is used in an iterative control scheme to bring the converter to BCM. The concept will be demonstrated on a boost converter using 650V GaN devices. The current mirroring circuit has been implemented with the same GaN device for the active switch, which we call SenseGaN. The circuit details and experimental verification will be presented.

7.8 Proposed boundary conduction mode control In a boost converter

7.8.1 Active switch current measurement with SenseGaN

In this method, a parallel sensing GaN is used for the current mirroring of the active power module. The schematic of the sensing technique for a boost converter is shown in Fig. 7.6. Having the same gate signal source, and considering a virtual grounding to force the same drain-source voltage for both devices, then the voltage drop across the sensing resistor proportionally reflects the active transistor current. Therefore, a sensing GaN (Q2) can effectively monitor the current of GaN power (Q1). Ideally, this technique is not limited by bandwidth, and can be perceived at the very high accurate measurement with significant low power loss. The compromise to choose the proper sensing resistor should be considered for the robustness of the system at higher switching frequency (smaller resistance) and lower loss (bigger resistance).

7.8.2 The proposed algorithm for BCM control

In the boost converter, since the SenseGaN can only be placed on the bottom side to avoid common mode voltage issues, it can only measure the current during ON time. Assuming to run the converter with the same average current marked in Fig.

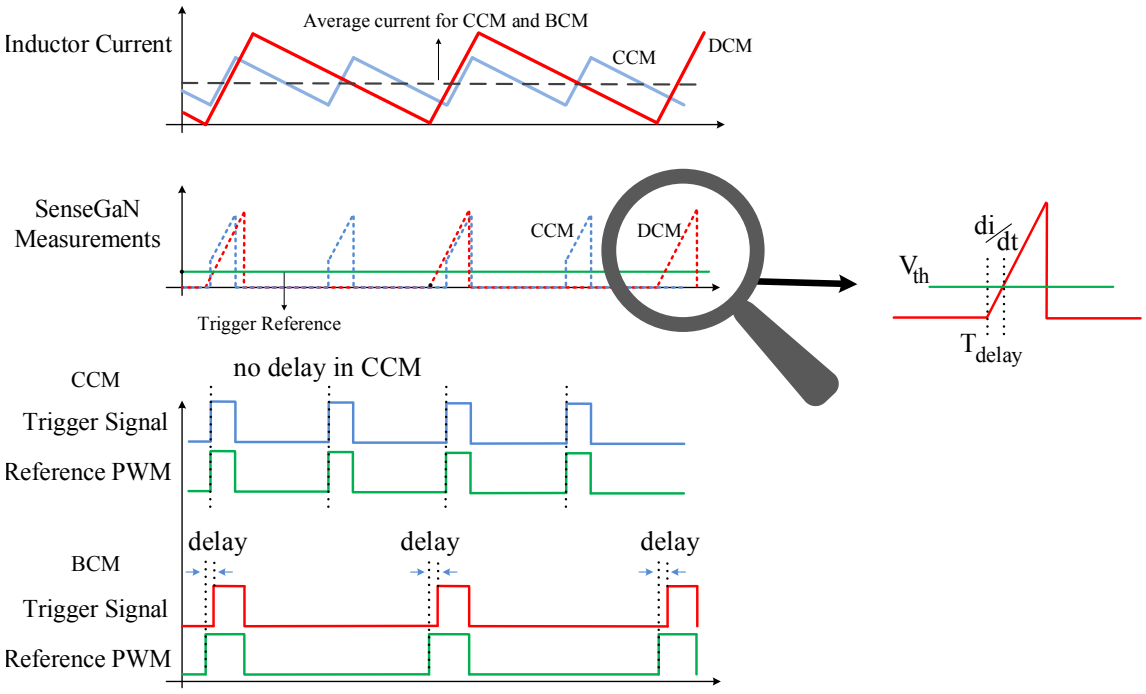


Figure 7.7: **The system operation mode and curser identifications**: a) The inductor current at CCM (blue) and BCM (red) with the same average current. b) The current monitoring with the SenseGaN for the active device in CCM and BCM. (here, the zoomed-in version of threshold trigger reference signal for delay generation is exposed) c) The microcontroller compares the trigger reference signal generated by the comparator and PWM signals to generate the delay signal in CCM and BCM.

7.7(a), the measurement at CCM is more like perpendicular trapezoid; however, in BCM the sensing element is characterized as a triangle shown in Fig. 7.7(b). This signature is used as an identifier to distinguish CCM and BCM. By monitoring of the input voltage and knowing the inductance value, the slope of inductor current can be calculated in each cycle. Since the slope for both CCM and BCM are the same, an analogue delay trigger signal generated through a fast comparator is considered as a parametric identification value.

Due to the small input threshold voltage of the comparator, the SenseGaN device does not capture the diagonal linear region at CCM condition. Therefore, the generated trigger signal respect to the reference PWM has a zero delay; however, in BCM, the trigger signal compared to the reference PWM signal has a constant non-zero

value. This delay can be calculated as: ($T_{delay} = L\frac{V_{th}}{V_{in}}$) where T_{delay} is the generated delay, V_{th} is the predefined input threshold voltage of the comparator, and V_{in}/L is the slope of the inductor current when the device is ON. The delay signal will be calculated in each cycle. Then based on the captured delay, the control action can be updated sequentially to find the BCM of the converter.

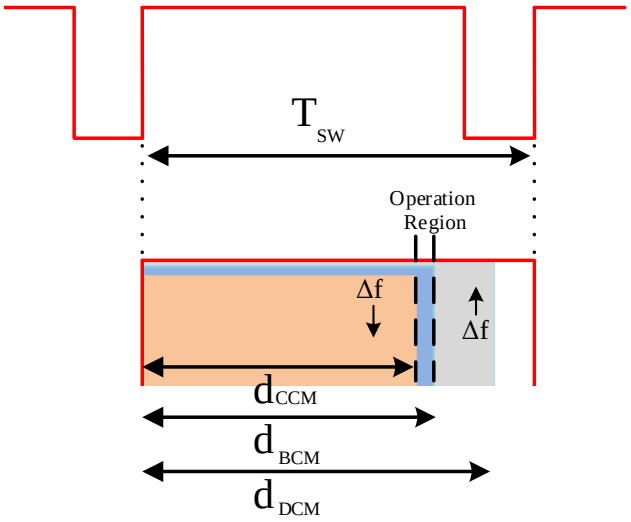


Figure 7.8: **The system operation modes**: The operational regions for distinguishing CCM, BCM, and DCM in a single cycle. Orange: CCM, Blue: Optimum region for BCM, Gray: DCM.

The first part of the algorithm is to distinguish the CCM and BCM conditions. Here, once the load condition changes (for instance, higher current), the microcontroller captures a zero delay, thus the converter operation is considered as CCM. Now based on the algorithm, the microcontroller gradually reduces the switching frequency to adaptively find the new BCM. This process will be continued till the generated non-zero delay matches with the calculated delay. Fig. 7.7(c) shows the delay comparisons of the algorithm in CCM and BCM.

The second part of the algorithm needs to be run to make sure the converter does not operate in DCM. This is very crucial because the generated delay signals in BCM and DCM have the same value. Here, by decreasing the switching frequency in small intervals from the BCM switching frequency the controller can still observe the

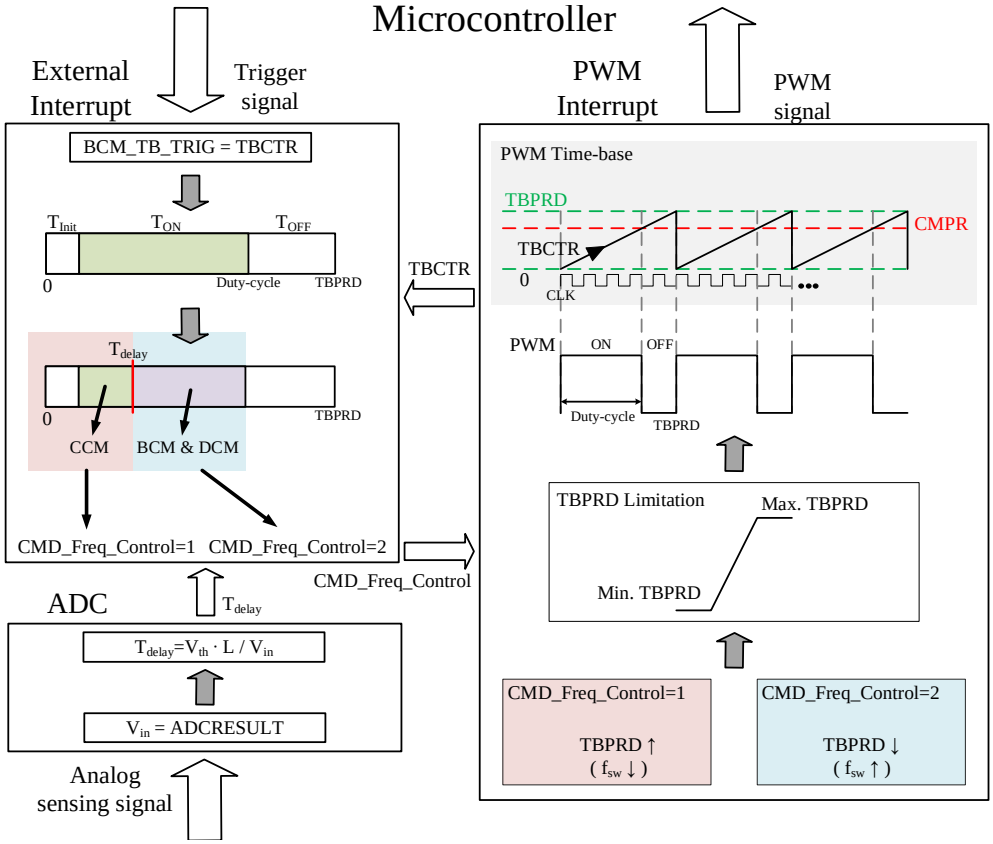


Figure 7.9: **SenseGaN control**: The scheme flow chart for the proposed BCM control algorithm.

same delay signal, and the converter operation is perceived at DCM; On the other way, assuming to run the converter with calculated delay, by minor increasing the switching frequency once the BCM delay is detected, the converter operation will be entered to CCM. Therefore, the converter always operates in a narrow region as highlighted blue in Fig. 7.8.

Visualization of the details of the implemented BCM control of the boost converter in the microcontroller is shown in Fig. 7.9. The algorithm consists of interconnection of multiple functions as External Interrupt (XINT), Analogue to Digital Converter (ADC), and PWM Interrupt. For the microcontroller, two main inputs are required to create a criterion representing BCM conditions, and detection of the current state of the boost converter. The first one is the input voltage, and the other is the trigger signal. The analogue input voltage signal is applied to ADC for the delay time

calculation, and the trigger signal enters to XINT for initiation of interrupt service routine.

Once the rising-edge of the trigger signal is received, the microcontroller executes the XINT. Therefore, it calculates the elapsed time of the trigger signal with Time-based Counter Register (TBCTR). The TBCTR is a counter register to generate PWM signal in microcontroller. As shown in Fig. 7.9, initially since TBCTR is zero, the PWM signal will be active high. When the TBCTR reaches to the Counter Compare Register (CMPR), the high PWM signal is forced to low, and once TBCTR reaches the Time Based Period Register (TBPRD), the TBCTR will be reset to zero. Since the TBCTR is synchronized with the PWM signal, the elapsed time of the trigger signal is calculated in each PWM cycle. Both CMPR and TBPRD are determined according to the operation condition of the boost converter.

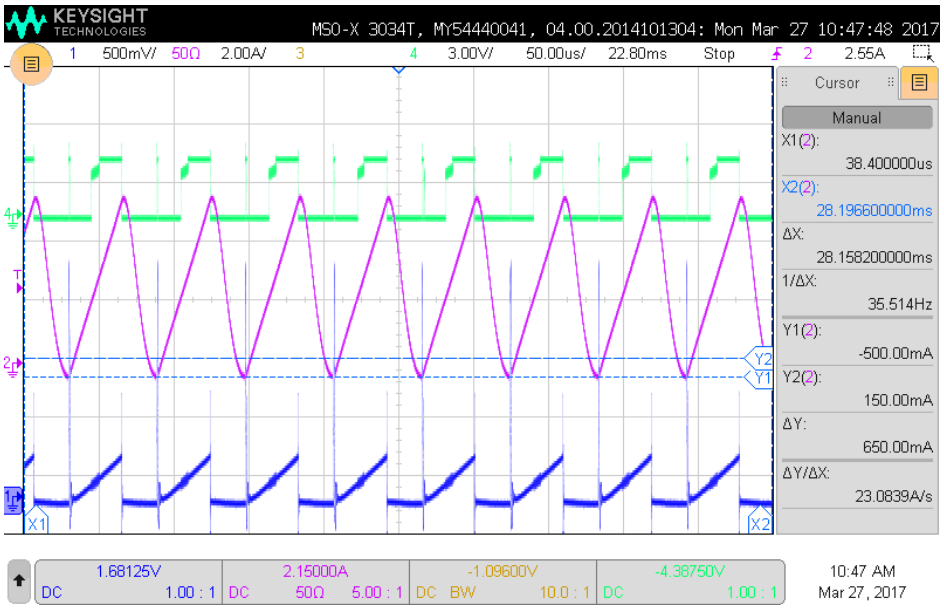


Figure 7.10: **Experimental results**: SenseGaN operation at 2.5A with 350mV/A sensitivity. Purple: inductor current measurement (amplifier current gun), Blue: SenseGaN measurement, Green: generated trigger signal from the analogue comparator (TLV3502).

Based on the calculation of the elapsed time, the status of the boost converter

operation mode can be determined. If the trigger time is shorter than the delay time, it means that the boost converter is in CCM. If the trigger time is longer than the delay time, it means that the boost converter is in BCM/DCM. Since the slope of the inductor current will remain constant even at different operation conditions, the inductor current at CCM hits the threshold level faster than BCM/DCM.

Once the comparison is over, regulation of the PWM switching frequency is executed to keep the operation mode in BCM. If the operation mode is CCM, the TBPRD is increased to reduce the switching frequency. If the operation mode is the BCM/DCM, the TBPRD is decreased to raise the switching frequency. By updating the TBPRD, the operation mode is regulated. Since the trigger signal for both BCM/DCM is the same, repetitive increase of the switching frequency is required to guarantee the narrow region represented in Fig. 7.8.

7.9 Experimental verification

To verify the effectiveness of the proposed method, a prototype was built in four-layer board. On the top layers, all the power components including the GaN devices and inductors are placed. Additional shield is implemented in the inner layer to reduce the effect of switching noises on the measurements circuits. On the bottom layer, conditioning and controlling circuits including the microcontroller (TMS320F28335), ultrafast Op-Amps and comparators are placed. In this setup, 650V/30A GaN devices (GS66508T, $R_{ds(on)} = 50\text{m}\Omega$) and the isolated gate drivers (Si8271-GB-IS) were used. Furthermore, multiple design criteria were considered such as bigger resistor on the gate path of the SenseGaN (Q2). This is essential to have sufficient delays for proper current mirroring from the main GaN power (Q1) and avoid voltage transients. Since the input capacitance of the both Power and sensing devices are the same, a bigger precision resistor is also added to the gate path of the SenseGaN to bring a proper delay and avoiding high voltage transient. Ultrafast precision rail-rail Op-Amp (LM6154) with high common mode rejection noise was used to provide virtual and

firm ground. The sensing resistor is chosen as 20Ω precision resistor with ultra-low tolerance ($< 0.1\%$). Multiple filter stages (f_c <1MHz) are also added to reduce the noise and achieve required signal scaling as shown in the schematic capture, Fig. 7.6. The converter was tested under different load conditions and switching frequencies to verify its sensitivity, linearity and system robust operation. An example of the circuit operation with active switch current measurement using SenseGaN is represented in Fig. 7.10.

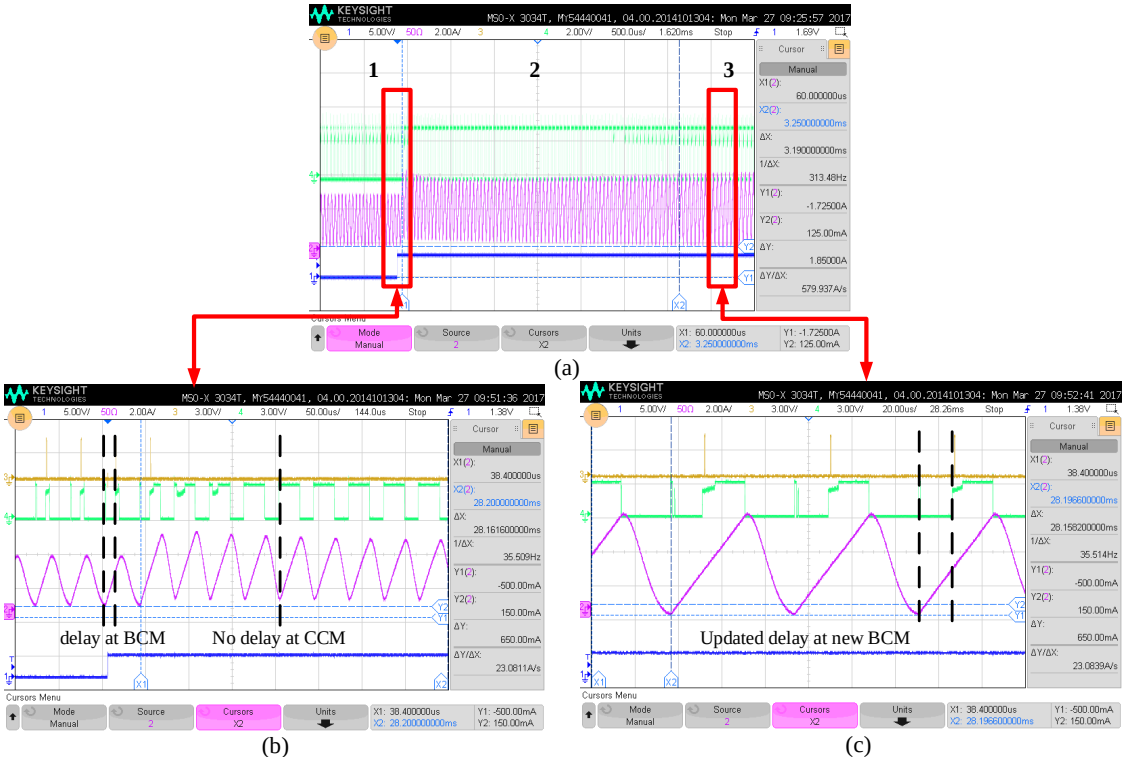


Figure 7.11: **Experimental results**: Implementation of BCM in a boost converter with SenseGaN. Purple: inductor current measured with an amplifier current gun, Green: generated trigger signal with the fast comparator Blue: trigger signal for load change. a) Converter operation at different CCM and BCM regions. b) Initial BCM condition (duty cycle: 40%), and transient to CCM (60%) c) New BCM steady-state condition for higher current after implementing the iterative control scheme. Delay detection between trigger signal and PWMs are highlighted in BCM and CCM operation.

Initially, the converter operates at 40% duty cycle with 24kHz under a resistive load of 8Ω. As shown in Fig. 7.11(a), the converter operates in BCM and the delay

is detected by the trigger signal. By increasing the duty cycle to 60%, the converter enters CCM and the trigger rising-edge becomes equal to the active switch on-time. In other words, there is no delay. This has been highlighted in Fig. 7.11(b). As mentioned, the delay makes sure the converter is in BCM. Through the microcontroller, the switching frequency sweeps with 1kHz steps to reach the desirable delay, indicating the converter is practically in BCM. In this example, the BCM operation reaches at 17kHz and has been highlighted in Fig. 7.11(c).

7.10 Isolated current mirroring in GaN-Iso-SenseGaN

With significant efforts in increasing the frequency and power in WBG semiconductors (especially GaN), novel sampling techniques are required to provide useful current information for the advanced control strategy [93]. SenseGaN is a powerful technique for active monitoring of the device, which is a proper way for the full integration into the power module. This method initially was introduced in [60], for current monitoring of an active switch in the boost converter. However, using this method for high voltage application where the common mode voltage is higher than ($> 30V$), there are some limitations on the filtering stages (OpAmp voltage).

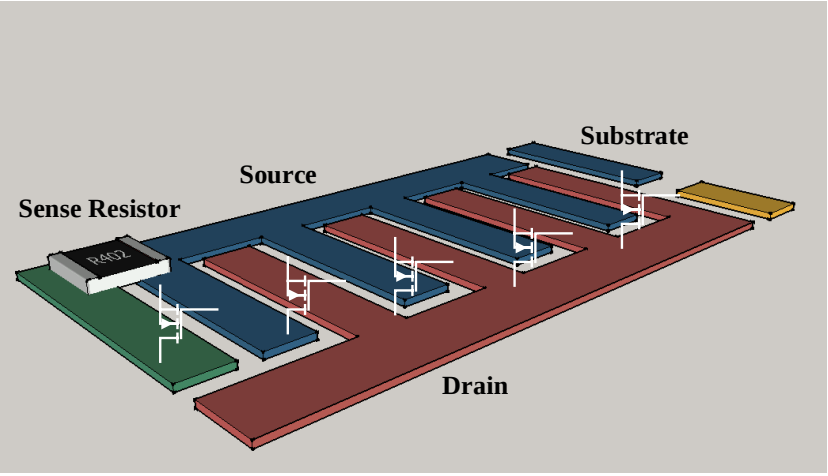


Figure 7.12: **Iso-SenseGaN configuration**: Proposing a scheme of Iso-SenseGaN for lateral dies based on available commercial products.

The target of this section is developing a discrete design of current mirroring method with the galvanic isolation to run a DC-DC boost converter and a DC-AC converter in Boundary Conduction Mode (BCM). The active switch current is sensed using the current mirroring technique shown in Fig. 7.12. To the best of my knowledge, no prior work has been published to sense the active current of GaN power transistors with the galvanic isolation to avoid common mode issues. I called this technique as the Iso-SenseGaN that current monitoring can be effectively used in all common power electronics converters as shown in Fig. 7.13.

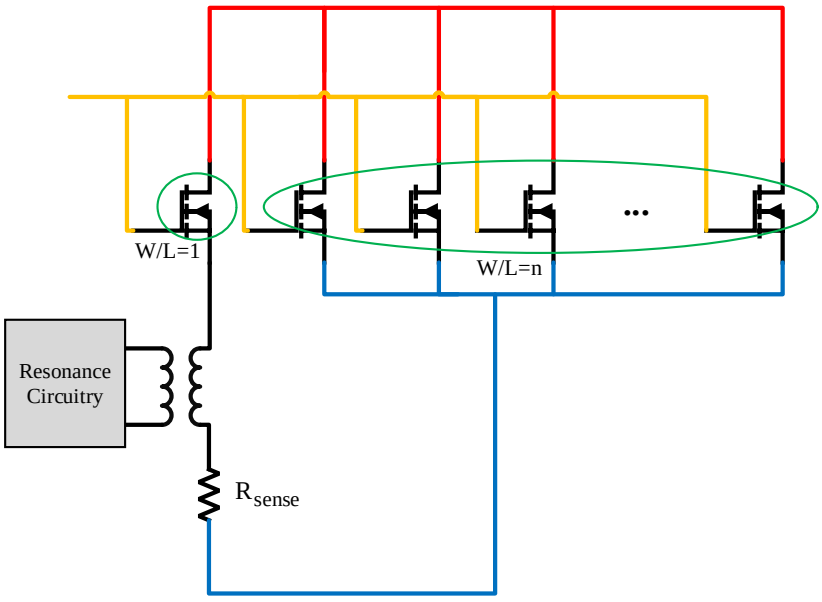


Figure 7.13: **Iso-SenseGaN**: The equivalent circuit model of the Iso-SenseGaN for the available lateral GaN.

There are three different methods to provide proper isolation to avoid the voltage common mode issue: a) optical, b) capacitive, and c) electromagnetic isolations. The first method relies on the light intensity proportional to the measured signal coming through the photoconductive element (typically a diode). However, this technique requires at least 0.7V to guarantee the diode is ON. The second method is a proper solution for many systems, but the capacitance characteristics make a longer delay on especially during fast transients. In the electromagnetic method, a pair of conduc-

tive coils provides a physical barrier between circuits. The proposed method is the combination of the second and third approaches as LLC, and virtual grounding are shown in Fig. 7.14.

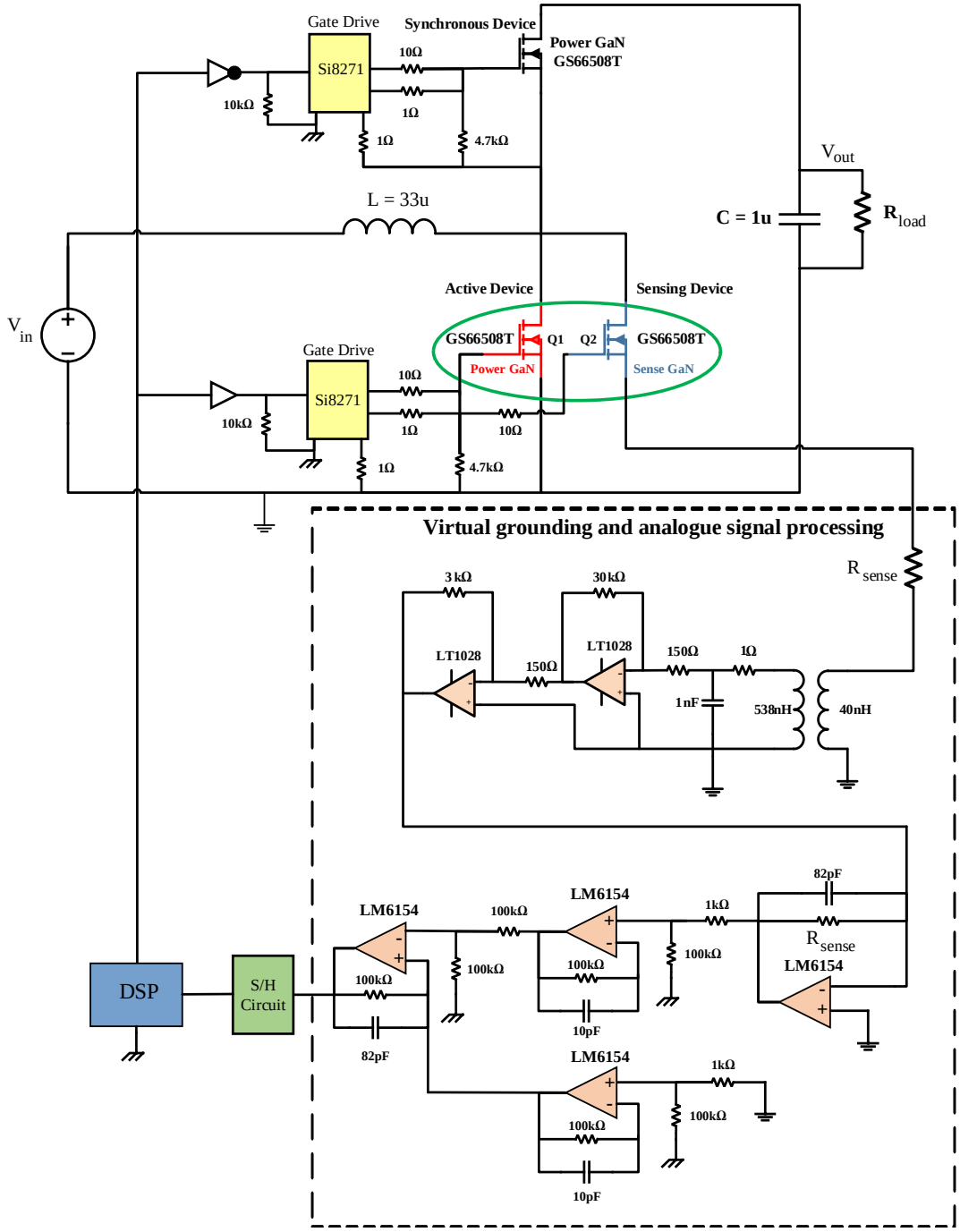


Figure 7.14: **Schematic capture**: a) Schematic of the virtual grounding for Iso-SenseGaN technique with galvanic isolation in a GaN boost converter.

7.11 Iso-SenseGaN characterization

To analyze the temperature dependency and select proper sense resistance, since both devices will be fabricated with the same technology, the thermal coupling between the transistors will be assumed similarly [82]. Thus, resistance variation of the GaN device at the different temperature is simplified as (7.4):

$$R_{DS(on)} = R^{25^\circ C}_{DS_{(ON)}} e^{(T-25^\circ C)/k} \tag{7.4}$$

where, T is the device temperature in Celsius and k is the thermal coefficient of the transistor. The simplified current ratio of the devices is shown in (7.5):

$$\frac{I_{Q1}}{I_{Q2}} = \frac{R^{25^\circ C}_{DS_{(ON)Q2}}}{R^{25^\circ C}_{DS_{(ON)Q1}}} + \frac{Z_{sense}}{R^{25^\circ C}_{DS_{(ON)Q1}} e^{(T-25^\circ C)/k_{Q1}}} \tag{7.5}$$

here, Z_{sense} is the total impedance of the Iso-SenseGaN path, and I_{Q1}, I_{Q2} show the current in the power and sense transistors, respectively. Based on (7.5), to reduce the effect of temperature dependency, the sensing resistor should be very small. However, the drawback is the higher drain current passes through Iso-SenseGaN (Q2), and consequently the high current increases the loss. Therefore, a simple Optimization Function (OF) for each specific design can be run to choose the proper resistance:

$$OF = k_1(P_{con} - \frac{{V_{sw}}^2}{Z_{sense}}) + k_2(1 + Z_{sense}) \tag{7.6}$$

where, P_{con} is the converter power, V_{sw} is the switching node voltage of the SenseGaN connection, k_1 and k_2 are the weighting factors for objective function, and constant ratio $R^{25^\circ C}_{DS_{(ON)Q2}}/R^{25^\circ C}_{DS_{(ON)Q1}}$ is considered as 1. The optimization results are provided in Fig. 7.15.

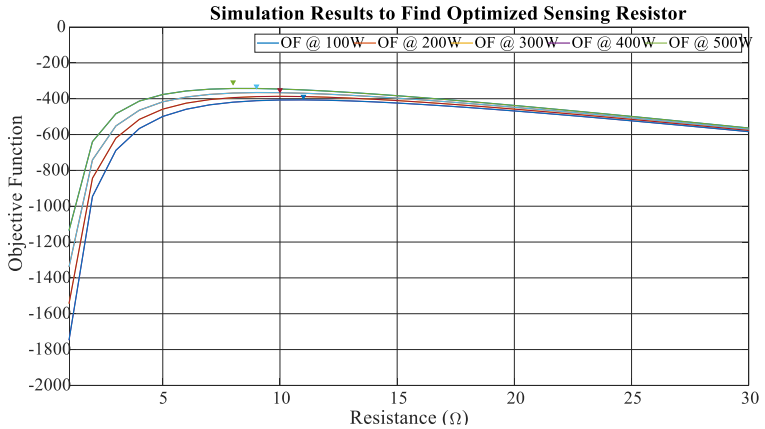


Figure 7.15: **Optimization in SenseGaN**: The compromise of higher performance (low resistance) vs. lower loss (high resistance) are analyzed in the OF.

7.12 Iso-SenseGaN in the BCM control of a DC-DC boost converter

To show the capability of the Iso-SenseGaN, the BCM control of common power electronics converters are proposed here. This method initially was introduced in [60], for current monitoring of an active switch in the boost converter. However, the constraints of solution time in microcontroller limit the bandwidth of this technique; Therefore, Iso-SenseGaN can be placed for each device (Q_1), and (Q_2) in the DC-DC boost converter as shown in Fig. 7.16.

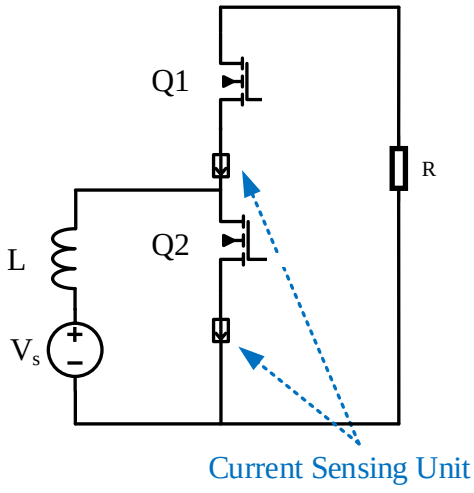


Figure 7.16: **BCM control of a DC-DC boost converter**: the system operation mode at the CCM (blue) and the BCM (red) with the same average current.

Once the converter operates at the BCM, the current waveform is characterized as triangle whereas, in the CCM, the current of SenseGaN is considered as trapezoid shown in Fig. 7.17. Having the information of the top and bottom devices, two fast analogue comparators are adjusted with two different thresholds that are placed for each device; the one for the top device indicates the zero current crossing, and for the bottom switch shows the maximum current. Once the trigger signal is received from the high threshold comparator, the bottom device will be turned OFF, and the low threshold comparator turns ON the bottom device, as verified in CHIL test as shown in Fig. 7.18 and Fig. 7.19 [94].

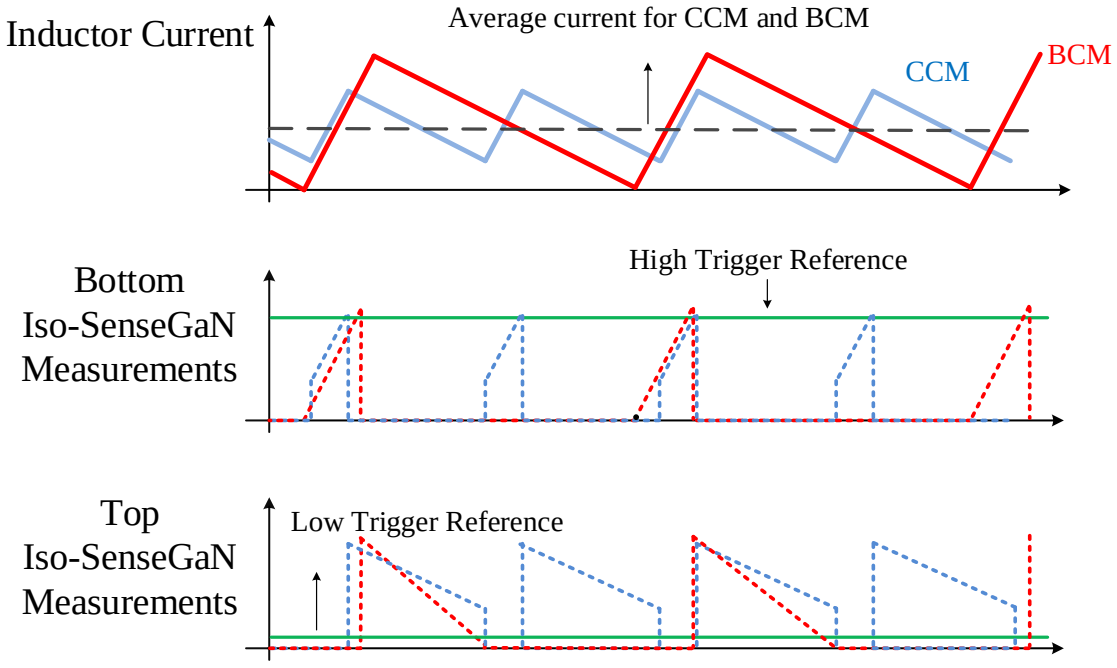


Figure 7.17: **BCM control of a DC-DC boost converter**: the current monitoring reflected in the Iso-SenseGaN. Two reference trigger signals are considered to turn-on the top and bottom devices consecutive.

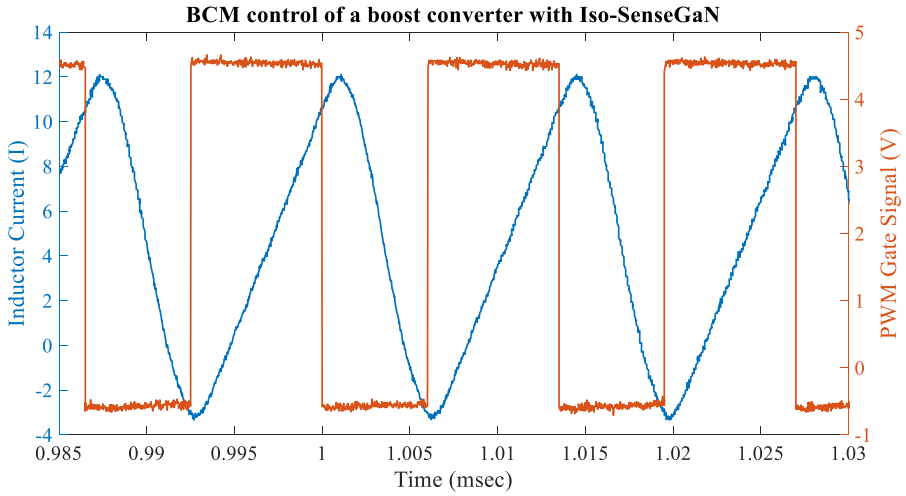


Figure 7.18: **BCM control of a DC-DC boost converter**: orange: PWM gate signals, blue: inductor current.

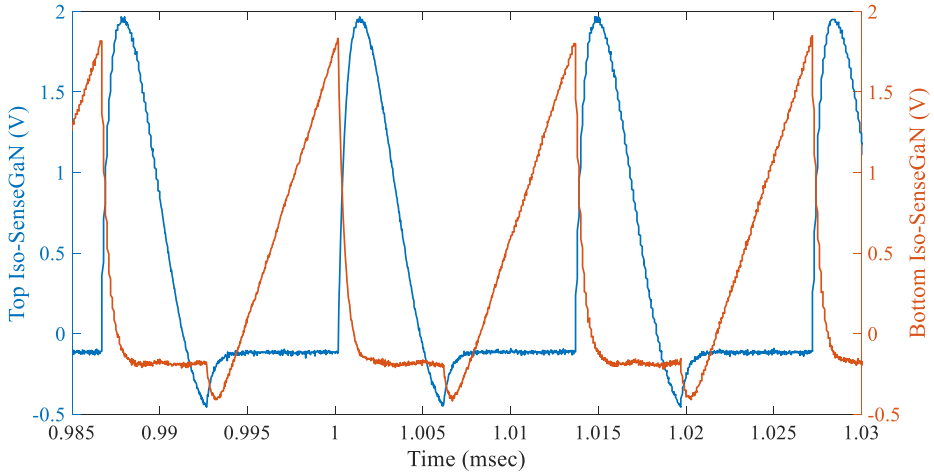


Figure 7.19: **BCM control of a DC-DC boost converter**: orange: bottom Iso-SenseGaN, blue: top Iso-SenseGaN outputs.

7.13 Iso-SenseGaN in the BCM control of a DC-AC converter

In this section, the potential of SenseGaN technique is used to control an inverter at the BCM. For each bottom devices, an individual Iso-SenseGaN/SenseGaN will be placed as shown in Fig. 7.20. Having the information on the bottom devices, two fast analogue comparators adjusted with two small thresholds voltages are considered for each of them, individually. The proposed sensor placement for BCM of the DC-AC converter is shown in Fig. 7.20.

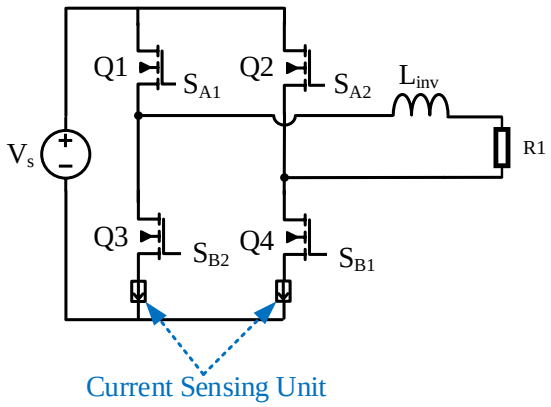


Figure 7.20: **(Iso)SenseGaN for the BCM control of a DC-AC converter**: The proposed architecture for the sensor placement in an inverter.

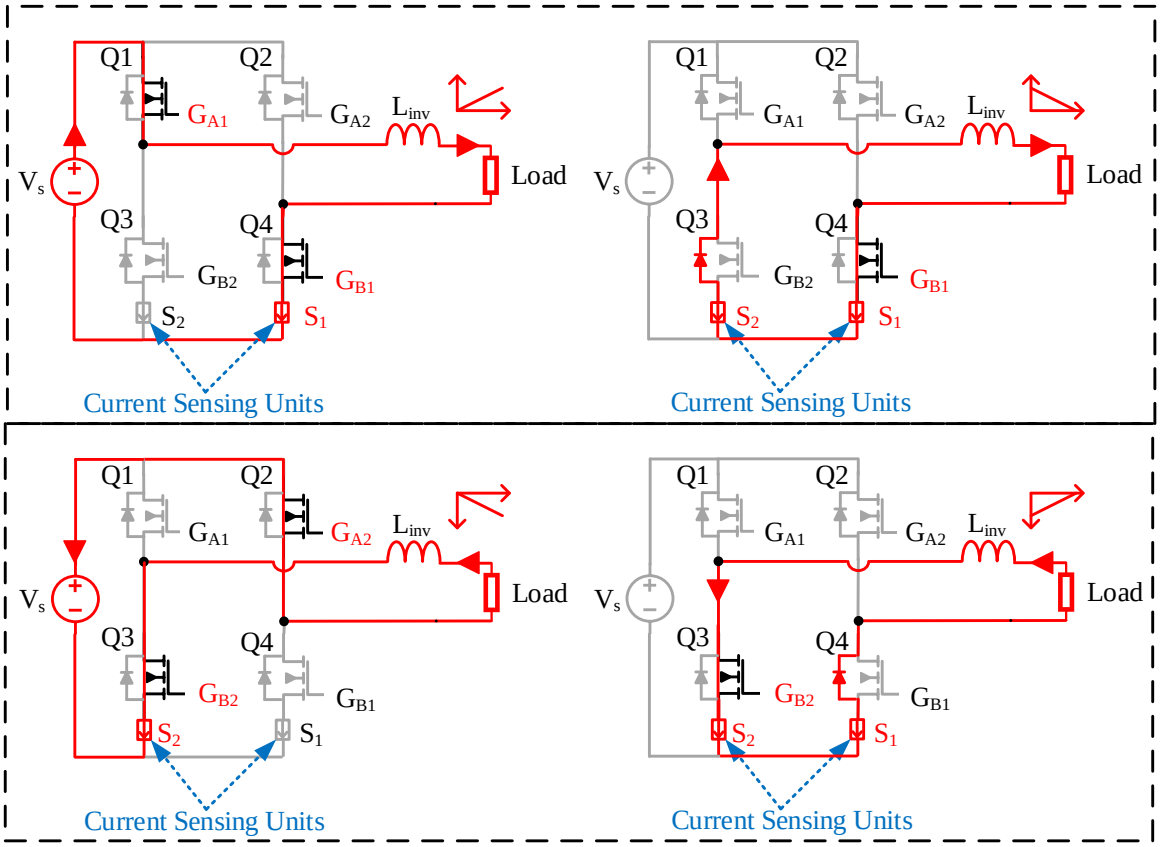


Figure 7.21: **Inverter operation**: The system operation for the BCM operation in the inverter, proposed by SenseGaN current mirroring techniques. The current path highlighted with red one shows the four modes of operation.

To understand the inverter operation, the current path is highlighted in Fig. 7.21. Knowing this, the fundamental switching frequency of the grid is considered as $60Hz$, where two bottom devices (Q_3) and (Q_4) turn on/off in each positive and negative cycles. However, the top switches (Q_1) and (Q_2) operate at the high switching frequency. Using the fast microcontroller (TMS320F28335) for the input signal and the analogue fourth order RC-filter using high-speed operational amplifiers (LM4820) will generate the reference signal. Therefore, the output of the current sensors will be compared with the generated reference current through the high-speed comparators as shown in Fig. 7.22.

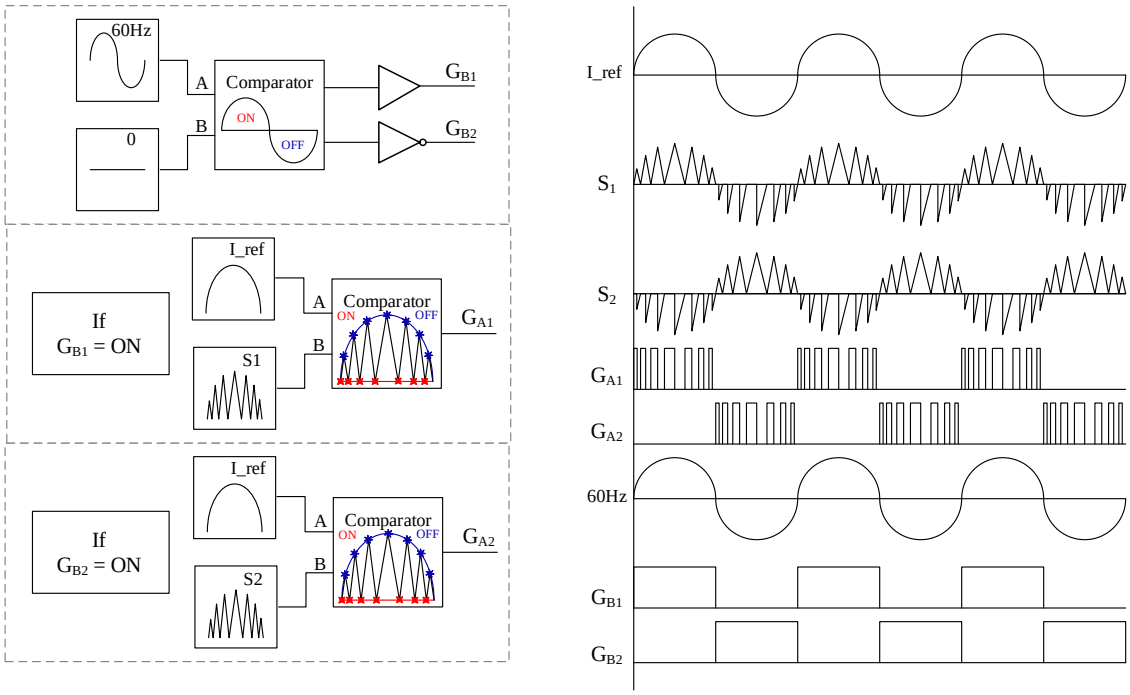


Figure 7.22: **Proposed BCM technique**: The analogue circuit logics for PWM generation through SenseGaN and the fundamental frequency of the grid.

The CHIL test result verifies the feasibility of the proposed BCM control strategy in a single-phase inverter as shown in Fig. 7.23 and Fig. 7.24. The microcontroller generates the switching signals for the four GaN switches based on the comparison between the current reference and the inductor current captured by the sensing GaN.

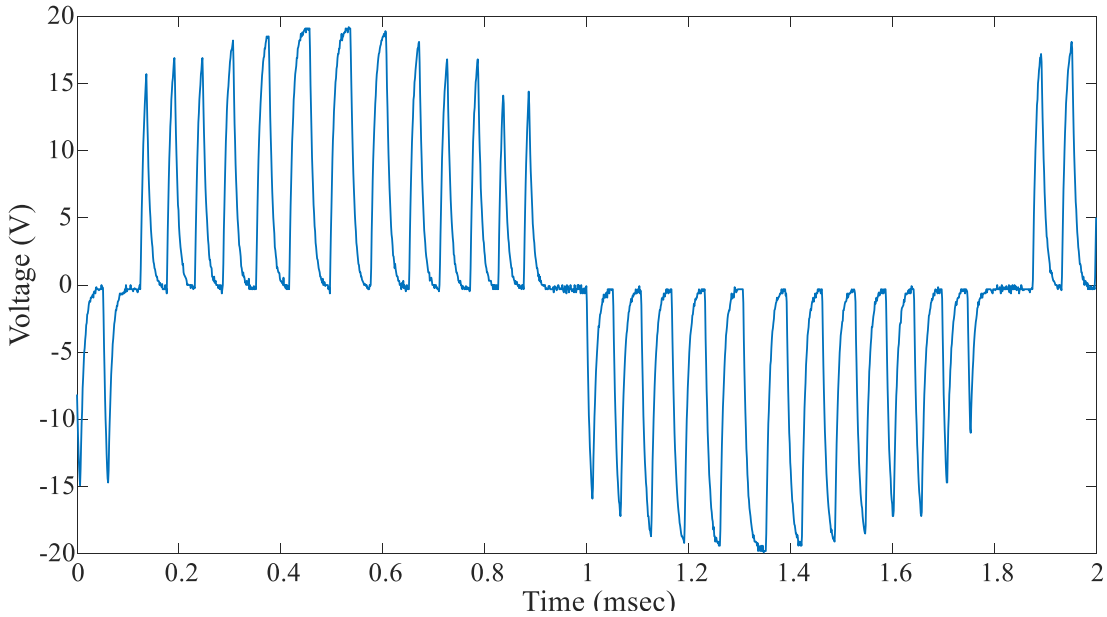


Figure 7.23: **SenseGaN for the BCM control of a DC-AC converter**: Two reference trigger signals are considered to turn-on the bottom devices consecutively. The closed loop operation of the DC-AC converter operation is verified in CHIL (blue: grid voltage)

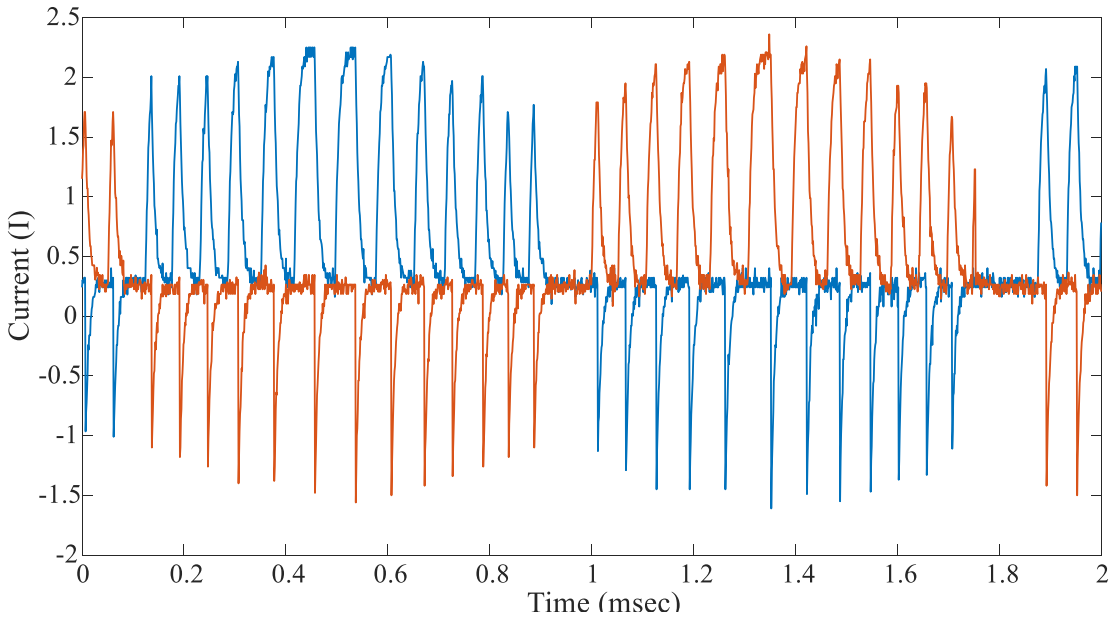


Figure 7.24: **SenseGaN for the BCM control of a DC-AC converter**: Two reference trigger signals are considered to turn-on the bottom devices consecutively. The closed loop operation of the DC-AC converter operation is verified in CHIL (top: bottom SenseGaN-1, orange: bottom SenseGaN-2)

Each SenseGaN current unit (S_1 or S_2) is used in each positive or negative cycle of the reference current. In the positive sequence, (Q_4) is turned on continuously. If the active switch current of the (Q_4), (I_{S1}), is zero, corresponding switch (Q_1) is ON. The inductor current is increased based on the inductor voltage and the inductance value. Once the inductor current reaches the current reference, the switch (Q_1) is turned off and the bypass loop with a diode in (Q_3) making the conduction path to decrease the inductor current to zero. Therefore, the BCM operation can be achieved with variable switching frequency based on the inductance, the input and output voltage, and the reference current. In the negative cycle, same procedure occurs with (I_{S2}), (Q_2), and (Q_3). The main important part numbers used for all the prototypes is provided in Table 7.1.

Table 7.1: Components in converter circuit design

Item	Manufacturer Part No.	Description
1	GS66516B	GaN transistors
2	SI8271GB-IS	Isolated gate driver
3	PES1-S5-S9-M-TR	Isolated power supply
4	ACM4520-142-2P-T000	Common mode choke filter
5	CD0603-Z3V9	Zener diode
6	LM6154BCM	OpAmp 100MHz Bandwidth
7	CL10C820FB8NNNC	82pF Filter capacitor
8	C1608X7R1H104K080AA	$0.1uF$ Bypass capacitor
9	C5750X7R2E105K230KA	$1uF$ Bypass capacitor
10	ERJ-3BQF1R0V	1Ω Resistor
11	ERJ-3EKF20R0V	20Ω Resistor
12	ERJ-PA3F4701V	4.7kΩ Resistor
13	ERJ-FC0603E50R0BST1	10kΩ Resistor

CHAPTER 8: CONCLUSIONS

This dissertation presented a new foundation to investigate the real-time reliability assessment of high-frequency power electronics converters, which the specific focus on GaN power devices. The fundamental failure mechanism of GaN power devices in today's technology was investigated, and the potential failure for the lateral GaN devices is studied intensely. The main concept of this dissertation was to provide a new path toward integration of advanced sensing method along with the applying the sophisticated and accurate analytical tools for deep leanings. A new methodology was developed for in-depth learning reliability analysis of high-frequency power converters with an edge. We proposed the deep LSTM for data training of power devices on the cloud server, and apply the reliability model for device resistance changes. The approach relied on the real-time $R_{ds(on)}$ data extraction from the power converter, and calibration of an adaptive model. The analysis was extended on an embedded system system-on-chip (SoC-TX2) using the CPU and GPU separately. The results showed the real-time convergence of the system with less than 11% average error, $85ms$ processing time through the GPU for power MOSFETs.

Due to the limitations of having enough data for the training and processing the system, co-simulation of GaN power devices was applied using FEA simulations. In this platform, the analysis of the aging of the GaN devices due to the soldering was developed on the cloud. Therefore, the simulation platform generates enough data for stress-strain loss generation of the solder fatigue, which eventually resulted in device $\Delta R_{ds(on)}$variations. This work was built on Hybrid Condition-based prediction known as Prognostics to assess the behavior of individual units based not only on their usage history as inferred from monitoring data but also on expected future load profiles.

More specifically, the focus was on deploying deep learning algorithms to exploit for the parameter estimation in power electronics engineering reliability. With the availability of the most granular information deduced from advanced devices, the new data-driven scheme can be used for system monitoring and possible lifetime extension GaN power converters.

For the future of this work, various things can be developed or improved. This work only focused on the fatigue analysis of solder joins as one of the most susceptible points in compound semiconductors such as GaN. While the other potential failure mechanism has not been studied here. Moreover, more samples are required to show the accuracy of the model in the longer term, which effectively can be helpful for improvement of the system modeling. The focus of this work was only on the static device resistance variations; however this would be extended to the extraction of dynamic $\Delta R_{ds(on)}$to distinguish device and package level failures. In the end, the integration of the advanced module of SenseGaN for advanced monitoring of GaN devices was only developed in the discrete model. Toward the integration of sensing and power devices for developing the smart modules can also be done.

CHAPTER A: PCB EMBEDDED INDUCTORS FOR HIGH-FREQUENCY POWER CONVERTERS

A.1 Introduction

This section presents a comprehensive method for designing a PCB embedded inductor suitable for high-frequency GaN-based converters, i.e., $5-20A$ and $< 10MHz$. The developed multi-objective algorithm is to maintain high efficiency of the power converter while achieving the desired power density. In particular, we consider all spatial parameters of embedded power inductor and formulate a procedure to maximize the inductance and minimize the resistance, and consequently minimize the temperature rise. The numerical calculations using the proposed method are verified through detailed FEA simulations. Finally, a very high efficient PCB embedded inductor with $50nH$, $8m\Omega$ total resistance (DC+AC) for 18A converter is presented, and its performance is evaluated through detailed FEA simulation and experiments.

Custom-designed inductors solicited in many ways represent an integral part of almost any power electronics converters. In many low-frequency applications, ferromagnetic core and magnetic-core inductors are used due to high and constant permeability, but in high-frequency power converters due to increasing core losses and temperature rise restrictions, magnetic inductors may not be used [95]. Therefore, replacing the magnetic core with air core can be proposed as one of the promising solutions. Different types of air-core inductors have been presented in many articles and for various applications; however, considerable challenges such as complexity of fabrication, low-quality factor, low efficiency, and high cost have been addressed. Among air-core inductors, PCB embedded ones are attractive due to their high-power density, desirable performance characteristics, low cost, and ease of manufacturing, which can

bring benefits of miniaturization and integration of the power circuits [96, 97, 98, 99]. To optimize the inductor design for a given application, much research has been done in literature, combining radio frequency circuits and power electronics to design SMPS with switching frequencies in the very high-frequency range (30-300MHz), but this range of frequency is more suitable for resonant DC-DC converters [100, 101, 102]. Even at the lower frequencies (13.56 MHz), some applications of PCB embedded inductors have been investigated in $\Phi 2$ class converter, whereby reducing switch voltage stress, 388W converter with 77% efficiency at 170 V nominal voltage is designed [103]. In [104], also the design of optimized PCB air-core toroid for high-frequency DC/DC converters with strict requirements in terms of volume and noise has been described. Thanks to the toroidal geometry, the energy is conserved inside the coil, and most of the flux is concentrated in the inner part of the toroid to minimize the absorbed energy [105]. Employing a non-air core PCB embedded inductor, and depending on the material and the shape of the core, anisotropic core losses, and the need for isolation between the magnetic foils, the multi-objective design is presented in [106]. For non-embedded inductors, more research can be found to optimize the design from various aspects [107, 108, 109, 110].

A useful compromise between efficiency and power density of a boost spiral inductor on 3.2kW is achieved using an optimized design procedure for power factor correction converters development. As shown in [108], there is a challenge in designing the PCB embedded inductor with a high-quality factor, i.e., high inductance with low resistance. For example, [111] describes a choice of hollow or full winding structural designs to maximize its quality factor based on the innermost and outmost radii of the winding as a measure of the hollowness of the winding for a coreless printed spiral winding inductor. In contrast to the aforementioned studies, the objective of this work is to conduct a comprehensive analysis, and design of PCB embedded air core inductors suitable for smoothing the output current of a voltage sourced inverters.

As the typical range of switching frequency for the inverters thanks to semiconductor developments such as GaN switches or Si-based AC-Stacked inverters, cannot be above 10MHz, the quality factor will be significantly lower compared to resonant DC-DC converters. To compensate this reduced value, inductor needs to be designed such that to maintain the high quality-factor and conclusively lower resistance. As expected, lowering the resistance not only helps to increase the efficiency due to the reduced conduction loss but also does help to reduce the thermal power loss dissipation, which results in a lower temperature rise of the inductor and higher power density. The focus so far has been towards achieving high inductance; however, in many emerging applications including utility applications, very high efficient inductor is required. Referring to [112], in inverters operating with 1-10MHz switching frequency, inductance value in the range of 50-300nH is sufficient to maintain the output current Total Harmonic Distortion (THD) below 5%.

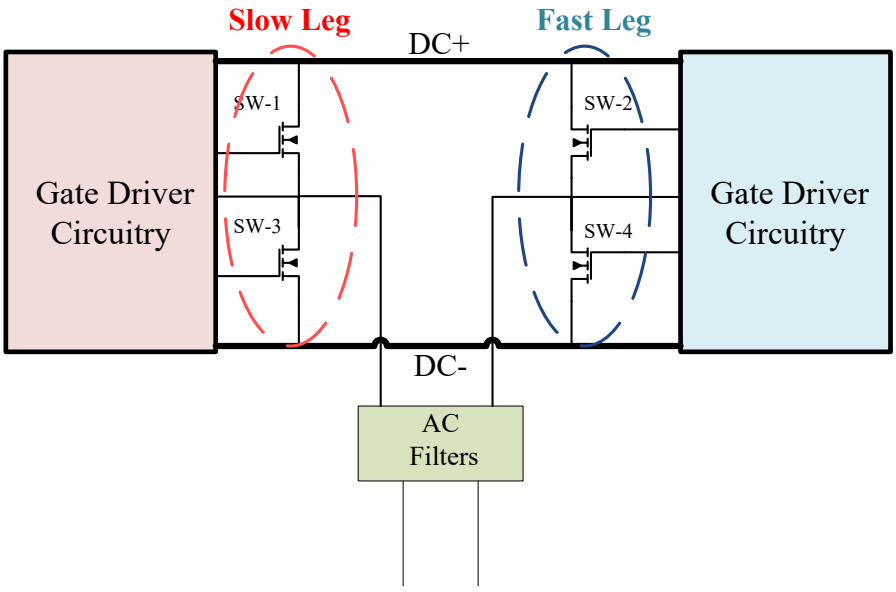


Figure A.1: **Schematic configuration**: The hybrid sinusoidal unipolar DC-AC converter topology considering one leg as fast switching, the second leg switching with grid frequency.

To effectively increase the efficiency of the inverter, one of the methodologies is to

provide hybrid sinusoidal unipolar switching pattern, where one leg of the inverter operates at grid switching frequency, and the other leg operates at much higher switching frequency as it shown graphically in Fig. A.1. Therefore, there is a great potential to run the converter at continuous conduction mode to get the benefits of full modulation with constant switching frequency, which make using PCB embedded inductor as a great candidate for this configuration. The most important research and applications of PCB inductors are summarized in Table A.1. To best of my knowledge [113], no prior work has been published to provide a comprehensive framework to design toroidal PCB embedded inductors considering the power density and efficiency (>98%) for such inverters.

Table A.1: Summary of important research on PCB inductors for power applications

Article	Inductor	Resistance	Current	Efficiency
Anderson [95, 98]	$50nH$	$209m\Omega$	N/A	N/A
Sullivan [97]	$230nH$	$10m\Omega$	<3A	<96%
Cheon [99]	$<10nH$	N/A	<200mA	<80%
Liang [103]	$150nH$	$42m\Omega$	<2A	<80%
Orlandi [104]	$150nH$	$42m\Omega$	N/A	N/A
Sullivan [111]	$20nH$	$50m\Omega$	N/A	N/A

A.2 The proposed method for the high-current PCB embedded inductor

The proposed multi-objective method formulates all the input/output variables for designing a PCB embedded inductor. The proposed method decouples ohmic losses of petals and vias for achieving high efficiency to get a lower temperature rise and tunes up parameters to obtain desirable inductance value. As shown in Fig. A.2, the algorithm process is running through three major sectors: 1: inductance (filtering) 2: petals (efficiency) and 3: vias (temperature rise) design considerations in six sequential levels. The algorithm starts from level-0 in which the baseline criteria for electrical and mechanical constraints are set. Mechanical constraints are inductor type (here toroidal), number of turns, height, inner and outer diameters. In this

work, electrical constraints are set as input voltage: 35Vdc, duty cycle: 50%, input DC current: 9A, output AC current: 18A rms, switching frequency: 1-10MHz, and desired output current ripple: <1%. The three major design sectors will be explained in the following steps.

A.2.1 Inductance design considerations

This sector calculation is performed to find the proper inductance value for the output filter of inverter considering the most prominent factors. Initially, a set of constraints need to be set such as the via minimum diameter, i.e., 1mm and the inner diameter ten times larger enough. Then, through an iterative process, the outer diameter and the number of turns will be adjusted to obtain the desired inductance.

$$L = \frac{N^2}{2\pi} h\mu_0 Ln(d_o/d_i) + \frac{d_i + d_o}{4}\mu_0\big[Ln(8\frac{d_i + d_o}{d_i - d_o}) - 2\big] \tag{A.1}$$

where N is the number of turns (petals), $h$is the PCB thickness (inductor height), μ_0 is the air permeability, d_i and d_o are the inner and outer diameters, respectively. As it shown in (A.1), by increasing the outer diameter, the number of turns, and height the inductance can be intensified; however, increasing the outer diameter may not be acceptable considering the desired density. Therefore, one solution would be to set the outer diameter and adjust the height and number of turns. With today standard manufacturing capability, one can easily obtain up to 35mm thickness for PCB and consequently, the number of turns that plays the dominant role in the inductance value. As it can be shown, the efficiency exacerbates due to this increase and a designer may have to adjust other parameters such as the inner diameter again. Nonetheless, the design proceeds once the desired inductance and density are obtained numerically, and in the following sectors, the efficiency will be optimized.

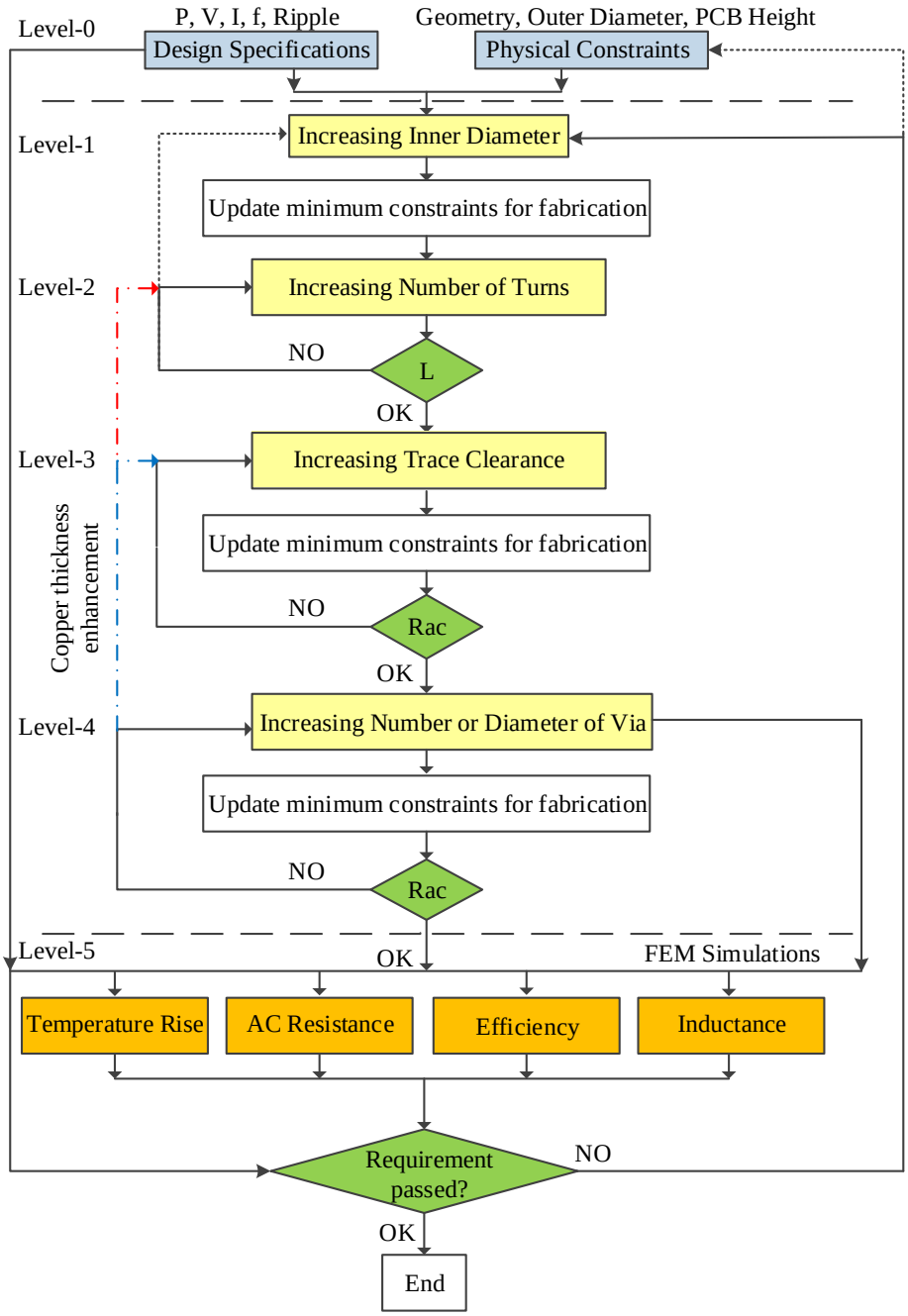


Figure A.2: **Optimization approach**: The algorithm descriptions to achieve the lowest resistance at the highest possible power density for the PCB embedded inductor within the 1-10MHz.

A.2.2 Petal design considerations

In this sector, the aim is to find the optimum petal size. Essentially, once the number of turns in the previous sector is set, the clearance between the petals are

adjusted to minimize the DC and AC resistance. The governing equation in this sector is (A.2):

$$R_{total} = N(2R_{petal} + R_{in-via}/N_{in-via} + R_{out-via}/N_{out-via}) \tag{A.2}$$

where R_{petal} is each petal resistance. R_{in-via} and N_{in-via} are the inner via resistance and numbers, $R_{out-via}$ and $N_{out-via}$ are the outer via resistance and numbers, and N is the number of petals (turns). In (A.2) the DC resistance, as well as AC resistance due to the skin and proximity effects, are considered. It can be shown that by petal clearance decrease, the skin effect is reduced, but the proximity effect is increased. Therefore, the total resistive losses are examined in this sector by adjusting the petal clearance. Further adjustment is performed in the next section to achieve the desired efficiency. In other words, a designer may relax the constraints in this step and conclude on the efficiency in the next step.

A.2.3 Via design considerations

In this part of the algorithm, via diameter and number are set in order to reduce the total resistance of the inductor further. Equation (A.2) still applies and contains two variables for the inner and outer vias. One approach to solve this optimization problem is to impose a set of constraints, for instance, the minimum diameter for a via, and continue the calculations using the constraints as boundary conditions. This process is performed for all the variables, and the result with the lowest resistance will be picked. In many applications, absolute temperature rise needs to be estimated in addition to the efficiency. Therefore, equation (3) is presented as the final step to verify the desired temperature rise for the minimal current.

$$\Delta T = kI^2(\sqrt{f} + \alpha)/x^3 \tag{A.3}$$

In (3), f is the switching frequency of the converter, and I shows the rms current. Moreover, k and α are constant numbers, and x is the ratio of the length to the surface area of the inductor. If the desired temperature rise is not met, the presented algorithm runs recursively to find an alternative solution. The details of the mathematical correlations are provided in [96, 112, 113].

A.3 Simulation and experimental results

In this section, the result of the optimization method will be analyzed and benchmarked with an example using JMAG software and a lab prototype. As stated in the previous section, the first step is to define the set of baseline electrical properties. In this work, it is assumed that the PCB-embedded inductor will be applicable for a single-phase inverter with the following nominal specifications: $35VDC$, $8.5A$ DC, 50% duty cycle, low frequency ($50/60Hz$) output current 17A AC, output current THD <1%, switching frequency 1-10MHz. The maximum temperature rise for the board is assumed to be $40C$. It can be shown that the inductance value in the range of 10nH to 100nH would be sufficient for such an inverter. Consequently, the design procedure was conducted to obtain such inductance while the occupied area and efficiency were optimized.

In this process, a designer can observe how the algorithm proceeds with all the possible acceptable solutions and choose the best one. For instance, different acceptable inductance values are obtained varying the power density and the number of turns while the efficiency is optimized. Since efficiency is one of our main concerns, $50nH$ inductance values with eight turns and the outer diameter of $30mm$ were selected as the optimum design (Fig. A.3). It is worth noting the unacceptable regions in Fig. A.4 in which the temperature rise is out of the acceptable bound, i.e., $40C$.

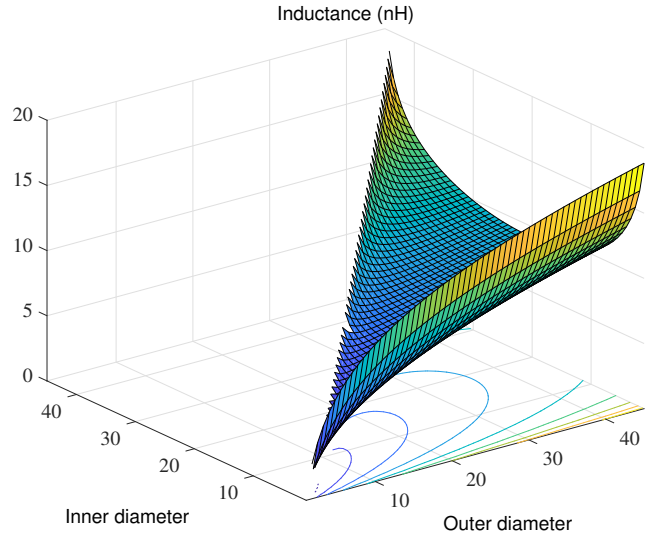


Figure A.3: **Numerical results**: The algorithm procedure for providing possible solutions for power density, and filtering requirements meeting from level-0 to level-2 based on proposed method. The selected candidate will be highlighted when the multiplying of the concavity and the derivative of function reach to optimum values. The possible solutions can be used for running the algorithm from level-3 to level-5.

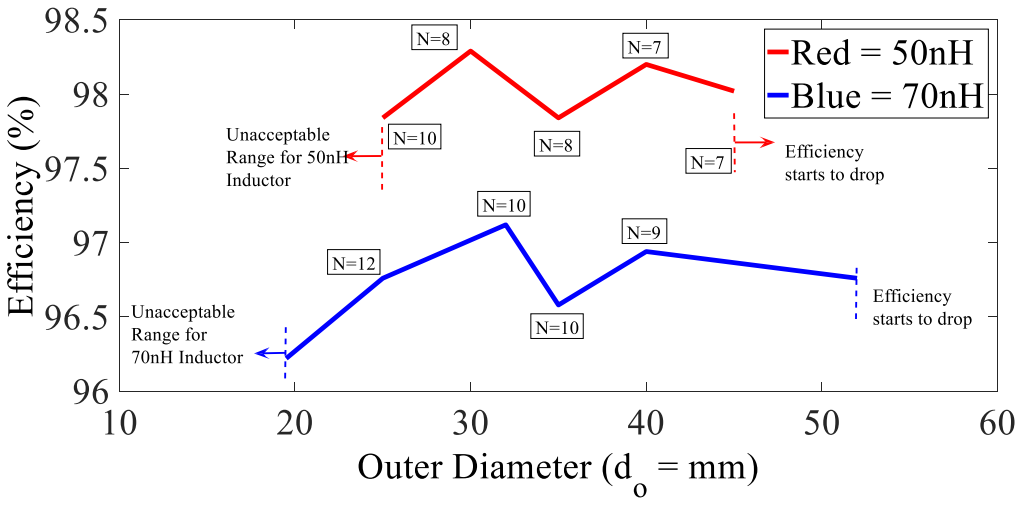


Figure A.4: **Simulation results**: The efficiency variations of the constant inductance with the minimum possible resistance, at the specific allocated area, are depicted through the algorithm. This shows that a high efficient inductor can be achieved in various geometry configurations with different outer diameter and number of turns; however, the smaller size is more desired to reach higher power density. The inner diameter of the inductor is set to 15mm to keep the temperature rise lower than $40C$ for $18A$. This provides a comprehensive legend for PCB embedded inductor designers in the defined frequency and power range.

CHAPTER B: CURRENT MEASUREMENT TECHNIQUES FOR HIGH-FREQUENCY POWER CONVERTERS

B.1 Introduction

Almost in all the power electronics applications such as power conversion in solar Photovoltaic (PV), wind turbine systems, motor drives, hybrid electric vehicles, current sensingâs role is highlighted significantly. Having accurate current sensing makes controlling, protection and monitoring feasible at different levels of power electronics systems. Modern the field of high-frequency is now more focused on the investigation of alternative and contact-less measurement approaches for higher efficiency [114, 115, 116, 117]. In traditional Si-based power converters, the frequency of the power circuits was relatively low (<100kHz), hence the rate of is limited. Thanks to the development of new generations of WBG transistors, switching frequency of new converters is increasing dramatically, i.e.,>1MHz and >30V, which requires more accurate, faster response and higher bandwidth current sensors [118, 119, 120].

There are various techniques to implement current sensing of power electronics converters. Utilization of these methods depends on applications, and it could be varied based on control strategy, overcurrent protection. This chapter focuses on possible techniques related to high-frequency current sensing, which can be implemented onto PCB to reach higher power density and integration. To evaluate the performance of these techniques the following factors have been taken into account: simplicity, response time, accuracy, power consumption, the practicality of implementation for high-frequency converters, the sensitivity to temperature and offset adjustment, and topology dependency. The most common techniques are: resistor-based, filter-based, inductor-based, hall-effect based, and MR-based.

B.2 Resisor-based current sensing

One of the simplest concepts to measure the current is resistor-based current sensing. The objective of this method is to measure the voltage drop across a sense resistor, which can be a simple representation of actual current [63, 76]. The crucial point is the performance of the measurement resistor had to be precisely characterized before as the characteristic of the sense resistor significantly affects the voltage drop across that and consequently changes the current measurement. These techniques can be effectively applied for most of the low switching frequency and high current or high switching frequency and low current applications. There are multiple methods for implementing this technique such as an external sense resistor, the internal resistance of the filter inductor, measurement of the drain-source of transistor resistance during turn-on $R_{ds(on)}$, and SenseFET [116].

In general, since the voltage drop across the resistor at high current increases proportionally to the current, the ohmic losses are also very high. Even considering the lower resistance in the main current path cannot solve the issue, as more conditioning circuit needs to be added. But since the lower resistance provides a lower voltage drop, this removes all the current ripple information, which cannot be practically retrieved by adding any additional circuits. Therefore, this method in power electronics converters has significant issues, especially at high power and high-frequency. Fig. B.1 shows the schematic of resistor-based current sensing.

The other method is to measure the internal resistance of the inductor in the market. This method inherently has the lower cost because of using the same inductor of the converter and potentially has higher accuracy. However, this method can only measure the current across the inductor path, which primarily can be varied from one topology to another. In other words, this technique cannot always capture the current across the required section for monitoring. Besides, this method cannot be implemented in high power applications and also where the switch current information

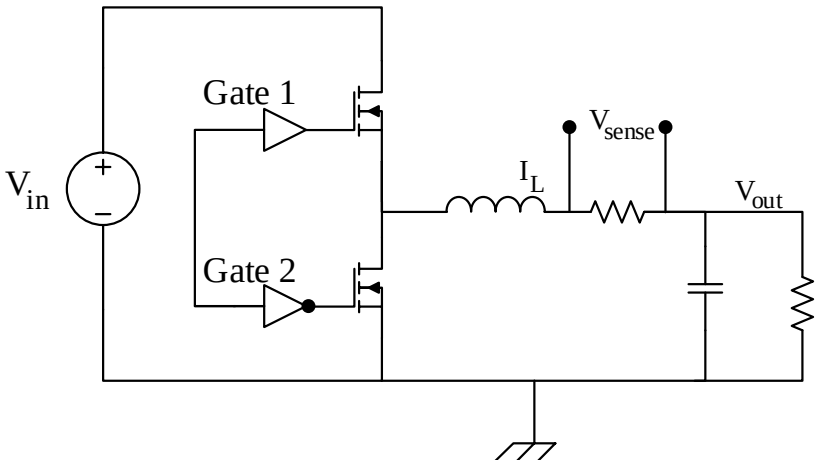


Figure B.1: **Shunt method**: Schematic of external sense resistor for capturing the inductor and output current. The voltage drop across the resistor theoretically can represent the actual current waveform; however, this method in practice has a lot of issues for high-frequency and high current applications.

is required. Measuring electrical resistance of MOSFETs have been used in [120]. This technique assumes that a transistor behaves like a resistor when it is the active region. This technique theoretically can be effective because there is no need to add a current sensor on the power path that can reduce the cost and the loss of the system. In most of proposed articles, this technique relies on calculating $R_{ds(on)}$ in (B.1):

$$R_{ds(on)} = \frac{L/W}{\mu C(V_{in} - V_{th})} \tag{B.1}$$

where L and W are length and width of transistor channel, C is the capacitance of oxide, μ is electron mobility, and V_{in} is the voltage across the switch and V_{th} shows the threshold voltage of the MOSFET. However, in reality, threshold voltage and the capacitance of oxide can be varied over the time under thermal and electrical aging. Moreover, it has also been shown the internal resistance of transistors in both Si-based and WBG-based technologies will be affected by junction temperature. Therefore, the

accuracy of this method is not guaranteed due to the variable performance of $R_{ds(on)}$ under hard switching, and higher temperature. The SenseFET approach has also been implemented in various applications for MOSFET technologies shown in Fig. B.2. In this technique, by adding another transistor with a scaled-down version of W/L, the actual waveform can be captured. The drain and gate of the measurement transistor would be the same as the main switch. Then, the source of measurement transistor will be connected through a Kelvin connection to a resistor, where the voltage drop across the resistor is representative of the main current.

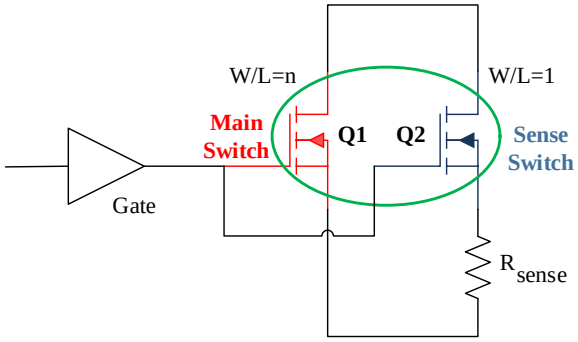


Figure B.2: **SenseFET**: General scheme of SenseFET. This technique should be implemented in an integrated package for higher performances.

This technique could be useful at low frequency and chip design, it is not isolated, and it has some technical challenges such as the difficulty of calibration, impedance matching, and bandwidth limitation at discrete design. The latter comes from the fact, and the measurement transistor typically should have much lower W/L, which requires both transistors have the same fabrication technology.

B.3 Filter-based current sensing

The other approach for current measurement is a filter-based technique, where the new RC filter in parallel has been added to the RL network of the output filter. By knowing the total impedance of the inductor, the equivalent series resistor of the

inductor, additional capacitance and resistor will be added accordingly such that the voltage drop across the filter stage can represent the current waveform.

A new technique is proposed for accurate filtering, actively calibrate the measurement, and consequently compensate the dynamic changes of passive components in [76]. However, this approach like resistive-based current sensing method, potentially has big challenges at high current and high-frequency due to lack of isolation, the variability of passive components over the time, complexity for implementing in the discrete design shown in Fig. B.3.

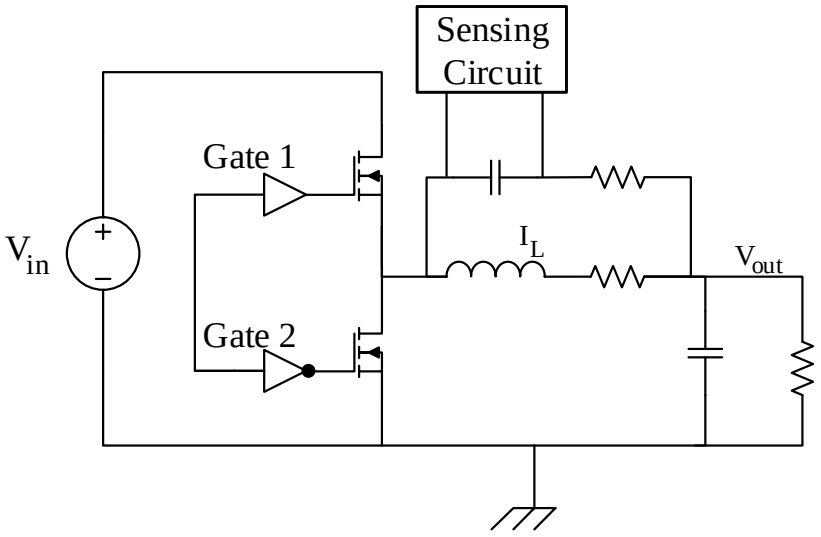


Figure B.3: **Filter method**: General schematic of filter-based current sensing. The active calibration for the passive element is required, and the common-mode voltage issue still exists in this approach.

B.4 Inductor-based current sensing

The other approach is induction-based methodology which introduced in various types to induce the voltage or current in the secondary circuit as the measurement. In wide area, these approaches can also be implemented with various technique, but they can be categorized as three main groups: AC current transformers, DC current transformers, and Rogowski-based current sensing techniques.

The AC current transformer is not a new concept. This method induced the current in the secondary winding and potentially has high performance for current measurement and can be applied in many power electronics applications. Although previously these transformers have been built in bulky, nowadays some companies like Coilcraft released high-performance current transformer sensor (CST7030 and CST4835) in small packages. They can measure the current at 20A, 48V, and 1MHz. However, due to the importance of capturing the DC current of converters, they are not very attractive for power electronics modules.

In DC current transformer, they typically have at least two cores with a rectifier, then the voltage drop across a resistor at the measurement section can provide current information. Due to the utilization of coil inductors, they can suffer from the saturation at the high switching frequency, and their typical applications in the market are not going beyond 100kHz. Rogowski-based current sensing, due to its inherent simplicity, and no bandwidth limitation is among the most popular techniques in high-frequency power converters.

The Rogowski-based current sensor typically consists of an air-core inductor with a low number of turns, where the primary current of the conductor can induce it. Then the picked up current information can be transformed to the voltage through an integrator circuit. They might be equipped with a reset signal to indicate the start and end point of integration [117, 121]. The captured voltage can be a good representative of the actual current waveform. In literature, this technique has been implemented successfully in many different ways, including high switching frequency WBG-based converters. There are multiple ways to improve the performance of the sensor such as decoupling power and control stage around the sensor area, implementing in a broader area, or also bringing a new shielding on control section of the sensor. One of the most common recommendations is to keep the pick-up current coil far from any magnetic component, which gives more immunity for pick-up coil. However, these solutions

also sacrifice the power density and bring more complexity for the measurement.

In practice measuring the inductor current and transistors are very critical for high-frequency converters. The information can be utilized for implementing the advanced controlling methods, or diagnostics of power switches. In the Rogowski-based method, inducing the current in the inductor creates a mutual inductance in the power loop, which potentially is a hazard for high-frequency converters. This comes from the fact that any unwanted magnetic fields near the pick-up coil should be avoided to reduce the chance of susceptibility of this method to noise. Therefore, this method needs accurate knowledge, thorough understanding and proper design of EMI on the converter power stage. The experimental results are reported in [67].

B.5 Hall effect-based current sensing

One of the most popular methods for measuring both AC and DC current is using Hall-effect sensors, which works according to Lorentz force. Due to the generation of magnetic fields in passing of current through a conductor, a voltage can be induced across a Hall element and represents the current waveform. Hall-effect sensors due to their low power consumption, easier implementation on high switching frequency converters, immunity respect to noise and compact designs are desirable for both academia and industry. In general, there are two types of the Hall-effect sensor under open-loop and closed loop operation. Both have excellent capability to capture high current (30A), and relatively high bandwidth (1MHz). But their sensitivity to temperature drift and offsets will be changed accordingly. Therefore, this needs to be considered as careful design of Hall cell geometry. These sensors have been studied at various current, and their characteristics have been demonstrated vastly [118, 122].

Using Hall-effect sensors in high-frequency converters need careful layout considerations including an intelligent decoupling and isolation of power stage and control stage to reduce reflection of the hall-effect sensor by radiated noise and EMIs. It is worthwhile to mention that DC current measurement could be potentially a big issue

due to saturation at a high current level. The experimental results are reported in [67].

B.6 Magneto resistor-based current sensing

Anisotropic Magneto-Resistors are based on metal alloys as opposed to MRs which are based on low bandgap semiconductors such as InSb/InAs. The most widely used AMR devices, which developed and integrated into a chip is composed of four Permalloy (Ni0.81F0.19) AMRs in a full sensitivity Wheatstone bridge configuration [123, 67]. MR based current sensors work on the principle of detecting the magnetic fields generated by current traveling through a trace on the PCB shown in Fig. B.4. The MR based current sensor is placed on top or underneath a trace carrying the current without any conductive contact with the current trace. The low-frequency current through the PCB trace generates a uniformly distributed magnetic field, which passes through the sensor along the default axis and thus the sensor responds by sensing the magnetic field [124].

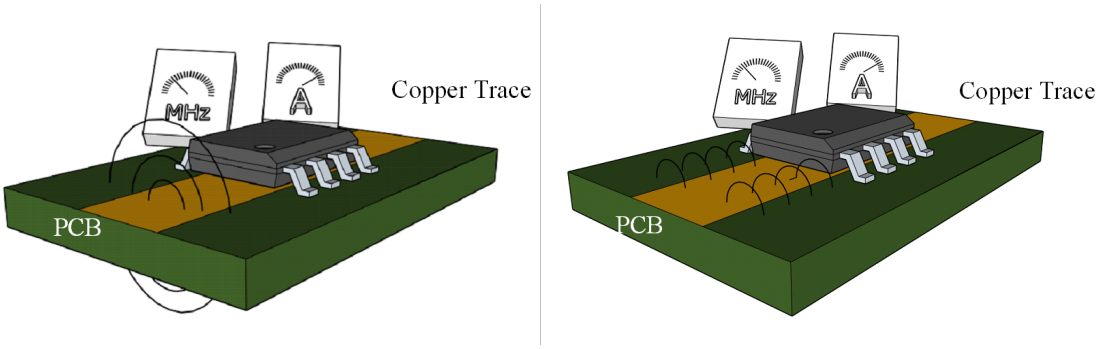


Figure B.4: **Magneto-Resistors sensor**: General operation of the contact-less AMR sensor: magnetic field generations at low frequency (left) and high-frequency (right) are shown.

For high-frequency current, especially above 1 MHz, the generated magnetic field is concentrated mostly on the edges of the trace due to the skin effect that results in a non-uniform magnetic field distribution around the PCB trace. Consequently, the detected magnetic field by the sensor is very weak at higher frequencies. For

high-frequency applications, due to skin effect, the magnetic field distribution is non-uniform and affects the sensitivity of the AMR based current sensors. Therefore, placing the sensor on the opposite side of the PCB for the current trace is not useful for accurate sensing above 1MHz. For better detection bandwidth and sensitivity, the magnetic field passing through the default axis of the sensor needs to be concentrated to make the field more uniform. Therefore, alternative and innovative magnetic concentration techniques need to be implemented to make the field normalized and more uniform.

CHAPTER C: ON SELF-HEALING OF SYSTEM LEVEL INVERTERS CONSIDERING CURRENT SENSOR INACCURACY AND AGING DEGRADATION

C.1 Introduction

Due to global warming in todayâs world, many governments encourage the renewable distributed generation technologies in power networks, and PV modules have led to a significant increase in system capacities [125, 126]. In power networks with high penetration of PV systems, an efficient and reliable operation of the system depends on the robust operation of the inverter system. Therefore, the robustness of inverters should be verified during the design and operation conditions [127]. To examine the robustness of grid-tied PV inverterâs, the comprehensive parameters are considered as efficiency, Total Harmonic Distortion (THD), Power Factor (PF) compliance, and Maximum Power Point Tracking (MPPT) accuracy.

The conversion efficiency has a significant impact on the robustness of PV inverters. This fact has been verified by multiple studies on control architecture, semiconductors modules, and physical component variations [128, 129]. The harmonic distortion analysis, as the second high impact index on PV system robustness, studied thoroughly in recent articles based on the power quality standards. Due to increasing the number of switching inverters in future smart grids, THD issue will become more severe[130, 131, 132]. Finally, PF compliance due to the reflection of distribution network reliability, as well as MPPT accuracy because of its dependability on ambient conditions and component inaccuracy, represent the robust operation of grid-tied PV inverters [133, 134, 135, 136, 137].

Therefore the Smart Inverter Robustness Index (SIRI) is used, as a performance

metric to evaluate the robustness of the grid-tied PV inverter systems [138]. The goal of this work is to model current sensor aging and propose a self-healing approach for performance improvement of the PV inverter systems. Then, a Kalman filter estimation techniques for compensation of the error will be used to mitigate the system error performance. The estimation method is an effective approach to improve the robustness of the system based on the state space model of the PV inverters. This is also helpful to build a platform for self-healing actions to enhance the system operation.

C.2 Robustness in Grid-tied PV Inverter

C.2.1 Smart inverter robustness analysis

Since the physical variations are a consequence of the inherent randomness in electrical components, to analyze the impact of these uncertainties on the performance of PV inverters, the system is statistically analyzed. For unformulated problems, Monte Carlo sampling method is used to provide sets of solutions with a particular confidence level. Since this approach requires a large set of random walks, advanced mathematical techniques should be applied to reduce the sampling time.

In this work, we use the stratified Monte Carlo, which is called Random Latin Hypercube Sampling (RLHS). The RLHS reduces overall sampling points and eventually improves the confidence level in the simulation. The cumulative distribution function of the model is divided into few equally probable sub-sections. Then, the equal number of sampling points will be selected from these sub-sections. Therefore, by spreading the sampling points, the minimum required sampling points will be reduced significantly [139, 140]. Finally, a novel SIRI parameter will be used to present the main operational characteristics of the grid connected PV inverters as shown in (C.1):

$$SIRI = Eff^* \times THD^* \times PF^* \times MPPT^* \tag{C.1}$$

$$Eff^* = \frac{Eff - k_{Eff}}{1 - k_{Eff}} \tag{C.2}$$

$$THD^* = \frac{THD - k_{THD}}{k_{THD}} \tag{C.3}$$

$$PF^* = \frac{PF - k_{PF}}{1 - k_{PF}} \tag{C.4}$$

$$MPPT^* = \frac{MPPT - k_{MPPT}}{1 - k_{MPPT}} \tag{C.5}$$

where PF^* represents power factor compliance, Eff^* is conversion efficiency, THD^* shows harmonic distortion, and $MPPT^*$ is the maximum power generated at the highest efficiency. For each performance characteristic, a limiting factor is defined. For conversion efficiency, PF, MPPT effectiveness, the imitating factor is the minimum acceptable based on standards. In our approach, the minimum acceptable conversion efficiency for the grid-tied PV inverter is assumed 95%; however, this value can be different based on application and configurations. The limit for PF compliance and MPPT effectiveness is defined as 99%. Finally, for the THD term, 5% is considered as the maximum acceptable value based on IEEE standard 519-1992. Assuming all positive terms of calculating in (C.1), SIRI results in a positive product which reflects the robust operation. Relative SIRI value defines the robustness operation of the PV inverter, and the maximum is limited to +1. However, if one or more terms of (1) get negative values, the inverter operates outside of the robustness region, and the SIRI will be flagged as -1 [138].

C.2.2 Inverter system modeling and challenges description

The general structure of the PV inverter controller model is proposed in Fig. C.1. This scheme consists of two cascaded control loops. In this figure, passive compo-

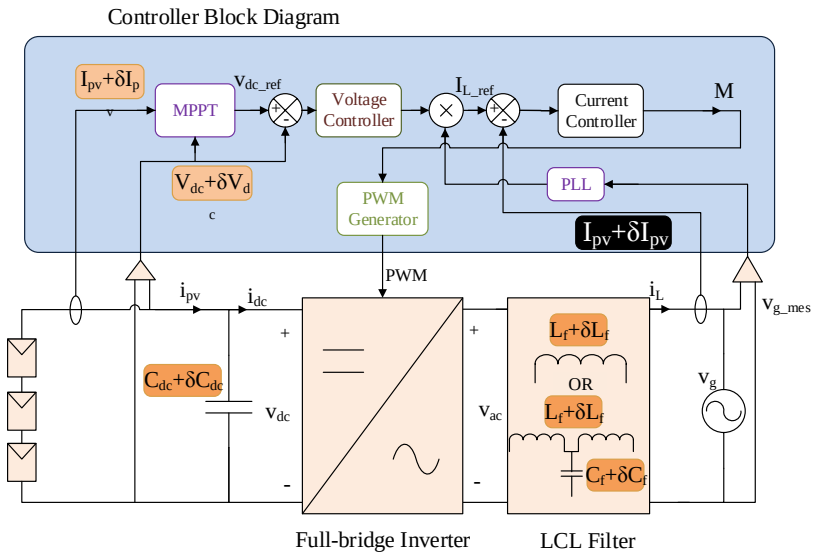


Figure C.1: **PV inverter schematic**: The proposed scheme for a single phase inverter with the control architecture

nents and sensing elements that could impact reversely on the inverter robustness are highlighted. The focus of this work is on output current sensing inaccuracies, which is shown as black. The mathematical modeling of state space equations are formulated to quantitatively track the single-phase inverter operation. The state variables are selected based on the DC input voltage, and output current injections with I_d and I_q components thoroughly discussed in [141, 142].

The controller effectiveness of a PV inverter could be affected directly by the current control loop. The previous study in AC-Stacked grid-tied PV inverters shows, with less than 18% measurement error, the converter enters to non-robust operation region. The condition could be more severe for single-phase PV inverters, with only 8% inaccuracies in the current measurement, the inverter loses its robustness. This study also shows that by using a proper filter algorithm, there is a chance to improve the current sensing performance and enhance the robustness of the PV inverters [143].

The current sensor response in two different scenarios with a minor and major covariance errors are depicted in Fig. C.2. This figure confirms by applying the Kalman

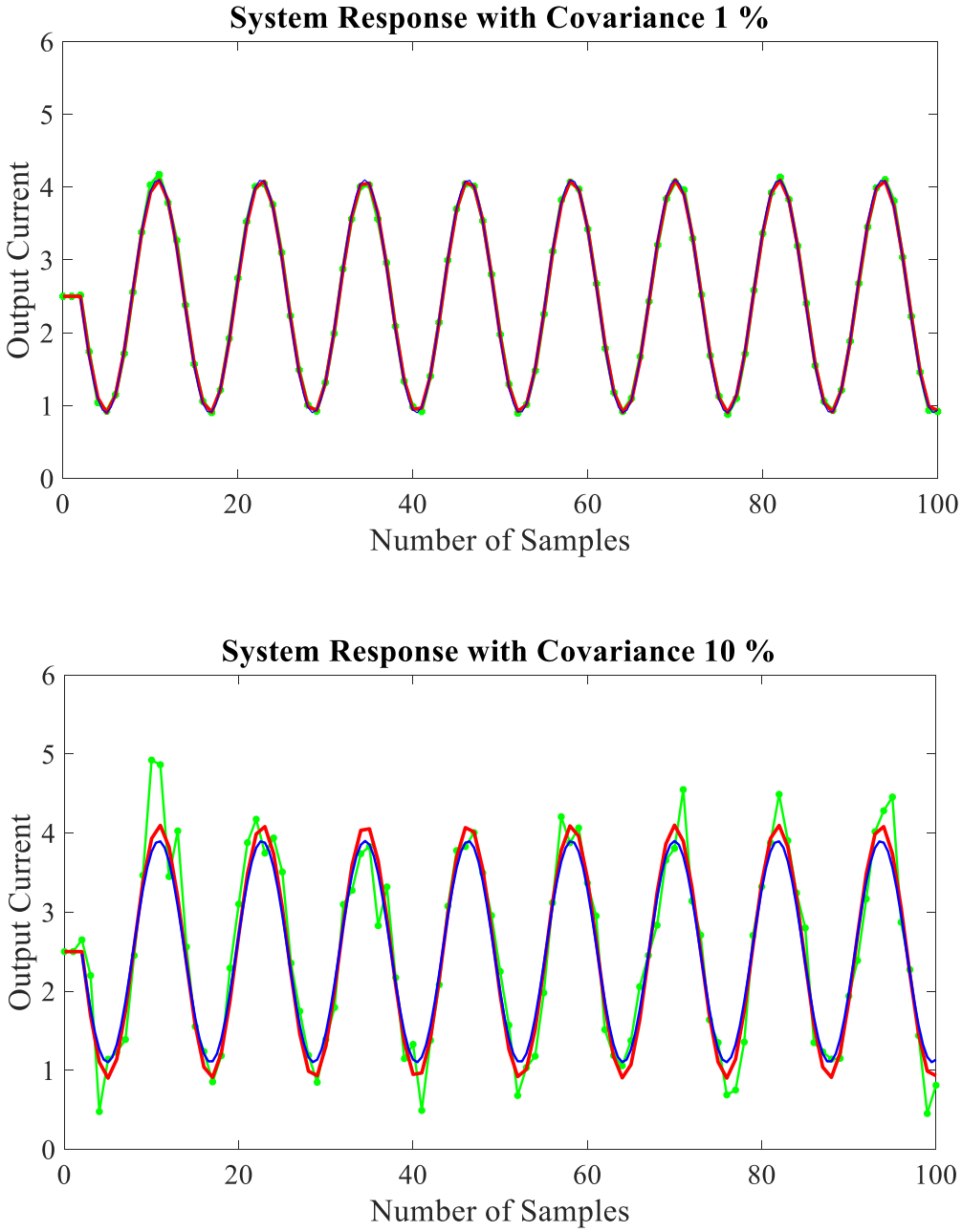


Figure C.2: **Simulation results**: The current sensor response under two different covariance measurement errors (1% and 10%). blue: ideal waveform, green: actual system reference response, red: modified system response correction with Kalman filter estimation.

filter estimator to denoise the current sensor output, the overall system response will be improved. The proposed model focuses on the manufacturer inaccuracy and sensor variations because of physical changes such as temperature and humidity. The

results also show when the plant observes the lower covariance sensor noise, the modified estimation is closer to the ideal waveform as expected. Although this model is a great example to confirm the potential of the estimation technique to improve the quality of the output current waveform, this method does not comment on the inaccuracy variations caused by the sensor aging. The reason refers to the sensitivity of the proposed model based on the applied filtering method. As the Kalman filter algorithm is mainly dependent on the physical model, and inaccuracy of the system modeling will result in wrong outputs. Therefore, there is a need to make a more precise model to improve the quality of the sensing limitations in the long-term runs.

C.3 Current Sensor Modeling

C.3.1 Sensor aging

The current sensor accuracy and its limitation have been discussed in articles as bandwidth limitations, temperature drift, and hysteresis saturation [63]. However, there are some other ambient condition variations such as temperature and humidity that effect on the current sensor features and inaccuracy.

For instance, in most of the Hall-Effect current sensors, zero current offset error, sensitivity changes, and non-linearity variations of the sensor respect to temperature have been reported [63]. For MR current sensors, non-linearity, or sensitivity to magnetic noise spectrum interference have been discussed in details in [67]. Lack of internal voltage references for flux gate sensors, or magnetic sensitivity in Rogowski-based current sensors are the most important limitations in the advanced sensors[76]. Although the new techniques for hybrid Rogowski-MR current sensor have been showed superior performance compared to the existing sensors, they are not commercially available yet. Therefore, it is crucial to model the current sensor performance due to the susceptibility to a noise and decouple them from system process noise [144].

In this study, a Hall-Effect current sensor (ACS730) is chosen due to its excellent performance under electromagnetic interfaces generated by the high switching

frequency inverters, and its relatively high accuracy. Based on the manufacturer datasheet, three different parameters of zero current offset inaccuracy, sensitivity changes, and non-linearity variations of the sensor are the main source of inaccuracies [145]. The absolute error of the sensor is represented as:

$$E_{abs} = E_{off} \times E_{sen} \times E_{lin} \tag{C.6}$$

where, E_{off}, E_{sen} and E_{lin} are zero current offset changes, sensitivity, and non-linearity variations, respectively. Therefore, the normalized covariance matrix of measurement error can be made accordingly. Since PV inverters will be used during days, the estimation modeling is derived based on white random error generation within the temperature range $10°C - 50°C$. This means the normalized covariance measurement matrix is modeled with (10% covariance error). Then, the updated observable matrix by applying filter gain will be replaced with measurement of the absolute value.

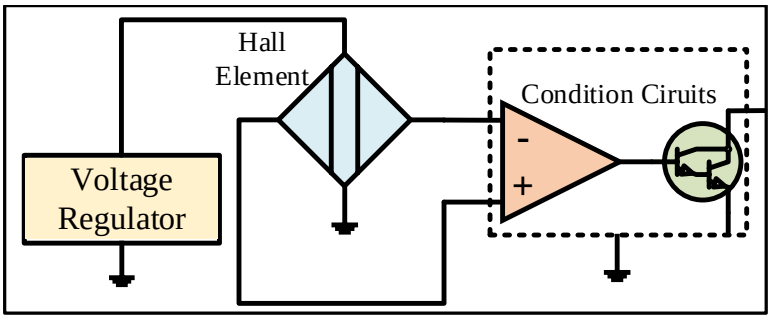


Figure C.3: **Current sensor model**: The scheme of Hall-Effect current sensor for age modeling.

For the aging model of the Hall-Effect sensor three major sections are consisting of a voltage regulator, Hall element, and the conditioning circuits as shown in Fig. C.3. Since the voltage regulator aging typically results in system trip protection, we focus only on the remaining items.

The sensitivity of the Hall-element could be varied based on the geometry and the

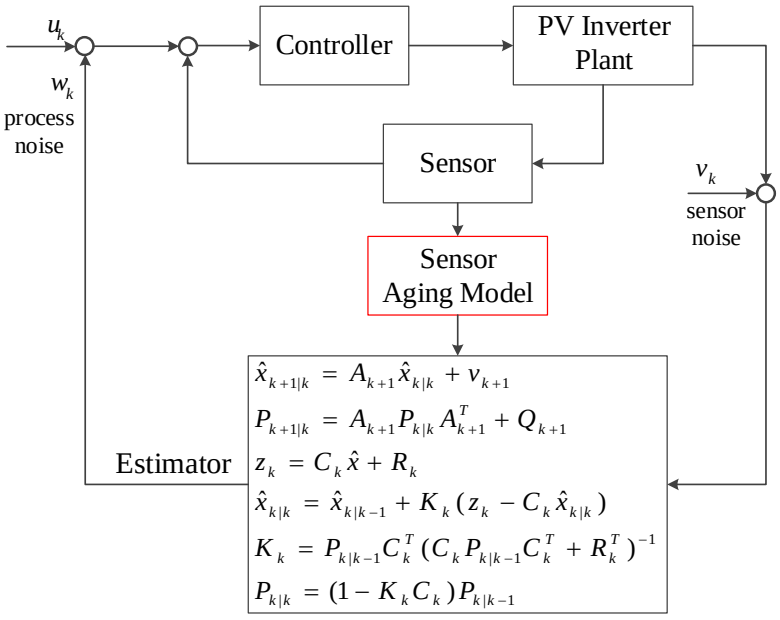


Figure C.4: **Self-healing scheme**: The proposed scheme for modified model of the PV inverter system considering the sensor characteristics and Kalman filter estimator.

sensor characteristics. The sensitivity of non-linear pickup resistance Hall element is also a function of internal resistance voltage, temperature and magnetic flux density, which follows as (C.7):

$$R_{PU} = f(V,T) \times (1 + \alpha B^2) \tag{C.7}$$

where V shows the resistor internal voltage drop across the Hall element, T shows the sensor operating temperature, B is the magnetic flux density of the Hall element, and α is the empirical parameter, which depends on the sensor design [146]. Based on the manufacturer information since the coercivity of magnetic polarization has high impact on the sensor inaccuracy over the time [147], therefore we modeled only magnetic flux density changes in (C.8):

$$\Delta B = (1 - \beta\Delta V) \tag{C.8}$$

where as β is the calibrated device sensitivity, and ΔV shows the voltage across the applied unknown field and the zero Gauss [148]. The error model for aging of the Hall element is simplied as follows:

$$\Delta R_{PU} = f(\hat{B})_{V,T} \tag{C.9}$$

where $f(\hat{B})_{V,T}$ shows the sensitivity changes of the Hall element due to magnetic flux density variations, assuming the normalized temperature and voltage changes are negligible.

Since the electronics circuits for the calibration also have degradation over the time, the model for Silicon-based Integrated Circuits is proposed as here:

$$\Delta MTTF = R_0 exp(\frac{-E_a}{kT}) \tag{C.10}$$

where $\Delta MTTF$ represents the median time to failure for the Integrated Circuits, E_a is the activation of the energy for the Silicon, T is the operating temperature of the sensor, k is a Boltzmann constant, and R_0 is the constant values that will be derived empirically based on the device characteristics [149, 150].

By applying all the correlations from (C.6)-(C.10), the sensor characteristics are provided as:

$$V_S^* = V_S + (1 - |E_{abs}|_{10}) \times \Delta R_{PU}(t) \times \Delta MTTF(t) \tag{C.11}$$

where as V_S^* shows the modified sensor measurement output, $E_{abs}|_{10}$ shows the absolute error of the sensor with 10% white noise covariance, $\Delta R_{PU}(t)$ and $\Delta MTTF(t)$ are the error degradation of the sensor sensitivity over the time.

C.3.2 Filter compensation and SIRI performance

In this section, a Kalman filter algorithm is designed to increase the current sensing accuracy and consequently improve the system robustness. The Kalman filter estimates unknown mathematical parameters with limited measurements and speeds up the response to disturbances. The Kalman filter is mostly running an algorithm with the proposed model and calculating the residual differences. Fig. C.4 shows how the parameters for Kalman filter are formulated. While the algorithm is running, the convergence of developed system reaches to a constant value provided by measurements and system process. Then the recursive equations will be updated to achieve the proper output estimation. The space vector $\hat{x}$ represents the state transition of the model. The propagator A_k matrix shows the estimate of the state of the next time interval as $k+1$. Furthermore, the covariance matrix of the state estimation is called P_k, and Q_k is a normalized covariance matrix of sensor noise introduced by v_k. Here, R_k is a normalized covariance matrix of the measurement error, and state transitions should be updated based on the proposed recursive equations [151]. Table C.1 summarizes the parameter selections for system modeling and calibrations.

Table C.1: Selected parameter for model development

Items	Parameter	Values	Unit
1	E_a	0.7	$e.V$
2	α	0.1-0.3	
3	β	0.001-0.005	
4	T	323	K
5	k	1.38×10^{-23}	m^2Kg/s^2K

To quantify the impact of robust system operation, a single phase grid-tied PV inverter was modeled in MATLAB Simulink. Since robustness analysis is a statistical analysis and requires several operating conditions, it is not practical to perform the analysis on hardware setup. Therefore, simulation models verified by hardware testbeds in the nominal operating point and statistical analysis is also performed on

the validated simulation model. In an individual PV inverter, the input voltage of the inverter is stabilized by a DC capacitor. The inverter switches at 40kHz, and the output voltage is filtered out by an LC filter.

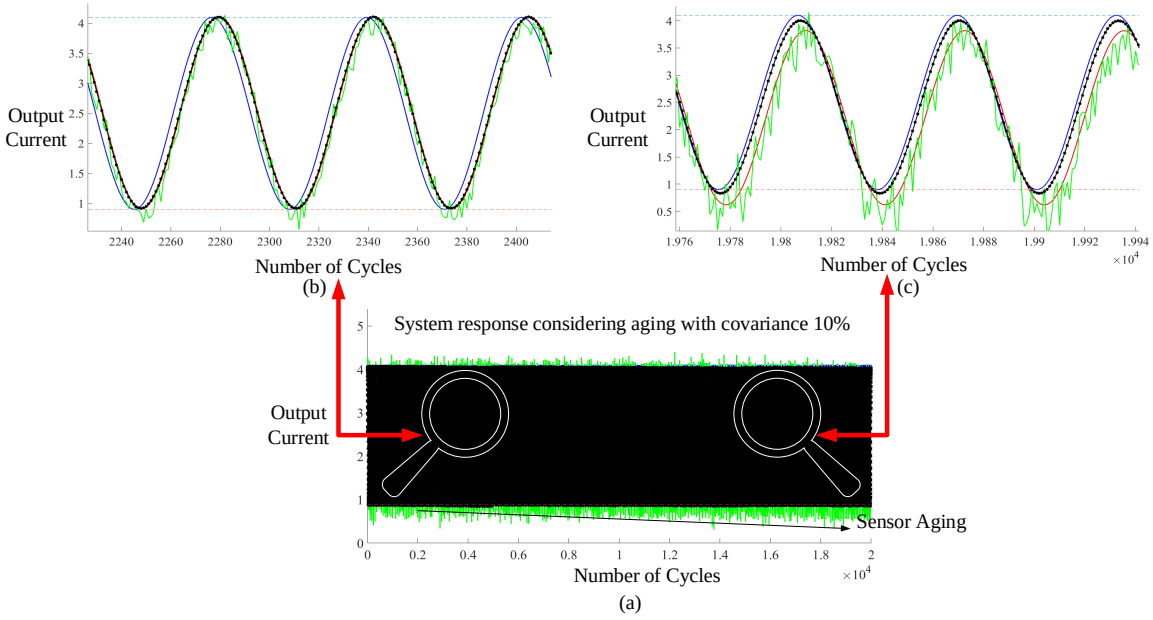


Figure C.5: **Simulation results**: The estimation results considered by a Kalman filter to the modified model of current sensor aging. The system response is modeled with 10% covariance error of the current sensor and shown based during the aging process. blue: ideal waveform, green: actual sensor measurement, red: system response correction with Kalman filter without aging considerations, black: system response correction with Kalman filter considering the aging process.

Table C.2 presents the impact of increasing current sensing inaccuracies on the robust operation of a single phase grid-tied PV inverter. As it shown in the table, increasing inaccuracies will reduce MPPT precision and system efficiency. This system operates in the robust region till 7% standard deviation, which is the boundary of robustness (Fig. C.5). For the inaccuracies more than 7%, the system enters in the non-robust region where SIRI sets on -1. Now by applying the sensor model degradation, the improvement can be achieved in the sensor response. The robustness analysis for system effectiveness performance was examined and the results presented

in Table C.3. The new results show the overall improvement in system robustness. The analysis also shows even though the system still enters the non-robust region, this happens for more severe sensor error around 11%, which is higher than the previous case.

Table C.2: Robustness comparison for single phase PV inverter under different current sensing inaccuracies without compensation

Standard Deviation	Efficiency	PF	THD	MPPT	SIRI
0%	98.23%	0.9996	1.30%	99.93%	0.4282
1%	97.13%	0.9997	1.37%	99.65%	0.1211
5%	96.90%	0.9994	1.40%	99.56%	0.096
7%	96.37%	0.9993	1.60%	99.12%	0.0237
8%	96.09%	0.9992	1.60%	98.95%	-1

Table C.3: Robustness comparison for single phase PV inverter under different current sensing inaccuracies with compensation

Standard Deviation	Efficiency	PF	THD	MPPT	SIRI
0%	98.23%	0.9996	1.30%	99.93%	0.4282
1%	98.00%	0.9997	1.37%	99.66%	0.1718
5%	97.68%	0.9994	1.40%	99.59%	0.1118
7%	97.33%	0.9993	1.60%	99.15%	0.0271
8%	96.95%	0.9992	1.60%	98.96%	0.0226
10%	95.85%	0.9989	1.65%	98.75%	0.0112
11%	95.37%	0.9989	1.66%	98.59%	-1

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