ENHANCED THERMALY MANAGED PACKAGING FOR III-NITRIDE LIGHT EMITTERS

by

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ABSTRACT

NICOLAS KUDSIEH. Enhanced thermally managed packaging Of III-nitride light emitters. (Under the direction of Dr. M. YASIN AKHTAR RAJA and Dr. MUHAMMAD KHIZAR)

In this Dissertation our work on ‘enhanced thermally managed packaging of high power semiconductor light sources for solid state lighting (SSL)’ is presented. The motivation of this research and development is to design thermally high stable cost-efficient packaging of single and multi-chip arrays of III-nitrides wide bandgap semiconductor light sources through mathematical modeling and simulations. Major issues linked with this technology are device overheating which causes serious degradation in their illumination intensity and decrease in the lifetime. In the introduction the basics of III-nitrides WBG semiconductor light emitters are presented along with necessary thermal management of high power cingulated and multi-chip LEDs and laser diodes. This work starts at chip level followed by its extension to fully packaged lighting modules and devices. Different III-nitride structures of multi-quantum well InGaN/GaN and AlGaN/GaN based LEDs and LDs were analyzed using advanced modeling and simulation for different packaging designs and high thermal conductivity materials. Study started with basic surface mounted devices using conventional packaging strategies and was concluded with the latest thermal management of chip-on-plate (COP) method. Newly discovered high thermal conductivity materials have also been incorporated for this work. Our study also presents the new approach of 2D heat spreaders using such materials for SSL and micro LED array packaging. Most of the work has been presented in international conferences proceedings and peer review journals. Some of the latest

work has also been submitted to well reputed international journals which are currently been reviewed for publication.

DEDICATION

This dissertation is not merely the result of one person's hard work. This dissertation was completed through the love and support of many unique individuals who gave everything to make this work a reality. I dedicate this Dissertation first to my aunt Souhila Kudsieh whom always had faith in me and spent her life pushing me in the right direction of knowledge. I also dedicate this work to my parents Salim & Fadia Kudsieh for all the love they gave and the hardships they endured to make this day come true. I also dedicate this dissertation to my guarding angles Farid & Mary-Jean Tranjan who helped me every step of the way to finish my studies and were my family for the last seven years. Mind always asks the how-questions, however only heart asks the why-questions. I found my answer in my love and life partner Elaine whose love and kindness were the final motivation in finishing this work. In all religions God knows everything, and I believe that we as humans are created to ask questions and seek answers. The more we know the closer to our creator we become so let us make knowledge be our stairs to heaven.

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CHAPTER 1: INTRODUCTION AND BACKGROUND

Photonic devices such as solid-state light emitters have gained tremendous attention over the last two decades for their unique features and commercial applications. Light Emitting Diodes (LEDs) and Laser Diodes (LDs) became very common in many applications enabling compact lighting, information transmission, storage, and flat-panel displays. Compact size and durability makes such devices ideal to be embedded in other systems or modules such as cell phones, computers, flat-panel TV screens and other displays [1]. Wide variety of semiconductor materials offer a broad spectral range of light emitters that meets the demand for many applications such as, data storage, chemical sensing, displays, traffic signals and of course the solar cells the inverse of the light-emitters. The growth of semiconductors light sources applications has increased their market share of the systems used in their fabrication as well. Millions of dollars are invested in such technologies; statisticians expect increasing demand on MOCVD systems that won't be even met before 2015 [2]. Additional systems such as wafers scribing and dicing, wafer level packaging, wire bonding, flip-chip bonding and thermal packaging equipment are also in high demand and keep increasing which reflects the growing production of LEDs/LDs modules and light engines in the consumer market.

1.1 Wide Bandgap Semiconductors As Light Emitters

III-V wide bandgap semiconductors have always been categorized as most suitable material system for light sources, which heavily depend on their energy-band

structures. Doped semiconductors have extra free charge carriers - electrons and holeswhich tend to exist in the lower more stable energy states in thermal equilibrium [3]. Two main energy levels involved in light emission process, are conduction- and valence-bands. In thermal equilibrium the free-electrons will be at the bottom of the conduction-band and holes will be at the top of the valence-band. Suitable electron excitation/injection will cause electrons to jump across the bandgap up to the lower states of the conduction–band. After a series of relaxation transits within the conduction band [4], electrons will end up in the bottom of the conduction band. Light is emitted when an electron drops from the bottom of the conduction-band to fill a hole in the top of the valance-band, this process releases amount of energy equal to the bandgap in the form of electro-magnetic waves (photons) with energy

$$E = h \times \nu \qquad 1.1$$

where ν is the frequency of the emitted photon.

Semiconductors materials that have the conduction-band minimum states and valence-band maximum states corresponding to the same value electron momentum (wave-number/k vector) are called direct bandgap materials while semiconductors that have the former values of minima and maxima corresponding to different momentum values are called indirect bandgap materials [5]. It was found that direct bandgap materials are efficient photon emitters because the process of absorbing and emitting energy satisfies the conservation momentum and energy principles without the need of any extra momentum changes and would make photon emission process a higher probability [3]. As for indirect bandgap such as Silicon, extra momentum is needed to

satisfy the conservation laws and that is achieved by emitting or absorbing phonons, this results in more relaxation time of the electron in the conduction-band and decrease the probability of photon emission thus all semiconductor light sources uses direct bandgap materials. Figures 1.1 and 1.2 shows the part of band structure of both direct and indirect bandgap semiconductor materials, respectively [3]

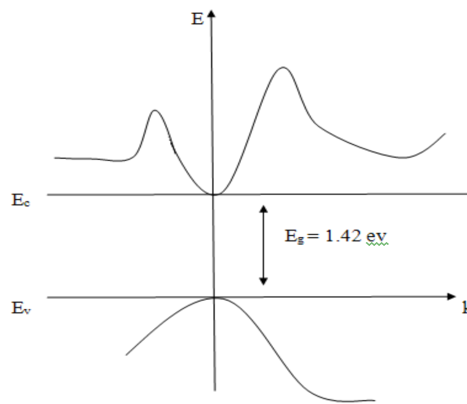


Figure 1.1: Direct bandgap structure in GaAs [3]

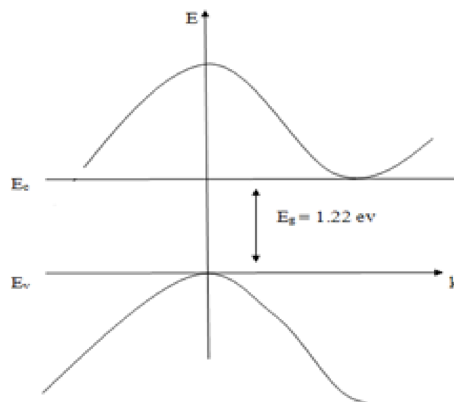


Figure 1.2: Indirect bandgap structure in Si [3]

Elemental semiconductors provide limited selection of wavelengths due to their inherent energy band structures, in addition to the fact that most of them are indirect bandgap materials. For the indirect bandgap, semiconductors the momentum vectors of holes in the maxima of valence-bands and K_e of electrons in the minima of conduction bands are different. Therefore, the momentum conservation requires phonon emission this affects the radiative recombination lifetime and rate and makes photon emission process less probable [6]. On the other hand compound semiconductors such as binary III-V like GaAs or GaN as well as several II-VI semiconductors have their minima of conduction and maxima of valence bands match as K=0. Thus, they readily satisfy momentum conservation along with energy conservation for recombining carriers (electrons- holes) and resulting photons [4]. These compound semiconductors provide a wide range wavelength selection. Table 1.1 shows some compound semiconductor materials and their bandgap and the accompanied emission wavelengths.

Table 1.1: Common semiconductor compounds bandgap and emission wavelengths [3]

Material	Bandgap type	Bandgap energy (eV)	Bandgap emission wavelength (nm)
GaN	D	3.39	366
GaP	I	2.26	549
GaAs	D	1.42	873
GaSb	D	0.73	1700
AlAs	I	2.16	574

1.2 Bandgap Engineering of WBG Semiconductor Emitter Structures

Conceptually, semiconductor light sources are made by combining two high-quality thin layers of p- and n- doped direct bandgap semiconductor materials together on an appropriate substrate. Metallic electrodes are added to the structure for applying a suitable forward voltage to inject current. Driving voltage injects the free electrons from the n-side towards the p-side while pushing holes from the opposite direction so that excitons (e-h pairs) are formed in the junction region [6]. Light is generated when electrons and holes combine radiatively. In other words, when electrons fall from the bottom of the conduction-band to fill a hole at the top of the valence-band photons are emitted. Wavelength of the emitted light is dependent on the bandgap of the material. Intensity of the emitted light is dependent on the number of electron-hole pairs that recombine radiatively in the junction region. LEDs and LD devices are made of appropriate layers of semiconductor materials that are deposited on the suitable substrate using various techniques such as MBE (molecular beam epitaxy), MOCVD (metal-organic chemical vapor phase epitaxy), e-beam evaporation, and gas ions sputtering.

Most of the LEDs or LD structures are fabricated at thicknesses of several micrometers scale with internal layers of several nanometers thickness. Using photolithographic and etching process various LEDs and LDs dies are mass produced on relatively large area wafers with diameters from 0.5 to 6 inches. Metal contacts are then deposited on both p and n regions for current injection and then tested. For non-conducting substrates, the processed devices wafers must be etched to expose the n-layer of the device for probing/injecting current into the device. Individual devices are

obtained by slicing and dicing the wafers. Figure 1.3 below shows the basic structure and operation of a semiconductor light emitter.

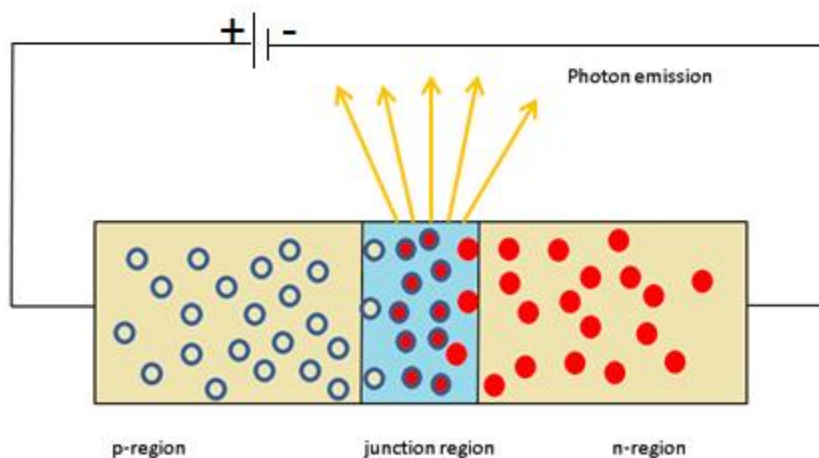


Figure 1.3: Basic structure of a LED device

The main parameter that determines the quality of a semiconductor light emitter is the internal quantum efficiency η, which is the ratio between radiative and non-radiative electron-hole recombinations. It can also be defined as the ratio between the number of photons emitted to the number of electrons excited to conduction band. The higher the internal quantum efficiency the better the device will be. Never the less, it is the external quantum efficiency that matters the most because it represents the light output of the device. It has been found that the external quantum efficiency is always smaller that

internal quantum efficiency due to many factors such as total internal reflection and diffraction limitations. Increasing external quantum efficiency is a major part of the device design and packaging process and it will be discussed thoroughly in the following chapters. .

Within the doped semiconductor material electron-hole recombinations have certain rates of occurrence per unit time, the total rate of these recombination include both radiative and non-radiative ones.

Considering the rate of radiative recombinations R_r and the rate for non-radiative recombination R_{nr}, the total rate of recombinations can be written as [3]:

$$R = R_r + R_{nr} \qquad 1.2$$

Based on the definition of internal quantum efficiency η is calculated as follows:

$$\eta = \frac{R_r}{R_r + R_{nr}} \qquad 1.3$$

Whereas, the internal quantum efficiency can also be written in terms of the lifetime of each type of recombinations. Considering the lifetime of radiative recombination is τ_r and the lifetime of non-radiative recombination is τ_{nr}, η can be expressed as:

$$\eta = \frac{\tau_{nr}}{\tau_r + \tau_{nr}} \qquad 1.4$$

Examining equation 1.4 it can be seen that for a semiconductor material to have high internal efficiency τ_r must be much smaller than τ_{nr}. In this case radiative recombinations will have much higher rate and overcome non-radiative recombinations.

This explains why indirect bandgap semiconductors are poor emitters, because the shape of the energy bands electrons has to pass several relaxation stages by emitting phonons this process will increase the lifetime for radiative recombinations therefore decrease the quantum efficiency. For example Si, which is an indirect bandgap material, has $\tau_r = 10$ ms while τ_{nr} = 100ns this results in Si have internal quantum efficiency of 10^{-5}.

Conserving high concentration of opposite charge carrier in the junction region is a very important factor to increase internal quantum efficiency however due to the forward biasing of such devices charge carrier may leak from the junction region to the opposite layer of the device where they are not desired and most likely to end up in nonradiative recombinations. Thus it is useful to keep the free carriers confined within the junction region. One of the common methods to achieve charge carrier confinement is the double heterojunction [4]. This technique is achieved sandwiching a smaller - usually p-doped- bandgap material between two opposite-doped larger bandgap material slabs, bandgap difference between the middle material and the side ones creates localized jumps in bandgap diagram, this discontinuity creates barrier that prevent selected charge carries form diffusing to undesired regions in a p-n junction type devices. This will also reduce the minority carrier current and increase the confinement of majority charge carrier in the junction region. Figure 1.4 shows the basic structure for p-p-n double heterojunction usually used in semiconductor light emitters. Figure 1.5 shows the energy bands diagram for such structure.

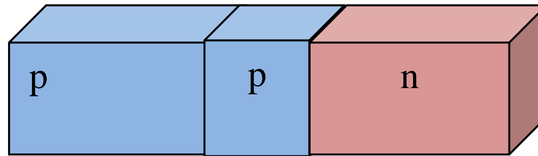


Figure 1.4: A Double p-n heterojunction structure

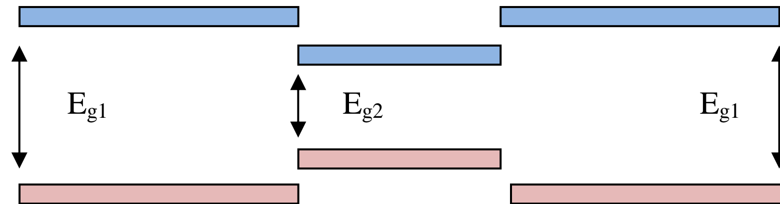


Figure 1.5: Energy band structure for a double heterojunction p-n device

The use of different bandgap semiconductor materials within the same device allows the selection of specific regions of the structure where light is absorbed. On the other hand, semiconductor materials with bandgap larger than the photon energy would be transparent and considered as window layers. Different bandgap energies will also give rise in refractive index difference; this difference can be used to create optical waveguides within the structure due to total internal reflection (TIR) [7].

The concept of confinement using double heterojunction was further improved by the introduction of quantum confinement structures. It was found that when the thickness

of the middle layer of a double heterojunction is compared or smaller than de Broglie wavelength of the thermal electron of the material. The energy of the electron residing in this layer has to be quantized and limited into specified levels. This creates much better confinement and also allows the selection of desired energy levels needed for the desired emission spectra (wavelength). Each electron will have three degrees of freedom (x,y,z), the introduction of quantum confinement structures will decrease these degrees of freedom accordingly. 1D confinement is achieved by creating quantum wells within the structure a thin enough layer(≤ 50 nm in the case of GaAs) by sandwiching it between two layers of a larger bandgap materials (barrier layers).

Figure 1.6 shows the energy bands diagram in a quantum well structure along with the allowed energy levels within the quantum well in a semiconductor material. The allowed energy levels of a particle of mass m confined in one dimensional infinitely deep quantum well is given as [4]:

$$E_n = \frac{n.h^2 \pi^2}{2md^2} \qquad n = 1,2,3,4,5, \ldots \qquad 1.5$$

Where h is Planck’s constant

m is the mass of the electron

d is the width of the quantum well

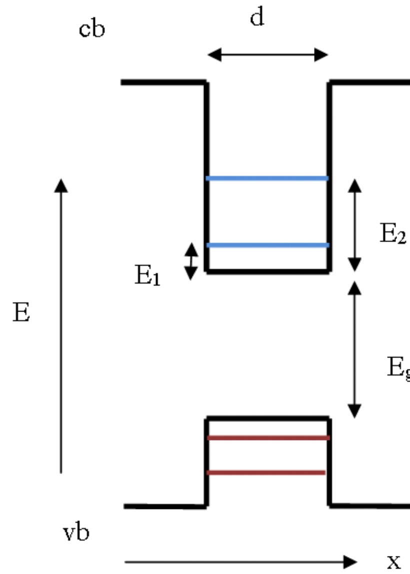


Figure 1.6: Energy levels diagram for one dimensional quantum well of semiconductor material

Considering the 1D case presented above it can be seen that electrons are only confined in the x-direction, so they should be treated as if they move in bulk semiconductor material in the (y,z) plane. The general electron energy-momentum equation in the conduction band of a bulk semiconductor is given as[4]:

$$E = E_C + \frac{h^2 k_1^2}{2m_c} + \frac{h^2 k_2^2}{2m_c} + \frac{h^2 k_3^2}{2m_c} \qquad 1.6$$

Where k_1, k_2, and k_3 represent the wave vector in x,y,z directions, respectively and E_c is the electron energy at the bottom of the conduction band. Considering the one dimensional quantum well case presented above the energy in the x direction is quantized and equation 6 can be written as [4]:

$$E = E_C + E_{nx} + \frac{h^2 k_2^2}{2m_c} + \frac{h^2 k_3^2}{2m_c} \qquad n= 1, 2, 3, 4, \qquad 1.7$$

Equation 1.7 shows that the x component of the electron energy is now limited to quantized values which mean that the motion of the electron in the x direction is also limited by the allowed values of k_1 which means confinement.

Further confinement can be achieved using different structures. For 2D confinement quantum wires are utilized where a thin wire of lower bandgap material is surrounded by a wider bandgap material if the wire was oriented in the z direction then electron energy components on both x and y will be quantized as presented in equation 5, electrons will move in the z direction as if they were moving in a bulk wire material. Figure 1.7 shows 3D structure of quantum wire.

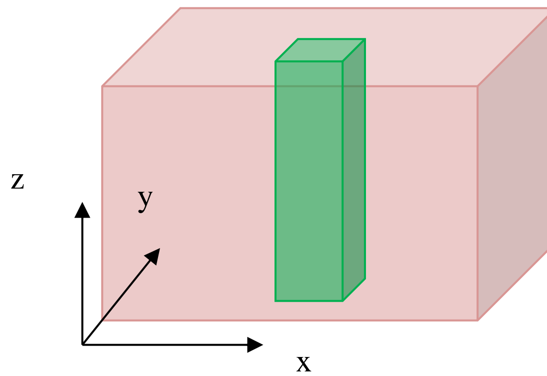


Figure 1.7: Basic quantum wire stretched in the z direction of semiconductor material

This type of 2D confinement changes the energy-momentum equation for electrons in the conduction band as follows [4]:

$$E = E_C + E_{nx} + E_{my} + \frac{h^2 k_3^2}{2m_c} \quad n,m = 1,2,3,4,\ldots \qquad 1.8$$

Carrier confinement can be extended to 3D by using Quantum dots, these structures composed of islands of low-bandgap semiconductor materials surrounded by higher-bandgap materials from all directions. The size if these dots should also be comparable to De Broglie wavelength cubed. Figure 1.8 illustrates the basic structure of a single quantum dot. In such structures the quantization of energy is achieved in all directions this would increase the selectivity of the desired energy levels involved in light emission and narrows the emission spectrum of the semiconductor light source.

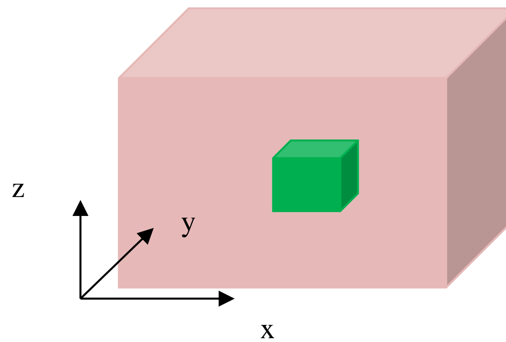


Figure 1.8: Basic quantum dot structure

Total energy of the electron in the conduction band is now fully quantized as can be seen in equation 1.9 below [4]:

$$E = E_C + E_{nx} + E_{my} + E_{lz} \qquad n,m,l =,1,2,3,4,\ldots.. \qquad 1.9$$

Although the basic structure of a LED or LD is a p-n junction, with a double heterojunction, or multi quantum wells (MQW), but there are many additional material layers needed to create efficient light emitters. Substrates and sometimes interface layers are needed to adjust the lattice during the growth process, while cladding layers are needed to control the charge carriers and emitted photon in the desired direction. Electron rich layers are also added above the junction layer in the direction of the p side of the device to act as electron blocking layer to decrease the flow of electrons out of the junction region and increase carrier confinement [4]. Metals are added as contact layers to provide suitable uniform driving current to operate the device. These layers are included in the device design depending on the type and application desired.

Various designs have been developed for solid state light emitters using the concepts presented above with different epi-layers structures to increase light emission, quantum efficiency, output intensity and directionality. Based on its planar wafer-grown structures, semiconductor light emitters fall into two main categories: surface (front/back)-emitters, and edge-emitters.

Surface-emitters are relatively the simpler of the two; they include an active region sandwiched between two opposite doped layers as depicted in figure 1.9. Thick substrate provides mechanical support and often as an n-type conductance, it is also used as a cathode for current injection into the device; suitable metal contacts are deposited on

the n-side substrate or entrenched by etching away epi layers to expose the n-region of the device. The p metal contacts (p-electrodes) are deposited on the top i.e., p-side surface of the device serving as anode [8].

As noted earlier, when the current is injected, the electrons flow in from n-side and "holes" flow in from the p-side and both type charge carries reach in the p-n junction region. Back emitters can have a simple double heterojunction as an active region or it can have single/multi quantum well structures. 2Light is generated in the active region by radiative recombination of excitons (electron-hole) pairs and emitted in all directions. The light output of such devices is collected from the top surface of the device (not covered by metal p contact). Emission pattern of such devices is suitable for general lighting purposes, because of the beam shape and divergence; these parameters can be controlled by some techniques that will be discussed further in this chapter.

Edge-emitters, on other hand, are relatively complicated in their internal structure because of the need to include additional layers for optical guidance (wave-guiding) and light confinement, these lower index layers along with the higher index active region act as a waveguide in which light is confined and directed to the edge of the device. Light output is collected form the edge of the active region. Light pattern emitted by edge emitters is different from that of surface emitters, the rectangular shape and small dimensions of the active region generate narrow, elliptical, diverging beams of light. The divergence and beam pattern are affected by the active region dimensions. The output of edge emitters has more directionality, thus they are not suitable for solid state lighting (SSL), but they are preferred in optical communications applications. Although this research is more directed toward SSL application, several edge emitters were modeled

and studied because of their important applications. Figure 1.10 shows the basic structure of an edge emitter device [9].

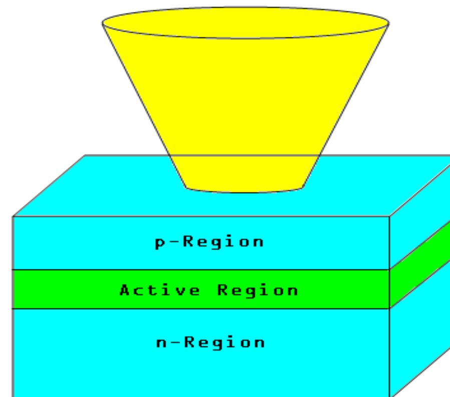


Figure 1.9: Basic structure of top emitter semiconductor light source

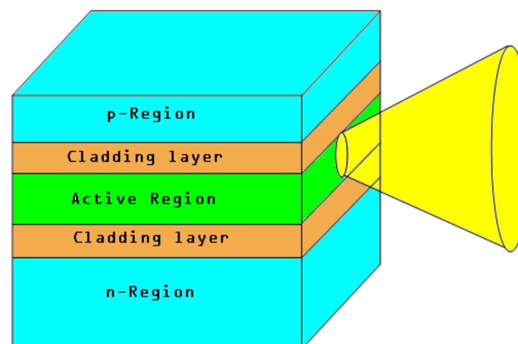


Figure 1.10: Basic structure of an edge-emitter semiconductor light source

Optical cavities can be added/embedded in both structures to provide optical feedback and therefore create a laser diode (LD). High refractive index contrast between semiconductor materials and air leads to high reflectivity on the interfaces. Thus laser diode die can be etched to create the optical cavity depending on the high reflectivity at both ends. This concept can be added to edge-emitters as in Fabry-Perot lasers and also to back emitters which create vertical cavity surface-emitting lasers (VCSELs) diodes [10]. The inclusion of multiple quantum wells (MQW) in laser diode structures enables obtaining very narrow band output due to the quantization of the energy levels at MQW region, and selective optical gain due to Fabry-Perot cavity. Additional technologies can also be added to the LD structure for such as Distributed Breagg Reflectors (DBR) or micro lenses and collimators.[11]

1.3 Device Packaging, Needs and Considerations

Semiconductor photon sources in both forms LEDs and LDs have great capabilities as electronic to photonic transducers; they also can perform inverse process as photodetectors. Semiconductor light sources are essential in many applications due to their high efficiency, durability, compact size, and high brightness along with low-cost. However, all of these devices are grown as thin layers (from nano and/or micro meter thicknesses) on substrate wafers by large numbers. The epitaxially grown wafers are processed by photolithography, variety of etching techniques and final metallization or contact deposition. On-wafer devices (on substrates) or diced chips are not useful for practical applications, as they are fragile small and very difficult to move or probe. For any practical applications, devices must be separated from the diced wafers and put into a form that will make them ready to be implemented in other systems and applications; this

process is called “Packaging”. Packaging is of a great importance because it gives the devices their final shape and size, with input leads for current/voltage supply, output windows for light-emission and sometimes micro optics for beam-shaping. Thus “optoelectronic packaging” determines the possible application of the devices and their modules.

A primary role of “packaging” of LED devices used in SSL is that it provides leads/terminals for voltage supply to the device to ensure suitable and easy current injection into chips by connecting to the power supply; and avoid any cut or shorting of the chip circuitry. This part of packaging have seen a lot of development from the traditional gold wires and contacts to the use of electrically conductive substrate materials, and flip-chip solder bump supported electrodes and ports [12].

As defined above internal quantum efficiency is the ratio of the photon emitted to the electrons injected into the active region. However, even with good internal quantum efficiency most of the generated light stays trapped inside the device. High index contrast between the semiconductor materials and air not only creates high reflectivity at the interfaces but also results in small critical angles at these interfaces which enhance total internal reflection at these interfaces. This effect is of concern for light emitters because it decreases the light output of the device. Light extraction is one of the most important aspects of the packaging process, considering that most of the commercial LEDs would typically have about 20 % external quantum efficiency.

Light extraction is enhanced by packaging through various methods, the most common most noticeable is encapsulation. Using transparent polymers the device is encapsulated by a dome that engulfs it creating intermediate index value between the chip

material and air, therefore decreases the reflectivity at the interfaces. Due to the lower index contrast between the polymer and air the value of the critical angle at this interface become larger, also the spherical or aspherical shape of the encapsulation decreases the probability of TIR (total internal reflection) to take place. Encapsulation became a standard procedure for LED/LD packaging process. Figure 1.11 shows the effect of encapsulation on light extraction efficiency of a back emitter LED device.

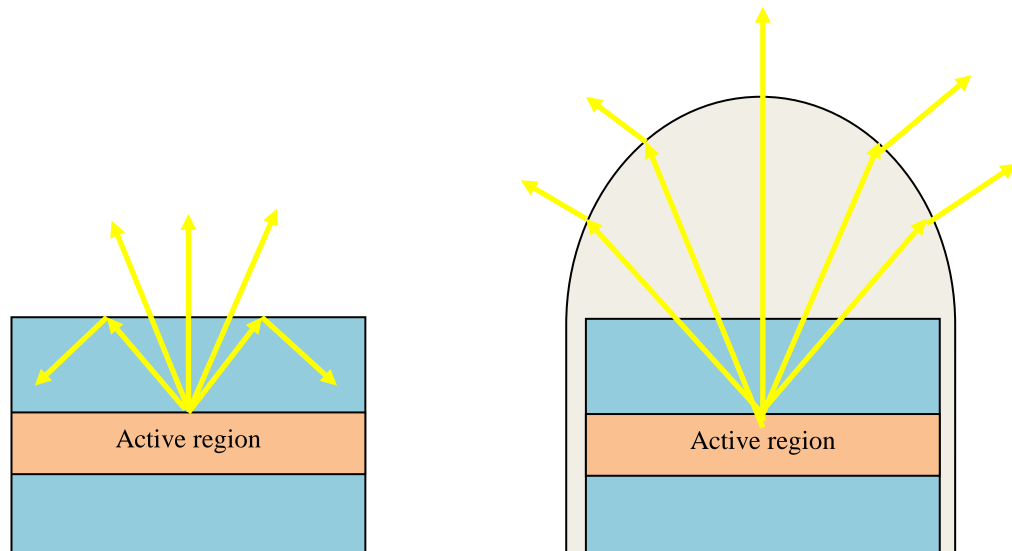


Figure 11: Encapsulation effects on light extraction efficiency for back emitter LED

Efficient light extraction should be always considered in any packaging design all packaging materials must be carefully selected to ensure a stable efficient output from the devices. Many designs and geometries have been introduced to increase light extraction

such as surface roughness and the inverted pyramids, and integrated Fresnel lenses. [13]

Based on the presented information above, it is evident that Packaging is the final stage of the fabrication process. Packaging dictates the final shape of the device and its performance and reliability; all high power LED packages must be designed to meet the following requirements:

1. control size of the device
2. ease of installation and maintenance
3. device protection and ease of handling
4. enhance performance and lifetime of the device
5. ensure high efficiency light extraction
6. ease of integration with electrical and optical components
7. Achieve thermal stability and long lifetime for the devices
8. low-cost and mass production capability

Like other electronic chips, there are two main methods for LED/LD packaging. Surface mounted device (SMD) and Flip-Chip mounted devices.

1.4 Surface Mounted Devices (SMD)

In SMD packaging, chip package comprises a supporting block with electric circuit patterns and at least one LED/LD attached to the supporting block. Circuit patterns of holes/vias, insulating layers, and conducting traces/pads are formed on and in the supporting block. SMD type LED/LD packages can be further assembled in groups and arrays to form a light modules that allow emitted light to travel in parallel with the mounting surfaces (in case on edge-emitters). The SMD manufacturing process is a

mature production process and thus easy for mass production with relatively low cost. Figure 1.12 shows the diagram of a typical SMD packaged LED. The use of this method is growing nowadays as vertical chip LED and VCSELs become more common. This method is preferred for low current density applications, and has low packaging density in unit area due to metal leads stands for power supply. New device designs such as vertical LEDs and new substrate materials have given SMD the ability of high power operation using conductive substrate. In these cases SMD allows the use of conductive substrate (SiC, Si, metals) which have very useful thermal, structural and economical properties. [14]

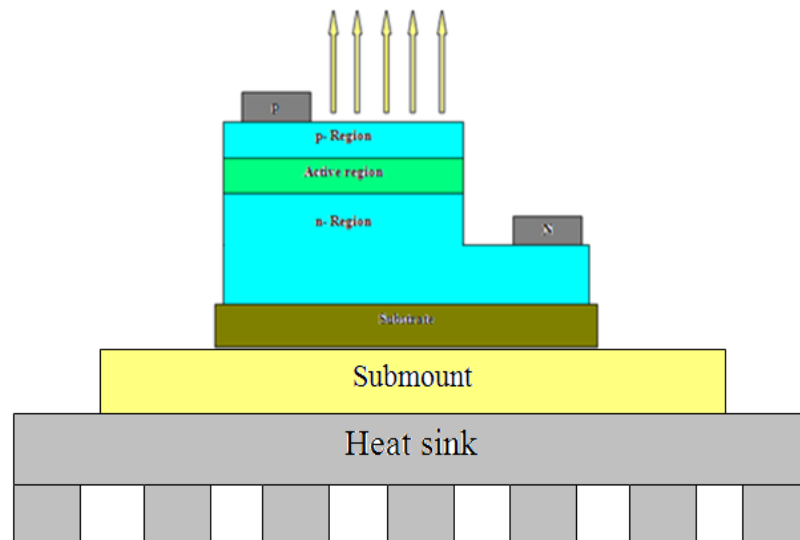


Figure 1.12: (SMD) surface mounted device LED

1.6 Flip-Chip Devices (FCD)

Flip-chip concept is based on the idea of fixing the LED/LD chip upside down on the supporting submount with the probing electrode attached by solder bumps underneath it. The LED/LD chips must have both p and n electrodes on the same side, epi-layers must be etched using various techniques in order to expose/reach the n-side of the chip. Using appropriate thermal interfacial materials (TIM/solders) the chips are connected to the two electrodes properly for forward biasing and current injection. For surface/back emitters most of the light is emitted from the back of the chip through the insulating/transparent substrate, and that makes Flip-Chip a more suitable packaging option for such devices. Probing metallization is patterned on the substrate and bumps (planner or stud types) are deposited at the intended locations of the devices. This method achieves the maximum device density per unit area. Figure 1.13 shows the basic diagrams of Flip-Chip for surface emitting devices. [15]

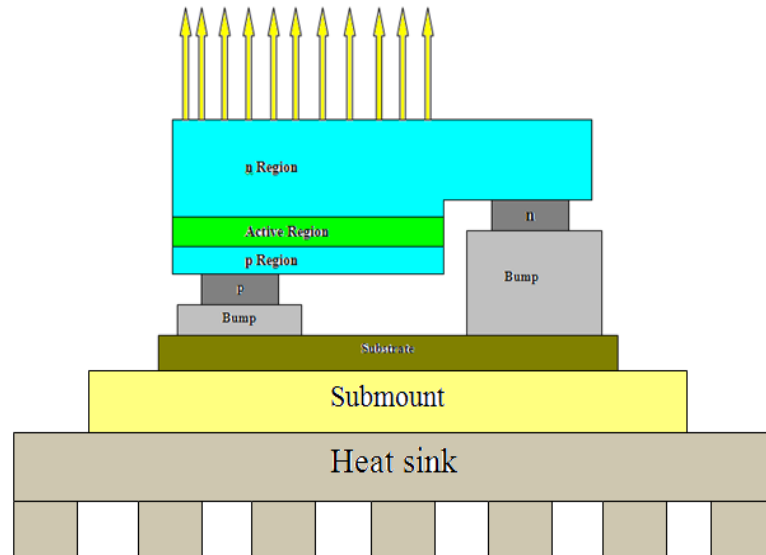


Figure 1.13: Flip-Chip packaged LED schematic

Intended applications and chip materials dictate the size and method of packaging. Packaging is concerned of many aspects of the device performance and light extraction is one of the top priorities of any package design. Small area, non-transparent metallization pads, and total internal reflection (TIR) results in most of the light produced by the device being trapped within the chip itself. An optimized and suitable package will always ensure low resistance current input with a maximum light output. This is usually done by final encapsulation which is the final stage of packaging to decrease the effects of TIR. Reflecting cups are also considered in some packages to direct the emitted light to a desired direction. Fiber-optic ports and micro lenses are also added in some cases to maximize coupling of the emitted light into an optical system.

Great expansion in the use of semiconductors light sources and the advent of replacing conventional lighting with solid state lighting requires that large number of

semiconductors emitters are to be produced and arranged in arrays on industrial levels. This process reveals lot of challenges regarding the efficiency, ease of fabrication, power consumption, and cost of these devices. Packaging development is an essential part to overcome these challenges and ensure efficient, cost-effective, and power-saving light sources for the future.

This research is aimed on the development of numerical and simulations models to design and evaluate efficient and low-cost packaging techniques. This is for the applications in high power LEDs for solid state lighting and with a focus to improve thermal stability and life-time of point light sources and related devices. This study starts at chip scale level, packaging material selection and comparative performance analysis, fully packaged device modeling and simulations. It expands to include heatsinks' design and cost optimization, and thermal analysis of high power LED assemblies and arrays, and finally the use of newly discovered nano-structures in the packaging of high power micro LED arrays. This work will help industry's increasing demands and to ensure more marketable and appealing lighting modules and light engines to consumers worldwide.

1.7 Heat Effects on High Power LED Devices

Generated heat in high-power LEDs and subsequent chip-packaging with efficient thermal management are the main focus of this work. Solid state lighting requires high performance, thermally stable low cost devices with improved lifetime, spectral stability, and device durability are needed to ensure good quality SSL modules. Beside the traditional issues of light extraction and internal quantum efficiency, thermal stability is one of the most important concerns when designing packaging of high power LEDs. Typically, low internal quantum efficiency means that the majority of the electron-hole

pairs in the active region will recombine non-radiatively. The non-radiative energy loss and extra energy of the electron-hole pairs beyond the band-edge transitions is released in the lattice as phonons which are quantized vibrations and deposits excess energy in such devices. This process results in increasing the device temperature and decrease of quantum efficiency [16]. In addition to this intrinsic problem, epi-layers growth processes contain high level of defects especially for III-Nitride wide bandgap structures . Defects and micro cracks create discontinuities in the lattice and become electron traps that keep excited electrons localized in the same vicinity, eventually these electrons release their extra energy as phonons thus increase the device temperature. All these effects take place as injected current flow across the epi layers of the device, also various epi-layers of semiconductor have intrinsic resistance which also causes Joule-heating The device heating due to Joule effect, non-radiative energy loss, and internal quantum efficiency loss all add up to overall thermal effects .

Considering that in typical LED devices about 20% of the electric energy is converted to light; it is evident that driving current produces a considerable amount of thermal energy that is dissipated within the LED epi-structure. This phenomenon is more dominant for high power LEDs considering the higher driving current used and more heat deposited in a small volume. Heat generated within LED structures can have serious effects on the device performance. Ultimately, this has negative impact on both the optical output power, color temperatures, color rendering index, color purity and the spectral properties of the emitted light.[17-18]

Figure 14 illustrates the drop in the output light intensity for a typical InGaN/GaN LD for different thermal management packages (different chip temperatures), a close

look at figure 1.14 shows the importance of packaging quality for the device performance, and output intensity. High quality materials achieve good thermal management and keep the chip junction temperature at suitable levels so the output is at maxima. Poor selection of packaging materials leads to thermally unstable light sources that suffer self-heating which results in compromised output intensity and poor lifetime. It has been found that a careful selection of the packaging design and thermal interfacial materials play critical role to create thermally managed light sources of high optical power densities with improved lifetimes. [19]

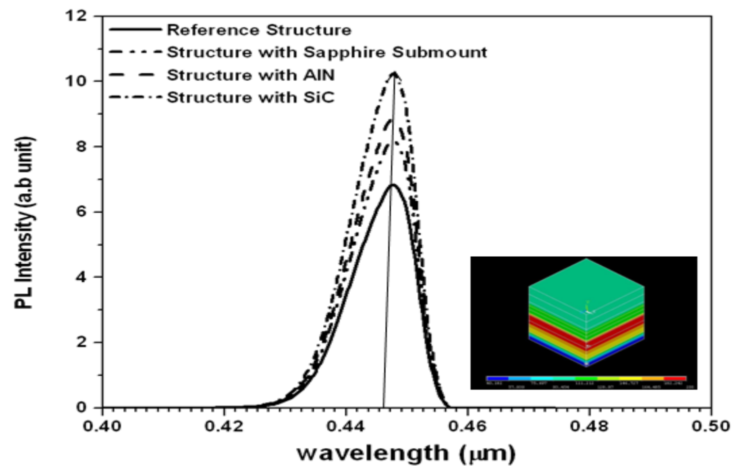


Figure 14: PL spectra of the MQWs InGaN/GaN LD structure after connected to different submounts [19]

On the other hand, this unwanted heat also affects the energy bands of the semiconductor device narrowing the bandgap which leads to red-shifts in the emitted light, and creates unexpected undesired wavelengths at the output spectrum. This will result in scattering electrons at deeper levels in the valance and conduction bands and gives rise to unexpected energy levels transactions of longer wavelengths [20]. Figure 1.15 shows the PL spectra for AlGaN/GaN LED at different temperatures with a 25 nm red shift and 50% drop in the optical output intensity was observed. Such redshift might be acceptable in some application such as SSL, but it can't be tolerated in other applications such as optical communication and some medical application. The large drop in output is not acceptable for any type of applications, especially SSL where multiple devices are assembled together to create high output.

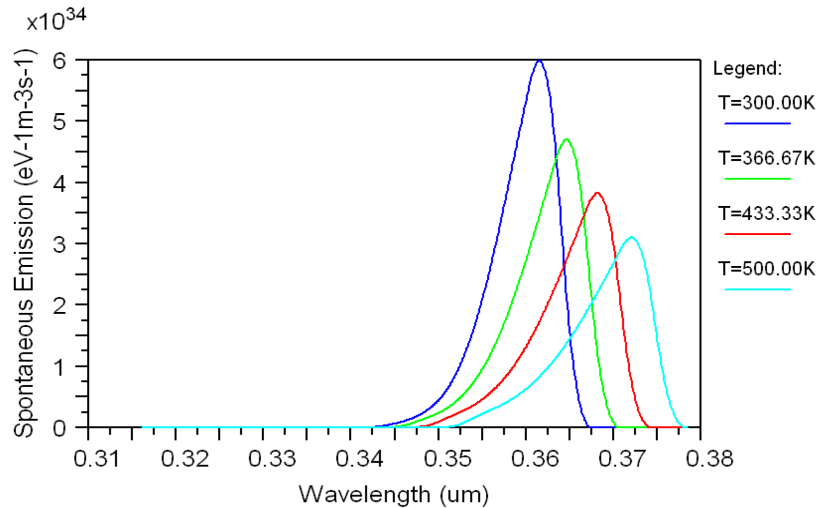


Figure 1.15: PL spectrum for AlGaN/GaN LED device at different chip temperatures

It has been observed that the decrease in the optical output intensity and red-shift in the emission spectra are the immediate impact of the generated heat within the junction layer of the device structures. Also, this heat also causes serious effects on the overall performance of these light sources. Where some of the stresses such as thermal stress and strain might cause serious degradation effects and ultimately results to a catastrophic failure of such devices [21]

In order to replace conventional incandescent light bulbs with solid state light sources such as high power LEDs, the later have to operate at the same color temperatures and should have equivalent or better color rendering index, color purity and optical power densities. Semiconductor light sources are suitable for SSL due to their compact size and low energy consumption. Phosphors converted white light sources are needed for SSL, however single low power LED based packages may not be able to produce high illumination intensities. The answer to the first problem would be to mix the three basic colors (red, blue and green) by placing three different LEDs that emit these colors on the same chip to create white light. This method is expensive and complicated and does not meet mass production demands. The other method is to use short wavelength devices (blue to UV) to excite a phosphors slab. The short wavelength high energy photons emitted by these LEDs excite phosphors atoms which generate various other colors via photoluminescence. III-Nitride based LEDS/LDs have that desired emission spectrum which makes them essential for any SSL application, thus they were the devices of choice for this work [22].

As mentioned earlier, dissipation of the generated unwanted heat is a priority for any package design. Careful selection of package materials is essential to achieve thermal

stability of light sources. Many packaging techniques have been developed over the years. They vary depending on the devices of interest (edge emitter, back emitter). In brief, thermal management has two types, namely passive and active. Passive thermal management deals with package designs that are designed to extract heat away from the structure and dissipate it to the ambient efficiently; this includes submount materials, thermal interfacial materials selection and heatsink designs. Active thermal management is focused on cooling techniques for photonic devices such as fan attached heatsinks, cooling by air or liquid gel channels. Serious efforts and resources have been dedicated toward the development of wide bandgap semiconductor light emitters to meet the goal of converting these into high power light sources for solid state lighting. More efficient high-power devices are needed, and larger assemblies and arrays of devices are required in order to replace conventional light sources. All of these demands have to be met by low-cost solutions to increase the marketability of these devices and speed up the transition into SSL. The need for cost-efficient and effective thermal management became more imminent. Industry is always on the look for new packaging materials and techniques to answer the expanding needs for high performance durable devices. This study is aimed to develop packaging options for thermal stability that is both cost-efficient and effective

1.8 Summary

In this chapter, we have presented a short introduction and basic principles of semiconductor light sources. Important parameters such as internal and external quantum efficiency were defined. Techniques needed to enhance light output have also been discussed. Quantum confinement through different structural variations has been briefly

explained. Semiconductor light emitters have many applications ranging from general lighting to optical communication and chemical sensing. Different types of devices have been developed over the past decades to fit their intended applications. The two major categories of solid-state light emitters are surface emitters and edge emitters.

The methodology of growing these devices on wafer substrate materials makes the devices very hard to handle or use in any application. Optoelectronic Packaging is the answer for these problems. Well packaged devices can be easily handled, probed and implemented in other systems. Packaging is also responsible for the critical issues linked with the external quantum efficiency and the light extraction, since most of the emitted light in the devices is trapped within their structures. Major packaging trends (SMD and Flip-Chip) methods were presented above along with some common packaging materials. Challenges facing this technology are also considered, total internal reflection, light extraction, encapsulation were all defined and discussed.

The thermal behavior of semiconductor light sources was analyzed; self-heating causes and effects were identified and explained along with the external heat causes due to Joule effect. The impact of device temperature on its performance was illustrated. The drop of output intensity and the red-shift of the emission spectrum were also considered and briefly discussed.

Subsequent chapters describe the work that was carried out following the most recent discoveries in packaging techniques like chip on plate COP packaging in order to improve and evaluate new packaged designs. The newest high potential packaging materials (Carbon nano tubes, Graphene few atomic layers films) are also included and considered in our search for new packaging designs rather than the traditional methods

being tested lately. One of the key contributions of the research is the inclusion of detailed LED structures for the thermal management of photonic devices, contrary to treating the whole device as single bulk material. Because semiconductor materials thermal properties change considerably with doping levels, in most of our modeling and simulation all the layers of these structures are considered with all their different thermal properties extracted from recent literature.

The second chapter of this dissertation includes a brief description of the research especially for the modeling tools and thermal packaging techniques used. Chapters 3 and 4 show our work and results for thermal management of high power LEDs for their wafer bonding, flip-chip bonding, chip on plate type packaging and many more. . Chapter 5 presents the thermal analysis of fully packaged devices using new chip-on-plate (COP) technique, along with heatsink designs and related comparative studies. Chapter 6 presents a generalization of the obtained results and their implementation to multiple COP packaged LED assemblies and thermal stability analysis of n×m array. Chapter was concluded with a a new approach of using next generation of higher thermal conductivity smart structures such as Graphene as heat spreader material. Chapter 7 summarizes major findings and comprehensive conclusions.

CHAPTER 2: DESIGN TOOLS AND METHOD OF STUDY

The first section of this chapter describes the development and progress of the presented research, from the thermal behavior of on-wafer unpackaged LED/LDs to the complete thermal analysis of fully packaged multiple-chip assemblies. Packaging techniques and novel materials considered in this study are also mentioned.

The later sections present the modeling and simulation modules used for this work. Two well recognized commercial simulation packages such as Rsoft LaserMod^{TM} and ANSYS13^{TM} were employed for this study. This chapter deals with an overview of the physical and mathematical models used. Along with detailed illustration of used software's capabilities that makes these suitable for presented research.

The final section of this chapter is dedicated to the advanced mathematical modeling used to support the numerical simulation of the design SSL structures and devices and study was concluded with the comparative studies of the designed models. Furthermore, thermal resistance circuit model is explained in details along with all necessary mathematical equations and flow charts.

2.1 Research and Development

As summarized in the previous chapter, thermal management of light emitters is an essential technique to develop efficient dependable lighting modules and engines for solid state lighting (SSL). For the last few years, there has been growing industrial demand for better quality yet cost-efficient high power light sources. Lighting modules and engines packages and the related layer by layer high thermal conductivity interfacial

material layers are among the key factors responsible for efficient packages. This work was aimed to design and investigate thermal packaging for SSL through novel high thermal conductivity material designs using mathematical modeling and simulations followed by comparing the calculated results to that of the experimental models available in the literature.

This study deals with some of the critical issues linked with the thermal stability of light sources starting from the basic stages of on-substrate unpackaged chip scale dies to fully packaged arrays and assemblies of high power LEDs. Various light sources which were designed, developed and fabricated in our nanophotonics laboratory were studied, The obtained results were compared to some of the published results for comparison. Using Rsoft design simulator, Light-Current-Voltage (L-I-V) characteristics of the modeled devices were plotted to illustrate ideas about their emission spectra, optical power densities and their illumination intensities. Various die-attach techniques based on solder bumps were considered for comparative thermal analysis along with variety of submount materials. The obtained temperature profiles were used for comparison in order to determine the solder bumps design and the related submount material optimization.

As a next step, the study was extended with the selection of suitable thermal interfacial material (TIM) [34], submount and heatsink materials in modeling. For this, different material groups have been modeled based on their thermal properties in order to achieve best possible material combination for the trial packaging models of AlGaN/GaN LEDs. Consequently, several strategies were modeled and tested through transient thermal analyses. Temperature profiles along top-down and bottom-up

directions within the packages were plotted for comparison. After employing different strategies based on 'best and worst' performing material combinations, thermal resistance circuit concepts were employed to calculate the devices' junction temperatures (for the best and worst performing structure).

At this stage, our research focus was on heat dissipation through conduction. This was mainly because encapsulation and small side areas submounts made negligible heat dissipation through convection. From obtained results, temperature profiles for various structures cross-sections were plotted and compared to ensure results' reliability and consistency.

Group transient thermal analysis of 'thermal interfacial material' (TIM), submount and heatsink were also carried out in order to optimize the best suited materials combination for high thermal stability packaging [23]. In addition to classical thermal interfacial materials, some of the newly developed thermally highly conductive materials were also employed. The most suitable selected material combinations were optimized by considering both performance and cost.

It has been found that "On-Wafer" thermal management has several limitations in terms of device design and geometries which are strictly controlled by the intended usage and the desired wavelengths. Low thermal conductivity of LED die is typically dictated by the type of layer by layer epi-structures and the metallization material used for the fabrication LEDs for the targeted wavelength. Therefore, special care should be involved for the selection of the thermal interfacial material layers of the packages in order to ensure good heat dissipation from the junction/active region to the ambient [24].

As a next step, the worked carried out as described above was extended for

heatsink design optimization. Briefly, heatsinks are among few critical elements always considered responsible for the dissipating of unwanted heat away from the chip scale die to the ambient through natural forced convection. These are very important components and are specialty designed for packaging. Mainly, our research focus has been towards the design and optimizing of compact yet low cost heatsinks. Excellent performance heatsink always play a critical role for the thermal stability and durability of high power light emitting diodes especially when operated at higher injected current densities.

Quite recently, a new type of packaging technique of Chip-On-Plate (COP) has been introduced for the advanced thermal management of high power lighting emitting diodes [25]. In brief, metallic plates of relatively higher thermal conductivities are used as submounts. These are also important due to their excellent thermal properties and ease of form-factor and readiness of use. Efforts have been to explored and deploy such advanced technique for the modeling and simulation of highly compact light sources. During this study, different high power light sources were analyzed numerically using COP packaging strategy and a comparative study of the junction temperature at different operating power values was performed through steady-state thermal analysis. This is important for the performance evaluation of different COP packages. For this study, mathematical calculations were performed using a TRC model specifically developed for the designed and numerical optimization of these packages [26].

This is noticed worthy that at this stage, the convection was not considered negligible in our modeling. This was mainly because for this technique, heatsink dissipate heat to the ambient. During this study, several heatsink designs such as plate-fins, pin-fins, and staggered pins heatsinks were designed [27-28]. Later these heatsinks were

modeled and simulated using special finite element method to evaluate their performance especially when attached to high power LEDs. Modeling results were corroborated by mathematical TRC calculations, and later these were employed to ensure results consistency. Among few main drivers of this study has been to explore, design and simulate a low cost packaging strategy for high power light sources. It has been found that packaging cost play critical role when it comes to mass production and the marketability of high optical power density lighting sources, modules and light engines. It is often more cost-efficient to choose low-cost heatsinks that ensure temperature of the device remains within the acceptable limits, than to use expensive heatsink that will cool the device much lower than the accepted limits [25].

The ultimate goal of this work is to develop a low cost packaging strategy for the thermal management of milli-watt and higher optical power devices for SSL applications. The scope of this work is expanded from a cingulated to that of multi-array of chip scale LEDs for their low cost thermal analysis and packaging. For this, we employed COP packaging technique using cingulated and multi-chip LED assemblies to study the thermal behavior and stability of these lighting modules. Different assemblies were designed for variety of elements (devices) arrangements and types of symmetry. Results showed the thermal effects of neighboring devices upon each other, and these effects were predicted to create chip temperature difference among the assembly elements. The cause of this difference was analyzed qualitatively using TRC model and also heat diffusion equation [29]. Different arrangements to suppress the unequal temperature effect among elements were modeled and simulated at different power levels. This is worth noticed that the obtained results were in good agreement with the theoretical

expectations and symmetrical behavior of each element. As described earlier, unwanted heat removal is very important for a successful thermal package. For this, newly developed packaging strategy of Carbon nano-tubes based nano and micro structures have gained tremendous interest due to their exceptional electrical and thermal properties [30]. The experimental success in using few layer Graphene (FLG) as heat-spreading sheets for GaN field effect transistors (FET)s, has encouraged us to extend the same idea for the packaging of high power LEDs and LDs for SSL applications. A proof of concept structure was designed based on COP package, although the device and FLG sheets dimensions were too large, a small drop in the device temperature was noticed. heat-spreading sheet concept was then introduced to micro-LED arrays to overcome the size limitations and enhance the effect of FLG heat spreaders . The small size of such devices made these m comparable to the available Graphene sheets (about 10μ long), and gave place to much higher device temperature reduction. This work is noteworthy and we hope it is a promising start using Graphene heat spreaders for the packaging of photonic devices.

2.2 Modeling and Simulation Tools

This research is centered on simulations, and theoretical models and calculations. Two well recognized simulation softwares were employed in this study. Device design and simulations were carried out using RSoft's LaserMod™. 3D packaging modeling and steady-state/transient thermal analyses were carried out using ANSYS13™. Both softwares are primarily finite element FEM analyzers. LaserMod is a 1D/2D photonic devices design software for simulating optical, electronic and thermal properties semiconductor lasers and light emitting diodes and photonic structures. It allows the

design and simulations of variety of photonic devices such as LED, LD, VCSELs, and solar cells. Simulations of various packaging structures are based on Minilase-II program [31], developed at the University of Illinois, at Urbana-Champaign. The graphical user interface (GUI) features enable the users to control every layer within the photonic device's structures and optimize doping levels, bias and dimensions. The software solves the carrier transport, and carrier-photon interactions, using a fully coupled numerical model based on finite element method depending on the device geometry CAD design.

This tool is capable of simulating 1D cross-section, suitable for broad-area lasers analysis, also more complicated structure with higher mode confinement requires a 2D simulation of laser cross-sections. This is necessary when considering the effects of carrier spreading and optical confinement by the changing geometry of ridge waveguide structures. Various available features and capabilities of LaserMod make it suitable for Fabry-Perot edge emitters as well as basic LED devices and also other active photonics such as solar cells. Figure 2.1shows the sample GUI of Rsoft and LaserMod used in this study.

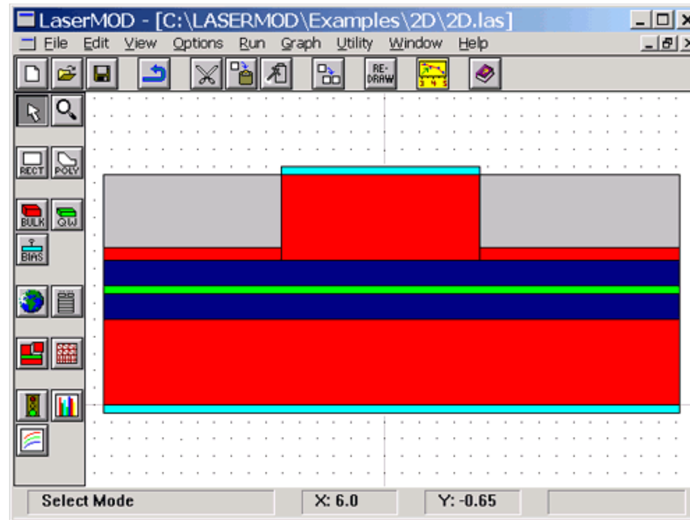


Figure 2.1: LaserMod GUI for CAD design of a 2D LD device.

LaserMod can provide steady-state analysis, for CW performance evaluation, in addition to transient analysis capabilities, for pulsed/modulated emission of devices. Various device performance plots, such as index / bandgap profiles, emission spectra, optical gain, and mode confinement can also be created. PL spectrum and optical gain can be simulated depending on carrier concentration and temperature which give the ability to observe and measure the effects of increasing temperature on the device's output. The software offers large material library to choose from with desired characteristics and combinations. Emission spectrum and modes pattern can be observed along with L-I-V characteristics. Figure 2.2 illustrates the L-I-V plots for a Fabry-Perot III-Nitride based LD.

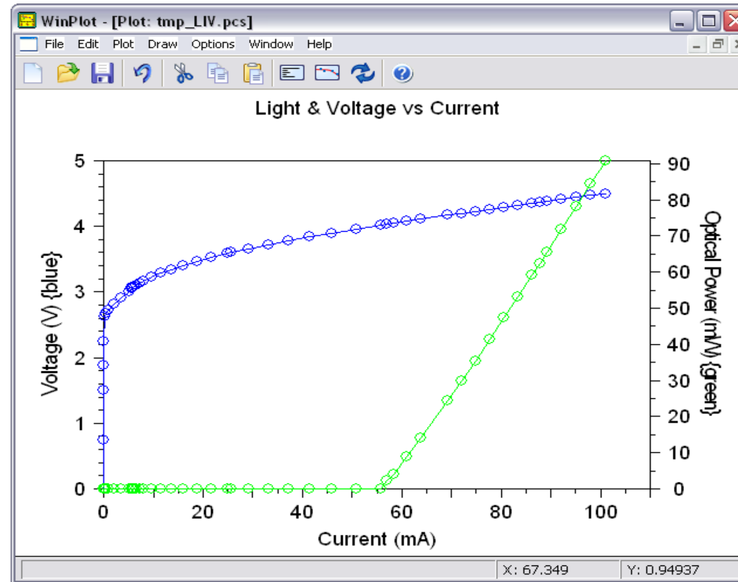


Figure 2.2: LaserMod L-I-V characteristics of a LD device.

Considering that the main focus of this dissertation is thermal management of photonic devices. Thermal analysis of such structures was our workhorse. In this research we carried out two types of thermal analysis, namely steady-state and transient. Steady-state thermal analysis is used to study the thermal behavior of systems when they reach thermal equilibrium and all thermal conditions in and around the structures become constant (steady-state) this type of thermal analysis was used in this research mainly to evaluate the thermal performance of complete packaged devices ie full LED package. On the other hand transient thermal analysis is used to study thermal behavior of systems at different points in time before reaching equilibrium where thermal boundary conditions are subject to changing overt time (transient), this type of thermal analysis was mainly used in comparative study among similar packaged designs that have different packaging

materials to clearly show thermal responses of different packaging material combinations. Thermal analysis of photonic devices was carried out using ANSYS™'13 engineering simulation program, which is finite element method based software [32]. ANSYS has excellent thermal analysis capabilities for both steady state and transient thermal behavior. Interface allows building 2D/3D models of the devices of interest to the appropriate scales. Any materials and their combinations could be modeled in the program based on its specific thermal and mechanical properties such as thermal conductivity, specific heat, and density. Specialty materials can also be modeled since ANSYS has the ability to include materials with anisotropic thermal and properties.

Once the model is built, thermal loads such as convection, heat generation, and initial temperature can be applied to desired volumes, areas, or even points of the structure. Convection is applied on the outer surfaces of the structure by inserting the suitable value for its coefficient; heat generation can be introduced for both areas and volumes depending on the type of the analysis (2D/3D). ANSYS heat generation function is related to the power dissipated in unit volume regardless of the source (electrical, chemical etc…).

Since ANSYS is a finite element analyzer, meshing is a very important step of any thermal analysis size and number of the elements has to be accounted for because each ANSYS can deal with limited number of elements at a time. Efficient selection of element sizes and mesh fineness at different location in the structure is essential to create the most realistic results [33]. ANSYS GUI is shown in figure 2.3 below as an example.

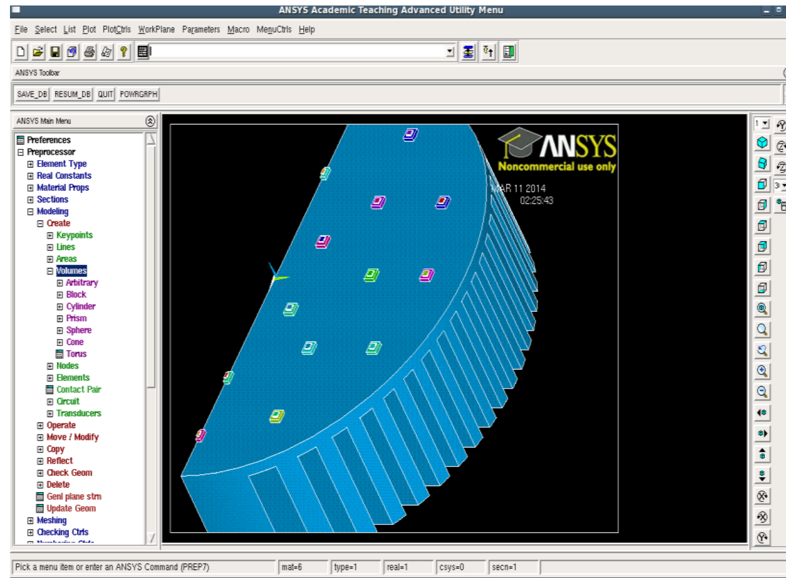


Figure 2.3: ANSYS13 GUI showing the design of 3D model of the package of multiple LED chips for SSL

ANSYS simulations are based on the first law of thermodynamics, which states that thermal energy is conserved. This law can be expressed as a differential equation of the form [34-35]:

$$\rho.C.\left(\frac{dT}{dt}+\vec{V}.\vec{\nabla}.T\right)+\vec{\nabla}.T.\vec{q}=\ddot{q} \qquad 2.1$$

Where: ρ is density, C is specific heat, T(x,y,z) is temperature, t is time, $\vec{V}$ is velocity vector of mass transport of heat, $\vec{q}$ is thermal flux vector, and $\ddot{q}$ is heat generation rate per unit volume.

Using Fourier law heat generation is related with thermal gradient and it can be expressed as:

$$\overrightarrow{q} = -[D]\vec{\nabla}.T \qquad 2.2$$

Where [D] is the thermal conductivity matrix and it is given as:

$$[D] = \begin{bmatrix} Kx & 0 & 0 \\ 0 & Ky & 0 \\ 0 & 0 & Kz \end{bmatrix} \qquad 2.3$$

K_x, K_y, K_z are thermal conductivity values for the material of interest. Combining equations 11 and 12 results in equation 13:

$$\rho.C.\left(\frac{dT}{dt} + \vec{V}.\vec{\nabla}.T\right) = -[D]\vec{\nabla}.T + \ddot{q} \qquad 2.4$$

Expanding equation 13 to more familiar form we get

$$\rho.C.\left(\frac{dT}{dt} + Vx\frac{dT}{dx} + Vy\frac{dT}{dy} + Vz\frac{dT}{dz}\right) =$$

$$\ddot{q} + \frac{d}{dx}\left(Kx\frac{dT}{dx}\right) + \frac{d}{dy}\left(Ky\frac{dT}{dy}\right) + \frac{d}{dz}\left(Kz\frac{dT}{dz}\right) \qquad 2.5$$

ANSYS uses finite element method (FEM) to solve the differential equations for obtaining the temperature at any time and any point of the structure after providing all loads and boundary conditions. Temperature distribution can be viewed at any point or anytime across the structure nodes localized temperature values can be obtained and

listed for every element of the model package and devices. Figure 2.4 shows temperature distribution in the package of high power LD device at the end of transient thermal analysis.

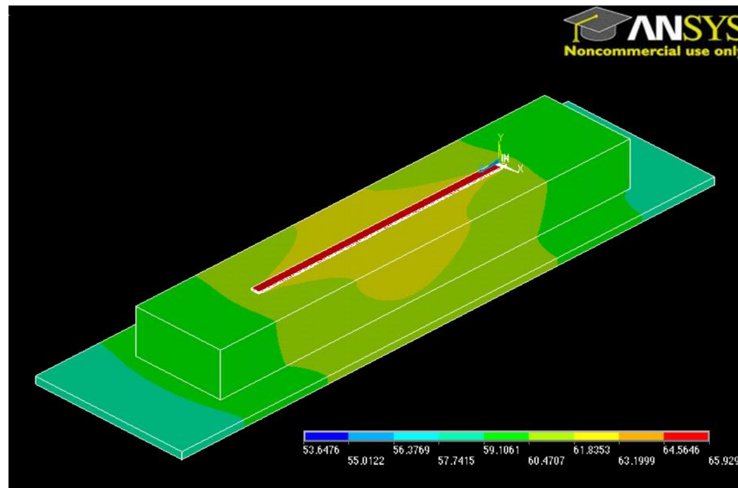


Figure 2.4: Temperature distribution in a packaged Laser Diode GaN/AlGaN Laser Diode.

Other thermal parameters such as thermal flux and thermal gradient can also be measured and plotted in a vector or contour plots of the 3D structure which is very helpful to understand the thermal behavior of the packages and view thermal paths within the structures. Path operations allow the users to define paths of several points throughout the structure and map any thermal parameter onto it in order to create parametric profiles. Animations of the results over time capabilities are also available to clearly show the

thermal behavior of the modelled packages. Figure 2.5 shows an example 3D vector plot of heat flux inside a fully packaged LED device. All features mentioned above made ANSYS-13 the tool of choice for all thermal analysis conducted in this research.

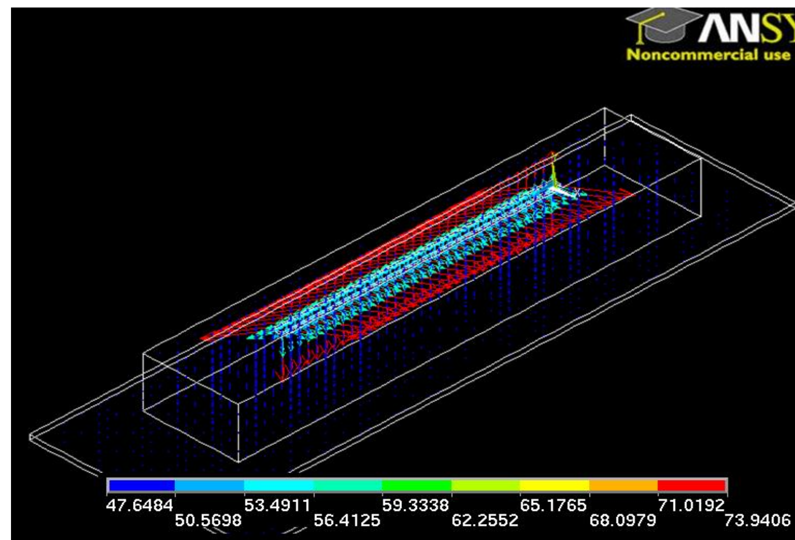


Figure 2.5: 3D vector plot of heat flux in a fully packaged LED chip mounted on heatsink.

2.3 Mathematical Model

Theoretical calculations are always considered very important for thermal mangement of chip-scale devices ; mathematical models were used to calculate some critical simulation parameters such as convection coefficients, heat generation functions, and junction temperature. Thermal resistence circuit (TRC) [26] is a mathematical model based on the analogy between thermal and electrical circuits. This model was modefied,

adapted, and employed in this study for calculating device junction temperatures. Thermal cuircuits are representation of device and packaging structures. Each different package would be represented by certain TRC diagram depending on its size, design and thermal path within the package.

Thermal resistance circuits used in our work contain only one component, which is thermal resistances. By definition theraml resistance is a thermal property of materials that represents the measurement of a temperature difference by which an object or material resist heat flow (heat per time unit or thermal resistance). Thermal resistance is highly size dependent. Each package and device layer contributes an independent thermal resistance to the total thermal resistance circuit.

Temperature difference between any two points is treated as potential difference; heat flow is the equivalent of electric current. In this sense calculating the temperature will be based on the simple Ohm's law for a given power value as:

$$P = \frac{\Delta T}{R_{th}} \qquad 2.6$$

Where P is the thermal flux (based on power dissipated) analogous to electric current "I", ΔT is the temperature difference between two points (just like potential difference), and R_{th} is the total thermal resistance between the two points. Knowing the power dissipated in the device packages and careful calculations of the total thermal resistance of the packages allows determining the device temperature considering that first point of interest is located within the active region and the second point is at the ambient.

Thermal resistances are treated as ‘Ohmic resistances’ in electric circuits; those can be connected in series or in parallel. Finding the total resistance similar rules apply as those in electrical circuits. It is important to identify and figure out when thermal resistances are in series or parallel. This is done based on tracing thermal paths in the structure, e.g., when there is only one thermal path through which heat flows/progresses in the structure, all thermal resistances of the material layers are considered to be in series as shown in figures 2.6 and 2.7, respectively.

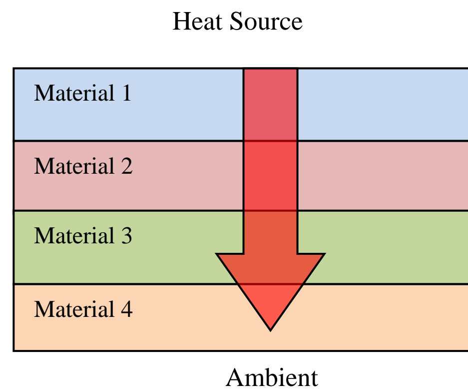


Figure 2.6: Thermal path in four-section stack of material layers

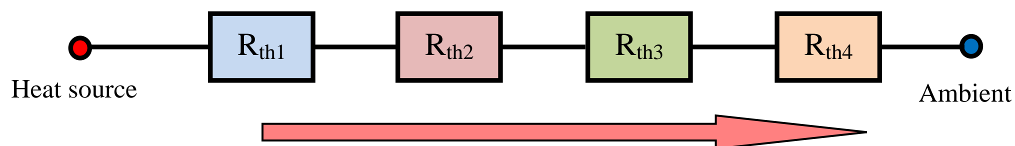


Figure 2.7: Series TRC diagram for one heat path through four-section stack of material layers

For more complicated thermal paths, thermal resistances can be found in parallel and series combinations. This often happens when thermal path branches out based on the structure or due to different material layers. In other words, when there are multiple thermal paths within the structure of interest, then thermal resistances can be modelled as combination of parallel and series. Figures 2.8 and 2.9 show an example of branching thermal paths and the thermal resistance circuit that represents it.

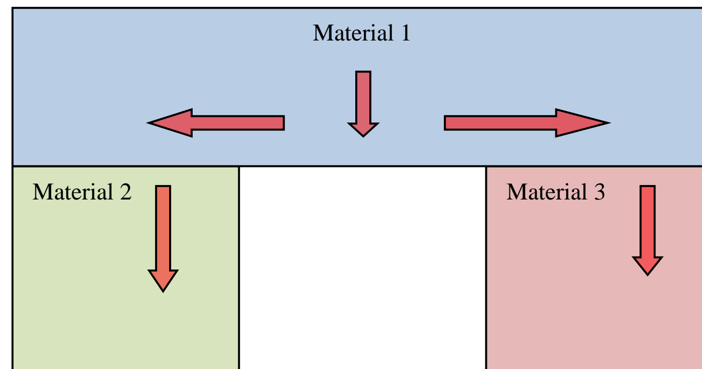


Figure 2.8: multiple thermal paths in gate-like arrangement of material layers

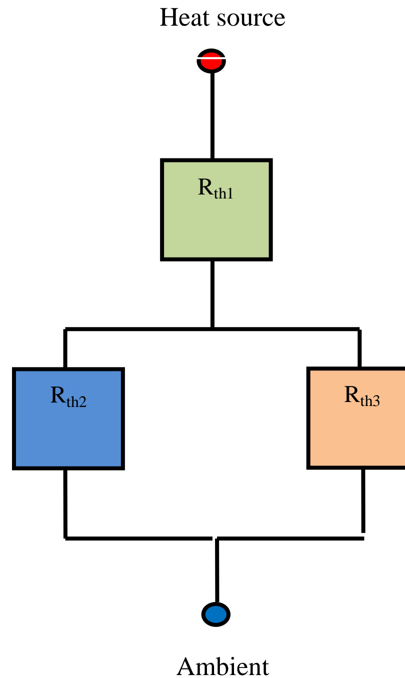


Figure 2.9: Parallel TRC diagram multiple heat path through bridge-like arrangement material layers

Thermal path definition is the first and most important step in TRC analysis approach. Once TRC diagrams are finalized, thermal resistances have to be evaluated in order to obtain the total thermal resistance of the structure.

Heat transfer occurs via three methods; conduction, convection, and radiation. Conduction takes place at the interfaces between solid objects thus in the case of solid-state light emitters it is the major method for heat transfer. Heat spreads from the active region to the other parts of the device mainly through conduction. However, thermal stability is achieved when the device temperature is relatively constant at a fixed operating power which requires a thermal equilibrium. Considering limited size of the

packaged device, it can be realized that heat is dissipated to the surrounding ambient to maintain that equilibrium. Heat transfer between solids and gases/fluids is achieved through convection. It this study, conduction and convection were only considered. Radiative heat transfer was not included in the analysis due to the small dimensions of the light emitting device surfaces; and thereby its small impact on the thermal behavior of the device.

As TRC diagram is defined, it is important to determine the nature of each thermal resistance. Conductive thermal resistances represent any thermal path within one material layer (solid material) such resistance values are calculated using the following equation:

$$R_{conductive} = \frac{L}{K \times A} \qquad 2.7$$

Where L is the length of the thermal path inside the material, K is the material thermal conductivity, and A the surface area perpendicular to the thermal path

‘Convective thermal resistances’ are located at every material/ambient interface. This includes the main thermal path, and the secondary paths branching out from it. Convective thermal resistances are calculated using the following equation:

$$R_{convective} = \frac{1}{h \times A} \qquad 2.8$$

Where h is the convection coefficient for material ambient interface.

After, all thermal resistance of the TRC are calculated, total thermal resistance is obtained using the basic rules of electrical resistors. When both ambient temperature and the dissipated power are known junction temperature can be easily found using Eq. 2.6

Each of the device packages are analyzed based on thier geometry and all thermal paths are considred taking into account conductive and convective thermal resistences. Chip temperatures are then calculated based on the power injected and the ambient temperature. In order to use this model effectivly many parameters have to be accounted for and thereby calculated. Convection coefficients , thermal resistances, and heatsink thermal resistance must be calculated for each fo the packaging design. Other theoretical concpts such as thermal mass and thermal diffusion are also employed to understand and justify the simulation results.

Theoretical results were put into comparison with the simulation data and the model proved to give staisfactory results. each different strucutre will be represented different thermal circuit which requier different calculations and thermal paths to be taken to consideration. This model was proved to give consistenent results with an acceptable error values.

2.4 Summary

In this chapter an overview of the research is presented, the methodolgy and aproach to the problem of self-heaing in semiconductor based lighgt sources were illustrated in a progressive manners from on-wafer unpackaged devices to fully packaged arrays. Conventional and new packaging techniques considered in this stduy were presented. Common and novel packaging materials included in this research were also

presented along with the modifications needed to include them effciently in the packaging process.

Simulation softwares employed in this research were presented, along with their mathematical base and useful capabilities that made them the workhorse for this study. Mathematical foundation of thermal resistance circuit model used in the study was presented along with the needed formulas and equations.

Next chapter presents the fisrt step of this research. A study of the thermal effects of bonding techniques is carried out for an on-wafer unpackaged LD device. Device structure and L-I-V characteristics are presented. Several bonding and submont materials are also introduced in a comparative fasion to clearly illustrate the best bonding design and submount material selection and their impact on the device outpt

CHAPTER 3 TRANSIENT THERMAL ANALYSIS OF InGaN/GaN LASER DIODES

Chapters 1 presented the concepts of solid-state light sources, their basic operation mechanisms and characteristics. Thermal effects on the devices output, spectral stability and lifetime were also discussed, in addition to common packaging types and materials. In chapter 2 research development and the approach for thermal management problem were presented along with the simulation softwares and mathematical model used. As suggested in chapter 2, in this chapter we investigate thermal management at the first level of the packaging process which is die attach on submount. III-Nitride LD device that we have developed was employed in this study. Two different die attach techniques were considered along with different submount materials. This part of the research is aiming to use modeling and simulation to find the best die attach method along with the best submount material options that will ensure sufficient heat dissipation from the junction layer to the heatsink creating more thermally stable devices.

3.1 Device Structure and Design

Solid-state lighting requires high power light emitting diodes (LED) / laser diodes (LD) devices in the blue to ultraviolet (UV) regions of the EM spectrum. GaN-based materials have attained major interest for visible to UV wavelengths LDs and LEDs. Since their emission spectral range is suitable for many applications such as chemical sensing, displays, traffic signals, backlighting displays, printers, and optoelectronic computer interconnects. However, the internal quantum efficiency and the thermal stability of such LDs/LEDs are pressing problems at room temperature. This is primarily

due to the activation of non-radiative recombinations, defects and high junction temperatures, which limit the output of these devices. As noted in previous chapters, high refractive index contrast at different levels of epitaxial structure, submount, and air gives rise to high reflectivity at the interfaces and decrease extraction efficiency [36]. Uncontrolled rise in the junction temperature results in a series of degradation effects on the device's performance. For example, due to high temperature, threshold current of LDs increase; at elevated lasing threshold current values, other serious problems such as low modal stability and output red-shift of lasing line are observed [37-38]. Therefore, transient thermal analysis and its careful study are critical for improved performance and better thermal stability As an example, a 2D design and simulation of the electro-optical characterization of InGaN/GaN MQW LD structure (with λ~445 nm) was carried out. Steady state thermal analysis, different packaging designs were also considered, analyzed and optimized. Thermal behavior of the LD chips was evaluated through numerical transient thermal analysis. Output power and threshold current of designed LD sources using vertical contact schemes were carefully analyzed and used as a reference for comparative study. L-I-V (Light-Current-Voltage) characteristics of various models were studies, and results were used to explore the impact of package materials on device performance. For the device in hand, MQWs were assumed to be square, and uncoupled but identical.

Rsoft LaserMod™ [31] was utilized to create a 2D model of the device, schematic of CAD design of an optimized LD structure is shown in figure 3.1. The proposed LD structures were based on Si-doped thick GaN substrate, consisting of an active region comprised of three ln_xGa_{1-x} N quantum wells (QWs) separated by four barriers. The

emission wavelength was controlled by adjusting the QWs composition *"x"* Some of the key parameters of other layers and general LDs design structure details are summarized in table 3.1. The optimization study was performed based on key assumptions, such as carrier transport in the heterostructures and electromagnetic wave-propagation in waveguide modes. Up to this point, unpackaged on-wafer devices are being modeled for its optoelectronic characteristics. Thermal behavior and Temperature distribution and package designs study would follow once the device's L-I-V results are obtained.

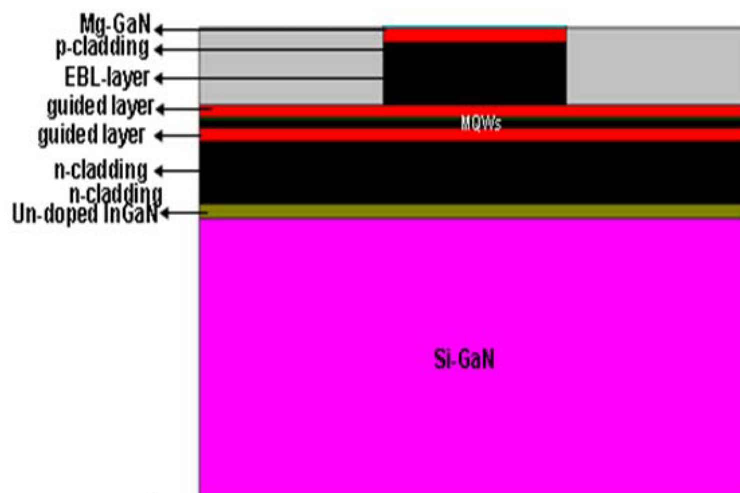


Figure 3.1: CAD design of MQWs InGaN/GaN LD

The TE and TM-modes modeling in waveguides is done using inherent birefringence in III-nitrides materials and Metallic electrodes on top of the LD structures. These are critical because the difference between the ordinary and extraordinary refractive indices is comparable with their variation across the heterostructures. Cladding

layers are added to the structure to create wave-guiding and support the modal stability [19]. For the reference structure modeling, no packaging layers were considered. As for transient thermal analysis, several fully packaged structures were modeled. Thermal distribution results were used as input parameters into the reference model to evaluate the impact of junction temperature on the output and emission spectrum of the LD device.

Table 3.1**:** Detail of layer by layer 445 nm LD structure [] use ref #

LAYER	MATERIAL	THICKNESS [nm]	DOPING [10^{18} cm^{-3}]
Submount	Sapphire, or AlN, or SiC	4500	--
p-electrode	Ni, Ag, Au	70	
Contact	GaN	30	79(Mg)
EB-Layer	$Al_{0.18}Ga_{0.82}N$	75	70(Mg)
p-Cladding	$Al_{0.17}Ga_{0.83}N$/GaN SL	150	75(Mg)
Waveguide	GaN	120	77(Mg)
Barrier	$In_{0.03}Ga_{0.97}N$	8.5	0
Quantum Well	$In_{0.14}Ga_{0.86}N$	4.0	0
Barrier	$In_{0.03}Ga_{0.97}N$	8.5	0
Quantum Well	$In_{0.14}Ga_{0.86}N$	4.0	0
Barrier	$In_{0.03}Ga_{0.97}N$	8.5	0
Guided Layer	GaN	100	5.7(Si)
n-Cladding	$Al_{0.15}Ga_{0.85}N$/GaN SL	500	1.9(Si)
n-doped Layer	$In_{0.05}Ga_{0.95}N$	200	5.5(Si)
Substrate	GaN	2500	5.5(Si)

3.2 Device Modeling and Simulation

The designed structure uses Si-doped GaN substrate followed by 200nm thick n-doped InGaN layer, 500nm n-doped AlGaN cladding layer, 100nm waveguide layer.

Next, an active region consisted of three $In_{0.14}Ga_{0.86}N$ multiple QWs sandwiched by four barriers. The structure was completed with a 120 nm thick p-guide layer, p-type cladding and $In_{0.2}Al_{0.8}$. Electron-blocking layers of 150nm and 75 nm, respectively, followed by a 20nm thick p-GaN contact layer. The epi-structure is shown in fig 3.1 The simulation was performed using Rsoft LaserMod™. The calculated refractive index profile and the optical intensity of the reference structure at laser axis are illustrated in figure 3.2.

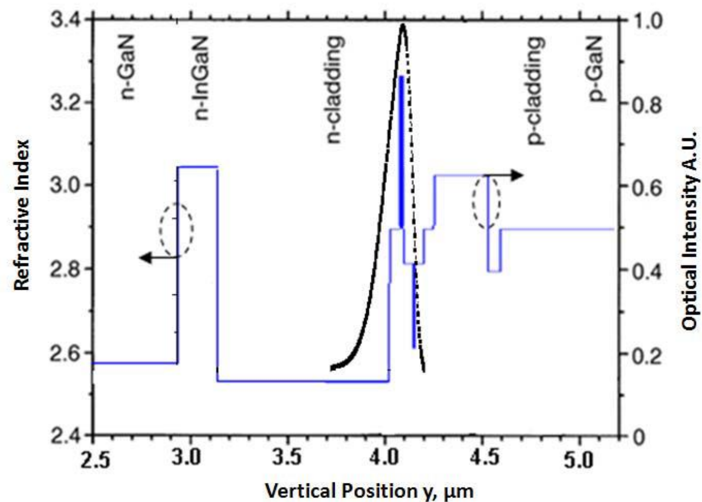


Figure 3.2: Profile of refractive index and optical intensity at laser axis.

Once the optimization of LD structures is accomplished, thermal analysis was carried out using FEM analyzer code ANSYS13™ in order to study the transient thermal response of the devices. For this task, 300×300 μm^2 LD mesa (3D) was modeled using the optimized reference structure. The proposed packaging structure includes fixing the LD chip on a submount layer for mechanical support and electrical biasing purposes. This

process is performed using metallic solder material. Considering flip-chip packaging model for the device, solder bumps are used to create contact areas on the submount. Planar and solder ball bumps packaging technique were employed to model different packaging designs, along with three submounts and thermal interfacial materials.

Standard metallic AuSn alloy was considered as the solder ball material. The selection of submount material plays an important role in the overall thermal management of the packages. Three different submounts materials were considered in this study, e.g., common Sapphire (Al_2O_3), SiC, and Diamond (C). Our thermal analysis used a systematic approach of evaluating heat dissipation for each of the different submount material for both planar as well as ball solder bumps structures. A comparative study of the results helps to determine the best bump design and submount material to achieve the best heat dissipation and ensure acceptable junction temperature to conserve modal and output stability.

Thermal analysis for the devices in transient as well as continuous-wave (CW) operation mode was carried out; the total operating time was set ~0.05 sec with an intermediate step of 0.00001 sec. The model was optimized such that the junction layer temperature would never exceed 200 ^{o}C; this would be needed to maintain realistic conditions to which fabricated devices are subjected. Thermal interfacial material such as Au metallization, AuSn soldering, diamond heat spreader pedestal, and Al heat sinks were used for the package. Adiabatic boundary conditions are set at the all sides. At 10 µs, the thermal diffusion length parameter for diamond is comparable with pedestal thickness (300 µm). This shows that Al heat sink has insignificant influence on temperature inside the GaN laser chip for operating times 10µs or shorter; thus it was not

considered in this study. The temperature distribution for a 300 × 300 μm^2 die designed using reference structure and planner contacts bumps under CW mode at 298K are shown in figure 3.3.

It is readily evident that for planar bumps heat spreading is uniform over the entire submount attached to the die through *p*-contacts side. Whereas, for similar die structure and dimensions, the temperature distributions in the submount for a solder-ball bumps are non-uniform as shown in figures 3.4 and 3.5.

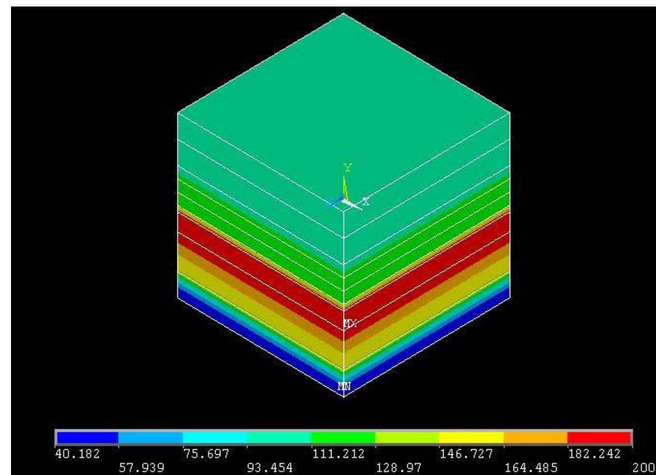


Figure 3.3: Temperature distribution of InGaN/GaN LDs with the die size of 300 × 300 μm^2 for submount with planner contacts (bumps).

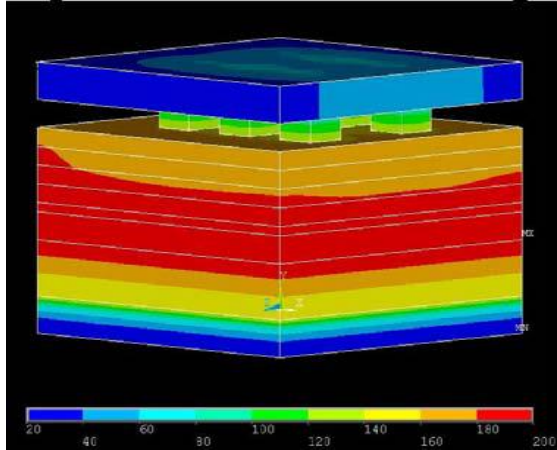


Figure 3.4: Temperature distribution of InGaN/GaN LDs with the mesa size of 300 × 300 μm^2 for submount with solder ball contacts (bumps)

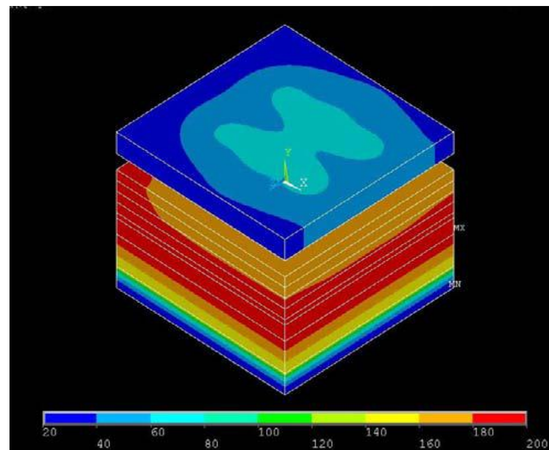


Figure 3.5: Top image of the temperature distribution of InGaN/GaN LDs with the mesa size of 300 × 300 μm^2 for submount with solder ball contacts (bumps)

For the case of solder ball bumps, localized islands of heat formed correspond to non-uniform heat distribution. However, for planner contacts, which can be produced either using electroplating or thermal evaporation [39]. The heat is spreading evenly without causing any non-uniformity. It is noteworthy that this study considers heat

removal via conduction only. Short operating time, small surfaces of the device and submount, in addition to the absence of heatsink, make heat dissipation through convection and radiation negligible. Convection effects and heatsink designs are considered in details in chapter 5 where thermal analysis is carried out for completely packaged devices.

3.3 Results and Discussion

At first, an emission spectrum and transient response of the optimized LD structure for 300 × 300 μm2 die (unpackaged) at different temperatures are evaluated. High die temperatures were used to show the drastic results of the device temperature on its output and spectral stability. It can be seen in figure 3.6 that a noticeable red-shift in the calculated spectrum and a drop in the output intensity were observed for corresponding increase in the temperature. This is caused by the self-heating of the structure, when operated at higher temperatures.

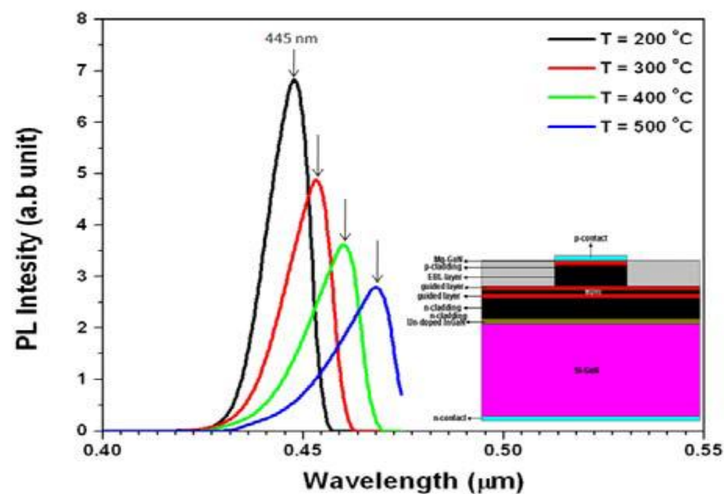


Figure 6: PL spectra of the MQWs based InGaN/GaN reference structure (non-packaged) at different temperatures.

Lasing modes and emission wavelength are dictated by the position of gain maximum in semiconductor material. Further, the threshold current density and slope efficiency are affected by the magnitude of gain and by the dependence of gain on the density of states and temperature. Whereas, phenomena's such as carrier-phonon and carrier-carrier scattering induces spectral broadening. It is noteworthy that wide quantum wells have ability of generating higher piezoelectric fields, therefore, more electrons and holes get separated by piezoelectric effect. This results in a decrease of optical gain and spontaneous emission. For simulations study, cavity length is ~500 μm, and the waveguide loss ~5 cm^{-1} were used.

The transient thermal analysis and the comparative study of the results were carried out by two stages. The first stage was to observe the temperature change in the submount over time for all the different structures that were modeled. Best performing design and material had more heat dissipation into the submount in shorter time; in other words, the structure with the highest submount temperature over the operating time would be the best thermally managed structure.

The second stage was to obtain temperature profile on a vertical path stretching from the junction layer to the submount at the end of the operating time and compare these profiles among all the structure modeled to select the best design and material for thermal management. Total of six structures along with the reference structure attached to submount using both planner and solder ball bumps package were modeled. $Al2O_3$, ceramic-AlN and SiC were used as submount materials. For the sake of comparison, similar thickness (~350 μm) was used for all submounts. The results of the first stage for both planar and ball solder bumps are presented figures 3.8 and 3.9. The dotted blue line

represents the temperature as function of time for a point in the submount when Al_2O_3 is used. The red dotted line shows the temperature rise in the submount over time when AlN is used. The black solid line represents the thermal response of submount when SiC is the material used. It can be seen that for both planar and solder bumps SiC heatsink will have the highest temperature which indicates better heat dissipation however it is important to notice the submount temperature values difference between planar and ball bumps structures. When SiC is used it can be seen that submount temperature reached 130 ^{o}C, for planar bumps whereas it reached 25 ^{o}C for ball bumps. Based on these findings its evident that planar bumps dissipated heat to the submount much better than the ball bumps did- up to 4 orders of magnitude.Stage-1 results showed consistency, it can be seen that for the case of Al2O_3 submount, heat conduction was poor in comparison to the other two submounts. However, on the other hand SiC showed much better performance compared to ceramic-AlN and Al_2O_3 submounts.

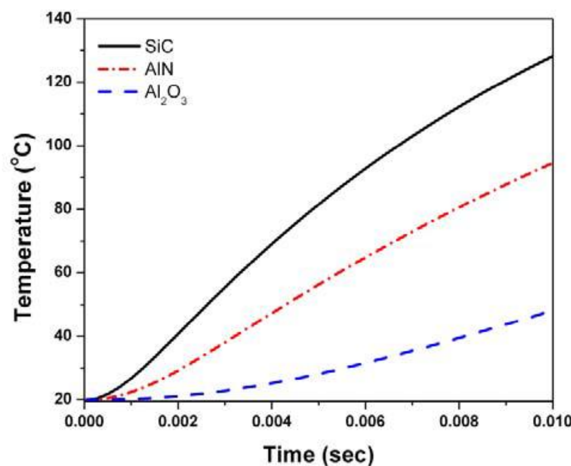


Figure 3.8: Transient response of SiC, ceramic-AlN and Al2O3 submounts for planner bumps packed LD.

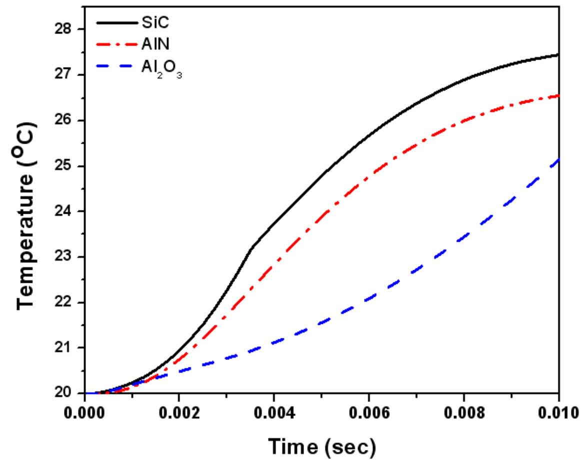


Figure 3.9: Transient response of SiC, ceramic-AlN and Al2O$_3$ submounts for solder ball bumps packed LD

The results of the second stage are shown in figures 3.10 and 3.11. Those show temperature profiles along a straight path from the junction layer to the bottom of the submount. Where the dashed and solid line represent temperature as a function of distance in microns from the junction layer to submount. the first segment of all temperature profiles - from 0.8 to 0.85 μm - shows temperature change within the LD structure thus the three profiles seems almost identical, however differences arise when heat reach the submount region due to different thermal properties between submount materials. By examining the results it can be seen that planar bumps and SiC submounts resulted in the highest dissipation for the LD package.

Results of the stages 1 and 2 came in agreement. Almost similar response was observed for solder ball bumps package. For the two cases, planner and solder bumps, SiC out performed in dissipating heat out compared to its other two counterparts. This is attributed due to the higher thermal conductivity and less material lattice mismatch.

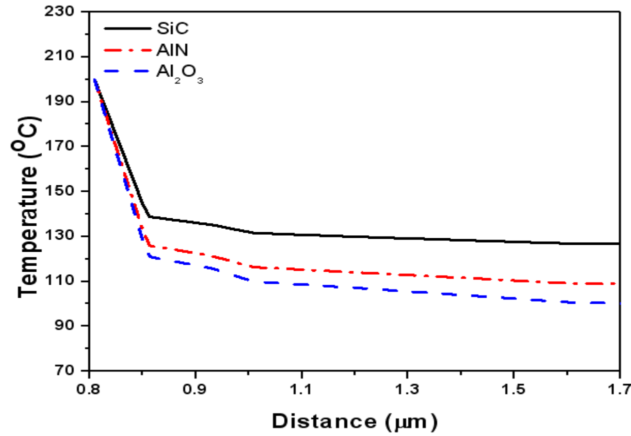


Figure 3.10: Heat dissipation of SiC, ceramic-AlN and Al2O3 for planner packed LD

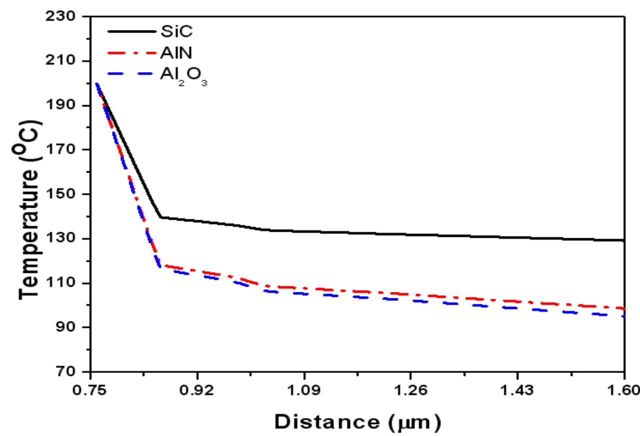


Figure 3.11: Heat dissipation of SiC, ceramic-AlN and Al2O3 for solder ball bumps packed LD

Finally, a comparative study of the planner to that of the solder ball bumps was performed using SiC package considering; overall, it seems the best performing submount material. The transient heat response and heat dissipation profiles for planar and ball bumps when SiC is used as submount are shown in figure 3.12 and 3.13, respectively. In Fig 3.12 the solid line represents submount temperature change over time

for the planar bumps structure. While the dashed line presents submount temperature change over time for ball bumps structure. It can be seen clearly that the transient heat dissipation response of planar package using SiC as submount is much better compared to solder ball pumps. This is due to the uniform spreading of the heat within the submount and dissipation without developing any localized effects.

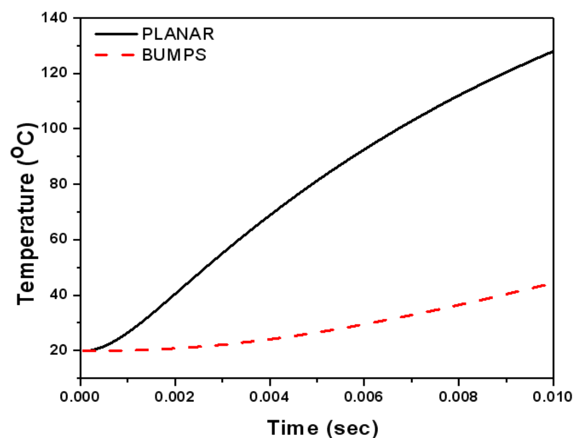


Figure 3.12: Heat dissipation of SiC for planner and solder ball bumps packaged LDs. Clearly planar are bumps structure has more heat dissipating to the submount

In Fig 3.13 the solid line represents submount temperature profile between junction and submount for the planar bumps structure. While the dashed line presents the same temperature profile for ball bumps structure. The two structures behave the same within the LD chip, however larger contact area and uniform heat distribution of the planar bumps give an advantage in heat dissipation into the submount.

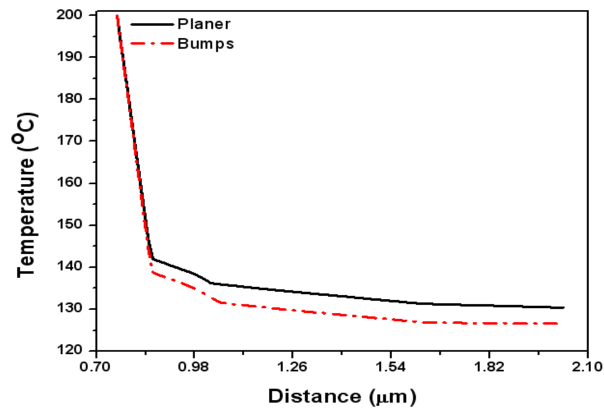


Figure 3.13: Heat dissipation of SiC for planner and solder ball bumps packaged LDs

The calculated L-I-V characteristics of the reference structure (unpackaged), Al_2O_3, ceramic-AlN and SiC package for the simulated 445 nm LD are shown in figure 3.14. The solid lines represent L-I-V characteristics of the unpackaged LD device. The dashed and dotted lines show the L-I-V plots for three possible LD packages using planar solder bumps. The obtained L-I-V results came in strong agreement with our simulated thermal results presented above. The packages with the best heat dissipation show the highest light output (L-I) and corresponding V-I characteristics exhibit higher voltage values for better heat-sinking. While the unpackaged devices show the lowest light output due to thermal effects. Good thermal management would lead to low junction temperatures which allows operating the devices at elevated injected currents but low losses, thus increasing the light output., Therefore, keeping the LEDs/LDs in an acceptable temperature will also ensure spectral stability of the emitted wavelengths.

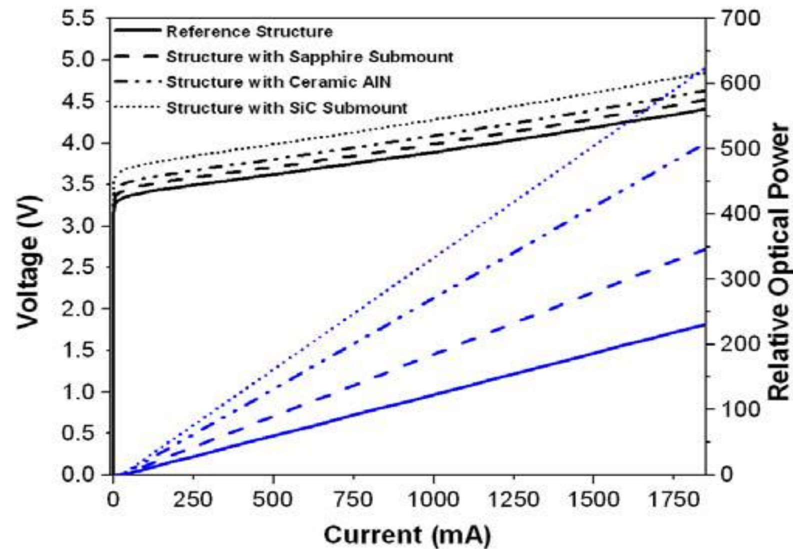


Figure 3.14: Calculated L-I-V Characteristics using planner submount package for (a) reference structure (without package), (b) Al_2O_3, (c) ceramic-AlN and (e) SiC.

For the sanity check and validation of the numerical findings/simulations presented in this chapter, it was beneficial to compare multiple experimental results related to L-I-V characteristics of III-Nitride devices reported in literature. Huh et. al. carried out experimental performance based temperature dependence study of InGaN/GaN MQW LED devices [40]. Several LEDs featuring different In-doping concentration were investigated by the authors of reference 40. Thiers findings show uniform drop in voltage as the device temperature increase regardless of the In-concentration. I-V characteristics are shown in figure 3.15. Comparing Huh's experimental results in figure 3.15 to our simulated results in figure 3.14, and taking into consideration the opposite orientation on the V and I axis –in figure 3.14 voltage is vertical and current is horizontal while in figure 3.15 voltage is horizontal and current is vertical-, similar V-I behavior is clearly observed. The voltage in both plots decreases as

the temperature of the device increases. The voltage change measured by Huh is around 5.5 V at 300 ^{o}K to 4.5 V at 423 ^{o}K [40], our simulation results predicts a voltage change of 4.5 to 5 V, where lowest voltage values are associated with the reference (hottest) LD device structure. The agreement between experimental results and simulated results presented in this study is essential for the development and accuracy of our later on research.

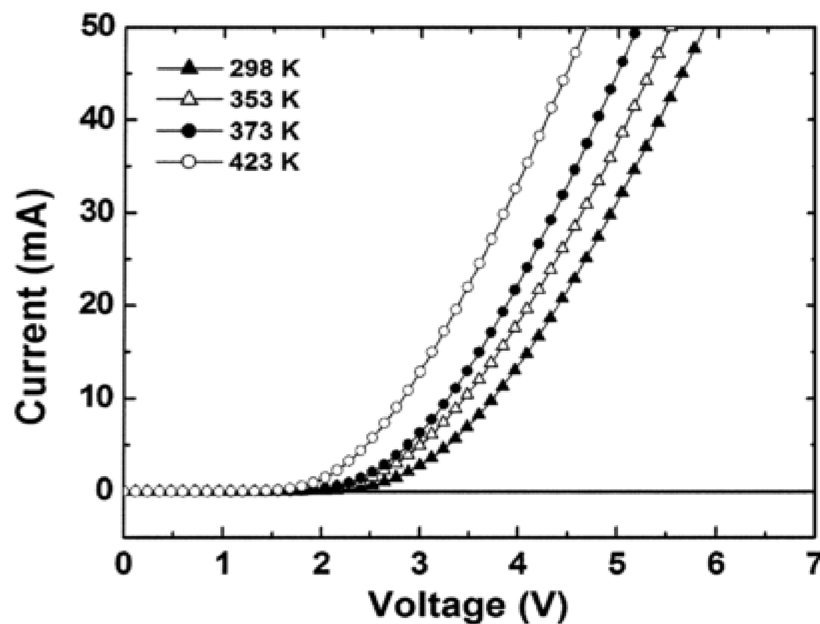


Figure 3.15: "V characteristics of the LED with 5% In composition in the MQWs as a function of the temperature" [40]

3.4 Summary

In this chapter, a theoretical study of the design and simulation for the transient heat analysis of 445 nm LD using Al_2O_3, ceramic-AlN, and SiC as submount materials for planner as well as solder ball bumps package was performed. This study is critical to improve the output and thermal stability of LD devices. With 3D numerical simulation,

we have investigated the effects of the planner and solder ball bumps packaged design for various situations. Comparative study shows that the transient response of temperature and heat dissipation from the structure strongly depends on the selection of the submount material and the packaged design. Planar solder bumps were found to be a better design for die attachment than ball solder bumps. Furthermore, results showed that SiC is the material of choice to be used as submount due to its high thermal conductivity and low lattice mismatch. This study was aimed to improve thermal management on chip level, knowing the most suitable die attach method is the first step to create enhanced thermally managed packages. In the next chapter the study will move to a new device and to the selection process of different thermal interfacial materials (TRIs), submount and heatsink materials different material combinations including conventional and novel material are used. Temperature profiles across different paths of the package are plotted and comparative study of the results was carried out to optimize the best performing structure. Next chapter discusses possible design for the packaging of III-Nitride Laser diodes along with comparative study and performance evaluation of different packaging material combinations, it also introduces a transient thermal analysis of heat dissipation in photonic devices structures.

CHAPTER 4: ON-CHIP SIMULATION FOR THERMAL ANALYSIS OF AlGaN/GaN ULTRAVIOLET LASER DIODES

After thorough introduction and background in chapter 1, chapter 2 presented our methodology for thermal analysis in details. Chapter 3 showed our thermal analysis results for different die attach methods and their impact on the device's junction temperature. In this chapter, the study is directed towards packaging materials optimization. Appropriate and optimal selection of packaging materials is essential for a successful packaging process. The essential steps in optimal device-packaging includes, i. die attach process using thermal interfacial materials, ii. Device mounting on submount layer, iii. Submount attachment to suitable heatsink, and finally encapsulation. Among these series of steps, thermal interfacial materials (TIM) play highly important role in attaching the device die to the submount; which is responsible for mechanical support and thermal management of the LED/LD devices. In the first section, the design and modeling of a new UV AlGaN/GaN LD device is presented. Besides the thermal behavior and dependence properties, L-I-V characteristics including output intensity and spectra are also presented. The second section of this chapter presents a package-design for the device of interest and proposes several options for electronic-packaging materials that existing in the industry and commonly used, and also considers relatively new Carbon Nano Tubes as a potential TIM option. In the third section, thermal modeling of the devices and its packing design are carried out for several possible material combinations. Simulations provide thermal profiles that are used for heat best performing

material combination and shows how it is utilized to estimate and determine the junction temperature of the devices.

4.1 Device Simulation and Packaging Materials for AlGaN/GaN UV LDs

Blue and UV Semiconductor light sources are the backbone of solid state lighting applications. AlGaN/GaN devices are among the promising options for SSL because of their emission spectra and their high power operation. However these materials still continue their growth process and development to reach the level of significant maturity. A big challenge continues that there are always high concentrations of defect densities, especially the 'threading' and 'point like defects' type in their epi-layers [41]. Also high contents of Al (~40%) give rise to grown epi-structure material imperfection issues and increases material resistivity. Typically, Joule effect is the main source of heat generation within epi-structures, high density of structural defects create discontinuities in the material lattice. These points in turn create electron traps that stop the flow of the electrons through the structure and into the active region which decrease the number of radiative recombinations thus decreasing the internal quantum efficiency and output of the devices. Also trapped electrons energies may be released through phonon -vibrations, results as heat [42] in the semiconductor epi-layers. Generally, for any emitter, most of the generated heat dissipates through its epi-structure by conduction. However, for any packaged and encapsulated device, small portion of heat can also be dissipated through the side walls of the package via convection route. In general the generated heat builds-up inside the chip and results in the degradation of the output characteristics, output intensity and the emission spectra of these devices. However, a good thermally managed package would ensure good heat removal from the epi-structures and guide the heat flux

efficiently to the heatsink that will transfer the heat to the ambient mainly through convection [43]. Considering that semiconductor materials selection and dimensions are dictated by the desired wavelengths, thermal management efforts are directed towards the packaging geometry and the thermal properties of its materials [44]. Suitable selection of the packaging materials and design can ensure good thermally managed devices with stable output and long lifetimes [45].

For the demonstration purpose, the device of choice was a multi-quantum well (MQW), AlGaN/GaN LD designed for operation in UV regime. Therefore, for this study, a MQW device epi-structure was considered for on-chip modeling and simulation of the designed package. Typical cavity length measured ~500 μm with width ~15 μm and the total epi-layers thickness was ~3.8 μm. The designed epi-structure has five quantum wells as an active region sandwiched between two cladding layers. An over all, devices epi-structure is shown in figure 4.1. The other supporting layers are defined as following. Electron blocking (EBL) layer was mainly incorporated to contain the overflow of the electron through the junction layer, and thereby, help improve the efficiency of the UV LDs. The designed chip also has two ~0.2 μm Au electrodes for current injection purposes. The fabrication of such emitters is often carried out by growing epi-structure either on sapphire (Al_2O_3) or SiC substrates and various other substrates such as Si are also being vigorously investigated worldwide. After running through a standard cleanroom fabrications process, the LD wafer is rum through a rapid thermal annealing and on-wafer characterization process. Prior their packaging, the processed wafers are lapped, polished, scribed and diced to obtain chip-scale devices for packaging.

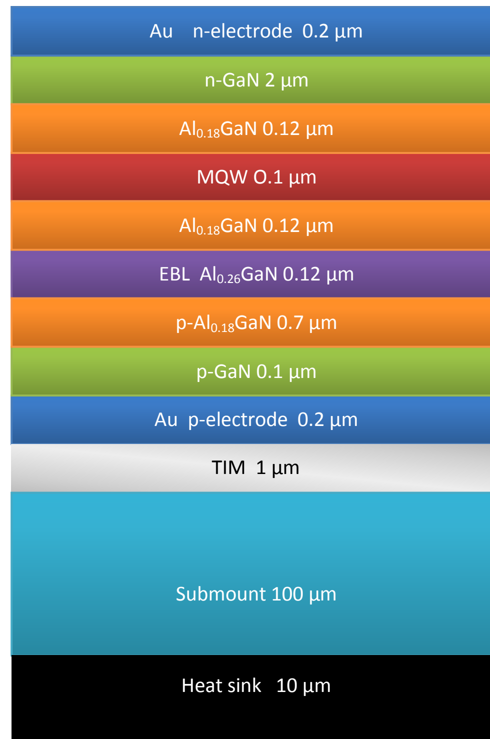


Fig 4.1: AlGaN/GaN UV LED chip with its detailed epilayers and the package structure (not to scale); however, typical layer thicknesses are denoted.

In practice, for most semiconductor light emitters p-side is always thinner to facilitate the holes flow, as holes often have low mobility and also the p-type material has lower conductivity as compare to the n-type layers. Such design employs a relatively shorter thermal path from the junction layer to the *p*-electrode. For such chip configuration, it is convenient to design packages such that submounts (~100 µm) are attached to the *p*-electrodes. The designed package for the LD devices under study was to attach the p-side of the device to a ~100 µm submount by ~1 µm thick TIM layer, submount is then connected to ~10 µm heat-sinks using metallic alloys filler. Sapphire substrates being a very low thermal conductivity material layer, is always etched away to

expose the *n*-electrodes for the package probing and testing and practical devices purposes. In the investigated design, the TIM layer was used as planar solder bumps. Compared to conventional solder ball bumps, a planer bump designed with the help of TIM layer is always helpful for the thermal management of UV LEDs [19]. 3D simulation and the thermal analysis of the proposed devices were performed using on-chip simulation. Fig. 4.2 shows a 3D model of the UV-LED chip mounted on a submount and attached to the heat sink.

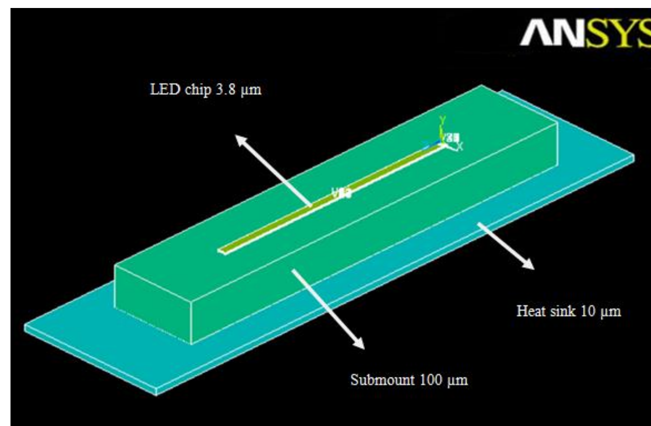


Figure 4.2: ANSYS13^{TM} generated 3D model of the LD chip mounted on submount [], dimensions are shown for the chip, submount and heatsink layers. Cavity length is 500 microns and heatsink length is 1.2 mm

The chip-scale device was modeled using RSOFT^{TM} LaserMod software package which employs finite element method (FFT) in order to simulate the optical gain and electronic properties [32]. A forward bias was set to 5 volts; LIV characteristics of the die are shown in Figure 4.3. The plot shows that an output power of ~ 1200 mW was

achieved for an applied voltage of ~5 volts, whereas, the corresponding injected current was ~800 mA.

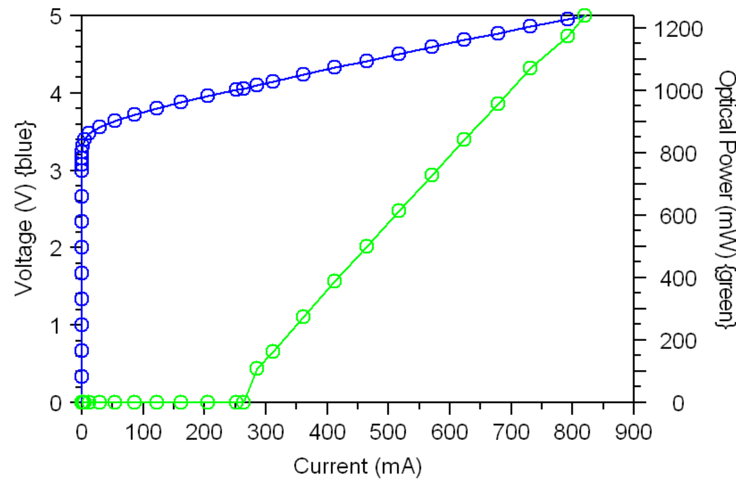


Figure 4.3: AlGaN UV LD chip L-I-V characteristics simulated using RSoft^{TM} package. Lasing threshold can be observed at observed at 3.6 V. output power start to increase to maxima of 1200 mW

4.2 Device Packaging Design and Materials

The effects of self-heating on the device performance can be observed clearly from the photoluminescence spectrum of the device. Heat affects the energy-levels of the semiconductor layers and shrinks the bandgap which leads to a red-shift in the emitted spectrum. Heat will also increase the lattice vibrations (phonons) in the material and thereby increase the probability of none-radiative recombinations. A noticeable red-shift in the output wavelength of the emitted light as a function of the temperature that

changed from 445 nm at 200 k to ~480 nm at ~500 k was estimated [14]. Also the intensity of the output decreases considerably as the temperature increases. A good thermal management of such devices will help decrease the adverse impact of high temperature on the device-performance and will lead to a more stable output and therefore, longer lifetime and higher reliability.

Since the device under study LD is an edge-emitting, the surface mounted devices (SMD) method was suitable for packaging [14]. Three layers of materials were used in the packaging process namely; TIM, submount, and heat sink. The aim is to test packages' ability to dissipate heat generated in the junction layers [46]. Several material systems were considered in the packaging process and the overall performance of each possible combination of these materials was determined by comparative study of the simulation results. For TIM layers, three options, namely $Au_{20}Sn_{80}$, $Ag_{3.5}Sn_{96.5}$ and CNT (Carbon Nano Tubes) were employed [47]. Metallic alloys are good for soldering because of their high thermal conductivity and relatively lower cost. Whereas, use of non-metallic materials such as CNT seems promising because, it has high thermal conductivity ~ 3000 W/m.k. However, it is not isotropic, i.e., it shows high thermal conductivity in the axial direction of nano tubes. Whereas, it has poor thermal conductivity (about 1.5 w/m.k) along transverse directions to the nano tube's axis [48]. This shortcoming makes CNT less suitable as submount or heat sink material. Nevertheless, if the tubes were oriented/grown perpendicular to the device surface, then CNT can be a very good TIM through which heat can be conducted vertically to the submount and finally to the heat sink. For submounts, three materials such as AlN, SiC, and diamond i.e. C were included in the investigations. For heatsink materials, Al and Cu

were considered. Our study aims to optimize the best combination of these materials for the packaging of the UV LD using 3D modeling and simulation.

4.3 Thermal Modeling and Simulation

Thermal analysis using finite element method (FEM) analyzer code was employed to study the transient thermal analysis. Fig. 4.2 shows the 3D model of the device attached to submounts by TIM layer and then attached to heatsink; the dimensions of the packaged devices were listed in detail above and also denoted in the diagram.

Most thermal studies of LED/LD devices were based on the assumption that LED chips are treated as “bulk material” with isotropic thermal properties [49]. The advantage and novelty of our model is that it takes into consideration the detail of epi-layers within LED chips and their thermal properties instead of treating the LED chip as a uniform bulk material with chosen thermal properties. This improvement helps to achieve more accurate and realistic results since doping in epi-layers can affect the thermal properties of semiconductor materials drastically [50]. Every epi-layer was modeled in the structure with suitable material properties depending on the doping concentrations. Transient analysis was based on the study of heat dissipation from the junction layer to the heat sink. The main method of heat transfer in such structures is conduction for the most part and convection when dissipating heat to ambient. Radiation is not of any importance because of its very little contribution; heat flow will mostly be pointing downwards from junction to heatsink. Upward flow can be neglected due to high thermal resistance of the encapsulation materials and ambient [51].

Measuring the temperature within the heatsink layer will define the efficiency of heat dissipation; a good package will have high heatsink temperature so more heat can be

removed through convection into the ambient. Three major thermal routes were considered, such as from junction layer to heatsink -along y-axis-, heatsink lateral cross-section -along x -axis, and heatsink vertical cross-section along z-axis-, were selected to produce temperature profiles as function of distance; plotted profiles were used for a comparative study of performance for each material combination in the package design. For the sake of a comparative study and also to decrease the simulation time needed, a maximum acceptable limit for junction temperature was used. In order to test the heat dissipation capabilities of the packaging, highest possible temperatures were considered. Also study was aimed to differentiate performance of different packaging materials as clear as possible. The selected junction temperatures were set to ~100 ^{o}C and the ambient temperature including the LED structure, submount and heat sink was kept ~ 0 ^{o}C. This high junction temperature value was used to clearly show the abilities of each material-set for heat dissipation and decrease simulation-time. On the other hand, the equilibrium time was chosen to be 500 sec with an intermediate time step of 5 sec.

Figure 4.4 shows an LD structure at the end of the transient analysis; it displays the temperature distribution color coded profiles along every layer at that time. It is evident that there is an asymmetry in heat distribution because of the rectangular shape of the LED chip under study. Based on the lateral and vertical cross-sectional paths, the heat distributions is useful to determine the structural performance. For this purpose, the four points, were assigned which mutually face each other across the center of the heat-sink, those were set as measurement points. The junction to heat-sink temperature profile was taken between two points in the middle of the junction layer and the heat sink.

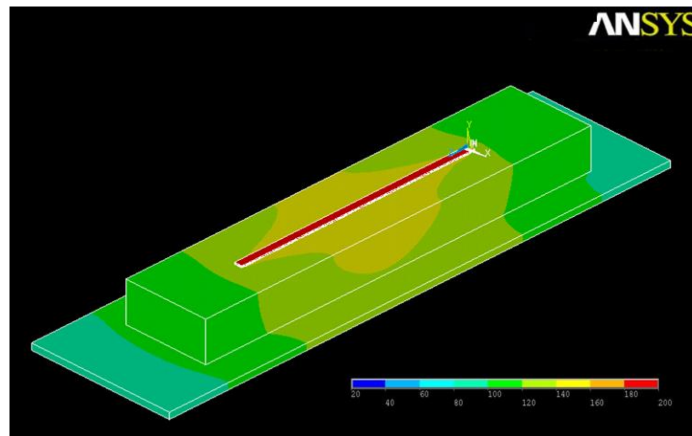


Figure 4.4: Heat distribution in LED package at 500 sec of operating time. Heat contours show heat dissipation from the LD chip to the packaging layers chip temperature was set to 200 ^{o}C while heatsink temperatures reached 80 ^{o}C.

4.4 Package Thermal Resistance Circuit Model

In order to expand the understanding of these results, it was useful to exploit additional thermal parameters such as thermal gradient and thermal flux. Both of these parameters were calculated for the best and poorest performing material combinations. These measurements were taken along the vertical line between the junction layer and heat-sink. These two parameters were consistent with our earlier results.

Relatively high junction temperature values were used in the simulations to test the thermal behavior of the packaging materials to the extreme realistic limits. And also it helped to show the performance differences between the various packaging options for purpose of clarity. For completing this study, it was tempting to calculate the expected junction temperatures for the devices of interest. Calculations were performed considering fully packaged devices in order to show how the selection of the packaging

materials directly affects the junction temperature. It contributes not only in heat dissipation but also to lowering the value of the junction temperature. The thermal resistance circuit (TRC) model was also employed in this study because it allowed a good theoretical estimation of junction temperature values. Junction temperature can be expressed by the following relation [52]:

$$T_j = T_a + (R_{thj-a} \times Pd) \quad (4.1)$$

Where: - T_j is the junction temperature

- T_a is the ambient temperature

- R_{thj-a} is the total thermal resistance from junction to heat sink

- P_d is the power dissipation in the LD/LED

Thermal resistance for a layer is calculated as:

$$R(C^o/W) = \frac{X}{kS} \quad (4.2)$$

Where: - X is the path-length of the heat (m)

- S is the area cross-section of the layer in the direction normal to heat flow
- K thermal conductivity (W/m.C.)

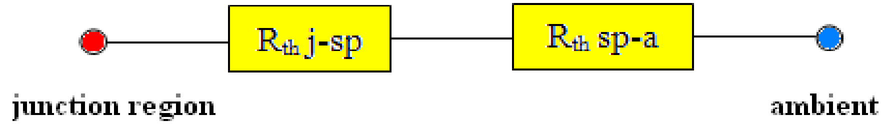


Figure 4.5: Thermal resistance schematic of a LD package, showing two thermal resistances in series

Using experimental values from literature of thermal conductivity for the semiconductor material in the epi-layers, metallic, and non-metallic materials in packaging and relation (4.2) thermal resistance for every layer in the structure was calculated and some are listed in table (4.1) Adding these values from junction layer to the heat sink, we calculated R_{th} j-a using the following:

$$R_{th\ j-a} = R_{th\ j-sp} + R_{th\ sp-a} \quad (4.3)$$

Where: R_{th} j-sp is thermal resistance from junction layer to solder point

R_{th} sp-a is thermal resistance from solder point to the ambient

Table 4.1 thermal resistance values for LED's epi layers and packaging material

Layer	Thermal resistance ($^oC/W$)
$1Al_{0.08}GaN$	0.133
$Al_{0.18}GaN$	3.56
$A_{0.26}GaN$	0.77
GaN	0.1
Au	0.03
$Ag_{3.6}Sn$	3.7
AlN	0.86
Aluminum	0.05
CNT	0.034
Diamond	0.245
Copper	0.003

4.5 Results and Comparative Study

We carried out 3D simulations of the designed structure and the transient thermal analysis of UV LDs and performed theoretical junction temperature calculations. Our study started with the design of UV LD structure and simulated using RSoft Design™ software package. The obtained EL spectra confirmed the peak emission intensity of the

targeted wavelength (333nm). For three dimensional transient thermal analyses, our focus has been comparing the distrib'2ution and dissipation of heat through the junction layers. As noted earlier, packaging model has been explored for three different TIMs ($Au_{20}Sn_{80}$, $Ag_{3.5}Sn_{96.5}$, $Ag_{3.5}Sn_{96.5}$, and CNT), submounts (AlN, SiC and diamond) and two heat-sink materials (Cu and Al), respectively. In all, eighteen (18) different combinations were analyzed using modeling and simulation.

Efforts were made to explore a suitable combination of TIM, submount, and the heat-sink for efficient packaging for the improved thermal management of the high-power UV LDs. The study was carried out by choosing one TIM material, and then testing it with all possible material combinations of submounts and heat sinks systematically. Results were then compared for each TIM material over each specific thermal path of the three mentioned above and earlier in reference [14]. Comparative study data are presented in detail in appendix A. This data was used to generate temperature profiles along the three selected routs described earlier.

This visual representation of the data helps in the selection and optimization process of the best packaging materials. A series of figures, Fig. 4.6 through 4.13 show temperature profiles for all material combinations considered along all three thermal routs defined above. Each TIM material was modeled with all possible combinations of submount and heatsink materials. Temperature profiles are grouped based on the TIM and thermal path then plotted together for the purpose of comparison.

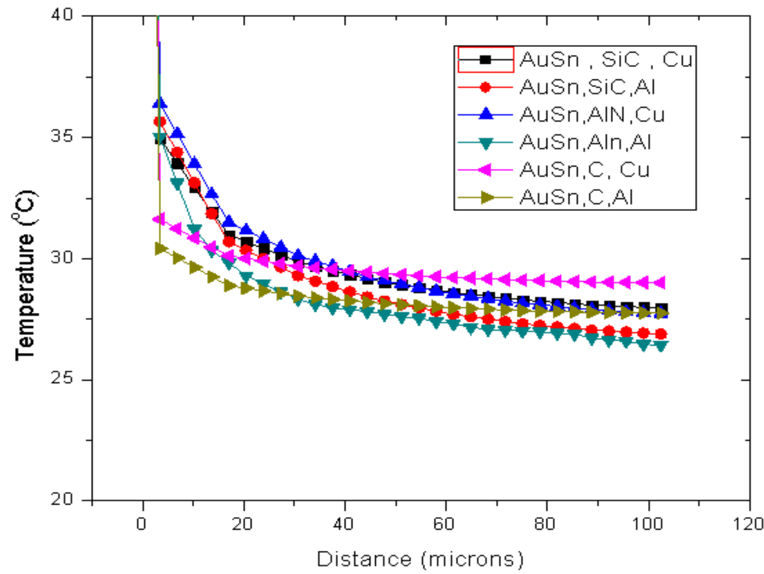


Figure 4.6: Temperature distribution along junction-to-heatsink thermal path for AuSn as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations.

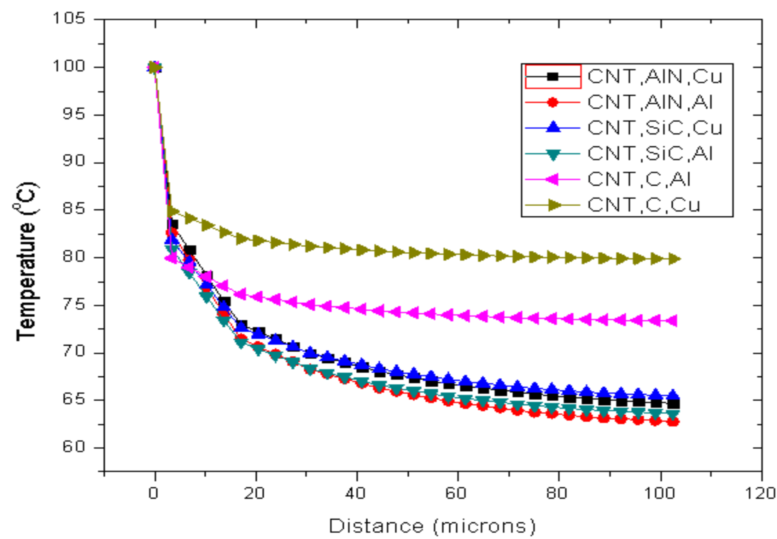


Figure 4.7: Temperature distribution along heatsink horizontal thermal path for CNT as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations.

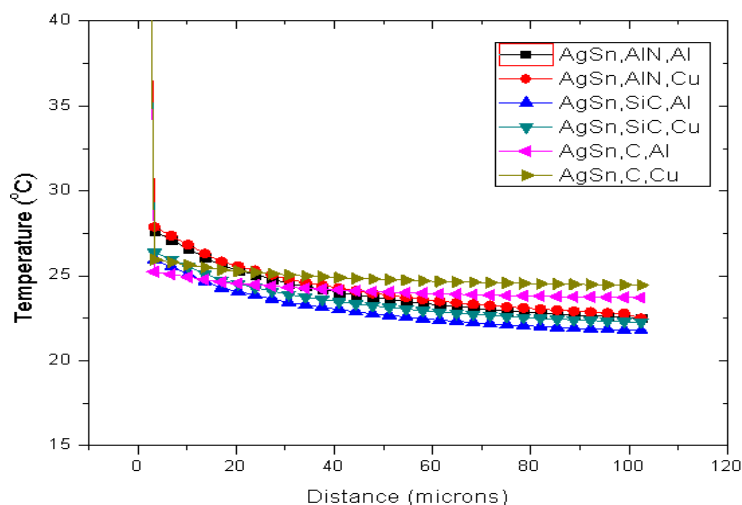


Figure 4.8: Temperature distribution along heatsink horizontal thermal path for AgSn as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations.

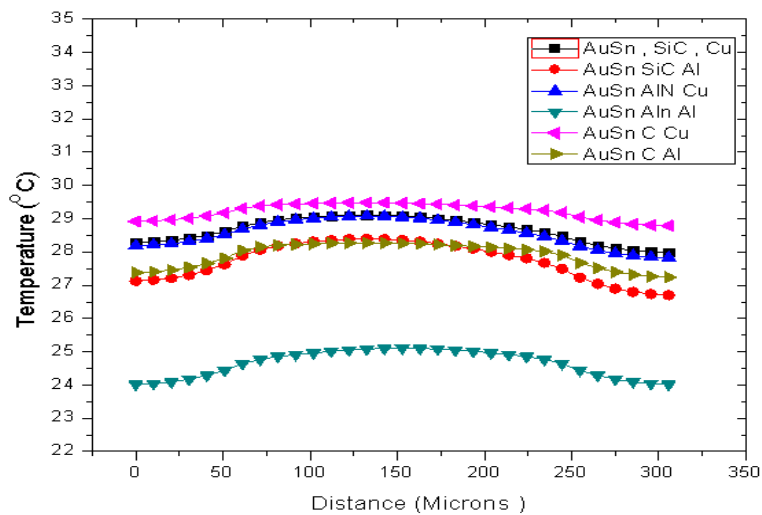


Figure 4.9: Temperature distribution along heatsink horizontal thermal path for AuSn as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations.

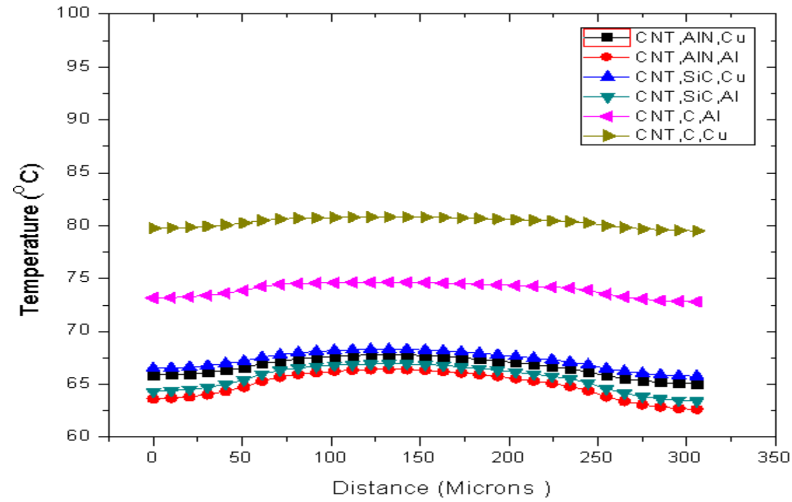


Figure 4.10: Temperature distribution along heatsink horizontal thermal path for CNT as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations

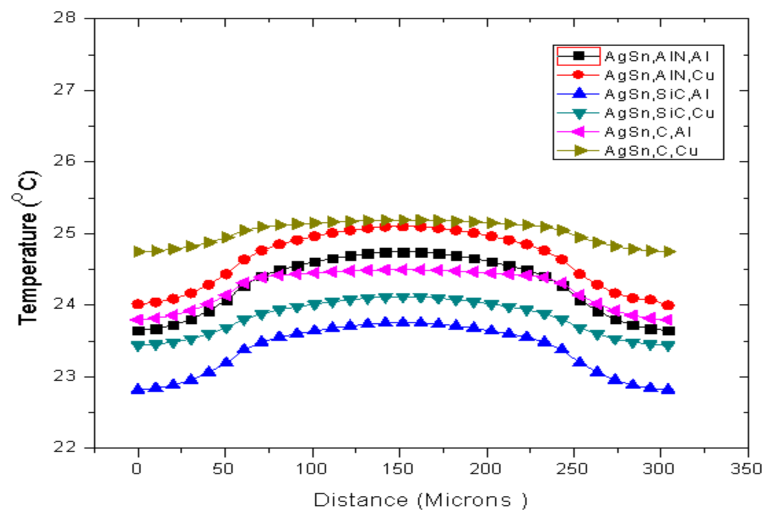


Figure 4.11: Temperature distribution along heatsink horizontal thermal path for AgSn as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations

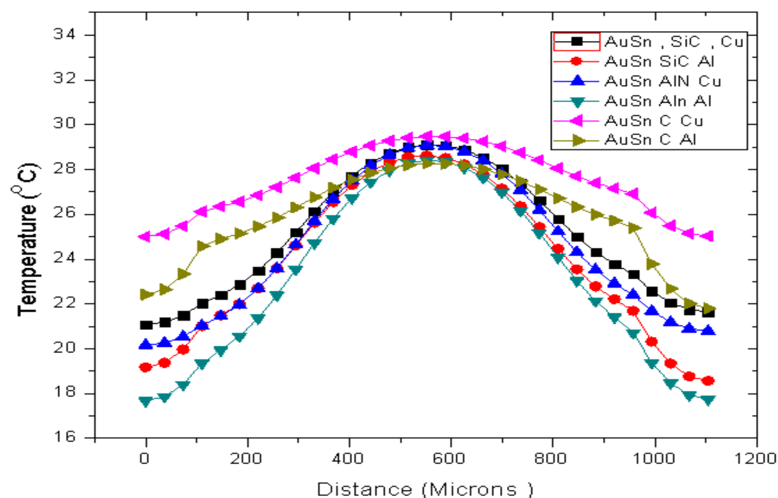


Figure 4.12: Temperature distribution along longitudinal horizontal thermal path for AuSn as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations

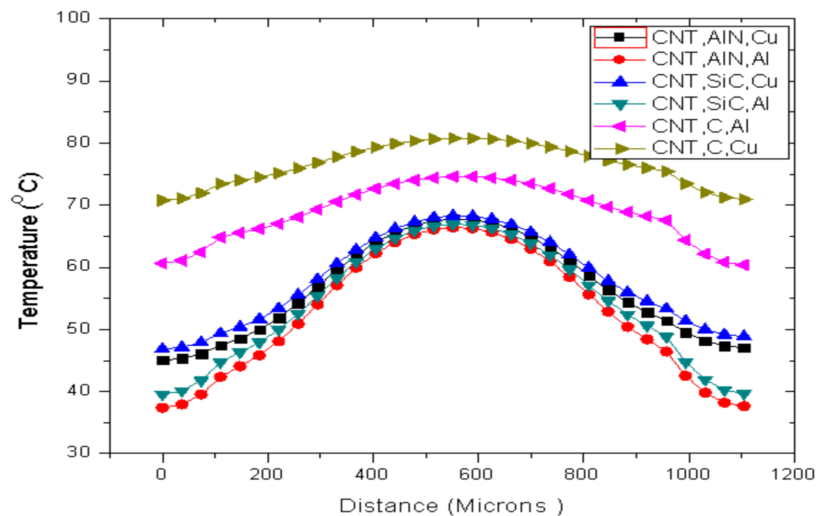


Figure 4.13: Temperature distribution along heatsink horizontal thermal path for CNT as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations

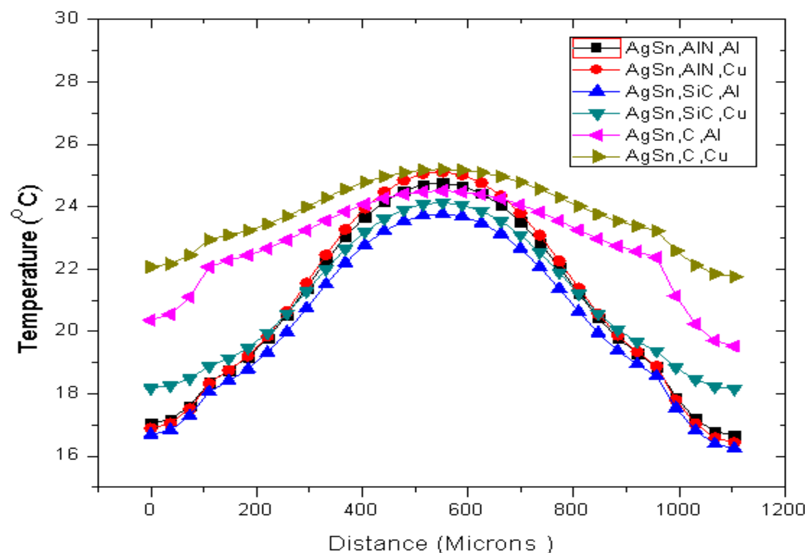


Figure 4.13: Temperature distribution along heatsink horizontal thermal path for AgSn as TIM and various submount and heatsink Materials. The legend symbols and colors represent different material combinations

Careful examination of the presented results show that heat distribution profiles along the lateral and cross-sectional directions for CNT, were best compared to $Au_{20}Sn_{80}$, $Ag_{3.5}Sn_{96.5}$ for diamond as substrate and Cu as heat-sink. The results came with good agreement for all the paths considered and showed nice consistency. In order to further strengthening these results, two more thermal parameters were also considered such as thermal gradient and thermal flux, respectively. It is evident from results that the best performing structure is CNT, C, Cu and on other hand the least performing structure consists of $Ag_{3.5}Sn_{96.5}$, AlN, and Al. To further strengthen these findings, additional thermal parameters were calculated and compared for the both best and worst performing structures the result illustrated in figures 4.14 and 4.15 which show a quantitative

comparison between thermal flux and gradient of these two structures On the thermal path that extends from junction to heat sink has length ~ 112 µm.

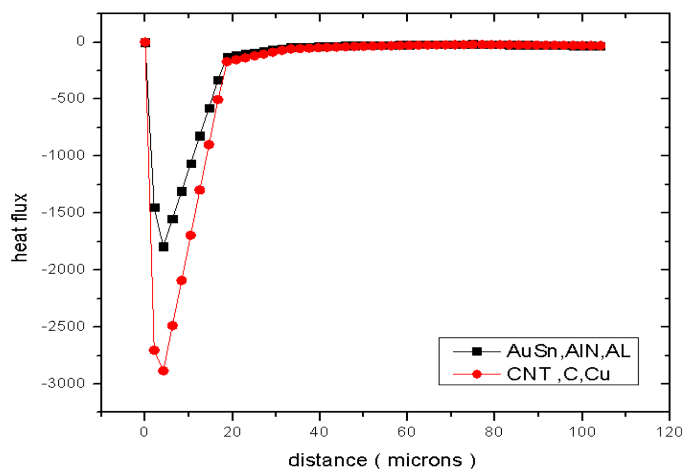


Figure 4.9: Heat flux comparison between the best and worst performing material combinations. Black squares and red dots symbols represent thermal flux of $Ag_{3.5}Sn_{96.5}$ AlN, Al and CNT, C, Cu structures respectively

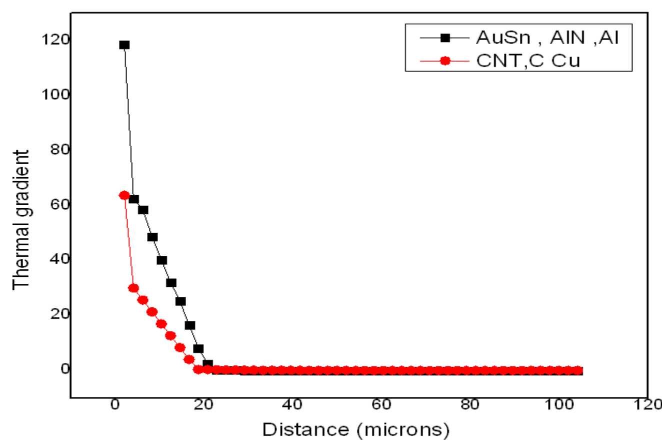


Figure 4.10: Thermal gradient comparison between the best and worst performing material combinations. Black squares and red dots symbols represent thermal flux of $Ag_{3.5}Sn_{96.5}$ AlN, Al and CNT, C, Cu structures respectively

By examining the thermal flux and gradient results, we immediately notice that the structure with CNT, C, Cu shows a clear advantage. It allows much more heat to pass through the structure to the heat sink. On other hand, the structure consisting of $Ag_{3.5}Sn_{96.5}$ AlN, Al shows higher thermal gradient values which means that heat is not evenly distributed in the structure and most of it is still trapped in the LED chip itself. This all comes with good agreement with the results obtained by examining the temperature profiles of different packaging options.

Knowing the best packaging options, our next step was to estimate junction temperature for these devices using our TRC model. The ambient temperature was set to 20 ^{o}C for these calculations, and the L-I-V data from LaserMode^{TM} LIV characteristics shown in Fig. 3 display that for maximum light output operating voltage was at ~4.90Volts which makes the driving current I = 790 mA. Therefore, the dissipated power can be estimated easily. Finally, taking into account all the calculated values for thermal resistance and power dissipated and ambient temperature values, we can determine the junction temperature from Eq. 4.1. By performing these calculations for the LD/LEDs packaged with $Ag_{3.5}Sn_{96.5}$ AlN, Al layer structures, it was found that Tj = 55.74 ^{o}C. While performing the same calculations for the LD/LED packaged with the optimized structure of CNT, C, Cu it was found that Tj = 38.91 ^{o}C. This last result clearly shows that the use of the better performing set of material layers not only dissipated heat efficiently but also decreased the junction temperature. This also is in agreement with the results of the transient thermal analysis.

4.6 Summary

In this part of research, AlGaN/GaN power LDs thermally managed packaging was investigated by modeling and studying numerically using a theoretical framework. Thermal 3D modeling and simulations were performed to show the best possible packaging options. The study included, 18 possible sets of the specialty packaging materials such as, three thermal interfacial layers of $Au_{20}Sn_{80}$ alloy , $Ag_{3.5}Sn_{96.5}$ alloy , and CNT (carbon nano tubes), three different submount materials of AlN, SiC, and diamond and two heat-sink material i.e., Al and Cu .comparative study of results shows that the CNT as TIM, diamond as submount and Cu as heat-sink is the best packaging choice of the materials considered in this study and the use of this set will ensure highest heat dissipation rate from the junction layer to heat-sink. Other thermal parameters such as thermal flux and gradient were also studied to confirm temperature profiles findings and were carried out for the best and worst packaging options and showed good consistency. Junction temperature was also theoretically determined using thermal resistance model and the data obtained from the device L-I-V characteristics for the best and worst performing structures. The results showed that when the best materials combination was used it resulted in junction temperature of 38.91 ^{o}C while the worst performing material set caused junction temperature to rise to 55.74 ^{o}C which come in consistence with the simulation results. Up to this stage, research was concerned about basic packaging materials and designs for several LD devices. Heat dissipation was evaluated through conduction only. The following chapter will present more complete thermal analysis for LED packages. Heat convection was included in the thermal analysis to achieve thermal equilibrium for CW (continues wave) operation. Complicated heatsink

designs will be introduced to LED devices and a performance comparative study will show the best heatsink design to ensure low-cost high performance, and thermally managed LED packaging.

CHAPTER 5 THERMAL ANALYSIS OF COP PACKAGED AlGaN/GaN BACK-EMITTING LEDS

In the previous chapter transient thermal analyses for different LD/LED packages using different material combinations was presented. The packaging was optimized based on thermal response due to heat conduction. The next step in this work was naturally to carry out a full thermal analysis for practical LED/LD packaging taking into account not only the materials, but also geometry, dimensions, and cost. This chapter contains a complete thermal study for high-power UV LED packages using the new chip-on-plate (COP) technique [25]. COP principle and advantages are presented in the first section of the chapter, along with the device, package, and heatsink designs considered in this study. Thermal FEM analyses and considerations are presented in the section 2 of this chapter. Simulation results were supported by mathematical model results to corroborate our findings, thermal resistance circuit model developed for this study is presented in the third section. All results and comparative studies of variety of packages are discussed in the results section to show the best performing package and heatsink design.

5.1 Chip-on-Plate (COP) Packaging Technique

Currently, solid-state lighting type emitters based on InGaN/GaN and AlGaN/GaN are in high demand for replacing conventional light sources. However, increasing demand requires these emitters to be thermally more stable with increased lifetime for their industrial applications. In order to address these challenges, advanced ackaging with local thermal management (LTM) has to be considered in the production

process of these devices. For most SSL applications, multiple arrays of LEDs/LDs arearranged in compact packages which increase the need for LTM and makes it even more challenging. As discussed in the previous chapters it is evident that LTM of such emitters is required mainly due to the generated heat, which gives rise to high junction temperatures, when operated at high injected currents [53]. The observed red-shift in the emitted wavelengths is also a result of the unwanted rise in the junction temperature, which could be responsible for their poor thermal stability, and eventual results as a decrease in the lifetime of such devices. It is therefore, critical to address these issues by improving device packaging techniques using new materials and techniques alongside with advanced numerical analysis techniques. Currently, many new packaging methodologies are being explored to overcome these issues.

When dealing with SSL applications, devices are expected to be on-mass production and assembly. Producing high-quality long-lifetime dependable devices is the main drive for developing photonics light sources; however, when it comes to marketing these devices, cost is also a major factor. For the SSL technology to replace the conventional lighting devices have to be durable efficient and low-cost too. Considering device fabrication and materials are dictated by the desired wavelengths and intensity. Based on this technicalities cost control measures are implemented through the packaging process, careful material selection and package design is the solution to ensure good quality yet cost-efficient devices.

Among the new packaging techniques COP - is presented for the advanced packaging of AlGaN/GaN based UV-LEDs for SSL. The unique features of this technique are the use of a low work-function and high-thermal conductivity metals as a

submount material. Compared to Si, SiC, and ceramic AlN, semiconductor grades (99.999%), Al has been recognized as the most suitable choice for the COP packaging. Al as a submount is a lower-cost replacement for more expensive SiC and AlN ceramics, another advantage of using metals for submounts is process friendliness and flexibility. Therefore, COP is among few low-cost and thermally efficient packaging methodologies. COP has clear advantage compared to a chip on board (COB) packaging technique, where multiple light sources are directly laid on a copper-based printed circuit board (PCB). Followed by their mounting on a heat-sink, for COP, high thermal conductivity Al-plates are used as a submount, rather than lower- thermal conductivity PCBs [53].

Due to its excellent thermal properties and large size, Al-plate plays an important role in providing mechanical support and the necessary heat flow path for dissipation through the heatsink due to its high isotropic thermal conductivity. Furthermore, Al-plate when in contact with Cu-heatsinks also helps to improve the thermal mass involved in heat dissipation, and adds packaging flexibility. Due to the ease of attaching Al-plates to other metallic heatsinks, it therefore increases the overall thermal stability and performance of the entire package. COP package will include the device die on its substrate to be attached to the metallic plate submount by solder alloy then the submount itself can be attached to a variety of heatsinks. For the research GaN/AlGaN UV-LEDs based on sapphire substrate were considered for optimal chip size of ~1mm^2. The necessary details of such structure are described elsewhere [25]. The packages were thermally analyzed using FEM code and mathematically studied using TRC model to show the performance of different COP packages using various heatsink designs.

5.2 Multiple Package Designs Modeling

The COP-package considered in this research include LED-chips mounted on Al-submount using Ag-solder metallic alloys. Typically, Al-plate is connected to heatsink via thermal grease. Heatsinks are the elements responsible for dissipating heat into the ambient through thermal convection. Heatsink design and dimensions are critical for efficient heat dissipation and also cost control, in order to make this study as useful and as realistic as possible, two major heatsink designs were selected for the comparative study, plate-fin heatsinks, and pin-fin heatsinks [54-55].

In this work, two different plate-fin heatsinks (A,B), and two different pin-fin heatsinks (C,D) were modeled and included in the COP package by attaching them to the Al-submount. It is worth noticing that all heatsinks models were accomplished using pure copper, mainly due to its high thermal conductivity. Some of the key parameters, such as the dimensions and fin/pin numbers of plate/pin fins heat-sinks used for this study are shown in tables 5.1 and 5.2. Among the key specifications of these heatsinks are their dimensions i.e., 128 mm^2 base was designed for all 4 heatsinks (A,B,C, D), all fins were 10 mm long. For the sake of comparison, similar-size heatsinks with different numbers of fins/pins and respective sizes were modeled. A simplified structure of COP type package is illustrated in figure 5.1 below.

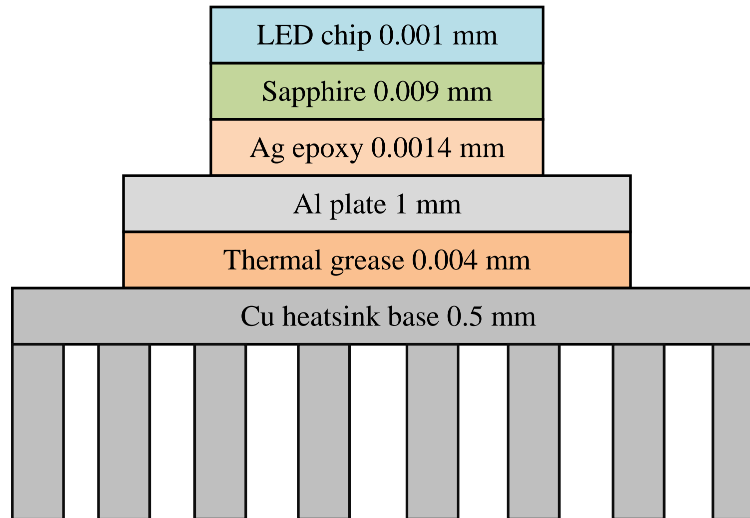


Figure 5.1: Schematic of a chip on plate (COP) LED package (not to the scale).

The primary motivation to use COP type packaging technique for AlGaN/GaN based high power UV LEDs is to lower the total thermal resistance of these devices when fully packaged. This would allow driving such emitters successfully at their high injected currents without significant increase to their junction temperature (T_j). Another key benefit is to lower the devices junction temperature, while keeping the same output, which is important for enhancing the reliability and lifetime. As discussed in previous chapters, it is evident that the generated heat is mostly channelized to flow from junction layer of the chip to the heatsink by thermal conduction. Low thermal conductivity of the encapsulation and small areas of the side walls of the device make heat dissipation through encapsulation and small side-wall surfaces of the chips neglected.

The generated heat will be removed by the heatsink into the ambient through natural convection. Heatsink's thermal exchange ability through the surrounding ambient

is a major factor in efficient heat dissipation. Optimizing proposed Al-submounts and heatsink designs can achieve more heat dissipation and enhance the package performance; this optimization vary among changing Al submount thickness, size and interspacing between fin/pins used for heatsinks. In this work, four (4) different heatsink designs were modeled in order to find the best performing heatsink design for the considered COP packaged device. It has also been found that such thermal improvement cannot be achieved by conventional flat-base type heat-sinks. The following table 5.1 and 5.2 show/ provide the number of fins and dimensions for the plate-fin heatsinks and the pin-fin heatsink modeled respectively.

Table 5.1. Plate-fin heat-sinks specifications

Heat-sink	Number of fins	Fin thickness
A	14	0.5 mm
B	7	1mm

Table 5.2. Pin-fin heat-sinks specifications

Heat-sink	Number of pins	pin thickness
C	196	0.5 mm
D	49	1mm

5.3 Thermal Modeling

Thermal analysis of the entire COP packaged GaN/AlGaN UV LED was performed using ANSYS-13^{TM}, a commercial finite element module for this study. In 2008 Tsai et. al presented a 2D simulation model using a cylindrical shape heat-sink design [25]. Our work present a 3D modeling and simulation of UV-LEDs using COP technique by attaching it to a variety of high thermal conductivity heatsinks. Some of the key thermal properties of the material used for this study are given table 5.3 [25]. Each thermal analysis was carried out including heat conduction through the package and convection on the outer surfaces of Al-submount and heatsinks. Furthermore, it was assumed that all the material systems used have perfect bonding; the radiative losses and the heat transfer due to radiation were insignificant. Moreover, convection was calculated by considering no air-flow (forced convection) on the heatsink.

For numerical analysis, we assumed uniform heat distribution at the junction layer which is suitable due to its small area. Heat generation functions were connected with the power level used to simulate accurate real-time self-heating effects. Three

different operating power values (1, 1.2, 15) Watts were used. The ambient temperature was set to be 20 ^{o}C as an initial thermal load along with the initial temperature of the entire structure. Each 3D model was carefully meshed with attention to the interfaces between layers to minimize errors and keep the analysis accurate after meshing each structure, thermal load were applied to each area and volume to create realistic continues wave (CW) operating conditions. Figure 5.2 shows a 3D model of COP package attached to heatsink (A)

Table 5.3 Material thermal properties for COP packaging [25]

Material	Thermal Conductivity W/m.C	Specific Heat J/kg.C
LED Chip	42	2000
Sapphire	35	712
Ag solder	8	761
Aluminum	220	910
Grease	3.6	1044
Copper	380	380

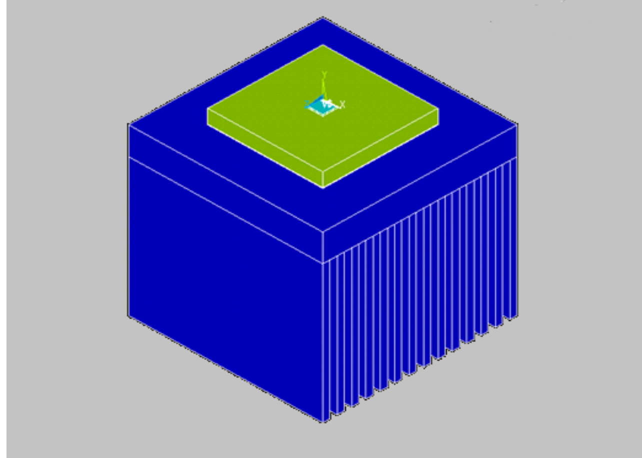


Figure 5.2: 3D view of COP package with using plate-fins heatsink A.

5.4 Thermal Resistance Model for Advanced Packaging

Regarding the cross-confirmation of FEM thermal analysis results of newly developed COP technique, theoretical thermal resistance circuit (TRC) model- described in chapter II- was also employed to re-evaluate the junction temperatures [26]. In TRC model if the ambient temperature and the dissipated power are known, junction temperature can be found easily by determining the total thermal resistance of the package simply by applying equation 2.6. The key for using TRC model is to develop a suitable thermal circuit of the considered structure [51]. Thermal paths have to be determined thoroughly form the source region to the ambient, accurate heat flow prediction is essential for drawing the structure's thermal circuit. The branching of thermal paths is also of high importance for setting different thermal resistances in series or in parallel. For our COP package heat flow was considered to be vertical from the LED chip towards heatsink, considering uniform heat generation in the chip, and the

small dimension of the substrate and solder alloy layer, heat flow from chip to Al-submount is represented by one thermal path. The relatively large submount layer presents a branching point for heat flow through its side surfaces and considering the 3D nature of the model, four horizontal ?perpendicular ?thermal paths were drawn in addition to the major vertical path. Each horizontal thermal path was studied individually for taking in consideration all possible the top and side surfaces of the Al-submount. Any length that heat travels within packaging layers will be considered as a conductive thermal resistance, any material-air interfaces are represented as convective thermal resistances. Figure 5.3 shows a 2D representation of horizontal thermal paths within Al-submount.

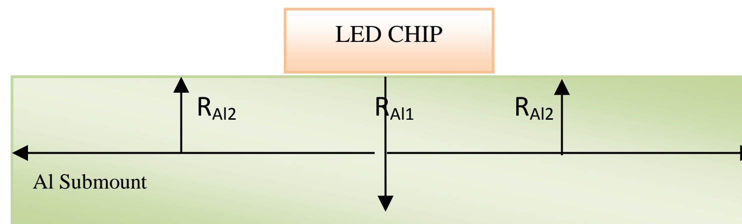


Figure 5.3: 2D representation of horizontal thermal paths within Al-submount, arrows represent different vertical and horizontal thermal paths for heat dissipation through the top and side surfaces of the Al-plate.

The main vertical thermal path continues to the heatsink. Considering the complex designs of heatsinks modeled in this study, heatsinks were treated as one material layer taking into account both conductive and convective aspects of them. Thermal resistance of each of different heatsinks was evaluated through mathematical

modeling; the type and dimensions of the heatsinks play important role in determining their respective thermal resistance values. The derivations of heatsink thermal resistance in details are available in the literature [27] [28] [43] [54]. All heatsinks have the same base dimensions but different types and pin/fin sizes. All heatsinks thermal resistances were calculated and employed in TRC calculations. Figure 5.6 shows the TRC diagram for all COP packages. The thermal circuit is the same for structures A, B, C, and D; however, the only difference is the value of the thermal resistance of the heatsink, which would clearly show the effect of different heatsink designs on the chip temperature.

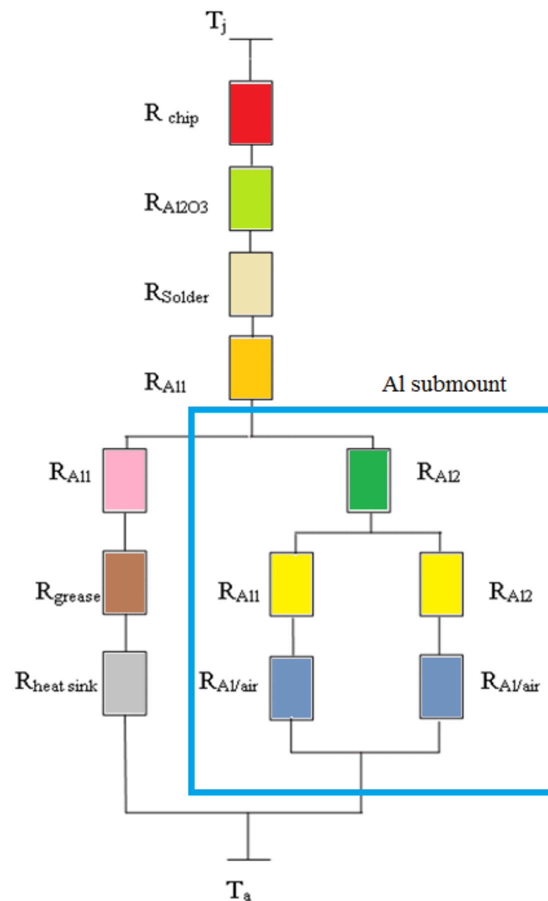


Figure 5.4: Thermal resistance circuit for a typical chip on plate (COP) package. The vertical thermal path branches at Al-submount and dissipate in the Al-submount (the right hand side resistance assembly), while the original vertical continues to the heatsink then to the ambient.

Thermal resistances R_{chip}, R_{Al2O3}, R_{Solder}, R_{Al1}, R_{Al2}, and R_{grease} are all conduction based, while $R_{Al/air}$ is convection based thermal resistance at Al/Air interface. The term $R_{heatsink}$, is the heatsink's total thermal resistance that includes both conductive and convective effects [20].

It is necessary to mention that TRC diagram shown above is a 2D representation showing the thermal circuit; however, for the realistic 3D structure, there will be four horizontal paths and each path will have its own thermal resistance; all those would be considered as four thermal resistances connected in parallel.

Considering;

$$R_1 = R_{Chip} + R_{Sio2} + R_{Solder} + R_{Al} \quad (5.1)$$

$$R_2 = R_{Al2} + \frac{1}{4} \times \left(\frac{1}{R_{Al1} + R_{Al/Air}} + \frac{1}{R_{Al2} + R_{Al/Air}} \right)^{-1} \quad (5.2)$$

$$R_3 = R_{Al1} + R_{Grease} + R_{Heat-sink} \quad (5.3)$$

Where the total thermal resistance can be given as;

$$R_{TH} = R_1 + \left(\frac{1}{R_2} + \frac{1}{R_3}\right)^{-1} \quad (5.4)$$

The junction temperature (T_j) values were determined using R_{th} results, which were determined using equations 5.1 to 5.4. The calculations show that inside Al-submount, the vertical thermal path offers less thermal resistance than the horizontal thermal paths, in other words, R_{Al1} is smaller than R_{Al2}. Therefore, most of the heat flow will be in the vertical direction following least thermal resistance path. Furthermore, heatsinks were also chosen based on their good thermal transfer and perfect flatness of

the contact areas. Although, simulated heatsink geometries seem different, but depending on the space constraints, their thermal resistances were closely matched. It was noticed that heatsink thermal resistance varied depending on their types and geometries, and fin density [56].

5.5 Results and Discussion

For the COP packaging of GaN/AlGaN based UV LED, as noted earlier, four different heatsinks designs were modeled and simulated using software package as well as numerically. Packaged device's junction temperatures were determined for each case at three different DC driving currents. Figure 5.5 and 5.6 show heat distribution at operating power of 1.5 W in COP packages connected to heatsinks A and C, respectively. The insets show a closer look at the heat map of the LED chip in each package. Furthermore, junction temperatures were also evaluated using TRC model developed above for all proposed COP package when attached to heatsinks A, B, C, and D. Figures 5.7 and 5.8 show chip temperature values for each type of heatsinks obtained by both FEM and TRC, respectively. Results came in a good agreement and were consistent with a relatively small difference of around 4 ^{o}C. The observed small temperature difference should be acceptable in the simulations, since we neglected convection on the side surfaces of both the LED chips and the substrates. We also ignored the contact thermal resistance at the fin/base interface for simplification. In the work presented earlier by Tsai et. al in [25] an experimental COP structure was created and tested at different power levels. 2D ANSYS FEM simulations along with TRC model were also employed to calculate device temperatures. Both TRC and FEM results were subject to comparative study to show the level of agreement, Tsai results plotted in figure 5.9 [25]. A deviation

of 1 to 2.5 °C between TRC and 2D FEM results i. evident. The deviation between our 3D FEM and TRC results is around 2.5 to 4.3 °C, however, this difference can be justified due to our 3D simulation and the higher complexity of heatsinks modeled in our study. Nonetheless, having a results agreement with similar range to that of an experimental data offers a strong support to the model presented in our study and justifies the level confidence of our findings.

Results demonstrate that densely pin-finned heat-sinks performed best out of the four considered, as the chip temperature was kept at its lowest values between 31 °C to 35 °C for the corresponding operating power levels. On the other hand, the less dense pin-fin and plate-fin heatsinks resulted in relatively higher chip temperatures. The integration between FEM modeling and theoretical TRC calculation presented in this work allows the evaluation and optimization of wide variety of COP packages, which helps finding the best balance between performance and cost.

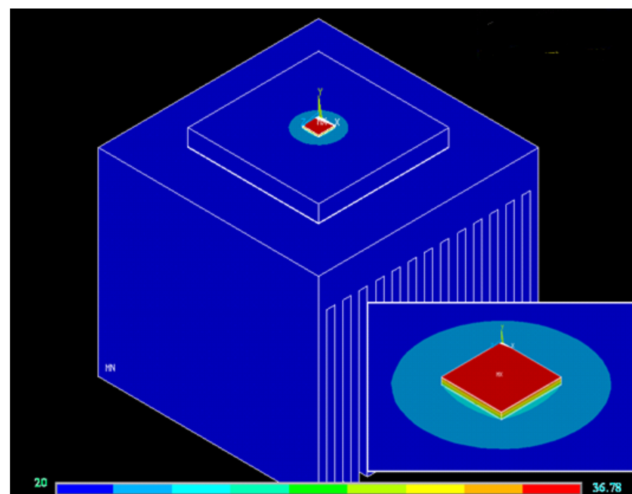


Figure 5.5: Heat dissipation for COP packages attached to heatsinks A at operating power of about 1.5 Watts (~700 mA current). The inset shows the enlarged view of the LED chips the color signifies the heat distribution. The color bars are the scales covering the temperatures from blue (20 °C) to red (36 °C).

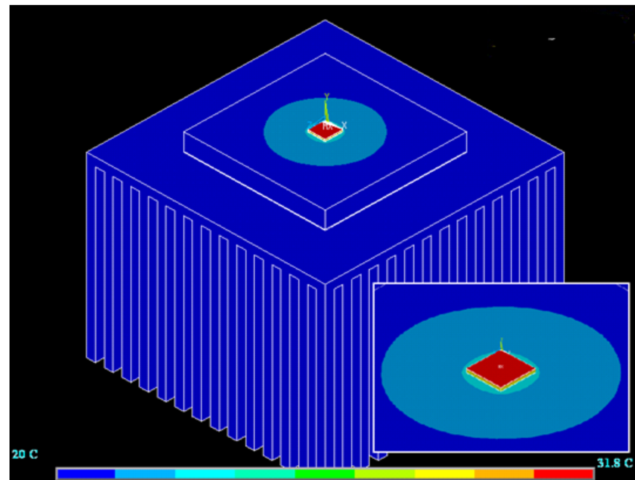


Figure 5.6: Heat dissipation for COP packages attached to heatsinks C at operating power of about 1.5 Watts (~700 mA current). The inset shows the enlarged view of the LED chips the color signifies the heat distribution. The color bars are the scales covering the temperatures from blue (20 ^{o}C) to red (36 ^{o}C).

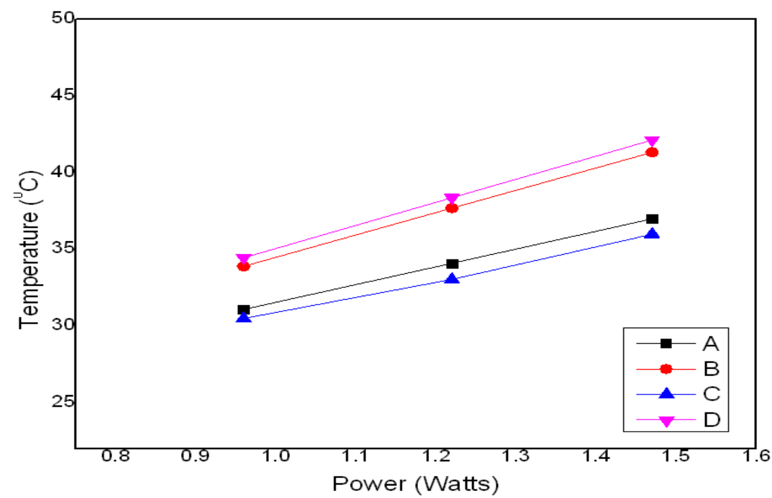


Figure 5.7: FEM junction temperatures as a function of input power (DC driving current) of various COP packages (A, B, C, and D).

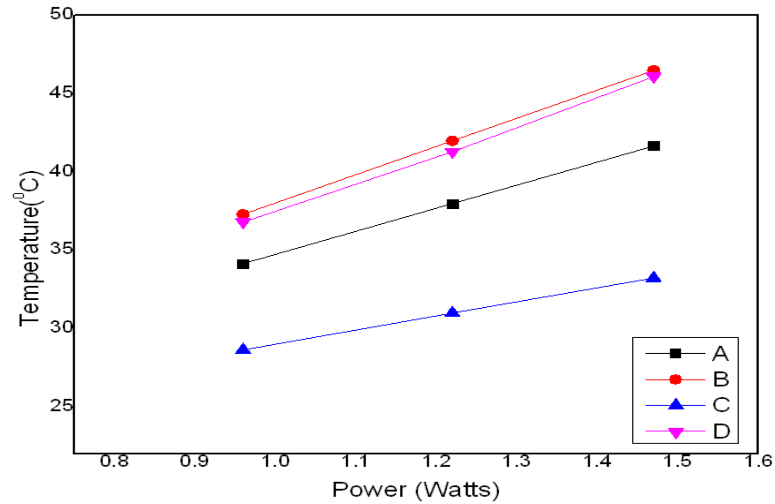


Figure 5.8: TRC junction temperatures as a function of input power (DC driving current) of various COP packages (A, B, C, and D).

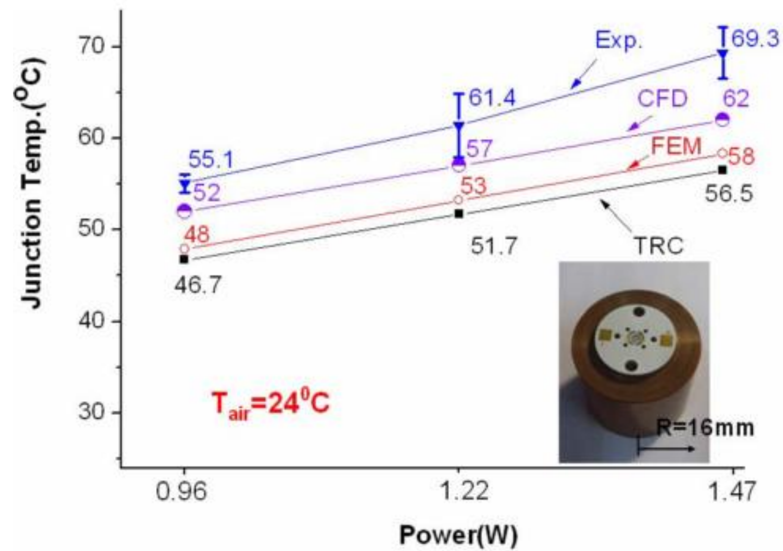


Figure 5.9: "Comparison of junction temperatures of COP LED module, determined from CFD, 2D FEM, TRC, and experiments under various powers (0.96W, 1.22W, 1.47W)" [25]

Results displayed in Figure 5.10 and 5.11 show cross-sectional heat profile through COP packages attached to heatsinks C, and B, respectively. A close examination of the thermal contours will show more uniform heat distribution for heatsink C structure rather than COP structure connected to heatsink B. Another indicator of good heat dissipation is high thermal flux. Numerical calculations were also carried using EFM code to compare heat fulx through the COP packages in the cases of heatsink C, and B., The results are presented in figure 5.12. A good thermally managed package would achieve high heat flux across the structure, thus more heat could be dissipated to the ambient. This study was conducted by choosing a small surface area at the base of a heat-sink for both types of heat-sinks B and C, as those exhibit the poorest and best thermal performance, respectively. These estimates were considered for three different operating powers, i.e., 1, 1.2, and 1.5 Watts, respectively. Examining flux results showed that heatsink C design/structure shows higher thermal flux thus better heat dissipation than heatsink B, which comes in agreement with our previous FEM and TRC findings presented above.

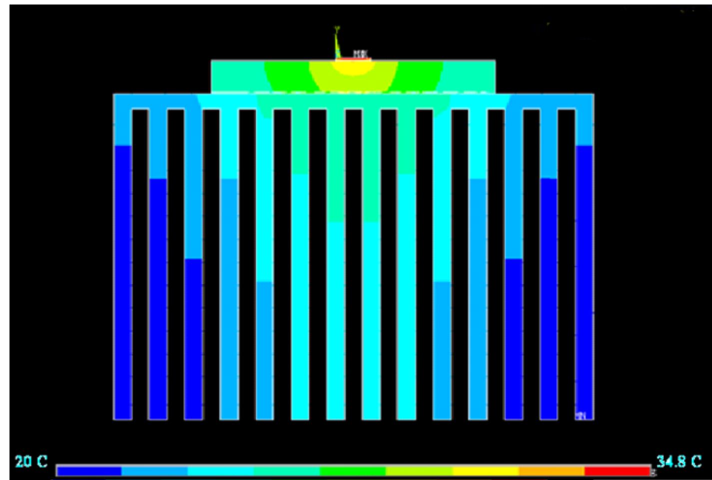


Figure 5.10: Cross-sectional view of Heat distribution in the COP package attached to heat-sink C at 1.5 W operating power that corresponds to 700 mA injected current

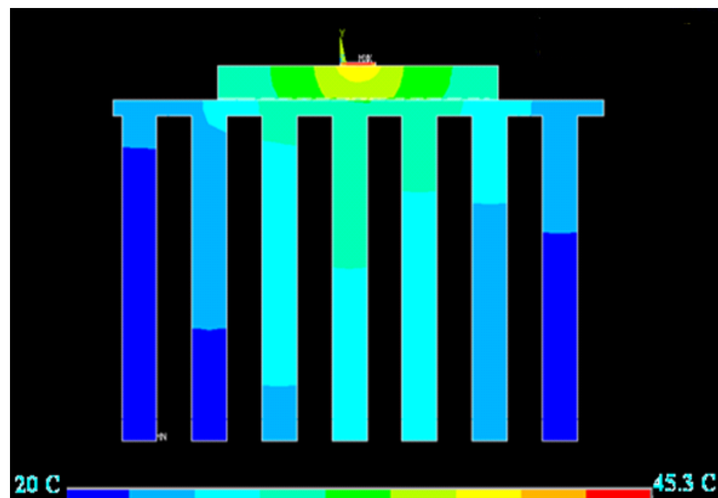


Figure 5.11: Cross-sectional view of Heat distribution in the COP package attached to heat-sink B at 1.5 W operating power that corresponds to 700 mA injected current.

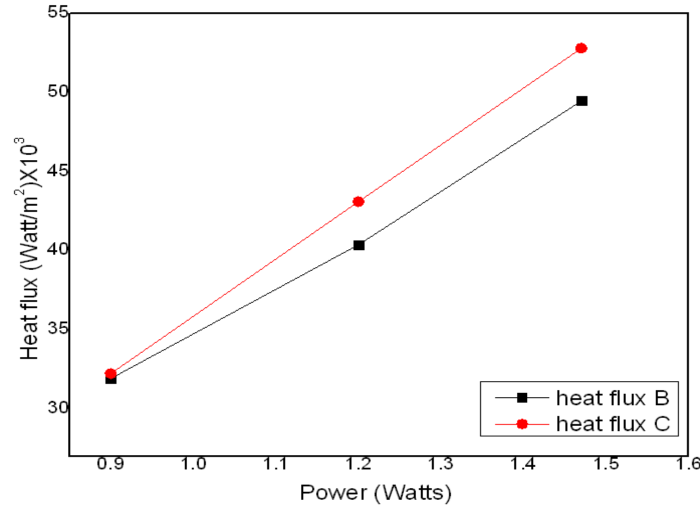


Figure 5.12: Heat flux across two COP packages attached to heat-sinks B (less densely finned plate-fins heat-sink) and C (densely finned pin-fins heatsink).

In order to clearly demonstrate the effect of packaging on device performance, ANSYS13™ was used to model an unpackaged device on 11×11×1 mm^3 mm thickness Sapphire substrate. The unpackaged devices were operated at similar current values as those of the packaged devices above. Junction temperatures were found to be around 124 ^oC at 1.2 W and 149 ^oC at 1.5 W operating powers. Beside the clear reduction in chip temperature, and for further illustration of the importance of packaging, Rsoft LaserMOD™ was employed to simulate and quantify PL intensity and spectrum for package C, and unpackaged devices at similar driving current values. FEM obtained temperature data was included in Rsoft LasreMOD™ simulations to compare the PL emission intensity and spectra between COP packaged device C and the unpackaged devices. Figure 5.13 and 5.14 show the PL results for unpackaged devices and the COP structure C at operating powers of 1.2 and 1.5, respectively.

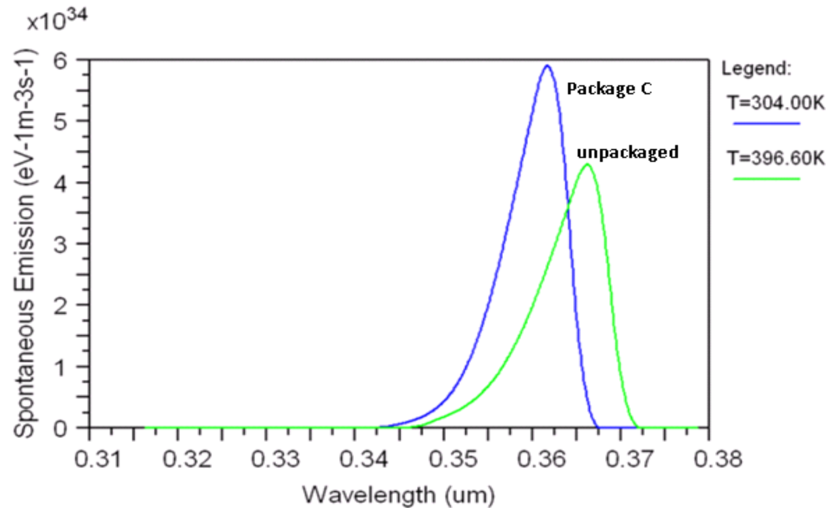


Figure 5.13: Photoluminescence intensity and spectrum for 'package C' and unpackaged AlGaN/GaN high power LED device at different operating power values at 1.2 W

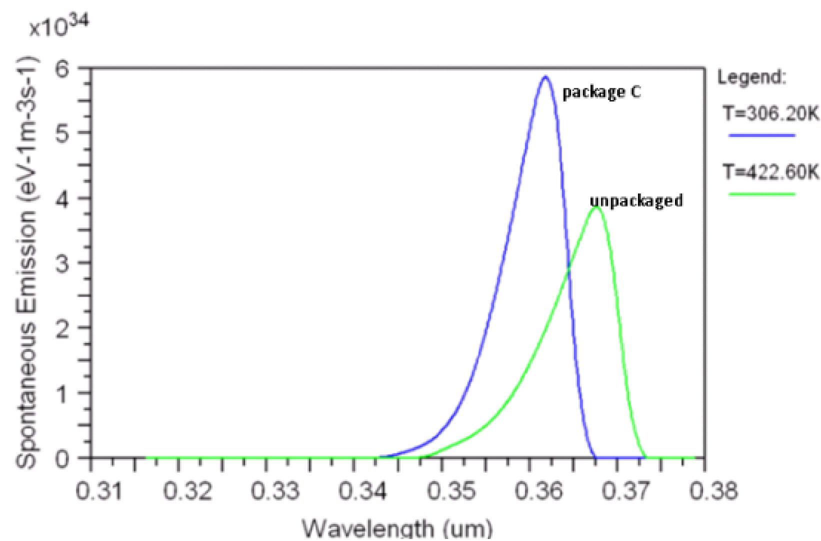


Figure 5.14 PL intensity and spectrum for package C and unpackaged AlGaN/GaN high power LED device at different operating power values at 1.5 W.

Results presented above show the major effects of COP packaging on the device performance. The higher junction temperature of the unpackaged device led to a red shift of ~ 7 nm at 1.5 W, which might be acceptable for lighting applications but it also caused a vivid 30% drop in the output intensity which is of great concern in SSL. Experimental

data is in agreement with our multi-software simulations. A. Poppe et. al experimentally tested the temperature dependence of the output of LED devices [57]. In their work, Poppe tested 7 different LED devices at different driving currents; his findings are shown in figure 5.15. Considering that the devices modeled in our simulation are high power, it is more suitable to compare our findings to Poppe's high-forward-current experimental results. A close look at figure 5.15 shows similar behavior to the one predicted by our simulations featuring a drop in the output power as device temperature rises. Furthermore, it can be realized that the drop of output power of the brightest LED (G2500) is between 800 to 575 lm which is about 28.5% and this comes in nice agreement with our reported above 30%.

High quality COP packaging helped to decrease the junction temperature canceled the red shift and improved the output intensity. This research helps determine the effects of each packaging option on the device and contributed to optimize and pick the lowest cost package that can keep the junction temperature and device performance at the acceptable limits.

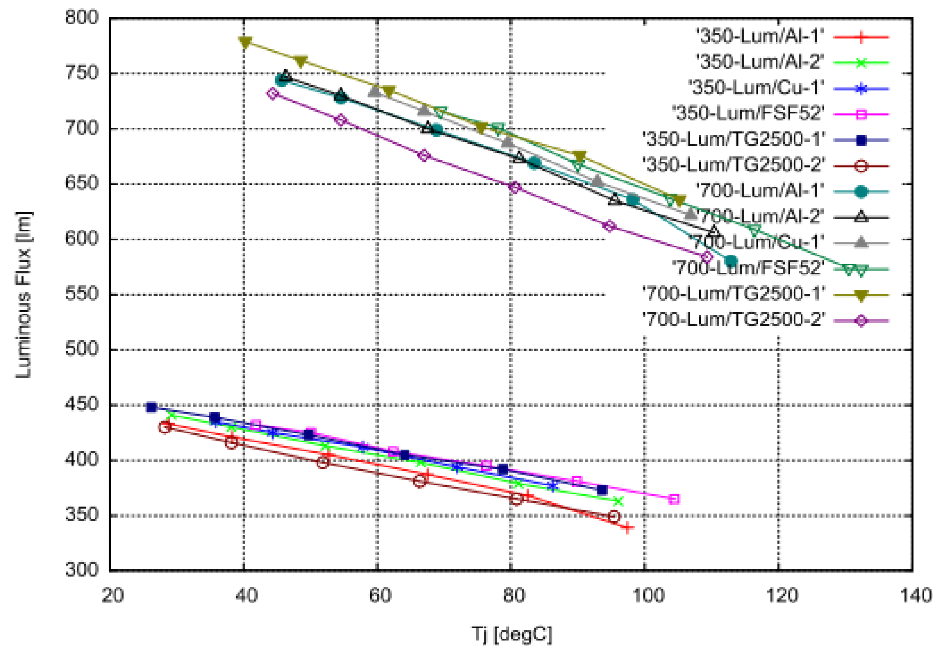


Figure 5.15: "Luminous flux plots of 7 different sample devices of Cree Xlamp MCE1 series of white LEDs as function of junction temperature at 350 mA (bottom plots) and 700 mA (top plots) forward currents" [57]

5.6 Summary

Chapter 5 combines all the work presented in the previous chapters 3, and 4. It presents thermal analysis of a complete package; the novel COP package designs were adopted for high power GaN/AlGaN UV LED chips for SSL applications. The thermal analysis went side by side with heatsink design study, as four different heatsinks representing two major heatsink types were modeled and simulated for different operating powers (i.e., driving currents). A thermal resistance circuit (i.e.,TRC) mathematical model was also employed to calculate the packaged devices chip temperatures to corroborate our simulated results. A careful study of all major thermal

paths was carried out before designing the TRC model. Comparative study of the results of both FEM and TRC showed that the achieved results were in good agreement at multiple operating power values ranging from 1 to 1.5 W. It was found that T_j was ~34^oC at an operating power of ~1.50 watts (about700 mA corresponding driving current) for the case of densely finned pin-fin heatsink. On the other hand, it was around 46.5^oC for less densely plate-finned heatsink for the similar operating conditions.

Thermal flux comparative study was also carried out between the best and worst performing heatsinks. Results came in good agreement with the thermal profiles and TRC predictions. The effects of packaging techniques on the performance of simulated devices in this study are presented using the variations in PL spectra and intensity of an unpackaged on-wafer device and COP packaged device attached to heatsink C. Results clearly demonstrated the effects of COP packaging on the device performance. Significant improvements in the intensity and spectrum of the packaged device were evident. However, since low-cost is a major interest and motivation of this study, we believe that the proposed method could be more effective when maximum acceptable junction temperature values are known. Therefore, low-cost heatsink designs could be optimized to keep junction temperatures at highest acceptable values. Additionally, the findings and results can be easily extended and adapted for the low-cost packaging of deep-UV LEDs and other devices. This work would also be extendable using our COP packaging design and methods incorporating various emerging interfacial materials e.g., carbon nano-tubes and suspended graphene films heat spreaders as will be discussed later. In the next chapter the research and development would be extended a step further. In the chapter six the concept of COP packaging is extended to multiple LED

assemblies for SSL applications. Mutual interaction effects between assembly elements (devices) are studied and evaluated along with analytical study of thermal stability and solutions to improve thermal uniformity of such assemblies.

CHAPTER VI: HIGH POWER LED ASSEMBLIES FOR SOILD-STATE LIGHTING

In the previous chapter COP packaging method and analysis was presented. Numerical simulations and analytical TRC calculations were carried out for various high-power LED devices. Different heatsink designs were included in the study. Comparative study of the findings was also presented. Results showed the clear performance advantage of using metal plates as submounts rather than conventional packaging materials (e.g., PCB boards); metals were are also far more cost-efficient in comparison to high quality ceramic based material such as AlN and SiC. The cost benefit is of great importance for the manufacturing and marketing of SSL technology. Solid state lighting employs large number of LED devices in many different arrangements depending on the desired lighting patterns, such multiple assemblies and operation of LED devices; it would give rise to new thermal management challenges that need to be addressed efficiently. In this chapter we extend Chip-on-Plate (COP) packaging concept to three different assemblies of multiple high power LEDs. Resulting thermal effects were estimated through numerical simulations for each design; the impact and severity of these effects on device temperature and performance were evaluated. Thermal resistance circuit (TRC) model and heat diffusion equation were employed in this study of thermal behavior of the assembly elements. Also, the effect of thermal uniformity on the emission spectra was evaluated for different operating powers, which helped to determine the best performing assembly design to reduce the undesirable effects of large assembly operation. Such findings are extremely useful in designing larger area LED light

modules where thermal non-uniformity effects are expected to be more severe on devices' lifetime and efficiency.

6.1 LED Assemblies General Considerations

The typical output of an average LED is about 20%, and the rest 80% goes into heating which presents a further reduction in the output power and the lifetime of SSL modules built using such point sources. As noted earlier, LEDs have a wide range of applications, some use individual devices e.g., short wavelength optical communication, chemical sensing, However, solid state lighting (SSL), require large assemblies of LEDs to produce similar or yet higher light intensity than conventional light sources [58-59].

In some cases array of LEDs are combined and integrated together in different assemblies to achieve desired levels of optical flux densities. However, incorporation of thermal management becomes a necessity to reach optimal performance of the design lighting modules in terms of their chip temperature, color purity, and color rendering index (CRI). This results in stable light output, spectral stability and longer lifetime. These improvements would ensure efficient, durable, and cost-efficient light sources, thus help to decrease the transition time needed to complete the transition from conventional light sources to next generation SSL technology [24]. When array type LED assemblies are designed, it is essential that all chips produce nearly similar light output and similar lifetime, these requirements can be met if all the array elements have similar thermal behavior. Similar individual devices attached to similar packaging designs are expected to have almost identical thermal performance, however, when arranged in one assembly new thermal conditions results in different thermal responses for the assembly elements. For the better understanding and evaluation of assembly performance, we

introduce thermal uniformity among various elements of the assembly as a method to evaluate array thermal stability. Generally, thermal uniformity is obtained by mapping the overall device's temperature profile over the entire assembly elements and calculating the maximum temperature difference between them. A high temperature difference would be an indicator of the poor thermal uniformity; whereas low temperature difference implies high thermal uniformity.

For this study multiple COP packaged LED devices were considered to be integrated in one assembly for SSL [25]. Considering that COP is one of the most recent packaging techniques, it was useful to study the thermal behavior of several COP packages when attached to one heatsink. AlGaN/GaN based devices with an operating power between 0.2-1.25 W (same considered in chapter IV) were chosen to design the multiple LED light modules. Figure 6.1shows the basic design of individual assembly elements (devices) used in this study and its COP packaging dimensions.

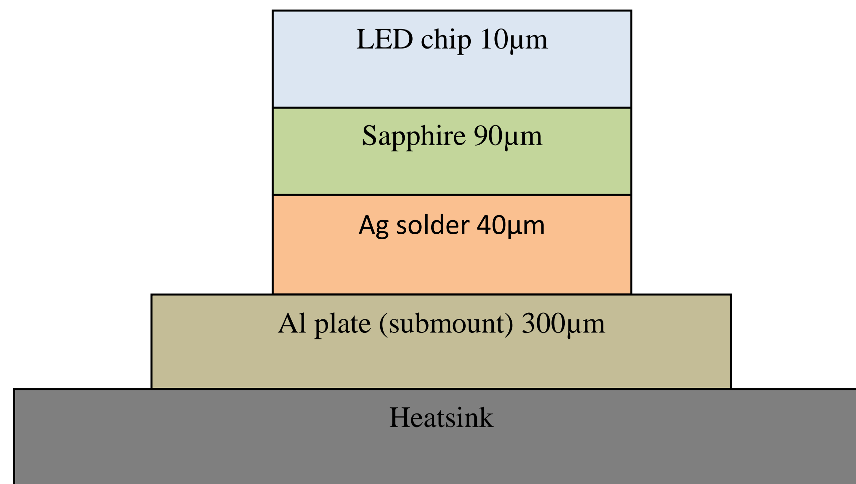


Figure 6.1: Cross-sectional view of COP LED package (not to the scale) and typical thicknesses of layers are denoted.

6.2 LED Assembly's Thermal Uniformity Analysis

As mentioned in previous chapters SSL technology aims to replace all conventional light sources with LED based light modules in order to generate similar and even higher optical output, multiple LEDs arrays have to be put in a single module (typical LED lamp may contain up to 20 devices or more). So far we have presented thermal analysis and packaging techniques for individual devices; however, thermal behavior of these LED chips when assembled together is essential in designing SSL solutions. In this part of the research, COP packaged device were chosen to be the building blocks of the intended lighting modules. Our lighting modules, in brief consist of 12- to-24 COP packaged LEDs attached to common heatsink. Thermal grease is used to fix the COP chips on the heatsink. Standard plate-fin copper heatsink of 1-cm in length and 1mm thickness were the heatsink of choice due to their high thermal conductivity and cost-effectiveness [62]. The packaging material selection is essential for good thermal performance and the assembly thermal stability [61]. High quantum efficiency of the devices will ensure high brightness output, taking into consideration limited light extraction efficiency of LED devices [62].

The understanding of thermal behavior of LEDs in an assembly can be realized not only considering the individual thermal behavior of each element, but also the mutual effects among the elements as well. Individual thermal behavior of assembly elements is best described using TRC model. As operating power dissipates through LED chips, heat is generated. Most heat spreads in vertical direction from the junction layer through the heatsink. However, heat is dissipated in the horizontal directions as well. Simplified thermal paths of individual COP LED device are shown in figure 6.2. It is

evident that the main thermal path is vertical from chip to heatsink; however, for simplicity it is feasible to consider that each thermal path has four horizontal channels branching at the base of the heatsink.

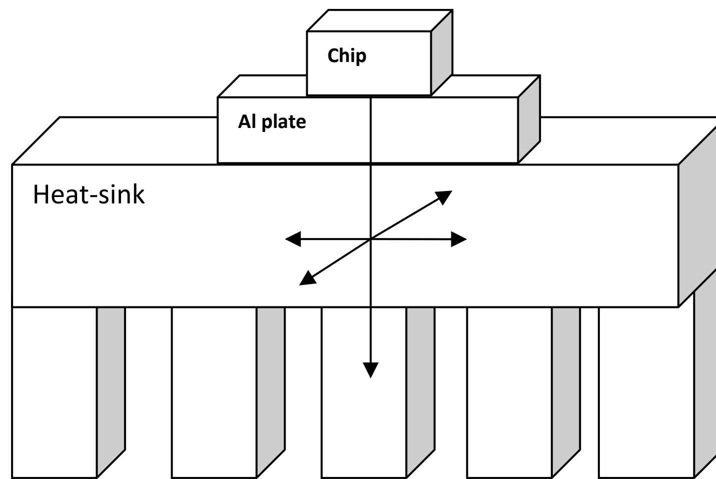


Figure 6.2: Thermal paths for one LED assembly element [ref]

Thermal resistance and thermal mass varies over each path depending on the material layers it includes and the path dimensions, thus different thermal paths would introduce different thermal resistance/thermal mass values in the TRC of each element [51]. For individually packaged devices symmetry limits these differences, whereas for multiple LED assemblies the location of each element results in different horizontal thermal paths, which leads to different thermal resistance values and chip temperature.

Figure 6.3 displays an example of how element location affects their TRC. Inner elements would have longer more uniform horizontal thermal paths rather than outer elements which are closer to the edge of the heatsink. This will give inner chips more thermal mass underneath them and increase their heat dissipation capabilities. It results in different elements having different total thermal resistances, considering identical devices and operating power levels, it is expected to observe different chip temperatures for different elements of the same assembly.

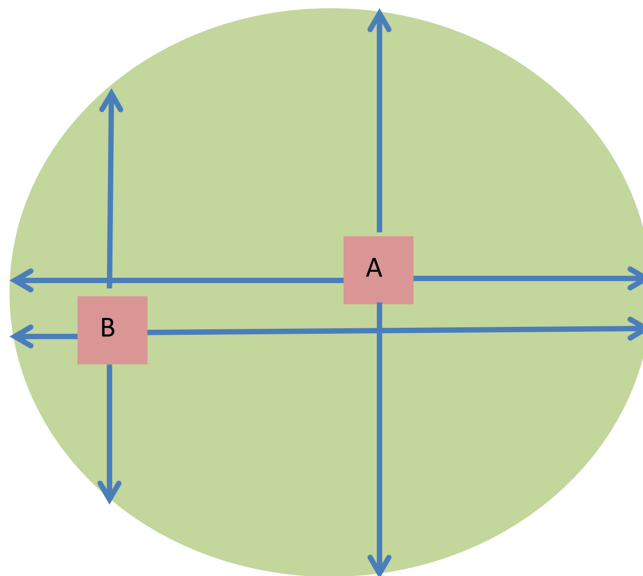


Figure 6.3: Top view of an LED assembly showing horizontal thermal paths for elements A and B; shorter thermal paths for element B indicates less thermal mass and higher thermal resistance in comparison to element A

Mutual effects among elements play essential part in the final heat distribution and thermal stability of the assembly. These mutual effects can be understood by employing heat diffusion equation to the assembly and solving it at the plane of the heatsink base. The heat diffusion equation (1) can be expressed as discussed in reference [29]:

$$\frac{\partial \mathrm{T(r,t)}}{\partial \mathrm{t}} - \frac{K}{\sigma\rho} . \nabla^2 T(r,t) = 0 \qquad (6.1)$$

Where T(r,t) is the temperature distribution over position and time, K is thermal conductivity, σ is specific heat, and ρ is density of material. The solution of such equation is obtained through separation of variables method and involves Fourier series and selected boundary conditions. Considering that thermal paths are through bulk material (heatsink material) and assuming the absence of heat source limit the problem to steady state initial conditions problem that equation 6.1 can be written as1D Laplace equation:

$$\nabla^2 T(x,t) = 0 \qquad (6.2)$$

The solution of equation 6.2 is given as:

$$T(x,t) = A.x + B \qquad (6.3)$$

Where A, and B are constants that are calculated based on the boundary conditions. The solution shows the impact of the element location on the thermal behavior; shorter thermal paths lead to less thermal diffusion efficiency and higher element temperature. Constant B in equation 6.3 is initial temperature dependent, i.e., in other words, it represents the effect of the neighboring elements. Having high initial temperature in the surrounding perimeter of an assembly element, would decrease the amount of heat dissipated from the element to the heatsink. Therefore, elements arrangement and positions have to be designed to unify initial temperature for all elements in order to achieve uniform heat dissipation and conserve thermal stability. Non-uniform thermal behavior, if increased, will create instability in output power and emission spectrum among the assembly elements. Based on the analysis presented above, one may come to the conclusion that such undesired effects can be suppressed by increasing the symmetry and uniformity of the assembly. Uniform arrangement that maintains almost constant element per unit area (element density) creates relatively equal horizontal thermal paths and provides almost similar thermal mass for each element. Such conditions would create homogenous boundary conditions and initial temperature values for all elements, thus would permits relatively similar heat diffusion capabilities for assembly elements and results in high thermal uniformity.

6.3 Light Modules Modeling

Numerical modeling was employed to support the findings of analytical study of packaging assemblies thermal uniformity presented above. Different assemblies were designed and modeled using ANSYS 13^{TM} finite element code, steady-state thermal analysis was carried out to observe devices temperature and evaluate thermal uniformity. Each design consisted of multiple devices/element attached to one general heatsink. The unit assembly element was chosen to be AlGaN/GaN high-power LED with die size 0.5×0.5 mm^2 each device is COP packaged using Al plate 1 mm thick. These devices were considered to design three different lighting-modules in order to study the degree of thermal uniformity for different device distribution [24]. A comparative study was also carried out to investigate the effects of design and element distribution on thermal uniformity and performance element arrangement for corresponding chips temperature, emission spectra and output. Three type lighting-modules/assemblies were modeled in this study. The first module design (A) consists of 12 elements organized in radial symmetry, and spread over a 1cm radius cylindrical plate-fin heatsink of 1cm fin length and 1mm thickness. The second design (B) is an extension of the first design with total of 24 LED chips attached to a bigger cylindrical plate-fin heat-sink of similar fin dimensions to design (A). The third module design (C) is a 12-element rectangular-distribution assembly with constant element per-unit area density attached to a rectangular plate-fin heatsink; it was ensured that all assemblies have similar fin dimensions for the accuracy of the results comparative study. All three assemblies were ‘modeled and meshed’ carefully with special attention to the chip-heatsink contact regions for consistency. Design (B) was modeled using only half domain of the structure.

This method can be used based on symmetry in order to minimize the processing time and to overcome those limitations linked with the use of the FEM analyzer. Modeled assemblies/lighting modules and their meshed structures are presented in figures 6.4 and 6.5, respectively.

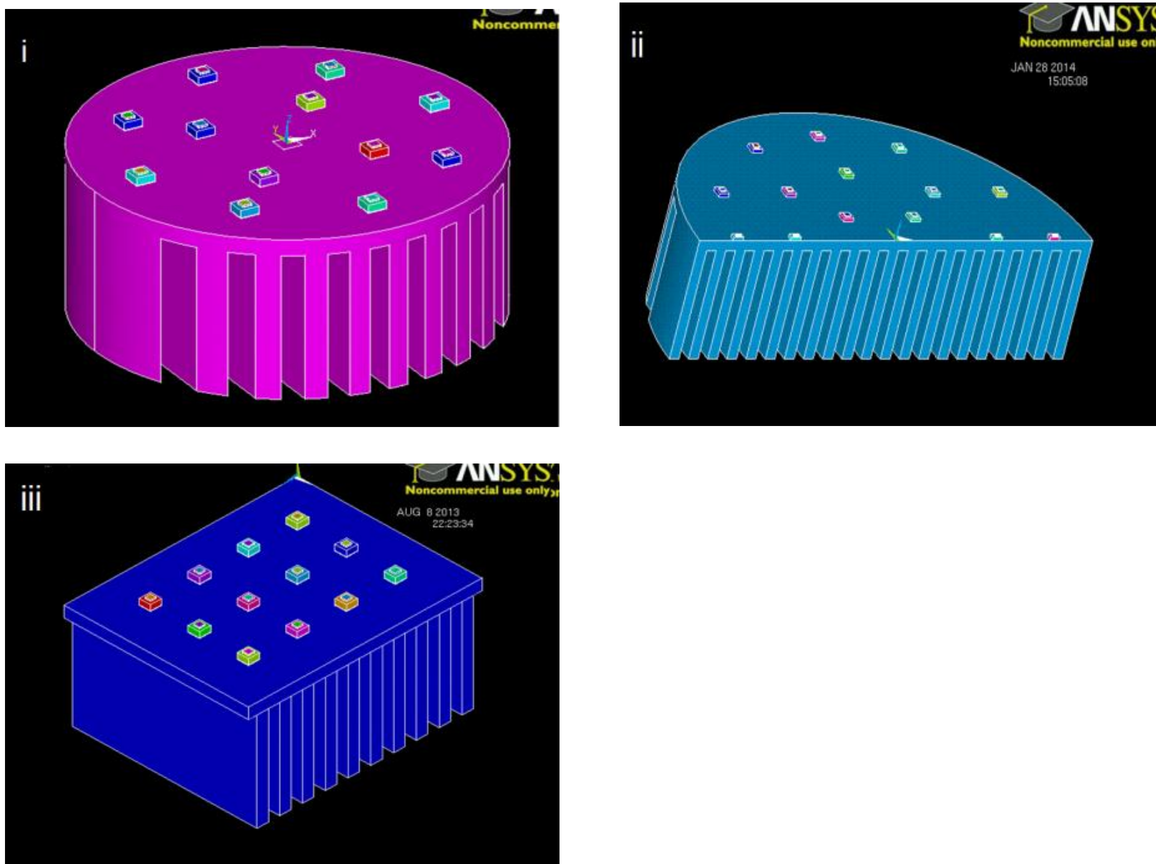


Figure 6.4: 3D models of different LED assemblies/modules. (i) Lighting-module (A), (ii) Lighting-module (B), and (iii) Lighting-module (C)

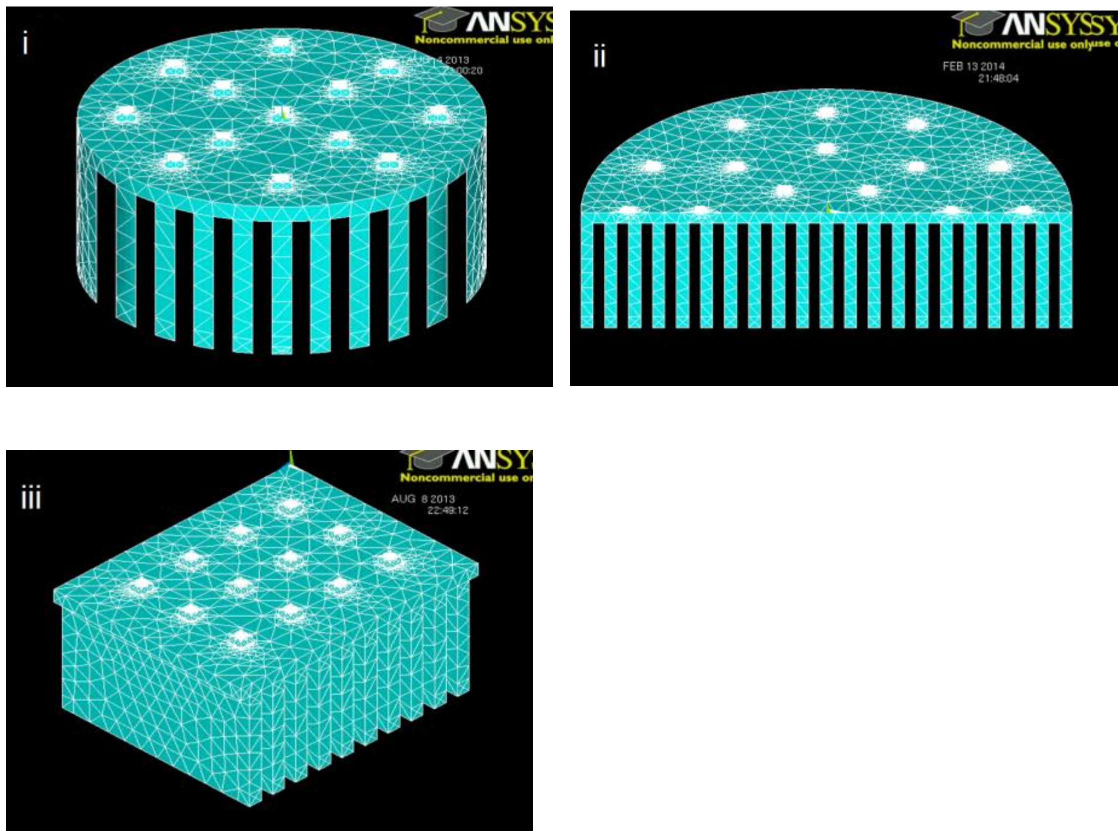


Figure. 6.5: 3D 'meshed models' of different LED assemblies. (i) Module/Assembly (A), (ii) Module/Assembly (B), and (iii) Module/Assembly (C)

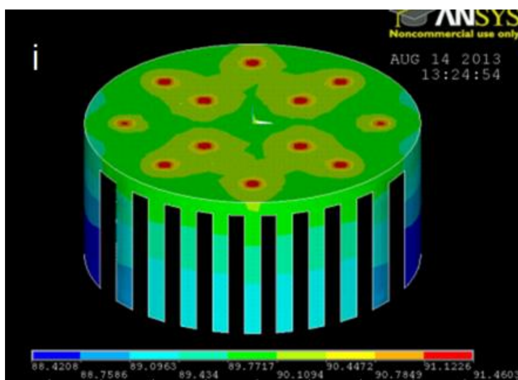
All lighting modules/assemblies were simulated using similar set of operating power values ranging from 0.25 W to 1.25 W. Thermal conduction and convection were both considered; thermal loads were carefully applied to each surface and interface to create real-time thermal behavior. Steady-state thermal analysis resulting temperature profiles of were used to determine the maximum temperature difference between the elements of each module/assembly at various operating powers. The comparative study followed was designed to show which of the structure achieved better thermal uniformity.

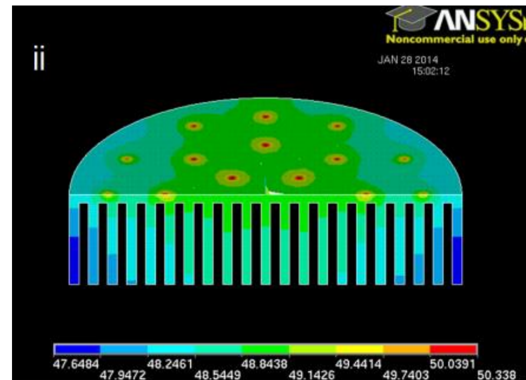
As discussed in previous chapters, heat has adverse effects of the output intensity and spectrum of LED devices. Therefore, in addition to the temperature contrast calculations, emission spectrum and output intensity comparative study was also carried out using temperature contrast data collected from thermal analysis. For SSL applications spectral purity is not the main concern especially for small spectrum shifts, however, output power level is vital for uniform performance and relatively similar elements lifetimes [61]. These calculations were carried out using Rsoft LaserMOD™ numerical photonics simulator. Results were used in an output comparative study for each light module at various operating power levels.

6.4 Results and Discussion

Results of steady-state thermal analysis for all the structures considered at multiple power levels show that chips temperature contrast is related to the elements layout and arrangements. It was found that more uniform and constant element-per-area distributions yield relatively lower temperature difference between the assembly elements. For 1.25 W, assembly (A) showed the highest temperature contrast of 7 ^{o}C whereas for the case of assembly (C) which has almost constant element-per-area density showed lowest temperature contrast value of ~ 0.7 ^{o}C. Whereas, assembly (B) which has relatively more uniform element distribution compared to (A) showed less temperature difference between its elements with a value of 4.5 ^{o}C at 1.25 W. The temperature difference calculated in these simulations is different from the chip temperature we usually focus on ΔT represents the max temperature change among assembly elements. Figure 6. 6 shows the temperature profiles in the heatsink for assemblies (A), (B), and (C) at operating power of 1.25 W a function of input power. Heat distribution contours can

also be used to investigate heat dissipation capabilities of each assembly. It can be seen that assembly (B)'s contours are the most uniform which is sign that its elements have almost the same temperature. Assemblies (A) and (B) show less uniform thermal behavior which is an evident of temperature difference between elements. These findings are in agreement with our theoretical predictions. The same simulations were conducted for all the structures at multiple operating power values. Element temperature difference was plotted as a function of input power values and results are presented in figure 6.7. Results show consistency and were in agreement with our initial findings, it is evident that ΔT increases as the operating power increases, however, it is evident that assembly with more constant element per area density will have minimum temperature difference among its elements





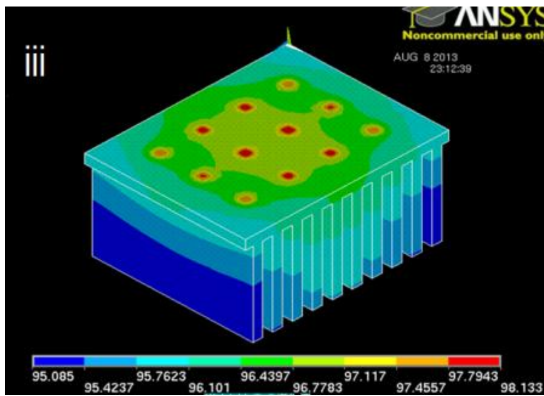


Figure. 6.6: Temperature contours in heatsink at 1.25 W operating power (i) assembly (A), (ii) assembly (B), (iii) assembly (C) it can be seen by comparison that heatsink (B) has more uniform contours, which indicates better thermal uniformity

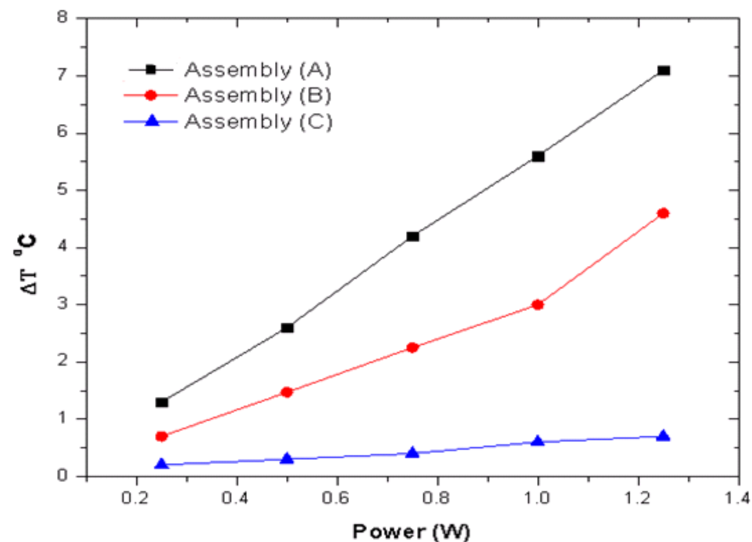


Figure 6.7: Chip temperature difference ΔT of assemblies (A), (B), and (C) at different operating powers

Our interest in elements temperature difference is based on the fact that element temperature has a direct impact on the emission spectrum and output power.

In order to appreciate these effects, RSoft LaserMOD™ was utilized to

investigate the changes in the emission spectrum and output intensity among assembly elements. All the three light modules considered in this research consisted of similar devices. Since thermal analysis shows that elements temperature difference increases with operating power and/or the number of elements, it was better to conduct this part of the study at the maximum operating power possible (2 W). Such elevated power value applied to structure (A) will result in maximum element temperature of 142 ^{o}C and a minimum element temperature of 127 ^{o}C this corresponds to 15 ^{o}C ΔT, however similar operating power level resulted in 1 ^{o}C ΔT for assembly (C). These temperature values were used in RSoft LasreMOD^{TM} simulations to see valuate the difference in the emission spectrum and output of the assembly elements. Selected Results are plotted in figures 6.8 and 6.9, respectively. By examining the results it can be noticed that high ΔT this difference resulted in over 2 nm red shift and 4% intensity. Even though the spectral change is small and might not be of great importance for SSL applications, intensity drop is a serious concern. And it is predicted to increase as the number of elements increase for larger assemblies this may lead to intensity degradation and different lifetimes of elements. On the other hand, small ΔT value for assembly (C) kept the emission spectra stable with no significant changes in both wavelength and output intensity. This output stability in (C) would ensure better performance and longer lifetime of the assembly and makes the rectangular design with uniform element distribution the best option of the three investigated.

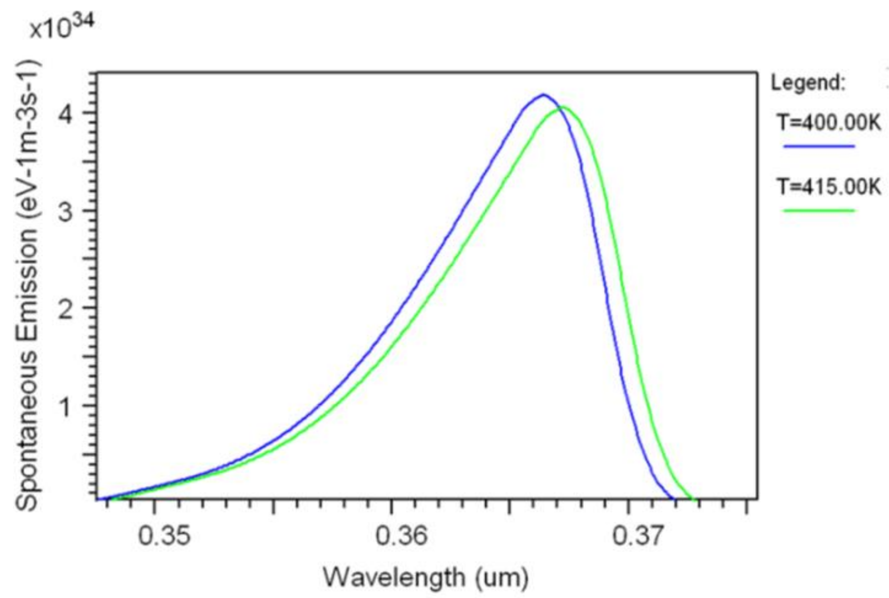


Figure 6.8. PL emission spectrum for min/max temperature elements of assembly (A) at 2 W

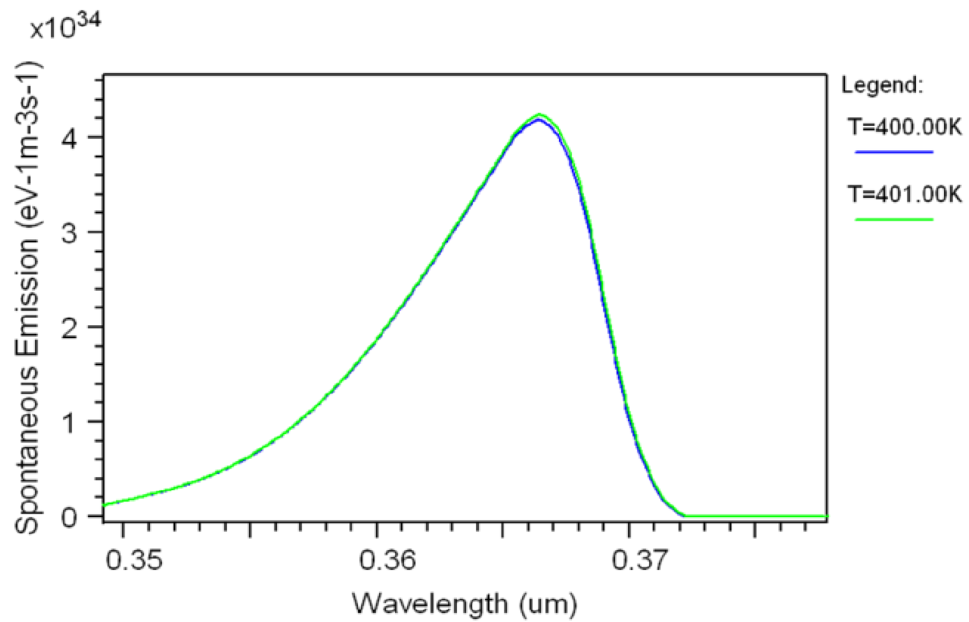


Figure 6.9. PL emission spectrum for min/max temperature elements of assembly (C) at 2W

6.5 Summary

In this chapter, we presented an analytical study of thermal behavior of LED assemblies used in SSL applications. This study was the natural progression of our packaging techniques research and a direct generalization of COP concept studied in previous chapter. Analytical study based on TRC and heat diffusion equation showed that temperature contrast among assembly elements. That can be decreased by increasing the symmetry of the assembly using uniform element per area designs as that in assembly (C). Three different assemblies showing different degrees of symmetry were modeled using ANSYS13^{TM} and simulation results are in agreement with our theoretical predictions. Suggested rectangular assembly (C) design showed much improvement in thermal uniformity rather than the two circular assemblies also considered. Results showed that there is a temperature difference among LED chips in each assembly. Furthermore, temperature contrast was found to be an order of magnitude higher in the circular assembly than that of the rectangular one. Results were consistent over a range of operating power levels. Moreover, the impact of these findings on the emission spectra was studied and employed in a comparative study. Those clearly show the effects of thermal non-uniformity on small red-shift and intensity drop observed in assembly with less uniformity, while it is unnoticeable in the assemblies with high thermal uniformity. We believe that this study provides a better understanding of the thermal behavior of LED assemblies and would be of significance designing much large-number LED chip-assemblies and subsystems in lighting systems for various applications.

CHAPTER 7: NOVEL GRAPHENE HEAT SPREADERS FOR MIRCO LED ARRAYS

This research extension was aimed to the improvement of thermal management of semiconductor light sources packaging. Throughout this work, we explored different packaging aspects and concerns ranging from on-wafer- to fully packaged-devices. Various packaging materials and techniques were considered for the purpose of improving device-packages' heat dissipation and thermal stability. In this chapter not only the potential of a new and promising packaging material is presented, but also a novel addition to conventional packages. Recently, discovered 2D Carbon structures (Graphene) show exceptionally interesting thermal properties including very high thermal conductivity, which provides such materials high potential for heat dissipation in photonics/electronics applications.

The implementation of such materials and structures (of graphene) in conventional LED/LD packaging has certain challenges due to their growth and size limitations. Again, thermal resistance circuit (TRC) was employed to explore the best method of implementation of these 2-d materials in photonics packaging. A brief overview on Graphene structures and thermal properties is presented in the first section of this chapter. The second section presents the modeling and simulation of heat dissipation in LED packages with Graphene heat spreader as a proof of concept. Based on our early findings, Graphene structures were introduced into micro-LED arrays used for optical communications. In the fourth section of this chapter, several arrays were modeled and simulated with different Graphene structures embedded within the array

package. Results and comparative study are presented in section five to display the significance and advantage of 2D Carbon structure in the packaging of solid-state light modules.

7.1 Graphene's Thermal Properties and Heat Spreaders Potential

In our research for the enhancement of thermal management of solid-state light emitters, it was evident that packaging designs and materials play an essential role in their thermal management. Thermal packages ensure the heat removal from the junction layer of the devices to the ambient through efficient heatsinks. It is imperative that packaging materials should be low-cost and selected carefully such that they offer the high quality thermal properties. The shape and the size of the heatsink determine the heat exchange rate with the ambient. This was discussed in somewhat detail in chapter 5.

Based on thermal resistance circuit model (TRC), presented in chapter 2 it is evident that creating additional thermal paths within the packaging structures introduces desired effects. That includes a decrease in the total thermal resistance of these packages which results in enhanced heat dissipation and lower device temperature [63]. An optimized additional thermal paths using high thermal conductivity material would introduce low thermal resistance in parallel with the basic thermal circuit of the package. Examining all packaging designs and models considered in this research, we found that this concept can be best realized by adding heat spreaders to the top surface of the LED/LD devices that remove heat directly from the device into the main heatsink (or an additional heatsink). However, this technique would require materials with high quality thermal properties to ensure its effectiveness.

Nano-structured Carbon materials have gained an increased interest in photonics

and electronics industry due to their unique electrical and thermal properties. Carbon based materials such as diamond and one-dimensional carbon nano-tubes (CNT) have been considered in this research as packaging materials for LD packages earlier in chapter 4 to optimize thermal interfacial materials (TIM) and submounts [64]. Carbon structures show drastic changes in thermal and electrical properties as their size and shape becomes smaller and smaller [65-66]. This leads to a wide range of values and various thermal behaviors. The most vital property for this study is thermal conductivity. Carbon shows a wide change of thermal conductivity ranges from ~0.01 W/mK in bulk carbon to above 2,000 W/mK at room temperature in diamond or graphene. 2D Carbon structures, like Graphite and Few-Layer Graphene (FLG), have very interesting thermal properties at room temperature, especially high thermal conductivity up to 2500 W/mk [67-68]. Such exceptional properties are due high phonon confinement in their 1D and 2D atomic systems [69]. This makes FLG material of choice to exploit the concept of heat spreaders. We expect that the introduction of these materials in III-nitrides light sources packaging will evidently improve their thermal management and stability. Graphene sheets are produced by various methods, sizes and thickness [70]. The use of these structures (Graphene quilts) have been directed to create nano-scale Graphene flakes that can be mixed with different metallic based alloys to create improved TIM that are used for die attaching [71]. FLG exfoliation on top of PMMA presented by Balandin et al [72] enables the fabrication and deposition of larger sheets of FLG (up to 10×10 μm^2). These sizes of Graphene quilts will make the use of graphene as heat spreaders possible. This concept was carried out and employed for the thermal management of microelectronics, especially GaN based field-effect transistors (FETs) [73-78].In this

chapter, we are extending this concept and the use of graphene for photonics thermal management and solid-state III-Nitride light emitters.

7.2 Proof-of-Concept Package Modeling

Based on the discussion presented above, Graphene-based heat spreaders can increase heat dissipation from the junction region of LED/LD devices, thus enhance thermal stability and output. As a proof of concept, we modeled a COP packaged LED with a chip size of 0.5×0.5 mm^2, device structure and dimensions are similar to the devices described in chapter 5. LED device was placed on Al plate and attached by thermal grease to simple rectangular Cu heatsink. Based on these device dimensions Graphene heat spreaders modeled were 1× 2 mm^2 with a thickness on 50 nm, such dimensions are too large for stable uniform quilt growth and mechanical stability. However they can be applied in this case due to the fact that quilts and device dimension have to be relatively comparable, and this modeling is designed merely as a proof of concept. The two quilts were suspended between the top surface of the device and two metallic bumps deposited on the top surface of the Al plate. Graphene quilts are in contact with 40% of the device top surface area as illustrated in figure 7.1

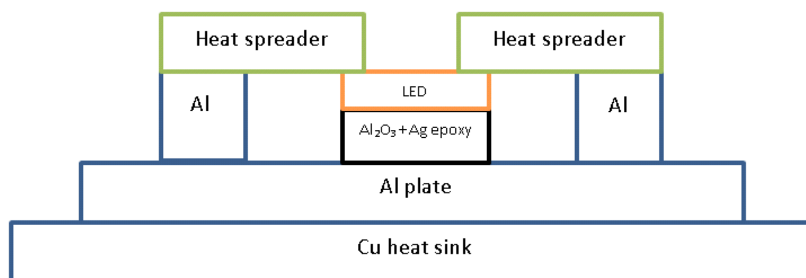


Figure 7.1cross-sectional view of large area COP LED package with Graphene heat spreaders (not to scale)

A reference structure without heat spreaders was also modeled for the sake of performance comparative study. Both structures were simulated at the same operating power levels of 2 W. Results showed that reference structure device temperature was about 91 ^{o}C at 2 W power, whereas the device temperature was estimated to be 88 ^{o}C for the Graphene modified structure as illustrated in figure 7.2.

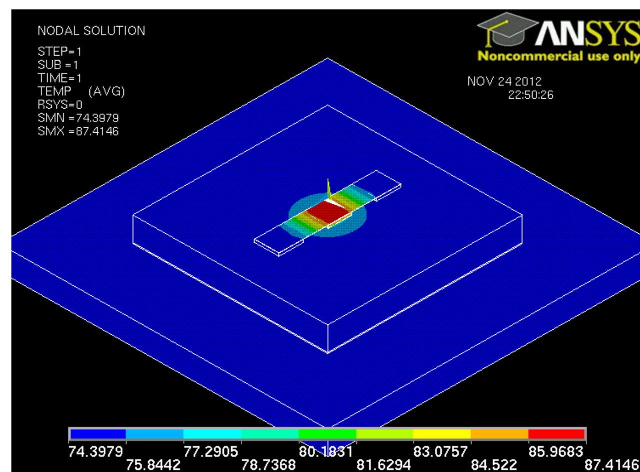


Figure 7.2 : Temperature distribution in Graphene quilts-modified COP package structure at 2W operating power

Preliminary results showed a small decrease in the device temperature up to 1.6 ^{o}C at 2 W power level. The calculated difference was relatively small but still showed that horizontal thermal heat-spreaders increased heat dissipation and resulted in a lower

device temperature. Further drop in the device temperature (up to 4 ^{o}C) was estimated by increasing the power level and increased the contact area between heat spreaders and the top surface of the LED device.

These results although consistent, were not applicable practically due to the large size of the Graphene quilts, and were not of great significance for thermal stability or cost-effectiveness. The challenge was to find an applicable configuration to implement realistic-size Graphene heat spreaders and obtain significant drops in the device temperature. Based on the successful implementation of FLG heat spreaders for FET transistors [72] and our proof of concept modeling, it was suitable to introduce such heat spreaders to micro-LED packages. The small dimensions of these devices make them suitable for the implementation of Graphene heat spreaders and ensure that the resultant device temperature drop will be significant.

7.3 Graphene Heat spreaders for micro-LED arrays

The promising results of using Graphene heat spreaders reported in literature [72] was the motivation for this work to introduce them in photonic device packaging. The size and dimensions of the Graphene quilts available recently are too small to be implemented in most of SSL LED packages due to their relatively large sizes ~1 mm^{2}chips, it can be seen that the effects of Graphene heat spreaders are not of great significance for regular LED chips., On the other hand, micro-LED devices present a promising opportunity due to their comparable dimensions [79-83]. Micro-LED devices have gained more interest, recently and were used in many applications. These devices are increasingly used in flat screen displays and compact optical systems such as video headsets, HD LED TVs [84]. However, micro-LEDs are mostly useful in fiber optic

communications networks as well. The small compact size of these devices makes them very suitable for light coupling into single mode and multi-mode fibers; surface area matching lowers light coupling losses. The integration of micro-lenses on the top surface of the micro-LED devices produces collimated beams and enhances into-fiber light launching [85-88]. Since the typical surface area of such devices ranges from $10\mu^2$ to $40\mu^2$; they are found to be suitable for the implementation of Graphene heat spreaders. In this study, an array of staggered 10 micro-LED for visible-light multi-channel communication system was considered for modeling and thermal analysis. As mentioned earlier, the size of micro-LEDs array is suitable for integration with optical fiber array bundles, enables multiple optical channels transmission simultaneously, bandwidth can be enlarged simply by increasing the number of micro-pixels and fibers in the bundle.

Devices considered in this study are on InGaN/GaN multi-quantum well LEDs, with peak emission wavelength of 470 nm [89]. The devices are shaped as concentric disks with 2.5 µm thickness for the n-region and 1µm thickness for the p-region., Figure 7.3 shows the diagram and dimensions of one array element.

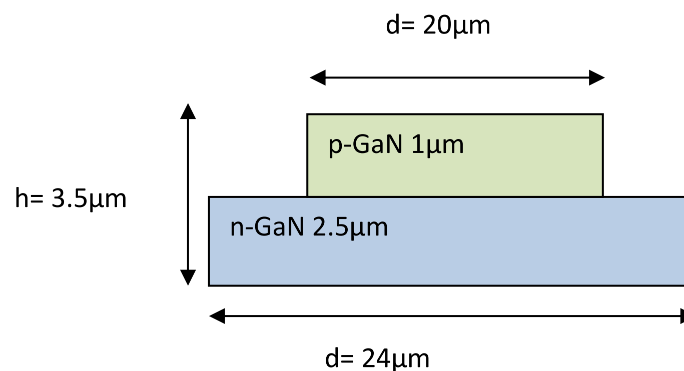


Figure 7.3: The shape and dimension of a LED an element in Array

7.4 Micro-LED Array Structure Modeling

In the case studied, ten devices were arranged in two staggered rows for optical communication applications. In-row devices center-to-center spacing was 125 μm. Devices were fabricated as 600×600×100 μm^3 on sapphire substrate. Operating power for such devise ranges from 2 to 5 mW based on the I-V characteristics given in literature. Substrate can then be attached to all packaging layers such as submount, and heatsink integrated to optical component or module [90].

In order to investigate the impact of Graphene heat spreaders ANSYS13™ finite element analysis module was employed. This study was conducted as follows; three different arrays-packages were modeled, including a reference structure with no heat spreaders, And two modified structures involving one-per-device and three-per-device FLG heat spreaders were analyzed. The later steps included to run a steady-state thermal analysis for each structure at different operating power levels simulating continuous wave (CW) operating conditions. Figure 7.4 shows the top view of the 3D model of the reference structure.

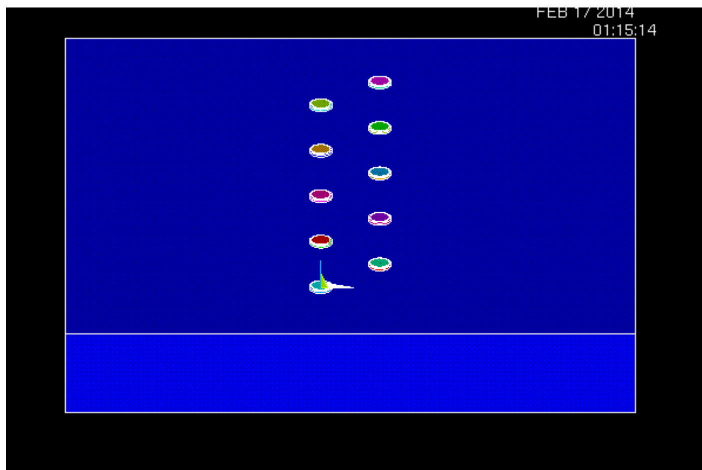


Figure 7.4: 3D model of reference structure involving 10 InGaN/GaN micro- LED arrays on sapphire with no heat spreaders attached.

In the one-per-device structure, Graphene heat spreaders were introduced to each structure as thin (~50 nm) FLG sheets. Al metallization strip about 500 µm long was deposited in between the two devices rows. With a thickness similar to that of the device's FLG sheets were suspended between top surface of the devices and the Al metallization. The contact area between heat spreaders and device was about 2 µm and the length of FLG quilts ~ 10 µm. Figure 7.5 below shows the 3D model of the one-per-device heat spreader structure.

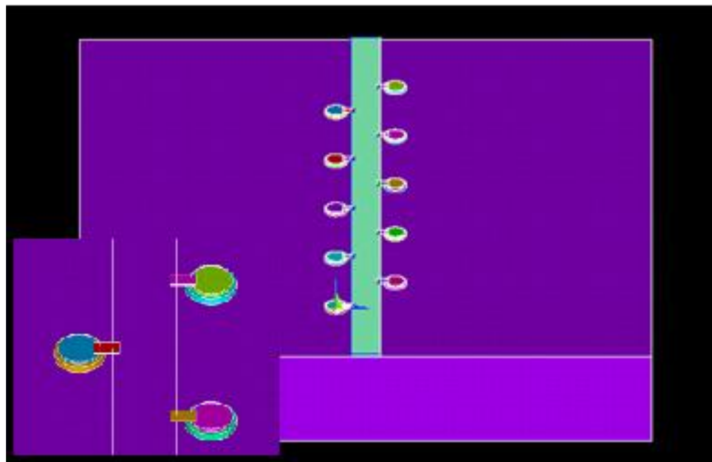


Figure 7.5: A 3D model of the single heat spreader micro LED array structure. Inset: a zoomed in view of the array elements attached to metallic strip by Graphene quilts

For further investigation of the impact of FLG heat spreaders on the device temperatures, the third structure was modeled with an increased number of heat spreaders attached to each array element. This configuration needed the metallic strip to be extended and branched into the spaces between each consecutive device of each row; this would allow the attachment of multiple heat spreaders to each device (up to 3). Figure 7.6 illustrates the 3D model of the 'multi-heat spreaders' micro-LED structure. All structures were 'meshed with special attention to FLG/LED contact regions' to ensure accurate low-errors results. Similar thermal loads were then applied to each structure including power levels and initial and ambient temperatures. Power values of 2, 3, 4, and 5 mW were used in the simulation while ambient the temperature was set to 20 ^{o}C at all times. In

these simulations thermal convection was neglected on the device and heat spreaders surfaces due to their small areas.

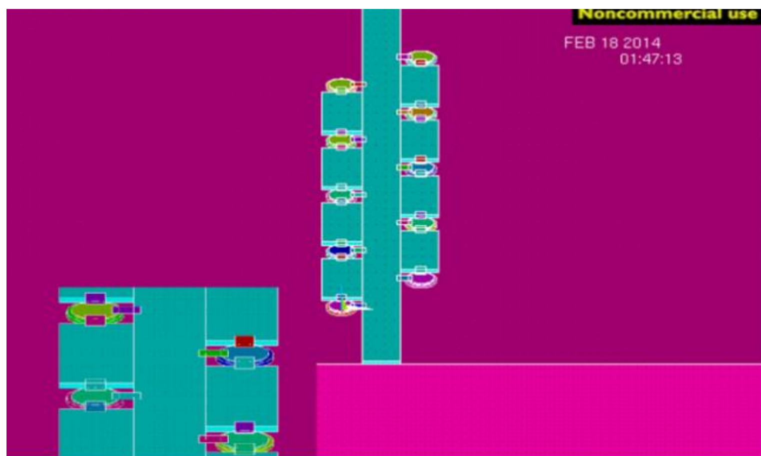


Figure 7.6: 3D model of the multi-heat spreader micro-LED array structure. Inset: a zoomed in view of the array elements attached to metallic strip by multiple Graphene quilts.

7.5 Results and Comparative Study

In this research multiple steady-state thermal analysis were carried out for the reference structure along with two modified structures arrays with FLG quilts. Reference structure modeling resulted in a maximum device local temperature of 212 ^{o}C at operating power of 5 mW. This relatively high temperature is caused by the small

dimensions of the micro-LED and the sapphire substrate. Figure 7.7 shows temperature distribution in reference structure at 5 mw operating power.

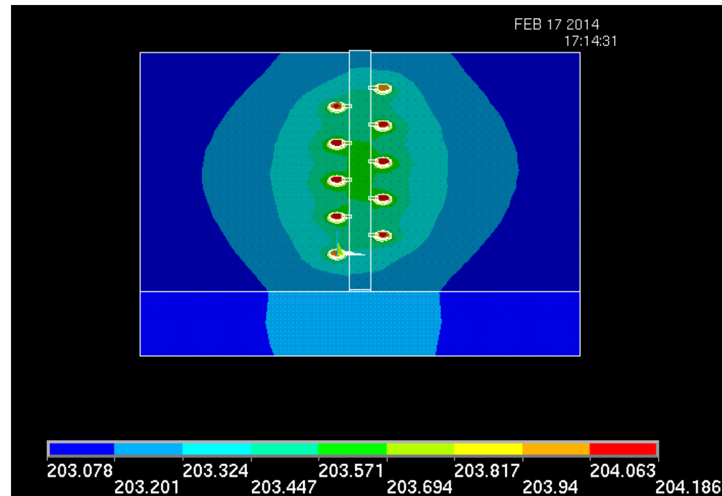


Figure 7.7: Temperature distribution in reference structure at 5 mw operating power

Same power level for one-per-device heat spreader structure resulted in device temperature of 204 ^{o}C. This 8 ^{o}C temperature drop is an indicator of a better heat dissipation in the structure. The inclusion of heat spreaders increased heat flow from the top surfaces of the devices to the Al strip and then to the substrate. Low thermal resistance offered by FLG heat spreaders lowers the total thermal resistance of the l structure thus decreases device temperature. Figure 7.8 presents a zoomed view of temperature distribution in ‘one-per-device heat spreader structure’ at 5 mw operating power.

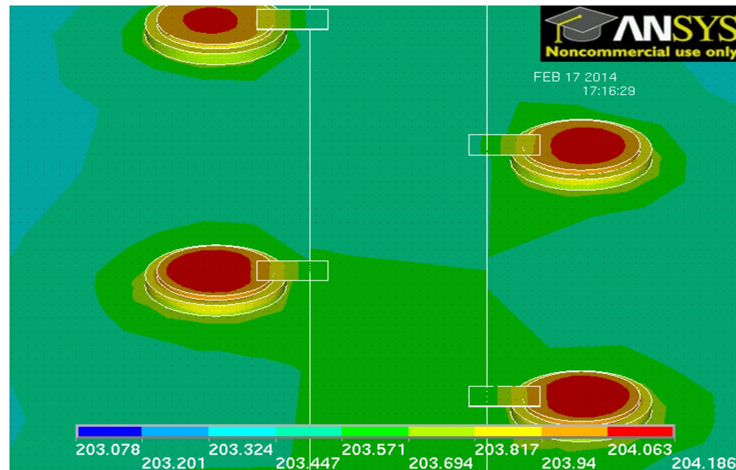


Figure 7.8: A zoomed view of temperature distribution in one-per-device heat spreader structure at 5 mw operating power

Three-per-device heat spreaders structure was also simulated at the same power level and device temperature was evaluated to 197 ^{o}C in contrast to 208 ^{o}C. This further reduction in the device temperature shows consistency and comes in agreement with our TRC predictions. Figure 7.9 illustrates temperature distribution in the ‘three-per-device heat spreaders modified structure.

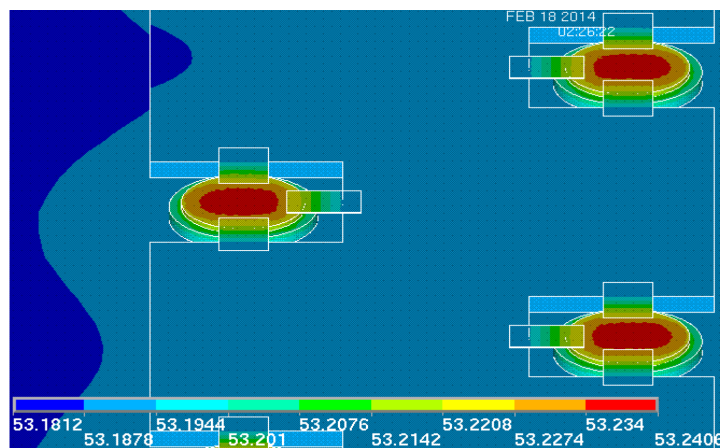


Figure 7.9: A zoomed view of 3D vector plot of heat flux in multiple heat spreader structure at 2 mw operating power

A thermal flux study illustrates the advantages of the heat spreaders. Thermal flux is relatively high in the heat spreaders; however, the total flux through the vertical direction into the substrate is larger. This is due to the large contact area with the device. Similar simulations were also carried out for the three structures at several operating power levels. Results were employed in comparative study to evaluate the performance of heat spreaders. Combined results are illustrated in figure 7.10.

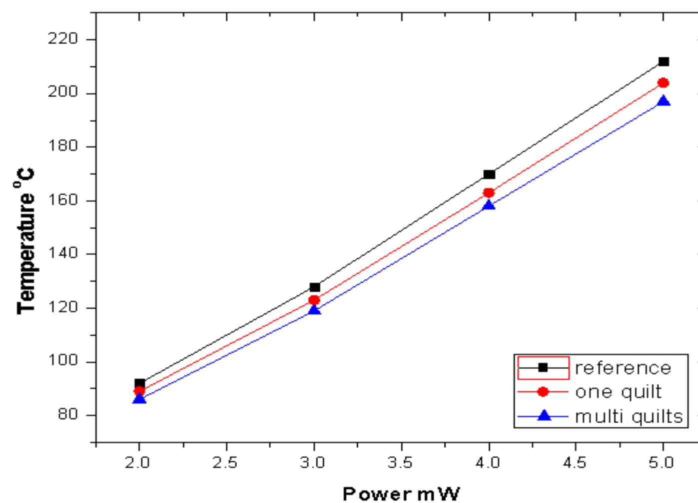


Figure 7.10: Simulated device temperature behavior as a function of operating power for reference, single, and multi heat spreaders (quilts) micro LED structures

A closer look at the results clearly shows that ‘multi-heat spreaders structure’ offers more reduction in the device temperature at all power levels used. This simply occurs as the multiple heat spreaders introduce multiple additional thermal paths and increase heat flux away from the device of the device and reduce the package thermal resistance leading to lower device temperature. Results are consistent at all operating

power values and confirm that the introduction of hear spreaders helped decrease the devices temperature.

7.6 Summary

This chapter we presented an introductory study of the incorporation of novel FLG heat spreaders into micro-LED arrays used in optical communication applications. Few layered Graphene (FLG) quilts were introduced to the array package as heat spreaders. Structural modifications have been developed and included in the reference array structure to ease the implementation of the heat spreaders to the reference structure. In this study, reference, one-per-device and three-per-device heat spreaders structures were designed and simulated. 3D models of the three structures were designed using ANSYS13^{TM} and steady-state thermal analysis was carried out. Various power levels were simulated for each structure and device temperatures were evaluated. Device temperature results for all the structures were used in a comparative study clearly evaluate the impact of heat spreaders on the overall device temperature. Results are consistent and in good agreement with our TRC predictions. One-per-device heat spreaders structure showed 8 ^{o}C reduction in the device temperature from that of the reference structure, while three-per-device structure exhibited 15 ^{o}C decrease from the reference structure device temperature. The outcomes presented in this work give excellent proof of the high potential of FLG heat spreaders for thermal management of solid-state light emitters. This study leads the way to further development and enhancement in Graphene heat spreaders technology. It is expected that more advances in the fabrication, production and dimensions of FLG quilts is going to lead to more

efficient heat spreaders opens the door for further improvement in SSL light modules thermal management.

CHAPTER 8: CONCLUSION AND FUTURE WORK

This chapter concludes the work presented in this dissertation. It also identifies and proposes the future work based on the research milestone and achievements. Each section of the chapter will summarize a stage in our research progression. The final section reciprocates our future research intentions−a logical progression. In our search for more efficient and thermally stable III-Nitride solid-state light emitters packaging, we developed and conducted a systematic investigation of LED/LD packaging. Starting from the basic on-wafer die attach techniques and materials, our work expanded to cover submounts and packaging material combinations selection. COP packaging method was considered along with numerical study of heatsink. Thermal analysis of multiple light modules was also carried out. Our research followed closely newly developed packaging techniques such as COP, and materials (CNT, FLG), work was carried out to further explore their potential and advantages consistent with underlying physics and optics principles. The last stage of this research was to introduce both a new concepts and materials into the packaging process of photonic devices, and we believe that our findings will offer a significant contribution to this new technology as applied to modern photonic devices and components.

8.1 Thermal Analysis of InGaN/GaN Laser Diodes

Transient thermal analysis of InGaN/GaN LD was carried out. Two die attached

techniques were considered to show the optimum design for effective thermal management. Planar and ball solder bumps structure were modeled and different submount materials were attached to the device to compare their heat dissipation capabilities. Results showed that planar solder bumps structures achieved better heat dissipation and kept the whole structure at lower temperature. This is attributed to larger contact area and the uniformity of heat dissipation from the LD die to the submount. On the other hand, out of the three submount material considered in this study, SiC was found to be the most suitable submount material.

8.2 On-chip Thermal Analysis of AlGaN/GaN LD and Packaging Material Selection.

This part of the research AlGaN/GaN LD device packaging was suggested and presented with wide variety of packaging materials for TIM, submount, and heatsinks. It also included newly discovered Carbon Nano Tubes CNT. The aim of this study was to evaluate the thermal performance of the package using different material combinations and conduct a comparative study to determine the best packaging options. The results of this study showed that CNT have high potential as TIM materials, diamond was the best choice of submount, and Cu was the best performing heatsink material. The results of this study were considered in all the steps that followed especially when dealing with complete packages.

8.3 Chip-On-Plate Packaging and Heatsink Design

This strategy was of high importance in this research and development work. A newly developed COP packaging method was considered along with theoretical study of heatsinks. Several COP structures were modeled and attached to different heatsink designs to evaluate their thermal performance. Based on performance, not only the most

effective heatsink designs but the most cost-efficient technique was also identified. Modeling results were corroborated by thermal resistance circuit (TRC) calculations to increase the accuracy and consistencies of the obtained results. Established results showed that densely finned and pin-fin heatsinks provided better heat dissipation and ensure lower device temperature than plate pin-fin heatsinks, however, it was not a cost-efficient strategy. This approach can be used as a strategy for testing new heatsink designs and find the optimum design that can combine best performance and low-cost.

8.4 Thermal Analysis of LED Assemblies

In this study, we tried to generalize our findings from individual devices packaging to multi-device assemblies. This step was of great importance, considering that our work is directed towards SSL applications. Previously studied COP packaged LEDs were arranged in various assemblies and geometric arrangements and attached those to one common heatsink, this was essential to study the collective thermal behavior of the devices and also to evaluate mutual effects among the devices. Findings showed that radial devices arrangements resulted in temperature contrast between assembly elements. These differences if increased can lead to output and lifetime differences. The reasons for such difference and contrast were studied and explained qualitatively using TRC model and heat diffusion equation. A modified uniform distribution geometrical structure was proposed and modeled. Comparative study of the results showed that the new design achieved a desired decrease in the thermal contrast as high as one order of magnitude. The results represented, will be highly useful for the designing and manufacturing of SSL light modules and large scale assemblies.

8.5 Graphene Heat Spreaders for Micro-LED Arrays

At this point of research, we introduced the concept FLG horizontal heat spreaders into photonic devices packaging. Newly discovered Graphene quilts were used in this study due to their high thermal conductivity. After a proof of concept modeling of a wide area LED device, we found that FLG heat spreaders will be most effective with micro-LED arrays due to their size limitations. A 10 micro-LED array for optical communications applications was modeled and modified with Graphene heat spreaders. Steady-state thermal analysis was carried out to investigate the effect of the new heat spreaders on device temperature. A 15 ^{o}C temperature drop in the devices temperature in comparison to the reference structure was estimated with our modified multi-heat spreader structure. Results showed the potential of 2D Carbon structures in the packaging of photonics devices.

8.6 Future Work and Research Intentions

The future work of this dissertation will be based on the goals and achievements of this study. As discussed in chapter 7, 2D Carbon materials is a promising material system for the advanced thermal management of solid-state light emitters. The research objective will be to further explore the potential of such materials and novel packaging designs and assemblies. A close collaboration with other research groups in this field, especially manufacturing and consumer industry to develop efficient yet thermally highly stable sources could ease the transition to solid-state lighting and other wavelength sensitive applications.

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IN REVIEW

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[7] Kudsieh N, Khizar M, and Raja M Y A," Novel Graphene heat spreaders for the thermal management of micro-LED arrays for optical communications" submitted for High-capacity Optical Networks & Enabling Technologies (HONET) (2014)

APPENDIX A: TIM MODELING DATA

Temperature distribution data of AlGaN/GaN LD package at 100 ^{o}C.

Table 4.2: temperature profiles along junction-to-heatsink thermal path for AuSn as TIM

Distance (µm)	Heatsink temperature ^{o}C					
Y	AuSn , SiC , Cu	AuSn, SiC,Al	AuSn, AlN,Cu	AuSn, Aln,Al	AuSn, C, Cu	AuSn ,C,Al
0	200	100	100	100	100	100
3.4133	69.926	35.6615	36.4135	35.028	31.6255	30.423
6.8267	67.896	34.3945	35.1615	33.128	31.2405	30.031
10.24	65.867	33.128	33.9095	31.2275	30.8555	29.6395
13.653	63.837	31.861	32.6575	30.346	30.4705	29.2475
17.067	61.971	30.6965	31.507	29.82	30.1165	28.8875
20.48	61.41	30.346	31.1605	29.294	30.0105	28.7795
23.893	60.85	29.995	30.814	28.96	29.905	28.6715
27.307	60.289	29.6445	30.468	28.6355	29.799	28.5635
30.72	59.728	29.294	30.1215	28.3285	29.693	28.4555
34.133	59.367	29.068	29.898	28.1125	29.6255	28.3865
37.547	59.023	28.8515	29.6845	27.8965	29.561	28.3205
40.96	58.678	28.6355	29.471	27.705	29.496	28.2545
44.373	58.333	28.4195	29.2575	27.5545	29.4315	28.1885
47.787	58.075	28.2565	29.097	27.4045	29.3835	28.1395
51.2	57.846	28.1125	28.9545	27.2825	29.3415	28.096
54.613	57.618	27.9685	28.8125	27.181	29.299	28.053
58.027	57.389	27.8245	28.67	27.0795	29.257	28.0095
61.44	57.2	27.705	28.552	27.0095	29.2225	27.974
64.853	57.042	27.6045	28.453	26.948	29.194	27.945
68.267	56.884	27.5045	28.354	26.887	29.1655	27.9155
71.68	56.726	27.4045	28.255	27.4045	29.137	27.8865
75.093	56.588	27.3165	28.1675	27.2825	29.1125	27.861
78.507	56.482	27.2485	28.1	27.181	29.094	27.842
81.92	56.376	27.181	28.0325	27.0795	29.076	27.8235
85.333	56.27	27.113	27.9645	27.0095	29.058	27.8045
88.747	56.172	27.0505	27.902	26.948	29.0415	27.7875
92.16	56.108	27.0095	27.86	26.887	29.032	27.7775
95.573	56.045	26.9685	27.818	27.0095	29.0225	27.768
98.987	55.982	26.9275	27.7765	26.948	29.013	27.758
102.4	55.919	26.887	27.7345	26.887	29.0035	27.748

Table 4.3: temperature profiles along junction-to-heatsink thermal path for CNT as TIM

Distance (µm)	Heatsink temperature ^oC					
Y	CNT, AlN,Cu	CNT, AlN,Al	CNT, SiC,Cu	CNT, SiC,Al	CNT, C,Al	CNT, C,Cu
0	200	100	100	100	100	100
3.4133	167.08	82.625	81.91	80.925	79.955	84.87
6.8267	161.68	79.77	79.535	78.425	78.985	84.14
10.24	156.28	76.92	77.165	75.92	78.015	83.405
13.653	150.87	74.07	74.79	73.42	77.045	82.675
17.067	145.91	71.45	72.61	71.115	76.15	82
20.48	144.4	70.655	71.95	70.425	75.885	81.8
23.893	142.9	69.86	71.29	69.73	75.62	81.595
27.307	141.4	69.07	70.63	69.035	75.35	81.395
30.72	139.89	68.275	69.975	68.34	75.085	81.195
34.133	138.92	67.76	69.545	67.89	74.915	81.065
37.547	137.98	67.27	69.14	67.46	74.75	80.94
40.96	137.05	66.775	68.735	67.035	74.59	80.815
44.373	136.12	66.285	68.325	66.605	74.425	80.695
47.787	135.41	65.915	68.02	66.28	74.305	80.6
51.2	134.79	65.585	67.75	65.995	74.2	80.52
54.613	134.16	65.255	67.48	65.71	74.095	80.44
58.027	133.54	64.925	67.21	65.425	73.99	80.36
61.44	133.01	64.65	66.985	65.19	73.905	80.29
64.853	132.58	64.42	66.8	64.995	73.835	80.235
68.267	132.14	64.19	66.61	64.8	73.765	80.185
71.68	131.7	63.96	66.425	64.6	73.695	80.13
75.093	131.31	63.76	66.26	64.43	73.635	80.08
78.507	131.01	63.605	66.135	64.3	73.59	80.045
81.92	130.71	63.445	66.01	64.17	73.545	80.01
85.333	130.41	63.29	65.885	64.04	73.505	79.975
88.747	130.13	63.145	65.77	63.92	73.465	79.945
92.16	129.94	63.055	65.695	63.845	73.445	79.925
95.573	129.76	62.96	65.62	63.77	73.425	79.91
98.987	129.57	62.865	65.545	63.695	73.405	79.89
102.4	129.38	62.77	65.47	63.62	73.38	79.875

Table 4.4: temperature profiles along junction-to-heatsink thermal path for AgSn as TIM

Distance (μm)	Heatsink temperature °C					
Y	AgSn,AlN, Al	AgSn,AlN, Cu	AgSn, SiC,Al	AgSn,SiC, Cu	AgSn, C,Al	AgSn, C,Cu
0	200	100	100	100	100	100
3.4133	55.277	27.878	25.9465	26.3795	25.2435	25.952
6.8267	54.236	27.358	25.523	25.9595	25.089	25.799
10.24	53.195	26.838	25.0995	25.5395	24.934	25.646
13.653	52.153	26.3175	24.676	25.119	24.7795	25.4935
17.067	51.182	25.8325	24.281	24.7275	24.635	25.3505
20.48	50.661	25.5715	24.069	24.5175	24.5575	25.274
23.893	50.14	25.311	23.8565	24.3075	24.4795	25.1975
27.307	49.619	25.05	23.6445	24.0975	24.402	25.121
30.72	49.099	24.7895	23.4325	23.888	24.324	25.0445
34.133	48.751	24.615	23.2905	23.748	24.272	24.993
37.547	48.413	24.4455	23.153	23.6125	24.2215	24.9435
40.96	48.076	24.2765	23.0155	23.477	24.171	24.894
44.373	47.74	24.1075	22.878	23.3415	24.1205	24.8445
47.787	47.478	23.976	22.771	23.2365	24.081	24.806
51.2	47.241	23.8565	22.6745	23.1415	24.0455	24.771
54.613	46.999	23.735	22.5755	23.0445	24.009	24.7355
58.027	46.758	23.6135	22.4775	22.9485	23.973	24.7005
61.44	46.555	23.511	22.394	22.867	23.942	24.6705
64.853	46.379	23.4225	22.3225	22.797	23.9155	24.6445
68.267	46.205	23.334	22.251	22.7275	23.889	24.619
71.68	46.031	23.2465	22.18	22.6585	23.863	24.594
75.093	45.876	23.168	22.1165	22.597	23.8395	24.571
78.507	45.75	23.104	22.065	22.547	23.8205	24.5525
81.92	45.625	23.04	22.014	22.497	23.801	24.5345
85.333	45.5	22.9765	21.9625	22.448	23.7825	24.516
88.747	45.383	22.917	21.915	22.4015	23.7645	24.499
92.16	45.296	22.8725	21.8795	22.3675	23.7515	24.487
95.573	45.21	22.8285	21.844	22.334	23.738	24.4745
98.987	45.124	22.7845	21.809	22.3	23.725	24.462
102.4	45.038	22.5	21.774	22.2665	23.712	24.4495

Table 4.5: temperature profiles along heatsink lateral thermal path for AuSn as TIM

Distance (µm)	Heatsink temperature ^{o}C					
X	AuSn , SiC , Cu	AuSn SiC Al	AuSn ,AlN Cu	AuSn, Aln Al	AuSn, C, Cu	AuSn, C, Al
0	28.3	27.125	28.194	24.0155	28.9225	27.3825
10.189	28.3185	27.155	28.2135	24.0415	28.9385	27.4085
20.379	28.354	27.2115	28.2505	24.09	28.967	27.4575
30.568	28.4115	27.305	28.311	24.169	29.0145	27.537
40.757	28.4995	27.447	28.404	24.288	29.085	27.6555
50.947	28.611	27.6275	28.5215	24.435	29.1765	27.811
61.136	28.7725	27.8905	28.6895	24.6385	29.3145	28.0465
71.325	28.882	28.0605	28.8105	24.7645	29.3845	28.155
81.515	28.964	28.1825	28.905	24.852	29.422	28.202
91.704	29.0135	28.254	28.9645	24.91	29.443	28.2265
101.89	29.055	28.3135	29.014	24.963	29.46	28.2465
112.08	29.089	28.361	29.054	25.011	29.474	28.2625
122.27	29.105	28.3845	29.0735	25.0475	29.4805	28.2705
132.46	29.1125	28.396	29.0825	25.078	29.4835	28.2745
142.65	29.107	28.3895	29.0765	25.0975	29.481	28.272
152.84	29.0845	28.36	29.05	25.102	29.471	28.261
163.03	29.0515	28.3165	29.012	25.0975	29.4565	28.2455
173.22	29.004	28.2535	28.9565	25.078	29.4355	28.223
183.41	28.9485	28.1785	28.8915	25.0475	29.4115	28.197
193.6	28.8875	28.0965	28.82	25.011	29.385	28.168
203.79	28.8195	28.003	28.7395	24.963	29.3565	28.136
213.98	28.7495	27.9065	28.657	24.91	29.3275	28.103
224.17	28.678	27.805	28.572	24.852	29.2975	28.069
234.35	28.5865	27.67	28.466	24.7645	29.256	28.0175
244.54	28.472	27.4915	28.3385	24.6385	29.184	27.9065
254.73	28.311	27.2275	28.1705	24.435	29.047	27.6715
264.92	28.1975	27.0435	28.051	24.288	28.955	27.516
275.11	28.107	26.897	27.9545	24.169	28.884	27.396
285.3	28.0465	26.799	27.8905	24.09	28.8365	27.3155
295.49	28.009	26.738	27.85	24.0415	28.807	27.266
305.68	27.987	26.703	27.827	24.0155	28.7905	27.239

Table 4.6: temperature profiles along heatsink lateral thermal path for CNTas TIM

Distance (µm)	Heatsink temperature °C					
X	CNT,AlN, Cu	CNT, AlN, Al	CNT, SiC, Cu	CNT,SiC, Al	CNT, C, Al	CNT, C, Cu
0	65.865	63.63	66.515	64.32	73.15	79.77
10.189	65.905	63.695	66.555	64.385	73.195	79.8
20.379	65.99	63.82	66.635	64.505	73.28	79.855
30.568	66.12	64.025	66.765	64.71	73.41	79.94
40.757	66.32	64.34	66.96	65.015	73.61	80.075
50.947	66.575	64.735	67.205	65.405	73.87	80.245
61.136	66.94	65.315	67.565	65.975	74.26	80.5
71.325	67.2	65.685	67.805	66.32	74.44	80.63
81.515	67.405	65.95	67.985	66.55	74.52	80.7
91.704	67.53	66.11	68.095	66.685	74.565	80.74
101.89	67.635	66.235	68.19	66.795	74.6	80.77
112.08	67.72	66.34	68.26	66.88	74.63	80.795
122.27	67.76	66.39	68.295	66.92	74.645	80.81
132.46	67.78	66.41	68.31	66.94	74.65	80.815
142.65	67.765	66.395	68.295	66.925	74.64	80.81
152.84	67.71	66.33	68.245	66.86	74.615	80.79
163.03	67.63	66.23	68.165	66.775	74.58	80.765
173.22	67.51	66.09	68.055	66.645	74.525	80.725
183.41	67.37	65.925	67.93	66.495	74.465	80.68
193.6	67.215	65.745	67.79	66.335	74.4	80.63
203.79	67.045	65.54	67.635	66.155	74.335	80.575
213.98	66.865	65.32	67.48	65.965	74.265	80.52
224.17	66.68	65.095	67.315	65.77	74.195	80.465
234.35	66.45	64.795	67.11	65.51	74.105	80.39
244.54	66.175	64.4	66.855	65.14	73.92	80.255
254.73	65.805	63.81	66.49	64.56	73.525	79.995
264.92	65.54	63.4	66.235	64.155	73.265	79.825
275.11	65.33	63.07	66.035	63.835	73.065	79.69
285.3	65.19	62.85	65.895	63.62	72.93	79.6
295.49	65.1	62.71	65.81	63.49	72.845	79.545
305.68	65.05	62.63	65.76	63.41	72.8	79.515

Table 4.7: temperature profiles along heatsink lateral thermal path for AgSn as TIM

Distance (µm)	Heatsink temperature ^{o}C					
X	AgSn, AlN, Al	AgSn, AlN, Cu	AgSn, SiC, Al	AgSn, SiC, Cu	AgSn, C, Al	AgSn, C, Cu
0	23.647	24.0155	22.817	23.4425	23.7985	24.7495
10.133	23.6735	24.0415	22.84	23.4575	23.8195	24.762
20.267	23.7225	24.09	22.8835	23.4855	23.859	24.785
30.4	23.8025	24.169	22.955	23.5315	23.924	24.8225
40.533	23.923	24.288	23.0615	23.601	24.02	24.8785
50.667	24.0715	24.435	23.194	23.6865	24.141	24.9485
60.8	24.2775	24.6385	23.378	23.8045	24.313	25.048
70.933	24.4055	24.7645	23.4855	23.882	24.389	25.0965
81.067	24.4935	24.852	23.5545	23.9385	24.4185	25.1205
91.2	24.552	24.91	23.6	23.979	24.4365	25.136
101.33	24.6055	24.963	23.6415	24.0165	24.4525	25.1505
111.47	24.654	25.011	23.68	24.051	24.4675	25.164
121.6	24.691	25.0475	23.7095	24.078	24.479	25.175
131.73	24.7215	25.078	23.734	24.1005	24.489	25.184
141.87	24.7415	25.0975	23.7505	24.115	24.4955	25.19
152	24.7455	25.102	23.754	24.1185	24.497	25.1915
162.13	24.7415	25.0975	23.7505	24.115	24.4955	25.19
172.27	24.7215	25.078	23.734	24.1005	24.489	25.184
182.4	24.691	25.0475	23.7095	24.078	24.479	25.175
192.53	24.654	25.011	23.68	24.051	24.4675	25.164
202.67	24.6055	24.963	23.6415	24.0165	24.4525	25.1505
212.8	24.552	24.91	23.6	23.979	24.4365	25.136
222.93	24.4935	24.852	23.5545	23.9385	24.4185	25.1205
233.07	24.4055	24.7645	23.4855	23.882	24.389	25.0965
243.2	24.2775	24.6385	23.378	23.8045	24.313	25.048
253.33	24.0715	24.435	23.194	23.6865	24.141	24.9485
263.47	23.923	24.288	23.0615	23.601	24.02	24.8785
273.6	23.8025	24.169	22.955	23.5315	23.924	24.8225
283.73	23.7225	24.1	22.8835	23.4855	23.859	24.785
293.87	23.6735	24.08	22.84	23.4575	23.8195	24.762
304	23.647	24	22.817	23.4425	23.7985	24.7495

Table 4.8: temperature profiles along heatsink vertical thermal path for AuSn as TIM

Distance (µm)	Heatsink temperature ^{o}C					
Z	AuSn , SiC , Cu	AuSn, SiC, Al	AuSn AlN Cu	AuSn, Aln Al	AuSn C Cu	AuSn, C, Al
0	21.0825	19.1635	20.1595	17.6755	25	22.4125
36.8	21.1855	19.368	20.2565	17.8575	25.1205	22.645
73.6	21.4855	19.967	20.5395	18.391	25.474	23.3255
110.4	22.018	21.008	21.0365	19.3485	26.115	24.566
147.2	22.397	21.485	21.442	19.935	26.3485	24.898
184	22.855	21.9905	21.9645	20.551	26.5615	25.1425
220.8	23.4835	22.695	22.684	21.3655	26.8485	25.458
257.6	24.278	23.5895	23.5945	22.384	27.2115	25.852
294.4	25.188	24.6025	24.636	23.5425	27.6285	26.3015
331.2	26.119	25.6185	25.6995	24.721	28.057	26.761
368	26.982	26.539	26.684	25.805	28.4555	27.1875
404.8	27.7125	27.301	27.515	26.7145	28.7955	27.5495
441.6	28.295	27.893	28.176	27.433	29.0695	27.841
478.4	28.725	28.313	28.66	27.956	29.2755	28.0595
515.2	28.995	28.553	28.9615	28.2775	29.41	28.2005
552	29.1095	28.6185	29.084	28.4035	29.4745	28.2665
588.8	29.0715	28.513	29.033	28.339	29.4695	28.2585
625.6	28.8795	28.2335	28.805	28.0815	29.395	28.175
662.4	28.5305	27.776	28.3975	27.626	29.249	28.0155
699.2	28.0325	27.149	27.8195	26.9815	29.035	27.7825
736	27.392	26.361	27.0775	26.153	28.7565	27.4795
772.8	26.626	25.437	26.1915	25.1595	28.4195	27.113
809.6	25.798	24.461	25.2345	24.0815	28.053	26.7135
846.4	24.997	23.542	24.3085	23.0325	27.698	26.3235
883.2	24.3135	22.7805	23.5185	22.1265	27.3945	25.986
920	23.7825	22.21	22.907	21.401	27.156	25.711
956.8	23.324	21.689	22.4015	20.706	26.913	25.392
993.6	22.5685	20.313	21.6805	19.3665	26.067	23.7805
1030.4	22.0515	19.3345	21.186	18.46	25.488	22.674
1067.2	21.7455	18.759	20.8925	17.9275	25.1465	22.021
1104	21.641	18.5625	20.792	17.746	25.03	21.7985

Table 4.9: temperature profiles along heatsink vertical thermal path for CNT as TIM

Distance (µm)	Heatsink temperature °C					
Z	CNT, AlN, Cu	CNT, AlN, Al	CNT,SiC,Cu	CNT, SiC, Al	CNT, C, Al	CNT, C, Cu
0	45.024	37.36	46.84	39.518	60.625	70.79
36.8	45.2935	37.907	47.1165	40.0885	61.09	71.085
73.6	46.0785	39.508	47.923	41.757	62.44	71.94
110.4	47.4495	42.357	49.3405	44.7375	64.865	73.47
147.2	48.5555	44.0725	50.365	46.32	65.56	74.02
184	49.9525	45.823	51.64	47.8965	66.175	74.505
220.8	51.855	48.097	53.39	49.9645	67.02	75.145
257.6	54.225	50.89	55.59	52.525	68.095	75.95
294.4	56.9	54.015	58.075	55.395	69.32	76.86
331.2	59.58	57.13	60.58	58.27	70.57	77.785
368	62.015	59.935	62.86	60.865	71.72	78.635
404.8	64.035	62.24	64.75	63.005	72.685	79.355
441.6	65.615	64.03	66.24	64.675	73.465	79.93
478.4	66.765	65.32	67.325	65.885	74.045	80.365
515.2	67.475	66.105	68.005	66.63	74.425	80.65
552	67.775	66.42	68.295	66.935	74.615	80.79
588.8	67.675	66.28	68.21	66.82	74.615	80.79
625.6	67.16	65.67	67.75	66.27	74.425	80.65
662.4	66.23	64.575	66.89	65.27	74.04	80.365
699.2	64.89	63.005	65.655	63.835	73.465	79.935
736	63.14	60.95	64.04	61.955	72.71	79.375
772.8	61.01	58.435	62.07	59.655	71.78	78.68
809.6	58.665	55.645	59.91	57.115	70.76	77.92
846.4	56.355	52.87	57.79	54.6	69.76	77.175
883.2	54.35	50.43	55.96	52.395	68.905	76.525
920	52.775	48.422	54.535	50.605	68.24	76
956.8	51.435	46.4295	53.315	48.808	67.57	75.445
993.6	49.4855	42.4865	51.33	44.722	64.385	73.455
1030.4	48.1395	39.782	49.9555	41.912	62.165	72.07
1067.2	47.338	38.181	49.1385	40.2465	60.835	71.245
1104	47.063	37.633	48.8585	39.6765	60.375	70.96

Table 4.10: temperature profiles along heatsink vertical thermal path for AuSn as TIM

Distance (µm)	Heatsink temperature ^{o}C					
Z (µm)	AgSn, AlN, Al	AgSn, AlN, Cu	AgSn, SiC, Al	AgSn, SiC, Cu	AgSn, C, Al	AgSn, C, Cu
0	17.0395	16.8885	16.6885	18.1855	20.36	22.0675
36.8	17.1845	17.0485	16.8405	18.2635	20.5505	22.1645
73.6	17.611	17.517	17.2855	18.49	21.1055	22.4485
110.4	18.356	18.331	18.059	18.8805	22.069	22.9415
147.2	18.7505	18.757	18.414	19.1335	22.2815	23.0915
184	19.181	19.215	18.791	19.4695	22.4405	23.235
220.8	19.779	19.8475	19.318	19.954	22.658	23.4375
257.6	20.538	20.6465	19.988	20.576	22.9325	23.697
294.4	21.3975	21.5495	20.747	21.2845	23.244	23.9925
331.2	22.257	22.454	21.5095	21.9985	23.557	24.291
368	23.0335	23.274	22.202	22.6495	23.8425	24.5635
404.8	23.6715	23.952	22.7755	23.19	24.0805	24.791
441.6	24.165	24.478	23.222	23.6125	24.2675	24.9705
478.4	24.512	24.85	23.538	23.9125	24.402	25.0995
515.2	24.7085	25.062	23.7195	24.085	24.481	25.176
552	24.76	25.118	23.7685	24.1335	24.506	25.2005
588.8	24.6695	25.021	23.689	24.0595	24.4775	25.1745
625.6	24.4335	24.769	23.4775	23.862	24.3955	25.097
662.4	24.048	24.358	23.1325	23.538	24.258	24.967
699.2	23.518	23.795	22.6595	23.095	24.0685	24.7875
736	22.8495	23.0885	22.066	22.5395	23.8295	24.561
772.8	22.0625	22.2605	21.371	21.891	23.5495	24.296
809.6	21.2295	21.386	20.6385	21.21	23.2535	24.0165
846.4	20.4435	20.5605	19.949	20.5725	22.974	23.754
883.2	19.7925	19.8745	19.379	20.0505	22.741	23.5385
920	19.3035	19.3555	18.9525	19.671	22.563	23.379
956.8	18.8645	18.88	18.5645	19.3755	22.3705	23.2285
993.6	17.883	17.7995	17.543	18.8385	21.136	22.5865
1030.4	17.1945	17.0355	16.8175	18.4565	20.237	22.122
1067.2	16.792	16.587	16.391	18.2305	19.706	21.848
1104	16.6555	16.434	16.2455	18.1535	19.5245	21.7545